**PUBLIC**

**UNITED STATES OF AMERICA**

**BEFORE THE FEDERAL TRADE COMMISSION**

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| **In the Matter of**<br>**RAMBUS INC.,**<br>**a corporation.** | **Docket No. 9302** |

**RESPONDENT RAMBUS INC.'S RESPONSES TO**

**COMPLAINT COUNSEL'S FIRST REQUEST FOR ADMISSIONS**

Pursuant to section 3.32 of the Federal Trade Commission's Rules of Practice, Respondent Rambus Inc. ("Rambus") hereby responds to the first set of interrogatories propounded by Complainant, served on December 30, 2002.

**GENERAL OBJECTIONS**

1. Rambus objects to Complainant's requests to the extent that they call for information protected from discovery by the attorney-client privilege, the work product doctrine, or any other applicable privilege.

2. Rambus objects to Complainant's requests to the extent that they seek confidential commercial information or trade secrets, such as business plans, financial results and projections, technical data, and revenue information.

3. Rambus objects to Complainant's definitions 1, 2, 4, 5 and 6 as vague, ambiguous and overly broad.

4. Rambus objects to Complainant's requests to the extent that they seek information previously provided to Complainant or available to it from public sources.

5. Rambus objects to Complainant's requests to the extent that they seek information protected from discovery pursuant to sections 3.31(c)(3)-(4).

6. Rambus reserves all of its evidentiary objections or other objections to the introduction or use of any response at any hearing in this action.

7. Rambus objects to Complainant's requests regarding the scope of Rambus's patents and patent applications as calling for a legal conclusion.

8. Rambus objects to Complainant's requests regarding the beliefs of Rambus's directors, officers or employees as to the scope, or potential scope, of Rambus's patents and patent applications as irrelevant to any issue raised by this matter. *See Rambus Inc. v. Infineon Technologies AG*, -- F.3d --, 2003 WL 187265, at *19 (Fed. Cir. Jan. 29, 2003) ("The JEDEC policy, though vague, does not create a duty premised on subjective beliefs. JEDEC's disclosure duty erects an objective standard. It does not depend on a member's subjective belief that its patents do or do not read on the proposed standard.").

9. Rambus objects to Complainant's requests regarding JEDEC presentations purportedly relating to features ultimately incorporated into the DDR SDRAM standards and regarding a survey ballot circulated by the JEDEC 42.3 Subcommittee between October and December, 1995, as irrelevant to any issue raised by this matter. *See Rambus Inc. v. Infineon Technologies AG*, -- F.3d --, 2003 WL 187265, at *20 (Fed. Cir. Jan. 29, 2003) ("[T]he disclosure duty, as defined by the EIA/JEDEC policy, did not arise before legitimate proposals were directed to and formal consideration began on the DDR-SDRAM standard.").

10. Rambus objects to Complainant's requests regarding the scope of claims in Rambus's patents and patent applications that were not pending during the time that Rambus was a member of JEDEC as irrelevant to any issue raised by this matter. *See Rambus Inc. v. Infineon Technologies AG*, -- F.3d --, 2003 WL 187265, at *17 (Fed. Cir. Jan. 29, 2003) ("[A] member's intentions to file or amend applications do not fall within the scope of JEDEC's disclosure duty.").

11. Rambus objects that its discovery and analysis is ongoing. Any statement

expressed herein is subject to change and/or supplementation.

**REQUEST FOR ADMISSION NO. 1:**

Admit that, to comply with JEDEC Standard No. 21-C, an SDRAM device must contain a mode register to store a value to determine CAS latency, where that value can be changed by programming the mode register.

**RESPONSE TO REQUEST FOR ADMISSION NO. 1:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JEDEC Standard No. 21-C is the subject of the request, which part of JEDEC Standard No. 21-C is the subject of the request, and the terms "mode register," "to determine CAS latency," and "programming." Rambus further objects to this request on the grounds that it is compound.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Section 3.11.5.1.3 of certain versions of JEDEC Standard No. 21-C did or does purport to relate, *inter alia*, to certain SDRAM devices and shows a representation of a "Mode Register" that is "located on the Synchronous DRAM (SDRAM or SGRAM) chip." Rambus further admits that Section 3.11.5.1.3 states that the purpose of the "Mode Register" is "to store the mode-of-operation data," that this data contains, *inter alia*, "the /CAS Latency," and that "[d]uring operation, this register (and therefore operation of the chip) may be changed."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 2:**

Admit that, to comply with JEDEC Standard No. 21-C, a DDR SDRAM device must contain a mode register to store a value to determine CAS latency, where that value can be changed by programming the mode register.

**RESPONSE TO REQUEST FOR ADMISSION NO. 2:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least

with respect to which version of JEDEC Standard No. 21-C is the subject of the request, which part of JEDEC Standard No. 21-C is the subject of the request, and the terms "mode register," "to determine CAS latency," and "programming." Rambus further objects to this request on the grounds that it is compound.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Section 3.11.5.1.3 of certain versions of JEDEC Standard No. 21-C did or does purport to relate, *inter alia*, to certain DDR SDRAM devices and shows a representation of a "Mode Register" that is "located on the Synchronous DRAM (SDRAM or SGRAM) chip." Rambus further admits that Section 3.11.5.1.3 states that the purpose of the "Mode Register" is "to store the mode-of-operation data," that this data contains, *inter alia*, "the /CAS Latency," and that "[d]uring operation, this register (and therefore operation of the chip) may be changed."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 3:**

Admit that, to comply with JEDEC Standard No. 21-C, an SDRAM device must contain a mode register to store a value to determine burst length, where that value can be changed by programming the mode register.

**RESPONSE TO REQUEST FOR ADMISSION NO. 3:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JEDEC Standard No. 21-C is the subject of the request, which part of JEDEC Standard No. 21-C is the subject of the request, and the terms "mode register," "to determine burst length," and "programming." Rambus further objects to this request on the grounds that it is compound.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Section 3.11.5.1.3 of certain versions of JEDEC Standard No. 21-C did or does purport to relate, *inter alia*, to certain SDRAM devices and shows a representation of

a "Mode Register" that is "located on the Synchronous DRAM (SDRAM or SGRAM) chip." Rambus further admits that Section 3.11.5.1.3 states that the purpose of the "Mode Register" is "to store the mode-of-operation data," that this data contains, *inter alia*, "the Burst Length," and that "[d]uring operation, this register (and therefore operation of the chip) may be changed."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 4:**

Admit that, to comply with JEDEC Standard No. 21-C, a DDR SDRAM device must contain a mode register to store a value to determine burst length, where that value can be changed by programming the mode register.

**RESPONSE TO REQUEST FOR ADMISSION NO. 4:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JEDEC Standard No. 21-C is the subject of the request, which part of JEDEC Standard No. 21-C is the subject of the request, and the terms "mode register," "to determine burst length," and "programming." Rambus further objects to this request on the grounds that it is compound.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Section 3.11.5.1.3 of certain versions of JEDEC Standard No. 21-C did or does purport to relate, *inter alia*, to certain DDR SDRAM devices and shows a representation of a "Mode Register" that is "located on the Synchronous DRAM (SDRAM or SGRAM) chip." Rambus further admits that Section 3.11.5.1.3 states that the purpose of the "Mode Register" is "to store the mode-of-operation data," that this data contains, *inter alia*, "the Burst Length," and that "[d]uring operation, this register (and therefore operation of the chip) may be changed."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 5:**

Admit that, to comply with JEDEC Standard No. 21-C, an SDRAM device must contain a mode register to store a value to determine block size, where that value can be changed by programming the mode register.

**RESPONSE TO REQUEST FOR ADMISSION NO. 5:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JEDEC Standard No. 21-C is the subject of the request, which part of JEDEC Standard No. 21-C is the subject of the request, and the terms "mode register," "to determine block size," and "programming." Rambus further objects to this request on the grounds that it is compound.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Section 3.11.5.1.3 of certain versions of JEDEC Standard No. 21-C did or does purport to relate, *inter alia*, to certain SDRAM devices and shows a representation of a "Mode Register" that is "located on the Synchronous DRAM (SDRAM or SGRAM) chip." Rambus further admits that Section 3.11.5.1.3 states that the purpose of the "Mode Register" is "to store the mode-of-operation data," that this data contains, *inter alia*, "the Burst Length," and that "[d]uring operation, this register (and therefore operation of the chip) may be changed."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 6:**

Admit that, to comply with JEDEC Standard No. 21-C, a DDR SDRAM device must contain a mode register to store a value to determine block size, where that value can be changed by programming the mode register.

**RESPONSE TO REQUEST FOR ADMISSION NO. 6:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JEDEC Standard No. 21-C is the subject of the request, which part of JEDEC Standard No. 21-C is the subject of the request, and the terms "mode register,"

"to determine block size," and "programming." Rambus further objects to this request on the grounds that it is compound.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Section 3.11.5.1.3 of certain versions of JEDEC Standard No. 21-C did or does purport to relate, *inter alia*, to certain DDR SDRAM devices and shows a representation of a "Mode Register" that is "located on the Synchronous DRAM (SDRAM or SGRAM) chip." Rambus further admits that Section 3.11.5.1.3 states that the purpose of the "Mode Register" is "to store the mode-of-operation data," that this data contains, *inter alia*, "the Burst Length," and that "[d]uring operation, this register (and therefore operation of the chip) may be changed."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 7:**

Admit that section 3.11.5.3 (page 3.11.5 –8) of JEDEC Standard No. 21-C, Release 4, shows programmable CAS latency.

**RESPONSE TO REQUEST FOR ADMISSION NO. 7:**

Rambus objects to this request on the grounds that it is vague and ambiguous at least with respect to the term "programmable CAS latency."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Section 3.11.5.3 of JEDEC Standard No. 21-C, Release 4, shows a representation of a "Mode Register" that is "located on the Synchronous DRAM (SDRAM) chip." Rambus further admits that Section 3.11.5.3 states that the purpose of the "Mode Register" is "to store the mode-of-operation data," that "[t]his data is written after power-on and before normal operation," that this data contains, *inter alia*, "the /CE Latency," and that "[d]uring operation, this register (and therefore operation of the chip) may be changed."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 8:**

Admit that section 3.11.5.1.3 of JEDEC Standard No. 21-C, Release 9, shows programmable CAS latency.

**RESPONSE TO REQUEST FOR ADMISSION NO. 8:**

Rambus objects to this request on the grounds that it is vague and ambiguous at least with respect to the term "programmable CAS latency."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Section 3.11.5.1.3 of JEDEC Standard No. 21-C, Release 9, shows a representation of a "Mode Register" that is "located on the Synchronous DRAM (SDRAM or SGRAM) chip." Rambus further admits that Section 3.11.5.1.3 states that the purpose of the "Mode Register" is "to store the mode-of-operation data," that "[t]his data is written after power-on and before normal operation," that this data contains, *inter alia*, "the /CAS Latency," and that "[d]uring operation, this register (and therefore operation of the chip) may be changed."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 9:**

Admit that section 3.11.5.3 (page 3.11.5 –8) of JEDEC Standard No. 21-C, Release 4, shows programmable burst length.

**RESPONSE TO REQUEST FOR ADMISSION NO. 9:**

Rambus objects to this request on the grounds that it is vague and ambiguous at least with respect to the term "programmable burst length."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Section 3.11.5.3 of JEDEC Standard No. 21-C, Release 4, shows a representation of a "Mode Register" that is "located on the Synchronous DRAM (SDRAM) chip." Rambus further admits that Section 3.11.5.3 states that the purpose of the "Mode Register" is "to store the mode-of-operation data," that "[t]his data is written after power-on and before normal operation," that this data contains, *inter alia*, "the Burst Length," and that

"[d]uring operation, this register (and therefore operation of the chip) may be changed."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 10:**

Admit that section 3.11.5.1.3 of JEDEC Standard No. 21-C, Release 9, shows programmable burst length.

**RESPONSE TO REQUEST FOR ADMISSION NO. 10:**

Rambus objects to this request on the grounds that it is vague and ambiguous at least with respect to the term "programmable burst length."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Section 3.11.5.1.3 of JEDEC Standard No. 21-C, Release 9, shows a representation of a "Mode Register" that is "located on the Synchronous DRAM (SDRAM or SGRAM) chip." Rambus further admits that Section 3.11.5.1.3 states that the purpose of the "Mode Register" is "to store the mode-of-operation data," that "[t]his data is written after power-on and before normal operation," that this data contains, *inter alia*, "the Burst Length," and that "[d]uring operation, this register (and therefore operation of the chip) may be changed."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 11:**

Admit that section 3.11.5.3 (page 3.11.5 –8) of JEDEC Standard No. 21-C, Release 4, shows programmable block size.

**RESPONSE TO REQUEST FOR ADMISSION NO. 11:**

Rambus objects to this request on the grounds that it is vague and ambiguous at least with respect to the term "programmable block size."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Section 3.11.5.3 of JEDEC Standard No. 21-C, Release 4, shows a representation of a "Mode Register" that is "located on the Synchronous DRAM (SDRAM) chip." Rambus further admits that Section 3.11.5.3 states that the purpose of the "Mode

Register" is "to store the mode-of-operation data," that "[t]his data is written after power-on and before normal operation," that this data contains, *inter alia,* "the Burst Length," and that "[d]uring operation, this register (and therefore operation of the chip) may be changed."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 12:**

Admit that section 3.11.5.1.3 of JEDEC Standard No. 21-C, Release 9, shows programmable block size.

**RESPONSE TO REQUEST FOR ADMISSION NO. 12:**

Rambus objects to this request on the grounds that it is vague and ambiguous at least with respect to the term "programmable block size."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Section 3.11.5.1.3 of JEDEC Standard No. 21-C, Release 9, shows a representation of a "Mode Register" that is "located on the Synchronous DRAM (SDRAM or SGRAM) chip." Rambus further admits that Section 3.11.5.1.3 states that the purpose of the "Mode Register" is "to store the mode-of-operation data," that "[t]his data is written after power-on and before normal operation," that this data contains, *inter alia*, "the Burst Length," and that "[d]uring operation, this register (and therefore operation of the chip) may be changed."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 13:**

Admit that section 3.11.5.3 (page 3.11.5 –8) of JEDEC Standard No. 21-C, Release 4, shows a Mode Register that stores mode-of-operation data, including the CAS Latency.

**RESPONSE TO REQUEST FOR ADMISSION NO. 13:**

Rambus objects to this request on the grounds that it is vague and ambiguous at least with respect to the terms "Mode Register," "mode-of-operation data," and "CAS Latency." Rambus further objects to this request on the grounds that it is compound.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Section 3.11.5.3 of JEDEC Standard No. 21-C, Release 4, shows a representation of a "Mode Register" that is "located on the Synchronous DRAM (SDRAM) chip." Rambus further admits that Section 3.11.5.3 states that the purpose of the "Mode Register" is "to store the mode-of-operation data," and that this data contains, *inter alia*, "the /CE Latency."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 14:**

Admit that section 3.11.5.1.3 of JEDEC Standard No. 21-C, Release 9, shows a Mode Register that stores mode-of-operation data, including the CAS Latency.

**RESPONSE TO REQUEST FOR ADMISSION NO. 14:**

Rambus objects to this request on the grounds that it is vague and ambiguous at least with respect to the terms "Mode Register," "mode-of-operation data," and "CAS Latency." Rambus further objects to this request on the grounds that it is compound.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Section 3.11.5.1.3 of JEDEC Standard No. 21-C, Release 9, shows a representation of a "Mode Register" that is "located on the Synchronous DRAM (SDRAM or SGRAM) chip." Rambus further admits that Section 3.11.5.1.3 states that the purpose of the "Mode Register" is "to store the mode-of-operation data," and that this data contains, *inter alia*, "the /CAS Latency."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 15:**

Admit that section 3.11.5.3 (page 3.11.5 –8) of JEDEC Standard No. 21-C, Release 4, shows a Mode Register that stores mode-of-operation data, including the Burst Length.

**RESPONSE TO REQUEST FOR ADMISSION NO. 15:**

Rambus objects to this request on the grounds that it is vague and ambiguous at least with respect to the terms "Mode Register" and "mode-of-operation data." Rambus further objects to this request on the grounds that it is compound.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Section 3.11.5.3 of JEDEC Standard No. 21-C, Release 4, shows a representation of a "Mode Register" that is "located on the Synchronous DRAM (SDRAM) chip." Rambus further admits that Section 3.11.5.3 states that the purpose of the "Mode Register" is "to store the mode-of-operation data," and that this data contains, *inter alia*, "the Burst Length."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 16:**

Admit that section 3.11.5.1.3 of JEDEC Standard No. 21-C, Release 9, shows a Mode Register that stores mode-of-operation data, including the Burst Length.

**RESPONSE TO REQUEST FOR ADMISSION NO. 16:**

Rambus objects to this request on the grounds that it is vague and ambiguous at least with respect to the terms "Mode Register" and "mode-of-operation data." Rambus further objects to this request on the grounds that it is compound.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Section 3.11.5.1.3 of JEDEC Standard No. 21-C, Release 9, shows a representation of a "Mode Register" that is "located on the Synchronous DRAM (SDRAM or SGRAM) chip." Rambus further admits that Section 3.11.5.1.3 states that the purpose of the "Mode Register" is "to store the mode-of-operation data," and that this data contains, *inter alia*, "the Burst Length."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 17:**

Admit that, in section 3.11.5.3 (page 3.11.5 –8) of JEDEC Standard No. 21-C, Release 4, the values stored in the Mode Register (and therefore the operation of the chip) can be changed.

**RESPONSE TO REQUEST FOR ADMISSION NO. 17:**

Rambus objects to this request on the grounds that it is vague and ambiguous at least with respect to the terms "Mode Register" and "operation of the chip." Rambus further objects to this request on the grounds that it is compound.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Section 3.11.5.3 of JEDEC Standard No. 21-C, Release 4, shows a representation of a "Mode Register" that is "located on the Synchronous DRAM (SDRAM) chip." Rambus further admits that Section 3.11.5.3 states that the purpose of the "Mode Register" is "to store the mode-of-operation data," and that "[d]uring operation, this register (and therefore operation of the chip) may be changed."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 18:**

Admit that, in section 3.11.5.1.3 of JEDEC Standard No. 21-C, Release 9, the values stored in the Mode Register (and therefore the operation of the chip) can be changed.

**RESPONSE TO REQUEST FOR ADMISSION NO. 18:**

Rambus objects to this request on the grounds that it is vague and ambiguous at least with respect to the terms "Mode Register" and "operation of the chip." Rambus further objects to this request on the grounds that it is compound.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Section 3.11.5.1.3 of JEDEC Standard No. 21-C, Release 9, shows a representation of a "Mode Register" that is "located on the Synchronous DRAM (SDRAM or SGRAM) chip." Rambus further admits that Section 3.11.5.1.3 states that the purpose of the "Mode Register" is "to store the mode-of-operation data," and that "[d]uring operation, this

register (and therefore operation of the chip) may be changed."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 19:**

Admit that section 3.11.5.3 (page 3.11.5 –8) of JEDEC Standard No. 21-C, Release 4, shows a programmable register to store a value that is representative of a delay time after which the device responds to a read request.

**RESPONSE TO REQUEST FOR ADMISSION NO. 19:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "programmable register," "representative of a delay time," and "responds to a read request." Rambus further objects to this request on the grounds that it is compound.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Section 3.11.5.3 of JEDEC Standard No. 21-C, Release 4, shows a representation of a "Mode Register" that is "located on the Synchronous DRAM (SDRAM) chip." Rambus further admits that Section 3.11.5.13 states that the purpose of the "Mode Register" is "to store the mode-of-operation data," that "[t]his data is written after power-on and before normal operation," that this data contains, *inter alia*, "the /CE Latency," and that "[d]uring operation, this register (and therefore operation of the chip) may be changed."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 20:**

Admit that section 3.11.5.1.3 of JEDEC Standard No. 21-C, Release 9, shows a programmable register to store a value that is representative of a delay time after which the device responds to a read request.

**RESPONSE TO REQUEST FOR ADMISSION NO. 20:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least

with respect to the terms "programmable register," "representative of a delay time," and "responds to a read request." Rambus further objects to this request on the grounds that it is compound.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Section 3.11.5.1.3 of JEDEC Standard No. 21-C, Release 9, shows a representation of a "Mode Register" that is "located on the Synchronous DRAM (SDRAM or SGRAM) chip." Rambus further admits that Section 3.11.5.1.3 states that the purpose of the "Mode Register" is "to store the mode-of-operation data," that "[t]his data is written after power-on and before normal operation," that this data contains, *inter alia*, "the /CAS Latency," and that "[d]uring operation, this register (and therefore operation of the chip) may be changed."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 21:**

Admit that section 3.11.5.3 (page 3.11.5 –8) of JEDEC Standard No. 21-C, Release 4, shows a programmable register that receives information that defines an amount of data to be output by the memory device in response to a read request.

**RESPONSE TO REQUEST FOR ADMISSION NO. 21:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "programmable register," "receives information," "defines an amount of data," and "in response to a read request." Rambus further objects to this request on the grounds that it is compound.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Section 3.11.5.3 of JEDEC Standard No. 21-C, Release 4, shows a representation of a "Mode Register" that is "located on the Synchronous DRAM (SDRAM) chip." Rambus further admits that Section 3.11.5.3 states that the purpose of the "Mode Register" is "to store the mode-of-operation data," that "[t]his data is written after power-on and before normal operation," that this data contains, *inter alia*, "the Burst Length," and that

"[d]uring operation, this register (and therefore operation of the chip) may be changed."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 22:**

Admit that section 3.11.5.3 (page 3.11.5 –8) of JEDEC Standard No. 21-C, Release 4, shows a programmable register to store a value that defines an amount of data to be output by the memory device in response to a read request.

**RESPONSE TO REQUEST FOR ADMISSION NO. 22:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "programmable register," "defines an amount of data," and "in response to a read request." Rambus further objects to this request on the grounds that it is compound.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Section 3.11.5.3 of JEDEC Standard No. 21-C, Release 4, shows a representation of a "Mode Register" that is "located on the Synchronous DRAM (SDRAM) chip." Rambus further admits that Section 3.11.5.3 states that the purpose of the "Mode Register" is "to store the mode-of-operation data," that "[t]his data is written after power-on and before normal operation," that this data contains, *inter alia*, "the Burst Length," and that "[d]uring operation, this register (and therefore operation of the chip) may be changed."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 23:**

Admit that section 3.11.5.1.3 of JEDEC Standard No. 21-C, Release 9, shows a programmable register that receives information that defines an amount of data to be output by the memory device in response to a read request.

**RESPONSE TO REQUEST FOR ADMISSION NO. 23:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least

with respect to the terms "programmable register," "receives information," "defines an amount of data," and "in response to a read request." Rambus further objects to this request on the grounds that it is compound.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Section 3.11.5.1.3 of JEDEC Standard No. 21-C, Release 9, shows a representation of a "Mode Register" that is "located on the Synchronous DRAM (SDRAM or SGRAM) chip." Rambus further admits that Section 3.11.5.1.3 states that the purpose of the "Mode Register" is "to store the mode-of-operation data," that "[t]his data is written after power-on and before normal operation," that this data contains, *inter alia*, "the Burst Length," and that "[d]uring operation, this register (and therefore operation of the chip) may be changed."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 24:**

Admit that section 3.11.5.1.3 of JEDEC Standard No. 21-C, Release 9, shows a programmable register that stores a value that defines an amount of data to be output by the memory device in response to a read request.

**RESPONSE TO REQUEST FOR ADMISSION NO. 24:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "programmable register," "defines an amount of data," and "in response to a read request." Rambus further objects to this request on the grounds that it is compound.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Section 3.11.5.1.3 of JEDEC Standard No. 21-C, Release 9, shows a representation of a "Mode Register" that is "located on the Synchronous DRAM (SDRAM or SGRAM) chip." Rambus further admits that Section 3.11.5.1.3 states that the purpose of the "Mode Register" is "to store the mode-of-operation data," that "[t]his data is written after power-on and before normal operation," that this data contains, *inter alia*, "the Burst Length," and that

"[d]uring operation, this register (and therefore operation of the chip) may be changed."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 25:**

Admit that, to comply with JEDEC Standard No. 21-C, an SDRAM device must contain a mode register as described in section 3.11.5.3 (page 3.11.5 –8) of Release 4.

**RESPONSE TO REQUEST FOR ADMISSION NO. 25:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JEDEC Standard No. 21-C is the subject of the request, which part of JEDEC Standard No. 21-C is the subject of the request.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Section 3.11.5.3 of JEDEC Standard No. 21-C, Release 4, did purport to relate, *inter alia*, to certain SDRAM devices and shows a representation of a "Mode Register" that is "located on the Synchronous DRAM (SDRAM) chip."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 26:**

Admit that, to comply with JEDEC Standard No. 21-C, an SDRAM device must contain a mode register as described in section 3.11.5.1.3 of Release 9.

**RESPONSE TO REQUEST FOR ADMISSION NO. 26:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JEDEC Standard No. 21-C is the subject of the request, which part of JEDEC Standard No. 21-C is the subject of the request.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Section 3.11.5.1.3 of JEDEC Standard No. 21-C, Release 9, did purport to relate, *inter alia*, to certain SDRAM devices and shows a representation of a "Mode Register" that is "located on the Synchronous DRAM (SDRAM or SGRAM) chip."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 27:**

Admit that, to comply with JEDEC Standard No. 21-C, a DDR SDRAM device must contain a mode register as described in section 3.11.5.1.3 of Release 9.

**RESPONSE TO REQUEST FOR ADMISSION NO. 27:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JEDEC Standard No. 21-C is the subject of the request, which part of JEDEC Standard No. 21-C is the subject of the request.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Section 3.11.5.1.3 of JEDEC Standard No. 21-C, Release 9, did purport to relate, *inter alia*, to certain DDR SDRAM devices and shows a representation of a "Mode Register" that is "located on the Synchronous DRAM (SDRAM or SGRAM) chip."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 28:**

Admit that, to comply with JEDEC Standard No. 21-C, an SDRAM device must contain a programmable register to store a value that is representative of a delay time after which the device responds to a read request.

**RESPONSE TO REQUEST FOR ADMISSION NO. 28:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JEDEC Standard No. 21-C is the subject of the request, which part of JEDEC Standard No. 21-C is the subject of the request and the terms "programmable register," "representative of a delay time," and "responds to a read request." Rambus further objects to this request on the grounds that it is compound.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Section 3.11.5.1.3 of certain versions of JEDEC Standard No. 21-C

did or does purport to relate, *inter alia*, to certain SDRAM devices and shows a representation of a "Mode Register" that is "located on the Synchronous DRAM (SDRAM or SGRAM) chip." Rambus further admits that Section 3.11.5.1.3 states that the purpose of the "Mode Register" is "to store the mode-of-operation data," that "[t]his data is written after power-on and before normal operation," that this data contains, *inter alia*, "the /CAS Latency," and that "[d]uring operation, this register (and therefore operation of the chip) may be changed."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 29:**

Admit that, to comply with JEDEC Standard No. 21-C, an SDRAM device must contain a programmable register that receives information that defines an amount of data to be output by the memory device in response to a read request.

**RESPONSE TO REQUEST FOR ADMISSION NO. 29:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JEDEC Standard No. 21-C is the subject of the request, which part of JEDEC Standard No. 21-C is the subject of the request and the terms "programmable register," "receives information," "defines an amount of data," and "in response to a read request." Rambus further objects to this request on the grounds that it is compound.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Section 3.11.5.1.3 of certain versions of JEDEC Standard No. 21-C did or does purport to relate to, *inter alia*, certain SDRAM devices and shows a representation of a "Mode Register" that is "located on the Synchronous DRAM (SDRAM or SGRAM) chip." Rambus further admits that Section 3.11.5.1.3 states that the purpose of the "Mode Register" is "to store the mode-of-operation data," that "[t]his data is written after power-on and before normal operation," that this data contains, *inter alia*, "the Burst Length," and that "[d]uring operation, this register (and therefore operation of the chip) may be changed."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 30:**

Admit that, to comply with JEDEC Standard No. 21-C, an SDRAM device must contain a programmable register to store a value that defines an amount of data to be output by the memory device in response to a read request.

**RESPONSE TO REQUEST FOR ADMISSION NO. 30:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JEDEC Standard No. 21-C is the subject of the request, which part of JEDEC Standard No. 21-C is the subject of the request and the terms "programmable register," "defines an amount of data," and "in response to a read request." Rambus further objects to this request on the grounds that it is compound.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Section 3.11.5.1.3 of certain versions of JEDEC Standard No. 21-C did or does purport to relate to, *inter alia*, certain SDRAM devices and shows a representation of a "Mode Register" that is "located on the Synchronous DRAM (SDRAM or SGRAM) chip." Rambus further admits that Section 3.11.5.1.3 states that the purpose of the "Mode Register" is "to store the mode-of-operation data," that "[t]his data is written after power-on and before normal operation," that this data contains, *inter alia*, "the Burst Length," and that "[d]uring operation, this register (and therefore operation of the chip) may be changed."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 31:**

Admit that, to comply with JEDEC Standard No. 21-C, a DDR SDRAM device must contain a programmable register to store a value that is representative of a delay time after which the device responds to a read request.

**RESPONSE TO REQUEST FOR ADMISSION NO. 31:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least

with respect to which version of JEDEC Standard No. 21-C is the subject of the request, which part of JEDEC Standard No. 21-C is the subject of the request and the terms "programmable register," "representative of a delay time," and "responds to a read request." Rambus further objects to this request on the grounds that it is compound.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Section 3.11.5.1.3 of certain versions of JEDEC Standard No. 21-C did or does purport to relate to, *inter alia*, certain DDR SDRAM devices and shows a representation of a "Mode Register" that is "located on the Synchronous DRAM (SDRAM or SGRAM) chip." Rambus further admits that Section 3.11.5.1.3 states that the purpose of the "Mode Register" is "to store the mode-of-operation data," that "[t]his data is written after power-on and before normal operation," that this data contains, *inter alia*, "the /CAS Latency," and that "[d]uring operation, this register (and therefore operation of the chip) may be changed."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 32:**

Admit that, to comply with JEDEC Standard No. 21-C, a DDR SDRAM device must contain a programmable register that receives information that defines an amount of data to be output by the memory device in response to a read request.

**RESPONSE TO REQUEST FOR ADMISSION NO. 32:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JEDEC Standard No. 21-C is the subject of the request, which part of JEDEC Standard No. 21-C is the subject of the request, and the terms "programmable register," "receives information," "defines an amount of data," and "in response to a read request." Rambus further objects to this request on the grounds that it is compound.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Section 3.11.5.1.3 of certain versions of JEDEC Standard No. 21-C did or does purport to relate to, *inter alia*, certain DDR SDRAM devices and shows a

representation of a "Mode Register" that is "located on the Synchronous DRAM (SDRAM or SGRAM) chip." Rambus further admits that Section 3.11.5.1.3 states that the purpose of the "Mode Register" is "to store the mode-of-operation data," that "[t]his data is written after power-on and before normal operation," that this data contains, *inter alia*, "the Burst Length," and that "[d]uring operation, this register (and therefore operation of the chip) may be changed."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 33:**

Admit that, to comply with JEDEC Standard No. 21-C, a DDR SDRAM device must contain a programmable register to store a value that defines an amount of data to be output by the memory device in response to a read request.

**RESPONSE TO REQUEST FOR ADMISSION NO. 33:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JEDEC Standard No. 21-C is the subject of the request, which part of JEDEC Standard No. 21-C is the subject of the request, and the terms "programmable register," "defines an amount of data," and "in response to a read request." Rambus further objects to this request on the grounds that it is compound.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Section 3.11.5.1.3 of certain versions of JEDEC Standard No. 21-C did or does purport to relate to, *inter alia*, certain DDR SDRAM devices and shows a representation of a "Mode Register" that is "located on the Synchronous DRAM (SDRAM or SGRAM) chip." Rambus further admits that Section 3.11.5.1.3 states that the purpose of the "Mode Register" is "to store the mode-of-operation data," that "[t]his data is written after power-on and before normal operation," that this data contains, *inter alia*, "the Burst Length," and that "[d]uring operation, this register (and therefore operation of the chip) may be changed."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 34:**

Admit that, to comply with JEDEC Standard No. 21-C, an SDRAM device must contain a programmable register to store a value which is representative of a delay time, that value being a number of clock cycles of an external clock, after which the SDRAM responds to a read request.

**RESPONSE TO REQUEST FOR ADMISSION NO. 34:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JEDEC Standard No. 21-C is the subject of the request, which part of JEDEC Standard No. 21-C is the subject of the request, and the terms "programmable register," "representative of a delay time," "a number of clock cycles," and "responds to a read request." Rambus further objects to this request on the grounds that it is compound.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Section 3.11.5.1.3 of certain versions of JEDEC Standard No. 21-C did or does purport to relate to, *inter alia*, certain SDRAM devices and shows a representation of a "Mode Register" that is "located on the Synchronous DRAM (SDRAM or SGRAM) chip." Rambus further admits that Section 3.11.5.1.3 states that the purpose of the "Mode Register" is "to store the mode-of-operation data," that "[t]his data is written after power-on and before normal operation," that this data contains, *inter alia*, "the /CAS Latency," and that "[d]uring operation, this register (and therefore operation of the chip) may be changed."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 35:**

Admit that, to comply with JEDEC Standard No. 21-C, a DDR SDRAM device must contain a programmable register to store a value which is representative of a delay time, that value being a number of clock cycles of an external clock, after which the SDRAM responds to a read request.

**RESPONSE TO REQUEST FOR ADMISSION NO. 35:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JEDEC Standard No. 21-C is the subject of the request, which part of JEDEC Standard No. 21-C is the subject of the request, and the terms "programmable register," "representative of a delay time," and "responds to a read request." Rambus further objects to this request on the grounds that it is compound.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Section 3.11.5.1.3 of certain versions of JEDEC Standard No. 21-C did or does purport to relate to, *inter alia*, certain DDR SDRAM devices and shows a representation of a "Mode Register" that is "located on the Synchronous DRAM (SDRAM or SGRAM) chip." Rambus further admits that Section 3.11.5.1.3 states that the purpose of the "Mode Register" is "to store the mode-of-operation data," that "[t]his data is written after power-on and before normal operation," that this data contains, *inter alia*, "the /CAS Latency," and that "[d]uring operation, this register (and therefore operation of the chip) may be changed.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 36:**

Admit that, to comply with JEDEC Standard No. 21-C, an SDRAM device must contain a programmable register operative to store information specifying a manner in which the semiconductor device is to respond to a read request or a write request.

**RESPONSE TO REQUEST FOR ADMISSION NO. 36:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JEDEC Standard No. 21-C is the subject of the request, which part of JEDEC Standard No. 21-C is the subject of the request, and the terms "programmable register," "operative to store information," "manner," and "respond to a read request," and "respond to . . . a write request." Rambus further objects to this request on the grounds that it is compound.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Section 3.11.5.1.3 of certain versions of JEDEC Standard No. 21-C did or does purport to relate to, *inter alia*, certain SDRAM devices and shows a representation of a "Mode Register" that is "located on the Synchronous DRAM (SDRAM or SGRAM) chip." Rambus further admits that Section 3.11.5.1.3 states that the purpose of the "Mode Register" is "to store the mode-of-operation data," that "[t]his data is written after power-on and before normal operation," that this data contains, *inter alia*, "the Burst Length, the Burst Type, the /CAS Latency . . ., and whether it is to be operating in Test Mode, or Normal operating mode," and that "[d]uring operation, this register (and therefore operation of the chip) may be changed."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 37:**

Admit that, to comply with JEDEC Standard No. 21-C, a DDR SDRAM device must contain a programmable register operative to store information specifying a manner in which the semiconductor device is to respond to a read request or a write request.

**RESPONSE TO REQUEST FOR ADMISSION NO. 37:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JEDEC Standard No. 21-C is the subject of the request, which part of JEDEC Standard No. 21-C is the subject of the request, and the terms "programmable register," "operative to store information," "manner," and "respond to a read request," and "respond to . . . a write request." Rambus further objects to this request on the grounds that it is compound.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Section 3.11.5.1.3 of certain versions of JEDEC Standard No. 21-C did or does purport to relate to, *inter alia*, certain DDR SDRAM devices and shows a representation of a "Mode Register" that is "located on the Synchronous DRAM (SDRAM or SGRAM) chip." Rambus further admits that Section 3.11.5.1.3 states that the purpose of the

"Mode Register" is "to store the mode-of-operation data," that "[t]his data is written after power-on and before normal operation," that this data contains, *inter alia*, "the Burst Length, the Burst Type, the /CAS Latency . . ., and whether it is to be operating in Test Mode, or Normal operating mode," and that "[d]uring operation, this register (and therefore operation of the chip) may be changed."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 38:**

Admit that, to comply with JEDEC Standard No. 21-C, an SDRAM device must contain a programmable access-time register operative to store information specifying a value indicative of an access time for the device, such that the device waits for the access time before responding to a read request.

**RESPONSE TO REQUEST FOR ADMISSION NO. 38:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JEDEC Standard No. 21-C is the subject of the request, which part of JEDEC Standard No. 21-C is the subject of the request, and the terms "programmable access-time register," "operative to store information," "indicative of an access time," "waits for the access time," and "responding to a read request." Rambus further objects to this request on the grounds that it is compound.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Section 3.11.5.1.3 of certain versions of JEDEC Standard No. 21-C did or does purport to relate to, *inter alia*, certain SDRAM devices and shows a representation of a "Mode Register" that is "located on the Synchronous DRAM (SDRAM or SGRAM) chip." Rambus further admits that Section 3.11.5.1.3 states that the purpose of the "Mode Register" is "to store the mode-of-operation data," that "[t]his data is written after power-on and before normal operation," that this data contains, *inter alia*, "the /CAS Latency," and that "[d]uring operation, this register (and therefore operation of the chip) may be changed."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 39:**

Admit that, to comply with JEDEC Standard No. 21-C, a DDR SDRAM device must contain a programmable access-time register operative to store information specifying a value indicative of an access time for the device, such that the device waits for the access time before responding to a read request.

**RESPONSE TO REQUEST FOR ADMISSION NO. 39:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JEDEC Standard No. 21-C is the subject of the request, which part of JEDEC Standard No. 21-C is the subject of the request, and the terms "programmable access-time register," "operative to store information," "indicative of an access time," "waits for the access time," and "responding to a read request." Rambus further objects to this request on the grounds that it is compound.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Section 3.11.5.1.3 of certain versions of JEDEC Standard No. 21-C did or does purport to relate to, *inter alia*, certain DDR SDRAM devices and shows a representation of a "Mode Register" that is "located on the Synchronous DRAM (SDRAM or SGRAM) chip." Rambus further admits that Section 3.11.5.1.3 states that the purpose of the "Mode Register" is "to store the mode-of-operation data," that "[t]his data is written after power-on and before normal operation," that this data contains, *inter alia*, "the /CAS Latency," and that "[d]uring operation, this register (and therefore operation of the chip) may be changed."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 40:**

Admit that, to comply with JEDEC Standard No. 21-C, an SDRAM device must contain a programmable register that receives information that defines an amount of data to be input by

the memory device in response to a write request.

**RESPONSE TO REQUEST FOR ADMISSION NO. 40:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JEDEC Standard No. 21-C is the subject of the request, which part of JEDEC Standard No. 21-C is the subject of the request, and the terms "programmable register," "receives information," "defines an amount of data" and "in response to a write request." Rambus further objects to this request on the grounds that it is compound.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Section 3.11.5.1.3 of certain versions of JEDEC Standard No. 21-C did or does purport to relate to, *inter alia*, certain SDRAM devices and shows a representation of a "Mode Register" that is "located on the Synchronous DRAM (SDRAM or SGRAM) chip." Rambus further admits that Section 3.11.5.1.3 states that the purpose of the "Mode Register" is "to store the mode-of-operation data," that "[t]his data is written after power-on and before normal operation," that this data contains, *inter alia*, "the Burst Length," and that "[d]uring operation, this register (and therefore operation of the chip) may be changed."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 41:**

Admit that, to comply with JEDEC Standard No. 21-C, a DDR SDRAM device must contain a programmable register that receives information that defines an amount of data to be input by the memory device in response to a write request.

**RESPONSE TO REQUEST FOR ADMISSION NO. 41:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JEDEC Standard No. 21-C is the subject of the request, which part of JEDEC Standard No. 21-C is the subject of the request, and the terms "programmable register," "receives information," "defines an amount of data" and "in response to a write request." Rambus further objects to this request on the grounds that it is compound.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Section 3.11.5.1.3 of certain versions of JEDEC Standard No. 21-C did or does purport to relate to, *inter alia*, certain DDR SDRAM devices and shows a representation of a "Mode Register" that is "located on the Synchronous DRAM (SDRAM or SGRAM) chip." Rambus further admits that Section 3.11.5.1.3 states that the purpose of the "Mode Register" is "to store the mode-of-operation data," that "[t]his data is written after power-on and before normal operation," that this data contains, *inter alia*, "the Burst Length," and that "[d]uring operation, this register (and therefore operation of the chip) may be changed."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 42:**

Admit that, to comply with JEDEC Standard No. 21-C, an SDRAM device must contain a programmable register to store a value that defines an amount of data to be input by the memory device in response to a write request.

**RESPONSE TO REQUEST FOR ADMISSION NO. 42:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JEDEC Standard No. 21-C is the subject of the request, which part of JEDEC Standard No. 21-C is the subject of the request, and the terms "programmable register," "defines an amount of data" and "in response to a write request." Rambus further objects to this request on the grounds that it is compound.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Section 3.11.5.1.3 of certain versions of JEDEC Standard No. 21-C did or does purport to relate to, *inter alia*, certain SDRAM devices and shows a representation of a "Mode Register" that is "located on the Synchronous DRAM (SDRAM or SGRAM) chip." Rambus further admits that Section 3.11.5.1.3 states that the purpose of the "Mode Register" is "to store the mode-of-operation data," that "[t]his data is written after power-on and before normal operation," that this data contains, *inter alia*, "the Burst Length," and that "[d]uring

operation, this register (and therefore operation of the chip) may be changed."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 43:**

Admit that, to comply with JEDEC Standard No. 21-C, a DDR SDRAM device must contain a programmable register to store a value that defines an amount of data to be input by the memory device in response to a write request.

**RESPONSE TO REQUEST FOR ADMISSION NO. 43:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JEDEC Standard No. 21-C is the subject of the request, which part of JEDEC Standard No. 21-C is the subject of the request, and the terms "programmable register," "defines an amount of data" and "in response to a write request." Rambus further objects to this request on the grounds that it is compound.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Section 3.11.5.1.3 of certain versions of JEDEC Standard No. 21-C did or does purport to relate to, *inter alia*, certain DDR SDRAM devices and shows a representation of a "Mode Register" that is "located on the Synchronous DRAM (SDRAM or SGRAM) chip." Rambus further admits that Section 3.11.5.1.3 states that the purpose of the "Mode Register" is "to store the mode-of-operation data," that "[t]his data is written after power-on and before normal operation," that this data contains, *inter alia*, "the Burst Length," and that "[d]uring operation, this register (and therefore operation of the chip) may be changed."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 44:**

Admit that, to comply with the JEDEC Double Data Rate (DDR) SDRAM Specification, JESD79, a DDR SDRAM device must contain a mode register to store a value to determine CAS latency, where that value can be changed by programming the mode register.

**RESPONSE TO REQUEST FOR ADMISSION NO. 44:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JESD79 is the subject of the request and the terms "mode register," "to determine CAS latency" and "programming." Rambus further objects to this request on the grounds that it is compound.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that JESD79, Release 1, purports to relate to certain DDR SDRAM devices. Rambus further admits that JESD79, Release 1, states in part:

"The Mode Register is used to define the specific mode of operation of the DDR SDRAM. This definition includes the selection of . . . a CAS latency . . . . The Mode Register is programmed via the MODE REGISTER SET command . . . and will retain the stored information until it is programmed again or the device loses power (except for bit A8, which is self-clearing).

"Mode Register bits . . . A4-A6 specify the CAS latency . . . . "

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 45:**

Admit that, to comply with the JEDEC Double Data Rate (DDR) SDRAM Specification, JESD79, a DDR SDRAM device must contain a mode register to store a value to determine burst length, where that value can be changed by programming the mode register.

**RESPONSE TO REQUEST FOR ADMISSION NO. 45:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JESD79 is the subject of the request and the terms "mode register," "to determine burst length" and "programming." Rambus further objects to this request on the grounds that it is compound.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that JESD79, Release 1, purports to relate to certain DDR SDRAM

devices. Rambus further admits that JESD79, Release 1, states in part:

"The Mode Register is used to define the specific mode of operation of the DDR SDRAM. This definition includes the selection of a burst length . . . . The Mode Register is programmed via the MODE REGISTER SET command . . . and will retain the stored information until it is programmed again or the device loses power (except for bit A8, which is self-clearing).

"Mode Register bits A0-A2 specify the burst length . . . . "

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 46:**

Admit that the JEDEC Double Data Rate (DDR) SDRAM Specification, JESD79, pages 8-10 and Figure 1, shows programmable CAS latency.

**RESPONSE TO REQUEST FOR ADMISSION NO. 46:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JESD79 is the subject of the request and the term "programmable CAS latency."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that page 8 of JESD79, Release 1, states in part:

"The Mode Register is used to define the specific mode of operation of the DDR SDRAM. This definition includes the selection of . . . a CAS latency . . . . The Mode Register is programmed via the MODE REGISTER SET command . . . and will retain the stored information until it is programmed again or the device loses power (except for bit A8, which is self-clearing).

"Mode Register bits . . . A4-A6 specify the CAS latency . . . . "

Rambus further admits that Figure 1 on page 9 of JESD79, Release 1, shows a representation of a "Mode Register" with bits A4-A6 designated as "CAS Latency."

Rambus further admits that page 10 of JESD79, Release 1, states in part:

"The READ latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first piece of output data. The latency can be set for to 2 or 2.5 clocks (latencies of 1.5 or 3 are optional, and one or both of these optional latencies might be supported by some vendors.

"If a READ command is registered at clock edge n, and the latency is m clocks, the data will be available normally coincident with clock edge n + m. Table 2 below indicates the operating frequencies at which each CAS latency setting can be used."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 47:**

Admit that the JEDEC Double Data Rate (DDR) SDRAM Specification, JESD79, pages 8-10 and Figure 1, shows programmable burst length.

**RESPONSE TO REQUEST FOR ADMISSION NO. 47:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JESD79 is the subject of the request and the term "programmable burst length."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that page 8 of JESD79, Release 1, states in part:

"The Mode Register is used to define the specific mode of operation of the DDR SDRAM. This definition includes the selection of a burst length . . . . The Mode Register is programmed via the MODE REGISTER SET command . . . and will retain the stored information until it is programmed again or the device loses power (except for bit A8, which is self-clearing).

"Mode Register bits A0-A2 specify the burst length . . . . "

Rambus further admits that Figure 1 on page 9 of JESD79, Release 1, shows a representation of a "Mode Register" with bits A0-A2 designated as "Burst Length."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 48:**

Admit that the JEDEC Double Data Rate (DDR) SDRAM Specification, JESD79, pages 8-10 and Figure 1, shows a Mode Register that stores mode-of-operation data, including the Burst Length.

**RESPONSE TO REQUEST FOR ADMISSION NO. 48:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JESD79 is the subject of the request and the terms "Mode Register," "mode-of-operation data," and "Burst Length."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that page 8 of JESD79, Release 1, states in part:

"The Mode Register is used to define the specific mode of operation of the DDR SDRAM. This definition includes the selection of a burst length . . . .

"Mode Register bits A0-A2 specify the burst length . . . . "

Rambus further admits that Figure 1 on page 9 of JESD79, Release 1, shows a representation of a "Mode Register" with bits A0-A2 designated as "Burst Length."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 49:**

Admit that the JEDEC Double Data Rate (DDR) SDRAM Specification, JESD79, pages 8-10 and Figure 1, shows a Mode Register that stores mode-of-operation data, including the CAS Latency.

**RESPONSE TO REQUEST FOR ADMISSION NO. 49:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JESD79 is the subject of the request and the terms "Mode Register," "mode-of-operation data, and "CAS Latency."

Rambus admits that page 8 of JESD79, Release 1, states in part:

"The Mode Register is used to define the specific mode of operation of the DDR SDRAM. This definition includes the selection of . . . a CAS latency . . . .

"Mode Register bits . . . A4-A6 specify the CAS latency . . . . "

Rambus further admits that Figure 1 on page 9 of JESD79, Release 1, shows a representation of a "Mode Register" with bits A4-A6 designated as "CAS Latency."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 50:**

Admit that the values contained in the Mode Register shown and described in the JEDEC Double Data Rate (DDR) SDRAM Specification, JESD79, pages 8-10 and Figure 1, (and therefore the operation of the chip) can be changed.

**RESPONSE TO REQUEST FOR ADMISSION NO. 50:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JESD79 is the subject of the request and the term "operation of the chip." Rambus further objects to this request on the ground that it is compound.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that page 8 of JESD79, Release 1, states in part:

"The Mode Register is used to define the specific mode of operation of the DDR SDRAM. . . . . The Mode Register is programmed via the MODE REGISTER SET command . . . and will retain the stored information until it is programmed again or the device loses power (except for bit A8, which is self-clearing)."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 51:**

Admit that the JEDEC Double Data Rate (DDR) SDRAM Specification, JESD79, pages 8-10 and Figure 1, shows a programmable register to store a value that is representative of a delay time after which the device responds to a read request.

**RESPONSE TO REQUEST FOR ADMISSION NO. 51:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JESD79 is the subject of the request and the terms "programmable register," "representative of a delay time," and "responds to a read request."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that page 8 of JESD79, Release 1, states in part:

"The Mode Register is used to define the specific mode of operation of the DDR SDRAM. This definition includes the selection of . . . a CAS latency . . . . The Mode Register is programmed via the MODE REGISTER SET command . . . and will retain the stored information until it is programmed again or the device loses power (except for bit A8, which is self-clearing).

"Mode Register bits . . . A4-A6 specify the CAS latency . . . . "

Rambus further admits that Figure 1 on page 9 of JESD79, Release 1, shows a representation of a "Mode Register" with bits A4-A6 designated as "CAS Latency."

Rambus further admits that page 10 of JESD79, Release 1, states in part:

"The READ latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first piece of output data. The latency can be set for to 2 or 2.5 clocks (latencies of 1.5 or 3 are optional, and one or both of these optional latencies might be supported by some vendors.

"If a READ command is registered at clock edge n, and the latency is m clocks, the data will be available normally coincident with clock edge n + m. Table 2 below indicates the operating frequencies at which each CAS latency setting can be used."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 52:**

Admit that the JEDEC Double Data Rate (DDR) SDRAM Specification, JESD79, pages 8-10 and Figure 1, shows a programmable register that receives block size information that

defines an amount of data to be output by the memory device in response to a read request.

**RESPONSE TO REQUEST FOR ADMISSION NO. 52:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JESD79 is the subject of the request and the terms "programmable register," "receives," "block size information," "defines an amount of data," and "response to a read request."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that page 8 of JESD79, Release 1, states in part:

"The Mode Register is used to define the specific mode of operation of the DDR SDRAM. This definition includes the selection of a burst length . . . .

"Mode Register bits A0-A2 specify the burst length . . . . "

Rambus further admits that Figure 1 on page 9 of JESD79, Release 1, shows a representation of a "Mode Register" with bits A0-A2 designated as "Burst Length."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 53:**

Admit that, to comply with the JEDEC Double Data Rate (DDR) SDRAM Specification, JESD79, a DDR SDRAM device must contain a mode register as described in pages 8-10 and Figure 1.

**RESPONSE TO REQUEST FOR ADMISSION NO. 53:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JESD79 is the subject of the request.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that certain parts of pages 8-10 and Figure 1 of JESD79, Release 1, purport to describe certain features of a "Mode Register," some of which appear to be designated as "optional," and that JESD79, Release 1, purports to "define the minimum set of requirements for JEDEC-compliant 64M x4/x8/x16 DDR SDRAMs."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 54:**

Admit that, to comply with the JEDEC Double Data Rate (DDR) SDRAM Specification, JESD79, a DDR SDRAM device must contain a programmable register to store a value that is representative of a delay time after which the device responds to a read request.

**RESPONSE TO REQUEST FOR ADMISSION NO. 54:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JESD79 is the subject of the request and the terms "programmable register," "representative of a delay time," and "responds to a read request."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that JESD79, Release 1, purports to relate to certain DDR SDRAM devices. Rambus further admits that page 8 of JESD79, Release 1, states in part:

"The Mode Register is used to define the specific mode of operation of the DDR SDRAM. This definition includes the selection of . . . a CAS latency . . . . The Mode Register is programmed via the MODE REGISTER SET command . . . and will retain the stored information until it is programmed again or the device loses power (except for bit A8, which is self-clearing).

"Mode Register bits . . . A4-A6 specify the CAS latency . . . . "

Rambus further admits that Figure 1 on page 9 of JESD79, Release 1, shows a representation of a "Mode Register" with bits A4-A6 designated as "CAS Latency."

Rambus further admits that page 10 of JESD79, Release 1, states in part:

"The READ latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first piece of output data. The latency can be set for to 2 or 2.5 clocks (latencies of 1.5 or 3 are optional, and one or both of these optional latencies might be supported by some vendors.

"If a READ command is registered at clock edge n, and the latency is m clocks, the data

will be available normally coincident with clock edge n + m. Table 2 below indicates the operating frequencies at which each CAS latency setting can be used."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 55:**

Admit that, to comply with the JEDEC Double Data Rate (DDR) SDRAM Specification, JESD79, a DDR SDRAM device must contain a programmable register that receives block size information that defines an amount of data to be output by the memory device in response to a read request.

**RESPONSE TO REQUEST FOR ADMISSION NO. 55:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JESD79 is the subject of the request and the terms "programmable register," "receives," "block size information," "defines an amount of data," and "response to a read request."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that JESD79, Release 1, purports to relate to certain DDR SDRAM devices. Rambus further admits that page 8 of JESD79, Release 1, states in part:

"The Mode Register is used to define the specific mode of operation of the DDR SDRAM. This definition includes the selection of a burst length . . . .

"Mode Register bits A0-A2 specify the burst length . . . . "

Rambus further admits that Figure 1 on page 9 of JESD79, Release 1, shows a representation of a "Mode Register" with bits A0-A2 designated as "Burst Length."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 56:**

Admit that section 3.11.5.5 of JEDEC Standard No. 21-C, Release 4, describes auto precharge.

**RESPONSE TO REQUEST FOR ADMISSION NO. 56:**

Rambus objects to this request on the grounds that it is vague and ambiguous with respect to the term "auto precharge"

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that section 3.11.5.5 of JEDEC Standard No. 21-C, Release 4, is headed "Auto Precharge" and purports to describe that feature.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 57:**

Admit that section 3.11.5.1.5 of JEDEC Standard No. 21-C, Release 9, describes auto precharge.

**RESPONSE TO REQUEST FOR ADMISSION NO. 57:**

Rambus objects to this request on the grounds that it is vague and ambiguous with respect to the term "auto precharge"

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that section 3.11.5.5 of JEDEC Standard No. 21-C, Release 9, is headed "Auto Precharge" and purports to describe that feature.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 58:**

Admit that the table contained in section 3.11.5.5 of JEDEC Standard No. 21-C, Release 4, defines the auto precharge options available during the column portion of any cycle.

**RESPONSE TO REQUEST FOR ADMISSION NO. 58:**

Rambus objects to this request on the grounds that it is vague and ambiguous at least with respect to the terms "auto precharge," "column portion," and "any cycle."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that section 3.11.5.5 of JEDEC Standard No. 21-C, Release 4, contains a

table, described as "defin[ing] the options available from A10 during the column address portion of any cycle," indicating the following two options: "Do not auto precharge, leave bank active at end of burst," and "Auto precharge bank specified by A11 at end of burst."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 59:**

Admit that the table contained in section 3.11.5.1.5 of JEDEC Standard No. 21-C, Release 9, defines the auto precharge options available during the column portion of any cycle.

**RESPONSE TO REQUEST FOR ADMISSION NO. 59:**

Rambus objects to this request on the grounds that it is vague and ambiguous at least with respect to the terms "auto precharge," "column portion," and "any cycle."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that section 3.11.5.1.5 of JEDEC Standard No. 21-C, Release 9, contains a table, described as "defin[ing] the options available from AP during the column address portion of any cycle," indicating the following two options: "Do not auto precharge, leave bank active at end of burst," and "Auto precharge bank specified by BA at end of burst."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 60:**

Admit that, to comply with JEDEC Standard No. 21-C, an SDRAM device must contain the auto precharge options described in section 3.11.5.5 of Release 4.

**RESPONSE TO REQUEST FOR ADMISSION NO. 60:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JEDEC Standard No. 21-C is the subject of the request, which part of JEDEC Standard No. 21-C is the subject of the request and the term "auto precharge options."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Section 3.11.5.5 of JEDEC Standard No. 21-C, Release 4, headed "Auto Precharge" did purport to relate to certain SDRAM devices and contains a table, described as "defin[ing] the options available from A10 during the column address portion of any cycle," indicating the following two options: "Do not auto precharge, leave bank active at end of burst," and "Auto precharge bank specified by A11 at end of burst."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 61:**

Admit that, to comply with JEDEC Standard No. 21-C, an SDRAM device must contain the auto precharge options described in section 3.11.5.1.5 of Release 9.

**RESPONSE TO REQUEST FOR ADMISSION NO. 61:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JEDEC Standard No. 21-C is the subject of the request, which part of JEDEC Standard No. 21-C is the subject of the request and the term "auto precharge options."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Section 3.11.5.1.5 of JEDEC Standard No. 21-C, Release 9, headed "Auto Precharge" did purport to relate to, *inter alia*, certain SDRAM devices and contains a table, described as "defin[ing] the options available from AP during the column address portion of any cycle," indicating the following two options: "Do not auto precharge, leave bank active at end of burst," and "Auto precharge bank specified by BA at end of burst."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 62:**

Admit that, to comply with JEDEC Standard No. 21-C, a DDR SDRAM device must contain the auto precharge options described in section 3.11.5.1.5.

**RESPONSE TO REQUEST FOR ADMISSION NO. 62:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JEDEC Standard No. 21-C is the subject of the request, which part of JEDEC Standard No. 21-C is the subject of the request and the term "auto precharge options."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Section 3.11.5.1.5 of JEDEC Standard No. 21-C, Release 9, headed "Auto Precharge" did purport to relate to, *inter alia*, certain DDR SDRAM devices and contains a table, described as "defin[ing] the options available from AP during the column address portion of any cycle," indicating the following two options: "Do not auto precharge, leave bank active at end of burst," and "Auto precharge bank specified by BA at end of burst."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 63:**

Admit that, to comply with JEDEC Standard No. 21-C, an SDRAM device must be able to respond to information sent along with a read request instructing it to automatically precharge bank(s) after each read request.

**RESPONSE TO REQUEST FOR ADMISSION NO. 63:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JEDEC Standard No. 21-C is the subject of the request, which part of JEDEC Standard No. 21-C is the subject of the request, and the terms "able to respond," "automatically precharge bank(s)," and "after each read request."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Section 3.11.5.1.5 of JEDEC Standard No. 21-C, Release 9, headed "Auto Precharge" did purport to relate to, *inter alia*, certain SDRAM devices and states, in part: "The user may specify that the bank currently being accessed precharge itself as soon as the burst is completed. This is done using the address bit AP during the column address cycle."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 64:**

Admit that, to comply with JEDEC Standard No. 21-C, an SDRAM device must have the ability to internally precharge a bank without first receiving a separate precharge command.

**RESPONSE TO REQUEST FOR ADMISSION NO. 64:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JEDEC Standard No. 21-C is the subject of the request, which part of JEDEC Standard No. 21-C is the subject of the request, and the terms "internally precharge a bank" and "separate precharge command."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Section 3.11.5.1.5 of JEDEC Standard No. 21-C, Release 9, headed "Auto Precharge" did purport to relate to, *inter alia*, certain SDRAM devices and states, in part: "The user may specify that the bank currently being accessed precharge itself as soon as the burst is completed. This is done using the address bit AP during the column address cycle."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 65:**

Admit that, to comply with JEDEC Standard No. 21-C, a DDR SDRAM device must be able to respond to information sent along with a read request instructing it to automatically precharge bank(s) for the next each read request.

**RESPONSE TO REQUEST FOR ADMISSION NO. 65:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JEDEC Standard No. 21-C is the subject of the request, which part of JEDEC Standard No. 21-C is the subject of the request, and the terms "able to respond," "automatically precharge bank(s)," and "next each read request."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Section 3.11.5.1.5 of JEDEC Standard No. 21-C, Release 9, headed "Auto Precharge" did purport to relate to, *inter alia*, certain DDR SDRAM devices and states, in part: "The user may specify that the bank currently being accessed precharge itself as soon as the burst is completed. This is done using the address bit AP during the column address cycle."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 66:**

Admit that, to comply with JEDEC Standard No. 21-C, a DDR SDRAM device must have the ability to internally precharge a bank without first receiving a separate precharge command.

**RESPONSE TO REQUEST FOR ADMISSION NO. 66:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JEDEC Standard No. 21-C is the subject of the request, which part of JEDEC Standard No. 21-C is the subject of the request, and the terms "internally precharge a bank" and "separate precharge command."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Section 3.11.5.1.5 of JEDEC Standard No. 21-C, Release 9, headed "Auto Precharge" did purport to relate to, *inter alia*, certain DDR SDRAM devices and states, in part: "The user may specify that the bank currently being accessed precharge itself as soon as the burst is completed. This is done using the address bit AP during the column address cycle."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 67:**

Admit that the JEDEC Double Data Rate (DDR) SDRAM Specification, JESD79, page 14, describes auto precharge.

**RESPONSE TO REQUEST FOR ADMISSION NO. 67:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least

with respect to which version of JESD79 is the subject of the request and the term "auto precharge."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that JESD79, Release 1, contains a section headed "Auto Precharge" on page 14 which purports to describe an "auto precharge" feature.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 68:**

Admit that the table contained in the JEDEC Double Data Rate (DDR) SDRAM Specification, JESD79, page 14, defines the auto precharge options available during the column portion of any cycle.

**RESPONSE TO REQUEST FOR ADMISSION NO. 68:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JESD79 is the subject of the request and the terms "auto precharge," "column portion," and "cycle."

Subject to and without waiving any objections, Rambus responds as follows:

There is no table on page 14 of JESD79, Release 1.

Rambus denies the request.

**REQUEST FOR ADMISSION NO. 69:**

Admit that, to comply with the JEDEC Double Data Rate (DDR) SDRAM Specification, JESD79, an SDRAM device must contain the auto precharge feature described at page 14.

**RESPONSE TO REQUEST FOR ADMISSION NO. 69:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JESD79 is the subject of the request and the term "SDRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that JESD79, Release 1, purports to relate to certain DDR SDRAM devices. Rambus further admits that page 8 of JESD79, Release 1, contains a section headed "Auto Precharge" on page 14 which purports to describe an "auto precharge" feature.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 70:**

Admit that, to comply with the JEDEC Double Data Rate (DDR) SDRAM Specification, JESD79, a DDR SDRAM device must permit the user to use A10 to enable auto precharge in conjunction with a specific read or write command.

**RESPONSE TO REQUEST FOR ADMISSION NO. 70:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JESD79 is the subject of the request and the terms "user," "auto precharge," and "read or write command."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that JESD79, Release 1, purports to relate to certain DDR SDRAM devices. Rambus further admits that page 8 of JESD79, Release 1, contains a section headed "Auto Precharge" on page 14 which states in part:

"AUTO PRECHARGE is a feature which performs the same individual-bank precharge function described above, but without requiring an explicit command. This is accomplished by using A10 to enable AUTO PRECHARGE in conjunction with a specific READ or WRITE command."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 71:**

Admit that, to comply with the JEDEC Double Data Rate (DDR) SDRAM Specification, JESD79, a DDR SDRAM device must permit the user to perform automatically, upon completion of the read or write burst, a precharge of the bank/row that is addressed with the read

or write command.

**RESPONSE TO REQUEST FOR ADMISSION NO. 71:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JESD79 is the subject of the request and the terms "user," "automatically," "bank/row," "the read or write burst," and "the read or write command."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that JESD79, Release 1, purports to relate to certain DDR SDRAM devices. Rambus further admits that page 8 of JESD79, Release 1, contains a section headed "Auto Precharge" on page 14 which states in part:

"AUTO PRECHARGE is a feature which performs the same individual-bank precharge function described above, but without requiring an explicit command. This is accomplished by using A10 to enable AUTO PRECHARGE in conjunction with a specific READ or WRITE command. A precharge of the bank/row that is addressed with the READ or WRITE command is automatically performed upon completion of the READ or WRITE burst."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 72:**

Admit that, to comply with the JEDEC Double Data Rate (DDR) SDRAM Specification, JESD79, a DDR SDRAM device must be able to respond to information sent along with a read request instructing it to automatically precharge bank(s) after each read request.

**RESPONSE TO REQUEST FOR ADMISSION NO. 72:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JESD79 is the subject of the request and the terms "respond to information," "read request," "automatically precharge bank(s)," and "after each read request."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that JESD79, Release 1, purports to relate to certain DDR SDRAM devices. Rambus further admits that page 8 of JESD79, Release 1, contains a section headed

"Auto Precharge" on page 14 which states in part:

"AUTO PRECHARGE is a feature which performs the same individual-bank precharge function described above, but without requiring an explicit command. This is accomplished by using A10 to enable AUTO PRECHARGE in conjunction with a specific READ or WRITE command. A precharge of the bank/row that is addressed with the READ or WRITE command is automatically performed upon completion of the READ or WRITE burst."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 73:**

Admit that, to comply with the JEDEC Double Data Rate (DDR) SDRAM Specification, JESD79, a DDR SDRAM device must have the ability to internally precharge a bank without first receiving a separate precharge command.

**RESPONSE TO REQUEST FOR ADMISSION NO. 73:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JESD79 is the subject of the request and the terms "internally precharge a bank" and "separate precharge command."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that JESD79, Release 1, purports to relate to certain DDR SDRAM devices. Rambus further admits that page 8 of JESD79, Release 1, contains a section headed "Auto Precharge" on page 14 which states in part:

"AUTO PRECHARGE is a feature which performs the same individual-bank precharge function described above, but without requiring an explicit command."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 74:**

Admit that, to comply with the JEDEC Double Data Rate (DDR) SDRAM Specification, JESD79, a DDR SDRAM device must be able to respond to information sent along with a read

request instructing it to automatically precharge bank(s) for the next each read request.

**RESPONSE TO REQUEST FOR ADMISSION NO. 74:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JESD79 is the subject of the request and the terms "respond to information," "read request," "automatically precharge bank(s)," and "next each read request."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that JESD79, Release 1, purports to relate to certain DDR SDRAM devices. Rambus further admits that page 8 of JESD79, Release 1, contains a section headed "Auto Precharge" on page 14 which states in part:

"AUTO PRECHARGE is a feature which performs the same individual-bank precharge function described above, but without requiring an explicit command. This is accomplished by using A10 to enable AUTO PRECHARGE in conjunction with a specific READ or WRITE command. A precharge of the bank/row that is addressed with the READ or WRITE command is automatically performed upon completion of the READ or WRITE burst."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 75:**

Admit that, to comply with the JEDEC Double Data Rate (DDR) SDRAM Specification, JESD79, a DDR SDRAM device must have the ability to internally precharge a bank without first receiving a separate precharge command.

**RESPONSE TO REQUEST FOR ADMISSION NO. 75:**

Rambus objects to this request as being duplicative of Request No. 73, and incorporates its objections and response thereto.

**REQUEST FOR ADMISSION NO. 76:**

Admit that section 3.11.5.2.9 of JEDEC Standard No. 21-C shows output of a first portion of data in response to a rising edge of a clock signal and a second portion of data in

response to a falling edge of a clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 76:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JEDEC Standard No. 21-C is the subject of the request and the terms "first portion of data," "second portion of data," "in response to," and "a clock signal."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Section 3.11.5.2.9 of certain versions of JEDEC Standard No. 21-C states: "The signal DQS shall be coincident with Read Data from the DDR SDRAM device. The timing diagram below shows the nominal relationship between data and DQS for read data at the output of the DDR SDRAM devices." Rambus further admits that Section 3.11.5.2.9 shows an idealized timing diagram including signals designated "CK (External)" and "Clock (Internal or Differential)," as well as "DQ (Output)." DQ is shown as transitioning coincident with rising and falling edges of DQS which, on this diagram, are shown as aligned with edges of CK and Clock.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 77:**

Admit that, to comply with JEDEC Standard No. 21-C, a DDR SDRAM device must output data as described in section 3.11.5.2.9.

**RESPONSE TO REQUEST FOR ADMISSION NO. 77:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JEDEC Standard No. 21-C is the subject of the request, which part of JEDEC Standard No. 21-C is the subject of the request, and what the designated section "describe[s]" with respect to data output.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 78:**

Admit that, to comply with JEDEC Standard No. 21-C, a DDR SDRAM device must output a first portion of data in response to a rising edge of a clock signal and a second portion of data in response to a falling edge of a clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 78:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JEDEC Standard No. 21-C is the subject of the request, which part of JEDEC Standard No. 21-C is the subject of the request, and the terms "first portion of data," "second portion of data," "in response to," and "a clock signal."

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 79:**

Admit that section 3.11.5.2.9 of JEDEC Standard No. 21-C shows input of a first portion of data in response to a rising edge of a clock signal and a second portion of data in response to a falling edge of a clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 79:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JEDEC Standard No. 21-C is the subject of the request, which part of JEDEC Standard No. 21-C is the subject of the request, and the terms "first portion of data," "second portion of data," "in response to," and "a clock signal."

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 80:**

Admit that, to comply with JEDEC Standard No. 21-C, a DDR SDRAM device must input data as described in section 3.11.5.2.9.

**RESPONSE TO REQUEST FOR ADMISSION NO. 80:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JEDEC Standard No. 21-C is the subject of the request, which part of JEDEC Standard No. 21-C is the subject of the request, and what the designated section "describe[s]" with respect to data input.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 81:**

Admit that, to comply with JEDEC Standard No. 21-C, a DDR SDRAM device must input a first portion of data in response to a rising edge of a clock signal and a second portion of data in response to a falling edge of a clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 81:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JEDEC Standard No. 21-C is the subject of the request, which part of JEDEC Standard No. 21-C is the subject of the request, and the terms "first portion of data," "second portion of data," "in response to," and "a clock signal."

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 82:**

Admit that, to comply with JEDEC Standard No. 21-C, a DDR SDRAM device must output a first portion of data synchronously with respect to a rising edge of an external clock signal and a second portion of data synchronously with respect to a falling edge of the external clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 82:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least

with respect to which version of JEDEC Standard No. 21-C is the subject of the request, which part of JEDEC Standard No. 21-C is the subject of the request, and the terms "first portion of data", "second portion of data," and "synchronously."

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 83:**

Admit that section 3.11.5.2.9 of JEDEC Standard No. 21-C shows data output occurring synchronously with respect to both the rising edge of the external clock signal and the falling edge of the external clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 83:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JEDEC Standard No. 21-C is the subject of the request and the terms "synchronously" and "external clock signal."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Section 3.11.5.2.9 of certain versions of JEDEC Standard No. 21-C states: "The signal DQS shall be coincident with Read Data from the DDR SDRAM device. The timing diagram below shows the nominal relationship between data and DQS for read data at the output of the DDR SDRAM devices." Rambus further admits that Section 3.11.5.2.9 shows an idealized timing diagram including signals designated "CK (External)" and "Clock (Internal or Differential)," as well as "DQ (Output)." DQ is shown as transitioning coincident with rising and falling edges of DQS which, on this diagram, are shown as aligned with edges of CK and Clock.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 84:**

Admit that, to comply with JEDEC Standard No. 21-C, a DDR SDRAM device must

input a first portion of data synchronously with respect to a rising edge of an external clock signal and a second portion of data synchronously with respect to a falling edge of the external clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 84:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JEDEC Standard No. 21-C is the subject of the request, which part of JEDEC Standard No. 21-C is the subject of the request, and the terms "first portion of data," "second portion of data," "external clock signal," and "synchronously."

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 85:**

Admit that section 3.11.5.2.9 of JEDEC Standard No. 21-C shows data input occurring synchronously with respect to both the rising edge of the external clock signal and the falling edge of the external clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 85:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JEDEC Standard No. 21-C is the subject of the request and the terms "external clock signal" and "synchronously."

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 86:**

Admit that, to comply with JEDEC Standard No. 21-C, a DDR SDRAM device must output a first portion of data synchronously with respect to a first external clock signal and a second portion of data synchronously with respect to a second external clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 86:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JEDEC Standard No. 21-C is the subject of the request, which part of JEDEC Standard No. 21-C is the subject of the request, and the terms "first portion of data," "second portion of data," "first external clock signal," "second external clock signal," and "synchronously."

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 87:**

Admit that section 3.11.5.2.9 of JEDEC Standard No. 21-C shows data output occurring synchronously with respect to a both a first external clock signal and a second external clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 87:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JEDEC Standard No. 21-C is the subject of the request and the terms "first external clock signal," "second external clock signal," and "synchronously."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Section 3.11.5.2.9 of certain versions of JEDEC Standard No. 21-C states: "The signal DQS shall be coincident with Read Data from the DDR SDRAM device. The timing diagram below shows the nominal relationship between data and DQS for read data at the output of the DDR SDRAM devices." Rambus further admits that Section 3.11.5.2.9 shows an idealized timing diagram including signals designated "CK (External)" and "Clock (Internal or Differential)," as well as "DQ (Output)." DQ is shown as transitioning coincident with rising and falling edges of DQS which, on this diagram, are shown as aligned with edges of CK and Clock.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 88:**

Admit that, to comply with JEDEC Standard No. 21-C, a DDR SDRAM device must input a first portion of data synchronously with respect to a first external clock signal and a second portion of data synchronously with respect to a second external clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 88:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JEDEC Standard No. 21-C is the subject of the request, which part of JEDEC Standard No. 21-C is the subject of the request, and the terms "first portion of data," "second portion of data," "first external clock signal," "second external clock signal," and "synchronously."

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 89:**

Admit that section 3.11.5.2.9 of JEDEC Standard No. 21-C shows data input occurring synchronously with respect to both a first and a second external clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 89:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JEDEC Standard No. 21-C is the subject of the request and the terms "first and a second external clock signal" and "synchronously."

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 90:**

Admit that, to comply with JEDEC Standard No. 21-C, a DDR SDRAM device must use a dual edge clocking scheme which inputs and outputs data synchronously with the rising and

falling edge of an external clock.

**RESPONSE TO REQUEST FOR ADMISSION NO. 90:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JEDEC Standard No. 21-C is the subject of the request and the terms "dual edge clocking scheme," "the rising and falling edge," "external clock signal," and "synchronously."

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 91:**

Admit that section 3.11.5.2.9 of JEDEC Standard No. 21-C shows data input and output occurring synchronously with the rising and falling edge of an external clock, according to a dual edge clocking scheme.

**RESPONSE TO REQUEST FOR ADMISSION NO. 91:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JEDEC Standard No. 21-C is the subject of the request and the terms "dual edge clocking scheme," "the rising and falling edge," "external clock signal," and "synchronously." Rambus further objects to this request on the ground that it is compound.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 92:**

Admit that Figure 44 of the JEDEC Double Data Rate (DDR) SDRAM Specification, JESD79, page 67, shows output of a first portion of data in response to a rising edge of a clock signal and a second portion of data in response to a falling edge of a clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 92:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least

with respect to which version of JESD79 is the subject of the request and the terms "first portion of data," "second portion of data," "in response to," and "a clock signal."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Figure 44 on page 67 of JESD79, Release 1, shows a timing diagram indicating data output (DQ) beginning in a window of time about the intersection of a rising edge of one clock signal (CK) with a falling edge of another (/CK), and subsequent data output beginning in a similar window about the intersection of a falling edge of CK with a rising edge of /CK. The time window is shown as beginning at $t_{LZ}$(min) (identified as -0.75 nanoseconds for certain DDR SDRAM devices on page 59 of JESD79, Release 1)) prior to the intersection point and ending at $t_{LZ}$(max) (identified as +0.75 nanoseconds for certain DDR SDRAM devices on page 59 of JESD79, Release 1)) after the intersection point.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 93:**

Admit that, to comply with Figure 44 of the JEDEC Double Data Rate (DDR) SDRAM Specification, JESD79, a DDR SDRAM device must output data as shown on page 67.

**RESPONSE TO REQUEST FOR ADMISSION NO. 93:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JESD79 is the subject of the request, what it means to "comply with" a figure, and, to the extent that the request is intended refer to JESD79, Release 1, which of the two "cases" of data output shown on Figure 44 is the subject of the request.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 94:**

Admit that, to comply with Figure 44 of the JEDEC Double Data Rate (DDR) SDRAM Specification, JESD79, page 67, a DDR SDRAM device must output a first portion of data in

response to a rising edge of a clock signal and a second portion of data in response to a falling edge of a clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 94:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JESD79 is the subject of the request, what it means to "comply with" a figure, to the extent that the request is intended refer to JESD79, Release 1, which of the two "cases" of data output shown on Figure 44 is the subject of the request, and the terms "first portion of data," "second portion of data," "in response to," and "a clock signal."

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 95:**

Admit that to comply with JEDEC Double Data Rate (DDR) SDRAM Specification, JESD79, page 28, shows input of a first portion of data in response to a rising edge of a data strobe and a second portion of data in response to a falling edge of a data strobe.

**RESPONSE TO REQUEST FOR ADMISSION NO. 95:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JESD79 is the subject of the request and the terms "first portion of data," "second portion of data," "in response to," and "a data strobe." Rambus further objects to the request as unintelligible.

**REQUEST FOR ADMISSION NO. 96:**

Admit that, to comply with JEDEC Double Data Rate (DDR) SDRAM Specification, JESD79, page 28, a DDR SDRAM device must input data as described on page 28.

**RESPONSE TO REQUEST FOR ADMISSION NO. 96:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JESD79 is the subject of the request, what it means to "comply

with" a single page of a specification, and to the extent that the request is intended refer to JESD79, Release 1, what is "described" with regard to data input in this diagram.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 97:**

Admit that, to comply with JEDEC Double Data Rate (DDR) SDRAM Specification, JESD79, page 28, a DDR SDRAM device must input a first portion of data in response to a rising edge of a data strobe and a second portion of data in response to a falling edge of a data strobe.

**RESPONSE TO REQUEST FOR ADMISSION NO. 97:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JESD79 is the subject of the request, what it means to "comply with" a single page of a specification, and the terms "first portion of data," "second portion of data," "in response to," and "a data strobe."

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 98:**

Admit that, to comply with Figure 44 of the JEDEC Double Data Rate (DDR) SDRAM Specification, JESD79, page 67, a DDR SDRAM device must output a first portion of data synchronously with respect to a rising edge of an external clock signal and a second portion of data synchronously with respect to a falling edge of the external clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 98:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JESD79 is the subject of the request, what it means to "comply with" a figure, to the extent that the request is intended refer to JESD79, Release 1, which of the

two "cases" of data output shown on Figure 44 is the subject of the request, and the terms "first portion of data," "second portion of data," "external clock signal," and "synchronously."

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 99:**

Admit that Figure 44 of the JEDEC Double Data Rate (DDR) SDRAM Specification, JESD79, page 67, shows data output occurring synchronously with respect to both the rising edge of the external clock signal and the falling edge of the external clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 99:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JESD79 is the subject of the request and the terms "external clock signal" and "synchronously."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Figure 44 on page 67 of JESD79, Release 1, shows a timing diagram indicating data output (DQ) beginning in a window of time about the intersection of a rising edge of one clock signal (CK) with a falling edge of another (/CK), and subsequent data output beginning in a similar window about the intersection of a falling edge of CK with a rising edge of /CK. The time window is shown as beginning at $t_{LZ}$(min) (identified as -0.75 nanoseconds for certain DDR SDRAM devices on page 59 of JESD79, Release 1)) prior to the intersection point and ending at $t_{LZ}$(max) (identified as +0.75 nanoseconds for certain DDR SDRAM devices on page 59 of JESD79, Release 1)) after the intersection point.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 100:**

Admit that, to comply with JEDEC Double Data Rate (DDR) SDRAM Specification, JESD79, page 28, a DDR SDRAM device must input a first portion of data synchronously with

respect to a rising edge of an external clock signal and a second portion of data synchronously with respect to a falling edge of the external clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 100:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JESD79 is the subject of the request, what it means to "comply with" a single page of a specification, and the terms "first portion of data," "second portion of data," "external clock signal," and "synchronously."

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 101:**

Admit that JEDEC Double Data Rate (DDR) SDRAM Specification, JESD79, page 28, shows data input occurring synchronously with respect to both the rising edge of the external clock signal and the falling edge of the external clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 101:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JESD79 is the subject of the request and the terms "external clock signal" and "synchronously."

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 102:**

Admit that, to comply with Figure 44 of the JEDEC Double Data Rate (DDR) SDRAM Specification, JESD79, page 67, a DDR SDRAM device must output a first portion of data synchronously with respect to a first external clock signal and a second portion of data synchronously with respect to a second external clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 102:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JESD79 is the subject of the request, what it means to "comply with" a figure, to the extent that the request is intended refer to JESD79, Release 1, which of the two "cases" of data output shown on Figure 44 is the subject of the request, and the terms "first portion of data," "second portion of data," "first external clock signal," "second external clock signal," and "synchronously."

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 103:**

Admit that Figure 44 of the JEDEC Double Data Rate (DDR) SDRAM Specification, JESD79, page 67, shows data output occurring synchronously with respect to a both a first external clock signal and a second external clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 103:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JESD79 is the subject of the request and the terms "first external clock signal," "second external clock signal," and "synchronously."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Figure 44 on page 67 of JESD79, Release 1, shows a timing diagram indicating data output (DQ) beginning in a window of time about the intersection of a rising edge of one clock signal (CK) with a falling edge of another (/CK), and subsequent data output beginning in a similar window about the intersection of a falling edge of CK with a rising edge of /CK. The time window is shown as beginning at $t_{LZ}$(min) (identified as -0.75 nanoseconds for certain DDR SDRAM devices on page 59 of JESD79, Release 1)) prior to the intersection point and ending at $t_{LZ}$(max) (identified as +0.75 nanoseconds for certain DDR SDRAM devices on page 59 of JESD79, Release 1)) after the intersection point.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 104:**

Admit that, to comply with JEDEC Double Data Rate (DDR) SDRAM Specification, JESD79, page 28, a DDR SDRAM device must input a first portion of data synchronously with respect to a first external clock signal and a second portion of data synchronously with respect to a second external clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 104:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JESD79 is the subject of the request, what it means to "comply with" a single page of a specification, and the terms "first portion of data," "second portion of data," "first external clock signal," "second external clock signal," and "synchronously."

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 105:**

Admit that JEDEC Double Data Rate (DDR) SDRAM Specification, JESD79, page 28, shows data input occurring synchronously with respect to both a first and a second external clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 105:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JESD79 is the subject of the request and the terms "a first and second external clock signal" and "synchronously."

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 106:**

Admit that, to comply with JEDEC Double Data Rate (DDR) SDRAM Specification, JESD79, a DDR SDRAM device must use a dual edge clocking scheme which inputs and outputs data synchronously with the rising and falling edge of an external clock.

**RESPONSE TO REQUEST FOR ADMISSION NO. 106:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JESD79 is the subject of the request and the terms "dual edge clocking scheme," "the rising and falling edge," and "synchronously."

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 107:**

Admit that JEDEC Double Data Rate (DDR) SDRAM Specification, JESD79, page 28, shows data input and output occurring synchronously with the rising and falling edge of an external clock, according to a dual edge clocking scheme.

**RESPONSE TO REQUEST FOR ADMISSION NO. 107:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JESD79 is the subject of the request and the terms "dual edge clocking scheme," "the rising and falling edge," and "synchronously."

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 108:**

Admit that section 3.11.5.2.11 of JEDEC Standard No. 21-C, Release 9, shows DLL enable/disable mode for DDR SDRAMs.

**RESPONSE TO REQUEST FOR ADMISSION NO. 108:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least

with respect to the term "DLL enable/disable mode."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Section 3.11.5.2.11 of JEDEC Standard No. 21-C, Release 9, purports to relate to, *inter alia*, certain DDR SDRAM devices and purports to define "the DLL disable/enable bit in the Extended Mode Register" for those devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 109:**

Admit that section 3.11.5.2.11 of JEDEC Standard No. 21-C, Release 9, contains an extended mode register definition containing a DLL enable/disable bit.

**RESPONSE TO REQUEST FOR ADMISSION NO. 109:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "extended mode register definition" and "DLL enable/disable bit."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Section 3.11.5.2.11 of JEDEC Standard No. 21-C, Release 9, refers to an extended mode register and purports to define "the DLL disable/enable bit in the Extended Mode Register."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 110:**

Admit that section 3.11.5.2.11 of JEDEC Standard No. 21-C, Release 9, shows a bit contained in the mode register that operates to enable and disable an on-chip DLL.

**RESPONSE TO REQUEST FOR ADMISSION NO. 110:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "mode register," "operates," and "on-chip DLL"

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Section 3.11.5.2.11 of JEDEC Standard No. 21-C, Release 9, refers

to an extended mode register and purports to define "the DLL disable/enable bit in the Extended Mode Register." The Section indicates that if this bit set to 0 corresponds to "DLL enable," and this bit set to 1 corresponds to "DLL disable."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 111:**

Admit that section 3.11.5.2.11 of JEDEC Standard No. 21-C, Release 9, contains an extended mode register definition containing an enable/disable bit for delay locked loop circuitry to generate an internal clock signal using an external clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 111:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "extended mode register definition," "enable/disable bit," "delay locked loop circuitry" and "generate an internal clock signal using an external clock signal."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Section 3.11.5.2.11 of JEDEC Standard No. 21-C, Release 9, refers to an extended mode register and purports to define "the DLL disable/enable bit in the Extended Mode Register." Rambus further admits that "DLL" is often used as an acronym for "delay locked loop."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 112:**

Admit that section 3.11.5.2.11 of JEDEC Standard No. 21-C, Release 9, shows a bit contained in the mode register that operates to enable and disable delay locked loop circuitry to generate an internal clock signal using an external clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 112:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "mode register," "operates," "delay locked loop circuitry" and

"generate an internal clock signal using an external clock signal."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Section 3.11.5.2.11 of JEDEC Standard No. 21-C, Release 9, refers to an extended mode register and purports to define "the DLL disable/enable bit in the Extended Mode Register." Rambus further admits that "DLL" is often used as an acronym for "delay locked loop."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 113:**

Admit that, to comply with JEDEC Standard No. 21-C, Release 9, a DDR SDRAM device must contain an extended mode register as defined in section 3.11.5.2.11.

**RESPONSE TO REQUEST FOR ADMISSION NO. 113:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which part of JEDEC Standard No. 21-C is the subject of the request.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 114:**

Admit that, to comply with JEDEC Standard No. 21-C, Release 9, a DDR SDRAM device must contain an extended mode register definition containing a DLL enable/disable bit.

**RESPONSE TO REQUEST FOR ADMISSION NO. 114:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which part of JEDEC Standard No. 21-C is the subject of the request and the terms "extended mode register definition" and "DLL enable/disable bit."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Section 3.11.5.2.11 of JEDEC Standard No. 21-C, Release 9, purports to relate, *inter alia*, to certain DDR SDRAM devices. Rambus further admits that that

section refers to an extended mode register and purports to define "the DLL disable/enable bit in the Extended Mode Register."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 115:**

Admit that, to comply with JEDEC Standard No. 21-C, Release 9, a DDR SDRAM device must contain a bit in the mode register that operates to enable and disable an on-chip DLL.

**RESPONSE TO REQUEST FOR ADMISSION NO. 115:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which part of JEDEC Standard No. 21-C is the subject of the request and the terms "mode register," "operates," and "on-chip DLL."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Section 3.11.5.2.11 of JEDEC Standard No. 21-C, Release 9, purports to relate, *inter alia*, to certain DDR SDRAM devices. Rambus further admits that this section refers to an extended mode register and purports to define "the DLL disable/enable bit in the Extended Mode Register." The Section indicates that if this bit set to 0 corresponds to "DLL enable," and this bit set to 1 corresponds to "DLL disable."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 116:**

Admit that, to comply with JEDEC Standard No. 21-C, Release 9, a DDR SDRAM device must contain an extended mode register definition containing an enable/disable bit for delay locked loop circuitry to generate an internal clock signal using an external clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 116:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which part of JEDEC Standard No. 21-C is the subject of the request and the

terms “extended mode register definition,” “enable/disable bit,” “delay locked loop circuitry” and “generate an internal clock signal using an external clock signal.”

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Section 3.11.5.2.11 of JEDEC Standard No. 21-C, Release 9, purports to relate, *inter alia*, to certain DDR SDRAM devices. Rambus further admits that this section refers to an extended mode register and purports to define “the DLL disable/enable bit in the Extended Mode Register.” Rambus further admits that “DLL” is often used as an acronym for “delay locked loop.”

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 117:**

Admit that, to comply with JEDEC Standard No. 21-C, Release 9, a DDR SDRAM device must contain a bit in the mode register that operates to enable and disable delay locked loop circuitry to generate an internal clock signal using an external clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 117:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which part of JEDEC Standard No. 21-C is the subject of the request and the terms “mode register,” “operates,” “delay locked loop circuitry” and “generate an internal clock signal using an external clock signal.”

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Section 3.11.5.2.11 of JEDEC Standard No. 21-C, Release 9, refers to an extended mode register and purports to define “the DLL disable/enable bit in the Extended Mode Register.” Rambus further admits that “DLL” is often used as an acronym for “delay locked loop.”

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 118:**

Admit that, to comply with JEDEC Standard No. 21-C, Release 9, a DDR SDRAM device must contain a PLL or a DLL on the DRAM which can be used to ensure that the data strobe and data coming off of a DRAM chip are sufficiently synchronized to the system clock so that the memory controller can capture that data.

**RESPONSE TO REQUEST FOR ADMISSION NO. 118:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which part of JEDEC Standard No. 21-C is the subject of the request and the terms "PLL," "DLL," "can be used," "data strobe," "a DRAM chip," and "sufficiently synchronized."

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 119:**

Admit that, to comply with JEDEC Standard No. 21-C, a DDR SDRAM device must contain delay locked loop circuitry to generate an internal clock signal using an external clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 119:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JEDEC Standard No. 21-C is the subject of the request, which part of JEDEC Standard No. 21-C is the subject of the request, and the terms "delay locked loop circuitry" and "generate an internal clock signal using an external clock signal."

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 120:**

Admit that a delay lock loop is a type of phase lock loop.

**RESPONSE TO REQUEST FOR ADMISSION NO. 120:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "delay lock loop" and "phase lock loop."

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 121:**

Admit that the JEDEC Double Data Rate (DDR) SDRAM Specification, JESD79, page 12, shows DLL enable/disable mode for DDR SDRAMs.

**RESPONSE TO REQUEST FOR ADMISSION NO. 121:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JESD79 is the subject of the request and the term "DLL enable/disable mode."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that JESD79, Release 1, purports to relate to certain DDR SDRAM devices. Rambus further admits that page 12 of JESD79, Release 1, states that "[t]he Extended Mode Register controls functions beyond those controlled by the Mode Register; these additional functions include DLL enable/disable . . . ." and that Figure 3 on that page, entitled "Extended Mode Register Definition" shows a representation of an Extended Mode Register that indicates that bit A0 equal to 0 corresponds to DLL enable and that bit A0 equal to 1 corresponds to DLL disable.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 122:**

Admit that the JEDEC Double Data Rate (DDR) SDRAM Specification, JESD79, page 12 contains an extended mode register definition containing a DLL enable/disable bit.

**RESPONSE TO REQUEST FOR ADMISSION NO. 122:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JESD79 is the subject of the request and the terms "extended mode register definition" and "DLL enable/disable bit."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that page 12 of JESD79, Release 1, states that "[t]he Extended Mode Register controls functions beyond those controlled by the Mode Register; these additional functions include DLL enable/disable . . . ." and that Figure 3 on that page, entitled "Extended Mode Register Definition" shows a representation of an Extended Mode Register that indicates that bit A0 equal to 0 corresponds to DLL enable and that bit A0 equal to 1 corresponds to DLL disable.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 123:**

Admit that the JEDEC Double Data Rate (DDR) SDRAM Specification, JESD79, page 12, shows a bit contained in the mode register that operates to enable and disable an on-chip DLL.

**RESPONSE TO REQUEST FOR ADMISSION NO. 123:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JESD79 is the subject of the request and the terms "mode register," "operates," and "on-chip DLL."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that page 12 of JESD79, Release 1, states that "[t]he Extended Mode Register controls functions beyond those controlled by the Mode Register; these additional functions include DLL enable/disable . . . ." and that Figure 3 on that page, entitled "Extended Mode Register Definition" shows a representation of an Extended Mode Register that indicates that bit A0 equal to 0 corresponds to DLL enable and that bit A0 equal to 1 corresponds to DLL

disable.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 124:**

Admit that the JEDEC Double Data Rate (DDR) SDRAM Specification, JESD79, page 12, contains an extended mode register definition containing an enable/disable bit for delay locked loop circuitry to generate an internal clock signal using an external clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 124:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JESD79 is the subject of the request and the terms "extended mode register definition," "enable/disable bit," "delay locked loop circuitry," and "generate an internal clock signal using an external clock signal."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that page 12 of JESD79, Release 1, states that "[t]he Extended Mode Register controls functions beyond those controlled by the Mode Register; these additional functions include DLL enable/disable . . . ." and that Figure 3 on that page, entitled "Extended Mode Register Definition" shows a representation of an Extended Mode Register that indicates that bit A0 equal to 0 corresponds to DLL enable and that bit A0 equal to 1 corresponds to DLL disable. Rambus further admits that "DLL" is often used as an acronym for "delay locked loop."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 125:**

Admit that the JEDEC Double Data Rate (DDR) SDRAM Specification, JESD79, page 12, shows a bit contained in the mode register that operates to enable and disable delay locked loop circuitry to generate an internal clock signal using an external clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 125:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least

with respect to which version of JESD79 is the subject of the request and the terms "mode register," "operates," "delay locked loop circuitry," and "generate an internal clock signal using an external clock signal."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that page 12 of JESD79, Release 1, states that "[t]he Extended Mode Register controls functions beyond those controlled by the Mode Register; these additional functions include DLL enable/disable . . . ." and that Figure 3 on that page, entitled "Extended Mode Register Definition" shows a representation of an Extended Mode Register that indicates that bit A0 equal to 0 corresponds to DLL enable and that bit A0 equal to 1 corresponds to DLL disable. Rambus further admits that "DLL" is often used as an acronym for "delay locked loop."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 126:**

Admit that, to comply with the JEDEC Double Data Rate (DDR) SDRAM Specification, JESD79, a DDR SDRAM device must contain an extended mode register as defined in section 3.11.5.2.11.

**RESPONSE TO REQUEST FOR ADMISSION NO. 126:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JESD79 is the subject of the request. To the extent that the request relates to JESD79, Release 1, Rambus objects to the request as unintelligible because there is no section 3.11.5.2.11 in the document.

**REQUEST FOR ADMISSION NO. 127:**

Admit that, to comply with the JEDEC Double Data Rate (DDR) SDRAM Specification, JESD79, a DDR SDRAM device must contain an extended mode register definition containing a DLL enable/disable bit.

**RESPONSE TO REQUEST FOR ADMISSION NO. 127:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JESD79 is the subject of the request and the terms "extended mode register definition" and "DLL enable/disable bit." It is further unclear what it means for a DDR SDRAM device to contain a "definition."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that JESD79, Release 1, purports to relate to certain DDR SDRAM devices. Rambus further admits that page 12 of JESD79, Release 1, states that "[t]he Extended Mode Register controls functions beyond those controlled by the Mode Register; these additional functions include DLL enable/disable . . . ." and that Figure 3 on that page, entitled "Extended Mode Register Definition" shows a representation of an Extended Mode Register that indicates that bit A0 equal to 0 corresponds to DLL enable and that bit A0 equal to 1 corresponds to DLL disable.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 128:**

Admit that, to comply with the JEDEC Double Data Rate (DDR) SDRAM Specification, JESD79, a DDR SDRAM device must contain a bit in the mode register that operates to enable and disable an on-chip DLL.

**RESPONSE TO REQUEST FOR ADMISSION NO. 128:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JESD79 is the subject of the request and the terms "mode register," "operates," and "on-chip DLL."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that JESD79, Release 1, purports to relate to certain DDR SDRAM devices. Rambus further admits that page 12 of JESD79, Release 1, states that "[t]he Extended Mode Register controls functions beyond those controlled by the Mode Register; these additional

functions include DLL enable/disable . . . .” and that Figure 3 on that page, entitled “Extended Mode Register Definition” shows a representation of an Extended Mode Register that indicates that bit A0 equal to 0 corresponds to DLL enable and that bit A0 equal to 1 corresponds to DLL disable.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 129:**

Admit that, to comply with the JEDEC Double Data Rate (DDR) SDRAM Specification, JESD79, a DDR SDRAM device must contain an extended mode register definition containing an enable/disable bit for delay locked loop circuitry to generate an internal clock signal using an external clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 129:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JESD79 is the subject of the request and the terms “extended mode register definition,” “enable/disable bit,” “delay locked loop circuitry,” and “generate an internal clock signal using an external clock signal.” It is further unclear what it means for a DDR SDRAM device to contain a “definition.”

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that JESD79, Release 1, purports to relate to certain DDR SDRAM devices. Rambus further admits that page 12 of JESD79, Release 1, states that “[t]he Extended Mode Register controls functions beyond those controlled by the Mode Register; these additional functions include DLL enable/disable . . . .” and that Figure 3 on that page, entitled “Extended Mode Register Definition” shows a representation of an Extended Mode Register that indicates that bit A0 equal to 0 corresponds to DLL enable and that bit A0 equal to 1 corresponds to DLL disable. Rambus further admits that “DLL” is often used as an acronym for “delay locked loop.”

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 130:**

Admit that, to comply with the JEDEC Double Data Rate (DDR) SDRAM Specification, JESD79, a DDR SDRAM device must contain a bit in the mode register that operates to enable and disable delay locked loop circuitry to generate an internal clock signal using an external clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 130:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JESD79 is the subject of the request and the terms "mode register," "operates," "delay locked loop circuitry," and "generate an internal clock signal using an external clock signal."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that JESD79, Release 1, purports to relate to certain DDR SDRAM devices. Rambus further admits that page 12 of JESD79, Release 1, states that "[t]he Extended Mode Register controls functions beyond those controlled by the Mode Register; these additional functions include DLL enable/disable . . . ." and that Figure 3 on that page, entitled "Extended Mode Register Definition" shows a representation of an Extended Mode Register that indicates that bit A0 equal to 0 corresponds to DLL enable and that bit A0 equal to 1 corresponds to DLL disable. Rambus further admits that "DLL" is often used as an acronym for "delay locked loop."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 131:**

Admit that, to comply with JEDEC Double Data Rate (DDR) SDRAM Specification, JESD79, a DDR SDRAM device must contain delay locked loop circuitry to generate an internal clock signal using an external clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 131:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JESD79 is the subject of the request and the terms "delay locked

loop circuitry," and "generate an internal clock signal using an external clock signal."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that JESD79, Release 1, purports to relate to certain DDR SDRAM devices. Rambus further admits that the functional block diagrams at pages 4-6 of JESD79 (which are identified as "not represent[ing] an actual circuit implementation") each show a block labeled "DLL" receiving a signal labeled "CLK" (external clock signals on the same diagrams appear to be labeled "CK" and "/CK") and that page 12 of JESD79 states that "[t]he DLL must be enabled for normal operation." Rambus further admits that "DLL" is often used as an acronym for "delay locked loop."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 132:**

Admit that, to comply with JEDEC Double Data Rate (DDR) SDRAM Specification, JESD79, a DDR SDRAM device must contain a PLL or a DLL on the DRAM which can be used to ensure that the data strobe and data coming off of a DRAM chip are sufficiently synchronized to the system clock so that the memory controller can capture that data.

**RESPONSE TO REQUEST FOR ADMISSION NO. 132:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least at least with respect to which version of JESD79 is the subject of the request and the terms "PLL," "DLL," "can be used," "data strobe," "a DRAM chip," and "sufficiently synchronized."

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 133:**

Admit that, between December 1991 and June 1996, various members of the JEDEC 42.3 Subcommittee made presentations showing programmable CAS latency.

**RESPONSE TO REQUEST FOR ADMISSION NO. 133:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "showing," and "programmable CAS latency." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that certain presentations made by members of the JEDEC 42.3 Subcommittee between December 1991 and June 1996 included features designated as, for example, programmable "latency of data to the clock," programmable "data clock latency," "programmable /RAS, /CAS latency," "programmable latency clock times," and "programmable latency." Certain presentations during this period also included a feature designated as a "mode register" or "mode field," with certain bits of the mode register or mode field reserved for a "Latency" or a "CAS Latency" value, and certain combinations of signals corresponding to a "mode set" or "mode register set" command.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 134:**

Admit that, between December 1991 and June 1996, various members of the JEDEC 42.3 Subcommittee made presentations proposing to incorporate programmable CAS latency into JEDEC SDRAM standards.

**RESPONSE TO REQUEST FOR ADMISSION NO. 134:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "programmable CAS latency," and "JEDEC SDRAM standards." Rambus further objects on the ground that it is not familiar with all presentations

made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that certain presentations made by members of the JEDEC 42.3 Subcommittee between December 1991 and June 1996, designated as relating to "Synchronous DRAM" or "SDRAM," included features designated as, for example, programmable "latency of data to the clock," programmable "data clock latency," "programmable /RAS, /CAS latency," "programmable latency clock times," and "programmable latency." Certain presentations during this period also included features designated as a "mode register" or a "mode field" with certain bits of the mode register or mode field reserved for a "Latency" or a "CAS Latency" value, and certain combinations of signals corresponding to a "mode set" or "mode register set" command.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 135:**

Admit that, between December 1991 and June 1996, various members of the JEDEC 42.3 Subcommittee made presentations showing a mode register that could be changed, thereby changing the operation of the chip.

**RESPONSE TO REQUEST FOR ADMISSION NO. 135:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "showing," "mode register," "changed," and "operation of the chip." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that certain presentations made by members of the JEDEC 42.3 Subcommittee between December 1991 and June 1996 included a feature designated as a "mode register," with certain "bit fields" of the mode register reserved for storing certain values, and specifying a combination of signals corresponding to a "mode register set" command used to set the values in the mode register. For example, one presentation (Minutes of JC 42.3 Committee Meeting #64, September 16-17, 1992, Attachment D) identifies the "bit fields" of the mode register as "OPCODE," "LTMODE [latency mode]," "WT [wrap type]," and "WL [wrap length]." The presentation notes that "[a]n MRS [mode register set] command must be used to initialize the device before any read or write operations can be issued to the device." Presumably, a subsequent "mode register set" command could be used to change the values stored in the bit fields within certain parameters.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 136:**

Admit that, between December 1991 and June 1996, various members of the JEDEC 42.3 Subcommittee made presentations proposing to incorporate into JEDEC SDRAM standards a mode register that could be changed, thereby changing the operation of the chip.

**RESPONSE TO REQUEST FOR ADMISSION NO. 136:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "mode register," "changed," "operation of the chip," and "JEDEC SDRAM standards." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that certain presentations made by members of the JEDEC 42.3 Subcommittee between December 1991 and June 1996, designated as relating to "Synchronous DRAM" or "SDRAM," included a feature designated as a "mode register," with certain "bit fields" of the mode register reserved for storing certain values, and specifying a combination of signals corresponding to a "mode register set" command used to set the values in the mode register. For example, one presentation (Minutes of JC 42.3 Committee Meeting #64, September 16-17, 1992, Attachment D) identifies the "bit fields" of the mode register as "OPCODE," "LTMODE [latency mode]," "WT [wrap type]," and "WL [wrap length]." The presentation notes that "[a]n MRS [mode register set] command must be used to initialize the device before any read or write operations can be issued to the device." Presumably, a subsequent "mode register set" command could be used to change the values stored in the bit fields within certain parameters.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 137:**

Admit that, between December 1991 and June 1996, various members of the JEDEC 42.3 Subcommittee made presentations showing a mode register to store a value to determine CAS latency, where that value can be changed by programming the mode register.

**RESPONSE TO REQUEST FOR ADMISSION NO. 137:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "showing," "mode register," "value to determine CAS latency," and "programming." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that certain presentations made by members of the JEDEC 42.3 Subcommittee between December 1991 and June 1996 included a feature designated as a "mode register" or "mode field," with certain bits of the mode register or mode field reserved for a "Latency" or a "CAS Latency" value, and certain combinations of signals corresponding to a "mode set" or "mode register set" command. Presumably, it was contemplated that a "mode set" or "mode register set" command could be used to change the values stored in the mode register within certain parameters.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 138:**

Admit that, between December 1991 and June 1996, various members of the JEDEC 42.3 Subcommittee made presentations proposing to incorporate into JEDEC SDRAM standards a mode register to store a value to determine CAS latency, where that value can be changed by programming the mode register.

**RESPONSE TO REQUEST FOR ADMISSION NO. 138:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "mode register," "value to determine CAS latency," "programming," and "JEDEC SDRAM standards." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that certain presentations made by members of the JEDEC 42.3 Subcommittee between December 1991 and June 1996, designated as relating to "Synchronous DRAM" or "SDRAM," included a feature designated as a "mode register" or "mode field," with certain bits of the mode register or mode field reserved for a "Latency" or a "CAS Latency"

value, and certain combinations of signals corresponding to a "mode set" or "mode register set" command. Presumably, it was contemplated that a "mode set" or "mode register set" command could be used to change the values stored in the mode register within certain parameters.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 139:**

Admit that, between December 1991 and June 1996, various members of the JEDEC 42.3 Subcommittee made presentations showing a mode register to store a value to determine burst length, where that value can be changed by programming the mode register.

**RESPONSE TO REQUEST FOR ADMISSION NO. 139:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "showing," "mode register," "value to determine burst length," and "programming." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that certain presentations made by members of the JEDEC 42.3 Subcommittee between December 1991 and June 1996 included a feature designated as a "mode register" or "mode field," with certain bits of the mode register or mode field reserved for a "wrap length" or a "burst length" value, and certain combinations of signals corresponding to a "mode set" or "mode register set" command. Presumably, it was contemplated that a "mode set" or "mode register set" command could be used to change the values stored in the mode register within certain parameters.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 140:**

Admit that, between December 1991 and June 1996, various members of the JEDEC 42.3 Subcommittee made presentations proposing to incorporate into JEDEC standards a mode register to store a value to determine burst length, where that value can be changed by programming the mode register.

**RESPONSE TO REQUEST FOR ADMISSION NO. 140:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "mode register," "value to determine burst length," "programming," and "JEDEC standards." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that certain presentations made by members of the JEDEC 42.3 Subcommittee between December 1991 and June 1996, designated as relating to certain devices that were the subject of JEDEC standardization efforts, included a feature designated as a "mode register" or "mode field," with certain bits of the mode register or mode field reserved for a "Wrap Length" or a "Burst Length" value, and certain combinations of signals corresponding to a "mode set" or "mode register set" command. Presumably, it was contemplated that a "mode set" or "mode register set" command could be used to change the values stored in the mode register within certain parameters.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 141:**

Admit that, between December 1991 and June 1996, various members of the JEDEC 42.3 Subcommittee made presentations showing a mode register that would store mode-of-operation

data, including the CAS latency.

**RESPONSE TO REQUEST FOR ADMISSION NO. 141:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "showing," "mode register," "mode-of-operation data" and "CAS latency." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that certain presentations made by members of the JEDEC 42.3 Subcommittee between December 1991 and June 1996 included a feature designated as a "mode register" or "mode field," with certain bits of the mode register or mode field reserved for a "Latency" or a "CAS Latency" value, and certain combinations of signals corresponding to a "mode set" or "mode register set" command. Presumably, it was contemplated that a "mode set" or "mode register set" command could be used to change the values stored in the mode register within certain parameters.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 142:**

Admit that, between December 1991 and June 1996, various members of the JEDEC 42.3 Subcommittee made presentations proposing to incorporate into JEDEC SDRAM standards a mode register that would store mode-of-operation data, including the CAS latency.

**RESPONSE TO REQUEST FOR ADMISSION NO. 142:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "mode register," "mode-of-operation data," "CAS latency," and "JEDEC SDRAM standards." Rambus further objects on the ground that it is not

familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that certain presentations made by members of the JEDEC 42.3 Subcommittee between December 1991 and June 1996, designated as relating to "Synchronous DRAM" or "SDRAM," included a feature designated as a "mode register" or "mode field," with certain bits of the mode register or mode field reserved for a "Latency" or a "CAS Latency" value, and certain combinations of signals corresponding to a "mode set" or "mode register set" command. Presumably, it was contemplated that a "mode set" or "mode register set" command could be used to change the values stored in the mode register within certain parameters.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 143:**

Admit that, between December 1991 and June 1996, various members of the JEDEC 42.3 Subcommittee made presentations showing a mode register that would store mode-of-operation data, including the burst length.

**RESPONSE TO REQUEST FOR ADMISSION NO. 143:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "showing," "mode register," "mode-of-operation data" and "burst length." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that certain presentations made by members of the JEDEC 42.3 Subcommittee between December 1991 and June 1996 included a feature designated as a "mode register" or "mode field," with certain bits of the mode register or mode field reserved for a "Wrap Length" or a "Burst Length" value, and certain combinations of signals corresponding to a "mode set" or "mode register set" command. Presumably, it was contemplated that a "mode set" or "mode register set" command could be used to change the values stored in the mode register within certain parameters.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 144:**

Admit that, between December 1991 and June 1996, various members of the JEDEC 42.3 Subcommittee made presentations proposing to incorporate into JEDEC SDRAM standards a mode register that would store mode-of-operation data, including the burst length.

**RESPONSE TO REQUEST FOR ADMISSION NO. 144:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "mode register," "mode-of-operation data," "burst length," and "JEDEC SDRAM standards." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that certain presentations made by members of the JEDEC 42.3 Subcommittee between December 1991 and June 1996, designated as relating to "Synchronous DRAM" or "SDRAM," included a feature designated as a "mode register" or "mode field," with certain bits of the mode register or mode field reserved for a "Wrap Length" or a "Burst Length" value, and certain combinations of signals corresponding to a "mode set" or "mode register set"

command. Presumably, it was contemplated that a "mode set" or "mode register set" command could be used to change the values stored in the mode register within certain parameters.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 145:**

Admit that, between December 1991 and June 1996, various members of the JEDEC 42.3 Subcommittee made presentations showing a programmable register that would store a value that is representative of a delay time after which the device would respond to a read request.

**RESPONSE TO REQUEST FOR ADMISSION NO. 145:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "showing," "programmable register," "representative of a delay time," "device," and "respond to a read request." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that certain presentations made by members of the JEDEC 42.3 Subcommittee between December 1991 and June 1996 included features designated as, for example, programmable "latency of data to the clock," programmable "data clock latency," "programmable /RAS, /CAS latency," "programmable latency clock times," and "programmable latency." Certain presentations during this period also included a feature designated as a "mode register" or "mode field," with certain bits of the mode register or mode field reserved for a "Latency" or a "CAS Latency" value, and certain combinations of signals corresponding to a "mode set" or "mode register set" command. One presentation (Minutes of JC 42.3 Committee Meeting #64, September 16-17, 1992, Attachment D), for example, stated in connection with the

Mode Register specified in that presentation that "[t]he first data output cycle of a read burst sequence can be programmed to occur 1, 2, 3 clock cycles after the read command. The read access time is always referenced to the column address."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 146:**

Admit that, between December 1991 and June 1996, various members of the JEDEC 42.3 Subcommittee made presentations proposing to incorporate into JEDEC SDRAM standards a programmable register that would store a value that is representative of a delay time after which the device would respond to a read request.

**RESPONSE TO REQUEST FOR ADMISSION NO. 146:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "programmable register," "representative of a delay time," "device," "respond to a read request," and "JEDEC SDRAM standards." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that certain presentations made by members of the JEDEC 42.3 Subcommittee between December 1991 and June 1996, designated as relating to "Synchronous DRAM" or "SDRAM," included features designated as, for example, programmable "latency of data to the clock," programmable "data clock latency," "programmable /RAS, /CAS latency," "programmable latency clock times," and "programmable latency." Certain presentations during this period also included a feature designated as a "mode register" or "mode field," with certain bits of the mode register or mode field reserved for a "Latency" or a "CAS Latency" value, and

certain combinations of signals corresponding to a "mode set" or "mode register set" command. One presentation (Minutes of JC 42.3 Committee Meeting #64, September 16-17, 1992, Attachment D), for example, stated in connection with the Mode Register specified in that presentation that "[t]he first data output cycle of a read burst sequence can be programmed to occur 1, 2, 3 clock cycles after the read command. The read access time is always referenced to the column address."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 147:**

Admit that, between December 1991 and June 1996, various members of the JEDEC 42.3 Subcommittee made presentations showing a programmable register that would receive block size information defining an amount of data to be output by the memory device in response to a read request.

**RESPONSE TO REQUEST FOR ADMISSION NO. 147:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "showing," "programmable register," "block size information," "defining an amount of data," and "response to a read request." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that certain presentations made by members of the JEDEC 42.3 Subcommittee between December 1991 and June 1996 included a feature designated as a "mode register" or "mode field," with certain bits of the mode register or mode field reserved for a "Wrap Length" or a "Burst Length" value, and certain combinations of signals corresponding to

a “mode set” or “mode register set” command.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 148:**

Admit that, between December 1991 and June 1996, various members of the JEDEC 42.3 Subcommittee made presentations proposing to incorporate into JEDEC SDRAM standards a programmable register that would receive block size information defining an amount of data to be output by the memory device in response to a read request.

**RESPONSE TO REQUEST FOR ADMISSION NO. 148:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms “presentations,” “programmable register,” “block size information,” “defining an amount of data,” “response to a read request,” and “JEDEC SDRAM standards.” Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, “presentations” is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that certain presentations made by members of the JEDEC 42.3 Subcommittee between December 1991 and June 1996, designated as relating to “Synchronous DRAM” or “SDRAM,” included a feature designated as a “mode register” or “mode field,” with certain bits of the mode register or mode field reserved for a “Wrap Length” or a “Burst Length” value, and certain combinations of signals corresponding to a “mode set” or “mode register set” command.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 149:**

Admit that, between December 1991 and June 1996, various members of the JC 42.3 Subcommittee made presentations proposing to incorporate programmable latency via a control register into JEDEC SDRAM standards.

**RESPONSE TO REQUEST FOR ADMISSION NO. 149:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "programmable latency," "control register," and "JEDEC SDRAM standards." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that certain presentations made by members of the JEDEC 42.3 Subcommittee between December 1991 and June 1996, designated as relating to "Synchronous DRAM" or "SDRAM," included features designated as, for example, programmable "latency of data to the clock," programmable "data clock latency," "programmable /RAS, /CAS latency," "programmable latency clock times," and "programmable latency." Certain presentations during this period also included features designated as a "mode register" or a "mode field" with certain bits of the mode register or mode field reserved for a "Latency" or a "CAS Latency" value, and certain combinations of signals corresponding to a "mode set" or "mode register set" command.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 150:**

Admit that, between December 1991 and June 1996, Rambus knew that various members of the JC 42.3 Subcommittee made presentations proposing to incorporate programmable latency via a control register into JEDEC SDRAM standards.

**RESPONSE TO REQUEST FOR ADMISSION NO. 150:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "programmable latency," "control register," and "JEDEC SDRAM standards." Rambus further objects on the ground that the request is vague and ambiguous as to what would constitute "knowledge" on the part of Rambus.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at certain times between December 1991 and June 1996, certain Rambus employees knew that certain presentations made by members of the JEDEC 42.3 Subcommittee between December 1991 and June 1996, designated as relating to "Synchronous DRAM" or "SDRAM," included features designated as, for example, programmable "latency of data to the clock," programmable "data clock latency," "programmable /RAS, /CAS latency," "programmable latency clock times," and "programmable latency." Certain Rambus employees also knew during this period that certain presentations included features designated as a "mode register" or a "mode field" with certain bits of the mode register or mode field reserved for a "Latency" or a "CAS Latency" value, and certain combinations of signals corresponding to a "mode set" or "mode register set" command.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 151:**

Admit that, between December 1991 and June 1996, various members of the JC 42.3 Subcommittee made presentations proposing to incorporate programmable access latency into JEDEC SDRAM standards.

**RESPONSE TO REQUEST FOR ADMISSION NO. 151:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "programmable access latency," and "JEDEC SDRAM standards." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and

is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that certain presentations made by members of the JEDEC 42.3 Subcommittee between December 1991 and June 1996, designated as relating to "Synchronous DRAM" or "SDRAM," included features designated as, for example, programmable "latency of data to the clock," programmable "data clock latency," "programmable /RAS, /CAS latency," "programmable latency clock times," and "programmable latency." Certain presentations during this period also included features designated as a "mode register" or a "mode field" with certain bits of the mode register or mode field reserved for a "Latency" or a "CAS Latency" value, and certain combinations of signals corresponding to a "mode set" or "mode register set" command.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 152:**

Admit that, between December 1991 and June 1996, Rambus knew that various members of the JC 42.3 Subcommittee made presentations proposing to incorporate programmable access latency into JEDEC SDRAM standards.

**RESPONSE TO REQUEST FOR ADMISSION NO. 152:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "programmable access latency," and "JEDEC SDRAM standards." Rambus further objects on the ground that the request is vague and ambiguous as to what would constitute "knowledge" on the part of Rambus.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at certain times between December 1991 and June 1996, certain Rambus employees knew that certain presentations made by members of the JEDEC 42.3 Subcommittee between December 1991 and June 1996, designated as relating to "Synchronous

DRAM" or "SDRAM," included features designated as, for example, programmable "latency of data to the clock," programmable "data clock latency," "programmable /RAS, /CAS latency," "programmable latency clock times," and "programmable latency." Certain Rambus employees also knew during this period that certain presentations included features designated as a "mode register" or a "mode field" with certain bits of the mode register or mode field reserved for a "Latency" or a "CAS Latency" value, and certain combinations of signals corresponding to a "mode set" or "mode register set" command.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 153:**

Admit that, between December 1991 and June 1996, various members of the JC 42.3 Subcommittee made presentations proposing to incorporate a writable configuration register permitting programmable CAS latency into JEDEC SDRAM standards.

**RESPONSE TO REQUEST FOR ADMISSION NO. 153:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "writable configuration register," "programmable CAS latency," and "JEDEC SDRAM standards." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that certain presentations made by members of the JEDEC 42.3 Subcommittee between December 1991 and June 1996, designated as relating to "Synchronous DRAM" or "SDRAM," included a feature designated as a "mode register" or "mode field," with certain bits of the mode register or mode field reserved for a "Latency" or a "CAS Latency" value, and certain combinations of signals corresponding to a "mode set" or "mode register set"

command.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 154:**

Admit that, between December 1991 and June 1996, Rambus knew that various members of the JC 42.3 Subcommittee made presentations proposing to incorporate a writable configuration register permitting programmable CAS latency into JEDEC SDRAM standards.

**RESPONSE TO REQUEST FOR ADMISSION NO. 154:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "writable configuration register," "programmable CAS latency," and "JEDEC SDRAM standards." Rambus further objects on the ground that the request is vague and ambiguous as to what would constitute "knowledge" on the part of Rambus.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at certain times between December 1991 and June 1996, certain Rambus employees knew that certain presentations made by members of the JEDEC 42.3 Subcommittee between December 1991 and June 1996, designated as relating to "Synchronous DRAM" or "SDRAM," included a feature designated as a "mode register" or "mode field," with certain bits of the mode register or mode field reserved for a "Latency" or a "CAS Latency" value, and certain combinations of signals corresponding to a "mode set" or "mode register set" command.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 155:**

Admit that, between December 1991 and June 1996, various members of the JC 42.3 Subcommittee made presentations proposing to incorporate the use of control registers to contain values which control RAS and CAS access timing into JEDEC SDRAM standards.

**RESPONSE TO REQUEST FOR ADMISSION NO. 155:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "control registers," "RAS and CAS access timing," and "JEDEC SDRAM standards." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that certain presentations made by members of the JEDEC 42.3 Subcommittee between December 1991 and June 1996, designated as relating to "Synchronous DRAM" or "SDRAM," included features designated as, for example, programmable "latency of data to the clock," programmable "data clock latency," "programmable /RAS, /CAS latency," "programmable latency clock times," and "programmable latency." Certain presentations during this period also included features designated as a "mode register" or a "mode field" with certain bits of the mode register or mode field reserved for a "Latency" or a "CAS Latency" value, and certain combinations of signals corresponding to a "mode set" or "mode register set" command.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 156:**

Admit that, between December 1991 and June 1996, Rambus knew that various members of the JC 42.3 Subcommittee made presentations proposing to incorporate the use of control registers to contain values which control RAS and CAS access timing into JEDEC SDRAM standards.

**RESPONSE TO REQUEST FOR ADMISSION NO. 156:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "control registers," "RAS and CAS access timing," and

"JEDEC SDRAM standards." Rambus further objects on the ground that the request is vague and ambiguous as to what would constitute "knowledge" on the part of Rambus.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at certain times between December 1991 and June 1996, certain Rambus employees knew that certain presentations made by members of the JEDEC 42.3 Subcommittee between December 1991 and June 1996, designated as relating to "Synchronous DRAM" or "SDRAM," included features designated as, for example, programmable "latency of data to the clock," programmable "data clock latency," "programmable /RAS, /CAS latency," "programmable latency clock times," and "programmable latency." Certain Rambus employees also knew during this period that certain presentations included features designated as a "mode register" or a "mode field" with certain bits of the mode register or mode field reserved for a "Latency" or a "CAS Latency" value, and certain combinations of signals corresponding to a "mode set" or "mode register set" command.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 157:**

Admit that, between December 1991 and June 1996, various members of the JC 42.3 Subcommittee made presentations proposing to incorporate the use of control registers to contain values which control RAS and CAS access timing into JEDEC SDRAM standards.

**RESPONSE TO REQUEST FOR ADMISSION NO. 157:**

Rambus objects to this request as duplicative of Request No. 155, and incorporates its objections and response thereto.

**REQUEST FOR ADMISSION NO. 158:**

Admit that, between December 1991 and June 1996, Rambus knew that various members of the JC 42.3 Subcommittee made presentations proposing to incorporate the use of control registers to contain values which control RAS and CAS access timing into JEDEC SDRAM

standards.

**RESPONSE TO REQUEST FOR ADMISSION NO. 158:**

Rambus objects to this request as duplicative of Request No. 156, and incorporates its objections and response thereto.

**REQUEST FOR ADMISSION NO. 159:**

Admit that, in 1992, Rambus voted on a ballot proposing to incorporate programmable CAS latency into JEDEC SDRAM standards.

**RESPONSE TO REQUEST FOR ADMISSION NO. 159:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "programmable CAS latency," and "JEDEC SDRAM standards."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that in 1992 it voted "no" on a ballot with subject designated as "Proposed Standard for 16M Bit x 4 Sync DRAM Mode Register;" the ballot related to a representation of a "Mode-Register," and accompanying diagram showing "Mode-Register write timing," with certain bits of the Mode-Register reserved for storing a value designated as "CAS Latency."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 160:**

Admit that, in 1992, Rambus voted on a ballot proposing to incorporate into JEDEC SDRAM standards a mode register that could be changed, thereby changing the operation of the chip.

**RESPONSE TO REQUEST FOR ADMISSION NO. 160:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "mode register," "changed," "operation of the chip," and "JEDEC SDRAM standards."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that in 1992 it voted "no" on a ballot with subject designated as "Proposed Standard for 16M Bit x 4 Sync DRAM Mode Register;" the ballot related to a representation of a "Mode-Register," and accompanying diagram showing "Mode-Register write timing," with certain bits of the Mode Register reserved for storing a values designated as "CAS Latency," "Wrap Length," and "Wrap Type,"

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 161:**

Admit that, in 1992, Rambus voted on a ballot proposing to incorporate into JEDEC SDRAM standards a mode register to store a value to determine CAS latency, where that value can be changed by programming the mode register.

**RESPONSE TO REQUEST FOR ADMISSION NO. 161:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "mode register," "to determine CAS latency," "programming," and "JEDEC SDRAM standards."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that in 1992 it voted "no" on a ballot with subject designated as "Proposed Standard for 16M Bit x 4 Sync DRAM Mode Register;" the ballot related to a representation of a "Mode-Register," and accompanying diagram showing "Mode-Register write timing," with certain bits of the Mode-Register reserved for storing a value designated as "CAS Latency."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 162:**

Admit that, in 1992, Rambus voted on a ballot proposing to incorporate into JEDEC standards a mode register to store a value to determine burst length, where that value can be

changed by programming the mode register.

**RESPONSE TO REQUEST FOR ADMISSION NO. 162:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "mode register," "to determine burst length," "programming," and "JEDEC SDRAM standards."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that in 1992 it voted "no" on a ballot with subject designated as "Proposed Standard for 16M Bit x 4 Sync DRAM Mode Register;" the ballot related to a representation of a "Mode-Register," and accompanying diagram showing "Mode-Register write timing," with certain bits of the Mode-Register reserved for storing a value designated as "Wrap Length."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 163:**

Admit that, in 1992, Rambus voted on a ballot proposing to incorporate into JEDEC SDRAM standards a mode register that would store mode-of-operation data, including the CAS latency.

**RESPONSE TO REQUEST FOR ADMISSION NO. 163:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "mode register," "mode-of-operation data," "CAS latency," and "JEDEC SDRAM standards."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that in 1992 it voted "no" on a ballot with subject designated as "Proposed Standard for 16M Bit x 4 Sync DRAM Mode Register;" the ballot related to a representation of a "Mode-Register," with certain bits of the Mode-Register reserved for storing a value designated as "CAS Latency."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 164:**

Admit that, in 1992, Rambus voted on a ballot proposing to incorporate into JEDEC SDRAM standards a mode register that would store mode-of-operation data, including the burst length.

**RESPONSE TO REQUEST FOR ADMISSION NO. 164:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "mode register," "mode-of-operation data," and "JEDEC SDRAM standards."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that in 1992 it voted "no" on a ballot with subject designated as "Proposed Standard for 16M Bit x 4 Sync DRAM Mode Register;" the ballot related to a representation of a "Mode-Register," with certain bits of the Mode-Register reserved for storing a value designated as "Wrap Length."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 165:**

Admit that, in 1992, Rambus voted on a ballot proposing to incorporate into JEDEC SDRAM standards a programmable register that would store a value that is representative of a delay time after which the device would respond to a read request.

**RESPONSE TO REQUEST FOR ADMISSION NO. 165:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "programmable register," "representative of a delay time," "respond to a read request," and "JEDEC SDRAM standards."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that in 1992 it voted "no" on a ballot with subject designated as "Proposed Standard for 16M Bit x 4 Sync DRAM Mode Register;" the ballot related to a

representation of a “Mode-Register,” and accompanying diagram showing “Mode-Register write timing,” with certain bits of the Mode-Register reserved for storing a value designated as “CAS Latency.”

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 166:**

Admit that, in 1992, Rambus voted on a ballot proposing to incorporate into JEDEC SDRAM standards a programmable register that would receive block size information defining an amount of data to be output by the memory device in response to a read request.

**RESPONSE TO REQUEST FOR ADMISSION NO. 166:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms “programmable register,” “block size information,” “defining an amount of data,” “in response to a read request,” and “JEDEC SDRAM standards.”

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that in 1992 it voted “no” on a ballot with subject designated as “Proposed Standard for 16M Bit x 4 Sync DRAM Mode Register;” the ballot related to a representation of a “Mode-Register,” and accompanying diagram showing “Mode-Register write timing,” with certain bits of the Mode-Register reserved for storing a value designated as “Wrap Length.”

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 167:**

Admit that, in 1992, Rambus voted on a ballot proposing to incorporate programmable latency via a control register into JEDEC SDRAM standards.

**RESPONSE TO REQUEST FOR ADMISSION NO. 167:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms “programmable latency,” “control register,” and “JEDEC SDRAM

standards."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that in 1992 it voted "no" on a ballot with subject designated as "Proposed Standard for 16M Bit x 4 Sync DRAM Mode Register;" the ballot related to a representation of a "Mode-Register," and accompanying diagram showing "Mode-Register write timing," with certain bits of the Mode-Register reserved for storing a value designated as "CAS Latency."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 168:**

Admit that, in 1992, Rambus voted on a ballot proposing to incorporate programmable access latency into JEDEC SDRAM standards.

**RESPONSE TO REQUEST FOR ADMISSION NO. 168:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "programmable access latency," and "JEDEC SDRAM standards."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that in 1992 it voted "no" on a ballot with subject designated as "Proposed Standard for 16M Bit x 4 Sync DRAM Mode Register;" the ballot related to a representation of a "Mode-Register," and accompanying diagram showing "Mode-Register write timing," with certain bits of the Mode-Register reserved for storing a value designated as "CAS Latency."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 169:**

Admit that, in 1992, Rambus voted on a ballot proposing to incorporate a writable configuration register permitting programmable CAS latency into JEDEC SDRAM standards.

**RESPONSE TO REQUEST FOR ADMISSION NO. 169:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "writable configuration register," "programmable CAS latency," and "JEDEC SDRAM standards."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that in 1992 it voted "no" on a ballot with subject designated as "Proposed Standard for 16M Bit x 4 Sync DRAM Mode Register;" the ballot related to a representation of a "Mode-Register," and accompanying diagram showing "Mode-Register write timing," with certain bits of the Mode-Register reserved for storing a value designated as "CAS Latency."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 170:**

Admit that, in 1992, Rambus voted on a ballot proposing to incorporate the use of control registers to contain values which control RAS and CAS access timing into JEDEC SDRAM standards.

**RESPONSE TO REQUEST FOR ADMISSION NO. 170:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "control registers," "RAS and CAS access timing," and "JEDEC SDRAM standards."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that in 1992 it voted "no" on a ballot with subject designated as "Proposed Standard for 16M Bit x 4 Sync DRAM Mode Register;" the ballot related to a representation of a "Mode-Register," with certain bits of the Mode-Register reserved for storing a value designated as "CAS Latency."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 171:**

Admit that, between December 1991 and June 1996, various members of the JEDEC 42.3 Subcommittee made presentations showing auto precharge.

**RESPONSE TO REQUEST FOR ADMISSION NO. 171:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "showing," and "auto precharge." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that certain presentations made by members of the JEDEC 42.3 Subcommittee between December 1991 and June 1996 included reference to and purported to describe features designated as, for example, "auto precharge," "autoprecharge," and "automatic precharge."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 172:**

Admit that, between December 1991 and June 1996, Rambus knew that various members of the JEDEC 42.3 Subcommittee made presentations showing auto precharge.

**RESPONSE TO REQUEST FOR ADMISSION NO. 172:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "showing," and "auto precharge." Rambus further objects on the ground that the request is vague and ambiguous as to what would constitute "knowledge" on the part of Rambus.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at certain times between December 1991 and June 1996, certain Rambus employees knew that certain presentations made by members of the JEDEC 42.3 Subcommittee between December 1991 and June 1996 included reference to and purported to describe features designated as, for example, "auto precharge," "autoprecharge," and "automatic precharge."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 173:**

Admit that, between December 1991 and June 1996, various members of the JEDEC 42.3 Subcommittee made presentations proposing to incorporate auto precharge into JEDEC SDRAM standards.

**RESPONSE TO REQUEST FOR ADMISSION NO. 173:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "auto precharge," and "JEDEC SDRAM standards." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that certain presentations made by members of the JEDEC 42.3 Subcommittee between December 1991 and June 1996, designated as relating to "Synchronous DRAM" or "SDRAM," included reference to and purported to describe features designated as, for example, "auto precharge," "autoprecharge," and "automatic precharge."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 174:**

Admit that, between December 1991 and June 1996, Rambus knew that various members of the JEDEC 42.3 Subcommittee made presentations proposing to incorporate auto precharge into JEDEC SDRAM standards.

**RESPONSE TO REQUEST FOR ADMISSION NO. 174:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "auto precharge," and "JEDEC SDRAM standards." Rambus further objects on the ground that the request is vague and ambiguous as to what would constitute "knowledge" on the part of Rambus.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at certain times between December 1991 and June 1996, certain Rambus employees knew that certain presentations made by members of the JEDEC 42.3 Subcommittee between December 1991 and June 1996, designated as relating to "Synchronous DRAM" or "SDRAM," included reference to and purported to describe features designated as, for example, "auto precharge," "autoprecharge," and "automatic precharge."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 175:**

Admit that, between December 1991 and June 1996, various members of the JEDEC 42.3 Subcommittee made presentations showing the auto precharge options available during the column portion of any cycle.

**RESPONSE TO REQUEST FOR ADMISSION NO. 175:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "showing," "auto precharge options," "column portion," and "any cycle." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable

inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that certain presentations made by members of the JEDEC 42.3 Subcommittee between December 1991 and June 1996 included reference to and purported to describe features designated as, for example, "auto precharge," "autoprecharge," and "automatic precharge."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 176:**

Admit that, between December 1991 and June 1996, Rambus knew that various members of the JEDEC 42.3 Subcommittee made presentations showing the auto precharge options available during the column portion of any cycle.

**RESPONSE TO REQUEST FOR ADMISSION NO. 176:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "showing," "auto precharge options," "column portion," and "any cycle." Rambus further objects on the ground that the request is vague and ambiguous as to what would constitute "knowledge" on the part of Rambus.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at certain times between December 1991 and June 1996, certain Rambus employees knew that certain presentations made by members of the JEDEC 42.3 Subcommittee between December 1991 and June 1996 included reference to and purported to describe features designated as, for example, "auto precharge," "autoprecharge," and "automatic precharge."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 177:**

Admit that, between December 1991 and June 1996, various members of the JEDEC 42.3 Subcommittee made presentations proposing to incorporate into JEDEC SDRAM standards the auto precharge options available during the column portion of any cycle.

**RESPONSE TO REQUEST FOR ADMISSION NO. 177:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "auto precharge options," "column portion," "any cycle." and "JEDEC SDRAM standards." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that certain presentations made by members of the JEDEC 42.3 Subcommittee between December 1991 and June 1996, designated as relating to "Synchronous DRAM" or "SDRAM," included reference to and purported to describe features designated as, for example, "auto precharge," "autoprecharge," and "automatic precharge."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 178:**

Admit that, between December 1991 and June 1996, Rambus knew that various members of the JEDEC 42.3 Subcommittee made presentations proposing to incorporate into JEDEC SDRAM standards the auto precharge options available during the column portion of any cycle.

**RESPONSE TO REQUEST FOR ADMISSION NO. 178:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "auto precharge options," "column portion," "any cycle." and "JEDEC SDRAM standards." Rambus further objects on the ground that the

request is vague and ambiguous as to what would constitute "knowledge" on the part of Rambus.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at certain times between December 1991 and June 1996, certain Rambus employees knew that certain presentations made by members of the JEDEC 42.3 Subcommittee between December 1991 and June 1996, designated as relating to "Synchronous DRAM" or "SDRAM," included reference to and purported to describe features designated as, for example, "auto precharge," "autoprecharge," and "automatic precharge."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 179:**

Admit that, between December 1991 and June 1996, various members of the JEDEC 42.3 Subcommittee made presentations showing a proposal to permit the user to specify that the bank currently being accessed precharge itself as soon as the burst is completed.

**RESPONSE TO REQUEST FOR ADMISSION NO. 179:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "showing," "the user," "the bank currently being accessed," "precharge itself, " and "the burst." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that certain presentations made by members of the JEDEC 42.3 Subcommittee between December 1991 and June 1996 included reference to and purported to describe features designated as, for example, "auto precharge," "autoprecharge," and "automatic precharge." Rambus further admits one such presentation (Minutes of JC 42.3 Committee Meeting #64, September 16-17, 1992, Attachment D) stated with respect to "autoprecharge:"

"The user may specify that the bank currently being accessed precharge itself as soon as the burst is completed."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 180:**

Admit that, between December 1991 and June 1996, Rambus knew that various members of the JEDEC 42.3 Subcommittee made presentations showing a proposal to permit the user to specify that the bank currently being accessed precharge itself as soon as the burst is completed.

**RESPONSE TO REQUEST FOR ADMISSION NO. 180:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "showing," "the user," "the bank currently being accessed," "precharge itself, " and "the burst." Rambus further objects on the ground that the request is vague and ambiguous as to what would constitute "knowledge" on the part of Rambus.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at certain times between December 1991 and June 1996, certain Rambus employees knew that certain presentations made by members of the JEDEC 42.3 Subcommittee between December 1991 and June 1996 included reference to and purported to describe features designated as, for example, "auto precharge," "autoprecharge," and "automatic precharge." Rambus further admits that certain Rambus employees knew during that period that one such presentation (Minutes of JC 42.3 Committee Meeting #64, September 16-17, 1992, Attachment D) stated with respect to "autoprecharge:" "The user may specify that the bank currently being accessed precharge itself as soon as the burst is completed."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 181:**

Admit that, between December 1991 and June 1996, various members of the JEDEC 42.3 Subcommittee made presentations proposing to incorporate into JEDEC SDRAM standards a

proposal to permit the user to specify that the bank currently being accessed precharge itself as soon as the burst is completed.

**RESPONSE TO REQUEST FOR ADMISSION NO. 181:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "the user," "the bank currently being accessed," "precharge itself, " "the burst," and "JEDEC SDRAM standards." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that certain presentations made by members of the JEDEC 42.3 Subcommittee between December 1991 and June 1996, designated as relating to "Synchronous DRAM or SDRAM," included reference to and purported to describe features designated as, for example, "auto precharge," "autoprecharge," and "automatic precharge." Rambus further admits one such presentation (Minutes of JC 42.3 Committee Meeting #64, September 16-17, 1992, Attachment D) stated with respect to "autoprecharge:" "The user may specify that the bank currently being accessed precharge itself as soon as the burst is completed."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 182:**

Admit that, between December 1991 and June 1996, Rambus knew that various members of the JEDEC 42.3 Subcommittee made presentations proposing to incorporate into JEDEC SDRAM standards a proposal to permit the user to specify that the bank currently being accessed precharge itself as soon as the burst is completed.

**RESPONSE TO REQUEST FOR ADMISSION NO. 182:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "the user," "the bank currently being accessed," "precharge itself, " "the burst," and "JEDEC SDRAM standards." Rambus further objects on the ground that the request is vague and ambiguous as to what would constitute "knowledge" on the part of Rambus.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at certain times between December 1991 and June 1996, certain Rambus employees knew that certain presentations made by members of the JEDEC 42.3 Subcommittee between December 1991 and June 1996, designated as relating to "Synchronous DRAM or SDRAM," included reference to and purported to describe features designated as, for example, "auto precharge," "autoprecharge," and "automatic precharge." Rambus further admits that certain Rambus employees knew during that period that one such presentation (Minutes of JC 42.3 Committee Meeting #64, September 16-17, 1992, Attachment D) stated with respect to "autoprecharge:" "The user may specify that the bank currently being accessed precharge itself as soon as the burst is completed."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 183:**

Admit that, between December 1991 and June 1996, various members of the JEDEC 42.3 Subcommittee made presentations proposing to incorporate into JEDEC SDRAM standards a proposal to permit the user to specify that the bank currently being accessed precharge itself as soon as the burst is completed.

**RESPONSE TO REQUEST FOR ADMISSION NO. 183:**

Rambus objects to this request as duplicative or Request No. 181, and incorporates its objections and response thereto.

**REQUEST FOR ADMISSION NO. 184:**

Admit that, between December 1991 and June 1996, Rambus knew that various members of the JEDEC 42.3 Subcommittee made presentations proposing to incorporate into JEDEC SDRAM standards a proposal to permit the user to specify that the bank currently being accessed precharge itself as soon as the burst is completed.

**RESPONSE TO REQUEST FOR ADMISSION NO. 184:**

Rambus objects to this request as duplicative or Request No. 182, and incorporates its objections and response thereto.

**REQUEST FOR ADMISSION NO. 185:**

Admit that, between December 1991 and June 1996, various members of the JC 42.3 Subcommittee made presentations proposing to incorporate into JEDEC SDRAM standards the idea that an SDRAM device must be able to respond to information sent along with a read request instructing it to automatically precharge bank(s) after each read request.

**RESPONSE TO REQUEST FOR ADMISSION NO. 185:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "idea," "respond to information," "sent along with a read request," "automatically precharge bank(s)," "each read request," and "JEDEC SDRAM standards." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that certain presentations made by members of the JEDEC 42.3 Subcommittee between December 1991 and June 1996, designated as relating to "Synchronous

DRAM" or "SDRAM," included reference to and purported to describe features designated as, for example, "auto precharge," "autoprecharge," and "automatic precharge."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 186:**

Admit that, between December 1991 and June 1996, Rambus knew that various members of the JC 42.3 Subcommittee made presentations proposing to incorporate into JEDEC SDRAM standards the idea that an SDRAM device must be able to respond to information sent along with a read request instructing it to automatically precharge bank(s) after each read request.

**RESPONSE TO REQUEST FOR ADMISSION NO. 186:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "idea," "respond to information," "sent along with a read request," "automatically precharge bank(s)," "each read request," and "JEDEC SDRAM standards." Rambus further objects on the ground that the request is vague and ambiguous as to what would constitute "knowledge" on the part of Rambus.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at certain times between December 1991 and June 1996, certain Rambus employees knew that certain presentations made by members of the JEDEC 42.3 Subcommittee between December 1991 and June 1996, designated as relating to "Synchronous DRAM" or "SDRAM," included reference to and purported to describe features designated as, for example, "auto precharge," "autoprecharge," and "automatic precharge."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 187:**

Admit that, between December 1991 and June 1996, various members of the JC 42.3 Subcommittee made presentations proposing to incorporate into JEDEC SDRAM standards the idea that an SDRAM device must have the ability to internally precharge a bank without first

receiving a separate precharge command.

**RESPONSE TO REQUEST FOR ADMISSION NO. 187:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "idea," "internally precharge a bank," "separate precharge command," and "JEDEC SDRAM standards." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that certain presentations made by members of the JEDEC 42.3 Subcommittee between December 1991 and June 1996, designated as relating to "Synchronous DRAM" or "SDRAM," included reference to and purported to describe features designated as, for example, "auto precharge," "autoprecharge," and "automatic precharge."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 188:**

Admit that, between December 1991 and June 1996, Rambus knew that various members of the JC 42.3 Subcommittee made presentations proposing to incorporate into JEDEC SDRAM standards the idea that an SDRAM device must have the ability to internally precharge a bank without first receiving a separate precharge command.

**RESPONSE TO REQUEST FOR ADMISSION NO. 188:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "idea," "internally precharge a bank," "separate precharge command," and "JEDEC SDRAM standards." Rambus further objects on the ground that the request is vague and ambiguous as to what would constitute "knowledge" on the part of

Rambus.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at certain times between December 1991 and June 1996, certain Rambus employees knew that certain presentations made by members of the JEDEC 42.3 Subcommittee between December 1991 and June 1996, designated as relating to "Synchronous DRAM" or "SDRAM," included reference to and purported to describe features designated as, for example, "auto precharge," "autoprecharge," and "automatic precharge."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 189:**

Admit that, between December 1991 and June 1996, various members of the JC 42.3 Subcommittee made presentations proposing to incorporate into JEDEC SDRAM standards the idea that an SDRAM device must be able to respond to information sent along with a read request instructing it to automatically precharge bank(s) for the next each read request.

**RESPONSE TO REQUEST FOR ADMISSION NO. 189:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "idea," "respond to information," "sent along with a read request," "automatically precharge bank(s)," "next each read request," and "JEDEC SDRAM standards." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that certain presentations made by members of the JEDEC 42.3 Subcommittee between December 1991 and June 1996, designated as relating to "Synchronous DRAM" or "SDRAM," included reference to and purported to describe features designated as,

for example, “auto precharge,” “autoprecharge,” and “automatic precharge.”

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 190:**

Admit that, between December 1991 and June 1996, Rambus knew that various members of the JC 42.3 Subcommittee made presentations proposing to incorporate into JEDEC SDRAM standards the idea that an SDRAM device must be able to respond to information sent along with a read request instructing it to automatically precharge bank(s) for the next each read request.

**RESPONSE TO REQUEST FOR ADMISSION NO. 190:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms “presentations,” “idea,” “respond to information,” “sent along with a read request,” “automatically precharge bank(s),” “next each read request,” and “JEDEC SDRAM standards.” Rambus further objects on the ground that the request is vague and ambiguous as to what would constitute “knowledge” on the part of Rambus.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at certain times between December 1991 and June 1996, certain Rambus employees knew that certain presentations made by members of the JEDEC 42.3 Subcommittee between December 1991 and June 1996, designated as relating to “Synchronous DRAM” or “SDRAM,” included reference to and purported to describe features designated as, for example, “auto precharge,” “autoprecharge,” and “automatic precharge.”

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 191:**

Admit that, between December 1991 and June 1996, various members of the JC 42.3 Subcommittee made presentations proposing to incorporate into JEDEC SDRAM standards the idea that an SDRAM device must have the ability to internally precharge a bank without first receiving a separate precharge command.

**RESPONSE TO REQUEST FOR ADMISSION NO. 191:**

Rambus objects to this request as duplicative of Request No. 187, and incorporates its objections and response thereto.

**REQUEST FOR ADMISSION NO. 192:**

Admit that, between December 1991 and June 1996, Rambus knew that various members of the JC 42.3 Subcommittee made presentations proposing to incorporate into JEDEC SDRAM standards the idea that an SDRAM device must have the ability to internally precharge a bank without first receiving a separate precharge command.

**RESPONSE TO REQUEST FOR ADMISSION NO. 192:**

Rambus objects to this request as duplicative of Request No. 188, and incorporates its objections and response thereto.

**REQUEST FOR ADMISSION NO. 193:**

Admit that, between December 1991 and June 1996, various members of the JEDEC 42.3 Subcommittee made presentations showing data output occurring on both edges of an external clock.

**RESPONSE TO REQUEST FOR ADMISSION NO. 193:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "showing," both edges," and "external clock." Rambus further objects that the request is vague and ambiguous as to what it means for data to be output "on" an edge of an external clock. Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

After having made reasonable inquiry, the information known to or readily obtainable by Rambus is insufficient for Rambus to admit or deny the request.

**REQUEST FOR ADMISSION NO. 194:**

Admit that, between December 1991 and June 1996, Rambus knew that various members of the JEDEC 42.3 Subcommittee made presentations showing data output occurring on both edges of an external clock.

**RESPONSE TO REQUEST FOR ADMISSION NO. 194:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "showing," both edges," and "external clock." Rambus further objects that the request is vague and ambiguous as to what it means for data to be output "on" an edge of an external clock. Rambus further objects on the ground that the request is vague and ambiguous as to what would constitute "knowledge" on the part of Rambus.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 195:**

Admit that, between December 1991 and June 1996, various members of the JEDEC 42.3 Subcommittee made presentations proposing to incorporate into JEDEC SDRAM standards data output occurring on both edges of an external clock.

**RESPONSE TO REQUEST FOR ADMISSION NO. 195:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "both edges," "external clock," and "JEDEC SDRAM standards." Rambus further objects that the request is vague and ambiguous as to what it means for data to be output "on" an edge of an external clock. Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such

presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

After having made reasonable inquiry, the information known to or readily obtainable by Rambus is insufficient for Rambus to admit or deny the request.

**REQUEST FOR ADMISSION NO. 196:**

Admit that, between December 1991 and June 1996, Rambus knew that various members of the JEDEC 42.3 Subcommittee made presentations proposing to incorporate into JEDEC SDRAM standards data output occurring on both edges of an external clock.

**RESPONSE TO REQUEST FOR ADMISSION NO. 196:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "both edges," "external clock," and "JEDEC SDRAM standards." Rambus further objects that the request is vague and ambiguous as to what it means for data to be output "on" an edge of an external clock. Rambus further objects on the ground that the request is vague and ambiguous as to what would constitute "knowledge" on the part of Rambus.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 197:**

Admit that, between December 1991 and June 1996, various members of the JEDEC 42.3 Subcommittee made presentations showing the output of a first portion of data in response to a rising edge of a clock signal and a second portion of data in response to a falling edge of a clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 197:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "showing," "first portion of data," "second portion of data," "in response to," and "a clock signal." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

After having made reasonable inquiry, the information known to or readily obtainable by Rambus is insufficient for Rambus to admit or deny the request.

**REQUEST FOR ADMISSION NO. 198:**

Admit that, between December 1991 and June 1996, Rambus knew that various members of the JEDEC 42.3 Subcommittee made presentations showing the output of a first portion of data in response to a rising edge of a clock signal and a second portion of data in response to a falling edge of a clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 198:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "showing," "first portion of data," "second portion of data," "in response to," and "a clock signal." Rambus further objects that the request is vague and ambiguous as to what it means for data to be output "on" an edge of an external clock. Rambus further objects on the ground that the request is vague and ambiguous as to what would constitute "knowledge" on the part of Rambus.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 199:**

Admit that, between December 1991 and June 1996, various members of the JEDEC 42.3 Subcommittee made presentations proposing to incorporate into JEDEC SDRAM standards the output of a first portion of data in response to a rising edge of a clock signal and a second portion of data in response to a falling edge of a clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 199:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "first portion of data," "second portion of data," "in response to," "a clock signal." and "JEDEC SDRAM standards." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

After having made reasonable inquiry, the information known to or readily obtainable by Rambus is insufficient for Rambus to admit or deny the request.

**REQUEST FOR ADMISSION NO. 200:**

Admit that, between December 1991 and June 1996, Rambus knew that various members of the JEDEC 42.3 Subcommittee made presentations proposing to incorporate into JEDEC SDRAM standards the output of a first portion of data in response to a rising edge of a clock signal and a second portion of data in response to a falling edge of a clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 200:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "first portion of data," "second portion of data," "in response to," "a clock signal." and "JEDEC SDRAM standards." Rambus further objects on the

ground that the request is vague and ambiguous as to what would constitute "knowledge" on the part of Rambus.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 201:**

Admit that, between December 1991 and June 1996, various members of the JEDEC 42.3 Subcommittee made presentations showing the input of a first portion of data in response to a rising edge of a data strobe and a second portion of data in response to a falling edge of a data strobe.

**RESPONSE TO REQUEST FOR ADMISSION NO. 201:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "showing," "first portion of data," "second portion of data," "in response to," and "a data strobe." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that IBM made a presentation regarding an "HST" [high speed toggle] DRAM in December 1991. (Minutes of JC 42.3 Meeting No. 60, Attachment M.) To the extent that this HST DRAM is considered to input a first portion of data in response to a rising edge of a data strobe and a second portion of data in response to a falling edge of a data strobe within the meaning of the request, Rambus admits that IBM made a presentation relating to this feature.

After having made reasonable inquiry, the information known to or readily obtainable by Rambus is insufficient for Rambus to further admit or deny the request.

**REQUEST FOR ADMISSION NO. 202:**

Admit that, between December 1991 and June 1996, Rambus knew that various members of the JEDEC 42.3 Subcommittee made presentations showing the input of a first portion of data in response to a rising edge of a data strobe and a second portion of data in response to a falling edge of a data strobe.

**RESPONSE TO REQUEST FOR ADMISSION NO. 202:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "showing," "first portion of data," "second portion of data," "in response to," and "a data strobe." Rambus further objects on the ground that the request is vague and ambiguous as to what would constitute "knowledge" on the part of Rambus.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that certain Rambus employees knew, at certain times between December 1991 and June 1996, that IBM made a presentation regarding an "HST" [high speed toggle] DRAM in December 1991. (Minutes of JC 42.3 Meeting No. 60, Attachment M.) To the extent that this HST DRAM is considered to input a first portion of data in response to a rising edge of a data strobe and a second portion of data in response to a falling edge of a data strobe within the meaning of the request, Rambus admits that certain Rambus employees knew that IBM made a presentation relating to this feature.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 203:**

Admit that, between December 1991 and June 1996, various members of the JEDEC 42.3 Subcommittee made presentations proposing to incorporate into JEDEC SDRAM standards the input of a first portion of data in response to a rising edge of a data strobe and a second portion of data in response to a falling edge of a data strobe.

**RESPONSE TO REQUEST FOR ADMISSION NO. 203:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least

with respect to the terms "presentations," "first portion of data," "second portion of data," "in response to," "a data strobe," and "JEDEC SDRAM standards." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

After having made reasonable inquiry, the information known to or readily obtainable by Rambus is insufficient for Rambus to admit or deny the request.

**REQUEST FOR ADMISSION NO. 204:**

Admit that, between December 1991 and June 1996, Rambus knew that various members of the JEDEC 42.3 Subcommittee made presentations proposing to incorporate into JEDEC SDRAM standards the input of a first portion of data in response to a rising edge of a data strobe and a second portion of data in response to a falling edge of a data strobe.

**RESPONSE TO REQUEST FOR ADMISSION NO. 204:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "first portion of data," "second portion of data," "in response to," "a data strobe," and "JEDEC SDRAM standards." Rambus further objects on the ground that the request is vague and ambiguous as to what would constitute "knowledge" on the part of Rambus.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 205:**

Admit that, between December 1991 and June 1996, various members of the JEDEC 42.3

Subcommittee made presentations showing the output a first portion of data synchronously with respect to a rising edge of an external clock signal and a second portion of data synchronously with respect to a falling edge of the external clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 205:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "showing," "first portion of data," "second portion of data," "synchronously," and "an external clock signal." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

After having made reasonable inquiry, the information known to or readily obtainable by Rambus is insufficient for Rambus to admit or deny the request.

**REQUEST FOR ADMISSION NO. 206:**

Admit that, between December 1991 and June 1996, Rambus knew that various members of the JEDEC 42.3 Subcommittee made presentations showing the output a first portion of data synchronously with respect to a rising edge of an external clock signal and a second portion of data synchronously with respect to a falling edge of the external clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 206:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "showing," "first portion of data," "second portion of data," "synchronously," and "an external clock signal." Rambus further objects on the ground that the request is vague and ambiguous as to what would constitute "knowledge" on the part of Rambus.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 207:**

Admit that, between December 1991 and June 1996, various members of the JEDEC 42.3 Subcommittee made presentations proposing to incorporate into JEDEC SDRAM standards the output a first portion of data synchronously with respect to a rising edge of an external clock signal and a second portion of data synchronously with respect to a falling edge of the external clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 207:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "first portion of data," "second portion of data," "synchronously," "an external clock signal." and "JEDEC SDRAM standards." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

After having made reasonable inquiry, the information known to or readily obtainable by Rambus is insufficient for Rambus to admit or deny the request.

**REQUEST FOR ADMISSION NO. 208:**

Admit that, between December 1991 and June 1996, Rambus knew that various members of the JEDEC 42.3 Subcommittee made presentations proposing to incorporate into JEDEC SDRAM standards the output a first portion of data synchronously with respect to a rising edge of an external clock signal and a second portion of data synchronously with respect to a falling

edge of the external clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 208:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "first portion of data," "second portion of data," "synchronously," "an external clock signal." and "JEDEC SDRAM standards." Rambus further objects on the ground that the request is vague and ambiguous as to what would constitute "knowledge" on the part of Rambus.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 209:**

Admit that, between December 1991 and June 1996, various members of the JEDEC 42.3 Subcommittee made presentations showing the input a first portion of data synchronously with respect to a rising edge of an external data strobe and a second portion of data synchronously with respect to a falling edge of the external data strobe.

**RESPONSE TO REQUEST FOR ADMISSION NO. 209:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "showing," "first portion of data," "second portion of data," "synchronously," and "an external data strobe." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that IBM made a presentation regarding an "HST" [high speed toggle] DRAM in December 1991. (Minutes of JC 42.3 Meeting No. 60, Attachment M.) To the extent

that this HST DRAM is considered to input a first portion of data synchronously with respect to a rising edge of an external data strobe and a second portion of data synchronously with respect to a falling edge of the external data strobe within the meaning of the request, Rambus admits that IBM made a presentation relating to this feature.

After having made reasonable inquiry, the information known to or readily obtainable by Rambus is insufficient for Rambus to further admit or deny the request.

**REQUEST FOR ADMISSION NO. 210:**

Admit that, between December 1991 and June 1996, Rambus knew that various members of the JEDEC 42.3 Subcommittee made presentations showing the input a first portion of data synchronously with respect to a rising edge of an external data strobe and a second portion of data synchronously with respect to a falling edge of the external data strobe.

**RESPONSE TO REQUEST FOR ADMISSION NO. 210:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "showing," "first portion of data," "second portion of data," "synchronously," and "an external data strobe." Rambus further objects on the ground that the request is vague and ambiguous as to what would constitute "knowledge" on the part of Rambus.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that certain Rambus employees knew, at certain times between December 1991 and June 1996, that IBM made a presentation regarding an "HST" [high speed toggle] DRAM in December 1991. (Minutes of JC 42.3 Meeting No. 60, Attachment M.) To the extent that this HST DRAM is considered to input a first portion of data synchronously with respect to a rising edge of an external data strobe and a second portion of data synchronously with respect to a falling edge of the external data strobe within the meaning of the request, Rambus admits that certain Rambus employees knew that IBM made a presentation relating to this feature.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 211:**

Admit that, between December 1991 and June 1996, various members of the JEDEC 42.3 Subcommittee made presentations proposing to incorporate into JEDEC SDRAM standards the input a first portion of data synchronously with respect to a rising edge of an external clock signal and a second portion of data synchronously with respect to a falling edge of the external data strobe.

**RESPONSE TO REQUEST FOR ADMISSION NO. 211:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "first portion of data," "second portion of data," "synchronously," "an external clock signal," "the external data strobe," and "JEDEC SDRAM standards." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

After having made reasonable inquiry, the information known to or readily obtainable by Rambus is insufficient for Rambus to admit or deny the request.

**REQUEST FOR ADMISSION NO. 212:**

Admit that, between December 1991 and June 1996, Rambus knew that various members of the JEDEC 42.3 Subcommittee made presentations proposing to incorporate into JEDEC SDRAM standards the input a first portion of data synchronously with respect to a rising edge of an external clock signal and a second portion of data synchronously with respect to a falling edge of the external data strobe.

**RESPONSE TO REQUEST FOR ADMISSION NO. 212:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "first portion of data," "second portion of data," "synchronously," "an external clock signal," "the external data strobe," and "JEDEC SDRAM standards." Rambus further objects on the ground that the request is vague and ambiguous as to what would constitute "knowledge" on the part of Rambus.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 213:**

Admit that, between December 1991 and June 1996, various members of the JEDEC 42.3 Subcommittee made presentations showing the input a first portion of data synchronously with respect to a first external data strobe and a second portion of data synchronously with respect to a second external data strobe.

**RESPONSE TO REQUEST FOR ADMISSION NO. 213:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "showing," "first portion of data," "second portion of data," "synchronously," "first external data strobe," and "second external data strobe." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

After having made reasonable inquiry, the information known to or readily obtainable by Rambus is insufficient for Rambus to admit or deny the request.

**REQUEST FOR ADMISSION NO. 214:**

Admit that, between December 1991 and June 1996, Rambus knew that various members of the JEDEC 42.3 Subcommittee made presentations showing the input a first portion of data synchronously with respect to a first external data strobe and a second portion of data synchronously with respect to a second external data strobe.

**RESPONSE TO REQUEST FOR ADMISSION NO. 214:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "showing," "first portion of data," "second portion of data," "synchronously," "first external data strobe," and "second external data strobe." Rambus further objects on the ground that the request is vague and ambiguous as to what would constitute "knowledge" on the part of Rambus.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 215:**

Admit that, between December 1991 and June 1996, various members of the JEDEC 42.3 Subcommittee made presentations proposing to incorporate into JEDEC SDRAM standards the input a first portion of data synchronously with respect to a first external data strobe and a second portion of data synchronously with respect to a second external data strobe.

**RESPONSE TO REQUEST FOR ADMISSION NO. 215:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "first portion of data," "second portion of data," "synchronously," "first external data strobe," "second external data strobe," and "JEDEC SDRAM standards." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to

presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

After having made reasonable inquiry, the information known to or readily obtainable by Rambus is insufficient for Rambus to admit or deny the request.

**REQUEST FOR ADMISSION NO. 216:**

Admit that, between December 1991 and June 1996, Rambus knew that various members of the JEDEC 42.3 Subcommittee made presentations proposing to incorporate into JEDEC SDRAM standards the input a first portion of data synchronously with respect to a first external data strobe and a second portion of data synchronously with respect to a second external data strobe.

**RESPONSE TO REQUEST FOR ADMISSION NO. 216:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "first portion of data," "second portion of data," "synchronously," "first external data strobe," "second external data strobe," and "JEDEC SDRAM standards." Rambus further objects on the ground that the request is vague and ambiguous as to what would constitute "knowledge" on the part of Rambus.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 217:**

Admit that, between December 1991 and June 1996, various members of the JEDEC 42.3 Subcommittee made presentations showing the output a first portion of data synchronously with respect to a first external clock signal and a second portion of data synchronously with respect to a second external clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 217:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least

with respect to the terms "presentations," "showing," "first portion of data," "second portion of data," "synchronously," "first external clock signal," and "second external clock signal." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

After having made reasonable inquiry, the information known to or readily obtainable by Rambus is insufficient for Rambus to admit or deny the request.

**REQUEST FOR ADMISSION NO. 218:**

Admit that, between December 1991 and June 1996, Rambus knew that various members of the JEDEC 42.3 Subcommittee made presentations showing the output a first portion of data synchronously with respect to a first external clock signal and a second portion of data synchronously with respect to a second external clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 218:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "showing," "first portion of data," "second portion of data," "synchronously," "first external clock signal," and "second external clock signal." Rambus further objects on the ground that the request is vague and ambiguous as to what would constitute "knowledge" on the part of Rambus.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 219:**

Admit that, between December 1991 and June 1996, various members of the JEDEC 42.3

Subcommittee made presentations proposing to incorporate into JEDEC SDRAM standards the output a first portion of data synchronously with respect to a first external clock signal and a second portion of data synchronously with respect to a second external clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 219:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "first portion of data," "second portion of data," "synchronously," "first external clock signal," "second external clock signal," and "JEDEC SDRAM standards." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

After having made reasonable inquiry, the information known to or readily obtainable by Rambus is insufficient for Rambus to admit or deny the request.

**REQUEST FOR ADMISSION NO. 220:**

Admit that, between December 1991 and June 1996, Rambus knew that various members of the JEDEC 42.3 Subcommittee made presentations proposing to incorporate into JEDEC SDRAM standards the output a first portion of data synchronously with respect to a first external clock signal and a second portion of data synchronously with respect to a second external clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 220:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "first portion of data," "second portion of data," "synchronously," "first external clock signal," "second external clock signal," and "JEDEC SDRAM standards." Rambus further objects on the ground that the request is vague and

ambiguous as to what would constitute "knowledge" on the part of Rambus.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 221:**

Admit that, between December 1991 and June 1996, various members of the JEDEC 42.3 Subcommittee made presentations showing the input a first portion of data synchronously with respect to a first external data strobe and a second portion of data synchronously with respect to a second external data strobe.

**RESPONSE TO REQUEST FOR ADMISSION NO. 221:**

Rambus objects to this request as duplicative of Request No. 213, and incorporates its objections and response thereto.

**REQUEST FOR ADMISSION NO. 222:**

Admit that, between December 1991 and June 1996, Rambus knew that various members of the JEDEC 42.3 Subcommittee made presentations showing the input a first portion of data synchronously with respect to a first external data strobe and a second portion of data synchronously with respect to a second external data strobe.

**RESPONSE TO REQUEST FOR ADMISSION NO. 222:**

Rambus objects to this request as duplicative of Request No. 214, and incorporates its objections and response thereto.

**REQUEST FOR ADMISSION NO. 223:**

Admit that, between December 1991 and June 1996, various members of the JEDEC 42.3 Subcommittee made presentations proposing to incorporate into JEDEC SDRAM standards the input a first portion of data synchronously with respect to a first external data strobe and a second portion of data synchronously with respect to a second external data strobe.

**RESPONSE TO REQUEST FOR ADMISSION NO. 223:**

Rambus objects to this request as duplicative of Request No. 215, and incorporates its objections and response thereto.

**REQUEST FOR ADMISSION NO. 224:**

Admit that, between December 1991 and June 1996, Rambus knew that various members of the JEDEC 42.3 Subcommittee made presentations proposing to incorporate into JEDEC SDRAM standards the input a first portion of data synchronously with respect to a first external data strobe and a second portion of data synchronously with respect to a second external data strobe.

**RESPONSE TO REQUEST FOR ADMISSION NO. 224:**

Rambus objects to this request as duplicative of Request No. 216, and incorporates its objections and response thereto.

**REQUEST FOR ADMISSION NO. 225:**

Admit that, between December 1991 and June 1996, various members of the JEDEC 42.3 Subcommittee made presentations showing the use of a dual edge clocking scheme which inputs and outputs data synchronously with the rising and falling edge of an external clock.

**RESPONSE TO REQUEST FOR ADMISSION NO. 225:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "showing," "dual edge clocking scheme," "synchronously," "the rising and falling edge" and "an external clock." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

After having made reasonable inquiry, the information known to or readily obtainable by Rambus is insufficient for Rambus to admit or deny the request.

**REQUEST FOR ADMISSION NO. 226:**

Admit that, between December 1991 and June 1996, Rambus knew that various members of the JEDEC 42.3 Subcommittee made presentations showing the use of a dual edge clocking scheme which inputs and outputs data synchronously with the rising and falling edge of an external clock.

**RESPONSE TO REQUEST FOR ADMISSION NO. 226:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "showing," "dual edge clocking scheme," "synchronously," "the rising and falling edge" and "an external clock." Rambus further objects on the ground that the request is vague and ambiguous as to what would constitute "knowledge" on the part of Rambus.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 227:**

Admit that, between December 1991 and June 1996, various members of the JEDEC 42.3 Subcommittee made presentations proposing to incorporate into JEDEC SDRAM standards the use of a dual edge clocking scheme which inputs and outputs data synchronously with the rising and falling edge of an external clock.

**RESPONSE TO REQUEST FOR ADMISSION NO. 227:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "dual edge clocking scheme," "synchronously," "the

rising and falling edge," "an external clock," and "JEDEC SDRAM standards." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

After having made reasonable inquiry, the information known to or readily obtainable by Rambus is insufficient for Rambus to admit or deny the request.

**REQUEST FOR ADMISSION NO. 228:**

Admit that, between December 1991 and June 1996, Rambus knew that various members of the JEDEC 42.3 Subcommittee made presentations proposing to incorporate into JEDEC SDRAM standards the use of a dual edge clocking scheme which inputs and outputs data synchronously with the rising and falling edge of an external clock.

**RESPONSE TO REQUEST FOR ADMISSION NO. 228:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "dual edge clocking scheme," "synchronously," "the rising and falling edge," "an external clock," and "JEDEC SDRAM standards." Rambus further objects on the ground that the request is vague and ambiguous as to what would constitute "knowledge" on the part of Rambus.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 229:**

Admit that, between December 1991 and June 1996, various members of the JEDEC 42.3 Subcommittee made presentations showing sampling of data occurring on both edges of an

external clock.

**RESPONSE TO REQUEST FOR ADMISSION NO. 229:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "showing," "sampling of data," "both edges," and "external clock." Rambus further objects that the request is vague and ambiguous as to what it means for data to be sampled "on" an edge of an external clock. Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Mitsubishi made a presentation regarding a "SyncLink SDRAM" in May 1995 which stated: "Reference clock both edges for input." (Minutes of JC 42.3 Meeting No. 75, Attachment BB.) To the extent that this SyncLink SDRAM is considered to sample data on both edges of an external clock within the meaning of this request, Rambus admits that Mitsubishi made a presentation relating to this feature.

After having made reasonable inquiry, the information known to or readily obtainable by Rambus is insufficient for Rambus to further admit or deny the request.

**REQUEST FOR ADMISSION NO. 230:**

Admit that, between December 1991 and June 1996, Rambus knew that various members of the JEDEC 42.3 Subcommittee made presentations showing sampling of data occurring on both edges of an external clock.

**RESPONSE TO REQUEST FOR ADMISSION NO. 230:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "showing," "sampling of data," "both edges," and

"external clock." Rambus further objects that the request is vague and ambiguous as to what it means for data to be sampled "on" an edge of an external clock. Rambus further objects on the ground that the request is vague and ambiguous as to what would constitute "knowledge" on the part of Rambus.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits certain Rambus employees knew at certain times between December 1991 and June 1996 that Mitsubishi made a presentation regarding a "SyncLink SDRAM" in May 1995 which stated: "Reference clock both edges for input." (Minutes of JC 42.3 Meeting No. 75, Attachment BB.) To the extent that this SyncLink SDRAM is considered to sample data on both edges of an external clock within the meaning of this request, Rambus admits that certain Rambus employees knew that Mitsubishi made a presentation relating to this feature.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 231:**

Admit that, between December 1991 and June 1996, various members of the JEDEC 42.3 Subcommittee made presentations proposing to incorporate into JEDEC SDRAM standards sampling of data occurring on both edges of an external clock.

**RESPONSE TO REQUEST FOR ADMISSION NO. 231:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "both edges," "sampling of data," "external clock," and "JEDEC SDRAM standards." Rambus further objects that the request is vague and ambiguous as to what it means for data to be sampled "on" an edge of an external clock. Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

After having made reasonable inquiry, the information known to or readily obtainable by Rambus is insufficient for Rambus to admit or deny the request.

**REQUEST FOR ADMISSION NO. 232:**

Admit that, between December 1991 and June 1996, Rambus knew that various members of the JEDEC 42.3 Subcommittee made presentations proposing to incorporate into JEDEC SDRAM standards sampling of data occurring on both edges of an external clock.

**RESPONSE TO REQUEST FOR ADMISSION NO. 232:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "sampling of data," "both edges," "external clock," and "JEDEC SDRAM standards." Rambus further objects that the request is vague and ambiguous as to what it means for data to be sampled "on" an edge of an external clock. Rambus further objects on the ground that the request is vague and ambiguous as to what would constitute "knowledge" on the part of Rambus.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 233:**

Admit that, between December 1991 and June 1996, various members of the JEDEC 42.3 Subcommittee made presentations showing data output occurring on the rising edge of the external clock and the falling edge of the external clock.

**RESPONSE TO REQUEST FOR ADMISSION NO. 233:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "showing," and "the external clock." Rambus further objects that the request is vague and ambiguous as to what it means for data to be output "on" an edge of an external clock. Rambus further objects on the ground that it is not familiar with all

presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

After having made reasonable inquiry, the information known to or readily obtainable by Rambus is insufficient for Rambus to admit or deny the request.

**REQUEST FOR ADMISSION NO. 234:**

Admit that, between December 1991 and June 1996, Rambus knew that various members of the JEDEC 42.3 Subcommittee made presentations showing data output occurring on the rising edge of the external clock and the falling edge of the external clock.

**RESPONSE TO REQUEST FOR ADMISSION NO. 234:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "showing," and "external clock." Rambus further objects that the request is vague and ambiguous as to what it means for data to be sampled "on" an edge of an external clock. Rambus further objects on the ground that the request is vague and ambiguous as to what would constitute "knowledge" on the part of Rambus.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 235:**

Admit that, between December 1991 and June 1996, various members of the JEDEC 42.3 Subcommittee made presentations proposing to incorporate into JEDEC SDRAM standards data output occurring on the rising edge of the external clock and the falling edge of the external clock.

**RESPONSE TO REQUEST FOR ADMISSION NO. 235:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "the external clock," and "JEDEC SDRAM standards." Rambus further objects that the request is vague and ambiguous as to what it means for data to be output "on" an edge of an external clock. Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

After having made reasonable inquiry, the information known to or readily obtainable by Rambus is insufficient for Rambus to admit or deny the request.

**REQUEST FOR ADMISSION NO. 236:**

Admit that, between December 1991 and June 1996, Rambus knew that various members of the JEDEC 42.3 Subcommittee made presentations proposing to incorporate into JEDEC SDRAM standards data output occurring on the rising edge of the external clock and the falling edge of the external clock.

**RESPONSE TO REQUEST FOR ADMISSION NO. 236:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "external clock," and "JEDEC SDRAM standards." Rambus further objects that the request is vague and ambiguous as to what it means for data to be sampled "on" an edge of an external clock. Rambus further objects on the ground that the request is vague and ambiguous as to what would constitute "knowledge" on the part of Rambus.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 237:**

Admit that, between December 1991 and June 1996, various members of the JEDEC 42.3 Subcommittee made presentations showing sampling of data occurring on the rising edge of the external clock and the falling edge of the external clock.

**RESPONSE TO REQUEST FOR ADMISSION NO. 237:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "showing," "sampling of data," and "the external clock." Rambus further objects that the request is vague and ambiguous as to what it means for data to be sampled "on" an edge of an external clock. Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Mitsubishi made a presentation regarding a "SyncLink SDRAM" in May 1995 which stated: "Reference clock both edges for input." (Minutes of JC 42.3 Meeting No. 75, Attachment BB.) To the extent that this SyncLink SDRAM is considered to sample data on the rising edge of the external clock and the falling edge of the external clock within the meaning of this request, Rambus admits that Mitsubishi made a presentation relating to this feature.

After having made reasonable inquiry, the information known to or readily obtainable by Rambus is insufficient for Rambus to further admit or deny the request.

**REQUEST FOR ADMISSION NO. 238:**

Admit that, between December 1991 and June 1996, Rambus knew that various members of the JEDEC 42.3 Subcommittee made presentations showing sampling of data occurring on the rising edge of the external clock and the falling edge of the external clock.

**RESPONSE TO REQUEST FOR ADMISSION NO. 238:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "showing," "sampling of data," and "external clock." Rambus further objects that the request is vague and ambiguous as to what it means for data to be sampled "on" an edge of an external clock. Rambus further objects on the ground that the request is vague and ambiguous as to what would constitute "knowledge" on the part of Rambus.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits certain Rambus employees knew at certain times between December 1991 and June 1996 that Mitsubishi made a presentation regarding a "SyncLink SDRAM" in May 1995 which stated: "Reference clock both edges for input." (Minutes of JC 42.3 Meeting No. 75, Attachment BB.) To the extent that this SyncLink SDRAM is considered to sample data on the rising edge of the external clock and the falling edge of the external clock within the meaning of this request, Rambus admits that certain Rambus employees knew that Mitsubishi made a presentation relating to this feature.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 239:**

Admit that, between December 1991 and June 1996, various members of the JEDEC 42.3 Subcommittee made presentations proposing to incorporate into JEDEC SDRAM standards sampling of data occurring on the rising edge of the external clock and the falling edge of the external clock.

**RESPONSE TO REQUEST FOR ADMISSION NO. 239:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "sampling of data," "the external clock," and "JEDEC SDRAM standards." Rambus further objects that the request is vague and ambiguous as to what it means for data to be output "on" an edge of an external clock. Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members

between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

After having made reasonable inquiry, the information known to or readily obtainable by Rambus is insufficient for Rambus to admit or deny the request.

**REQUEST FOR ADMISSION NO. 240:**

Admit that, between December 1991 and June 1996, Rambus knew that various members of the JEDEC 42.3 Subcommittee made presentations proposing to incorporate into JEDEC SDRAM standards sampling of data occurring on the rising edge of the external clock and the falling edge of the external clock.

**RESPONSE TO REQUEST FOR ADMISSION NO. 240:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "sampling of data," "external clock," and "JEDEC SDRAM standards." Rambus further objects that the request is vague and ambiguous as to what it means for data to be sampled "on" an edge of an external clock. Rambus further objects on the ground that the request is vague and ambiguous as to what would constitute "knowledge" on the part of Rambus.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**\REQUEST FOR ADMISSION NO. 241:**

Admit that, between December 1991 and June 1996, various members of the JEDEC 42.3 Subcommittee made presentations showing output, in response to a read request, a first portion of data synchronously with respect to a rising edge of an external clock signal and a second

portion of data synchronously with respect to a falling edge of the external clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 241:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "showing," "in response to," "read request," "first portion of data," "second portion of data," "synchronously," and "an external clock signal." Rambus further objects that the request is vague and ambiguous as to what it means for data to be sampled "on" an edge of an external clock. Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

After having made reasonable inquiry, the information known to or readily obtainable by Rambus is insufficient for Rambus to admit or deny the request.

**REQUEST FOR ADMISSION NO. 242:**

Admit that, between December 1991 and June 1996, Rambus knew that various members of the JEDEC 42.3 Subcommittee made presentations showing output, in response to a read request, a first portion of data synchronously with respect to a rising edge of an external clock signal and a second portion of data synchronously with respect to a falling edge of the external clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 242:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "showing," "in response to," "read request," "first portion of data," "second portion of data," "synchronously," and "an external clock signal." Rambus further objects on the ground that the request is vague and ambiguous as to what would constitute "knowledge" on the part of Rambus.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 243:**

Admit that, between December 1991 and June 1996, various members of the JEDEC 42.3 Subcommittee made presentations proposing to incorporate into JEDEC SDRAM standards output, in response to a read request, a first portion of data synchronously with respect to a rising edge of an external clock signal and a second portion of data synchronously with respect to a falling edge of the external clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 243:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "in response to," "read request," "first portion of data," "second portion of data," "synchronously," "an external clock signal," and "JEDEC SDRAM standards." Rambus further objects that the request is vague and ambiguous as to what it means for data to be sampled "on" an edge of an external clock. Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

After having made reasonable inquiry, the information known to or readily obtainable by Rambus is insufficient for Rambus to admit or deny the request.

**REQUEST FOR ADMISSION NO. 244:**

Admit that, between December 1991 and June 1996, Rambus knew that various members of the JEDEC 42.3 Subcommittee made presentations proposing to incorporate into JEDEC

SDRAM standards output, in response to a read request, a first portion of data synchronously with respect to a rising edge of an external clock signal and a second portion of data synchronously with respect to a falling edge of the external clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 244:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "in response to," "read request," "first portion of data," "second portion of data," "synchronously," "an external clock signal," and "JEDEC SDRAM standards." Rambus further objects on the ground that the request is vague and ambiguous as to what would constitute "knowledge" on the part of Rambus.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 245:**

Admit that, between December 1991 and June 1996, various members of the JEDEC 42.3 Subcommittee made presentations showing sampling, in response to a read request, a first portion of data synchronously with respect to a rising edge of an external clock signal and a second portion of data synchronously with respect to a falling edge of the external clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 245:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "showing," "sampling," "in response to," "read request," "first portion of data," "second portion of data," "synchronously," and "an external clock signal." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

After having made reasonable inquiry, the information known to or readily obtainable by Rambus is insufficient for Rambus to admit or deny the request.

**REQUEST FOR ADMISSION NO. 246:**

Admit that, between December 1991 and June 1996, Rambus knew that various members of the JEDEC 42.3 Subcommittee made presentations showing sampling, in response to a read request, a first portion of data synchronously with respect to a rising edge of an external clock signal and a second portion of data synchronously with respect to a falling edge of the external clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 246:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "showing," "sampling," "in response to," "read request," "first portion of data," "second portion of data," "synchronously," and "an external clock signal." Rambus further objects on the ground that the request is vague and ambiguous as to what would constitute "knowledge" on the part of Rambus.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 247:**

Admit that, between December 1991 and June 1996, various members of the JEDEC 42.3 Subcommittee made presentations proposing to incorporate into JEDEC SDRAM standards sampling, in response to a read request, a first portion of data synchronously with respect to a rising edge of an external clock signal and a second portion of data synchronously with respect to a falling edge of the external clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 247:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "sampling," "in response to," "read request," "first

portion of data," "second portion of data," "synchronously," "an external clock signal," and "JEDEC SDRAM standards." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

After having made reasonable inquiry, the information known to or readily obtainable by Rambus is insufficient for Rambus to admit or deny the request.

**REQUEST FOR ADMISSION NO. 248:**

Admit that, between December 1991 and June 1996, Rambus knew that various members of the JEDEC 42.3 Subcommittee made presentations proposing to incorporate into JEDEC SDRAM standards sampling, in response to a read request, a first portion of data synchronously with respect to a rising edge of an external clock signal and a second portion of data synchronously with respect to a falling edge of the external clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 248:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "showing," "sampling," "in response to," "read request," "first portion of data," "second portion of data," "synchronously," "an external clock signal," and "JEDEC SDRAM standards." Rambus further objects on the ground that the request is vague and ambiguous as to what would constitute "knowledge" on the part of Rambus.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 249:**

Admit that, between October and December 1995, the JEDEC 42.3 Subcommittee

circulated a survey ballot asking members whether they believed future generations of SDRAMs could benefit from sampling inputs on both edges of an external clock.

**RESPONSE TO REQUEST FOR ADMISSION NO. 249:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "sampling inputs on both edges of an external clock," "survey ballot," "could benefit," and "future generations of SDRAMs."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that between October and December 1995, the JEDEC 42.3 Subcommittee circulated what purported to be a "survey ballot" asking members, *inter alia*: "Does your company believe future generations of SDRAMs could benefit from using BOTH edges of the clock for sampling inputs?"

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 250:**

Admit that, between October and December 1995, Rambus received a JEDEC 42.3 Subcommittee survey ballot asking members whether they believed future generations of SDRAMs could benefit from sampling inputs on both edges of an external clock.

**RESPONSE TO REQUEST FOR ADMISSION NO. 250:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "sampling inputs on both edges of an external clock," "survey ballot," "could benefit," and "future generations of SDRAMs."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that between October and December 1995 it received what purported to be a JEDEC 42.3 Subcommittee survey ballot asking members, *inter alia*: "Does your company believe future generations of SDRAMs could benefit from using BOTH edges of the clock for sampling inputs?"

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 251:**

Admit that, between October and December 1995, the JEDEC 42.3 Subcommittee circulated a survey ballot asking members whether they believed future generations of SDRAMs could benefit from sampling inputs on the rising edge of an external clock and the falling edge of an external clock.

**RESPONSE TO REQUEST FOR ADMISSION NO. 251:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "sampling inputs on the rising edge of an external clock and the falling edge of an external clock," "survey ballot," "could benefit," and "future generations of SDRAMs."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that between October and December 1995, the JEDEC 42.3 Subcommittee circulated what purported to be a survey ballot asking members, *inter alia*: "Does your company believe future generations of SDRAMs could benefit from using BOTH edges of the clock for sampling inputs?"

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 252:**

Admit that, between October and December 1995, Rambus received a JEDEC 42.3 Subcommittee survey ballot asking members whether they believed future generations of SDRAMs could benefit from sampling inputs on the rising edge of an external clock and the falling edge of an external clock.

**RESPONSE TO REQUEST FOR ADMISSION NO. 252:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "sampling inputs on the rising edge of an external clock and the falling edge of an external clock," "survey ballot," "could benefit," and "future generations of

SDRAMs."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that between October and December 1995 it received what purported to be a JEDEC 42.3 Subcommittee survey ballot asking members, *inter alia*: "Does your company believe future generations of SDRAMs could benefit from using BOTH edges of the clock for sampling inputs?"

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 253:**

Admit that, between December 1991 and June 1996, various members of the JC 42.3 Subcommittee made presentations proposing to incorporate the idea of clocking data on both edges of the clock into JEDEC SDRAM standards.

**RESPONSE TO REQUEST FOR ADMISSION NO. 253:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "idea," "clocking data," "both edges," "the clock," and "JEDEC SDRAM standards." Rambus further objects that the request is vague and ambiguous as to what it means for data to be clocked "on" an edge of an external clock. Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

After having made reasonable inquiry, the information known to or readily obtainable by Rambus is insufficient for Rambus to admit or deny the request.

**REQUEST FOR ADMISSION NO. 254:**

Admit that, between December 1991 and June 1996, Rambus knew that various members of the JC 42.3 Subcommittee made presentations proposing to incorporate the idea of clocking data on both edges of the clock into JEDEC SDRAM standards.

**RESPONSE TO REQUEST FOR ADMISSION NO. 254:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "idea," "clocking data," "both edges," "the clock," and "JEDEC SDRAM standards." Rambus further objects that the request is vague and ambiguous as to what it means for data to be clocked "on" an edge of an external clock. Rambus further objects on the ground that the request is vague and ambiguous as to what would constitute "knowledge" on the part of Rambus.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 255:**

Admit that, between December 1991 and June 1996, various members of the JC 42.3 Subcommittee made presentations proposing to incorporate the use of both edges of the clock for transmission of address, commands, or data into JEDEC SDRAM standards.

**RESPONSE TO REQUEST FOR ADMISSION NO. 255:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "use of both edges," "the clock," "transmission," and "JEDEC SDRAM standards." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

After having made reasonable inquiry, the information known to or readily obtainable by Rambus is insufficient for Rambus to admit or deny the request.

**REQUEST FOR ADMISSION NO. 256:**

Admit that, between December 1991 and June 1996, Rambus knew that various members of the JC 42.3 Subcommittee made presentations proposing to incorporate the use of both edges of the clock for transmission of address, commands, or data into JEDEC SDRAM standards.

**RESPONSE TO REQUEST FOR ADMISSION NO. 256:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "use of both edges," "the clock," "transmission," and "JEDEC SDRAM standards." Rambus further objects that the request is vague and ambiguous as to what it means for data to be clocked "on" an edge of an external clock. Rambus further objects on the ground that the request is vague and ambiguous as to what would constitute "knowledge" on the part of Rambus.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 257:**

Admit that, between December 1991 and June 1996, various members of the JC 42.3 Subcommittee made presentations proposing to incorporate the idea of a receiver circuit for latching information in response to a rising edge of the clock signal to the falling edge of the clock signal into JEDEC SDRAM standards.

**RESPONSE TO REQUEST FOR ADMISSION NO. 257:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "idea," "receiver circuit for latching information," "in response to," "the clock signal," and "JEDEC SDRAM standards." Rambus further objects that the request is unintelligible in its reference to "latching information in response to a rising edge

of the clock signal to the falling edge of the clock signal." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

**REQUEST FOR ADMISSION NO. 258:**

Admit that, between December 1991 and June 1996, Rambus knew that various members of the JC 42.3 Subcommittee made presentations proposing to incorporate the idea of a receiver circuit for latching information in response to a rising edge of the clock signal to the falling edge of the clock signal into JEDEC SDRAM standards.

**RESPONSE TO REQUEST FOR ADMISSION NO. 258:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "idea," "receiver circuit for latching information," "in response to," "the clock signal," and "JEDEC SDRAM standards." Rambus further objects that the request is unintelligible in its reference to "latching information in response to a rising edge of the clock signal to the falling edge of the clock signal." Rambus further objects on the ground that the request is vague and ambiguous as to what would constitute "knowledge" on the part of Rambus.

**REQUEST FOR ADMISSION NO. 259:**

Admit that, between December 1991 and June 1996, various members of the JEDEC 42.3 Subcommittee made presentations showing on-chip PLL or on-chip DLL circuitry.

**RESPONSE TO REQUEST FOR ADMISSION NO. 259:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "showing," "on-chip PLL," and "on-chip DLL."

Rambus further objects to the request as compound. Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that certain presentations made by members of the JEDEC 42.3 Subcommittee between December 1991 and June 1996 included terms such as, for example, "Phase Locks," "PLL," "on-chip PLL," and "on chip PLL/DLL," without showing corresponding circuitry.

After having made reasonable inquiry, the information known to or readily obtainable by Rambus is insufficient for Rambus to admit or deny the request.

**REQUEST FOR ADMISSION NO. 260:**

Admit that, between December 1991 and June 1996, Rambus knew that various members of the JEDEC 42.3 Subcommittee made presentations showing on-chip PLL or on-chip DLL circuitry.

**RESPONSE TO REQUEST FOR ADMISSION NO. 260:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "showing," "on-chip PLL," and "on-chip DLL." Rambus further objects to the request as compound. Rambus further objects on the ground that the request is vague and ambiguous as to what would constitute "knowledge" on the part of Rambus.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits at certain times December 1991 and June 1996 certain Rambus employees knew that certain presentations made by members of the JEDEC 42.3 Subcommittee included terms such as, for example, "Phase Locks," "PLL," "On-Chip PLL," and "On Chip

PLL/DLL," without showing corresponding circuitry.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 261:**

Admit that, between December 1991 and June 1996, various members of the JEDEC 42.3 Subcommittee made presentations proposing to incorporate into JEDEC SDRAM standards on-chip PLL or on-chip DLL circuitry.

**RESPONSE TO REQUEST FOR ADMISSION NO. 261:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "on-chip PLL," "on-chip DLL," and "JEDEC SDRAM standards." Rambus further objects to the request as compound. Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that certain presentations made by members of the JEDEC 42.3 Subcommittee, designated as relating to "SDRAM," between December 1991 and June 1996 included terms such as, for example, "PLL," and "on chip PLL/DLL," without showing corresponding circuitry.

After having made reasonable inquiry, the information known to or readily obtainable by Rambus is insufficient for Rambus to admit or deny the request.

**REQUEST FOR ADMISSION NO. 262:**

Admit that, between December 1991 and June 1996, Rambus knew that various members of the JEDEC 42.3 Subcommittee made presentations proposing to incorporate into JEDEC

SDRAM standards on-chip PLL or on-chip DLL circuitry.

**RESPONSE TO REQUEST FOR ADMISSION NO. 262:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "on-chip PLL," "on-chip DLL," and "JEDEC SDRAM standards." Rambus further objects to the request as compound. Rambus further objects on the ground that the request is vague and ambiguous as to what would constitute "knowledge" on the part of Rambus.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at certain times between December 1991 and June 1996 certain Rambus employees knew that certain presentations made by members of the JEDEC 42.3 Subcommittee, designating as relating to "SDRAM," included terms such as, for example, "PLL," "On-Chip PLL," and "On Chip PLL/DLL," without showing corresponding circuitry.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 263:**

Admit that, between December 1991 and June 1996, various members of the JEDEC 42.3 Subcommittee made presentations showing phase locked loop circuitry or delay locked loop circuitry to generate an internal clock signal using an external clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 263:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "showing," "on-chip PLL," and "on-chip DLL." Rambus further objects to the request as compound. Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that certain presentations made by members of the JEDEC 42.3 Subcommittee between December 1991 and June 1996 included terms such as, for example, "Phase Locks," "PLL," "on-chip PLL," and "on chip PLL/DLL," without showing corresponding circuitry. Rambus also admits that NEC made a presentation on or about September 14, 1994 showing, *inter alia*, a "PLL Enable Mode (Option)" for a "16M SDRAM Mode Register," including a diagram, labeled "On-Chip-PLL Improves Access Time (tAC), with a block designated "PLL" receiving a signal designated "CLK" and apparently generating a signal designated "iCLK."

After having made reasonable inquiry, the information known to or readily obtainable by Rambus is insufficient for Rambus to admit or deny the request.

**REQUEST FOR ADMISSION NO. 264:**

Admit that, between December 1991 and June 1996, Rambus knew that various members of the JEDEC 42.3 Subcommittee made presentations showing phase locked loop circuitry or delay locked loop circuitry to generate an internal clock signal using an external clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 264:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "showing," "on-chip PLL," and "on-chip DLL." Rambus further objects to the request as compound. Rambus further objects on the ground that the request is vague and ambiguous as to what would constitute "knowledge" on the part of Rambus.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at certain times between December 1991 and June 1996 certain Rambus employees knew that certain presentations made by members of the JEDEC 42.3 Subcommittee included terms such as, for example, "Phase Locks," "PLL," "on-chip PLL," and "on chip PLL/DLL," without showing corresponding circuitry. Rambus also admits certain Rambus employees knew that NEC made a presentation on or about September 14, 1994

showing, *inter alia*, a "PLL Enable Mode (Option)" for a "16M SDRAM Mode Register," including a diagram, labeled "On-Chip-PLL Improves Access Time (tAC), with a block designated "PLL" receiving a signal designated "CLK" and apparently generating a signal designated "iCLK."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 265:**

Admit that, between December 1991 and June 1996, various members of the JEDEC 42.3 Subcommittee made presentations proposing to incorporate into JEDEC SDRAM standards phase locked loop circuitry or delay locked loop circuitry to generate an internal clock signal using an external clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 265:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "on-chip PLL," "on-chip DLL," and "JEDEC SDRAM standards." Rambus further objects to the request as compound. Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that certain presentations made by members of the JEDEC 42.3 Subcommittee between December 1991 and June 1996, designated as relating to "SDRAM," included terms such as, for example, " "PLL," "on-chip PLL," and "on chip PLL/DLL," without showing corresponding circuitry. Rambus also admits that NEC made a presentation on or about September 14, 1994 showing, *inter alia*, a "PLL Enable Mode (Option)" for a "16M SDRAM Mode Register," including a diagram, labeled "On-Chip-PLL Improves Access Time (tAC), with

a block designated "PLL" receiving a signal designated "CLK" and apparently generating a signal designated "iCLK."

After having made reasonable inquiry, the information known to or readily obtainable by Rambus is insufficient for Rambus to further admit or deny the request.

**REQUEST FOR ADMISSION NO. 266:**

Admit that, between December 1991 and June 1996, Rambus knew that various members of the JEDEC 42.3 Subcommittee made presentations proposing to incorporate into JEDEC SDRAM standards phase locked loop circuitry or delay locked loop circuitry to generate an internal clock signal using an external clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 266:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "on-chip PLL," "on-chip DLL," and "JEDEC SDRAM standards." Rambus further objects to the request as compound. Rambus further objects on the ground that the request is vague and ambiguous as to what would constitute "knowledge" on the part of Rambus.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at certain times between December 1991 and June 1996 certain Rambus employees knew that certain presentations made by members of the JEDEC 42.3 Subcommittee, designated as relating to "SDRAM," included terms such as, for example, "Phase Locks," "PLL," "on-chip PLL," and "on chip PLL/DLL," without showing corresponding circuitry. Rambus also admits certain Rambus employees knew that NEC made a presentation on or about September 14, 1994 showing, *inter alia*, a "PLL Enable Mode (Option)" for a "16M SDRAM Mode Register," including a diagram, labeled "On-Chip-PLL Improves Access Time (tAC), with a block designated "PLL" receiving a signal designated "CLK" and apparently generating a signal designated "iCLK."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 267:**

Admit that, between October and December 1995, the JEDEC 42.3 Subcommittee circulated a survey ballot asking members whether they believed an on-chip PLL or DLL was important for future generations of SDRAMs.

**RESPONSE TO REQUEST FOR ADMISSION NO. 267:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "survey ballot," "on-chip PLL or DLL," "important," and "future generations of SDRAMs."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that between October and December 1995, the JEDEC 42.3 Subcommittee circulated what purported to be a survey ballot asking members, *inter alia*: "Does your company believe that an on chip PLL or DLL is important to reduce the access time from the clock for future generations of SDRAMs."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 268:**

Admit that, between October and December 1995, Rambus received a JEDEC 42.3 Subcommittee survey ballot asking members whether they believed an on-chip PLL or DLL was important for future generations of SDRAMs.

**RESPONSE TO REQUEST FOR ADMISSION NO. 268:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "survey ballot," "on-chip PLL or DLL," "important," and "future generations of SDRAMs."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that between October and December 1995, it received what purported to be a JEDEC 42.3 Subcommittee survey ballot asking members, *inter alia*: "Does your company

believe that an on chip PLL or DLL is important to reduce the access time from the clock for future generations of SDRAMs."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 269:**

Admit that, between December 1991 and June 1996, various members of the JC 42.3 Subcommittee made presentations proposing to incorporate having phase lock loop on DRAM to control delays inside and outside DRAM into JEDEC SDRAM standards.

**RESPONSE TO REQUEST FOR ADMISSION NO. 269:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "having phase lock loop on DRAM" "control delays inside and outside DRAM," and "JEDEC SDRAM standards." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at certain times between December 1991 and June 1996 certain Rambus employees knew that certain presentations made by members of the JEDEC 42.3 Subcommittee, designated as relating to "SDRAM," included terms such as, for example, "Phase Locks," "PLL," "on-chip PLL," and "on chip PLL/DLL," without showing corresponding circuitry. Rambus also admits certain Rambus employees knew that NEC made a presentation on or about September 14, 1994 showing, *inter alia*, a "PLL Enable Mode (Option)" for a "16M SDRAM Mode Register" and stating as an "Advantage[] of On-Chip PLL" that it "Improves access time."

After having made reasonable inquiry, the information known to or readily obtainable by

Rambus is insufficient for Rambus to admit or deny the request.

**REQUEST FOR ADMISSION NO. 270:**

Admit that, between December 1991 and June 1996, Rambus knew that various members of the JC 42.3 Subcommittee made presentations proposing to incorporate having phase lock loop on DRAM to control delays inside and outside DRAM into JEDEC SDRAM standards.

**RESPONSE TO REQUEST FOR ADMISSION NO. 270:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "phase lock loop on DRAM" "control delays inside and outside DRAM," and "JEDEC SDRAM standards." Rambus further objects to the request as compound. Rambus further objects on the ground that the request is vague and ambiguous as to what would constitute "knowledge" on the part of Rambus.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at certain times between December 1991 and June 1996 certain Rambus employees knew that certain presentations made by members of the JEDEC 42.3 Subcommittee, designated as relating to "SDRAM," included terms such as, for example, "Phase Locks," "PLL," "on-chip PLL," and "on chip PLL/DLL," without showing corresponding circuitry. Rambus also admits certain Rambus employees knew that NEC made a presentation on or about September 14, 1994 showing, *inter alia*, a "PLL Enable Mode (Option)" for a "16M SDRAM Mode Register" and stating as an "Advantage[] of On-Chip PLL" that it "Improves access time."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 271:**

Admit that, between December 1991 and June 1996, various members of the JC 42.3 Subcommittee made presentations proposing to incorporate using a PLL/DLL circuit on a DRAM to reduce input buffer skews into JEDEC SDRAM standards.

**RESPONSE TO REQUEST FOR ADMISSION NO. 271:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "PLL/DLL circuit" "input buffer skews," and "JEDEC SDRAM standards." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at certain times between December 1991 and June 1996 certain Rambus employees knew that certain presentations made by members of the JEDEC 42.3 Subcommittee, designated as relating to "SDRAM," included terms such as, for example, "PLL," "on-chip PLL," and "on chip PLL/DLL."

After having made reasonable inquiry, the information known to or readily obtainable by Rambus is insufficient for Rambus to admit or deny the request.

**REQUEST FOR ADMISSION NO. 272:**

Admit that, between December 1991 and June 1996, Rambus knew that various members of the JC 42.3 Subcommittee made presentations proposing to incorporate using a PLL/DLL circuit on a DRAM to reduce input buffer skews into JEDEC SDRAM standards.

**RESPONSE TO REQUEST FOR ADMISSION NO. 272:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "PLL/DLL circuit" "input buffer skews," and "JEDEC SDRAM standards." Rambus further objects to the request as compound. Rambus further objects on the ground that the request is vague and ambiguous as to what would constitute "knowledge" on the part of Rambus.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at certain times between December 1991 and June 1996 certain Rambus employees knew that certain presentations made by members of the JEDEC 42.3 Subcommittee, designated as relating to "SDRAM," included terms such as, for example, "PLL," "on-chip PLL," and "on chip PLL/DLL."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 273:**

Admit that, between December 1991 and June 1996, various members of the JC 42.3 Subcommittee made presentations proposing to incorporate a DRAM with PLL clock generation into the JEDEC SDRAM standards.

**RESPONSE TO REQUEST FOR ADMISSION NO. 273:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "incorporate a DRAM . . . into the JEDEC SDRAM standards," "PLL clock generation," and "JEDEC SDRAM standards." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that certain presentations made by members of the JEDEC 42.3 Subcommittee between December 1991 and June 1996, designated as relating to "SDRAM," included terms such as, for example, " "PLL," "on-chip PLL," and "on chip PLL/DLL." Rambus also admits that NEC made a presentation on or about September 14, 1994 showing, *inter alia*, a "PLL Enable Mode (Option)" for a "16M SDRAM Mode Register," including a diagram, labeled "On-Chip-PLL Improves Access Time (tAC), with a block designated "PLL" receiving a signal designated "CLK" and apparently generating a signal designated "iCLK."

After having made reasonable inquiry, the information known to or readily obtainable by Rambus is insufficient for Rambus to further admit or deny the request.

**REQUEST FOR ADMISSION NO. 274:**

Admit that, between December 1991 and June 1996, Rambus knew that various members of the JC 42.3 Subcommittee made presentations proposing to incorporate a DRAM with PLL clock generation into the JEDEC SDRAM standards.

**RESPONSE TO REQUEST FOR ADMISSION NO. 274:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "incorporate a DRAM . . . into the JEDEC SDRAM standards," "PLL clock generation," and "JEDEC SDRAM standards." Rambus further objects to the request as compound. Rambus further objects on the ground that the request is vague and ambiguous as to what would constitute "knowledge" on the part of Rambus.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at certain times between December 1991 and June 1996 certain Rambus employees knew that certain presentations made by members of the JEDEC 42.3 Subcommittee, designated as relating to "SDRAM," included terms such as, for example, "PLL," "on-chip PLL," and "on chip PLL/DLL." Rambus also admits certain Rambus employees knew that NEC made a presentation on or about September 14, 1994 showing, *inter alia*, a "PLL Enable Mode (Option)" for a "16M SDRAM Mode Register," including a diagram, labeled "On-Chip-PLL Improves Access Time (tAC), with a block designated "PLL" receiving a signal designated "CLK" and apparently generating a signal designated "iCLK."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 275:**

Admit that, between December 1991 and June 1996, various members of the JC 42.3 Subcommittee made presentations proposing to incorporate using a PLL on an SDRAM into the

JEDEC standards.

**RESPONSE TO REQUEST FOR ADMISSION NO. 275:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "using a PLL on an SDRAM" "PLL," and "JEDEC standards." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that certain presentations made by members of the JEDEC 42.3 Subcommittee between December 1991 and June 1996, designated as relating to "SDRAM," included terms such as, for example, "PLL," "on-chip PLL," and "on chip PLL/DLL."

After having made reasonable inquiry, the information known to or readily obtainable by Rambus is insufficient for Rambus to further admit or deny the request.

**REQUEST FOR ADMISSION NO. 276:**

Admit that, between December 1991 and June 1996, Rambus knew that various members of the JC 42.3 Subcommittee made presentations proposing to incorporate using a PLL on an SDRAM into the JEDEC standards.

**RESPONSE TO REQUEST FOR ADMISSION NO. 276:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "using a PLL on an SDRAM" "PLL," and "JEDEC standards." Rambus further objects to the request as compound. Rambus further objects on the ground that the request is vague and ambiguous as to what would constitute "knowledge" on the part of Rambus.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at certain times between December 1991 and June 1996 certain Rambus employees knew that certain presentations made by members of the JEDEC 42.3 Subcommittee, designated as relating to "SDRAM," included terms such as, for example, "PLL," "on-chip PLL," and "on chip PLL/DLL."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 277:**

Admit that, between December 1991 and June 1996, various members of the JC 42.3 Subcommittee made presentations proposing to incorporate using a DLL to compensate for the output delay into the JEDEC SDRAM standards.

**RESPONSE TO REQUEST FOR ADMISSION NO. 277:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "using a DLL" "to compensate for the output delay," and "JEDEC SDRAM standards." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that certain presentations made by members of the JEDEC 42.3 Subcommittee between December 1991 and June 1996, designated as relating to "SDRAM," included terms such as, for example, "on chip PLL/DLL."

After having made reasonable inquiry, the information known to or readily obtainable by Rambus is insufficient for Rambus to further admit or deny the request.

**REQUEST FOR ADMISSION NO. 278:**

Admit that, between December 1991 and June 1996, Rambus knew that various members

of the JC 42.3 Subcommittee made presentations proposing to incorporate using a DLL to compensate for the output delay into the JEDEC SDRAM standards.

**RESPONSE TO REQUEST FOR ADMISSION NO. 278:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "presentations," "using a DLL" "to compensate for the output delay," and "JEDEC SDRAM standards." Rambus further objects to the request as compound. Rambus further objects on the ground that the request is vague and ambiguous as to what would constitute "knowledge" on the part of Rambus.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at certain times between December 1991 and June 1996 certain Rambus employees knew that certain presentations made by members of the JEDEC 42.3 Subcommittee, designated as relating to "SDRAM," included terms such as, for example, "on chip PLL/DLL."

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 279:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus had claims in pending patent applications that, if included in an issued patent, would be infringed by a non-compatible DRAM device containing a programmable register operative to store information specifying a manner in which the semiconductor device is to respond to a read request or a write request.

**RESPONSE TO REQUEST FOR ADMISSION NO. 279:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "believed," "programmable register," "operative to store information," "manner," "respond to a read request," "respond to a . . . write request," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus had any claims in pending patent applications that, if included in an issued patent, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 280:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus could amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would be infringed by a non-compatible DRAM device using a programmable register operative to store information specifying a manner in which the semiconductor device is to respond to a read request or a write request.

**RESPONSE TO REQUEST FOR ADMISSION NO. 280:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "could amend its pending patent applications, or file continuation or divisional applications, to add claims," and the terms "believed," "programmable register," "operative to store information," "manner," "respond to a read request," "respond to a . . . write request," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus could amend its pending patent applications or file continuation or divisional applications to add valid claims

that, if included in an issued patent application, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 281:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus had claims in pending patent applications that, if included in an issued patent, would cover the use of programmable CAS latency in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 281:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "believed," "programmable CAS latency," "cover" and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus had any claims in pending patent applications that, if included in an issued patent, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 282:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus could amend pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would cover the use of programmable CAS latency in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 282:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "could amend its pending patent applications, or file continuation or divisional applications, to add claims," and the terms "believed," "programmable CAS latency," "cover" and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus could amend its pending patent applications or file continuation or divisional applications to add valid claims that, if included in an issued patent application, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 283:**

Admit that, at one or more times between December 1991 and June 1996, Rambus

attempted to amend pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would cover the use of programmable CAS latency in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 283:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "attempted to amend pending patent applications, or file continuation or divisional applications, to add claims" and the terms "programmable CAS latency," "cover" and "non-compatible DRAM device." Rambus further objects to the request as compound. Rambus further objects that the request calls for a legal conclusion. Rambus further objects to this request on the grounds that Rambus is not familiar, and cannot through reasonable inquiry become familiar, with the operation of all non-compatible DRAM devices. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at one or more times between December 1991 and June 1996, Rambus amended its pending U.S. patent applications, filed continuation applications, and filed divisional applications. Rambus is not presently aware of any non-compatible devices that would infringe claims that were amended in or added to its U.S. Patent applications between December 1991 and June 1996 if such claims were included in an issued patent, with the exception of MDRAM devices designed by MoSys. By preliminary amendment dated September 6, 1994, Rambus properly added claims in its patent application with serial number 08/222,646 that were fully supported by the specification and that Rambus intended would read on MoSys MDRAM. *See, e.g., Kingsdown Medical Consultants, Ltd. v. Hollister, Inc.*, 863 F.2d 867, 874 (Fed. Cir. 1988), *cert. denied*, 490 U.S. 1067 (1989) ("nor is it in any manner improper

to amend or insert claims intended to cover a competitor's product the applicant's attorney has learned about during the prosecution of a patent application"). After the application issued as U.S. Patent No. 5,513,327 and the MoSys device was closely examined, Rambus informed MoSys of Rambus's belief that MoSys was infringing the patent. The parties settled their dispute and no infringement ruling was ultimately obtained.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 284:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus had claims in pending patent applications that, if included in an issued patent, would cover a non-compatible DRAM device containing a register to store a value to determine CAS latency, where that value can be changed by programming the mode register.

**RESPONSE TO REQUEST FOR ADMISSION NO. 284:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "believed," "to determine CAS latency," "programming," "mode register," "cover" and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 285:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus could amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would cover a non-compatible DRAM device containing a register to store a value to determine CAS latency, where that value can be changed by programming the mode register.

**RESPONSE TO REQUEST FOR ADMISSION NO. 285:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "could amend its pending patent applications, or file continuation or divisional applications, to add claims," and the terms "believed," "to determine CAS latency," "programming," "mode register," "cover" and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus could amend its pending patent applications or file continuation or divisional applications to add valid claims that, if included in an issued patent application, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 286:**

Admit that, at one or more times between December 1991 and June 1996, Rambus attempted to amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would cover a non-compatible DRAM device containing a register to store a value to determine CAS latency, where that value can be changed by programming the mode register.

**RESPONSE TO REQUEST FOR ADMISSION NO. 286:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "attempted to amend pending patent applications, or file continuation or divisional applications, to add claims" and the terms "to determine CAS latency,"

"programming," "mode register," "cover" and "non-compatible DRAM device." Rambus further objects to the request as compound. Rambus further objects that the request calls for a legal conclusion. Rambus further objects to this request on the grounds that Rambus is not familiar, and cannot through reasonable inquiry become familiar, with the operation of all non-compatible DRAM devices. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at one or more times between December 1991 and June 1996, Rambus amended its pending U.S. patent applications, filed continuation applications, and filed divisional applications. Rambus is not presently aware of any non-compatible devices that would infringe claims that were amended in or added to its U.S. Patent applications between December 1991 and June 1996 if such claims were included in an issued patent, with the exception of MDRAM devices designed by MoSys. By preliminary amendment dated September 6, 1994, Rambus properly added claims in its patent application with serial number 08/222,646 that were fully supported by the specification and that Rambus intended would read on MoSys MDRAM. *See, e.g., Kingsdown Medical Consultants, Ltd. v. Hollister, Inc.*, 863 F.2d 867, 874 (Fed. Cir. 1988), *cert. denied*, 490 U.S. 1067 (1989) ("nor is it in any manner improper to amend or insert claims intended to cover a competitor's product the applicant's attorney has learned about during the prosecution of a patent application"). After the application issued as U.S. Patent No. 5,513,327 and the MoSys device was closely examined, Rambus informed MoSys of Rambus's belief that MoSys was infringing the patent. The parties settled their dispute and no infringement ruling was ultimately obtained.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 287:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus had claims in pending patent applications that, if included in an issued patent, would cover the use of a programmable register to store a value that is representative of a delay time after which the device responds to a read request in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 287:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "believed," "programmable register," "representative of a delay time," "responds to a read request," "cover" and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus had any claims in pending patent applications that, if included in an issued patent, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 288:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus could amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would cover the use of a programmable register to store a value that is

representative of a delay time after which the device responds to a read request in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 288:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "could amend its pending patent applications, or file continuation or divisional applications, to add claims," and the terms "believed," "programmable register," "representative of a delay time," "responds to a read request," "cover" and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus could amend its pending patent applications or file continuation or divisional applications to add valid claims that, if included in an issued patent application, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 289:**

Admit that, at one or more times between December 1991 and June 1996, Rambus attempted to amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would cover the use of a programmable register to store a value that is representative of a delay time after which the device responds to a read request in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 289:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "attempted to amend pending patent applications, or file continuation or divisional applications, to add claims" and the terms "programmable register," "representative of a delay time," "responds to a read request," "cover" and "non-compatible DRAM device." Rambus further objects to the request as compound. Rambus further objects that the request calls for a legal conclusion. Rambus further objects to this request on the grounds that Rambus is not familiar, and cannot through reasonable inquiry become familiar, with the operation of all non-compatible DRAM devices. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at one or more times between December 1991 and June 1996, Rambus amended its pending U.S. patent applications, filed continuation applications, and filed divisional applications. Rambus is not presently aware of any non-compatible devices that would infringe claims that were amended in or added to its U.S. Patent applications between December 1991 and June 1996 if such claims were included in an issued patent, with the exception of MDRAM devices designed by MoSys. By preliminary amendment dated September 6, 1994, Rambus properly added claims in its patent application with serial number 08/222,646 that were fully supported by the specification and that Rambus intended would read on MoSys MDRAM. *See, e.g., Kingsdown Medical Consultants, Ltd. v. Hollister, Inc.*, 863 F.2d 867, 874 (Fed. Cir. 1988), *cert. denied*, 490 U.S. 1067 (1989) ("nor is it in any manner improper to amend or insert claims intended to cover a competitor's product the applicant's attorney has learned about during the prosecution of a patent application"). After the application issued as

U.S. Patent No. 5,513,327 and the MoSys device was closely examined, Rambus informed MoSys of Rambus's belief that MoSys was infringing the patent. The parties settled their dispute and no infringement ruling was ultimately obtained.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 290:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus had claims in pending patent applications that, if included in an issued patent, would be infringed by a non-compatible DRAM device using programmable CAS latency.

**RESPONSE TO REQUEST FOR ADMISSION NO. 290:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "believed," "programmable CAS latency," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus had any claims in pending patent applications that, if included in an issued patent, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 291:**

Admit that, at various times between December 1991 and June 1996, various directors,

officers or employees of Rambus believed that Rambus could amend pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would be infringed by a non-compatible DRAM device using programmable CAS latency.

**RESPONSE TO REQUEST FOR ADMISSION NO. 291:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "could amend its pending patent applications, or file continuation or divisional applications, to add claims," and the terms "believed," "programmable CAS latency," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus could amend its pending patent applications or file continuation or divisional applications to add valid claims that, if included in an issued patent application, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 292:**

Admit that, at one or more times between December 1991 and June 1996, Rambus attempted to amend pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would be infringed by a non-compatible DRAM device using programmable CAS latency.

**RESPONSE TO REQUEST FOR ADMISSION NO. 292:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "attempted to amend pending patent applications, or file continuation or divisional applications, to add claims" and the terms "programmable CAS latency," and "non-compatible DRAM device." Rambus further objects to the request as compound. Rambus further objects that the request calls for a legal conclusion. Rambus further objects to this request on the grounds that Rambus is not familiar, and cannot through reasonable inquiry become familiar, with the operation of all non-compatible DRAM devices. Rambus further objects that whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at one or more times between December 1991 and June 1996, Rambus amended its pending U.S. patent applications, filed continuation applications, and filed divisional applications. Rambus is not presently aware of any non-compatible devices that would infringe claims that were amended in or added to its U.S. Patent applications between December 1991 and June 1996 if such claims were included in an issued patent, with the exception of MDRAM devices designed by MoSys. By preliminary amendment dated September 6, 1994, Rambus properly added claims in its patent application with serial number 08/222,646 that were fully supported by the specification and that Rambus intended would read on MoSys MDRAM. *See, e.g.*, *Kingsdown Medical Consultants, Ltd. v. Hollister, Inc.*, 863 F.2d 867, 874 (Fed. Cir. 1988), *cert. denied*, 490 U.S. 1067 (1989) ("nor is it in any manner improper to amend or insert claims intended to cover a competitor's product the applicant's attorney has learned about during the prosecution of a patent application"). After the application issued as U.S. Patent No. 5,513,327 and the MoSys device was closely examined, Rambus informed MoSys of Rambus's belief that MoSys was infringing the patent. The parties settled their

dispute and no infringement ruling was ultimately obtained.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 293:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus had claims in pending patent applications that, if included in an issued patent, would be infringed by a non-compatible DRAM device containing a register to store a value to determine CAS latency, where that value can be changed by programming the mode register.

**RESPONSE TO REQUEST FOR ADMISSION NO. 293:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "believed," "to determine CAS latency," "programming," "mode register," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus had any claims in pending patent applications that, if included in an issued patent, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 294:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus could amend its pending patent

applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would be infringed by a non-compatible DRAM device containing a register to store a value to determine CAS latency,.

**RESPONSE TO REQUEST FOR ADMISSION NO. 294:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "could amend its pending patent applications, or file continuation or divisional applications, to add claims," and the terms "believed," "to determine CAS latency," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus could amend its pending patent applications or file continuation or divisional applications to add valid claims that, if included in an issued patent application, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 295:**

Admit that, at one or more times between December 1991 and June 1996, Rambus attempted to amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would be infringed by a non-compatible DRAM device containing a register to store a value to determine CAS latency, where that value can be changed by programming the mode register.

**RESPONSE TO REQUEST FOR ADMISSION NO. 295:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "attempted to amend pending patent applications, or file continuation or divisional applications, to add claims" and the terms "to determine CAS latency," "programming," "mode register," and "non-compatible DRAM device." Rambus further objects to the request as compound. Rambus further objects that the request calls for a legal conclusion. Rambus further objects to this request on the grounds that Rambus is not familiar, and cannot through reasonable inquiry become familiar, with the operation of all non-compatible DRAM devices. Rambus further objects that whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at one or more times between December 1991 and June 1996, Rambus amended its pending U.S. patent applications, filed continuation applications, and filed divisional applications. Rambus is not presently aware of any non-compatible devices that would infringe claims that were amended in or added to its U.S. Patent applications between December 1991 and June 1996 if such claims were included in an issued patent, with the exception of MDRAM devices designed by MoSys. By preliminary amendment dated September 6, 1994, Rambus properly added claims in its patent application with serial number 08/222,646 that were fully supported by the specification and that Rambus intended would read on MoSys MDRAM. *See, e.g., Kingsdown Medical Consultants, Ltd. v. Hollister, Inc.*, 863 F.2d 867, 874 (Fed. Cir. 1988), *cert. denied*, 490 U.S. 1067 (1989) ("nor is it in any manner improper to amend or insert claims intended to cover a competitor's product the applicant's attorney has learned about during the prosecution of a patent application"). After the application issued as U.S. Patent No. 5,513,327 and the MoSys device was closely examined, Rambus informed

MoSys of Rambus's belief that MoSys was infringing the patent. The parties settled their dispute and no infringement ruling was ultimately obtained.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 296:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus had claims in pending patent applications that, if included in an issued patent, would be infringed by a non-compatible DRAM device using a programmable register to store a value that is representative of a delay time after which the device responds to a read request.

**RESPONSE TO REQUEST FOR ADMISSION NO. 296:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "believed," "programmable register," "representative of a delay time," "responds to a read request," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus had any claims in pending patent applications that, if included in an issued patent, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request..

**REQUEST FOR ADMISSION NO. 297:**

Admit that, at various times between December 1991 and June 1996, various directors,

officers or employees of Rambus believed that Rambus could amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would be infringed by a non-compatible DRAM device using a programmable register to store a value that is representative of a delay time after which the device responds to a read request.

**RESPONSE TO REQUEST FOR ADMISSION NO. 297:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "could amend its pending patent applications, or file continuation or divisional applications, to add claims," and the terms "believed," "programmable register," "representative of a delay time," "responds to a read request," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus could amend its pending patent applications or file continuation or divisional applications to add valid claims that, if included in an issued patent application, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 298:**

Admit that, at one or more times between December 1991 and June 1996, Rambus attempted to amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would be infringed by a non-

compatible DRAM device using a programmable register to store a value that is representative of a delay time after which the device responds to a read request.

**RESPONSE TO REQUEST FOR ADMISSION NO. 298:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "attempted to amend pending patent applications, or file continuation or divisional applications, to add claims" and the terms "programmable register," "representative of a delay time," "responds to a read request," and "non-compatible DRAM device." Rambus further objects to the request as compound. Rambus further objects that the request calls for a legal conclusion. Rambus further objects to this request on the grounds that Rambus is not familiar, and cannot through reasonable inquiry become familiar, with the operation of all non-compatible DRAM devices. Rambus further objects that whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at one or more times between December 1991 and June 1996, Rambus amended its pending U.S. patent applications, filed continuation applications, and filed divisional applications. Rambus is not presently aware of any non-compatible devices that would infringe claims that were amended in or added to its U.S. Patent applications between December 1991 and June 1996 if such claims were included in an issued patent, with the exception of MDRAM devices designed by MoSys. By preliminary amendment dated September 6, 1994, Rambus properly added claims in its patent application with serial number 08/222,646 that were fully supported by the specification and that Rambus intended would read on MoSys MDRAM. *See, e.g., Kingsdown Medical Consultants, Ltd. v. Hollister, Inc.*, 863 F.2d 867, 874 (Fed. Cir. 1988), *cert. denied*, 490 U.S. 1067 (1989) ("nor is it in any manner improper to amend or insert claims intended to cover a competitor's product the applicant's attorney has

learned about during the prosecution of a patent application"). After the application issued as U.S. Patent No. 5,513,327 and the MoSys device was closely examined, Rambus informed MoSys of Rambus's belief that MoSys was infringing the patent. The parties settled their dispute and no infringement ruling was ultimately obtained.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 299:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus had claims in pending patent applications that, if included in an issued patent, would be infringed by a non-compatible DRAM device containing a programmable register to store a value which is representative of a delay time, that value being a number of clock cycles of an external clock, after which the SDRAM responds to a read request.

**RESPONSE TO REQUEST FOR ADMISSION NO. 299:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "believed," "programmable register," "representative of a delay time," "a number of clock cycles," "an external clock," "the SDRAM," "responds to a read request," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus had any claims in pending patent applications that, if included in an issued patent, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 300:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus could amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would be infringed by a non-compatible DRAM device using a programmable register to store a value which is representative of a delay time, that value being a number of clock cycles of an external clock, after which the SDRAM responds to a read request.

**RESPONSE TO REQUEST FOR ADMISSION NO. 300:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "could amend its pending patent applications, or file continuation or divisional applications, to add claims," and the terms "believed," "programmable register," "representative of a delay time," "a number of clock cycles," "an external clock," "the SDRAM," "responds to a read request," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus could amend its pending patent applications or file continuation or divisional applications to add valid claims that, if included in an issued patent application, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 301:**

Admit that, at one or more times between December 1991 and June 1996, Rambus attempted to amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would be infringed by a non-compatible DRAM device using a programmable register to store a value which is representative of a delay time, that value being a number of clock cycles of an external clock, after which the SDRAM responds to a read request.

**RESPONSE TO REQUEST FOR ADMISSION NO. 301:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "attempted to amend pending patent applications, or file continuation or divisional applications, to add claims" and the terms "programmable register," "representative of a delay time," "a number of clock cycles," "an external clock," "the SDRAM," "responds to a read request," and "non-compatible DRAM device." Rambus further objects to the request as compound. Rambus further objects that the request calls for a legal conclusion. Rambus further objects to this request on the grounds that Rambus is not familiar, and cannot through reasonable inquiry become familiar, with the operation of all non-compatible DRAM devices. Rambus further objects that whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at one or more times between December 1991 and June 1996, Rambus amended its pending U.S. patent applications, filed continuation applications, and filed divisional applications. Rambus is not presently aware of any non-compatible devices that would infringe claims that were amended in or added to its U.S. Patent applications between December 1991 and June 1996 if such claims were included in an issued patent, with the exception of MDRAM devices designed by MoSys. By preliminary amendment dated

September 6, 1994, Rambus properly added claims in its patent application with serial number 08/222,646 that were fully supported by the specification and that Rambus intended would read on MoSys MDRAM. *See*, *e.g.*, *Kingsdown Medical Consultants, Ltd. v. Hollister, Inc.*, 863 F.2d 867, 874 (Fed. Cir. 1988), *cert. denied*, 490 U.S. 1067 (1989) ("nor is it in any manner improper to amend or insert claims intended to cover a competitor's product the applicant's attorney has learned about during the prosecution of a patent application"). After the application issued as U.S. Patent No. 5,513,327 and the MoSys device was closely examined, Rambus informed MoSys of Rambus's belief that MoSys was infringing the patent. The parties settled their dispute and no infringement ruling was ultimately obtained.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 302:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus had claims in pending patent applications that, if included in an issued patent, would be infringed by a non-compatible DRAM device containing a programmable access-time register operative to store information specifying a value indicative of an access time for the device, such that the device waits for the access time before responding to a read request.

**RESPONSE TO REQUEST FOR ADMISSION NO. 302:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "believed," "programmable access-time register," "indicative of an access time," "waits for the access time," "responding to a read request," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus had any claims in pending patent applications that, if included in an issued patent, would be infringed by non-

compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 303:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus could amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would be infringed by a non-compatible DRAM device using a programmable access-time register operative to store information specifying a value indicative of an access time for the device, such that the device waits for the access time before responding to a read request.

**RESPONSE TO REQUEST FOR ADMISSION NO. 303:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "could amend its pending patent applications, or file continuation or divisional applications, to add claims," and the terms "believed," "programmable access-time register," "indicative of an access time," "waits for the access time," "responding to a read request," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus could amend its pending patent applications or file continuation or divisional applications to add valid claims that, if included in an issued patent application, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered

belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 304:**

Admit that, at one or more times between December 1991 and June 1996, Rambus attempted to amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would be infringed by a non-compatible DRAM device using a programmable access-time register operative to store information specifying a value indicative of an access time for the device, such that the device waits for the access time before responding to a read request.

**RESPONSE TO REQUEST FOR ADMISSION NO. 304:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "attempted to amend pending patent applications, or file continuation or divisional applications, to add claims" and the terms "programmable access-time register," "indicative of an access time," "waits for the access time," "responding to a read request," and "non-compatible DRAM device." Rambus further objects to the request as compound. Rambus further objects that the request calls for a legal conclusion. Rambus further objects to this request on the grounds that Rambus is not familiar, and cannot through reasonable inquiry become familiar, with the operation of all non-compatible DRAM devices. Rambus further objects that whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at one or more times between December 1991 and June 1996,

Rambus amended its pending U.S. patent applications, filed continuation applications, and filed divisional applications. Rambus is not presently aware of any non-compatible devices that would infringe claims that were amended in or added to its U.S. Patent applications between December 1991 and June 1996 if such claims were included in an issued patent, with the exception of MDRAM devices designed by MoSys. By preliminary amendment dated September 6, 1994, Rambus properly added claims in its patent application with serial number 08/222,646 that were fully supported by the specification and that Rambus intended would read on MoSys MDRAM. *See, e.g.*, *Kingsdown Medical Consultants, Ltd. v. Hollister, Inc.*, 863 F.2d 867, 874 (Fed. Cir. 1988), *cert. denied*, 490 U.S. 1067 (1989) ("nor is it in any manner improper to amend or insert claims intended to cover a competitor's product the applicant's attorney has learned about during the prosecution of a patent application"). After the application issued as U.S. Patent No. 5,513,327 and the MoSys device was closely examined, Rambus informed MoSys of Rambus's belief that MoSys was infringing the patent. The parties settled their dispute and no infringement ruling was ultimately obtained.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 305:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus had claims in pending patent applications that, if included in an issued patent, would cover the use of programmable burst length in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 305:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "believed," "programmable burst length," "cover," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned

and considered belief, between December 1991 and June 1996, that Rambus had any claims in pending patent applications that, if included in an issued patent, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 306:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus could amend pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would cover the use of programmable burst length in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 306:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "could amend its pending patent applications, or file continuation or divisional applications, to add claims," and the terms "believed," "programmable burst length," "cover," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus could amend its pending patent applications or file continuation or divisional applications to add valid claims that, if included in an issued patent application, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered

belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 307:**

Admit that, at one or more times between December 1991 and June 1996, Rambus attempted to amend pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would cover the use of programmable burst length in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 307:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "attempted to amend pending patent applications, or file continuation or divisional applications, to add claims" and the terms "programmable burst length," "cover," and "non-compatible DRAM device." Rambus further objects to the request as compound. Rambus further objects that the request calls for a legal conclusion. Rambus further objects to this request on the grounds that Rambus is not familiar, and cannot through reasonable inquiry become familiar, with the operation of all non-compatible DRAM devices. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at one or more times between December 1991 and June 1996, Rambus amended its pending U.S. patent applications, filed continuation applications, and filed divisional applications. Rambus is not presently aware of any non-compatible devices that

would infringe claims that were amended in or added to its U.S. Patent applications between December 1991 and June 1996 if such claims were included in an issued patent, with the exception of MDRAM devices designed by MoSys. By preliminary amendment dated September 6, 1994, Rambus properly added claims in its patent application with serial number 08/222,646 that were fully supported by the specification and that Rambus intended would read on MoSys MDRAM. *See, e.g.*, *Kingsdown Medical Consultants, Ltd. v. Hollister, Inc.*, 863 F.2d 867, 874 (Fed. Cir. 1988), *cert. denied*, 490 U.S. 1067 (1989) ("nor is it in any manner improper to amend or insert claims intended to cover a competitor's product the applicant's attorney has learned about during the prosecution of a patent application"). After the application issued as U.S. Patent No. 5,513,327 and the MoSys device was closely examined, Rambus informed MoSys of Rambus's belief that MoSys was infringing the patent. The parties settled their dispute and no infringement ruling was ultimately obtained.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 308:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus had claims in pending patent applications that, if included in an issued patent, would cover a non-compatible DRAM device containing a register to store a value to determine burst length, where that value can be changed by programming the mode register where that value can be changed by programming the mode register.

**RESPONSE TO REQUEST FOR ADMISSION NO. 308:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "believed," "to determine burst length," programming," "mode register," "cover," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned

and considered belief, between December 1991 and June 1996, that Rambus had any claims in pending patent applications that, if included in an issued patent, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 309:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus could amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would cover a non-compatible DRAM device containing a register to store a value to determine burst length, where that value can be changed by programming the mode register.

**RESPONSE TO REQUEST FOR ADMISSION NO. 309:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "could amend its pending patent applications, or file continuation or divisional applications, to add claims," and the terms "believed," "to determine burst length," programming," "mode register," "cover," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus could amend its pending patent applications or file continuation or divisional applications to add valid claims that, if included in an issued patent application, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered

belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 310:**

Admit that, at one or more times between December 1991 and June 1996, Rambus attempted to amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would cover a non-compatible DRAM device containing a register to store a value to determine burst length, where that value can be changed by programming the mode register.

**RESPONSE TO REQUEST FOR ADMISSION NO. 310:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "attempted to amend pending patent applications, or file continuation or divisional applications, to add claims" and the terms "to determine burst length," programming," "mode register," "cover," and "non-compatible DRAM device." Rambus further objects to the request as compound. Rambus further objects that the request calls for a legal conclusion. Rambus further objects to this request on the grounds that Rambus is not familiar, and cannot through reasonable inquiry become familiar, with the operation of all non-compatible DRAM devices. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at one or more times between December 1991 and June 1996, Rambus amended its pending U.S. patent applications, filed continuation applications, and filed

divisional applications. Rambus is not presently aware of any non-compatible devices that would infringe claims that were amended in or added to its U.S. Patent applications between December 1991 and June 1996 if such claims were included in an issued patent, with the exception of MDRAM devices designed by MoSys. By preliminary amendment dated September 6, 1994, Rambus properly added claims in its patent application with serial number 08/222,646 that were fully supported by the specification and that Rambus intended would read on MoSys MDRAM. *See, e.g.*, *Kingsdown Medical Consultants, Ltd. v. Hollister, Inc.*, 863 F.2d 867, 874 (Fed. Cir. 1988), *cert. denied*, 490 U.S. 1067 (1989) ("nor is it in any manner improper to amend or insert claims intended to cover a competitor's product the applicant's attorney has learned about during the prosecution of a patent application"). After the application issued as U.S. Patent No. 5,513,327 and the MoSys device was closely examined, Rambus informed MoSys of Rambus's belief that MoSys was infringing the patent. The parties settled their dispute and no infringement ruling was ultimately obtained.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 311:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus had claims in pending patent applications that, if included in an issued patent, would cover a non-compatible DRAM device containing a register to store a value to determine block size, where that value can be changed by programming the mode register.

**RESPONSE TO REQUEST FOR ADMISSION NO. 311:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "believed," "to determine block size," programming," "mode register," "cover," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned

and considered belief, between December 1991 and June 1996, that Rambus had any claims in pending patent applications that, if included in an issued patent, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 312:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus could amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would cover a non-compatible DRAM device containing a register to store a value to determine block size, where that value can be changed by programming the mode register.

**RESPONSE TO REQUEST FOR ADMISSION NO. 312:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "could amend its pending patent applications, or file continuation or divisional applications, to add claims," and the terms "believed," "to determine block size," programming," "mode register," "cover," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus could amend its pending patent applications or file continuation or divisional applications to add valid claims that, if included in an issued patent application, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered

belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 313:**

Admit that, at one or more times between December 1991 and June 1996, Rambus attempted to amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would cover a non-compatible DRAM device containing a register to store a value to determine block size, where that value can be changed by programming the mode register.

**RESPONSE TO REQUEST FOR ADMISSION NO. 313:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "attempted to amend pending patent applications, or file continuation or divisional applications, to add claims" and the terms "to determine block size," programming," "mode register," "cover," and "non-compatible DRAM device." Rambus further objects to the request as compound. Rambus further objects that the request calls for a legal conclusion. Rambus further objects to this request on the grounds that Rambus is not familiar, and cannot through reasonable inquiry become familiar, with the operation of all non-compatible DRAM devices. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at one or more times between December 1991 and June 1996, Rambus amended its pending U.S. patent applications, filed continuation applications, and filed

divisional applications. Rambus is not presently aware of any non-compatible devices that would infringe claims that were amended in or added to its U.S. Patent applications between December 1991 and June 1996 if such claims were included in an issued patent, with the exception of MDRAM devices designed by MoSys. By preliminary amendment dated September 6, 1994, Rambus properly added claims in its patent application with serial number 08/222,646 that were fully supported by the specification and that Rambus intended would read on MoSys MDRAM. *See, e.g.*, *Kingsdown Medical Consultants, Ltd. v. Hollister, Inc.*, 863 F.2d 867, 874 (Fed. Cir. 1988), *cert. denied*, 490 U.S. 1067 (1989) ("nor is it in any manner improper to amend or insert claims intended to cover a competitor's product the applicant's attorney has learned about during the prosecution of a patent application"). After the application issued as U.S. Patent No. 5,513,327 and the MoSys device was closely examined, Rambus informed MoSys of Rambus's belief that MoSys was infringing the patent. The parties settled their dispute and no infringement ruling was ultimately obtained.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 314:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus had claims in pending patent applications that, if included in an issued patent, would cover the use in a non-compatible DRAM device of a programmable register that receives information that defines an amount of data to be output by the memory device in response to a read request.

**RESPONSE TO REQUEST FOR ADMISSION NO. 314:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "believed," "programmable register," "receives information," "defines an amount of data," "in response to a read request," "cover," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus had any claims in pending patent applications that, if included in an issued patent, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 315:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus could amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would cover the use in a non-compatible DRAM device of a programmable register that receives information that defines an amount of data to be output by the memory device in response to a read request.

**RESPONSE TO REQUEST FOR ADMISSION NO. 315:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "could amend its pending patent applications, or file continuation or divisional applications, to add claims," and the terms "believed," "programmable register," "receives information," "defines an amount of data," "in response to a read request," "cover," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus could amend its pending patent applications or file continuation or divisional applications to add valid claims

that, if included in an issued patent application, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 316:**

Admit that, at one or more times between December 1991 and June 1996, Rambus attempted to amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would cover the use in a non-compatible DRAM device of a programmable register that receives information that defines an amount of data to be output by the memory device in response to a read request.

**RESPONSE TO REQUEST FOR ADMISSION NO. 316:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "attempted to amend pending patent applications, or file continuation or divisional applications, to add claims" and the terms "programmable register," "receives information," "defines an amount of data," "in response to a read request," "cover," and "non-compatible DRAM device." Rambus further objects to the request as compound. Rambus further objects that the request calls for a legal conclusion. Rambus further objects to this request on the grounds that Rambus is not familiar, and cannot through reasonable inquiry become familiar, with the operation of all non-compatible DRAM devices. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be

determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at one or more times between December 1991 and June 1996, Rambus amended its pending U.S. patent applications, filed continuation applications, and filed divisional applications. Rambus is not presently aware of any non-compatible devices that would infringe claims that were amended in or added to its U.S. Patent applications between December 1991 and June 1996 if such claims were included in an issued patent, with the exception of MDRAM devices designed by MoSys. By preliminary amendment dated September 6, 1994, Rambus properly added claims in its patent application with serial number 08/222,646 that were fully supported by the specification and that Rambus intended would read on MoSys MDRAM. *See, e.g., Kingsdown Medical Consultants, Ltd. v. Hollister, Inc.*, 863 F.2d 867, 874 (Fed. Cir. 1988), *cert. denied*, 490 U.S. 1067 (1989) ("nor is it in any manner improper to amend or insert claims intended to cover a competitor's product the applicant's attorney has learned about during the prosecution of a patent application"). After the application issued as U.S. Patent No. 5,513,327 and the MoSys device was closely examined, Rambus informed MoSys of Rambus's belief that MoSys was infringing the patent. The parties settled their dispute and no infringement ruling was ultimately obtained.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 317:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus had claims in pending patent applications that, if included in an issued patent, would be infringed by a non-compatible DRAM device using programmable burst length.

**RESPONSE TO REQUEST FOR ADMISSION NO. 317:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "believed," "programmable burst length" and "non-compatible DRAM

device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus had any claims in pending patent applications that, if included in an issued patent, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 318:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus could amend pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would be infringed by a non-compatible DRAM device using programmable burst length.

**RESPONSE TO REQUEST FOR ADMISSION NO. 318:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "could amend its pending patent applications, or file continuation or divisional applications, to add claims," and the terms "believed," "programmable burst length" and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus could amend its pending patent applications or file continuation or divisional applications to add valid claims

that, if included in an issued patent application, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 319:**

Admit that, at one or more times between December 1991 and June 1996, Rambus attempted to amend pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would be infringed by a non-compatible DRAM device using programmable burst length.

**RESPONSE TO REQUEST FOR ADMISSION NO. 319:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "attempted to amend pending patent applications, or file continuation or divisional applications, to add claims" and the terms "programmable burst length" and "non-compatible DRAM device." Rambus further objects to the request as compound. Rambus further objects that the request calls for a legal conclusion. Rambus further objects to this request on the grounds that Rambus is not familiar, and cannot through reasonable inquiry become familiar, with the operation of all non-compatible DRAM devices. Rambus further objects that whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at one or more times between December 1991 and June 1996,

Rambus amended its pending U.S. patent applications, filed continuation applications, and filed divisional applications. Rambus is not presently aware of any non-compatible devices that would infringe claims that were amended in or added to its U.S. Patent applications between December 1991 and June 1996 if such claims were included in an issued patent, with the exception of MDRAM devices designed by MoSys. By preliminary amendment dated September 6, 1994, Rambus properly added claims in its patent application with serial number 08/222,646 that were fully supported by the specification and that Rambus intended would read on MoSys MDRAM. *See, e.g.*, *Kingsdown Medical Consultants, Ltd. v. Hollister, Inc.*, 863 F.2d 867, 874 (Fed. Cir. 1988), *cert. denied*, 490 U.S. 1067 (1989) ("nor is it in any manner improper to amend or insert claims intended to cover a competitor's product the applicant's attorney has learned about during the prosecution of a patent application"). After the application issued as U.S. Patent No. 5,513,327 and the MoSys device was closely examined, Rambus informed MoSys of Rambus's belief that MoSys was infringing the patent. The parties settled their dispute and no infringement ruling was ultimately obtained.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 320:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus had claims in pending patent applications that, if included in an issued patent, would be infringed by a non-compatible DRAM device using programmable block size.

**RESPONSE TO REQUEST FOR ADMISSION NO. 320:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "believed," "programmable block size" and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned

and considered belief, between December 1991 and June 1996, that Rambus had any claims in pending patent applications that, if included in an issued patent, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 321:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus could amend pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would be infringed by a non-compatible DRAM device using programmable block size.

**RESPONSE TO REQUEST FOR ADMISSION NO. 321:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "could amend its pending patent applications, or file continuation or divisional applications, to add claims," and the terms "believed," "programmable block size" and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus could amend its pending patent applications or file continuation or divisional applications to add valid claims that, if included in an issued patent application, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered

belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 322:**

Admit that, at one or more times between December 1991 and June 1996, Rambus attempted to amend pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would be infringed by a non-compatible DRAM device using programmable block size.

**RESPONSE TO REQUEST FOR ADMISSION NO. 322:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "attempted to amend pending patent applications, or file continuation or divisional applications, to add claims" and the terms "programmable block size" and "non-compatible DRAM device." Rambus further objects to the request as compound. Rambus further objects that the request calls for a legal conclusion. Rambus further objects to this request on the grounds that Rambus is not familiar, and cannot through reasonable inquiry become familiar, with the operation of all non-compatible DRAM devices. Rambus further objects that whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at one or more times between December 1991 and June 1996, Rambus amended its pending U.S. patent applications, filed continuation applications, and filed divisional applications. Rambus is not presently aware of any non-compatible devices that would infringe claims that were amended in or added to its U.S. Patent applications between

December 1991 and June 1996 if such claims were included in an issued patent, with the exception of MDRAM devices designed by MoSys. By preliminary amendment dated September 6, 1994, Rambus properly added claims in its patent application with serial number 08/222,646 that were fully supported by the specification and that Rambus intended would read on MoSys MDRAM. *See, e.g., Kingsdown Medical Consultants, Ltd. v. Hollister, Inc.*, 863 F.2d 867, 874 (Fed. Cir. 1988), *cert. denied*, 490 U.S. 1067 (1989) ("nor is it in any manner improper to amend or insert claims intended to cover a competitor's product the applicant's attorney has learned about during the prosecution of a patent application"). After the application issued as U.S. Patent No. 5,513,327 and the MoSys device was closely examined, Rambus informed MoSys of Rambus's belief that MoSys was infringing the patent. The parties settled their dispute and no infringement ruling was ultimately obtained.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 323:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus had claims in pending patent applications that, if included in an issued patent, would be infringed by a non-compatible DRAM device containing a register to store a value that defines an amount of data to be output by the memory device in response to a read request, where that value can be changed by programming the mode register.

**RESPONSE TO REQUEST FOR ADMISSION NO. 323:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "believed," "defines an amount of data," "in response to a read request," "programming," "mode register," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus had any claims in

pending patent applications that, if included in an issued patent, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 324:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus could amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would be infringed by a non-compatible DRAM device containing a register to store a value that defines an amount of data to be output by the memory device in response to a read request, where that value can be changed by programming the mode register.

**RESPONSE TO REQUEST FOR ADMISSION NO. 324:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "could amend its pending patent applications, or file continuation or divisional applications, to add claims," and the terms "believed," "defines an amount of data," "in response to a read request," "programming," "mode register," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus could amend its pending patent applications or file continuation or divisional applications to add valid claims that, if included in an issued patent application, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys.

Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 325:**

Admit that, at one or more times between December 1991 and June 1996, Rambus attempted to amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would be infringed by a non-compatible DRAM device containing a register to store a value that defines an amount of data to be output by the memory device in response to a read request, where that value can be changed by programming the mode register.

**RESPONSE TO REQUEST FOR ADMISSION NO. 325:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "attempted to amend pending patent applications, or file continuation or divisional applications, to add claims" and the terms "defines an amount of data," "in response to a read request," "programming," "mode register," and "non-compatible DRAM device." Rambus further objects to the request as compound. Rambus further objects that the request calls for a legal conclusion. Rambus further objects to this request on the grounds that Rambus is not familiar, and cannot through reasonable inquiry become familiar, with the operation of all non-compatible DRAM devices. Rambus further objects that whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at one or more times between December 1991 and June 1996, Rambus amended its pending U.S. patent applications, filed continuation applications, and filed divisional applications. Rambus is not presently aware of any non-compatible devices that would infringe claims that were amended in or added to its U.S. Patent applications between December 1991 and June 1996 if such claims were included in an issued patent, with the exception of MDRAM devices designed by MoSys. By preliminary amendment dated September 6, 1994, Rambus properly added claims in its patent application with serial number 08/222,646 that were fully supported by the specification and that Rambus intended would read on MoSys MDRAM. *See, e.g.*, *Kingsdown Medical Consultants, Ltd. v. Hollister, Inc.*, 863 F.2d 867, 874 (Fed. Cir. 1988), *cert. denied*, 490 U.S. 1067 (1989) ("nor is it in any manner improper to amend or insert claims intended to cover a competitor's product the applicant's attorney has learned about during the prosecution of a patent application"). After the application issued as U.S. Patent No. 5,513,327 and the MoSys device was closely examined, Rambus informed MoSys of Rambus's belief that MoSys was infringing the patent. The parties settled their dispute and no infringement ruling was ultimately obtained.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 326:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus had claims in pending patent applications that, if included in an issued patent, would be infringed by a non-compatible DRAM device containing a programmable register that receives information that defines an amount of data to be input by the memory device in response to a write request.

**RESPONSE TO REQUEST FOR ADMISSION NO. 326:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "believed," "programmable register," "receives information," "defines an amount of data," "in response to a write request," "would cover by," and "non-compatible

DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus had any claims in pending patent applications that, if included in an issued patent, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 327:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus could amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would cover by a non-compatible DRAM device containing a programmable register that receives information that defines an amount of data to be input by the memory device in response to a write request.

**RESPONSE TO REQUEST FOR ADMISSION NO. 327:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "could amend its pending patent applications, or file continuation or divisional applications, to add claims," and the terms "believed," "programmable register," "receives information," "defines an amount of data," "in response to a write request," "would cover by," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned

and considered belief, between December 1991 and June 1996, that Rambus could amend its pending patent applications or file continuation or divisional applications to add valid claims that, if included in an issued patent application, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 328:**

Admit that, at one or more times between December 1991 and June 1996, Rambus attempted to amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would cover by a non-compatible DRAM device containing a programmable register that receives information that defines an amount of data to be input by the memory device in response to a write request.

**RESPONSE TO REQUEST FOR ADMISSION NO. 328:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "attempted to amend pending patent applications, or file continuation or divisional applications, to add claims" and the terms "programmable register," "receives information," "defines an amount of data," "in response to a write request," "would cover by," and "non-compatible DRAM device." Rambus further objects to the request as compound. Rambus further objects that the request calls for a legal conclusion. Rambus further objects to this request on the grounds that Rambus is not familiar, and cannot through reasonable inquiry become familiar, with the operation of all non-compatible DRAM devices. Rambus further objects that, to the extent that "cover by" is to be interpreted as "be infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the

DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at one or more times between December 1991 and June 1996, Rambus amended its pending U.S. patent applications, filed continuation applications, and filed divisional applications. Rambus is not presently aware of any non-compatible devices that would infringe claims that were amended in or added to its U.S. Patent applications between December 1991 and June 1996 if such claims were included in an issued patent, with the exception of MDRAM devices designed by MoSys. By preliminary amendment dated September 6, 1994, Rambus properly added claims in its patent application with serial number 08/222,646 that were fully supported by the specification and that Rambus intended would read on MoSys MDRAM. *See, e.g.*, *Kingsdown Medical Consultants, Ltd. v. Hollister, Inc.*, 863 F.2d 867, 874 (Fed. Cir. 1988), *cert. denied*, 490 U.S. 1067 (1989) ("nor is it in any manner improper to amend or insert claims intended to cover a competitor's product the applicant's attorney has learned about during the prosecution of a patent application"). After the application issued as U.S. Patent No. 5,513,327 and the MoSys device was closely examined, Rambus informed MoSys of Rambus's belief that MoSys was infringing the patent. The parties settled their dispute and no infringement ruling was ultimately obtained.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 329:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus had claims in pending patent applications that, if included in an issued patent, would cover by a non-compatible DRAM device containing a programmable register to store a value that defines an amount of data to be input by the memory device in response to a write request.

**RESPONSE TO REQUEST FOR ADMISSION NO. 329:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "believed," "defines an amount of data," "in response to a write request," "programmable register," "would cover by," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus had any claims in pending patent applications that, if included in an issued patent, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 330:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus could amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would cover by a non-compatible DRAM device containing a programmable register to store a value that defines an amount of data to be input by the memory device in response to a write request.

**RESPONSE TO REQUEST FOR ADMISSION NO. 330:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "could amend its pending patent applications, or file continuation or divisional applications, to add claims," and the terms "believed," "defines an amount of data," "in response to a write request," "programmable register," "would cover by," and "non-

compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus could amend its pending patent applications or file continuation or divisional applications to add valid claims that, if included in an issued patent application, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 331:**

Admit that, at one or more times between December 1991 and June 1996, Rambus attempted to amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would cover by a non-compatible DRAM device containing a programmable register to store a value that defines an amount of data to be input by the memory device in response to a write request.

**RESPONSE TO REQUEST FOR ADMISSION NO. 331:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "attempted to amend pending patent applications, or file continuation or divisional applications, to add claims" and the terms "programmable register," "defines an amount of data," "in response to a write request," "would cover by," and "non-compatible DRAM device." Rambus further objects to the request as compound. Rambus further objects that the request calls for a legal conclusion. Rambus further objects to this request on the grounds that Rambus is not familiar, and cannot through reasonable inquiry become familiar,

with the operation of all non-compatible DRAM devices. Rambus further objects that, to the extent that "cover by" is to be interpreted as "be infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at one or more times between December 1991 and June 1996, Rambus amended its pending U.S. patent applications, filed continuation applications, and filed divisional applications. Rambus is not presently aware of any non-compatible devices that would infringe claims that were amended in or added to its U.S. Patent applications between December 1991 and June 1996 if such claims were included in an issued patent, with the exception of MDRAM devices designed by MoSys. By preliminary amendment dated September 6, 1994, Rambus properly added claims in its patent application with serial number 08/222,646 that were fully supported by the specification and that Rambus intended would read on MoSys MDRAM. *See, e.g., Kingsdown Medical Consultants, Ltd. v. Hollister, Inc.*, 863 F.2d 867, 874 (Fed. Cir. 1988), *cert. denied*, 490 U.S. 1067 (1989) ("nor is it in any manner improper to amend or insert claims intended to cover a competitor's product the applicant's attorney has learned about during the prosecution of a patent application"). After the application issued as U.S. Patent No. 5,513,327 and the MoSys device was closely examined, Rambus informed MoSys of Rambus's belief that MoSys was infringing the patent. The parties settled their dispute and no infringement ruling was ultimately obtained.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 332:**

Admit that between December 1991 and June 1996, Rambus, through any one of its directors, officers or employees, believed that it had claims in pending patent applications or

issued patents that would cover a synchronous DRAM device that output data on the rising and the falling edge of a clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 332:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "through any one of its directors, officers or employees," "believed," "the rising and the falling edge," "a clock signal," "cover," and "synchronous DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus had any claims in pending patent applications that, if included in an issued patent, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 333:**

Admit that between December 1991 and June 1996, Rambus, through any one of its directors, officers or employees, believed that it had claims in pending patent applications or issued patents that would cover a synchronous DRAM device that input data on the rising and the falling edge of a clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 333:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "through any one of its directors, officers or employees," "believed," "the rising and the falling edge," "a clock signal," "cover," and "synchronous DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus had any claims in pending patent applications that, if included in an issued patent, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 334:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus had claims in pending patent applications that, if included in an issued patent, would cover the output a first portion of data in response to a rising edge of a clock signal and a second portion of data in response to a falling edge of a clock signal in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 334:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "believed," "first portion of data," "second portion of data," "in response to," "a clock signal," "cover," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus had any claims in pending patent applications that, if included in an issued patent, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the

Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 335:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus could amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would cover the output a first portion of data in response to a rising edge of a clock signal and a second portion of data in response to a falling edge of a clock signal in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 335:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "could amend its pending patent applications, or file continuation or divisional applications, to add claims," and the terms "believed," "first portion of data," "second portion of data," "in response to," "a clock signal," "cover," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus could amend its pending patent applications or file continuation or divisional applications to add valid claims that, if included in an issued patent application, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 336:**

Admit that, at one or more times between December 1991 and June 1996, Rambus attempted to amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would cover the output a first portion of data in response to a rising edge of a clock signal and a second portion of data in response to a falling edge of a clock signal in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 336:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "attempted to amend pending patent applications, or file continuation or divisional applications, to add claims" and the terms "first portion of data," "second portion of data," "in response to," "a clock signal," "cover," and "non-compatible DRAM device." Rambus further objects to the request as compound. Rambus further objects that the request calls for a legal conclusion. Rambus further objects to this request on the grounds that Rambus is not familiar, and cannot through reasonable inquiry become familiar, with the operation of all non-compatible DRAM devices. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at one or more times between December 1991 and June 1996, Rambus amended its pending U.S. patent applications, filed continuation applications, and filed divisional applications. Rambus is not presently aware of any non-compatible devices that would infringe claims that were amended in or added to its U.S. Patent applications between

December 1991 and June 1996 if such claims were included in an issued patent, with the exception of MDRAM devices designed by MoSys. By preliminary amendment dated September 6, 1994, Rambus properly added claims in its patent application with serial number 08/222,646 that were fully supported by the specification and that Rambus intended would read on MoSys MDRAM. *See, e.g., Kingsdown Medical Consultants, Ltd. v. Hollister, Inc.*, 863 F.2d 867, 874 (Fed. Cir. 1988), *cert. denied*, 490 U.S. 1067 (1989) ("nor is it in any manner improper to amend or insert claims intended to cover a competitor's product the applicant's attorney has learned about during the prosecution of a patent application"). After the application issued as U.S. Patent No. 5,513,327 and the MoSys device was closely examined, Rambus informed MoSys of Rambus's belief that MoSys was infringing the patent. The parties settled their dispute and no infringement ruling was ultimately obtained.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 337:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus had claims in pending patent applications that, if included in an issued patent, would cover the input of a first portion of data in response to a rising edge of a clock signal and a second portion of data in response to a falling edge of a clock signal in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 337:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "believed," "first portion of data," "second portion of data," "in response to," "a clock signal," "cover," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus had any claims in pending patent applications that, if included in an issued patent, would be infringed by non-

compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 338:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus could amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would cover the input of a first portion of data in response to a rising edge of a clock signal and a second portion of data in response to a falling edge of a clock signal in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 338:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "could amend its pending patent applications, or file continuation or divisional applications, to add claims," and the terms "believed," "first portion of data," "second portion of data," "in response to," "a clock signal," "cover," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus could amend its pending patent applications or file continuation or divisional applications to add valid claims that, if included in an issued patent application, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered

belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 339:**

Admit that, at one or more times between December 1991 and June 1996, Rambus attempted to amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would cover the input of a first portion of data in response to a rising edge of a clock signal and a second portion of data in response to a falling edge of a clock signal in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 339:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "attempted to amend pending patent applications, or file continuation or divisional applications, to add claims" and the terms "first portion of data," "second portion of data," "in response to," "a clock signal," "cover," and "non-compatible DRAM device." Rambus further objects to the request as compound. Rambus further objects that the request calls for a legal conclusion. Rambus further objects to this request on the grounds that Rambus is not familiar, and cannot through reasonable inquiry become familiar, with the operation of all non-compatible DRAM devices. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at one or more times between December 1991 and June 1996,

Rambus amended its pending U.S. patent applications, filed continuation applications, and filed divisional applications. Rambus is not presently aware of any non-compatible devices that would infringe claims that were amended in or added to its U.S. Patent applications between December 1991 and June 1996 if such claims were included in an issued patent, with the exception of MDRAM devices designed by MoSys. By preliminary amendment dated September 6, 1994, Rambus properly added claims in its patent application with serial number 08/222,646 that were fully supported by the specification and that Rambus intended would read on MoSys MDRAM. *See, e.g.*, *Kingsdown Medical Consultants, Ltd. v. Hollister, Inc.*, 863 F.2d 867, 874 (Fed. Cir. 1988), *cert. denied*, 490 U.S. 1067 (1989) ("nor is it in any manner improper to amend or insert claims intended to cover a competitor's product the applicant's attorney has learned about during the prosecution of a patent application"). After the application issued as U.S. Patent No. 5,513,327 and the MoSys device was closely examined, Rambus informed MoSys of Rambus's belief that MoSys was infringing the patent. The parties settled their dispute and no infringement ruling was ultimately obtained.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 340:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus had claims in pending patent applications that, if included in an issued patent, would cover the output of a first portion of data synchronously with respect to a rising edge of an external clock signal and a second portion of data synchronously with respect to a falling edge of the external clock signal in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 340:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "believed," "first portion of data," "second portion of data," "synchronously," "external clock signal," "cover," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus had any claims in pending patent applications that, if included in an issued patent, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 341:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus could amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would cover the output of a first portion of data synchronously with respect to a rising edge of an external clock signal and a second portion of data synchronously with respect to a falling edge of the external clock signal in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 341:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "could amend its pending patent applications, or file continuation or divisional applications, to add claims," and the terms "believed," "first portion of data," "second portion of data," "synchronously," "external clock signal," "cover," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus could amend its

pending patent applications or file continuation or divisional applications to add valid claims that, if included in an issued patent application, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 342:**

Admit that, at one or more times between December 1991 and June 1996, Rambus attempted to amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would cover the output of a first portion of data synchronously with respect to a rising edge of an external clock signal and a second portion of data synchronously with respect to a falling edge of the external clock signal in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 342:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "attempted to amend pending patent applications, or file continuation or divisional applications, to add claims" and the terms "first portion of data," "second portion of data," "synchronously," "external clock signal," "cover," and "non-compatible DRAM device." Rambus further objects to the request as compound. Rambus further objects that the request calls for a legal conclusion. Rambus further objects to this request on the grounds that Rambus is not familiar, and cannot through reasonable inquiry become familiar, with the operation of all non-compatible DRAM devices. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of

the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at one or more times between December 1991 and June 1996, Rambus amended its pending U.S. patent applications, filed continuation applications, and filed divisional applications. Rambus is not presently aware of any non-compatible devices that would infringe claims that were amended in or added to its U.S. Patent applications between December 1991 and June 1996 if such claims were included in an issued patent, with the exception of MDRAM devices designed by MoSys. By preliminary amendment dated September 6, 1994, Rambus properly added claims in its patent application with serial number 08/222,646 that were fully supported by the specification and that Rambus intended would read on MoSys MDRAM. *See, e.g.*, *Kingsdown Medical Consultants, Ltd. v. Hollister, Inc.*, 863 F.2d 867, 874 (Fed. Cir. 1988), *cert. denied*, 490 U.S. 1067 (1989) ("nor is it in any manner improper to amend or insert claims intended to cover a competitor's product the applicant's attorney has learned about during the prosecution of a patent application"). After the application issued as U.S. Patent No. 5,513,327 and the MoSys device was closely examined, Rambus informed MoSys of Rambus's belief that MoSys was infringing the patent. The parties settled their dispute and no infringement ruling was ultimately obtained.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 343:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus had claims in pending patent applications that, if included in an issued patent, would cover when data output occurs synchronously with respect to both the rising edge of the external clock signal and the falling edge of the external clock signal in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 343:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "believed," "synchronously," "external clock signal," "would cover when," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus had any claims in pending patent applications that, if included in an issued patent, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 344:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus could amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would cover when data output occurs synchronously with respect to both the rising edge of the external clock signal and the falling edge of the external clock signal in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 344:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "could amend its pending patent applications, or file continuation or divisional applications, to add claims," and the terms "believed," "synchronously," "external clock signal," "would cover when," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus could amend its pending patent applications or file continuation or divisional applications to add valid claims that, if included in an issued patent application, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 345:**

Admit that, at one or more times between December 1991 and June 1996, Rambus attempted to amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would cover when data output occurs synchronously with respect to both the rising edge of the external clock signal and the falling edge of the external clock signal in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 345:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "attempted to amend pending patent applications, or file continuation or divisional applications, to add claims" and the terms "synchronously," "external clock signal," "would cover when," and "non-compatible DRAM device." Rambus further objects to the request as compound. Rambus further objects that the request calls for a legal conclusion. Rambus further objects to this request on the grounds that Rambus is not familiar, and cannot through reasonable inquiry become familiar, with the operation of all non-compatible DRAM devices. Rambus further objects that, to the extent that "cover when" is to be interpreted as

"infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at one or more times between December 1991 and June 1996, Rambus amended its pending U.S. patent applications, filed continuation applications, and filed divisional applications. Rambus is not presently aware of any non-compatible devices that would infringe claims that were amended in or added to its U.S. Patent applications between December 1991 and June 1996 if such claims were included in an issued patent, with the exception of MDRAM devices designed by MoSys. By preliminary amendment dated September 6, 1994, Rambus properly added claims in its patent application with serial number 08/222,646 that were fully supported by the specification and that Rambus intended would read on MoSys MDRAM. *See, e.g.*, *Kingsdown Medical Consultants, Ltd. v. Hollister, Inc.*, 863 F.2d 867, 874 (Fed. Cir. 1988), *cert. denied*, 490 U.S. 1067 (1989) ("nor is it in any manner improper to amend or insert claims intended to cover a competitor's product the applicant's attorney has learned about during the prosecution of a patent application"). After the application issued as U.S. Patent No. 5,513,327 and the MoSys device was closely examined, Rambus informed MoSys of Rambus's belief that MoSys was infringing the patent. The parties settled their dispute and no infringement ruling was ultimately obtained.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 346:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus had claims in pending patent applications that, if included in an issued patent, would cover the input of a first portion of data synchronously with respect to a rising edge of an external clock signal and a second portion of

data synchronously with respect to a falling edge of the external clock signal in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 346:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "believed," "first portion of data," "second portion of data," "synchronously," "external clock signal," "cover," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus had any claims in pending patent applications that, if included in an issued patent, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 347:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus could amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would cover the input of a first portion of data synchronously with respect to a rising edge of an external clock signal and a second portion of data synchronously with respect to a falling edge of the external clock signal in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 347:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "could amend its pending patent applications, or file continuation or

divisional applications, to add claims," and the terms "believed," "first portion of data," "second portion of data," "synchronously," "external clock signal," "cover," and "non-compatible DRAM device."

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Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 348:**

Admit that, at one or more times between December 1991 and June 1996, Rambus attempted to amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would cover the input of a first portion of data synchronously with respect to a rising edge of an external clock signal and a second portion of data synchronously with respect to a falling edge of the external clock signal in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 348:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "attempted to amend pending patent applications, or file continuation or divisional applications, to add claims" and the terms "first portion of data," "second portion of data," "synchronously," "external clock signal," "cover," and "non-compatible DRAM device."

Rambus further objects to the request as compound. Rambus further objects that the request calls for a legal conclusion. Rambus further objects to this request on the grounds that Rambus is not familiar, and cannot through reasonable inquiry become familiar, with the operation of all non-compatible DRAM devices. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at one or more times between December 1991 and June 1996, Rambus amended its pending U.S. patent applications, filed continuation applications, and filed divisional applications. Rambus is not presently aware of any non-compatible devices that would infringe claims that were amended in or added to its U.S. Patent applications between December 1991 and June 1996 if such claims were included in an issued patent, with the exception of MDRAM devices designed by MoSys. By preliminary amendment dated September 6, 1994, Rambus properly added claims in its patent application with serial number 08/222,646 that were fully supported by the specification and that Rambus intended would read on MoSys MDRAM. *See, e.g., Kingsdown Medical Consultants, Ltd. v. Hollister, Inc.*, 863 F.2d 867, 874 (Fed. Cir. 1988), *cert. denied*, 490 U.S. 1067 (1989) ("nor is it in any manner improper to amend or insert claims intended to cover a competitor's product the applicant's attorney has learned about during the prosecution of a patent application"). After the application issued as U.S. Patent No. 5,513,327 and the MoSys device was closely examined, Rambus informed MoSys of Rambus's belief that MoSys was infringing the patent. The parties settled their dispute and no infringement ruling was ultimately obtained.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 349:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus had claims in pending patent applications that, if included in an issued patent, would cover when data input occurs synchronously with respect to both the rising edge of the external clock signal and the falling edge of the external clock signal in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 349:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "believed," "synchronously," "external clock signal," "would cover when," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus had any claims in pending patent applications that, if included in an issued patent, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 350:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus could amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would cover when data input occurs synchronously with respect to both the rising edge of the external clock signal and the falling edge of the external clock signal in a non-

compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 350:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "could amend its pending patent applications, or file continuation or divisional applications, to add claims," and the terms "believed," "synchronously," "external clock signal," "would cover when," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus could amend its pending patent applications or file continuation or divisional applications to add valid claims that, if included in an issued patent application, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 351:**

Admit that, at one or more times between December 1991 and June 1996, Rambus attempted to amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would cover when data input occurs synchronously with respect to both the rising edge of the external clock signal and the falling edge of the external clock signal in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 351:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "attempted to amend pending patent applications, or file continuation

or divisional applications, to add claims" and the terms "synchronously," "external clock signal," "would cover when," and "non-compatible DRAM device." Rambus further objects to the request as compound. Rambus further objects that the request calls for a legal conclusion. Rambus further objects to this request on the grounds that Rambus is not familiar, and cannot through reasonable inquiry become familiar, with the operation of all non-compatible DRAM devices. Rambus further objects that, to the extent that "cover when" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at one or more times between December 1991 and June 1996, Rambus amended its pending U.S. patent applications, filed continuation applications, and filed divisional applications. Rambus is not presently aware of any non-compatible devices that would infringe claims that were amended in or added to its U.S. Patent applications between December 1991 and June 1996 if such claims were included in an issued patent, with the exception of MDRAM devices designed by MoSys. By preliminary amendment dated September 6, 1994, Rambus properly added claims in its patent application with serial number 08/222,646 that were fully supported by the specification and that Rambus intended would read on MoSys MDRAM. *See, e.g.*, *Kingsdown Medical Consultants, Ltd. v. Hollister, Inc.*, 863 F.2d 867, 874 (Fed. Cir. 1988), *cert. denied*, 490 U.S. 1067 (1989) ("nor is it in any manner improper to amend or insert claims intended to cover a competitor's product the applicant's attorney has learned about during the prosecution of a patent application"). After the application issued as U.S. Patent No. 5,513,327 and the MoSys device was closely examined, Rambus informed MoSys of Rambus's belief that MoSys was infringing the patent. The parties settled their dispute and no infringement ruling was ultimately obtained.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 352:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus had claims in pending patent applications that, if included in an issued patent, would cover the output of a first portion of data synchronously with respect to a first external clock signal and a second portion of data synchronously with respect to a second external clock signal in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 352:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "believed," "first portion of data," "second portion of data," "synchronously," "first external clock signal," "second external clock signal," "cover," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus had any claims in pending patent applications that, if included in an issued patent, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 353:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus could amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an

issued patent, would cover the output of a first portion of data synchronously with respect to a first external clock signal and a second portion of data synchronously with respect to a second external clock signal in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 353:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "could amend its pending patent applications, or file continuation or divisional applications, to add claims," and the terms "believed," "first portion of data," "second portion of data," "synchronously," "first external clock signal," "second external clock signal," "cover," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus could amend its pending patent applications or file continuation or divisional applications to add valid claims that, if included in an issued patent application, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 354:**

Admit that, at one or more times between December 1991 and June 1996, Rambus attempted to amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would cover the output of a first portion of data synchronously with respect to a first external clock signal and a second portion of data synchronously with respect to a second external clock signal in a non-compatible DRAM

device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 354:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "attempted to amend pending patent applications, or file continuation or divisional applications, to add claims" and the terms "first portion of data," "second portion of data," "synchronously," "first external clock signal," "second external clock signal," "cover," and "non-compatible DRAM device." Rambus further objects to the request as compound. Rambus further objects that the request calls for a legal conclusion. Rambus further objects to this request on the grounds that Rambus is not familiar, and cannot through reasonable inquiry become familiar, with the operation of all non-compatible DRAM devices. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at one or more times between December 1991 and June 1996, Rambus amended its pending U.S. patent applications, filed continuation applications, and filed divisional applications. Rambus is not presently aware of any non-compatible devices that would infringe claims that were amended in or added to its U.S. Patent applications between December 1991 and June 1996 if such claims were included in an issued patent, with the exception of MDRAM devices designed by MoSys. By preliminary amendment dated September 6, 1994, Rambus properly added claims in its patent application with serial number 08/222,646 that were fully supported by the specification and that Rambus intended would read on MoSys MDRAM. *See, e.g., Kingsdown Medical Consultants, Ltd. v. Hollister, Inc.*, 863 F.2d 867, 874 (Fed. Cir. 1988), *cert. denied*, 490 U.S. 1067 (1989) ("nor is it in any manner improper to amend or insert claims intended to cover a competitor's product the applicant's attorney has

learned about during the prosecution of a patent application"). After the application issued as U.S. Patent No. 5,513,327 and the MoSys device was closely examined, Rambus informed MoSys of Rambus's belief that MoSys was infringing the patent. The parties settled their dispute and no infringement ruling was ultimately obtained.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 355:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus had claims in pending patent applications that, if included in an issued patent, would cover when data output occurs synchronously with respect to a both a first external clock signal and a second external clock signal in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 355:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "believed," "synchronously," "first external clock signal," "second external clock signal," "would cover when," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus had any claims in pending patent applications that, if included in an issued patent, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 356:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus could amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would cover when data output occurs synchronously with respect to a both a first external clock signal and a second external clock signal in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 356:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "could amend its pending patent applications, or file continuation or divisional applications, to add claims," and the terms "believed," "synchronously," "first external clock signal," "second external clock signal," "would cover when," and "non-compatible DRAM device."

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Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 357:**

Admit that, at one or more times between December 1991 and June 1996, Rambus

attempted to amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would cover when data output occurs synchronously with respect to a both a first external clock signal and a second external clock signal in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 357:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "attempted to amend pending patent applications, or file continuation or divisional applications, to add claims" and the terms "synchronously," "first external clock signal," "second external clock signal," "would cover when," and "non-compatible DRAM device." Rambus further objects to the request as compound. Rambus further objects that the request calls for a legal conclusion. Rambus further objects to this request on the grounds that Rambus is not familiar, and cannot through reasonable inquiry become familiar, with the operation of all non-compatible DRAM devices. Rambus further objects that, to the extent that "cover when" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

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on MoSys MDRAM. *See, e.g.*, *Kingsdown Medical Consultants, Ltd. v. Hollister, Inc.*, 863 F.2d 867, 874 (Fed. Cir. 1988), *cert. denied*, 490 U.S. 1067 (1989) ("nor is it in any manner improper to amend or insert claims intended to cover a competitor's product the applicant's attorney has learned about during the prosecution of a patent application"). After the application issued as U.S. Patent No. 5,513,327 and the MoSys device was closely examined, Rambus informed MoSys of Rambus's belief that MoSys was infringing the patent. The parties settled their dispute and no infringement ruling was ultimately obtained.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 358:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus had claims in pending patent applications that, if included in an issued patent, would cover the input of a first portion of data synchronously with respect to a first external clock signal and a second portion of data synchronously with respect to a second external clock signal in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 358:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "believed," "first portion of data," "second portion of data," "synchronously," "first external clock signal," "second external clock signal," "cover," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus had any claims in pending patent applications that, if included in an issued patent, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the

Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 359:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus could amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would cover the input of a first portion of data synchronously with respect to a first external clock signal and a second portion of data synchronously with respect to a second external clock signal in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 359:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "could amend its pending patent applications, or file continuation or divisional applications, to add claims," and the terms "believed," "first portion of data," "second portion of data," "synchronously," "first external clock signal," "second external clock signal," "cover," and "non-compatible DRAM device."

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Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 360:**

Admit that, at one or more times between December 1991 and June 1996, Rambus attempted to amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would cover the input of a first portion of data synchronously with respect to a first external clock signal and a second portion of data synchronously with respect to a second external clock signal in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 360:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "attempted to amend pending patent applications, or file continuation or divisional applications, to add claims" and the terms "first portion of data," "second portion of data," "synchronously," "first external clock signal," "second external clock signal," "cover," and "non-compatible DRAM device." Rambus further objects to the request as compound. Rambus further objects that the request calls for a legal conclusion. Rambus further objects to this request on the grounds that Rambus is not familiar, and cannot through reasonable inquiry become familiar, with the operation of all non-compatible DRAM devices. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

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Rambus admits that at one or more times between December 1991 and June 1996, Rambus amended its pending U.S. patent applications, filed continuation applications, and filed divisional applications. Rambus is not presently aware of any non-compatible devices that

would infringe claims that were amended in or added to its U.S. Patent applications between December 1991 and June 1996 if such claims were included in an issued patent, with the exception of MDRAM devices designed by MoSys. By preliminary amendment dated September 6, 1994, Rambus properly added claims in its patent application with serial number 08/222,646 that were fully supported by the specification and that Rambus intended would read on MoSys MDRAM. *See, e.g.*, *Kingsdown Medical Consultants, Ltd. v. Hollister, Inc.*, 863 F.2d 867, 874 (Fed. Cir. 1988), *cert. denied*, 490 U.S. 1067 (1989) ("nor is it in any manner improper to amend or insert claims intended to cover a competitor's product the applicant's attorney has learned about during the prosecution of a patent application"). After the application issued as U.S. Patent No. 5,513,327 and the MoSys device was closely examined, Rambus informed MoSys of Rambus's belief that MoSys was infringing the patent. The parties settled their dispute and no infringement ruling was ultimately obtained.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 361:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus had claims in pending patent applications that, if included in an issued patent, would cover when data input occurs synchronously with respect to both a first and a second external clock signal in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 361:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "believed," "synchronously," "first . . . external clock signal," "second external clock signal," "would cover when," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus had any claims in

pending patent applications that, if included in an issued patent, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 362:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus could amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would cover when data input occurs synchronously with respect to both a first and a second external clock signal in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 362:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "could amend its pending patent applications, or file continuation or divisional applications, to add claims," and the terms "believed," "synchronously," "first . . . external clock signal," "second external clock signal," "would cover when," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus could amend its pending patent applications or file continuation or divisional applications to add valid claims that, if included in an issued patent application, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered

belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 363:**

Admit that, at one or more times between December 1991 and June 1996, Rambus attempted to amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would cover when data input occurs synchronously with respect to both a first and a second external clock signal in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 363:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "attempted to amend pending patent applications, or file continuation or divisional applications, to add claims" and the terms "synchronously," "first . . . external clock signal," "second external clock signal," "would cover when," and "non-compatible DRAM device." Rambus further objects to the request as compound. Rambus further objects that the request calls for a legal conclusion. Rambus further objects to this request on the grounds that Rambus is not familiar, and cannot through reasonable inquiry become familiar, with the operation of all non-compatible DRAM devices. Rambus further objects that, to the extent that "cover when" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at one or more times between December 1991 and June 1996,

Rambus amended its pending U.S. patent applications, filed continuation applications, and filed divisional applications. Rambus is not presently aware of any non-compatible devices that would infringe claims that were amended in or added to its U.S. Patent applications between December 1991 and June 1996 if such claims were included in an issued patent, with the exception of MDRAM devices designed by MoSys. By preliminary amendment dated September 6, 1994, Rambus properly added claims in its patent application with serial number 08/222,646 that were fully supported by the specification and that Rambus intended would read on MoSys MDRAM. *See, e.g.*, *Kingsdown Medical Consultants, Ltd. v. Hollister, Inc.*, 863 F.2d 867, 874 (Fed. Cir. 1988), *cert. denied*, 490 U.S. 1067 (1989) ("nor is it in any manner improper to amend or insert claims intended to cover a competitor's product the applicant's attorney has learned about during the prosecution of a patent application"). After the application issued as U.S. Patent No. 5,513,327 and the MoSys device was closely examined, Rambus informed MoSys of Rambus's belief that MoSys was infringing the patent. The parties settled their dispute and no infringement ruling was ultimately obtained.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 364:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus had claims in pending patent applications that, if included in an issued patent, would cover the use of a dual edge clocking scheme which inputs and outputs data synchronously with the rising and falling edge of an external clock in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 364:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "believed," "dual edge clocking scheme," "synchronously," "the rising and falling edge," "external clock signal," "cover," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus had any claims in pending patent applications that, if included in an issued patent, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 365:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus could amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would cover the use of a dual edge clocking scheme which inputs and outputs data synchronously with the rising and falling edge of an external clock in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 365:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "could amend its pending patent applications, or file continuation or divisional applications, to add claims," and the terms "believed," "dual edge clocking scheme," "synchronously," "the rising and falling edge," "external clock signal," "cover," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus could amend its pending patent applications or file continuation or divisional applications to add valid claims

that, if included in an issued patent application, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 366:**

Admit that, at one or more times between December 1991 and June 1996, Rambus attempted to amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would cover the use of a dual edge clocking scheme which inputs and outputs data synchronously with the rising and falling edge of an external clock in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 366:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "attempted to amend pending patent applications, or file continuation or divisional applications, to add claims" and the terms "dual edge clocking scheme," "synchronously," "the rising and falling edge," "external clock signal," "cover," and "non-compatible DRAM device." Rambus further objects to the request as compound. Rambus further objects that the request calls for a legal conclusion. Rambus further objects to this request on the grounds that Rambus is not familiar, and cannot through reasonable inquiry become familiar, with the operation of all non-compatible DRAM devices. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be

determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at one or more times between December 1991 and June 1996, Rambus amended its pending U.S. patent applications, filed continuation applications, and filed divisional applications. Rambus is not presently aware of any non-compatible devices that would infringe claims that were amended in or added to its U.S. Patent applications between December 1991 and June 1996 if such claims were included in an issued patent, with the exception of MDRAM devices designed by MoSys. By preliminary amendment dated September 6, 1994, Rambus properly added claims in its patent application with serial number 08/222,646 that were fully supported by the specification and that Rambus intended would read on MoSys MDRAM. *See, e.g., Kingsdown Medical Consultants, Ltd. v. Hollister, Inc.*, 863 F.2d 867, 874 (Fed. Cir. 1988), *cert. denied*, 490 U.S. 1067 (1989) ("nor is it in any manner improper to amend or insert claims intended to cover a competitor's product the applicant's attorney has learned about during the prosecution of a patent application"). After the application issued as U.S. Patent No. 5,513,327 and the MoSys device was closely examined, Rambus informed MoSys of Rambus's belief that MoSys was infringing the patent. The parties settled their dispute and no infringement ruling was ultimately obtained.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 367:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus had claims in pending patent applications that, if included in an issued patent, would cover when data input and output occurs synchronously with the rising and falling edge of an external clock, according to a dual edge clocking scheme in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 367:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least

with respect to the terms "believed," "synchronously," "the rising and falling edge," "external clock signal," "dual edge clocking scheme," "would cover when," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus had any claims in pending patent applications that, if included in an issued patent, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 368:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus could amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would cover when data input and output occurs synchronously with the rising and falling edge of an external clock, according to a dual edge clocking scheme in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 368:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "could amend its pending patent applications, or file continuation or divisional applications, to add claims," and the terms "believed," "synchronously," "the rising and falling edge," "external clock signal," "dual edge clocking scheme," "would cover when," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus could amend its pending patent applications or file continuation or divisional applications to add valid claims that, if included in an issued patent application, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 369:**

Admit that, at one or more times between December 1991 and June 1996, Rambus attempted to amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would cover when data input and output occurs synchronously with the rising and falling edge of an external clock, according to a dual edge clocking scheme in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 369:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "attempted to amend pending patent applications, or file continuation or divisional applications, to add claims" and the terms "synchronously," "the rising and falling edge," "external clock signal," "dual edge clocking scheme," "would cover when," and "non-compatible DRAM device." Rambus further objects to the request as compound. Rambus further objects that the request calls for a legal conclusion. Rambus further objects to this request on the grounds that Rambus is not familiar, and cannot through reasonable inquiry become familiar, with the operation of all non-compatible DRAM devices. Rambus further

objects that, to the extent that "cover when" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at one or more times between December 1991 and June 1996, Rambus amended its pending U.S. patent applications, filed continuation applications, and filed divisional applications. Rambus is not presently aware of any non-compatible devices that would infringe claims that were amended in or added to its U.S. Patent applications between December 1991 and June 1996 if such claims were included in an issued patent, with the exception of MDRAM devices designed by MoSys. By preliminary amendment dated September 6, 1994, Rambus properly added claims in its patent application with serial number 08/222,646 that were fully supported by the specification and that Rambus intended would read on MoSys MDRAM. *See, e.g., Kingsdown Medical Consultants, Ltd. v. Hollister, Inc.*, 863 F.2d 867, 874 (Fed. Cir. 1988), *cert. denied*, 490 U.S. 1067 (1989) ("nor is it in any manner improper to amend or insert claims intended to cover a competitor's product the applicant's attorney has learned about during the prosecution of a patent application"). After the application issued as U.S. Patent No. 5,513,327 and the MoSys device was closely examined, Rambus informed MoSys of Rambus's belief that MoSys was infringing the patent. The parties settled their dispute and no infringement ruling was ultimately obtained.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 370:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus had claims in pending patent applications that, if included in an issued patent, would be infringed by a non-compatible DRAM

device that output a first portion of data in response to a rising edge of a clock signal and a second portion of data in response to a falling edge of a clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 370:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "believed," "first portion of data," "second portion of data," "in response to," "a clock signal," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus had any claims in pending patent applications that, if included in an issued patent, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 371:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus could amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would be infringed by a non-compatible DRAM device that output a first portion of data in response to a rising edge of a clock signal and a second portion of data in response to a falling edge of a clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 371:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "could amend its pending patent applications, or file continuation or

divisional applications, to add claims," and the terms "believed," "first portion of data," "second portion of data," "in response to," "a clock signal," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus could amend its pending patent applications or file continuation or divisional applications to add valid claims that, if included in an issued patent application, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 372:**

Admit that, at one or more times between December 1991 and June 1996, Rambus attempted to amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would be infringed by a non-compatible DRAM device that output a first portion of data in response to a rising edge of a clock signal and a second portion of data in response to a falling edge of a clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 372:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "attempted to amend pending patent applications, or file continuation or divisional applications, to add claims" and the terms "first portion of data," "second portion of data," "in response to," "a clock signal," and "non-compatible DRAM device." Rambus further objects to the request as compound. Rambus further objects that the request calls for a legal conclusion. Rambus further objects to this request on the grounds that Rambus is not familiar,

and cannot through reasonable inquiry become familiar, with the operation of all non-compatible DRAM devices. Rambus further objects that whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at one or more times between December 1991 and June 1996, Rambus amended its pending U.S. patent applications, filed continuation applications, and filed divisional applications. Rambus is not presently aware of any non-compatible devices that would infringe claims that were amended in or added to its U.S. Patent applications between December 1991 and June 1996 if such claims were included in an issued patent, with the exception of MDRAM devices designed by MoSys. By preliminary amendment dated September 6, 1994, Rambus properly added claims in its patent application with serial number 08/222,646 that were fully supported by the specification and that Rambus intended would read on MoSys MDRAM. *See, e.g.*, *Kingsdown Medical Consultants, Ltd. v. Hollister, Inc.*, 863 F.2d 867, 874 (Fed. Cir. 1988), *cert. denied*, 490 U.S. 1067 (1989) ("nor is it in any manner improper to amend or insert claims intended to cover a competitor's product the applicant's attorney has learned about during the prosecution of a patent application"). After the application issued as U.S. Patent No. 5,513,327 and the MoSys device was closely examined, Rambus informed MoSys of Rambus's belief that MoSys was infringing the patent. The parties settled their dispute and no infringement ruling was ultimately obtained.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 373:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus had claims in pending patent

applications that, if included in an issued patent, would be infringed by a non-compatible DRAM device that input a first portion of data in response to a rising edge of a clock signal and a second portion of data in response to a falling edge of a clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 373:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "believed," "first portion of data," "second portion of data," "in response to," "a clock signal," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus had any claims in pending patent applications that, if included in an issued patent, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 374:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus could amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would be infringed by a non-compatible DRAM device that input a first portion of data in response to a rising edge of a clock signal and a second portion of data in response to a falling edge of a clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 374:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least

with respect to the phrase "could amend its pending patent applications, or file continuation or divisional applications, to add claims," and the terms "believed," "first portion of data," "second portion of data," "in response to," "a clock signal," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus could amend its pending patent applications or file continuation or divisional applications to add valid claims that, if included in an issued patent application, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 375:**

Admit that, at one or more times between December 1991 and June 1996, Rambus attempted to amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would be infringed by a non-compatible DRAM device that input a first portion of data in response to a rising edge of a clock signal and a second portion of data in response to a falling edge of a clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 375:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "attempted to amend pending patent applications, or file continuation or divisional applications, to add claims" and the terms "first portion of data," "second portion of data," "in response to," "a clock signal," and "non-compatible DRAM device." Rambus further objects to the request as compound. Rambus further objects that the request calls for a legal

conclusion. Rambus further objects to this request on the grounds that Rambus is not familiar, and cannot through reasonable inquiry become familiar, with the operation of all non-compatible DRAM devices. Rambus further objects that whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at one or more times between December 1991 and June 1996, Rambus amended its pending U.S. patent applications, filed continuation applications, and filed divisional applications. Rambus is not presently aware of any non-compatible devices that would infringe claims that were amended in or added to its U.S. Patent applications between December 1991 and June 1996 if such claims were included in an issued patent, with the exception of MDRAM devices designed by MoSys. By preliminary amendment dated September 6, 1994, Rambus properly added claims in its patent application with serial number 08/222,646 that were fully supported by the specification and that Rambus intended would read on MoSys MDRAM. *See*, *e.g.*, *Kingsdown Medical Consultants, Ltd. v. Hollister, Inc.*, 863 F.2d 867, 874 (Fed. Cir. 1988), *cert. denied*, 490 U.S. 1067 (1989) ("nor is it in any manner improper to amend or insert claims intended to cover a competitor's product the applicant's attorney has learned about during the prosecution of a patent application"). After the application issued as U.S. Patent No. 5,513,327 and the MoSys device was closely examined, Rambus informed MoSys of Rambus's belief that MoSys was infringing the patent. The parties settled their dispute and no infringement ruling was ultimately obtained.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 376:**

Admit that, at various times between December 1991 and June 1996, various directors,

officers or employees of Rambus believed that Rambus had claims in pending patent applications that, if included in an issued patent, would be infringed by a non-compatible DRAM device that output a first portion of data synchronously with respect to a rising edge of an external clock signal and a second portion of data synchronously with respect to a falling edge of the external clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 376:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "believed," "first portion of data," "second portion of data," "synchronously," "external clock signal," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus had any claims in pending patent applications that, if included in an issued patent, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 377:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus could amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would be infringed by a non-compatible DRAM device that output a first portion of data synchronously with respect to a rising edge of an external clock signal and a second portion of data synchronously with respect to a falling edge of the external clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 377:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "could amend its pending patent applications, or file continuation or divisional applications, to add claims," and the terms "believed," "first portion of data," "second portion of data," "synchronously," "external clock signal," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus could amend its pending patent applications or file continuation or divisional applications to add valid claims that, if included in an issued patent application, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 378:**

Admit that, at one or more times between December 1991 and June 1996, Rambus attempted to amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would be infringed by a non-compatible DRAM device that output a first portion of data synchronously with respect to a rising edge of an external clock signal and a second portion of data synchronously with respect to a falling edge of the external clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 378:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least

with respect to the phrase "attempted to amend pending patent applications, or file continuation or divisional applications, to add claims" and the terms "first portion of data," "second portion of data," "synchronously," "external clock signal," and "non-compatible DRAM device." Rambus further objects to the request as compound. Rambus further objects that the request calls for a legal conclusion. Rambus further objects to this request on the grounds that Rambus is not familiar, and cannot through reasonable inquiry become familiar, with the operation of all non-compatible DRAM devices. Rambus further objects that whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at one or more times between December 1991 and June 1996, Rambus amended its pending U.S. patent applications, filed continuation applications, and filed divisional applications. Rambus is not presently aware of any non-compatible devices that would infringe claims that were amended in or added to its U.S. Patent applications between December 1991 and June 1996 if such claims were included in an issued patent, with the exception of MDRAM devices designed by MoSys. By preliminary amendment dated September 6, 1994, Rambus properly added claims in its patent application with serial number 08/222,646 that were fully supported by the specification and that Rambus intended would read on MoSys MDRAM. *See, e.g.*, *Kingsdown Medical Consultants, Ltd. v. Hollister, Inc.*, 863 F.2d 867, 874 (Fed. Cir. 1988), *cert. denied*, 490 U.S. 1067 (1989) ("nor is it in any manner improper to amend or insert claims intended to cover a competitor's product the applicant's attorney has learned about during the prosecution of a patent application"). After the application issued as U.S. Patent No. 5,513,327 and the MoSys device was closely examined, Rambus informed MoSys of Rambus's belief that MoSys was infringing the patent. The parties settled their dispute and no infringement ruling was ultimately obtained.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 379:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus had claims in pending patent applications that, if included in an issued patent, would be infringed by a non-compatible DRAM device where data output occurs synchronously with respect to both the rising edge of the external clock signal and the falling edge of the external clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 379:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "believed," "synchronously," "external clock signal," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus had any claims in pending patent applications that, if included in an issued patent, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 380:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus could amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an

issued patent, would be infringed by a non-compatible DRAM device where data output occurs synchronously with respect to both the rising edge of the external clock signal and the falling edge of the external clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 380:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "could amend its pending patent applications, or file continuation or divisional applications, to add claims," and the terms "believed," "synchronously," "external clock signal," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus could amend its pending patent applications or file continuation or divisional applications to add valid claims that, if included in an issued patent application, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 381:**

Admit that, at one or more times between December 1991 and June 1996, Rambus attempted to amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would be infringed by a non-compatible DRAM device where data output occurs synchronously with respect to both the rising edge of the external clock signal and the falling edge of the external clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 381:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "attempted to amend pending patent applications, or file continuation or divisional applications, to add claims" and the terms "synchronously," "external clock signal," and "non-compatible DRAM device." Rambus further objects to the request as compound. Rambus further objects that the request calls for a legal conclusion. Rambus further objects to this request on the grounds that Rambus is not familiar, and cannot through reasonable inquiry become familiar, with the operation of all non-compatible DRAM devices. Rambus further objects that whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at one or more times between December 1991 and June 1996, Rambus amended its pending U.S. patent applications, filed continuation applications, and filed divisional applications. Rambus is not presently aware of any non-compatible devices that would infringe claims that were amended in or added to its U.S. Patent applications between December 1991 and June 1996 if such claims were included in an issued patent, with the exception of MDRAM devices designed by MoSys. By preliminary amendment dated September 6, 1994, Rambus properly added claims in its patent application with serial number 08/222,646 that were fully supported by the specification and that Rambus intended would read on MoSys MDRAM. *See, e.g.*, *Kingsdown Medical Consultants, Ltd. v. Hollister, Inc.*, 863 F.2d 867, 874 (Fed. Cir. 1988), *cert. denied*, 490 U.S. 1067 (1989) ("nor is it in any manner improper to amend or insert claims intended to cover a competitor's product the applicant's attorney has learned about during the prosecution of a patent application"). After the application issued as U.S. Patent No. 5,513,327 and the MoSys device was closely examined, Rambus informed MoSys of Rambus's belief that MoSys was infringing the patent. The parties settled their

dispute and no infringement ruling was ultimately obtained.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 382:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus had claims in pending patent applications that, if included in an issued patent, would be infringed by a non-compatible DRAM device that inputs a first portion of data synchronously with respect to a rising edge of an external clock signal and a second portion of data synchronously with respect to a falling edge of the external clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 382:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "believed," "first portion of data," "second portion of data," "synchronously," "external clock signal," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus had any claims in pending patent applications that, if included in an issued patent, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 383:**

Admit that, at various times between December 1991 and June 1996, various directors,

officers or employees of Rambus believed that Rambus could amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would be infringed by a non-compatible DRAM device that inputs a first portion of data synchronously with respect to a rising edge of an external clock signal and a second portion of data synchronously with respect to a falling edge of the external clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 383:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "could amend its pending patent applications, or file continuation or divisional applications, to add claims," and the terms "believed," "first portion of data," "second portion of data," "synchronously," "external clock signal," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus could amend its pending patent applications or file continuation or divisional applications to add valid claims that, if included in an issued patent application, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 384:**

Admit that, at one or more times between December 1991 and June 1996, Rambus attempted to amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would be infringed by a non-

compatible DRAM device that inputs a first portion of data synchronously with respect to a rising edge of an external clock signal and a second portion of data synchronously with respect to a falling edge of the external clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 384:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "attempted to amend pending patent applications, or file continuation or divisional applications, to add claims" and the terms "first portion of data," "second portion of data," "synchronously," "external clock signal," and "non-compatible DRAM device." Rambus further objects to the request as compound. Rambus further objects that the request calls for a legal conclusion. Rambus further objects to this request on the grounds that Rambus is not familiar, and cannot through reasonable inquiry become familiar, with the operation of all non-compatible DRAM devices. Rambus further objects that whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at one or more times between December 1991 and June 1996, Rambus amended its pending U.S. patent applications, filed continuation applications, and filed divisional applications. Rambus is not presently aware of any non-compatible devices that would infringe claims that were amended in or added to its U.S. Patent applications between December 1991 and June 1996 if such claims were included in an issued patent, with the exception of MDRAM devices designed by MoSys. By preliminary amendment dated September 6, 1994, Rambus properly added claims in its patent application with serial number 08/222,646 that were fully supported by the specification and that Rambus intended would read on MoSys MDRAM. *See, e.g., Kingsdown Medical Consultants, Ltd. v. Hollister, Inc.*, 863 F.2d 867, 874 (Fed. Cir. 1988), *cert. denied*, 490 U.S. 1067 (1989) ("nor is it in any manner improper

to amend or insert claims intended to cover a competitor's product the applicant's attorney has learned about during the prosecution of a patent application"). After the application issued as U.S. Patent No. 5,513,327 and the MoSys device was closely examined, Rambus informed MoSys of Rambus's belief that MoSys was infringing the patent. The parties settled their dispute and no infringement ruling was ultimately obtained.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 385:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus had claims in pending patent applications that, if included in an issued patent, would be infringed by a non-compatible DRAM device where data input occurs synchronously with respect to both the rising edge of the external clock signal and the falling edge of the external clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 385:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "believed," "synchronously," "external clock signal," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus had any claims in pending patent applications that, if included in an issued patent, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 386:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus could amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would be infringed by a non-compatible DRAM device where data input occurs synchronously with respect to both the rising edge of the external clock signal and the falling edge of the external clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 386:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "could amend its pending patent applications, or file continuation or divisional applications, to add claims," and the terms "believed," "synchronously," "external clock signal," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus could amend its pending patent applications or file continuation or divisional applications to add valid claims that, if included in an issued patent application, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 387:**

Admit that, at one or more times between December 1991 and June 1996, Rambus

attempted to amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would be infringed by a non-compatible DRAM device where data input occurs synchronously with respect to both the rising edge of the external clock signal and the falling edge of the external clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 387:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "attempted to amend pending patent applications, or file continuation or divisional applications, to add claims" and the terms "synchronously," "external clock signal," and "non-compatible DRAM device." Rambus further objects to the request as compound. Rambus further objects that the request calls for a legal conclusion. Rambus further objects to this request on the grounds that Rambus is not familiar, and cannot through reasonable inquiry become familiar, with the operation of all non-compatible DRAM devices. Rambus further objects that whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at one or more times between December 1991 and June 1996, Rambus amended its pending U.S. patent applications, filed continuation applications, and filed divisional applications. Rambus is not presently aware of any non-compatible devices that would infringe claims that were amended in or added to its U.S. Patent applications between December 1991 and June 1996 if such claims were included in an issued patent, with the exception of MDRAM devices designed by MoSys. By preliminary amendment dated September 6, 1994, Rambus properly added claims in its patent application with serial number 08/222,646 that were fully supported by the specification and that Rambus intended would read on MoSys MDRAM. *See, e.g., Kingsdown Medical Consultants, Ltd. v. Hollister, Inc.*, 863 F.2d 867, 874 (Fed. Cir. 1988), *cert. denied*, 490 U.S. 1067 (1989) ("nor is it in any manner improper

to amend or insert claims intended to cover a competitor's product the applicant's attorney has learned about during the prosecution of a patent application"). After the application issued as U.S. Patent No. 5,513,327 and the MoSys device was closely examined, Rambus informed MoSys of Rambus's belief that MoSys was infringing the patent. The parties settled their dispute and no infringement ruling was ultimately obtained.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 388:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus had claims in pending patent applications that, if included in an issued patent, would be infringed by a non-compatible DRAM device that outputs a first portion of data synchronously with respect to a first external clock signal and a second portion of data synchronously with respect to a second external clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 388:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "believed," "first portion of data," "second portion of data," "synchronously," "first external clock signal," "second external clock signal," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus had any claims in pending patent applications that, if included in an issued patent, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 389:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus could amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would be infringed by a non-compatible DRAM device that outputs a first portion of data synchronously with respect to a first external clock signal and a second portion of data synchronously with respect to a second external clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 389:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "could amend its pending patent applications, or file continuation or divisional applications, to add claims," and the terms "believed," "first portion of data," "second portion of data," "synchronously," "first external clock signal," "second external clock signal," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus could amend its pending patent applications or file continuation or divisional applications to add valid claims that, if included in an issued patent application, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 390:**

Admit that, at one or more times between December 1991 and June 1996, Rambus attempted to amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would be infringed by a non-compatible DRAM device that outputs a first portion of data synchronously with respect to a first external clock signal and a second portion of data synchronously with respect to a second external clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 390:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "attempted to amend pending patent applications, or file continuation or divisional applications, to add claims" and the terms "first portion of data," "second portion of data," "synchronously," "first external clock signal," "second external clock signal," and "non-compatible DRAM device." Rambus further objects to the request as compound. Rambus further objects that the request calls for a legal conclusion. Rambus further objects to this request on the grounds that Rambus is not familiar, and cannot through reasonable inquiry become familiar, with the operation of all non-compatible DRAM devices. Rambus further objects that whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at one or more times between December 1991 and June 1996, Rambus amended its pending U.S. patent applications, filed continuation applications, and filed divisional applications. Rambus is not presently aware of any non-compatible devices that would infringe claims that were amended in or added to its U.S. Patent applications between December 1991 and June 1996 if such claims were included in an issued patent, with the exception of MDRAM devices designed by MoSys. By preliminary amendment dated

September 6, 1994, Rambus properly added claims in its patent application with serial number 08/222,646 that were fully supported by the specification and that Rambus intended would read on MoSys MDRAM. *See, e.g., Kingsdown Medical Consultants, Ltd. v. Hollister, Inc.*, 863 F.2d 867, 874 (Fed. Cir. 1988), *cert. denied*, 490 U.S. 1067 (1989) ("nor is it in any manner improper to amend or insert claims intended to cover a competitor's product the applicant's attorney has learned about during the prosecution of a patent application"). After the application issued as U.S. Patent No. 5,513,327 and the MoSys device was closely examined, Rambus informed MoSys of Rambus's belief that MoSys was infringing the patent. The parties settled their dispute and no infringement ruling was ultimately obtained.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 391:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus had claims in pending patent applications that, if included in an issued patent, would be infringed by a non-compatible DRAM device where data output occurs synchronously with respect to a both a first external clock signal and a second external clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 391:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "believed," "synchronously," "first external clock signal," "second external clock signal," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus had any claims in pending patent applications that, if included in an issued patent, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a

reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 392:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus could amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would be infringed by a non-compatible DRAM device where data output occurs synchronously with respect to a both a first external clock signal and a second external clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 392:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "could amend its pending patent applications, or file continuation or divisional applications, to add claims," and the terms "believed," "synchronously," "first external clock signal," "second external clock signal," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus could amend its pending patent applications or file continuation or divisional applications to add valid claims that, if included in an issued patent application, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 393:**

Admit that, at one or more times between December 1991 and June 1996, Rambus attempted to amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would be infringed by a non-compatible DRAM device where data output occurs synchronously with respect to a both a first external clock signal and a second external clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 393:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "attempted to amend pending patent applications, or file continuation or divisional applications, to add claims" and the terms "synchronously," "first external clock signal," "second external clock signal," and "non-compatible DRAM device." Rambus further objects to the request as compound. Rambus further objects that the request calls for a legal conclusion. Rambus further objects to this request on the grounds that Rambus is not familiar, and cannot through reasonable inquiry become familiar, with the operation of all non-compatible DRAM devices. Rambus further objects that whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at one or more times between December 1991 and June 1996, Rambus amended its pending U.S. patent applications, filed continuation applications, and filed divisional applications. Rambus is not presently aware of any non-compatible devices that would infringe claims that were amended in or added to its U.S. Patent applications between December 1991 and June 1996 if such claims were included in an issued patent, with the

exception of MDRAM devices designed by MoSys. By preliminary amendment dated September 6, 1994, Rambus properly added claims in its patent application with serial number 08/222,646 that were fully supported by the specification and that Rambus intended would read on MoSys MDRAM. *See, e.g., Kingsdown Medical Consultants, Ltd. v. Hollister, Inc.*, 863 F.2d 867, 874 (Fed. Cir. 1988), *cert. denied*, 490 U.S. 1067 (1989) ("nor is it in any manner improper to amend or insert claims intended to cover a competitor's product the applicant's attorney has learned about during the prosecution of a patent application"). After the application issued as U.S. Patent No. 5,513,327 and the MoSys device was closely examined, Rambus informed MoSys of Rambus's belief that MoSys was infringing the patent. The parties settled their dispute and no infringement ruling was ultimately obtained.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 394:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus had claims in pending patent applications that, if included in an issued patent, would be infringed by a non-compatible DRAM device that inputs a first portion of data synchronously with respect to a first external clock signal and a second portion of data synchronously with respect to a second external clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 394:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "believed," "first portion of data," "second portion of data," "synchronously," "first external clock signal," "second external clock signal," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus had any claims in pending patent applications that, if included in an issued patent, would be infringed by non-

compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 395:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus could amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would be infringed by a non-compatible DRAM device that inputs a first portion of data synchronously with respect to a first external clock signal and a second portion of data synchronously with respect to a second external clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 395:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "could amend its pending patent applications, or file continuation or divisional applications, to add claims," and the terms "believed," "first portion of data," "second portion of data," "synchronously," "first external clock signal," "second external clock signal," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus could amend its pending patent applications or file continuation or divisional applications to add valid claims that, if included in an issued patent application, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered

belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 396:**

Admit that, at one or more times between December 1991 and June 1996, Rambus attempted to amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would be infringed by a non-compatible DRAM device that inputs a first portion of data synchronously with respect to a first external clock signal and a second portion of data synchronously with respect to a second external clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 396:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "attempted to amend pending patent applications, or file continuation or divisional applications, to add claims" and the terms "first portion of data," "second portion of data," "synchronously," "first external clock signal," "second external clock signal," and "non-compatible DRAM device." Rambus further objects to the request as compound. Rambus further objects that the request calls for a legal conclusion. Rambus further objects to this request on the grounds that Rambus is not familiar, and cannot through reasonable inquiry become familiar, with the operation of all non-compatible DRAM devices. Rambus further objects that whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at one or more times between December 1991 and June 1996,

Rambus amended its pending U.S. patent applications, filed continuation applications, and filed divisional applications. Rambus is not presently aware of any non-compatible devices that would infringe claims that were amended in or added to its U.S. Patent applications between December 1991 and June 1996 if such claims were included in an issued patent, with the exception of MDRAM devices designed by MoSys. By preliminary amendment dated September 6, 1994, Rambus properly added claims in its patent application with serial number 08/222,646 that were fully supported by the specification and that Rambus intended would read on MoSys MDRAM. *See, e.g.*, *Kingsdown Medical Consultants, Ltd. v. Hollister, Inc.*, 863 F.2d 867, 874 (Fed. Cir. 1988), *cert. denied*, 490 U.S. 1067 (1989) ("nor is it in any manner improper to amend or insert claims intended to cover a competitor's product the applicant's attorney has learned about during the prosecution of a patent application"). After the application issued as U.S. Patent No. 5,513,327 and the MoSys device was closely examined, Rambus informed MoSys of Rambus's belief that MoSys was infringing the patent. The parties settled their dispute and no infringement ruling was ultimately obtained.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 397:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus had claims in pending patent applications that, if included in an issued patent, would be infringed by a non-compatible DRAM device where data input occurs synchronously with respect to both a first and a second external clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 397:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "believed," "synchronously," "first . . . external clock signal," "second external clock signal," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus had any claims in pending patent applications that, if included in an issued patent, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 398:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus could amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would be infringed by a non-compatible DRAM device where data input occurs synchronously with respect to both a first and a second external clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 398:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "could amend its pending patent applications, or file continuation or divisional applications, to add claims," and the terms "believed," "synchronously," "first . . . external clock signal," "second external clock signal," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus could amend its pending patent applications or file continuation or divisional applications to add valid claims that, if included in an issued patent application, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys.

Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 399:**

Admit that, at one or more times between December 1991 and June 1996, Rambus attempted to amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would be infringed by a non-compatible DRAM device where data input occurs synchronously with respect to both a first and a second external clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 399:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "attempted to amend pending patent applications, or file continuation or divisional applications, to add claims" and the terms "synchronously," "first . . . external clock signal," "second external clock signal," and "non-compatible DRAM device." Rambus further objects to the request as compound. Rambus further objects that the request calls for a legal conclusion. Rambus further objects to this request on the grounds that Rambus is not familiar, and cannot through reasonable inquiry become familiar, with the operation of all non-compatible DRAM devices. Rambus further objects that whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at one or more times between December 1991 and June 1996,

Rambus amended its pending U.S. patent applications, filed continuation applications, and filed divisional applications. Rambus is not presently aware of any non-compatible devices that would infringe claims that were amended in or added to its U.S. Patent applications between December 1991 and June 1996 if such claims were included in an issued patent, with the exception of MDRAM devices designed by MoSys. By preliminary amendment dated September 6, 1994, Rambus properly added claims in its patent application with serial number 08/222,646 that were fully supported by the specification and that Rambus intended would read on MoSys MDRAM. *See, e.g.*, *Kingsdown Medical Consultants, Ltd. v. Hollister, Inc.*, 863 F.2d 867, 874 (Fed. Cir. 1988), *cert. denied*, 490 U.S. 1067 (1989) ("nor is it in any manner improper to amend or insert claims intended to cover a competitor's product the applicant's attorney has learned about during the prosecution of a patent application"). After the application issued as U.S. Patent No. 5,513,327 and the MoSys device was closely examined, Rambus informed MoSys of Rambus's belief that MoSys was infringing the patent. The parties settled their dispute and no infringement ruling was ultimately obtained.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 400:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus had claims in pending patent applications that, if included in an issued patent, would be infringed by a non-compatible DRAM device that uses a dual edge clocking scheme which inputs and outputs data synchronously with the rising and falling edge of an external clock.

**RESPONSE TO REQUEST FOR ADMISSION NO. 400:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "believed," "dual edge clocking scheme," "synchronously," "the rising and falling edge," "external clock," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus had any claims in pending patent applications that, if included in an issued patent, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 401:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus could amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would be infringed by a non-compatible DRAM device that uses a dual edge clocking scheme which inputs and outputs data synchronously with the rising and falling edge of an external clock.

**RESPONSE TO REQUEST FOR ADMISSION NO. 401:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "could amend its pending patent applications, or file continuation or divisional applications, to add claims," and the terms "believed," "dual edge clocking scheme," "synchronously," "the rising and falling edge," "external clock," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus could amend its pending patent applications or file continuation or divisional applications to add valid claims

that, if included in an issued patent application, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 402:**

Admit that, at one or more times between December 1991 and June 1996, Rambus attempted to amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would be infringed by a non-compatible DRAM device that uses a dual edge clocking scheme which inputs and outputs data synchronously with the rising and falling edge of an external clock.

**RESPONSE TO REQUEST FOR ADMISSION NO. 402:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "attempted to amend pending patent applications, or file continuation or divisional applications, to add claims" and the terms "dual edge clocking scheme," "synchronously," "the rising and falling edge," "external clock," and "non-compatible DRAM device." Rambus further objects to the request as compound. Rambus further objects that the request calls for a legal conclusion. Rambus further objects to this request on the grounds that Rambus is not familiar, and cannot through reasonable inquiry become familiar, with the operation of all non-compatible DRAM devices. Rambus further objects that whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at one or more times between December 1991 and June 1996, Rambus amended its pending U.S. patent applications, filed continuation applications, and filed divisional applications. Rambus is not presently aware of any non-compatible devices that would infringe claims that were amended in or added to its U.S. Patent applications between December 1991 and June 1996 if such claims were included in an issued patent, with the exception of MDRAM devices designed by MoSys. By preliminary amendment dated September 6, 1994, Rambus properly added claims in its patent application with serial number 08/222,646 that were fully supported by the specification and that Rambus intended would read on MoSys MDRAM. *See*, *e.g.*, *Kingsdown Medical Consultants, Ltd. v. Hollister, Inc.*, 863 F.2d 867, 874 (Fed. Cir. 1988), *cert. denied*, 490 U.S. 1067 (1989) ("nor is it in any manner improper to amend or insert claims intended to cover a competitor's product the applicant's attorney has learned about during the prosecution of a patent application"). After the application issued as U.S. Patent No. 5,513,327 and the MoSys device was closely examined, Rambus informed MoSys of Rambus's belief that MoSys was infringing the patent. The parties settled their dispute and no infringement ruling was ultimately obtained.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 403:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus had claims in pending patent applications that, if included in an issued patent, would be infringed by a non-compatible DRAM device where data input and output occurs synchronously with the rising and falling edge of an external clock, according to a dual edge clocking scheme.

**RESPONSE TO REQUEST FOR ADMISSION NO. 403:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "believed," "dual edge clocking scheme," "synchronously," "the rising

and falling edge," "external clock," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus had any claims in pending patent applications that, if included in an issued patent, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 404:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus could amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would be infringed by a non-compatible DRAM device where data input and output occurs synchronously with the rising and falling edge of an external clock, according to a dual edge clocking scheme.

**RESPONSE TO REQUEST FOR ADMISSION NO. 404:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "could amend its pending patent applications, or file continuation or divisional applications, to add claims," and the terms "believed," "dual edge clocking scheme," "synchronously," "the rising and falling edge," "external clock," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned

and considered belief, between December 1991 and June 1996, that Rambus could amend its pending patent applications or file continuation or divisional applications to add valid claims that, if included in an issued patent application, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 405:**

Admit that, at one or more times between December 1991 and June 1996, Rambus attempted to amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would be infringed by a non-compatible DRAM device where data input and output occurs synchronously with the rising and falling edge of an external clock, according to a dual edge clocking scheme.

**RESPONSE TO REQUEST FOR ADMISSION NO. 405:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "attempted to amend pending patent applications, or file continuation or divisional applications, to add claims" and the terms "dual edge clocking scheme," "synchronously," "the rising and falling edge," "external clock," and "non-compatible DRAM device." Rambus further objects to the request as compound. Rambus further objects that the request calls for a legal conclusion. Rambus further objects to this request on the grounds that Rambus is not familiar, and cannot through reasonable inquiry become familiar, with the operation of all non-compatible DRAM devices. Rambus further objects that whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the

doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at one or more times between December 1991 and June 1996, Rambus amended its pending U.S. patent applications, filed continuation applications, and filed divisional applications. Rambus is not presently aware of any non-compatible devices that would infringe claims that were amended in or added to its U.S. Patent applications between December 1991 and June 1996 if such claims were included in an issued patent, with the exception of MDRAM devices designed by MoSys. By preliminary amendment dated September 6, 1994, Rambus properly added claims in its patent application with serial number 08/222,646 that were fully supported by the specification and that Rambus intended would read on MoSys MDRAM. *See, e.g., Kingsdown Medical Consultants, Ltd. v. Hollister, Inc.*, 863 F.2d 867, 874 (Fed. Cir. 1988), *cert. denied*, 490 U.S. 1067 (1989) ("nor is it in any manner improper to amend or insert claims intended to cover a competitor's product the applicant's attorney has learned about during the prosecution of a patent application"). After the application issued as U.S. Patent No. 5,513,327 and the MoSys device was closely examined, Rambus informed MoSys of Rambus's belief that MoSys was infringing the patent. The parties settled their dispute and no infringement ruling was ultimately obtained.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 406:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus had claims in pending patent applications that, if included in an issued patent, would cover on-chip PLL or on-chip DLL circuitry in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 406:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least

with respect to the terms "believed," "on-chip PLL" "on-chip DLL" "cover," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus had any claims in pending patent applications that, if included in an issued patent, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 407:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus could amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would cover on-chip PLL or on-chip DLL circuitry in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 407:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "could amend its pending patent applications, or file continuation or divisional applications, to add claims," and the terms "believed," "on-chip PLL" "on-chip DLL" "cover," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus could amend its

pending patent applications or file continuation or divisional applications to add valid claims that, if included in an issued patent application, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 408:**

Admit that, at various times between December 1991 and June 1996, Rambus attempted to amend pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would cover on-chip PLL or on-chip DLL circuitry in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 408:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "attempted to amend pending patent applications, or file continuation or divisional applications, to add claims" and the terms "on-chip PLL" "on-chip DLL" "cover," and "non-compatible DRAM device." Rambus further objects to the request as compound. Rambus further objects that the request calls for a legal conclusion. Rambus further objects to this request on the grounds that Rambus is not familiar, and cannot through reasonable inquiry become familiar, with the operation of all non-compatible DRAM devices. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at one or more times between December 1991 and June 1996, Rambus amended its pending U.S. patent applications, filed continuation applications, and filed divisional applications. Rambus is not presently aware of any non-compatible devices that would infringe claims that were amended in or added to its U.S. Patent applications between December 1991 and June 1996 if such claims were included in an issued patent, with the exception of MDRAM devices designed by MoSys. By preliminary amendment dated September 6, 1994, Rambus properly added claims in its patent application with serial number 08/222,646 that were fully supported by the specification and that Rambus intended would read on MoSys MDRAM. *See*, *e.g.*, *Kingsdown Medical Consultants, Ltd. v. Hollister, Inc.*, 863 F.2d 867, 874 (Fed. Cir. 1988), *cert. denied*, 490 U.S. 1067 (1989) ("nor is it in any manner improper to amend or insert claims intended to cover a competitor's product the applicant's attorney has learned about during the prosecution of a patent application"). After the application issued as U.S. Patent No. 5,513,327 and the MoSys device was closely examined, Rambus informed MoSys of Rambus's belief that MoSys was infringing the patent. The parties settled their dispute and no infringement ruling was ultimately obtained.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 409:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus had claims in pending patent applications that, if included in an issued patent, would cover phase locked loop circuitry or delay locked loop circuitry to generate an internal clock signal using an external clock signal in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 409:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "believed," "phase locked loop circuitry" "delay locked loop circuitry,"

"generate an internal clock signal using an external clock signal," "cover," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus had any claims in pending patent applications that, if included in an issued patent, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 410:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus could amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would cover phase locked loop circuitry or delay locked loop circuitry to generate an internal clock signal using an external clock signal in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 410:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "could amend its pending patent applications, or file continuation or divisional applications, to add claims," and the terms "believed," "phase locked loop circuitry" "delay locked loop circuitry," "generate an internal clock signal using an external clock signal," "cover," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned

and considered belief, between December 1991 and June 1996, that Rambus could amend its pending patent applications or file continuation or divisional applications to add valid claims that, if included in an issued patent application, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 411:**

Admit that, at various times between December 1991 and June 1996, Rambus attempted to amend pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would cover phase locked loop circuitry or delay locked loop circuitry to generate an internal clock signal using an external clock signal in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 411:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "attempted to amend pending patent applications, or file continuation or divisional applications, to add claims" and the terms "phase locked loop circuitry" "delay locked loop circuitry," "generate an internal clock signal using an external clock signal," "cover," and "non-compatible DRAM device." Rambus further objects to the request as compound. Rambus further objects that the request calls for a legal conclusion. Rambus further objects to this request on the grounds that Rambus is not familiar, and cannot through reasonable inquiry become familiar, with the operation of all non-compatible DRAM devices. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the

DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at one or more times between December 1991 and June 1996, Rambus amended its pending U.S. patent applications, filed continuation applications, and filed divisional applications. Rambus is not presently aware of any non-compatible devices that would infringe claims that were amended in or added to its U.S. Patent applications between December 1991 and June 1996 if such claims were included in an issued patent, with the exception of MDRAM devices designed by MoSys. By preliminary amendment dated September 6, 1994, Rambus properly added claims in its patent application with serial number 08/222,646 that were fully supported by the specification and that Rambus intended would read on MoSys MDRAM. *See, e.g.*, *Kingsdown Medical Consultants, Ltd. v. Hollister, Inc.*, 863 F.2d 867, 874 (Fed. Cir. 1988), *cert. denied*, 490 U.S. 1067 (1989) ("nor is it in any manner improper to amend or insert claims intended to cover a competitor's product the applicant's attorney has learned about during the prosecution of a patent application"). After the application issued as U.S. Patent No. 5,513,327 and the MoSys device was closely examined, Rambus informed MoSys of Rambus's belief that MoSys was infringing the patent. The parties settled their dispute and no infringement ruling was ultimately obtained.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 412:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus had claims in pending patent applications that, if included in an issued patent, would cover phase locked loop circuitry or delay locked loop circuitry to generate an internal clock signal using an external clock signal in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 412:**

Rambus objects to this request as duplicative of Request No. 409, and incorporates its objections and response thereto.

**REQUEST FOR ADMISSION NO. 413:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus could amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would cover phase locked loop circuitry or delay locked loop circuitry to generate an internal clock signal using an external clock signal in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 413:**

Rambus objects to this request as duplicative of Request No. 410, and incorporates its objections and response thereto.

**REQUEST FOR ADMISSION NO. 414:**

Admit that, at various times between December 1991 and June 1996, Rambus attempted to amend pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would cover phase locked loop circuitry or delay locked loop circuitry to generate an internal clock signal using an external clock signal in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 414:**

Rambus objects to this request as duplicative or Request No. 411, and incorporates its objections and response thereto.

**REQUEST FOR ADMISSION NO. 415:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus had claims in pending patent

applications that, if included in an issued patent, would cover having a phase lock loop on DRAM to control delays inside and outside a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 415:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "believed," "phase lock loop" "on DRAM," "to control delays inside and outside," "cover," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus had any claims in pending patent applications that, if included in an issued patent, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 416:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus could amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would cover having a phase lock loop on DRAM to control delays inside and outside a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 416:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "could amend its pending patent applications, or file continuation or divisional applications, to add claims," and the terms "believed," "phase lock loop" "on

DRAM," "to control delays inside and outside," "cover," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus could amend its pending patent applications or file continuation or divisional applications to add valid claims that, if included in an issued patent application, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 417:**

Admit that, at various times between December 1991 and June 1996, Rambus attempted to amend pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would cover having a phase lock loop on DRAM to control delays inside and outside a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 417:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "attempted to amend pending patent applications, or file continuation or divisional applications, to add claims" and the terms "phase lock loop" "on DRAM," "to control delays inside and outside," "cover," and "non-compatible DRAM device." Rambus further objects to the request as compound. Rambus further objects that the request calls for a legal conclusion. Rambus further objects to this request on the grounds that Rambus is not familiar, and cannot through reasonable inquiry become familiar, with the operation of all non-compatible DRAM devices. Rambus further objects that, to the extent that "cover" is to be

interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at one or more times between December 1991 and June 1996, Rambus amended its pending U.S. patent applications, filed continuation applications, and filed divisional applications. Rambus is not presently aware of any non-compatible devices that would infringe claims that were amended in or added to its U.S. Patent applications between December 1991 and June 1996 if such claims were included in an issued patent, with the exception of MDRAM devices designed by MoSys. By preliminary amendment dated September 6, 1994, Rambus properly added claims in its patent application with serial number 08/222,646 that were fully supported by the specification and that Rambus intended would read on MoSys MDRAM. *See, e.g.*, *Kingsdown Medical Consultants, Ltd. v. Hollister, Inc.*, 863 F.2d 867, 874 (Fed. Cir. 1988), *cert. denied*, 490 U.S. 1067 (1989) ("nor is it in any manner improper to amend or insert claims intended to cover a competitor's product the applicant's attorney has learned about during the prosecution of a patent application"). After the application issued as U.S. Patent No. 5,513,327 and the MoSys device was closely examined, Rambus informed MoSys of Rambus's belief that MoSys was infringing the patent. The parties settled their dispute and no infringement ruling was ultimately obtained.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 418:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus had claims in pending patent applications that, if included in an issued patent, would cover using a PLL/DLL circuit on a

DRAM to reduce input buffer skews in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 418:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "believed," "PLL/DLL circuit," "to reduce input buffer skews," "cover," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus had any claims in pending patent applications that, if included in an issued patent, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 419:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus could amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would cover using a PLL/DLL circuit on a DRAM to reduce input buffer skews in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 419:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "could amend its pending patent applications, or file continuation or divisional applications, to add claims," and the terms "believed," "PLL/DLL circuit," "to reduce input buffer skews," "cover," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus could amend its pending patent applications or file continuation or divisional applications to add valid claims that, if included in an issued patent application, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 420:**

Admit that, at various times between December 1991 and June 1996, Rambus attempted to amend pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would cover using a PLL/DLL circuit on a DRAM to reduce input buffer skews in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 420:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "attempted to amend pending patent applications, or file continuation or divisional applications, to add claims" and the terms "PLL/DLL circuit," "to reduce input buffer skews," "cover," and "non-compatible DRAM device." Rambus further objects to the request as compound. Rambus further objects that the request calls for a legal conclusion. Rambus further objects to this request on the grounds that Rambus is not familiar, and cannot through reasonable inquiry become familiar, with the operation of all non-compatible DRAM devices. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend

on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at one or more times between December 1991 and June 1996, Rambus amended its pending U.S. patent applications, filed continuation applications, and filed divisional applications. Rambus is not presently aware of any non-compatible devices that would infringe claims that were amended in or added to its U.S. Patent applications between December 1991 and June 1996 if such claims were included in an issued patent, with the exception of MDRAM devices designed by MoSys. By preliminary amendment dated September 6, 1994, Rambus properly added claims in its patent application with serial number 08/222,646 that were fully supported by the specification and that Rambus intended would read on MoSys MDRAM. *See, e.g.*, *Kingsdown Medical Consultants, Ltd. v. Hollister, Inc.*, 863 F.2d 867, 874 (Fed. Cir. 1988), *cert. denied*, 490 U.S. 1067 (1989) ("nor is it in any manner improper to amend or insert claims intended to cover a competitor's product the applicant's attorney has learned about during the prosecution of a patent application"). After the application issued as U.S. Patent No. 5,513,327 and the MoSys device was closely examined, Rambus informed MoSys of Rambus's belief that MoSys was infringing the patent. The parties settled their dispute and no infringement ruling was ultimately obtained.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 421:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus had claims in pending patent applications that, if included in an issued patent, would cover a DRAM with PLL clock generation in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 421:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "believed," "PLL clock generation," "cover," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus had any claims in pending patent applications that, if included in an issued patent, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 422:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus could amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would cover a DRAM with PLL clock generation in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 422:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "could amend its pending patent applications, or file continuation or divisional applications, to add claims," and the terms "believed," "PLL clock generation," "cover," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus could amend its pending patent applications or file continuation or divisional applications to add valid claims that, if included in an issued patent application, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 423:**

Admit that, at various times between December 1991 and June 1996, Rambus attempted to amend pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would cover a DRAM with PLL clock generation in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 423:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "attempted to amend pending patent applications, or file continuation or divisional applications, to add claims" and the terms "PLL clock generation," "cover," and "non-compatible DRAM device." Rambus further objects to the request as compound. Rambus further objects that the request calls for a legal conclusion. Rambus further objects to this request on the grounds that Rambus is not familiar, and cannot through reasonable inquiry become familiar, with the operation of all non-compatible DRAM devices. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the

doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at one or more times between December 1991 and June 1996, Rambus amended its pending U.S. patent applications, filed continuation applications, and filed divisional applications. Rambus is not presently aware of any non-compatible devices that would infringe claims that were amended in or added to its U.S. Patent applications between December 1991 and June 1996 if such claims were included in an issued patent, with the exception of MDRAM devices designed by MoSys. By preliminary amendment dated September 6, 1994, Rambus properly added claims in its patent application with serial number 08/222,646 that were fully supported by the specification and that Rambus intended would read on MoSys MDRAM. *See, e.g., Kingsdown Medical Consultants, Ltd. v. Hollister, Inc.*, 863 F.2d 867, 874 (Fed. Cir. 1988), *cert. denied*, 490 U.S. 1067 (1989) ("nor is it in any manner improper to amend or insert claims intended to cover a competitor's product the applicant's attorney has learned about during the prosecution of a patent application"). After the application issued as U.S. Patent No. 5,513,327 and the MoSys device was closely examined, Rambus informed MoSys of Rambus's belief that MoSys was infringing the patent. The parties settled their dispute and no infringement ruling was ultimately obtained.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 424:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus had claims in pending patent applications that, if included in an issued patent, would cover using a PLL on an SDRAM in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 424:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least

with respect to the terms "believed," "PLL," "SDRAM," "cover," and "non-compatible DRAM device." Rambus further objects that the request is unintelligible in its use of the phrase "PLL on an SDRAM in a non-compatible DRAM device."

**REQUEST FOR ADMISSION NO. 425:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus could amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would cover using a PLL on an SDRAM in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 425:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "could amend its pending patent applications, or file continuation or divisional applications, to add claims," and the terms "believed," "PLL," "SDRAM," "cover," and "non-compatible DRAM device." Rambus further objects that the request is unintelligible in its use of the phrase "PLL on an SDRAM in a non-compatible DRAM device."

**REQUEST FOR ADMISSION NO. 426:**

Admit that, at various times between December 1991 and June 1996, Rambus attempted to amend pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would cover using a PLL on an SDRAM in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 426:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "attempted to amend pending patent applications, or file continuation or divisional applications, to add claims" and the terms "PLL," "SDRAM," "cover," and "non-compatible DRAM device." Rambus further objects that the request is unintelligible in its use of the phrase "PLL on an SDRAM in a non-compatible DRAM device."

**REQUEST FOR ADMISSION NO. 427:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus had claims in pending patent applications that, if included in an issued patent, would cover using a DLL to compensate for the output delay in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 427:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "believed," "DLL," "to compensate for the output delay," "cover," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus had any claims in pending patent applications that, if included in an issued patent, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 428:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus could amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would cover using a DLL to compensate for the output delay in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 428:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "could amend its pending patent applications, or file continuation or divisional applications, to add claims," and the terms "believed," "DLL," "to compensate for the output delay," "cover," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus could amend its pending patent applications or file continuation or divisional applications to add valid claims that, if included in an issued patent application, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 429:**

Admit that, at various times between December 1991 and June 1996, Rambus attempted to amend pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would cover using a DLL to compensate for the output delay in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 429:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "attempted to amend pending patent applications, or file continuation or divisional applications, to add claims" and the terms "DLL," "to compensate for the output delay," "cover," and "non-compatible DRAM device." Rambus further objects to the request as

compound. Rambus further objects that the request calls for a legal conclusion. Rambus further objects to this request on the grounds that Rambus is not familiar, and cannot through reasonable inquiry become familiar, with the operation of all non-compatible DRAM devices. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at one or more times between December 1991 and June 1996, Rambus amended its pending U.S. patent applications, filed continuation applications, and filed divisional applications. Rambus is not presently aware of any non-compatible devices that would infringe claims that were amended in or added to its U.S. Patent applications between December 1991 and June 1996 if such claims were included in an issued patent, with the exception of MDRAM devices designed by MoSys. By preliminary amendment dated September 6, 1994, Rambus properly added claims in its patent application with serial number 08/222,646 that were fully supported by the specification and that Rambus intended would read on MoSys MDRAM. *See, e.g., Kingsdown Medical Consultants, Ltd. v. Hollister, Inc.*, 863 F.2d 867, 874 (Fed. Cir. 1988), *cert. denied*, 490 U.S. 1067 (1989) ("nor is it in any manner improper to amend or insert claims intended to cover a competitor's product the applicant's attorney has learned about during the prosecution of a patent application"). After the application issued as U.S. Patent No. 5,513,327 and the MoSys device was closely examined, Rambus informed MoSys of Rambus's belief that MoSys was infringing the patent. The parties settled their dispute and no infringement ruling was ultimately obtained.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 430:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus had claims in pending patent applications that, if included in an issued patent, would cover the use of a PLL or a DLL in a non-compatible DRAM device to ensure that the data strobe and data coming off of a DRAM chip are sufficiently synchronized to the system clock so that the memory controller can capture that data.

**RESPONSE TO REQUEST FOR ADMISSION NO. 430:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "believed," "PLL" "DLL," "data strobe," "sufficiently synchronized," "the memory controller," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus had any claims in pending patent applications that, if included in an issued patent, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 431:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus could amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would cover the use of a PLL or a DLL in a non-compatible DRAM device to

ensure that the data strobe and data coming off of a DRAM chip are sufficiently synchronized to the system clock so that the memory controller can capture that data.

**RESPONSE TO REQUEST FOR ADMISSION NO. 431:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "could amend its pending patent applications, or file continuation or divisional applications, to add claims," and the terms "believed," "PLL" "DLL," "data strobe," "sufficiently synchronized," "the memory controller," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus could amend its pending patent applications or file continuation or divisional applications to add valid claims that, if included in an issued patent application, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 432:**

Admit that, at various times between December 1991 and June 1996, Rambus attempted to amend pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would cover the use of a PLL or a DLL in a non-compatible DRAM device to ensure that the data strobe and data coming off of a DRAM chip are sufficiently synchronized to the system clock so that the memory controller can capture that data.

**RESPONSE TO REQUEST FOR ADMISSION NO. 432:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "attempted to amend pending patent applications, or file continuation or divisional applications, to add claims" and the terms "PLL" "DLL," "data strobe," "sufficiently synchronized," "the memory controller," and "non-compatible DRAM device." Rambus further objects to the request as compound. Rambus further objects that the request calls for a legal conclusion. Rambus further objects to this request on the grounds that Rambus is not familiar, and cannot through reasonable inquiry become familiar, with the operation of all non-compatible DRAM devices. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at one or more times between December 1991 and June 1996, Rambus amended its pending U.S. patent applications, filed continuation applications, and filed divisional applications. Rambus is not presently aware of any non-compatible devices that would infringe claims that were amended in or added to its U.S. Patent applications between December 1991 and June 1996 if such claims were included in an issued patent, with the exception of MDRAM devices designed by MoSys. By preliminary amendment dated September 6, 1994, Rambus properly added claims in its patent application with serial number 08/222,646 that were fully supported by the specification and that Rambus intended would read on MoSys MDRAM. *See, e.g., Kingsdown Medical Consultants, Ltd. v. Hollister, Inc.*, 863 F.2d 867, 874 (Fed. Cir. 1988), *cert. denied*, 490 U.S. 1067 (1989) ("nor is it in any manner improper to amend or insert claims intended to cover a competitor's product the applicant's attorney has learned about during the prosecution of a patent application"). After the application issued as

U.S. Patent No. 5,513,327 and the MoSys device was closely examined, Rambus informed MoSys of Rambus's belief that MoSys was infringing the patent. The parties settled their dispute and no infringement ruling was ultimately obtained.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 433:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus had claims in pending patent applications that, if included in an issued patent, would be infringed by a non-compatible DRAM device with on-chip PLL or on-chip DLL circuitry.

**RESPONSE TO REQUEST FOR ADMISSION NO. 433:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "believed," "on-chip PLL," "on-chip DLL," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus had any claims in pending patent applications that, if included in an issued patent, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 434:**

Admit that, at various times between December 1991 and June 1996, various directors,

officers or employees of Rambus believed that Rambus could amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would be infringed by a non-compatible DRAM device with on-chip PLL or on-chip DLL circuitry.

**RESPONSE TO REQUEST FOR ADMISSION NO. 434:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "could amend its pending patent applications, or file continuation or divisional applications, to add claims," and the terms "believed," "on-chip PLL," "on-chip DLL," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus could amend its pending patent applications or file continuation or divisional applications to add valid claims that, if included in an issued patent application, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 435:**

Admit that, at various times between December 1991 and June 1996, Rambus attempted to amend pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would be infringed by a non-compatible DRAM device with on-chip PLL or on-chip DLL circuitry.

**RESPONSE TO REQUEST FOR ADMISSION NO. 435:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "attempted to amend pending patent applications, or file continuation or divisional applications, to add claims" and the terms "on-chip PLL," "on-chip DLL," and "non-compatible DRAM device." Rambus further objects to the request as compound. Rambus further objects that the request calls for a legal conclusion. Rambus further objects to this request on the grounds that Rambus is not familiar, and cannot through reasonable inquiry become familiar, with the operation of all non-compatible DRAM devices. Rambus further objects that whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at one or more times between December 1991 and June 1996, Rambus amended its pending U.S. patent applications, filed continuation applications, and filed divisional applications. Rambus is not presently aware of any non-compatible devices that would infringe claims that were amended in or added to its U.S. Patent applications between December 1991 and June 1996 if such claims were included in an issued patent, with the exception of MDRAM devices designed by MoSys. By preliminary amendment dated September 6, 1994, Rambus properly added claims in its patent application with serial number 08/222,646 that were fully supported by the specification and that Rambus intended would read on MoSys MDRAM. *See, e.g.*, *Kingsdown Medical Consultants, Ltd. v. Hollister, Inc.*, 863 F.2d 867, 874 (Fed. Cir. 1988), *cert. denied*, 490 U.S. 1067 (1989) ("nor is it in any manner improper to amend or insert claims intended to cover a competitor's product the applicant's attorney has learned about during the prosecution of a patent application"). After the application issued as U.S. Patent No. 5,513,327 and the MoSys device was closely examined, Rambus informed MoSys of Rambus's belief that MoSys was infringing the patent. The parties settled their

dispute and no infringement ruling was ultimately obtained.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 436:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus had claims in pending patent applications that, if included in an issued patent, would be infringed by a non-compatible DRAM device with phase locked loop circuitry or delay locked loop circuitry to generate an internal clock signal using an external clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 436:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "believed," "phase locked loop circuitry," "delay locked loop circuitry," "to generate an internal clock signal using an external clock signal," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus had any claims in pending patent applications that, if included in an issued patent, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 437:**

Admit that, at various times between December 1991 and June 1996, various directors,

officers or employees of Rambus believed that Rambus could amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would be infringed by a non-compatible DRAM device with phase locked loop circuitry or delay locked loop circuitry to generate an internal clock signal using an external clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 437:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "could amend its pending patent applications, or file continuation or divisional applications, to add claims," and the terms "believed," "phase locked loop circuitry," "delay locked loop circuitry," "to generate an internal clock signal using an external clock signal," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus could amend its pending patent applications or file continuation or divisional applications to add valid claims that, if included in an issued patent application, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 438:**

Admit that, at various times between December 1991 and June 1996, Rambus attempted to amend pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would be infringed by a non-compatible DRAM

device with phase locked loop circuitry or delay locked loop circuitry to generate an internal clock signal using an external clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 438:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "attempted to amend pending patent applications, or file continuation or divisional applications, to add claims" and the terms "phase locked loop circuitry," "delay locked loop circuitry," "to generate an internal clock signal using an external clock signal," and "non-compatible DRAM device." Rambus further objects to the request as compound. Rambus further objects that the request calls for a legal conclusion. Rambus further objects to this request on the grounds that Rambus is not familiar, and cannot through reasonable inquiry become familiar, with the operation of all non-compatible DRAM devices. Rambus further objects that whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at one or more times between December 1991 and June 1996, Rambus amended its pending U.S. patent applications, filed continuation applications, and filed divisional applications. Rambus is not presently aware of any non-compatible devices that would infringe claims that were amended in or added to its U.S. Patent applications between December 1991 and June 1996 if such claims were included in an issued patent, with the exception of MDRAM devices designed by MoSys. By preliminary amendment dated September 6, 1994, Rambus properly added claims in its patent application with serial number 08/222,646 that were fully supported by the specification and that Rambus intended would read on MoSys MDRAM. *See, e.g., Kingsdown Medical Consultants, Ltd. v. Hollister, Inc.*, 863 F.2d 867, 874 (Fed. Cir. 1988), *cert. denied*, 490 U.S. 1067 (1989) ("nor is it in any manner improper to amend or insert claims intended to cover a competitor's product the applicant's attorney has

learned about during the prosecution of a patent application"). After the application issued as U.S. Patent No. 5,513,327 and the MoSys device was closely examined, Rambus informed MoSys of Rambus's belief that MoSys was infringing the patent. The parties settled their dispute and no infringement ruling was ultimately obtained.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 439:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus had claims in pending patent applications that, if included in an issued patent, would be infringed by a non-compatible DRAM device with phase locked loop circuitry or delay locked loop circuitry to generate an internal clock signal using an external clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 439:**

Rambus objects to this request as duplicative of Request No. 436, and incorporates its objections and response thereto.

**REQUEST FOR ADMISSION NO. 440:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus could amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would be infringed by a non-compatible DRAM device with phase locked loop circuitry or delay locked loop circuitry to generate an internal clock signal using an external clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 440:**

Rambus objects to this request as duplicative of Request No. 437, and incorporates its objections and response thereto.

**REQUEST FOR ADMISSION NO. 441:**

Admit that, at various times between December 1991 and June 1996, Rambus attempted to amend pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would be infringed by a non-compatible DRAM device with phase locked loop circuitry or delay locked loop circuitry to generate an internal clock signal using an external clock signal.

**RESPONSE TO REQUEST FOR ADMISSION NO. 441:**

Rambus objects to this request as duplicative of Request No. 438, and incorporates its objections and response thereto.

**REQUEST FOR ADMISSION NO. 442:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus had claims in pending patent applications that, if included in an issued patent, would be infringed by a non-compatible DRAM device with a phase lock loop on DRAM to control delays inside and outside the DRAM.

**RESPONSE TO REQUEST FOR ADMISSION NO. 442:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "believed," "phase lock loop," "on DRAM," "to control delays inside and outside," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus had any claims in pending patent applications that, if included in an issued patent, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated

September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 443:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus could amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would be infringed by a non-compatible DRAM device with a phase lock loop on DRAM to control delays inside and outside the DRAM.

**RESPONSE TO REQUEST FOR ADMISSION NO. 443:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "could amend its pending patent applications, or file continuation or divisional applications, to add claims," and the terms "believed," "phase lock loop," "on DRAM," "to control delays inside and outside," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus could amend its pending patent applications or file continuation or divisional applications to add valid claims that, if included in an issued patent application, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 444:**

Admit that, at various times between December 1991 and June 1996, Rambus attempted to amend pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would be infringed by a non-compatible DRAM device with a phase lock loop on DRAM to control delays inside and outside the DRAM.

**RESPONSE TO REQUEST FOR ADMISSION NO. 444:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "attempted to amend pending patent applications, or file continuation or divisional applications, to add claims" and the terms "phase lock loop," "on DRAM," "to control delays inside and outside," and "non-compatible DRAM device." Rambus further objects to the request as compound. Rambus further objects that the request calls for a legal conclusion. Rambus further objects to this request on the grounds that Rambus is not familiar, and cannot through reasonable inquiry become familiar, with the operation of all non-compatible DRAM devices. Rambus further objects that whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at one or more times between December 1991 and June 1996, Rambus amended its pending U.S. patent applications, filed continuation applications, and filed divisional applications. Rambus is not presently aware of any non-compatible devices that would infringe claims that were amended in or added to its U.S. Patent applications between December 1991 and June 1996 if such claims were included in an issued patent, with the exception of MDRAM devices designed by MoSys. By preliminary amendment dated September 6, 1994, Rambus properly added claims in its patent application with serial number 08/222,646 that were fully supported by the specification and that Rambus intended would read

on MoSys MDRAM. *See, e.g.*, *Kingsdown Medical Consultants, Ltd. v. Hollister, Inc.*, 863 F.2d 867, 874 (Fed. Cir. 1988), *cert. denied*, 490 U.S. 1067 (1989) ("nor is it in any manner improper to amend or insert claims intended to cover a competitor's product the applicant's attorney has learned about during the prosecution of a patent application"). After the application issued as U.S. Patent No. 5,513,327 and the MoSys device was closely examined, Rambus informed MoSys of Rambus's belief that MoSys was infringing the patent. The parties settled their dispute and no infringement ruling was ultimately obtained.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 445:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus had claims in pending patent applications that, if included in an issued patent, would be infringed by a non-compatible DRAM device with a PLL/DLL circuit on the DRAM to reduce input buffer skews.

**RESPONSE TO REQUEST FOR ADMISSION NO. 445:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "believed," "PLL/DLL circuit," "to reduce input buffer skews," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus had any claims in pending patent applications that, if included in an issued patent, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 446:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus could amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would be infringed by a non-compatible DRAM device with a PLL/DLL circuit on the DRAM to reduce input buffer skews.

**RESPONSE TO REQUEST FOR ADMISSION NO. 446:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "could amend its pending patent applications, or file continuation or divisional applications, to add claims," and the terms "believed," "PLL/DLL circuit," "to reduce input buffer skews," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus could amend its pending patent applications or file continuation or divisional applications to add valid claims that, if included in an issued patent application, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 447:**

Admit that, at various times between December 1991 and June 1996, Rambus attempted

to amend pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would be infringed by a non-compatible DRAM device with a PLL/DLL circuit on a DRAM to reduce input buffer skews.

**RESPONSE TO REQUEST FOR ADMISSION NO. 447:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "attempted to amend pending patent applications, or file continuation or divisional applications, to add claims" and the terms "PLL/DLL circuit," "to reduce input buffer skews," and "non-compatible DRAM device." Rambus further objects to the request as compound. Rambus further objects that the request calls for a legal conclusion. Rambus further objects to this request on the grounds that Rambus is not familiar, and cannot through reasonable inquiry become familiar, with the operation of all non-compatible DRAM devices. Rambus further objects that whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at one or more times between December 1991 and June 1996, Rambus amended its pending U.S. patent applications, filed continuation applications, and filed divisional applications. Rambus is not presently aware of any non-compatible devices that would infringe claims that were amended in or added to its U.S. Patent applications between December 1991 and June 1996 if such claims were included in an issued patent, with the exception of MDRAM devices designed by MoSys. By preliminary amendment dated September 6, 1994, Rambus properly added claims in its patent application with serial number 08/222,646 that were fully supported by the specification and that Rambus intended would read on MoSys MDRAM. *See, e.g., Kingsdown Medical Consultants, Ltd. v. Hollister, Inc.*, 863 F.2d 867, 874 (Fed. Cir. 1988), *cert. denied*, 490 U.S. 1067 (1989) ("nor is it in any manner improper to amend or insert claims intended to cover a competitor's product the applicant's attorney has

learned about during the prosecution of a patent application"). After the application issued as U.S. Patent No. 5,513,327 and the MoSys device was closely examined, Rambus informed MoSys of Rambus's belief that MoSys was infringing the patent. The parties settled their dispute and no infringement ruling was ultimately obtained.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 448:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus had claims in pending patent applications that, if included in an issued patent, would be infringed by a non-compatible DRAM device with PLL clock generation.

**RESPONSE TO REQUEST FOR ADMISSION NO. 448:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "believed," "PLL clock generation" and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus had any claims in pending patent applications that, if included in an issued patent, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 449:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus could amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would be infringed by a non-compatible DRAM device with PLL clock generation.

**RESPONSE TO REQUEST FOR ADMISSION NO. 449:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "could amend its pending patent applications, or file continuation or divisional applications, to add claims," and the terms "believed," "PLL clock generation" and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus could amend its pending patent applications or file continuation or divisional applications to add valid claims that, if included in an issued patent application, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 450:**

Admit that, at various times between December 1991 and June 1996, Rambus attempted to amend pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would be infringed by a non-compatible DRAM

device with PLL clock generation.

**RESPONSE TO REQUEST FOR ADMISSION NO. 450:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "attempted to amend pending patent applications, or file continuation or divisional applications, to add claims" and the terms "PLL clock generation" and "non-compatible DRAM device." Rambus further objects to the request as compound. Rambus further objects that the request calls for a legal conclusion. Rambus further objects to this request on the grounds that Rambus is not familiar, and cannot through reasonable inquiry become familiar, with the operation of all non-compatible DRAM devices. Rambus further objects that whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at one or more times between December 1991 and June 1996, Rambus amended its pending U.S. patent applications, filed continuation applications, and filed divisional applications. Rambus is not presently aware of any non-compatible devices that would infringe claims that were amended in or added to its U.S. Patent applications between December 1991 and June 1996 if such claims were included in an issued patent, with the exception of MDRAM devices designed by MoSys. By preliminary amendment dated September 6, 1994, Rambus properly added claims in its patent application with serial number 08/222,646 that were fully supported by the specification and that Rambus intended would read on MoSys MDRAM. *See, e.g., Kingsdown Medical Consultants, Ltd. v. Hollister, Inc.*, 863 F.2d 867, 874 (Fed. Cir. 1988), *cert. denied*, 490 U.S. 1067 (1989) ("nor is it in any manner improper to amend or insert claims intended to cover a competitor's product the applicant's attorney has learned about during the prosecution of a patent application"). After the application issued as U.S. Patent No. 5,513,327 and the MoSys device was closely examined, Rambus informed

MoSys of Rambus's belief that MoSys was infringing the patent. The parties settled their dispute and no infringement ruling was ultimately obtained.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 451:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus had claims in pending patent applications that, if included in an issued patent, would be infringed by a non-compatible DRAM device using a PLL.

**RESPONSE TO REQUEST FOR ADMISSION NO. 451:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "believed," "using a PLL" and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus had any claims in pending patent applications that, if included in an issued patent, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 452:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus could amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an

issued patent, would be infringed by a non-compatible DRAM device using a PLL.

**RESPONSE TO REQUEST FOR ADMISSION NO. 452:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "could amend its pending patent applications, or file continuation or divisional applications, to add claims," and the terms "believed," "using a PLL" and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus could amend its pending patent applications or file continuation or divisional applications to add valid claims that, if included in an issued patent application, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 453:**

Admit that, at various times between December 1991 and June 1996, Rambus attempted to amend pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would be infringed by a non-compatible DRAM device using a PLL.

**RESPONSE TO REQUEST FOR ADMISSION NO. 453:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "attempted to amend pending patent applications, or file continuation or divisional applications, to add claims" and the terms "using a PLL" and "non-compatible

DRAM device." Rambus further objects to the request as compound. Rambus further objects that the request calls for a legal conclusion. Rambus further objects to this request on the grounds that Rambus is not familiar, and cannot through reasonable inquiry become familiar, with the operation of all non-compatible DRAM devices. Rambus further objects that whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at one or more times between December 1991 and June 1996, Rambus amended its pending U.S. patent applications, filed continuation applications, and filed divisional applications. Rambus is not presently aware of any non-compatible devices that would infringe claims that were amended in or added to its U.S. Patent applications between December 1991 and June 1996 if such claims were included in an issued patent, with the exception of MDRAM devices designed by MoSys. By preliminary amendment dated September 6, 1994, Rambus properly added claims in its patent application with serial number 08/222,646 that were fully supported by the specification and that Rambus intended would read on MoSys MDRAM. *See, e.g., Kingsdown Medical Consultants, Ltd. v. Hollister, Inc.*, 863 F.2d 867, 874 (Fed. Cir. 1988), *cert. denied*, 490 U.S. 1067 (1989) ("nor is it in any manner improper to amend or insert claims intended to cover a competitor's product the applicant's attorney has learned about during the prosecution of a patent application"). After the application issued as U.S. Patent No. 5,513,327 and the MoSys device was closely examined, Rambus informed MoSys of Rambus's belief that MoSys was infringing the patent. The parties settled their dispute and no infringement ruling was ultimately obtained.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 454:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus had claims in pending patent applications that, if included in an issued patent, would be infringed by a non-compatible DRAM device using a DLL to compensate for the output delay in a DRAM.

**RESPONSE TO REQUEST FOR ADMISSION NO. 454:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "believed," "DLL," "to compensate for the output delay in a DRAM," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus had any claims in pending patent applications that, if included in an issued patent, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 455:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus could amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would be infringed by a non-compatible DRAM device using a DLL to compensate for the output delay in a DRAM.

**RESPONSE TO REQUEST FOR ADMISSION NO. 455:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "could amend its pending patent applications, or file continuation or divisional applications, to add claims," and the terms "believed," "DLL," "to compensate for the output delay in a DRAM," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus could amend its pending patent applications or file continuation or divisional applications to add valid claims that, if included in an issued patent application, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 456:**

Admit that, at various times between December 1991 and June 1996, Rambus attempted to amend pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would be infringed by a non-compatible DRAM device using a DLL to compensate for the output delay in a DRAM.

**RESPONSE TO REQUEST FOR ADMISSION NO. 456:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "attempted to amend pending patent applications, or file continuation or divisional applications, to add claims" and the terms "DLL," "to compensate for the output delay in a DRAM," and "non-compatible DRAM device." Rambus further objects to the request

as compound. Rambus further objects that the request calls for a legal conclusion. Rambus further objects to this request on the grounds that Rambus is not familiar, and cannot through reasonable inquiry become familiar, with the operation of all non-compatible DRAM devices. Rambus further objects that whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at one or more times between December 1991 and June 1996, Rambus amended its pending U.S. patent applications, filed continuation applications, and filed divisional applications. Rambus is not presently aware of any non-compatible devices that would infringe claims that were amended in or added to its U.S. Patent applications between December 1991 and June 1996 if such claims were included in an issued patent, with the exception of MDRAM devices designed by MoSys. By preliminary amendment dated September 6, 1994, Rambus properly added claims in its patent application with serial number 08/222,646 that were fully supported by the specification and that Rambus intended would read on MoSys MDRAM. *See, e.g., Kingsdown Medical Consultants, Ltd. v. Hollister, Inc.*, 863 F.2d 867, 874 (Fed. Cir. 1988), *cert. denied*, 490 U.S. 1067 (1989) ("nor is it in any manner improper to amend or insert claims intended to cover a competitor's product the applicant's attorney has learned about during the prosecution of a patent application"). After the application issued as U.S. Patent No. 5,513,327 and the MoSys device was closely examined, Rambus informed MoSys of Rambus's belief that MoSys was infringing the patent. The parties settled their dispute and no infringement ruling was ultimately obtained.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 457:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus had claims in pending patent applications that, if included in an issued patent, would be infringed by a non-compatible DRAM device using an on-chip PLL or a DLL to ensure that the data strobe and data coming off of a DRAM chip are sufficiently synchronized to the system clock so that the memory controller can capture that data.

**RESPONSE TO REQUEST FOR ADMISSION NO. 457:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "believed," "on-chip PLL," "DLL," "data strobe," "sufficiently synchronized," "the memory controller," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus had any claims in pending patent applications that, if included in an issued patent, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 458:**

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus could amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would be infringed by a non-compatible DRAM device using an on-chip PLL or a

DLL to ensure that the data strobe and data coming off of a DRAM chip are sufficiently synchronized to the system clock so that the memory controller can capture that data.

**RESPONSE TO REQUEST FOR ADMISSION NO. 458:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "could amend its pending patent applications, or file continuation or divisional applications, to add claims," and the terms "believed," "on-chip PLL," "DLL," "data strobe," "sufficiently synchronized," "the memory controller," and "non-compatible DRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus could amend its pending patent applications or file continuation or divisional applications to add valid claims that, if included in an issued patent application, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 459:**

Admit that, at various times between December 1991 and June 1996, Rambus attempted to amend pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would be infringed by a non-compatible DRAM device using an on-chip PLL or a DLL to ensure that the data strobe and data coming off of a DRAM chip are sufficiently synchronized to the system clock so that the memory controller can capture that data.

**RESPONSE TO REQUEST FOR ADMISSION NO. 459:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "attempted to amend pending patent applications, or file continuation or divisional applications, to add claims" and the terms "on-chip PLL," "DLL," "data strobe," "sufficiently synchronized," "the memory controller," and "non-compatible DRAM device." Rambus further objects to the request as compound. Rambus further objects that the request calls for a legal conclusion. Rambus further objects to this request on the grounds that Rambus is not familiar, and cannot through reasonable inquiry become familiar, with the operation of all non-compatible DRAM devices. Rambus further objects that whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at one or more times between December 1991 and June 1996, Rambus amended its pending U.S. patent applications, filed continuation applications, and filed divisional applications. Rambus is not presently aware of any non-compatible devices that would infringe claims that were amended in or added to its U.S. Patent applications between December 1991 and June 1996 if such claims were included in an issued patent, with the exception of MDRAM devices designed by MoSys. By preliminary amendment dated September 6, 1994, Rambus properly added claims in its patent application with serial number 08/222,646 that were fully supported by the specification and that Rambus intended would read on MoSys MDRAM. *See, e.g., Kingsdown Medical Consultants, Ltd. v. Hollister, Inc.*, 863 F.2d 867, 874 (Fed. Cir. 1988), *cert. denied*, 490 U.S. 1067 (1989) ("nor is it in any manner improper to amend or insert claims intended to cover a competitor's product the applicant's attorney has learned about during the prosecution of a patent application"). After the application issued as U.S. Patent No. 5,513,327 and the MoSys device was closely examined, Rambus informed

MoSys of Rambus's belief that MoSys was infringing the patent. The parties settled their dispute and no infringement ruling was ultimately obtained.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 460:**

Admit that Rambus has one or more issued patents claiming a priority date before June 1996 containing claims that cover the use of programmable CAS latency in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 460:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "programmable CAS latency," "cover," and "non-compatible DRAM device." Rambus further objects that the request calls for a legal conclusion. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has asserted that claims of certain patents claiming a priority date before June 1996 are infringed by certain non-compatible DRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 461:**

Admit that Rambus has one or more pending patent applications containing claims that, if included in an issued patent, would cover the use of programmable CAS latency in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 461:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "programmable CAS latency," "cover," and "non-compatible DRAM device." Rambus further objects that the request calls for a legal conclusion. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 462:**

Admit that Rambus has alleged that JEDEC-compliant SDRAM devices using programmable CAS latency infringe one or more of its patents that claim a priority date before June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 462:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the term "programmable CAS latency."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain devices purporting to be JEDEC-compliant SDRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 463:**

Admit that Rambus has alleged that JEDEC-compliant DDR SDRAM devices using

programmable CAS latency infringe one or more of its patents that claim a priority date before June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 463:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the term "programmable CAS latency."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain devices purporting to be JEDEC-compliant DDR SDRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 464:**

Admit that Rambus has one or more issued patents containing claims that cover a non-compatible DRAM device containing a register to store a value to determine CAS latency, where that value can be changed by programming the mode register.

**RESPONSE TO REQUEST FOR ADMISSION NO. 464:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "to determine CAS latency," "programming," "mode register," "cover," and "non-compatible DRAM device." Rambus further objects that the request calls for a legal conclusion. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has asserted that claims of certain patents claiming a priority date before June 1996 are infringed by certain non-compatible DRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 465:**

Admit that Rambus has one or more pending patent applications containing claims that, if contained in an issued patent, would cover a non-compatible DRAM device containing a register to store a value to determine CAS latency, where that value can be changed by programming the mode register.

**RESPONSE TO REQUEST FOR ADMISSION NO. 465:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "to determine CAS latency," "programming," "mode register," "cover," and "non-compatible DRAM device." Rambus further objects that the request calls for a legal conclusion. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has a number of patent applications containing claims that, if contained in an issued patent, might be infringed by certain non-compatible DRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 466:**

Admit that Rambus has alleged that JEDEC-compliant SDRAM devices containing a register to store a value to determine CAS latency, where that value can be changed by programming the mode register, infringe one or more of its patents that claim a priority date before June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 466:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "to determine CAS latency," "programming," and "mode register,"

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain devices purporting to be JEDEC-compliant SDRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 467:**

Admit that Rambus has alleged that JEDEC-compliant DDR SDRAM devices containing a register to store a value to determine CAS latency, where that value can be changed by programming the mode register, infringe one or more of its patents that claim a priority date before June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 467:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "to determine CAS latency," "programming," and "mode register,"

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain devices purporting to be JEDEC-compliant DDR SDRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 468:**

Admit that Rambus has one or more issued patents containing claims that cover the use of a programmable register to store a value that is representative of a delay time after which the device responds to a read request in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 468:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "programmable register," "representative of a delay time," "responds to a read request," "cover," and "non-compatible DRAM device." Rambus further objects that the request calls for a legal conclusion. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has asserted that claims of certain patents claiming a priority date before June 1996 are infringed by certain non-compatible DRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 469:**

Admit that Rambus has one or more pending patent applications containing claims that, if included in an issued patent, would cover the use of a programmable register to store a value that is representative of a delay time after which the device responds to a read request in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 469:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "programmable register," "representative of a delay time," "responds to a read request," "cover," and "non-compatible DRAM device." Rambus further objects that the request calls for a legal conclusion. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of

the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 470:**

Admit that Rambus has alleged that JEDEC-compliant SDRAM devices that use a programmable register to store a value that is representative of a delay time after which the device responds to a read request infringe one or more of its patents that claim a priority date before June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 470:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "programmable register," "representative of a delay time," and "responds to a read request,"

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain devices purporting to be JEDEC-compliant SDRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 471:**

Admit that Rambus has alleged that JEDEC-compliant DDR SDRAM devices that use a programmable register to store a value that is representative of a delay time after which the device responds to a read request infringe one or more of its patents that claim a priority date before June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 471:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "programmable register," "representative of a delay time," and "responds to a read request."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain devices purporting to be JEDEC-compliant DDR SDRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 472:**

Admit that Rambus has one or more issued patents containing claims that would be infringed by a non-compatible DRAM device containing a programmable register to store a value which is representative of a delay time, that value being a number of clock cycles of an external clock, after which the SDRAM responds to a read request.

**RESPONSE TO REQUEST FOR ADMISSION NO. 472:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "programmable register," "representative of a delay time," "SDRAM," "responds to a read request," "cover," and "non-compatible DRAM device." Rambus further objects that the request calls for a legal conclusion. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has asserted that claims of certain patents claiming a priority date

before June 1996 are infringed by certain non-compatible DRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 473:**

Admit that Rambus has one or more pending patent applications containing claims that, if contained in an issued patent, would be infringed by a non-compatible DRAM device containing a programmable register to store a value which is representative of a delay time, that value being a number of clock cycles of an external clock, after which the SDRAM responds to a read request.

**RESPONSE TO REQUEST FOR ADMISSION NO. 473:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "programmable register," "representative of a delay time," "SDRAM," "responds to a read request," "cover," and "non-compatible DRAM device." Rambus further objects that the request calls for a legal conclusion. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has a number of patent applications containing claims that, if contained in an issued patent, might be infringed by certain non-compatible DRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 474:**

Admit that Rambus has alleged that JEDEC-compliant SDRAM devices that contain a programmable register to store a value which is representative of a delay time, that value being a

number of clock cycles of an external clock, after which the SDRAM responds to a read request, infringe one or more of its patents that claim a priority date before June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 474:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "programmable register," "representative of a delay time," "SDRAM," and "responds to a read request."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain devices purporting to be JEDEC-compliant SDRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 475:**

Admit that Rambus has alleged that JEDEC-compliant DDR SDRAM devices that contain a programmable register to store a value which is representative of a delay time, that value being a number of clock cycles of an external clock, after which the SDRAM responds to a read request, infringe one or more of its patents that claim a priority date before June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 475:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "programmable register," "representative of a delay time," "SDRAM," and "responds to a read request."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain devices purporting to be JEDEC-compliant SDRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 476:**

Admit that Rambus has one or more issued patents containing claims that would be infringed by a non-compatible DRAM device containing a programmable access-time register operative to store information specifying a value indicative of an access time for the device, such that the device waits for the access time before responding to a read request.

**RESPONSE TO REQUEST FOR ADMISSION NO. 476:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "programmable access-time register," "specifying a value indicative of an access time," "waits for the access time" "responding to a read request," "cover," and "non-compatible DRAM device." Rambus further objects that the request calls for a legal conclusion. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has asserted that claims of certain patents claiming a priority date before June 1996 are infringed by certain non-compatible DRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 477:**

Admit that Rambus has one or more pending patent applications containing claims that, if included in an issued patent, would be infringed by a non-compatible DRAM device containing a programmable access-time register operative to store information specifying a value indicative of an access time for the device, such that the device waits for the access time before responding to a read request.

**RESPONSE TO REQUEST FOR ADMISSION NO. 477:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "programmable access-time register," "specifying a value indicative of an access time," "waits for the access time" "responding to a read request," "cover," and "non-compatible DRAM device." Rambus further objects that the request calls for a legal conclusion. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has a number of patent applications containing claims that, if contained in an issued patent, might be infringed by certain non-compatible DRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 478:**

Admit that Rambus has alleged that JEDEC-compliant SDRAM devices that contain a programmable access-time register operative to store information specifying a value indicative of an access time for the device, such that the device waits for the access time before responding to a read request, infringe one or more of its patents that claim a priority date before June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 478:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "programmable access-time register," "specifying a value indicative of an access time," "waits for the access time" and "responding to a read request."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain devices purporting to be JEDEC-compliant

SDRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 479:**

Admit that Rambus has alleged that JEDEC-compliant DDR SDRAM devices that contain a programmable access-time register operative to store information specifying a value indicative of an access time for the device, such that the device waits for the access time before responding to a read request, infringe one or more of its patents that claim a priority date before June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 479:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "programmable access-time register," "specifying a value indicative of an access time," "waits for the access time" and "responding to a read request."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain devices purporting to be JEDEC-compliant DDR SDRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 480:**

Admit that Rambus has alleged that JEDEC-compliant SDRAM devices containing a programmable register that receives block size information that defines an amount of data to be output by the device in response to a read request infringe patents that it owns and that claim a priority date of April 18, 1990.

**RESPONSE TO REQUEST FOR ADMISSION NO. 480:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "programmable register," "block size information," "defines an amount

of data" and "in response to a read request."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date of April 18, 1990 are infringed by certain devices purporting to be JEDEC-compliant SDRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 481:**

Admit that Rambus owns patents claiming a priority date of April 18, 1990 that it believes covers the use of a programmable register that receives block size information that defines an amount of data to be output by the device in response to a read request in JEDEC-compliant SDRAM devices.

**RESPONSE TO REQUEST FOR ADMISSION NO. 481:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "believes," "covers," "programmable register," "block size information," "defines an amount of data" and "in response to a read request." Rambus further objects that the request calls for a legal conclusion. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 482:**

Admit that Rambus has one or more issued patents claiming a priority date before June

1996 containing claims that cover the use of a mode register in a non-compatible DRAM device to store a value to determine burst length, where that value can be changed by programming the mode register.

**RESPONSE TO REQUEST FOR ADMISSION NO. 482:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "cover", "mode register," "value to determine burst length," "programming," and "non-compatible DRAM device." Rambus further objects that the request calls for a legal conclusion. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain non-compatible DRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 483:**

Admit that Rambus has one or more pending patent applications containing claims that, if included in an issued patent, would cover the use of a mode register in a non-compatible DRAM device to store a value to determine burst length, where that value can be changed by programming the mode register.

**RESPONSE TO REQUEST FOR ADMISSION NO. 483:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "cover", "mode register," "value to determine burst length," "programming," and "non-compatible DRAM device." Rambus further objects that the request

calls for a legal conclusion. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 484:**

Admit that Rambus has alleged that JEDEC-compliant SDRAM devices using a mode register to store a value to determine burst length, where that value can be changed by programming the mode register, infringe one or more of its patents that claim a priority date before June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 484:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "mode register," "value to determine burst length" and "programming."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain devices purporting to be JEDEC-compliant SDRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 485:**

Admit that Rambus has alleged that JEDEC-compliant DDR SDRAM devices using a mode register to store a value to determine burst length, where that value can be changed by programming the mode register, infringe one or more of its patents that claim a priority date

before June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 485:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "mode register," "value to determine burst length" and "programming."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain devices purporting to be JEDEC-compliant DDR SDRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 486:**

Admit that Rambus has one or more issued patents claiming a priority date before June 1996 containing claims that cover the use of a mode register in a non-compatible DRAM device to store a value to determine block size, where that value can be changed by programming the mode register.

**RESPONSE TO REQUEST FOR ADMISSION NO. 486:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "mode register," "value to determine burst length," "programming," "cover," and "non-compatible DRAM device." Rambus further objects that the request calls for a legal conclusion. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has asserted that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain non-compatible DRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 487:**

Admit that Rambus has one or more pending patent applications containing claims that, if included in an issued patent, would cover the use of a mode register in a non-compatible DRAM device to store a value to determine block size, where that value can be changed by programming the mode register.

**RESPONSE TO REQUEST FOR ADMISSION NO. 487:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "mode register," "value to determine burst length," "programming." and "cover." Rambus further objects that the request calls for a legal conclusion. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 488:**

Admit that Rambus has alleged that JEDEC-compliant SDRAM devices using a mode register to store a value to determine block size, where that value can be changed by programming the mode register, infringe one or more of its patents that claim a priority date before June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 488:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "mode register," "value to determine block size" and "programming."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain devices purporting to be JEDEC-compliant SDRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 489:**

Admit that Rambus has alleged that JEDEC-compliant DDR SDRAM devices using a mode register to store a value to determine block size, where that value can be changed by programming the mode register, infringe one or more of its patents that claim a priority date before June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 489:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "mode register," "value to determine block size" and "programming."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain devices purporting to be JEDEC-compliant DDR SDRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 490:**

Admit that Rambus has one or more issued patents claiming a priority date before June 1996 containing claims that cover the use of a Mode Register in a non-compatible DRAM device that stores mode-of-operation data, including the Burst Length.

**RESPONSE TO REQUEST FOR ADMISSION NO. 490:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "Mode Register," "mode-of-operation data," "cover," and "non-

compatible DRAM device." Rambus further objects that the request calls for a legal conclusion. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has asserted that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain non-compatible DRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 491:**

Admit that Rambus has one or more pending patent applications containing claims that, if included in an issued patent, would cover the use a Mode Register in a non-compatible DRAM device that stores mode-of-operation data, including the Burst Length.

**RESPONSE TO REQUEST FOR ADMISSION NO. 491:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "Mode Register," "mode-of-operation data," "cover," and "non-compatible DRAM device." Rambus further objects that the request calls for a legal conclusion. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 492:**

Admit that Rambus has alleged that JEDEC-compliant SDRAM devices using a Mode Register that stores mode-of-operation data, including the Burst Length, infringe one or more of its patents that claim a priority date before June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 492:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "Mode Register" and "mode-of-operation data."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain devices purporting to be JEDEC-compliant SDRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 493:**

Admit that Rambus has alleged that JEDEC-compliant DDR SDRAM devices using a Mode Register that stores mode-of-operation data, including the Burst Length, infringe one or more of its patents that claim a priority date before June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 493:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "Mode Register" and "mode-of-operation data."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain devices purporting to be JEDEC-compliant DDR SDRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 494:**

Admit that Rambus has one or more issued patents claiming a priority date before June 1996 containing claims that cover the use of a Mode Register in a non-compatible DRAM device that can be changed to thereby change the operation of the chip.

**RESPONSE TO REQUEST FOR ADMISSION NO. 494:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "Mode Register," "changed," "operation of the chip," "cover," and "non-compatible DRAM device." Rambus further objects that the request calls for a legal conclusion. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has asserted that claims of certain patents claiming a priority date before June 1996 are infringed by certain non-compatible DRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 495:**

Admit that Rambus has one or more pending patent applications containing claims that, if included in an issued patent, would cover the use a Mode Register in a non-compatible DRAM device that can be changed to thereby change the operation of the chip.

**RESPONSE TO REQUEST FOR ADMISSION NO. 495:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "Mode Register," "changed," "operation of the chip," "cover," and "non-compatible DRAM device." Rambus further objects that the request calls for a legal conclusion. Rambus further objects that, to the extent that "cover" is to be interpreted as

"infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 496:**

Admit that Rambus has alleged that JEDEC-compliant SDRAM devices using a Mode Register that can be changed (and thereby change the operation of the chip) infringe one or more of its patents that claim a priority date before June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 496:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "Mode Register," "changed," and "operation of the chip."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain devices purporting to be JEDEC-compliant SDRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 497:**

Admit that Rambus has alleged that JEDEC-compliant DDR SDRAM devices using a Mode Register that can be changed (and thereby change the operation of the chip) infringe one or more of its patents that claim a priority date before June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 497:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "Mode Register," "changed," and "operation of the chip."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain devices purporting to be JEDEC-compliant DDR SDRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 498:**

Admit that Rambus has one or more issued patents claiming a priority date before June 1996 containing claims that cover the use of a programmable register to store a value that defines an amount of data to be output by the memory device in response to a read request in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 498:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "cover," "programmable register," "defines an amount of data," "response to a read request," and "non-compatible DRAM device." Rambus further objects that the request calls for a legal conclusion. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain non-compatible DRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 499:**

Admit that Rambus has one or more pending patent applications containing claims that, if included in an issued patent, would cover the use a programmable register to store a value that defines an amount of data to be output by the memory device in response to a read request in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 499:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "cover," "programmable register," "defines an amount of data," "response to a read request," and "non-compatible DRAM device." Rambus further objects that the request calls for a legal conclusion. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 500:**

Admit that Rambus has alleged that JEDEC-compliant SDRAM devices using a programmable register to store a value that defines an amount of data to be output by the memory device in response to a read request infringe one or more of its patents that claim a priority date before June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 500:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "programmable register," "defines an amount of data" and "response to a read request."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain devices purporting to be JEDEC-compliant SDRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 501:**

Admit that Rambus has alleged that JEDEC-compliant DDR SDRAM devices using a programmable register to store a value that defines an amount of data to be output by the memory device in response to a read request infringe one or more of its patents that claim a priority date before June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 501:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "programmable register," "defines an amount of data" and "response to a read request."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain devices purporting to be JEDEC-compliant DDR SDRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 502:**

Admit that Rambus has one or more issued patents claiming a priority date before June 1996 containing claims that would cover a programmable register that receives information that defines an amount of data to be output by the memory device in response to a read request in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 502:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "cover," "programmable register," "receives information," "defines an amount of data," "response to a read request," and "non-compatible DRAM device." Rambus further objects that the request calls for a legal conclusion. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain non-compatible DRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 503:**

Admit that Rambus has one or more pending patent applications containing claims that, if included in an issued patent, would cover the use a programmable register that receives information that defines an amount of data to be output by the memory device in response to a read request in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 503:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "cover," "programmable register," "receives information," "defines an amount of data," "response to a read request," and "non-compatible DRAM device." Rambus further objects that the request calls for a legal conclusion. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each

and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 504:**

Admit that Rambus has alleged that JEDEC-compliant SDRAM devices using a programmable register that receives information that defines an amount of data to be output by the memory device in response to a read request infringe one or more of its patents that claim a priority date before June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 504:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "programmable register," "receives information," "defines an amount of data" and "response to a read request."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain devices purporting to be JEDEC-compliant SDRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 505:**

Admit that Rambus has alleged that JEDEC-compliant DDR SDRAM devices using a programmable register that receives information that defines an amount of data to be output by the memory device in response to a read request infringe one or more of its patents that claim a priority date before June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 505:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "programmable register," "receives information," "defines an amount of data" and "response to a read request."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain devices purporting to be JEDEC-compliant DDR SDRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 506:**

Admit that Rambus has one or more issued patents claiming a priority date before June 1996 containing claims that would cover a programmable register operative to store information specifying a manner in which the semiconductor device is to respond to a read request or a write request in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 506:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "cover," "programmable register," "specifying a manner," "the semiconductor device," "respond to a read request," "respond to a . . . write request," and "non-compatible DRAM device." Rambus further objects that the request calls for a legal conclusion. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has asserted that claims of certain patents claiming a priority date

before June 1996 are infringed by certain non-compatible DRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 507:**

Admit that Rambus has one or more pending patent applications containing claims that, if included in an issued patent, would cover a programmable register operative to store information specifying a manner in which the semiconductor device is to respond to a read request or a write request in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 507:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "cover," "programmable register," "specifying a manner," "the semiconductor device," "respond to a read request," "respond to a . . . write request," and "non-compatible DRAM device." Rambus further objects that the request calls for a legal conclusion. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 508:**

Admit that Rambus has alleged that JEDEC-compliant SDRAM devices using a programmable register operative to store information specifying a manner in which the semiconductor device is to respond to a read request or a write request infringe one or more of its patents that claim a priority date before June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 508:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "programmable register," "specifying a manner," "the semiconductor device," "respond to a read request," and "respond to a . . . write request."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain devices purporting to be JEDEC-compliant SDRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 509:**

Admit that Rambus has alleged that JEDEC-compliant DDR SDRAM devices using a programmable register operative to store information specifying a manner in which the semiconductor device is to respond to a read request or a write request infringe one or more of its patents that claim a priority date before June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 509:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "programmable register," "specifying a manner," "the semiconductor device," "respond to a read request," and "respond to a . . . write request."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain devices purporting to be JEDEC-compliant DDR SDRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 510:**

Admit that Rambus has one or more issued patents claiming a priority date before June

1996 containing claims that would cover a programmable register that receives information that defines an amount of data to be input by the memory device in response to a write request in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 510:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "cover," "programmable register," "receives information," "defines an amount of data," "response to a write request," and "non-compatible DRAM device." Rambus further objects that the request calls for a legal conclusion. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain non-compatible DRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 511:**

Admit that Rambus has one or more pending patent applications containing claims that, if included in an issued patent, would cover a programmable register that receives information that defines an amount of data to be input by the memory device in response to a write request in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 511:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "cover," "programmable register," "receives information," "defines an amount of data," "response to a write request," and "non-compatible DRAM device." Rambus

further objects that the request calls for a legal conclusion. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 512:**

Admit that Rambus has alleged that JEDEC-compliant SDRAM devices using a programmable register that receives information that defines an amount of data to be input by the memory device in response to a write request infringe one or more of its patents that claim a priority date before June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 512:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "programmable register," "receives information," "defines an amount of data" and "response to a write request."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain devices purporting to be JEDEC-compliant SDRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 513:**

Admit that Rambus has alleged that JEDEC-compliant DDR SDRAM devices using a programmable register that receives information that defines an amount of data to be input by the

memory device in response to a write request infringe one or more of its patents that claim a priority date before June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 513:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "programmable register," "receives information," "defines an amount of data" and "response to a write request."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain devices purporting to be JEDEC-compliant DDR SDRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 514:**

Admit that Rambus has one or more issued patents claiming a priority date before June 1996 containing claims that would cover a programmable register to store a value that defines an amount of data to be input by the memory device in response to a write request in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 514:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "programmable register," "defines an amount of data," "response to a write request," "cover," and "non-compatible DRAM device." Rambus further objects that the request calls for a legal conclusion. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain non-compatible DRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 515:**

Admit that Rambus has one or more pending patent applications containing claims that, if included in an issued patent, would cover a programmable register to store a value that defines an amount of data to be input by the memory device in response to a write request in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 515:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "programmable register," "defines an amount of data," "response to a write request," "cover," and "non-compatible DRAM device." Rambus further objects that the request calls for a legal conclusion. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 516:**

Admit that Rambus has alleged that JEDEC-compliant SDRAM devices using a programmable register to store a value that defines an amount of data to be input by the memory device in response to a write request in response to a write request infringe one or more of its

patents that claim a priority date before June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 516:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "programmable register," "defines an amount of data" and "response to a write request in response to a write request."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain devices purporting to be JEDEC-compliant SDRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 517:**

Admit that Rambus has alleged that JEDEC-compliant DDR SDRAM devices a programmable register to store a value that defines an amount of data to be input by the memory device in response to a write request infringe one or more of its patents that claim a priority date before June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 517:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "devices a programmable register," "defines an amount of data" and "response to a write request."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain devices purporting to be JEDEC-compliant DDR SDRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 518:**

Admit that Rambus has alleged that JEDEC-compliant DDR SDRAM devices that output data synchronously with respect to the rising and falling edge of an external clock signal infringe patents that it owns and that claim a priority date of April 18, 1990.

**RESPONSE TO REQUEST FOR ADMISSION NO. 518:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "synchronously," "rising and falling edge" and "external clock signal."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain devices purporting to be JEDEC-compliant DDR SDRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 519:**

Admit that Rambus owns patents claiming a priority date of April 18, 1990 that it believes covers the output of data synchronously with respect to the rising and falling edge of an external clock signal in JEDEC-compliant DDR SDRAM devices.

**RESPONSE TO REQUEST FOR ADMISSION NO. 519:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "believes," "covers," "synchronously," "rising and falling edge" and "external clock signal." Rambus further objects that the request calls for a legal conclusion. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain devices purporting to be JEDEC-compliant DDR SDRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 520:**

Admit that Rambus has one or more issued patents claiming a priority date before June 1996 containing claims that would cover the output of a first portion of data in response to a rising edge of a clock signal and a second portion of data in response to a falling edge of a clock signal in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 520:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "cover," "first portion of data," "second portion of data," "a clock signal," and "non-compatible DRAM device." Rambus further objects that the request calls for a legal conclusion. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain non-compatible DRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 521:**

Admit that Rambus has one or more pending patent applications containing claims that, if included in an issued patent, would cover the output of a first portion of data in response to a rising edge of a clock signal and a second portion of data in response to a falling edge of a clock

signal in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 521:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "cover," "first portion of data," "second portion of data," "a clock signal," and "non-compatible DRAM device." Rambus further objects that the request calls for a legal conclusion. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 522:**

Admit that Rambus has alleged that JEDEC-compliant SDRAM devices where the output of a first portion of data in response to a rising edge of a clock signal and a second portion of data in response to a falling edge of a clock signal infringe one or more of its patents that claim a priority date before June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 522:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "JEDEC-compliant SDRAM devices," "first portion of data," "second portion of data" and "a clock signal."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain devices purporting to be JEDEC-compliant SDRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 523:**

Admit that Rambus has alleged that JEDEC-compliant DDR SDRAM devices where the output of a first portion of data in response to a rising edge of a clock signal and a second portion of data in response to a falling edge of a clock signal infringe one or more of its patents that claim a priority date before June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 523:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "first portion of data," "second portion of data" and "a clock signal."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain devices purporting to be JEDEC-compliant DDR SDRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 524:**

Admit that Rambus has one or more issued patents claiming a priority date before June 1996 containing claims that would cover the input of a first portion of data in response to a rising edge of a clock signal and a second portion of data in response to a falling edge of a clock signal in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 524:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "cover," "first portion of data," "second portion of data," "a clock signal," and "non-compatible DRAM device." Rambus further objects that the request calls for a legal conclusion. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either

literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain non-compatible DRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 525:**

Admit that Rambus has one or more pending patent applications containing claims that, if included in an issued patent, would cover the input of a first portion of data in response to a rising edge of a clock signal and a second portion of data in response to a falling edge of a clock signal in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 525:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "cover," "first portion of data," "second portion of data," "a clock signal," and "non-compatible DRAM device." Rambus further objects that the request calls for a legal conclusion. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 526:**

Admit that Rambus has alleged that JEDEC-compliant SDRAM devices where the input of a first portion of data in response to a rising edge of a clock signal and a second portion of

data in response to a falling edge of a clock signal infringe one or more of its patents that claim a priority date before June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 526:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "JEDEC-compliant SDRAM devices," "first portion of data," "second portion of data" and "a clock signal."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain devices purporting to be JEDEC-compliant SDRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 527:**

Admit that Rambus has alleged that JEDEC-compliant DDR SDRAM devices where the input of a first portion of data in response to a rising edge of a clock signal and a second portion of data in response to a falling edge of a clock signal infringe one or more of its patents that claim a priority date before June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 527:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "first portion of data," "second portion of data" and "a clock signal."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain devices purporting to be JEDEC-compliant SDRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 528:**

Admit that Rambus has one or more issued patents claiming a priority date before June 1996 containing claims that would cover the output of a first portion of data synchronously with respect to a rising edge of an external clock signal and a second portion of data synchronously with respect to a falling edge of the external clock signal in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 528:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "cover," "synchronously," "first portion of data," "second portion of data," "external clock signal," and "non-compatible DRAM device." Rambus further objects that the request calls for a legal conclusion. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain non-compatible DRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 529:**

Admit that Rambus has one or more pending patent applications containing claims that, if included in an issued patent, would cover the output of a first portion of data synchronously with respect to a rising edge of an external clock signal and a second portion of data synchronously with respect to a falling edge of the external clock signal in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 529:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least

with respect to the terms "cover," "synchronously," "first portion of data," "second portion of data," "external clock signal," and "non-compatible DRAM device." Rambus further objects that the request calls for a legal conclusion. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 530:**

Admit that Rambus has alleged that JEDEC-compliant SDRAM devices where the output of a first portion of data synchronously with respect to a rising edge of an external clock signal and a second portion of data synchronously with respect to a falling edge of the external clock signal infringe one or more of its patents that claim a priority date before June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 530:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "JEDEC-compliant SDRAM devices," "synchronously," "first portion of data," "second portion of data" and "external clock signal."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain devices purporting to be JEDEC-compliant SDRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 531:**

Admit that Rambus has alleged that JEDEC-compliant DDR SDRAM devices where the output of a first portion of data synchronously with respect to a rising edge of an external clock signal and a second portion of data synchronously with respect to a falling edge of the external clock signal infringe one or more of its patents that claim a priority date before June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 531:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "synchronously," "first portion of data," "second portion of data" and "external clock signal."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain devices purporting to be JEDEC-compliant DDR SDRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 532:**

Admit that Rambus has one or more issued patents claiming a priority date before June 1996 containing claims that would cover data output occurring synchronously with respect to both the rising edge of the external clock signal and the falling edge of the external clock signal in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 532:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "cover," "synchronously," "external clock signal," and "non-compatible DRAM device." Rambus further objects that the request calls for a legal conclusion. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the

doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain non-compatible DRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 533:**

Admit that Rambus has one or more pending patent applications containing claims that, if included in an issued patent, would cover data output occurring synchronously with respect to both the rising edge of the external clock signal and the falling edge of the external clock signal in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 533:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "cover," "synchronously," "external clock signal," and "non-compatible DRAM device." Rambus further objects that the request calls for a legal conclusion. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 534:**

Admit that Rambus has alleged that JEDEC-compliant SDRAM devices where data output occurs synchronously with respect to both the rising edge of the external clock signal and

the falling edge of the external clock signal infringe one or more of its patents that claim a priority date before June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 534:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "JEDEC-compliant SDRAM devices," "synchronously," and "external clock signal."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain devices purporting to be JEDEC-compliant SDRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 535:**

Admit that Rambus has alleged that JEDEC-compliant DDR SDRAM devices where data output occurs synchronously with respect to both the rising edge of the external clock signal and the falling edge of the external clock signal infringe one or more of its patents that claim a priority date before June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 535:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "synchronously" and "external clock signal."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain devices purporting to be JEDEC-compliant DDR SDRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 536:**

Admit that Rambus has one or more issued patents claiming a priority date before June 1996 containing claims that would cover the input of a first portion of data synchronously with respect to a rising edge of an external clock signal and a second portion of data synchronously with respect to a falling edge of the external clock signal in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 536:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "cover," "synchronously," "first portion of data," "second portion of data," "external clock signal," and "non-compatible DRAM device." Rambus further objects that the request calls for a legal conclusion. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain non-compatible DRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 537:**

Admit that Rambus has one or more pending patent applications containing claims that, if included in an issued patent, would cover the input of a first portion of data synchronously with respect to a rising edge of an external clock signal and a second portion of data synchronously with respect to a falling edge of the external clock signal in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 537:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least

with respect to the terms "cover," "synchronously," "first portion of data," "second portion of data," "external clock signal," and "non-compatible DRAM device." Rambus further objects that the request calls for a legal conclusion. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 538:**

Admit that Rambus has alleged that JEDEC-compliant SDRAM devices where the input of a first portion of data synchronously with respect to a rising edge of an external clock signal and a second portion of data synchronously with respect to a falling edge of the external clock signal infringe one or more of its patents that claim a priority date before June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 538:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "JEDEC-compliant SDRAM devices," "synchronously," "first portion of data," "second portion of data," and "external clock signal."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain devices purporting to be JEDEC-compliant SDRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 539:**

Admit that Rambus has alleged that JEDEC-compliant DDR SDRAM devices where the input of a first portion of data synchronously with respect to a rising edge of an external clock signal and a second portion of data synchronously with respect to a falling edge of the external clock signal infringe one or more of its patents that claim a priority date before June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 539:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "synchronously," "first portion of data," "second portion of data," and "external clock signal."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain devices purporting to be JEDEC-compliant DDR SDRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 540:**

Admit that Rambus has one or more issued patents claiming a priority date before June 1996 containing claims that would cover data input occurring synchronously with respect to both the rising edge of the external clock signal and the falling edge of the external clock signal in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 540:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "cover," "synchronously," "external clock signal," and "non-compatible DRAM device." Rambus further objects that the request calls for a legal conclusion. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the

doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain non-compatible DRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 541:**

Admit that Rambus has one or more pending patent applications containing claims that, if included in an issued patent, would cover data input occurring synchronously with respect to both the rising edge of the external clock signal and the falling edge of the external clock signal in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 541:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "cover," "synchronously," "external clock signal," and "non-compatible DRAM device." Rambus further objects that the request calls for a legal conclusion. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 542:**

Admit that Rambus has alleged that JEDEC-compliant SDRAM devices where data input occurs synchronously with respect to both the rising edge of the external clock signal and the

falling edge of the external clock signal infringe one or more of its patents that claim a priority date before June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 542:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "JEDEC-compliant SDRAM devices," "synchronously," and "external clock signal."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain devices purporting to be JEDEC-compliant SDRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 543:**

Admit that Rambus has alleged that JEDEC-compliant DDR SDRAM devices where data input occurs synchronously with respect to both the rising edge of the external clock signal and the falling edge of the external clock signal infringe one or more of its patents that claim a priority date before June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 543:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "synchronously" and "external clock signal."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain devices purporting to be JEDEC-compliant DDR SDRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 544:**

Admit that Rambus has one or more issued patents claiming a priority date before June 1996 containing claims that would cover the output of a first portion of data synchronously with respect to a first external clock signal and a second portion of data synchronously with respect to a second external clock signal in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 544:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "cover," "synchronously," "first portion of data," "second portion of data," "first external clock signal," "second external clock signal," and "non-compatible DRAM device." Rambus further objects that the request calls for a legal conclusion. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain non-compatible DRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 545:**

Admit that Rambus has one or more pending patent applications containing claims that, if included in an issued patent, would cover the output of a first portion of data synchronously with respect to a first external clock signal and a second portion of data synchronously with respect to a second external clock signal in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 545:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least

with respect to the terms "cover," "synchronously," "first portion of data," "second portion of data," "first external clock signal," "second external clock signal," and "non-compatible DRAM device." Rambus further objects that the request calls for a legal conclusion. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 546:**

Admit that Rambus has alleged that JEDEC-compliant SDRAM devices where the output of a first portion of data synchronously with respect to a first external clock signal and a second portion of data synchronously with respect to a second external clock signal infringe one or more of its patents that claim a priority date before June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 546:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "JEDEC-compliant SDRAM devices," "synchronously," "first portion of data," "second portion of data," "first external clock signal," and "second external clock signal."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain devices purporting to be JEDEC-compliant SDRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 547:**

Admit that Rambus has alleged that JEDEC-compliant DDR SDRAM devices where the output of a first portion of data synchronously with respect to a first external clock signal and a second portion of data synchronously with respect to a second external clock signal infringe one or more of its patents that claim a priority date before June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 547:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "synchronously," "first portion of data," "second portion of data," "first external clock signal," and "second external clock signal."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain devices purporting to be JEDEC-compliant DDR SDRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 548:**

Admit that Rambus has one or more issued patents claiming a priority date before June 1996 containing claims that would cover data output occurring synchronously with respect to a both a first external clock signal and a second external clock signal in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 548:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "cover," "synchronously," "first external clock signal," "second external clock signal," and "non-compatible DRAM device." Rambus further objects that the request calls for a legal conclusion. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of

the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain non-compatible DRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 549:**

Admit that Rambus has one or more pending patent applications containing claims that, if included in an issued patent, would cover data output occurring synchronously with respect to both a first external clock signal and a second external clock signal in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 549:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "cover," "synchronously," "first external clock signal," "second external clock signal," and "non-compatible DRAM device." Rambus further objects that the request calls for a legal conclusion. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 550:**

Admit that Rambus has alleged that JEDEC-compliant SDRAM devices where data output occurs synchronously with respect to both a first external clock signal and a second external clock signal infringe one or more of its patents that claim a priority date before June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 550:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "JEDEC-compliant SDRAM devices," "synchronously," "first external clock signal," and "second external clock signal."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain devices purporting to be JEDEC-compliant SDRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 551:**

Admit that Rambus has alleged that JEDEC-compliant DDR SDRAM devices where data output occurs synchronously with respect to both a first external clock signal and a second external clock signal infringe one or more of its patents that claim a priority date before June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 551:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "synchronously," "first external clock signal," and "second external clock signal."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain devices purporting to be JEDEC-compliant DDR

SDRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 552:**

Admit that Rambus has one or more issued patents claiming a priority date before June 1996 containing claims that would cover the input of a first portion of data synchronously with respect to a first external clock signal and a second portion of data synchronously with respect to a second external clock signal in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 552:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "cover," "synchronously," "first portion of data," "second portion of data," "first external clock signal," "second external clock signal," and "non-compatible DRAM device." Rambus further objects that the request calls for a legal conclusion. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain non-compatible DRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 553:**

Admit that Rambus has one or more pending patent applications containing claims that, if included in an issued patent, would cover the input of a first portion of data synchronously with respect to a first external clock signal and a second portion of data synchronously with respect to

a second external clock signal in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 553:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "cover," "synchronously," "first portion of data," "second portion of data," "first external clock signal," "second external clock signal," and "non-compatible DRAM device." Rambus further objects that the request calls for a legal conclusion. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 554:**

Admit that Rambus has alleged that JEDEC-compliant SDRAM devices where the input of a first portion of data synchronously with respect to a first external clock signal and a second portion of data synchronously with respect to a second external clock signal infringe one or more of its patents that claim a priority date before June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 554:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "JEDEC-compliant SDRAM devices," "synchronously," "first portion of data," "second portion of data," "first external clock signal," and "second external clock signal."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain devices purporting to be JEDEC-compliant

SDRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 555:**

Admit that Rambus has alleged that JEDEC-compliant DDR SDRAM devices where the input of a first portion of data synchronously with respect to a first external clock signal and a second portion of data synchronously with respect to a second external clock signal infringe one or more of its patents that claim a priority date before June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 555:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "synchronously," "first portion of data," "second portion of data," "first external clock signal," and "second external clock signal."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain devices purporting to be JEDEC-compliant DDR SDRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 556:**

Admit that Rambus has one or more issued patents claiming a priority date before June 1996 containing claims that would cover data input occurring synchronously with respect to both a first and a second external clock signal in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 556:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "cover," "synchronously," "first . . . external clock signal," "second external clock signal," and "non-compatible DRAM device." Rambus further objects that the request calls for a legal conclusion. Rambus further objects that, to the extent that "cover" is to

be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain non-compatible DRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 557:**

Admit that Rambus has one or more pending patent applications containing claims that, if included in an issued patent, would cover data input occurring synchronously with respect to both a first and a second external clock signal in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 557:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "cover," "synchronously," "first . . . external clock signal," "second external clock signal," and "non-compatible DRAM device." Rambus further objects that the request calls for a legal conclusion. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 558:**

Admit that Rambus has alleged that JEDEC-compliant SDRAM devices where data input occurs synchronously with respect to both a first and a second external clock signal infringe one or more of its patents that claim a priority date before June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 558:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "JEDEC-compliant SDRAM devices," "synchronously," "first . . . external clock signal," and "second external clock signal."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain devices purporting to be JEDEC-compliant SDRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 559:**

Admit that Rambus has alleged that JEDEC-compliant DDR SDRAM devices where data input occurs synchronously with respect to both a first and a second external clock signal infringe one or more of its patents that claim a priority date before June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 559:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "synchronously," "first . . . external clock signal," and "second external clock signal."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain devices purporting to be JEDEC-compliant DDR SDRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 560:**

Admit that Rambus has one or more issued patents claiming a priority date before June 1996 containing claims that would cover the use of a dual edge clocking scheme which inputs and outputs data synchronously with the rising and falling edge of an external clock in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 560:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "cover," "dual edge clocking scheme," "synchronously," "rising and falling edge," "external clock signal," and "non-compatible DRAM device." Rambus further objects that the request calls for a legal conclusion. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain non-compatible DRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 561:**

Admit that Rambus has one or more pending patent applications containing claims that, if included in an issued patent, would cover the use of a dual edge clocking scheme which inputs and outputs data synchronously with the rising and falling edge of an external clock in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 561:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "cover," "dual edge clocking scheme," "synchronously," "rising and falling edge," "external clock signal," and "non-compatible DRAM device." Rambus further objects that the request calls for a legal conclusion. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 562:**

Admit that Rambus has alleged that JEDEC-compliant SDRAM devices that use a dual edge clocking scheme which inputs and outputs data synchronously with the rising and falling edge of an external clock infringe one or more of its patents that claim a priority date before June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 562:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "JEDEC-compliant SDRAM devices," "dual edge clocking scheme," "synchronously," "rising and falling edge," and "external clock signal."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain devices purporting to be JEDEC-compliant SDRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 563:**

Admit that Rambus has alleged that JEDEC-compliant DDR SDRAM devices that use a dual edge clocking scheme which inputs and outputs data synchronously with the rising and falling edge of an external clock infringe one or more of its patents that claim a priority date before June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 563:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "dual edge clocking scheme," "synchronously," "rising and falling edge," and "external clock signal."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain devices purporting to be JEDEC-compliant DDR SDRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 564:**

Admit that Rambus has one or more issued patents claiming a priority date before June 1996 containing claims that would cover data input and output occurring synchronously with the rising and falling edge of an external clock, according to a dual edge clocking scheme in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 564:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "cover," "dual edge clocking scheme," "synchronously," "rising and falling edge," "external clock," and "non-compatible DRAM device." Rambus further objects that the request calls for a legal conclusion. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed

by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain non-compatible DRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 565:**

Admit that Rambus has one or more pending patent applications containing claims that, if included in an issued patent, would cover data input and output occurring synchronously with the rising and falling edge of an external clock, according to a dual edge clocking scheme in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 565:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "cover," "dual edge clocking scheme," "synchronously," "rising and falling edge," "external clock," and "non-compatible DRAM device." Rambus further objects that the request calls for a legal conclusion. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 566:**

Admit that Rambus has alleged that JEDEC-compliant SDRAM devices where data input and output occurs synchronously with the rising and falling edge of an external clock, according to a dual edge clocking scheme infringe one or more of its patents that claim a priority date before June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 566:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "JEDEC-compliant SDRAM devices," "dual edge clocking scheme," "synchronously," "rising and falling edge," and "external clock."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain devices purporting to be JEDEC-compliant SDRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 567:**

Admit that Rambus has alleged that JEDEC-compliant DDR SDRAM devices where data input and output occurs synchronously with the rising and falling edge of an external clock, according to a dual edge clocking scheme infringe one or more of its patents that claim a priority date before June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 567:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "dual edge clocking scheme," "synchronously," "rising and falling edge," and "external clock."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain devices purporting to be JEDEC-compliant DDR

SDRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 568:**

Admit that Rambus has alleged that JEDEC-compliant DDR SDRAM devices that contain delay locked loop circuitry to generate an internal clock signal using an external clock signal infringe patents that it owns and that claim a priority date of April 18, 1990.

**RESPONSE TO REQUEST FOR ADMISSION NO. 568:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "delay locked loop circuitry," and "generate an internal clock signal using an external clock signal."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date of April 18, 1990 are infringed by certain devices purporting to be JEDEC-compliant DDR SDRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 569:**

Admit that Rambus owns patents claiming a priority date of April 18, 1990 that it believes covers the use of delay locked loop circuitry to generate an internal clock signal using an external clock signal in JEDEC-compliant DDR SDRAM devices.

**RESPONSE TO REQUEST FOR ADMISSION NO. 569:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "believes," "covers," "delay locked loop circuitry," and "generate an internal clock signal using an external clock signal." Rambus further objects that the request calls for a legal conclusion. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given

DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain devices purporting to be JEDEC-compliant DDR SDRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 570:**

Admit that Rambus has one or more issued patents claiming a priority date before June 1996 containing claims that would cover on-chip PLL or on-chip DLL circuitry in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 570:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "on-chip PLL," "on-chip DLL," "cover," and "non-compatible DRAM device." Rambus further objects that the request calls for a legal conclusion. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain non-compatible DRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 571:**

Admit that Rambus has one or more pending patent applications containing claims that, if included in an issued patent, would cover on-chip PLL or on-chip DLL circuitry in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 571:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "on-chip PLL," "on-chip DLL," "cover," and "non-compatible DRAM device." Rambus further objects that the request calls for a legal conclusion. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 572:**

Admit that Rambus has alleged that JEDEC-compliant SDRAM devices with on-chip PLL or on-chip DLL circuitry infringe one or more of its patents that claim a priority date before June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 572:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "JEDEC-compliant SDRAM devices," "on-chip PLL," and "on-chip DLL."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain devices purporting to be JEDEC-compliant

SDRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 573:**

Admit that Rambus has alleged that JEDEC-compliant DDR SDRAM devices with on-chip PLL or on-chip DLL circuitry infringe one or more of its patents that claim a priority date before June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 573:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "on-chip PLL" and "on-chip DLL."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain devices purporting to be JEDEC-compliant DDR SDRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 574:**

Admit that Rambus has one or more issued patents claiming a priority date before June 1996 containing claims that would cover phase locked loop circuitry or delay locked loop circuitry to generate an internal clock signal using an external clock signal in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 574:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "phase locked loop circuitry," "delay locked loop circuitry," "generate an internal clock signal using an external clock signal," "cover," and "non-compatible DRAM device." Rambus further objects that the request calls for a legal conclusion. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any

particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain non-compatible DRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 575:**

Admit that Rambus has one or more pending patent applications containing claims that, if included in an issued patent, would cover phase locked loop circuitry or delay locked loop circuitry to generate an internal clock signal using an external clock signal in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 575:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "phase locked loop circuitry," "delay locked loop circuitry," "generate an internal clock signal using an external clock signal," "cover," and "non-compatible DRAM device." Rambus further objects that the request calls for a legal conclusion. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 576:**

Admit that Rambus has alleged that JEDEC-compliant SDRAM devices with phase locked loop circuitry or delay locked loop circuitry to generate an internal clock signal using an external clock signal infringe one or more of its patents that claim a priority date before June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 576:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "JEDEC-compliant SDRAM devices," "phase locked loop circuitry," "delay locked loop circuitry," and "generate an internal clock signal using an external clock signal."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain devices purporting to be JEDEC-compliant SDRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 577:**

Admit that Rambus has alleged that JEDEC-compliant DDR SDRAM devices phase locked loop circuitry or delay locked loop circuitry to generate an internal clock signal using an external clock signal infringe one or more of its patents that claim a priority date before June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 577:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "phase locked loop circuitry," "delay locked loop circuitry," and "generate an internal clock signal using an external clock signal."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority

date before June 1996 are infringed by certain devices purporting to be JEDEC-compliant DDR SDRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 578:**

Admit that Rambus has one or more issued patents claiming a priority date before June 1996 containing claims that would cover phase lock loop on DRAM to control delays inside and outside DRAM in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 578:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "phase lock loop on DRAM," "control delays inside and outside DRAM," "cover," and "non-compatible DRAM device." Rambus further objects that the request calls for a legal conclusion. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain non-compatible DRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 579:**

Admit that Rambus has one or more pending patent applications containing claims that, if included in an issued patent, would cover phase lock loop on DRAM to control delays inside and outside DRAM in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 579:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "phase lock loop on DRAM," "control delays inside and outside DRAM," "cover," and "non-compatible DRAM device." Rambus further objects that the request calls for a legal conclusion. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 580:**

Admit that Rambus has alleged that JEDEC-compliant SDRAM devices with a phase lock loop on DRAM to control delays inside and outside DRAM infringe one or more of its patents that claim a priority date before June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 580:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "JEDEC-compliant SDRAM devices," "phase lock loop on DRAM," and "control delays inside and outside DRAM."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain devices purporting to be JEDEC-compliant SDRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 581:**

Admit that Rambus has alleged that JEDEC-compliant DDR SDRAM devices with a phase lock loop on DRAM to control delays inside and outside DRAM infringe one or more of its patents that claim a priority date before June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 581:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "phase lock loop on DRAM" and "control delays inside and outside DRAM."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain devices purporting to be JEDEC-compliant DDR SDRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 582:**

Admit that Rambus has one or more issued patents claiming a priority date before June 1996 containing claims that would cover using a PLL/DLL circuit on a DRAM to reduce input buffer skews in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 582:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "PLL/DLL circuit," "reduce input buffer skews," "cover," and "non-compatible DRAM device." Rambus further objects that the request calls for a legal conclusion. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain non-compatible DRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 583:**

Admit that Rambus has one or more pending patent applications containing claims that, if included in an issued patent, would cover using a PLL/DLL circuit on a DRAM to reduce input buffer skews in a non-compatible DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 583:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "PLL/DLL circuit," "reduce input buffer skews," "cover," and "non-compatible DRAM device." Rambus further objects that the request calls for a legal conclusion. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 584:**

Admit that Rambus has alleged that JEDEC-compliant SDRAM devices using a PLL/DLL circuit on a DRAM to reduce input buffer skews infringe one or more of its patents that claim a priority date before June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 584:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least

with respect to the terms "JEDEC-compliant SDRAM devices," "PLL/DLL circuit," and "reduce input buffer skews."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain devices purporting to be JEDEC-compliant SDRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 585:**

Admit that Rambus has alleged that JEDEC-compliant DDR SDRAM devices using a PLL/DLL circuit on a DRAM to reduce input buffer skews infringe one or more of its patents that claim a priority date before June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 585:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "PLL/DLL circuit," and "reduce input buffer skews."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain devices purporting to be JEDEC-compliant DDR SDRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 586:**

Admit that Rambus has one or more issued patents claiming a priority date before June 1996 containing claims that would cover a non-compatible DRAM with PLL clock generation.

**RESPONSE TO REQUEST FOR ADMISSION NO. 586:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "PLL clock generation," "cover," and "non-compatible DRAM."

Rambus further objects that the request calls for a legal conclusion. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain non-compatible DRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 587:**

Admit that Rambus has one or more pending patent applications containing claims that, if included in an issued patent, would cover a non-compatible DRAM with PLL clock generation.

**RESPONSE TO REQUEST FOR ADMISSION NO. 587:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "PLL clock generation," "cover," and "non-compatible DRAM." Rambus further objects that the request calls for a legal conclusion. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 588:**

Admit that Rambus has alleged that JEDEC-compliant SDRAM devices with PLL clock generation infringe one or more of its patents that claim a priority date before June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 588:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "JEDEC-compliant SDRAM devices" and "PLL clock generation."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain devices purporting to be JEDEC-compliant SDRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 589:**

Admit that Rambus has alleged that JEDEC-compliant DDR SDRAM devices with PLL clock generation infringe one or more of its patents that claim a priority date before June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 589:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the term "PLL clock generation."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain devices purporting to be JEDEC-compliant DDR SDRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 590:**

Admit that Rambus has one or more issued patents claiming a priority date before June 1996 containing claims that would cover using a PLL on an SDRAM in a non-compatible

DRAM.

**RESPONSE TO REQUEST FOR ADMISSION NO. 590:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "using a PLL," "cover," and "non-compatible DRAM." Rambus further objects that the term "an SDRAM in a non-compatible DRAM" is unintelligible.

**REQUEST FOR ADMISSION NO. 591:**

Admit that Rambus has one or more pending patent applications containing claims that, if included in an issued patent, would cover using a PLL on an SDRAM in a non-compatible DRAM.

**RESPONSE TO REQUEST FOR ADMISSION NO. 591:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "using a PLL," "cover," and "non-compatible DRAM." Rambus further objects that the term "an SDRAM in a non-compatible DRAM" is unintelligible.

**REQUEST FOR ADMISSION NO. 592:**

Admit that Rambus has alleged that JEDEC-compliant SDRAM devices using a PLL on an SDRAM infringe one or more of its patents that claim a priority date before June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 592:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "JEDEC-compliant SDRAM devices," "using a PLL," and "an SDRAM."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain devices purporting to be JEDEC-compliant SDRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 593:**

Admit that Rambus has alleged that JEDEC-compliant DDR SDRAM devices using a PLL on an SDRAM infringe one or more of its patents that claim a priority date before June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 593:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "using a PLL" and "an SDRAM."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain devices purporting to be JEDEC-compliant DDR SDRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 594:**

Admit that Rambus has one or more issued patents claiming a priority date before June 1996 containing claims that would cover using a DLL to compensate for the output delay in a non-compatible DRAM.

**RESPONSE TO REQUEST FOR ADMISSION NO. 594:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "using a DLL," "compensate for the output delay," "cover," and "non-compatible DRAM." Rambus further objects that the request calls for a legal conclusion. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain non-compatible DRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 595:**

Admit that Rambus has one or more pending patent applications containing claims that, if included in an issued patent, would cover using a DLL to compensate for the output delay in a non-compatible DRAM.

**RESPONSE TO REQUEST FOR ADMISSION NO. 595:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "using a DLL," "compensate for the output delay," "cover," and "non-compatible DRAM." Rambus further objects that the request calls for a legal conclusion. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 596:**

Admit that Rambus has alleged that JEDEC-compliant SDRAM devices using a DLL to compensate for the output delay infringe one or more of its patents that claim a priority date before June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 596:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least

with respect to the terms "JEDEC-compliant SDRAM devices," "using a DLL," and "compensate for the output delay."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain devices purporting to be JEDEC-compliant SDRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 597:**

Admit that Rambus has alleged that JEDEC-compliant DDR SDRAM devices using a DLL to compensate for the output delay infringe one or more of its patents that claim a priority date before June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 597:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "using a DLL" and "compensate for the output delay."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it has alleged that claims of certain of its patents claiming a priority date before June 1996 are infringed by certain devices purporting to be JEDEC-compliant DDR SDRAM devices.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 598:**

Admit that JEDEC was more likely to attempt to develop alternative methods or technologies to provide any feature needed by a JEDEC standard if the members of the relevant JEDEC committee were aware that the method or technology currently proposed for inclusion in the standard was covered by the claims of a patent, or potentially covered by the claims of a patent application, than if the method or technology were not covered by the claims of a patent,

or potentially covered by the claims of a patent application.

**RESPONSE TO REQUEST FOR ADMISSION NO. 598:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "JEDEC," "alternative methods or technologies," "feature needed by a JEDEC standard," "relevant JEDEC committee," "covered," and "potentially covered." Rambus also objects that the request poses an incomplete hypothetical which fails to specify, for example, the sort of methods or technologies at issue, the feasibility of implementing alternative methods or technologies, the ease of implementing alternative methods or technologies, the cost of implementing alternative methods or technologies, the terms of a potential patent license, or the views of JEDEC members about the validity of any patent at issue or the likelihood of a valid patent issuing with respect to any patent application at issue.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 599:**

Admit that JEDEC's discovery of the fact that a method or technology proposed for a JEDEC standard is covered by the claims of a patent, or potentially covered by the claims of a patent application, makes it more likely that JEDEC will attempt to develop an alternative method or technology to provide the same feature than if JEDEC does not discover that fact.

**RESPONSE TO REQUEST FOR ADMISSION NO. 599:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "JEDEC," "alternative method or technology," "feature," "covered," and "potentially covered." Rambus also objects that the request poses an incomplete hypothetical which fails to specify, for example, the sort of method or technology at issue, the feasibility of implementing an alternative method or technology, the ease of implementing an alternative method or technology, the cost of implementing an alternative method or technology, the terms of a potential patent license, or the views of JEDEC members about the validity of any

patent at issue or the likelihood of a valid patent issuing with respect to any patent application at issue.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 600:**

Admit that, for synchronous DRAM, there is at least one technically feasible method or technology, in addition to programmable CAS latency, that can be used to set the CAS latency of a DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 600:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "synchronous DRAM," "technically feasible method or technology," "programmable CAS latency," and "set the CAS latency." Rambus further objects that the request poses an incomplete hypothetical which fails to specify, for example, the type of system in which the DRAM is to be used or its corresponding performance criteria.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it would be possible, as a technical matter, without regard to the costs or difficulties associated with implementation, and without regard to the resulting performance, to modify the design of a purportedly JEDEC-compliant SDRAM so that the number of clock cycles to transpire between the receipt of a read instruction and the output of corresponding data by the SDRAM were fixed at manufacture.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 601:**

Admit that, for synchronous DRAM, there is at least one technically feasible method or technology, in addition to that required by the JEDEC standard 21-C, that can be used to set the CAS latency of a DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 601:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "synchronous DRAM," "technically feasible method or technology," and "set the CAS latency." Rambus further objects that the request is vague and ambiguous with respect to the version and requirements of JEDEC standard 21-C at issue. Rambus further objects that the request poses an incomplete hypothetical which fails to specify, for example, the type of system in which the DRAM is to be used or its corresponding performance criteria.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it would be possible, as a technical matter, without regard to the costs or difficulties associated with implementation, and without regard to the resulting performance, to modify the design of a purportedly JEDEC-compliant SDRAM so that the number of clock cycles to transpire between the receipt of a read instruction and the output of corresponding data by the SDRAM were fixed at manufacture.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 602:**

Admit that, for synchronous DRAM, there is at least one technically feasible method or technology, in addition to that currently used by JEDEC-compliant SDRAM and DDR SDRAM, that can be used to set the CAS latency of a DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 602:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "synchronous DRAM," "technically feasible method or technology," and "set the CAS latency." Rambus further objects that the request is vague and ambiguous with respect to the feature of JEDEC-compliant SDRAM and DDR SDRAM at issue and with respect to the type of JEDEC-compliant SDRAM or DDR SDRAM at issue. Rambus further objects that the request is compound. Rambus further objects that the request poses an incomplete hypothetical which fails to specify, for example, the type of system in which the DRAM is to be

used or its corresponding performance criteria.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it would be possible, as a technical matter, without regard to the costs or difficulties associated with implementation, and without regard to the resulting performance, to modify the design of a purportedly JEDEC-compliant SDRAM so that the number of clock cycles to transpire between the receipt of a read instruction and the output of corresponding data by the SDRAM were fixed at manufacture.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 603:**

Admit that permanently fixing the CAS latency at a single value is a technically feasible method of setting the CAS latency of a synchronous DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 603:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "synchronous DRAM device," "technically feasible method," and "CAS latency." Rambus further objects that the request poses an incomplete hypothetical which fails to specify, for example, the type of system in which the DRAM is to be used or its corresponding performance criteria.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it would be possible, as a technical matter, without regard to the costs or difficulties associated with implementation, and without regard to the resulting performance, to modify the design of a purportedly JEDEC-compliant SDRAM so that the number of clock cycles to transpire between the receipt of a read instruction and the output of corresponding data by the SDRAM were fixed at manufacture.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 604:**

Admit that having the memory controller signal the CAS latency through separate pins on each DRAM device is a technically feasible method of setting the CAS latency of a synchronous DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 604:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "synchronous DRAM device," "technically feasible method," "the memory controller," "setting the CAS latency," and "separate pins." Rambus further objects that the request poses an incomplete hypothetical which fails to specify, for example, the type of system in which the DRAM is to be used or its corresponding performance criteria.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it would be possible, as a technical matter, without regard to the costs or difficulties associated with implementation, and without regard to the resulting performance, to modify the design of a purportedly JEDEC-compliant SDRAM and the system in which the SDRAM is designed to operate so that the number of clock cycles to transpire between the receipt of a read instruction and the output of corresponding data by the SDRAM were specified through signals received by the added pins from a memory controller.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 605:**

Admit that setting the CAS latency through the command structure of the read command is a technically feasible method of setting the CAS latency of a synchronous DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 605:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "synchronous DRAM device," "technically feasible method," "setting the CAS latency," and "command structure of the read command." Rambus further objects that

the request poses an incomplete hypothetical which fails to specify, for example, the type of system in which the DRAM is to be used or its corresponding performance criteria.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it would be possible, as a technical matter, without regard to the costs or difficulties associated with implementation, and without regard to the resulting performance, to modify the design of a purportedly JEDEC-compliant SDRAM and the system in which the SDRAM is designed to operate, so that different read instructions would be used depending on the number of clock cycles to transpire between the receipt of the read instruction and the output of corresponding data by the SDRAM.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 606:**

Admit that using fixed latency parts, as described in Jacob, Expert Report on Synchronous DRAM Architectures, Organizations and Alternative Technologies, pages 52-56, is a technically feasible method of setting the CAS latency of a synchronous DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 606:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms “synchronous DRAM device,” “fixed latency parts” “technically feasible method” and “setting the CAS latency.” Rambus further objects that the request is vague and ambiguous in that the referenced pages of the Jacob Report discuss numerous topics. Rambus further objects that the request poses an incomplete hypothetical which fails to specify, for example, the type of system in which the DRAM is to be used or its corresponding performance criteria.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it would be possible, as a technical matter, without regard to the costs or difficulties associated with implementation, and without regard to the resulting performance, to modify the design of a purportedly JEDEC-compliant SDRAM so that the

number of clock cycles to transpire between the receipt of a read instruction and the output of corresponding data by the SDRAM were fixed at manufacture.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 607:**

Admit that explicitly identifying the CAS latency in the read or write command, as described in Jacob, Expert Report on Synchronous DRAM Architectures, Organizations and Alternative Technologies, pages 52-56, is a technically feasible method of setting the CAS latency of a synchronous DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 607:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "synchronous DRAM device," "identifying the CAS latency in the read or write command" "technically feasible method" and "setting the CAS latency." Rambus further objects that the request is vague and ambiguous in that the referenced pages of the Jacob Report discuss numerous topics. Rambus further objects that the request is compound. Rambus further objects that the request poses an incomplete hypothetical which fails to specify, for example, the type of system in which the DRAM is to be used or its corresponding performance criteria.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it would be possible, as a technical matter, without regard to the costs or difficulties associated with implementation, and without regard to the resulting performance, to modify the design of a purportedly JEDEC-compliant SDRAM and the system in which the SDRAM is designed to operate, so that different read instructions would be used depending on the number of clock cycles to transpire between the receipt of the read instruction and the output of corresponding data by the SDRAM.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 608:**

Admit that programming CAS latency by blowing fuses on the DRAM, as described in Jacob, Expert Report on Synchronous DRAM Architectures, Organizations and Alternative Technologies, pages 52-56, is a technically feasible method of setting the CAS latency of a synchronous DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 608:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "synchronous DRAM device," "programming CAS latency," "blowing fuses on the DRAM," "technically feasible method" and "setting the CAS latency." Rambus further objects that the request is vague and ambiguous in that the referenced pages of the Jacob Report discuss numerous topics. Rambus further objects that the request is compound. Rambus further objects that the request poses an incomplete hypothetical which fails to specify, for example, the type of system in which the DRAM is to be used or its corresponding performance criteria.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 609:**

Admit that scaling CAS latency with clock frequency, as described in Jacob, Expert Report on Synchronous DRAM Architectures, Organizations and Alternative Technologies, pages 52-56, is a technically feasible method of setting the CAS latency of a synchronous DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 609:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "synchronous DRAM device," "scaling CAS latency with clock frequency" "technically feasible method" and "setting the CAS latency." Rambus further objects that the request is vague and ambiguous in that the referenced pages of the Jacob Report discuss

numerous topics. Rambus further objects that the request is compound. Rambus further objects that the request poses an incomplete hypothetical which fails to specify, for example, the type of system in which the DRAM is to be used or its corresponding performance criteria. Rambus further objects that the section on page 55 of the Jacob Report headed "Scale CAS Latency with Clock Frequency," is vague and ambiguous in that it gives no detail about how this "alternative" is to be implemented.

**REQUEST FOR ADMISSION NO. 610:**

Admit that using an existing pin or a new, dedicated pin to identify the latency via two or more different voltage levels asserted by the memory controller, as described in Jacob, Expert Report on Synchronous DRAM Architectures, Organizations and Alternative Technologies, pages 52-56, is a technically feasible method of setting the CAS latency of a synchronous DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 610:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "synchronous DRAM device," "identify the latency," "technically feasible method" and "setting the CAS latency." Rambus further objects that the request is vague and ambiguous in that the referenced pages of the Jacob Report discuss numerous topics. Rambus further objects that the request is compound. Rambus further objects that the request poses an incomplete hypothetical which fails to specify, for example, the type of system in which the DRAM is to be used or its corresponding performance criteria.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 611:**

Admit that using asynchronous DRAM, as described in Jacob, Expert Report on Synchronous DRAM Architectures, Organizations and Alternative Technologies, pages 52-56, is

a technically feasible method of setting the CAS latency of a synchronous DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 611:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "synchronous DRAM device," "asynchronous DRAM," "technically feasible method" and "setting the CAS latency." Rambus further objects that the request is vague and ambiguous in that the referenced pages of the Jacob Report discuss numerous topics. Rambus further objects that the request poses an incomplete hypothetical which fails to specify, for example, the type of system in which the DRAM is to be used or its corresponding performance criteria. Rambus further objects that the request is unintelligible in its reference to using "asynchronous DRAM" to "set[] CAS latency" in a "synchronous DRAM."

**REQUEST FOR ADMISSION NO. 612:**

Admit that, for synchronous DRAM, there is at least one technically feasible method or technology, in addition to programmable burst length, that can be used to set the burst length of a DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 612:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "synchronous DRAM," "technically feasible method or technology," "programmable burst length," and "set the burst length." Rambus further objects that the request poses an incomplete hypothetical which fails to specify, for example, the type of system in which the DRAM is to be used or its corresponding performance criteria.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it would be possible, as a technical matter, without regard to the costs or difficulties associated with implementation, and without regard to the resulting performance, to modify the design of a purportedly JEDEC-compliant SDRAM so that the amount of data that the SDRAM outputs in response to any single read instruction were fixed at manufacture.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 613:**

Admit that, for synchronous DRAM, there is at least one technically feasible method or technology, in addition to that required by the JEDEC standard 21-C, that can be used to set the burst length of a DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 613:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "synchronous DRAM," "technically feasible method or technology," and "set the burst length." Rambus further objects that the request is vague and ambiguous with respect to the version and requirements of JEDEC standard 21-C at issue. Rambus further objects that the request poses an incomplete hypothetical which fails to specify, for example, the type of system in which the DRAM is to be used or its corresponding performance criteria.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it would be possible, as a technical matter, without regard to the costs or difficulties associated with implementation, and without regard to the resulting performance, to modify the design of a purportedly JEDEC-compliant SDRAM so that the amount of data that the SDRAM outputs in response to any single read instruction were fixed at manufacture.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 614:**

Admit that, for synchronous DRAM, there is at least one technically feasible method or technology, in addition to that currently used by JEDEC-compliant SDRAM and DDR SDRAM, that can be used to set the burst length of a DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 614:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least

with respect to the terms "synchronous DRAM device," "technically feasible method," and "set the burst length." Rambus further objects that the request poses an incomplete hypothetical which fails to specify, for example, the type of system in which the DRAM is to be used or its corresponding performance criteria.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it would be possible, as a technical matter, without regard to the costs or difficulties associated with implementation, and without regard to the resulting performance, to modify the design of a purportedly JEDEC-compliant SDRAM so that the amount of data that the SDRAM outputs in response to any single read instruction were fixed at manufacture.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 615:**

Admit that fixing the burst length at a single value is a technically feasible method of setting the burst length of a synchronous DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 615:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "synchronous DRAM device," "technically feasible method," and "setting the burst length." Rambus further objects that the request poses an incomplete hypothetical which fails to specify, for example, the type of system in which the DRAM is to be used or its corresponding performance criteria.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it would be possible, as a technical matter, without regard to the costs or difficulties associated with implementation, and without regard to the resulting performance, to modify the design of a purportedly JEDEC-compliant SDRAM so that the amount of data that the SDRAM outputs in response to any single read instruction were fixed at manufacture.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 616:**

Admit that having the memory controller signal the burst length through separate pins on each DRAM device is a technically feasible method of setting the burst length of a synchronous DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 616:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "synchronous DRAM device," "technically feasible method," "the memory controller," "setting the burst length," and "separate pins." Rambus further objects that the request poses an incomplete hypothetical which fails to specify, for example, the type of system in which the DRAM is to be used or its corresponding performance criteria.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it would be possible, as a technical matter, without regard to the costs or difficulties associated with implementation, and without regard to the resulting performance, to modify the design of a purportedly JEDEC-compliant SDRAM and the system in which the SDRAM is designed to operate so that the amount of data that the SDRAM outputs in response to any single read instruction were specified through signals received by the added pins from a memory controller.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 617:**

Admit that setting the burst length through the command structure of the read command is a technically feasible method of setting the burst length of a synchronous DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 617:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "synchronous DRAM device," "technically feasible method," "setting

the burst length," and "command structure of the read command." Rambus further objects that the request poses an incomplete hypothetical which fails to specify, for example, the type of system in which the DRAM is to be used or its corresponding performance criteria.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it would be possible, as a technical matter, without regard to the costs or difficulties associated with implementation, and without regard to the resulting performance, to modify the design of a purportedly JEDEC-compliant SDRAM and the system in which the SDRAM is designed to operate, so that different read instructions would be used depending on the amount of data that the SDRAM is to output in response to the read instruction

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 618:**

Admit that setting the burst length through the use of a burst interrupt feature is a technically feasible method of setting the burst length of a synchronous DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 618:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "synchronous DRAM device," "technically feasible method," "setting the burst length," and "command structure of the read command." Rambus further objects that the request poses an incomplete hypothetical which fails to specify, for example, the type of system in which the DRAM is to be used or its corresponding performance criteria.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it would be possible, as a technical matter, without regard to the costs or difficulties associated with implementation, and without regard to the resulting performance, to modify the design of a purportedly JEDEC-compliant SDRAM so that the amount of data that the SDRAM outputs in response to any single read instruction were fixed at manufacture at some maximum value and, if a smaller amount of data were desired, to interrupt or terminate the data output in some manner.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 619:**

Admit that using a short fixed burst length, as described in Jacob, Expert Report on Synchronous DRAM Architectures, Organizations and Alternative Technologies, pages 56-61, is a technically feasible method of setting the burst length of a synchronous DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 619:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "synchronous DRAM device," "short fixed burst length" "technically feasible method" and "setting the burst length." Rambus further objects that the request is vague and ambiguous in that the referenced pages of the Jacob Report discuss numerous topics. Rambus further objects that the request poses an incomplete hypothetical which fails to specify, for example, the type of system in which the DRAM is to be used or its corresponding performance criteria.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it would be possible, as a technical matter, without regard to the costs or difficulties associated with implementation, and without regard to the resulting performance, to modify the design of a purportedly JEDEC-compliant SDRAM so that the amount of data that the SDRAM outputs in response to any single read instruction were fixed at manufacture.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 620:**

Admit that explicitly identifying the burst length in the read or write command, as described in Jacob, Expert Report on Synchronous DRAM Architectures, Organizations and Alternative Technologies, pages 56-61, is a technically feasible method of setting the burst length of a synchronous DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 620:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "synchronous DRAM device," "identifying the burst length in the read or write command" "technically feasible method" and "setting the burst length." Rambus further objects that the request is vague and ambiguous in that the referenced pages of the Jacob Report discuss numerous topics. Rambus further objects that the request is compound. Rambus further objects that the request poses an incomplete hypothetical which fails to specify, for example, the type of system in which the DRAM is to be used or its corresponding performance criteria.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it would be possible, as a technical matter, without regard to the costs or difficulties associated with implementation, and without regard to the resulting performance, to modify the design of a purportedly JEDEC-compliant SDRAM and the system in which the SDRAM is designed to operate, so that different read instructions would be used depending on the amount of data that the SDRAM outputs in response to the read instruction.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 621:**

Admit that programming burst length by blowing fuses on the DRAM, as described in Jacob, Expert Report on Synchronous DRAM Architectures, Organizations and Alternative Technologies, pages 56-61, is a technically feasible method of setting the burst length of a synchronous DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 621:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "synchronous DRAM device," "programming burst length," "blowing fuses on the DRAM," "technically feasible method" and "setting the burst length." Rambus further objects that the request is vague and ambiguous in that the referenced pages of the Jacob Report discuss numerous topics. Rambus further objects that the request is compound. Rambus

further objects that the request poses an incomplete hypothetical which fails to specify, for example, the type of system in which the DRAM is to be used or its corresponding performance criteria.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 622:**

Admit that using a long fixed burst length coupled with the burst-terminate command, as described in Jacob, Expert Report on Synchronous DRAM Architectures, Organizations and Alternative Technologies, pages 56-61, is a technically feasible method of setting the burst length of a synchronous DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 622:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "synchronous DRAM device," "long fixed burst length," "burst terminate command," "technically feasible method" and "setting the burst length." Rambus further objects that the request is vague and ambiguous in that the referenced pages of the Jacob Report discuss numerous topics. Rambus further objects that the request is compound. Rambus further objects that the request poses an incomplete hypothetical which fails to specify, for example, the type of system in which the DRAM is to be used or its corresponding performance criteria.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that it would be possible, as a technical matter, without regard to the costs or difficulties associated with implementation, and without regard to the resulting performance, to modify the design of a purportedly JEDEC-compliant SDRAM so that the amount of data that the SDRAM outputs in response to any single read instruction were fixed at manufacture at some maximum value and, if a smaller amount of data were desired, to interrupt or terminate the data output in some manner.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 623:**

Admit that using a burst-EDO style protocol where each CAS pulse toggles out a single column of data, as described in Jacob, Expert Report on Synchronous DRAM Architectures, Organizations and Alternative Technologies, pages 56-61, is a technically feasible method of setting the burst length of a synchronous DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 623:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "synchronous DRAM device," "burst-EDO style protocol," "CAS pulse," "toggles out a single column of data," "technically feasible method" and "setting the burst length." Rambus further objects that the request is vague and ambiguous in that the referenced pages of the Jacob Report discuss numerous topics. Rambus further objects that the request poses an incomplete hypothetical which fails to specify, for example, the type of system in which the DRAM is to be used or its corresponding performance criteria. Rambus further objects that the request is unintelligible in its reference to using "burst-EDO style protocol" to "set[] burst length" in a "synchronous DRAM device."

**REQUEST FOR ADMISSION NO. 624:**

Admit that using an existing pin or a new, dedicated pin to identify the burst length via multiple voltage levels, as described in Jacob, Expert Report on Synchronous DRAM Architectures, Organizations and Alternative Technologies, pages 56-61, is a technically feasible method of setting the burst length of a synchronous DRAM device.

**RESPONSE TO REQUEST FOR ADMISSION NO. 624:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "synchronous DRAM device," "identify the burst length," "technically feasible method" and "setting the burst length." Rambus further objects that the request is vague

and ambiguous in that the referenced pages of the Jacob Report discuss numerous topics. Rambus further objects that the request is compound. Rambus further objects that the request poses an incomplete hypothetical which fails to specify, for example, the type of system in which the DRAM is to be used or its corresponding performance criteria.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 625:**

Admit that, for synchronous DRAM, there is at least one technically feasible method or technology, in addition to the use of a PLL or a DLL on the DRAM, that can be used to ensure that the data strobe and data coming off of a DRAM chip is sufficiently synchronized to the system clock so that the memory controller can capture that data.

**RESPONSE TO REQUEST FOR ADMISSION NO. 625:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "synchronous DRAM," "technically feasible method or technology," "PLL," "DLL," "the data strobe," and "sufficiently synchronized." Rambus further objects that the request poses an incomplete hypothetical which fails to specify, for example, the type of system in which the DRAM is to be used or its corresponding performance criteria.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 626:**

Admit that, for synchronous DRAM, there is at least one technically feasible method or technology, in addition to that required by the JEDEC standard 21-C, that can be used to ensure that the data strobe and data coming off of a DRAM chip is sufficiently synchronized to the system clock so that the memory controller can capture that data.

**RESPONSE TO REQUEST FOR ADMISSION NO. 626:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "synchronous DRAM," "technically feasible method or technology," and "sufficiently synchronized." Rambus further objects that the request is vague and ambiguous with respect to the version and requirements of JEDEC standard 21-C at issue. Rambus also objects that the request poses an incomplete hypothetical which fails to specify, for example, the type of system in which the DRAM is to be used or its corresponding performance criteria.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 627:**

Admit that, for synchronous DRAM, there is at least one technically feasible method or technology, in addition to that currently used by JEDEC-compliant DDR SDRAM, that can be used to ensure that the data strobe and data coming off of a DRAM chip is sufficiently synchronized to the system clock so that the memory controller can capture that data.

**RESPONSE TO REQUEST FOR ADMISSION NO. 627:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "synchronous DRAM," "technically feasible method or technology," and "sufficiently synchronized." Rambus further objects that the request is vague and ambiguous with respect to the feature of JEDEC-compliant DDR SDRAM at issue and with respect to the type of JEDEC-compliant DDR SDRAM at issue. Rambus also objects that the request poses an incomplete hypothetical which fails to specify, for example, the type of system in which the DRAM is to be used or its corresponding performance criteria.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 628:**

Admit that moving the PLL/DLL circuitry to the memory controller is a technically feasible method of ensuring that the data strobe and data coming off of a DRAM chip is sufficiently synchronized to the system clock so that the memory controller can capture that data.

**RESPONSE TO REQUEST FOR ADMISSION NO. 628:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "PLL/DLL circuitry," "the memory controller," "technically feasible method," "the data strobe," and "sufficiently synchronized." Rambus further objects that the request poses an incomplete hypothetical which fails to specify, for example, the type of system in which the DRAM is to be used or its corresponding performance criteria.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 629:**

Admit that moving the PLL/DLL circuitry to each DIMM is a technically feasible method of ensuring that the data strobe and data coming off of a DRAM chip is sufficiently synchronized to the system clock so that the memory controller can capture that data.

**RESPONSE TO REQUEST FOR ADMISSION NO. 629:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "PLL/DLL circuitry," "each DIMM," "technically feasible method," "the data strobe," and "sufficiently synchronized." Rambus further objects that the request poses an incomplete hypothetical which fails to specify, for example, the type of system in which the DRAM is to be used or its corresponding performance criteria.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 630:**

Admit that using a periodic calibration technique (sometimes called vernier) is a technically feasible method of ensuring that the data strobe and data coming off of a DRAM chip is sufficiently synchronized to the system clock so that the memory controller can capture that data.

**RESPONSE TO REQUEST FOR ADMISSION NO. 630:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "periodic calibration technique," "vernier," "technically feasible method," "the data strobe," and "sufficiently synchronized." Rambus further objects that the request poses an incomplete hypothetical which fails to specify, for example, the type of system in which the DRAM is to be used or its corresponding performance criteria.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 631:**

Admit that achieving high bandwidth using more DRAM pins or module pins, not clock frequency, as described in Jacob, Expert Report on Synchronous DRAM Architectures, Organizations and Alternative Technologies, pages 65-68, is a technically feasible method of ensuring that the data strobe and data coming off of a DRAM chip is sufficiently synchronized to the system clock so that the memory controller can capture that data.

**RESPONSE TO REQUEST FOR ADMISSION NO. 631:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "more DRAM pins or module pins," "clock frequency," "technically feasible method," "the data strobe," and "sufficiently synchronized." Rambus further objects that the request is compound. Rambus further objects that the request is vague and ambiguous in that the referenced pages of the Jacob Report discuss numerous topics. Rambus further objects that the request poses an incomplete hypothetical which fails to specify, for example, the type of

system in which the DRAM is to be used or its corresponding performance criteria.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 632:**

Admit that using a vernier method to measure and account for dynamic changes in skew, as described in Jacob, Expert Report on Synchronous DRAM Architectures, Organizations and Alternative Technologies, pages 65-68, is a technically feasible method of ensuring that the data strobe and data coming off of a DRAM chip is sufficiently synchronized to the system clock so that the memory controller can capture that data.

**RESPONSE TO REQUEST FOR ADMISSION NO. 632:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "vernier method," "dynamic changes in skew," "technically feasible method," "the data strobe," and "sufficiently synchronized." Rambus further objects that the request is vague and ambiguous in that the referenced pages of the Jacob Report discuss numerous topics. Rambus further objects that the request poses an incomplete hypothetical which fails to specify, for example, the type of system in which the DRAM is to be used or its corresponding performance criteria.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 633:**

Admit that putting the DLL on the memory controller, as described in Jacob, Expert Report on Synchronous DRAM Architectures, Organizations and Alternative Technologies, pages 65-68, is a technically feasible method of ensuring that the data strobe and data coming off of a DRAM chip is sufficiently synchronized to the system clock so that the memory controller can capture that data.

**RESPONSE TO REQUEST FOR ADMISSION NO. 633:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "DLL," "the memory controller," "technically feasible method," "the data strobe," and "sufficiently synchronized." Rambus further objects that the request is vague and ambiguous in that the referenced pages of the Jacob Report discuss numerous topics. Rambus further objects that the request poses an incomplete hypothetical which fails to specify, for example, the type of system in which the DRAM is to be used or its corresponding performance criteria.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 634:**

Admit that use of off-chip (on-module) DLLs, as described in Jacob, Expert Report on Synchronous DRAM Architectures, Organizations and Alternative Technologies, pages 65-68, is a technically feasible method of ensuring that the data strobe and data coming off of a DRAM chip is sufficiently synchronized to the system clock so that the memory controller can capture that data.

**RESPONSE TO REQUEST FOR ADMISSION NO. 634:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "off-chip (on module)," "DLLs," "technically feasible method," "the data strobe," and "sufficiently synchronized." Rambus further objects that the request is vague and ambiguous in that the referenced pages of the Jacob Report discuss numerous topics. Rambus further objects that the request poses an incomplete hypothetical which fails to specify, for example, the type of system in which the DRAM is to be used or its corresponding performance criteria.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 635:**

Admit that use of asynchronous DRAM, as described in Jacob, Expert Report on Synchronous DRAM Architectures, Organizations and Alternative Technologies, pages 65-68, is a technically feasible method of ensuring that the data strobe and data coming off of a DRAM chip is sufficiently synchronized to the system clock so that the memory controller can capture that data.

**RESPONSE TO REQUEST FOR ADMISSION NO. 635:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "asynchronous DRAM," "technically feasible method," "the data strobe," and "sufficiently synchronized." Rambus further objects that the request is vague and ambiguous in that the referenced pages of the Jacob Report discuss numerous topics. Rambus further objects that the request poses an incomplete hypothetical which fails to specify, for example, the type of system in which the DRAM is to be used or its corresponding performance criteria. Rambus further objects that the request is unintelligible in its reference to "asynchronous DRAM" being used to "synchronize[]" a "data strobe" and "data" to a "system clock."

**REQUEST FOR ADMISSION NO. 636:**

Admit that, for synchronous DRAM, there is at least one technically feasible method or technology, in addition to dual-edged clocking, that can be used to increase the bandwidth of DRAM systems beyond that of PC-133 SDRAM.

**RESPONSE TO REQUEST FOR ADMISSION NO. 636:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "synchronous DRAM," "dual-edged clocking," "DRAM systems," and "technically feasible method or technology." Rambus further objects that the request is vague and ambiguous because the bandwidth available from memory in a system is a product of

numerous factors other than whether the memory is "PC-133 SDRAM," and that different types of PC-133 SDRAM can lead to different memory bandwidth even in a given system. Rambus further objects that the request poses an incomplete hypothetical; methods of increasing bandwidth that are possible in one system may not be possible in another.

**REQUEST FOR ADMISSION NO. 637:**

Admit that, for synchronous DRAM, there is at least one technically feasible method or technology, in addition to that required by the JEDEC standard 21-C, that can be used to increase the bandwidth of DRAM systems beyond that of PC-133 SDRAM.

**RESPONSE TO REQUEST FOR ADMISSION NO. 637:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "synchronous DRAM," "DRAM systems," and "technically feasible method or technology." Rambus further objects that the request is vague and ambiguous with respect to the version and requirements of JEDEC standard 21-C at issue. Rambus further objects that the request is vague and ambiguous because the bandwidth available from memory in a system is a product of numerous factors other than whether the memory is "PC-133 SDRAM," and that different types of PC-133 SDRAM can lead to different memory bandwidth even in a given system. Rambus further objects that the request poses an incomplete hypothetical; methods of increasing bandwidth that are possible in one system may not be possible in another.

**REQUEST FOR ADMISSION NO. 638:**

Admit that, for synchronous DRAM, there is at least one technically feasible method or technology, in addition to that currently used by JEDEC-compliant DDR SDRAM, that can be used to increase the bandwidth of DRAM systems beyond that of PC-133 SDRAM.

**RESPONSE TO REQUEST FOR ADMISSION NO. 638:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least

with respect to the terms "synchronous DRAM," "DRAM systems," and "technically feasible method or technology." Rambus further objects that the request is vague and ambiguous with respect to the feature of JEDEC-compliant SDRAM and DDR SDRAM at issue and with respect to the type of JEDEC-compliant SDRAM or DDR SDRAM at issue. Rambus further objects that the request is vague and ambiguous because the bandwidth available from memory in a system is a product of numerous factors other than whether the memory is "PC-133 SDRAM," and that different types of PC-133 SDRAM can lead to different memory bandwidth even in a given system. Rambus further objects that the request poses an incomplete hypothetical; methods of increasing bandwidth that are possible in one system may not be possible in another.

**REQUEST FOR ADMISSION NO. 639:**

Admit that increasing the speed at which DRAMs could operate is a technically feasible method that can be used to increase the bandwidth of DRAM systems beyond that of PC-133 SDRAM.

**RESPONSE TO REQUEST FOR ADMISSION NO. 639:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "increasing the speed at which DRAMs could operate," "DRAM systems," and "technically feasible method." Rambus further objects that the request is vague and ambiguous because the bandwidth available from memory in a system is a product of numerous factors other than whether the memory is "PC-133 SDRAM," and that different types of PC-133 SDRAM can lead to different memory bandwidth even in a given system. Rambus further objects that the request poses an incomplete hypothetical; methods of increasing bandwidth that are possible in one system may not be possible in another.

**REQUEST FOR ADMISSION NO. 640:**

Admit that interleaving data between different DIMMs onto the same data bus is a technically feasible method that can be used to increase the bandwidth of DRAM systems

beyond that of PC-133 SDRAM.

**RESPONSE TO REQUEST FOR ADMISSION NO. 640:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "interleaving data between different DIMMs onto the same data bus," "DRAM systems," and "technically feasible method." Rambus further objects that the request is vague and ambiguous because the bandwidth available from memory in a system is a product of numerous factors other than whether the memory is "PC-133 SDRAM," and that different types of PC-133 SDRAM can lead to different memory bandwidth even in a given system. Rambus further objects that the request poses an incomplete hypothetical; methods of increasing bandwidth that are possible in one system may not be possible in another.

**REQUEST FOR ADMISSION NO. 641:**

Admit that interleaving data between different banks on each DRAM onto the same data bus is a technically feasible method that can be used to increase the bandwidth of DRAM systems beyond that of PC-133 SDRAM.

**RESPONSE TO REQUEST FOR ADMISSION NO. 641:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "interleaving data between different banks on each DRAM onto the same data bus," "DRAM systems," and "technically feasible method." Rambus further objects that the request is vague and ambiguous because the bandwidth available from memory in a system is a product of numerous factors other than whether the memory is "PC-133 SDRAM," and that different types of PC-133 SDRAM can lead to different memory bandwidth even in a given system. Rambus further objects that the request poses an incomplete hypothetical; methods of increasing bandwidth that are possible in one system may not be possible in another.

**REQUEST FOR ADMISSION NO. 642:**

Admit that increasing the width of the data bus is a technically feasible method that can

be used to increase the bandwidth of DRAM systems beyond that of PC-133 SDRAM.

**RESPONSE TO REQUEST FOR ADMISSION NO. 642:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "increasing the width of the data bus," "DRAM systems," and "technically feasible method." Rambus further objects that the request is vague and ambiguous because the bandwidth available from memory in a system is a product of numerous factors other than whether the memory is "PC-133 SDRAM," and that different types of PC-133 SDRAM can lead to different memory bandwidth even in a given system. Rambus further objects that the request poses an incomplete hypothetical; methods of increasing bandwidth that are possible in one system may not be possible in another.

**REQUEST FOR ADMISSION NO. 643:**

Admit that use of two or more interleaved memory banks on-chip and assign a different clock signal to each bank, as described in Jacob, Expert Report on Synchronous DRAM Architectures, Organizations and Alternative Technologies, pages 65-68, is a technically feasible method that can be used to increase the bandwidth of DRAM systems beyond that of PC-133 SDRAM.

**RESPONSE TO REQUEST FOR ADMISSION NO. 643:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "increasing the width of the data bus," "DRAM systems," and "technically feasible method." Rambus further objects that the request is vague and ambiguous because the bandwidth available from memory in a system is a product of numerous factors other than whether the memory is "PC-133 SDRAM," and that different types of PC-133 SDRAM can lead to different memory bandwidth even in a given system. Rambus further objects that the request poses an incomplete hypothetical; methods of increasing bandwidth that are possible in one system may not be possible in another.

**REQUEST FOR ADMISSION NO. 644:**

Admit that keeping each DRAM single data rate and interleaving banks on the module, as described in Jacob, Expert Report on Synchronous DRAM Architectures, Organizations and Alternative Technologies, pages 65-68, is a technically feasible method that can be used to increase the bandwidth of DRAM systems beyond that of PC-133 SDRAM.

**RESPONSE TO REQUEST FOR ADMISSION NO. 644:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "keeping each DRAM single data rate," "interleaving banks on the module," "DRAM systems," and "technically feasible method." Rambus further objects that the request is vague and ambiguous in that the referenced pages of the Jacob Report discuss numerous topics, but do not appear to discuss any type of "interleaving." Rambus further objects that the request is vague and ambiguous because the bandwidth available from memory in a system is a product of numerous factors other than whether the memory is "PC-133 SDRAM," and that different types of PC-133 SDRAM can lead to different memory bandwidth even in a given system. Rambus further objects that the request poses an incomplete hypothetical; methods of increasing bandwidth that are possible in one system may not be possible in another.

**REQUEST FOR ADMISSION NO. 645:**

Admit that increasing the number of pins per DRAM, as described in Jacob, Expert Report on Synchronous DRAM Architectures, Organizations and Alternative Technologies, pages 65-68, is a technically feasible method that can be used to increase the bandwidth of DRAM systems beyond that of PC-133 SDRAM.

**RESPONSE TO REQUEST FOR ADMISSION NO. 645:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "increasing the number of pins per DRAM," "DRAM systems," and "technically feasible method." Rambus further objects that the request is vague and ambiguous in that the referenced pages of the Jacob Report discuss numerous topics. Rambus further

objects that the request is vague and ambiguous because the bandwidth available from memory in a system is a product of numerous factors other than whether the memory is "PC-133 SDRAM," and that different types of PC-133 SDRAM can lead to different memory bandwidth even in a given system. Rambus further objects that the request poses an incomplete hypothetical; methods of increasing bandwidth that are possible in one system may not be possible in another.

**REQUEST FOR ADMISSION NO. 646:**

Admit that increasing the number of pins per module, as described in Jacob, Expert Report on Synchronous DRAM Architectures, Organizations and Alternative Technologies, pages 65-68, is a technically feasible method that can be used to increase the bandwidth of DRAM systems beyond that of PC-133 SDRAM.

**RESPONSE TO REQUEST FOR ADMISSION NO. 646:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "increasing the number of pins per module," "DRAM systems," and "technically feasible method." Rambus further objects that the request is vague and ambiguous in that the referenced pages of the Jacob Report discuss numerous topics. Rambus further objects that the request is vague and ambiguous because the bandwidth available from memory in a system is a product of numerous factors other than whether the memory is "PC-133 SDRAM," and that different types of PC-133 SDRAM can lead to different memory bandwidth even in a given system. Rambus further objects that the request poses an incomplete hypothetical; methods of increasing bandwidth that are possible in one system may not be possible in another.

**REQUEST FOR ADMISSION NO. 647:**

Admit that doubling the clock frequency, as described in Jacob, Expert Report on Synchronous DRAM Architectures, Organizations and Alternative Technologies, pages 65-68, is

a technically feasible method that can be used to increase the bandwidth of DRAM systems beyond that of PC-133 SDRAM.

**RESPONSE TO REQUEST FOR ADMISSION NO. 647:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "doubling the clock frequency," "DRAM systems," and "technically feasible method." Rambus further objects that the request is vague and ambiguous in that the referenced pages of the Jacob Report discuss numerous topics, but do not appear to discuss "doubling the clock frequency." Rambus further objects that the request is vague and ambiguous because the bandwidth available from memory in a system is a product of numerous factors other than whether the memory is "PC-133 SDRAM," and that different types of PC-133 SDRAM can lead to different memory bandwidth even in a given system. Rambus further objects that the request poses an incomplete hypothetical; methods of increasing bandwidth that are possible in one system may not be possible in another.

**REQUEST FOR ADMISSION NO. 648:**

Admit that use of simultaneous bidirectional I/O drivers, as described in Jacob, Expert Report on Synchronous DRAM Architectures, Organizations and Alternative Technologies, pages 65-68, is a technically feasible method that can be used to increase the bandwidth of DRAM systems beyond that of PC-133 SDRAM.

**RESPONSE TO REQUEST FOR ADMISSION NO. 648:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "simultaneous bidirectional I/O drivers," "DRAM systems," and "technically feasible method." Rambus further objects that the request is vague and ambiguous in that the referenced pages of the Jacob Report discuss numerous topics. Rambus further objects that the request is vague and ambiguous because the bandwidth available from memory in a system is a product of numerous factors other than whether the memory is "PC-133 SDRAM," and that different types of PC-133 SDRAM can lead to different memory bandwidth

even in a given system. Rambus further objects that the request poses an incomplete hypothetical; methods of increasing bandwidth that are possible in one system may not be possible in another.

**REQUEST FOR ADMISSION NO. 649:**

Admit that use of toggle mode, as described in Jacob, Expert Report on Synchronous DRAM Architectures, Organizations and Alternative Technologies, pages 65-68, is a technically feasible method that can be used to increase the bandwidth of DRAM systems beyond that of PC-133 SDRAM.

**RESPONSE TO REQUEST FOR ADMISSION NO. 649:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "toggle mode," "DRAM systems," and "technically feasible method." Rambus further objects that the request is vague and ambiguous in that the referenced pages of the Jacob Report discuss numerous topics. Rambus further objects that the request is vague and ambiguous because the bandwidth available from memory in a system is a product of numerous factors other than whether the memory is "PC-133 SDRAM," and that different types of PC-133 SDRAM can lead to different memory bandwidth even in a given system. Rambus further objects that the request poses an incomplete hypothetical; methods of increasing bandwidth that are possible in one system may not be possible in another.

**REQUEST FOR ADMISSION NO. 650:**

Admit that Rambus has been able to increase the price that its licensees must pay to incorporate some technologies into synchronous DRAM, over what those licensees were paying prior to their license with Rambus.

**RESPONSE TO REQUEST FOR ADMISSION NO. 650:**

Rambus objects to this request as vague and ambiguous at least with respect to the terms "the price that its licensees must pay to incorporate some technologies," "some technologies,"

"synchronous DRAM," and "what those licensees were paying prior to their license with Rambus." The request is also unintelligible. For example, the phrase "the price that its licensees must pay to incorporate some technologies" could refer to licensing fees paid to Rambus. This interpretation renders the request unintelligible, however, because the request later compares this "price" to "what those licensees were paying prior to their license with Rambus" and therefore, apparently, cannot refer to licensing fees. To the extent "the price that its licensees must pay to incorporate some technologies" is meant to refer to design, implementation, or manufacturing costs, there is no reason to believe an increase in such costs would be related to a change in status due to entering into a license with Rambus. To the contrary, the cost of incorporation of certain technology could be reduced due to the transfer of Rambus know-how. In any event, to the extent that the request is referring to design, implementation, or manufacturing costs, Rambus does not possess, and would be unable to obtain after reasonable inquiry, data concerning DRAM manufacturers' costs before and after some of those manufacturers began paying a licensing fee to Rambus that would be sufficient for Rambus to admit or deny the request.

**REQUEST FOR ADMISSION NO. 651:**

Admit that Rambus's ability to increase the price that its licensees must pay to incorporate some technologies into synchronous DRAM, over what those licensees were paying prior to their license with Rambus, is the result of patents claiming priority back to the '898 patent application filed by Rambus in April of 1990.

**RESPONSE TO REQUEST FOR ADMISSION NO. 651:**

Rambus incorporates its response to Request No. 650 and otherwise denies this request, except that Rambus admits that a portion of the licensing fee paid by Rambus licensees for the use of Rambus intellectual property in SDRAMs and DDR SDRAMs results from licensing rights to patents that claim priority back to Rambus's '898 patent application, which was filed in April of 1990.

**REQUEST FOR ADMISSION NO. 652:**

Admit that Rambus has been able to increase the price that its licensees must pay to incorporate programmable CAS latency into synchronous DRAM, over what those licensees were paying prior to their license with Rambus.

**RESPONSE TO REQUEST FOR ADMISSION NO. 652:**

Rambus objects to this request as vague and ambiguous at least with respect to the terms "the price that its licensees must pay to incorporate programmable CAS latency," "programmable CAS latency," "synchronous DRAM," and "what those licensees were paying prior to their license with Rambus." The request is also unintelligible. For example, the phrase "the price that its licensees must pay to incorporate programmable CAS latency" could refer to licensing fees paid to Rambus. This interpretation renders the request unintelligible, however, because the request later compares this "price" to "what those licensees were paying prior to their license with Rambus" and therefore, apparently, cannot refer to licensing fees. To the extent "the price that its licensees must pay to incorporate programmable CAS latency" is meant to refer to design, implementation, or manufacturing costs, there is no reason to believe an increase in such costs would be related to a change in status due to entering into a license with Rambus. To the contrary, the cost of incorporation of certain technology could be reduced due to the transfer of Rambus know-how. In any event, to the extent that the request is referring to design, implementation, or manufacturing costs, Rambus does not possess, and would be unable to obtain after reasonable inquiry, data concerning DRAM manufacturers' costs before and after some of those manufacturers began paying a licensing fee to Rambus that would be sufficient for Rambus to admit or deny the request.

**REQUEST FOR ADMISSION NO. 653:**

Admit that Rambus's ability to increase the price that its licensees must pay to incorporate programmable CAS latency into synchronous DRAM, over what those licensees

were paying prior to their license with Rambus, is the result of patents claiming priority back to the '898 patent application filed by Rambus in April of 1990.

**RESPONSE TO REQUEST FOR ADMISSION NO. 653:**

Rambus incorporates its response to Request No. 652 and otherwise denies this request, except that Rambus admits that a portion of the licensing fee paid by Rambus licensees for the use of Rambus intellectual property in SDRAMs and DDR SDRAMs results from licensing rights to patents that claim priority back to Rambus's '898 patent application, which was filed in April of 1990.

**REQUEST FOR ADMISSION NO. 654:**

Admit that Rambus has been able to increase the price that its licensees must pay to incorporate programmable burst length into synchronous DRAM, over what those licensees were paying prior to their license with Rambus.

**RESPONSE TO REQUEST FOR ADMISSION NO. 654:**

Rambus objects to this request as vague and ambiguous at least with respect to the terms "the price that its licensees must pay to incorporate programmable burst length," "programmable burst length," "synchronous DRAM," and "what those licensees were paying prior to their license with Rambus." The request is also unintelligible. For example, the phrase "the price that its licensees must pay to incorporate programmable burst length" could refer to licensing fees paid to Rambus. This interpretation renders the request unintelligible, however, because the request later compares this "price" to "what those licensees were paying prior to their license with Rambus" and therefore, apparently, cannot refer to licensing fees. To the extent "the price that its licensees must pay to incorporate programmable burst length" is meant to refer to design, implementation, or manufacturing costs, there is no reason to believe an increase in such costs would be related to a change in status due to entering into a license with Rambus. To the contrary, the cost of incorporation of certain technology could be reduced due to the transfer of Rambus know-how. In any event, to the extent that the request is referring to design,

implementation, or manufacturing costs, Rambus does not possess, and would be unable to obtain after reasonable inquiry, data concerning DRAM manufacturers' costs before and after some of those manufacturers began paying a licensing fee to Rambus that would be sufficient for Rambus to admit or deny the request.

**REQUEST FOR ADMISSION NO. 655:**

Admit that Rambus's ability to increase the price that its licensees must pay to incorporate programmable burst length into synchronous DRAM, over what those licensees were paying prior to their license with Rambus, is the result of patents claiming priority back to the '898 patent application filed by Rambus in April of 1990.

**RESPONSE TO REQUEST FOR ADMISSION NO. 655:**

Rambus incorporates its response to Request No. 654 and otherwise denies this request, except that Rambus admits that a portion of the licensing fee paid by Rambus licensees for the use of Rambus intellectual property in SDRAMs and DDR SDRAMs results from licensing rights to patents that claim priority back to Rambus's '898 patent application, which was filed in April of 1990.

**REQUEST FOR ADMISSION NO. 656:**

Admit that Rambus has been able to increase the price that its licensees must pay to incorporate the combination of programmable CAS latency and programmable burst length into synchronous DRAM, over what those licensees were paying prior to their license with Rambus.

**RESPONSE TO REQUEST FOR ADMISSION NO. 656:**

Rambus objects to this request as vague and ambiguous at least with respect to the terms "the price that its licensees must pay to incorporate the combination of programmable CAS latency and programmable burst length," "programmable CAS latency," "programmable burst length," "synchronous DRAM," and "what those licensees were paying prior to their license with Rambus." The request is also unintelligible. For example, the phrase "the price that its licensees

must pay to incorporate the combination of programmable CAS latency and programmable burst length" could refer to licensing fees paid to Rambus. This interpretation renders the request unintelligible, however, because the request later compares this "price" to "what those licensees were paying prior to their license with Rambus" and therefore, apparently, cannot refer to licensing fees. To the extent "the price that its licensees must pay to incorporate the combination of programmable CAS latency and programmable burst length" is meant to refer to design, implementation, or manufacturing costs, there is no reason to believe an increase in such costs would be related to a change in status due to entering into a license with Rambus. To the contrary, the cost of incorporation of certain technology could be reduced due to the transfer of Rambus know-how. In any event, to the extent that the request is referring to design, implementation, or manufacturing costs, Rambus does not possess, and would be unable to obtain after reasonable inquiry, data concerning DRAM manufacturers' costs before and after some of those manufacturers began paying a licensing fee to Rambus that would be sufficient for Rambus to admit or deny the request.

**REQUEST FOR ADMISSION NO. 657:**

Admit that Rambus's ability to increase the price that its licensees must pay to incorporate the combination of programmable CAS latency and programmable burst length into synchronous DRAM, over what those licensees were paying prior to their license with Rambus, is the result of patents claiming priority back to the '898 patent application filed by Rambus in April of 1990.

**RESPONSE TO REQUEST FOR ADMISSION NO. 657:**

Rambus incorporates its response to Request No. 656 and otherwise denies this request, except that Rambus admits that a portion of the licensing fee paid by Rambus licensees for the use of Rambus intellectual property in SDRAMs and DDR SDRAMs results from licensing rights to patents that claim priority back to Rambus's '898 patent application, which was filed in April of 1990.

**REQUEST FOR ADMISSION NO. 658:**

Admit that Rambus has been able to increase the price that its licensees must pay to incorporate the ability of synchronous DRAM to operate on both edges of a clock, over what those licensees were paying prior to their license with Rambus.

**RESPONSE TO REQUEST FOR ADMISSION NO. 658:**

Rambus objects to this request as vague and ambiguous at least with respect to the terms "the price that its licensees must pay to incorporate the ability of synchronous DRAM to operate on both edges of a clock," "ability to operate on both edges of a clock," "synchronous DRAM," and "what those licensees were paying prior to their license with Rambus." The request is also unintelligible. For example, the phrase "the price that its licensees must pay to incorporate the ability of synchronous DRAM to operate on both edges of a clock" could refer to licensing fees paid to Rambus. This interpretation renders the request unintelligible, however, because the request later compares this "price" to "what those licensees were paying prior to their license with Rambus" and therefore, apparently, cannot refer to licensing fees. To the extent "the price that its licensees must pay to incorporate the ability of synchronous DRAM to operate on both edges of a clock" is meant to refer to design, implementation, or manufacturing costs, there is no reason to believe an increase in such costs would be related to a change in status due to entering into a license with Rambus. To the contrary, the cost of incorporation of certain technology could be reduced due to the transfer of Rambus know-how. In any event, to the extent that the request is referring to design, implementation, or manufacturing costs, Rambus does not possess, and would be unable to obtain after reasonable inquiry, data concerning DRAM manufacturers' costs before and after some of those manufacturers began paying a licensing fee to Rambus that would be sufficient for Rambus to admit or deny the request.

**REQUEST FOR ADMISSION NO. 659:**

Admit that Rambus's ability to increase the price that its licensees must pay to

incorporate the ability of synchronous DRAM to operate on both edges of a clock, over what those licensees were paying prior to their license with Rambus, is the result of patents claiming priority back to the '898 patent application filed by Rambus in April of 1990.

**RESPONSE TO REQUEST FOR ADMISSION NO. 659:**

Rambus incorporates its response to Request No. 658 and otherwise denies this request, except that Rambus admits that a portion of the licensing fee paid by Rambus licensees for the use of Rambus intellectual property in SDRAMs and DDR SDRAMs results from licensing rights to patents that claim priority back to Rambus's '898 patent application, which was filed in April of 1990.

**REQUEST FOR ADMISSION NO. 660:**

Admit that Rambus has been able to increase the price that its licensees must pay to incorporate a PLL or a DLL onto synchronous DRAM, over what those licensees were paying prior to their license with Rambus.

**RESPONSE TO REQUEST FOR ADMISSION NO. 660:**

Rambus objects to this request as vague and ambiguous at least with respect to the terms "the price that its licensees must pay to incorporate a PLL or a DLL," "PLL," "DLL," "synchronous DRAM," and "what those licensees were paying prior to their license with Rambus." The request is also unintelligible. For example, the phrase "the price that its licensees must pay to incorporate a PLL or a DLL" could refer to licensing fees paid to Rambus. This interpretation renders the request unintelligible, however, because the request later compares this "price" to "what those licensees were paying prior to their license with Rambus" and therefore, apparently, cannot refer to licensing fees. To the extent "the price that its licensees must pay to incorporate a PLL or a DLL" is meant to refer to design, implementation, or manufacturing costs, there is no reason to believe an increase in such costs would be related to a change in status due to entering into a license with Rambus. To the contrary, the cost of incorporation of certain technology could be reduced due to the transfer of Rambus know-how. In any event, to

the extent that the request is referring to design, implementation, or manufacturing costs, Rambus does not possess, and would be unable to obtain after reasonable inquiry, data concerning DRAM manufacturers' costs before and after some of those manufacturers began paying a licensing fee to Rambus that would be sufficient for Rambus to admit or deny the request.

**REQUEST FOR ADMISSION NO. 661:**

Admit that Rambus's ability to increase the price that its licensees must pay to incorporate a PLL or a DLL onto synchronous DRAM, over what those licensees were paying prior to their license with Rambus, is the result of patents claiming priority back to the '898 patent application filed by Rambus in April of 1990.

**RESPONSE TO REQUEST FOR ADMISSION NO. 661:**

Rambus incorporates its response to Request No. 660 and otherwise denies this request, except that Rambus admits that a portion of the licensing fee paid by Rambus licensees for the use of Rambus intellectual property in SDRAMs and DDR SDRAMs results from licensing rights to patents that claim priority back to Rambus's '898 patent application, which was filed in April of 1990.

**REQUEST FOR ADMISSION NO. 662:**

Admit that Rambus has been able to increase the price that its licensees must pay, over what those licensees were paying prior to their license with Rambus, to incorporate the combination of the following technologies onto synchronous DRAM: programmable CAS latency, programmable burst length, the ability of synchronous DRAM to operate on both edges of a clock, and the ability to incorporate a PLL or a DLL.

**RESPONSE TO REQUEST FOR ADMISSION NO. 662:**

Rambus objects to this request as vague and ambiguous at least with respect to the terms "the price that its licensees must pay to incorporate the combination of . . . programmable CAS

latency, programmable burst length, the ability of synchronous DRAM to operate on both edges of a clock, and the ability to incorporate a PLL or a DLL," "programmable CAS latency," "programmable burst length," "ability . . . to operate on both edges of a clock," "ability to incorporate a PLL or a DLL," "PLL," "DLL," "synchronous DRAM," and "what those licensees were paying prior to their license with Rambus." The request is also unintelligible. For example, the phrase "the price that its licensees must pay to incorporate the combination of . . . programmable CAS latency, programmable burst length, the ability of synchronous DRAM to operate on both edges of a clock, and the ability to incorporate a PLL or a DLL" could refer to licensing fees paid to Rambus. This interpretation renders the request unintelligible, however, because the request later compares this "price" to "what those licensees were paying prior to their license with Rambus" and therefore, apparently, cannot refer to licensing fees. To the extent "the price that its licensees must pay to incorporate the combination of . . . programmable CAS latency, programmable burst length, the ability of synchronous DRAM to operate on both edges of a clock, and the ability to incorporate a PLL or a DLL" is meant to refer to design, implementation, or manufacturing costs, there is no reason to believe an increase in such costs would be related to a change in status due to entering into a license with Rambus. To the contrary, the cost of incorporation of certain technology could be reduced due to the transfer of Rambus know-how. In any event, to the extent that the request is referring to design, implementation, or manufacturing costs, Rambus does not possess, and would be unable to obtain after reasonable inquiry, data concerning DRAM manufacturers' costs before and after some of those manufacturers began paying a licensing fee to Rambus that would be sufficient for Rambus to admit or deny the request.

**REQUEST FOR ADMISSION NO. 663:**

Admit that Rambus's ability to increase the price that its licensees must pay, over what those licensees were paying prior to their license with Rambus, to incorporate the combination of the following technologies onto synchronous DRAM: programmable CAS latency,

programmable burst length, the ability of synchronous DRAM to operate on both edges of a clock, and the ability to incorporate a PLL or a DLL, is the result of patents claiming priority back to the '898 patent application filed by Rambus in April of 1990.

**RESPONSE TO REQUEST FOR ADMISSION NO. 663:**

Rambus incorporates its response to Request No. 662 and otherwise denies this request, except that Rambus admits that a portion of the licensing fee paid by Rambus licensees for the use of Rambus intellectual property in SDRAMs and DDR SDRAMs results from licensing rights to patents that claim priority back to Rambus's '898 patent application, which was filed in April of 1990.

**REQUEST FOR ADMISSION NO. 664:**

Admit that, if Rambus wins its patent suits, it will have the power to raise the price of some technologies incorporated in synchronous DRAM.

**RESPONSE TO REQUEST FOR ADMISSION NO. 664:**

Rambus objects to this request as vague and ambiguous, at least with respect to the terms "its patent suits," "power," "price of some technologies," and "synchronous DRAM."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that if its patents are ultimately held infringed and not invalid in the litigations between it and Infineon, Hynix and Micron, and other defenses to patent infringement are not upheld, Rambus would have the legal right to exclude those companies from making, using, or selling certain synchronous DRAMs containing certain Rambus intellectual property. Rambus notes that those companies already have the right, by way of licenses with Rambus, to incorporate Rambus intellectual property into certain types of synchronous DRAM known as Direct RDRAM.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 665:**

Admit that, if Rambus wins its patent suits, its ability to raise the price of some technologies incorporated in synchronous DRAM will be the result of patents claiming priority back to the '898 patent application filed by Rambus in April of 1990.

**RESPONSE TO REQUEST FOR ADMISSION NO. 665:**

Rambus incorporates its response to Request No. 664 and denies the remainder of this request, except that Rambus admits that a portion of the licensing fee paid by Rambus licensees for the use of Rambus intellectual property in SDRAMs and DDR SDRAMs results from licensing rights to patents that claim priority back to Rambus's '898 patent application, which was filed in April of 1990.

**REQUEST FOR ADMISSION NO. 666:**

Admit that, if Rambus wins its patent suits, it will have the power to raise the price DRAM manufacturers must pay to incorporate programmable CAS latency into synchronous DRAM containing that feature.

**RESPONSE TO REQUEST FOR ADMISSION NO. 666:**

Rambus objects to this request as vague and ambiguous, at least with respect to the terms "its patent suits," "power," "price DRAM manufacturers must pay," "programmable CAS latency," and "synchronous DRAM."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that if its patents are ultimately held infringed and not invalid in the litigations between it and Infineon, Hynix and Micron, and other defenses to patent infringement are not upheld, Rambus would have the legal right to exclude those companies from making, using, or selling certain synchronous DRAMs containing certain Rambus intellectual property. Rambus notes that those companies already have the right, by way of licenses with Rambus, to incorporate Rambus intellectual property into certain types of synchronous DRAM known as Direct RDRAM.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 667:**

Admit that, if Rambus wins its patent suits, its ability to raise the price DRAM manufacturers must pay to incorporate programmable CAS latency in synchronous DRAM will be the result of patents claiming priority back to the '898 patent application filed by Rambus in April of 1990.

**RESPONSE TO REQUEST FOR ADMISSION NO. 667:**

Rambus incorporates its response to Request No. 666 and denies the remainder of this request, except that Rambus admits that a portion of the licensing fee paid by Rambus licensees for the use of Rambus intellectual property in SDRAMs and DDR SDRAMs results from licensing rights to patents that claim priority back to Rambus's '898 patent application, which was filed in April of 1990.

**REQUEST FOR ADMISSION NO. 668:**

Admit that, if Rambus wins its patent suits, it will have the power to raise the price DRAM manufacturers must pay to incorporate programmable burst length into synchronous DRAM containing that feature.

**RESPONSE TO REQUEST FOR ADMISSION NO. 668:**

Rambus objects to this request as vague and ambiguous, at least with respect to the terms "its patent suits," "power," "price DRAM manufacturers must pay," "programmable burst length," and "synchronous DRAM."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that if its patents are ultimately held infringed and not invalid in the litigations between it and Infineon, Hynix and Micron, and other defenses to patent infringement are not upheld, Rambus would have the legal right to exclude those companies from making, using, or selling certain synchronous DRAMs containing certain Rambus intellectual property.

Rambus notes that those companies already have the right, by way of licenses with Rambus, to incorporate Rambus intellectual property into certain types of synchronous DRAM known as Direct RDRAM.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 669:**

Admit that, if Rambus wins its patent suits, its ability to raise the price DRAM manufacturers must pay to incorporate programmable burst length in synchronous DRAM will be the result of patents claiming priority back to the '898 patent application filed by Rambus in April of 1990.

**RESPONSE TO REQUEST FOR ADMISSION NO. 669:**

Rambus incorporates its response to Request No. 668 and denies the remainder of this request, except that Rambus admits that a portion of the licensing fee paid by Rambus licensees for the use of Rambus intellectual property in SDRAMs and DDR SDRAMs results from licensing rights to patents that claim priority back to Rambus's '898 patent application, which was filed in April of 1990.

**REQUEST FOR ADMISSION NO. 670:**

Admit that, if Rambus wins its patent suits, it will have the power to raise the price DRAM manufacturers must pay to incorporate the combination of programmable CAS latency and programmable burst length into synchronous DRAM containing that feature.

**RESPONSE TO REQUEST FOR ADMISSION NO. 670:**

Rambus objects to this request as vague and ambiguous, at least with respect to the terms "its patent suits," "power," "price DRAM manufacturers must pay," "programmable CAS latency," "programmable burst length," and "synchronous DRAM."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that if its patents are ultimately held infringed and not invalid in the

litigations between it and Infineon, Hynix and Micron, and other defenses to patent infringement are not upheld, Rambus would have the legal right to exclude those companies from making, using, or selling certain synchronous DRAMs containing certain Rambus intellectual property. Rambus notes that those companies already have the right, by way of licenses with Rambus, to incorporate Rambus intellectual property into certain types of synchronous DRAM known as Direct RDRAM.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 671:**

Admit that, if Rambus wins its patent suits, its ability to raise the price DRAM manufacturers must pay to incorporate the combination of programmable CAS latency and programmable burst length into synchronous DRAM will be the result of patents claiming priority back to the '898 patent application filed by Rambus in April of 1990.

**RESPONSE TO REQUEST FOR ADMISSION NO. 671:**

Rambus incorporates its response to Request No. 670 and denies the remainder of this request, except that Rambus admits that a portion of the licensing fee paid by Rambus licensees for the use of Rambus intellectual property in SDRAMs and DDR SDRAMs results from licensing rights to patents that claim priority back to Rambus's '898 patent application, which was filed in April of 1990.

**REQUEST FOR ADMISSION NO. 672:**

Admit that, if Rambus wins its patent suits, it will have the power to raise the price DRAM manufacturers must pay to incorporate the ability of synchronous DRAM to operate on both edges of a clock on synchronous DRAM containing that feature.

**RESPONSE TO REQUEST FOR ADMISSION NO. 672:**

Rambus objects to this request as vague and ambiguous, at least with respect to the terms "its patent suits," "power," "price DRAM manufacturers must pay," "ability . . . to operate on

both edges of a clock" and "synchronous DRAM."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that if its patents are ultimately held infringed and not invalid in the litigations between it and Infineon, Hynix and Micron, and other defenses to patent infringement are not upheld, Rambus would have the legal right to exclude those companies from making, using, or selling certain synchronous DRAMs containing certain Rambus intellectual property. Rambus notes that those companies already have the right, by way of licenses with Rambus, to incorporate Rambus intellectual property into certain types of synchronous DRAM known as Direct RDRAM.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 673:**

Admit that, if Rambus wins its patent suits, its ability to raise the price DRAM manufacturers must pay to incorporate the ability of synchronous DRAM to operate on both edges of a clock will be the result of patents claiming priority back to the '898 patent application filed by Rambus in April of 1990.

**RESPONSE TO REQUEST FOR ADMISSION NO. 673:**

Rambus incorporates its response to Request No. 672 and denies the remainder of this request, except that Rambus admits that a portion of the licensing fee paid by Rambus licensees for the use of Rambus intellectual property in SDRAMs and DDR SDRAMs results from licensing rights to patents that claim priority back to Rambus's '898 patent application, which was filed in April of 1990.

**REQUEST FOR ADMISSION NO. 674:**

Admit that, if Rambus wins its patent suits, it will have the power to raise the price DRAM manufacturers must pay to incorporate a PLL or a DLL onto synchronous DRAM on synchronous DRAM containing that feature.

**RESPONSE TO REQUEST FOR ADMISSION NO. 674:**

Rambus objects to this request as vague and ambiguous, at least with respect to the terms "its patent suits," "power," "price DRAM manufacturers must pay," "PLL," "DLL," and "synchronous DRAM."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that if its patents are ultimately held infringed and not invalid in the litigations between it and Infineon, Hynix and Micron, and other defenses to patent infringement are not upheld, Rambus would have the legal right to exclude those companies from making, using, or selling certain synchronous DRAMs containing certain Rambus intellectual property. Rambus notes that those companies already have the right, by way of licenses with Rambus, to incorporate Rambus intellectual property into certain types of synchronous DRAM known as Direct RDRAM.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 675:**

Admit that, if Rambus wins its patent suits, its ability to raise the price DRAM manufacturers must pay to incorporate a PLL or a DLL onto synchronous DRAM will be the result of patents claiming priority back to the '898 patent application filed by Rambus in April of 1990.

**RESPONSE TO REQUEST FOR ADMISSION NO. 675:**

Rambus incorporates its response to Request No. 674 and denies the remainder of this request, except that Rambus admits that a portion of the licensing fee paid by Rambus licensees for the use of Rambus intellectual property in SDRAMs and DDR SDRAMs results from licensing rights to patents that claim priority back to Rambus's '898 patent application, which was filed in April of 1990.

**REQUEST FOR ADMISSION NO. 676:**

Admit that if Rambus wins its patent suits, it will have the power to raise the price DRAM manufacturers must pay to incorporate the combination of the following technologies onto synchronous DRAM: programmable CAS latency, programmable burst length, the ability of synchronous DRAM to operate on both edges of a clock, and the ability to incorporate a PLL or a DLL.

**RESPONSE TO REQUEST FOR ADMISSION NO. 676:**

Rambus objects to this request as vague and ambiguous, at least with respect to the terms "its patent suits," "power," "price DRAM manufacturers must pay," "programmable CAS latency," "programmable burst length," "ability . . . to operate on both edges of a clock," "ability to incorporate a PLL or a DLL," "PLL," "DLL," and "synchronous DRAM."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that if its patents are ultimately held infringed and not invalid in the litigations between it and Infineon, Hynix and Micron, and other defenses to patent infringement are not upheld, Rambus would have the legal right to exclude those companies from making, using, or selling certain synchronous DRAMs containing certain Rambus intellectual property. Rambus notes that those companies already have the right, by way of licenses with Rambus, to incorporate Rambus intellectual property into certain types of synchronous DRAM known as Direct RDRAM.

Rambus otherwise denies the request.

**REQUEST FOR ADMISSION NO. 677:**

Admit that if Rambus wins its patent suits, its ability to increase the price DRAM manufacturers must pay to incorporate the combination of the following technologies onto synchronous DRAM: programmable CAS latency, programmable burst length, the ability of synchronous DRAM to operate on both edges of a clock, and the ability to incorporate a PLL or a DLL, will be the result of patents claiming priority back to the '898 patent application filed by

Rambus in April of 1990.

**RESPONSE TO REQUEST FOR ADMISSION NO. 677:**

Rambus incorporates its response to Request No. 676 and denies the remainder of this request, except that Rambus admits that a portion of the licensing fee paid by Rambus licensees for the use of Rambus intellectual property in SDRAMs and DDR SDRAMs results from licensing rights to patents that claim priority back to Rambus's '898 patent application, which was filed in April of 1990.

**REQUEST FOR ADMISSION NO. 678:**

Admit that over 90%, by revenue, of all DRAM sold in 1994 was JEDEC-compliant DRAM.

**RESPONSE TO REQUEST FOR ADMISSION NO. 678:**

Rambus objects to the request as vague and ambiguous, at least with respect to the term "JEDEC-compliant DRAM."

Subject to and without waiving any objections, Rambus responds as follows:

After having made reasonable inquiry, the information known to or readily obtainable by Rambus is insufficient for Rambus to admit or deny the request.

**REQUEST FOR ADMISSION NO. 679:**

Admit that over 90%, by units shipped, of all DRAM sold in 1994 was JEDEC-compliant DRAM.

**RESPONSE TO REQUEST FOR ADMISSION NO. 679:**

Rambus objects to the request as vague and ambiguous, at least with respect to the terms "units" and "JEDEC-compliant DRAM."

Subject to and without waiving any objections, Rambus responds as follows:

After having made reasonable inquiry, the information known to or readily obtainable by Rambus is insufficient for Rambus to admit or deny the request.

**REQUEST FOR ADMISSION NO. 680:**

Admit that over 90%, by the volume of bits shipped, of all DRAM sold in 1994 was JEDEC compliant DRAM.

**RESPONSE TO REQUEST FOR ADMISSION NO. 680:**

Rambus objects to the request as vague and ambiguous, at least with respect to the term "JEDEC-compliant DRAM."

Subject to and without waiving any objections, Rambus responds as follows:

After having made reasonable inquiry, the information known to or readily obtainable by Rambus is insufficient for Rambus to admit or deny the request.

**REQUEST FOR ADMISSION NO. 681:**

Admit that over 90%, by revenue, of all DRAM sold in 1995 was JEDEC-compliant DRAM.

**RESPONSE TO REQUEST FOR ADMISSION NO. 681:**

Rambus objects to the request as vague and ambiguous, at least with respect to the term "JEDEC-compliant DRAM."

Subject to and without waiving any objections, Rambus responds as follows:

After having made reasonable inquiry, the information known to or readily obtainable by Rambus is insufficient for Rambus to admit or deny the request.

**REQUEST FOR ADMISSION NO. 682:**

Admit that over 90%, by units shipped, of all DRAM sold in 1995 was JEDEC-compliant DRAM.

**RESPONSE TO REQUEST FOR ADMISSION NO. 682:**

Rambus objects to the request as vague and ambiguous, at least with respect to the terms "units" and "JEDEC-compliant DRAM."

Subject to and without waiving any objections, Rambus responds as follows:

After having made reasonable inquiry, the information known to or readily obtainable by Rambus is insufficient for Rambus to admit or deny the request.

**REQUEST FOR ADMISSION NO. 683:**

Admit that over 90%, by the volume of bits shipped, of all DRAM sold in 1995 was JEDEC-compliant DRAM.

**RESPONSE TO REQUEST FOR ADMISSION NO. 683:**

Rambus objects to the request as vague and ambiguous, at least with respect to the term "JEDEC-compliant DRAM."

Subject to and without waiving any objections, Rambus responds as follows:

After having made reasonable inquiry, the information known to or readily obtainable by Rambus is insufficient for Rambus to admit or deny the request.

**REQUEST FOR ADMISSION NO. 684:**

Admit that over 90%, by revenue, of all DRAM sold in 1996 was JEDEC-compliant DRAM.

**RESPONSE TO REQUEST FOR ADMISSION NO. 684:**

Rambus objects to the request as vague and ambiguous, at least with respect to the term "JEDEC-compliant DRAM."

Subject to and without waiving any objections, Rambus responds as follows:

After having made reasonable inquiry, the information known to or readily obtainable by Rambus is insufficient for Rambus to admit or deny the request.

**REQUEST FOR ADMISSION NO. 685:**

Admit that over 90%, by units shipped, of all DRAM sold in 1996 was JEDEC-compliant

DRAM.

**RESPONSE TO REQUEST FOR ADMISSION NO. 685:**

Rambus objects to the request as vague and ambiguous, at least with respect to the terms "units" and "JEDEC-compliant DRAM."

Subject to and without waiving any objections, Rambus responds as follows:

After having made reasonable inquiry, the information known to or readily obtainable by Rambus is insufficient for Rambus to admit or deny the request.

**REQUEST FOR ADMISSION NO. 686:**

Admit that over 90%, by the volume of bits shipped, of all DRAM sold in 1996 was JEDEC-compliant DRAM.

**RESPONSE TO REQUEST FOR ADMISSION NO. 686:**

Rambus objects to the request as vague and ambiguous, at least with respect to the term "JEDEC-compliant DRAM."

Subject to and without waiving any objections, Rambus responds as follows:

After having made reasonable inquiry, the information known to or readily obtainable by Rambus is insufficient for Rambus to admit or deny the request.

**REQUEST FOR ADMISSION NO. 687:**

Admit that over 90%, by revenue, of all DRAM sold in 1997 was JEDEC-compliant DRAM.

**RESPONSE TO REQUEST FOR ADMISSION NO. 687:**

Rambus objects to the request as vague and ambiguous, at least with respect to the term "JEDEC-compliant DRAM."

Subject to and without waiving any objections, Rambus responds as follows:

After having made reasonable inquiry, the information known to or readily obtainable by Rambus is insufficient for Rambus to admit or deny the request.

**REQUEST FOR ADMISSION NO. 688:**

Admit that over 90%, by units shipped, of all DRAM sold in 1997 was JEDEC-compliant DRAM.

**RESPONSE TO REQUEST FOR ADMISSION NO. 688:**

Rambus objects to the request as vague and ambiguous, at least with respect to the terms "units" and "JEDEC-compliant DRAM."

Subject to and without waiving any objections, Rambus responds as follows:

After having made reasonable inquiry, the information known to or readily obtainable by Rambus is insufficient for Rambus to admit or deny the request.

**REQUEST FOR ADMISSION NO. 689:**

Admit that over 90%, by the volume of bits shipped, of all DRAM sold in 1997 was JEDEC-compliant DRAM.

**RESPONSE TO REQUEST FOR ADMISSION NO. 689:**

Rambus objects to the request as vague and ambiguous, at least with respect to the term "JEDEC-compliant DRAM."

Subject to and without waiving any objections, Rambus responds as follows:

After having made reasonable inquiry, the information known to or readily obtainable by Rambus is insufficient for Rambus to admit or deny the request.

**REQUEST FOR ADMISSION NO. 690:**

Admit that over 90%, by revenue, of all DRAM sold in 1998 was JEDEC-compliant DRAM.

**RESPONSE TO REQUEST FOR ADMISSION NO. 690:**

Rambus objects to the request as vague and ambiguous, at least with respect to the term "JEDEC-compliant DRAM."

Subject to and without waiving any objections, Rambus responds as follows:

After having made reasonable inquiry, the information known to or readily obtainable by Rambus is insufficient for Rambus to admit or deny the request.

**REQUEST FOR ADMISSION NO. 691:**

Admit that over 90%, by units shipped, of all DRAM sold in 1998 was JEDEC-compliant DRAM.

**RESPONSE TO REQUEST FOR ADMISSION NO. 691:**

Rambus objects to the request as vague and ambiguous, at least with respect to the terms "units" and "JEDEC-compliant DRAM."

Subject to and without waiving any objections, Rambus responds as follows:

After having made reasonable inquiry, the information known to or readily obtainable by Rambus is insufficient for Rambus to admit or deny the request.

**REQUEST FOR ADMISSION NO. 692:**

Admit that over 90%, by the volume of bits shipped, of all DRAM sold in 1998 was JEDEC-compliant DRAM.

**RESPONSE TO REQUEST FOR ADMISSION NO. 692:**

Rambus objects to the request as vague and ambiguous, at least with respect to the term "JEDEC-compliant DRAM."

Subject to and without waiving any objections, Rambus responds as follows:

After having made reasonable inquiry, the information known to or readily obtainable by Rambus is insufficient for Rambus to admit or deny the request.

**REQUEST FOR ADMISSION NO. 693:**

Admit that over 90%, by revenue, of all DRAM sold in 1999 was JEDEC-compliant DRAM.

**RESPONSE TO REQUEST FOR ADMISSION NO. 693:**

Rambus objects to the request as vague and ambiguous, at least with respect to the term "JEDEC-compliant DRAM."

Subject to and without waiving any objections, Rambus responds as follows:

After having made reasonable inquiry, the information known to or readily obtainable by Rambus is insufficient for Rambus to admit or deny the request.

**REQUEST FOR ADMISSION NO. 694:**

Admit that over 90%, by units shipped, of all DRAM sold in 1999 was JEDEC-compliant DRAM.

**RESPONSE TO REQUEST FOR ADMISSION NO. 694:**

Rambus objects to the request as vague and ambiguous, at least with respect to the terms "units" and "JEDEC-compliant DRAM."

Subject to and without waiving any objections, Rambus responds as follows:

After having made reasonable inquiry, the information known to or readily obtainable by Rambus is insufficient for Rambus to admit or deny the request.

**REQUEST FOR ADMISSION NO. 695:**

Admit that over 90%, by the volume of bits shipped, of all DRAM sold in 1999 was JEDEC-compliant DRAM.

**RESPONSE TO REQUEST FOR ADMISSION NO. 695:**

Rambus objects to the request as vague and ambiguous, at least with respect to the term "JEDEC-compliant DRAM."

Subject to and without waiving any objections, Rambus responds as follows:

After having made reasonable inquiry, the information known to or readily obtainable by Rambus is insufficient for Rambus to admit or deny the request.

**REQUEST FOR ADMISSION NO. 696:**

Admit that over 90%, by revenue, of all DRAM sold in 2000 was JEDEC-compliant DRAM.

**RESPONSE TO REQUEST FOR ADMISSION NO. 696:**

Rambus objects to the request as vague and ambiguous, at least with respect to the term "JEDEC-compliant DRAM."

Subject to and without waiving any objections, Rambus responds as follows:

After having made reasonable inquiry, the information known to or readily obtainable by Rambus is insufficient for Rambus to admit or deny the request.

**REQUEST FOR ADMISSION NO. 697:**

Admit that over 90%, by units shipped, of all DRAM sold in 2000 was JEDEC-compliant DRAM.

**RESPONSE TO REQUEST FOR ADMISSION NO. 697:**

Rambus objects to the request as vague and ambiguous, at least with respect to the terms "units" and "JEDEC-compliant DRAM."

Subject to and without waiving any objections, Rambus responds as follows:

After having made reasonable inquiry, the information known to or readily obtainable by Rambus is insufficient for Rambus to admit or deny the request.

**REQUEST FOR ADMISSION NO. 698:**

Admit that over 90%, by the volume of bits shipped, of all DRAM sold in 2000 was JEDEC-compliant DRAM.

**RESPONSE TO REQUEST FOR ADMISSION NO. 698:**

Rambus objects to the request as vague and ambiguous, at least with respect to the term "JEDEC-compliant DRAM."

Subject to and without waiving any objections, Rambus responds as follows:

After having made reasonable inquiry, the information known to or readily obtainable by Rambus is insufficient for Rambus to admit or deny the request.

**REQUEST FOR ADMISSION NO. 699:**

Admit that over 90%, by revenue, of all DRAM sold in 2001 was JEDEC-compliant DRAM.

**RESPONSE TO REQUEST FOR ADMISSION NO. 699:**

Rambus objects to the request as vague and ambiguous, at least with respect to the term "JEDEC-compliant DRAM."

Subject to and without waiving any objections, Rambus responds as follows:

After having made reasonable inquiry, the information known to or readily obtainable by Rambus is insufficient for Rambus to admit or deny the request.

**REQUEST FOR ADMISSION NO. 700:**

Admit that over 90%, by units shipped, of all DRAM sold in 2001 was JEDEC-compliant DRAM.

**RESPONSE TO REQUEST FOR ADMISSION NO. 700:**

Rambus objects to the request as vague and ambiguous, at least with respect to the terms "units" and "JEDEC-compliant DRAM."

Subject to and without waiving any objections, Rambus responds as follows:

After having made reasonable inquiry, the information known to or readily obtainable by Rambus is insufficient for Rambus to admit or deny the request.

**REQUEST FOR ADMISSION NO. 701:**

Admit that over 90%, by the volume of bits shipped, of all DRAM sold in 2001 was JEDEC-compliant DRAM.

**RESPONSE TO REQUEST FOR ADMISSION NO. 701:**

Rambus objects to the request as vague and ambiguous, at least with respect to the term "JEDEC-compliant DRAM."

Subject to and without waiving any objections, Rambus responds as follows:

After having made reasonable inquiry, the information known to or readily obtainable by Rambus is insufficient for Rambus to admit or deny the request.

**REQUEST FOR ADMISSION NO. 702:**

Admit that over 90%, by revenue, of all DRAM sold in 2002 was JEDEC-compliant DRAM.

**RESPONSE TO REQUEST FOR ADMISSION NO. 702:**

Rambus objects to the request as vague and ambiguous, at least with respect to the term "JEDEC-compliant DRAM."

Subject to and without waiving any objections, Rambus responds as follows:

After having made reasonable inquiry, the information known to or readily obtainable by Rambus is insufficient for Rambus to admit or deny the request.

**REQUEST FOR ADMISSION NO. 703:**

Admit that over 90%, by units shipped, of all DRAM sold in 2002 was JEDEC-compliant DRAM.

**RESPONSE TO REQUEST FOR ADMISSION NO. 703:**

Rambus objects to the request as vague and ambiguous, at least with respect to the terms "units" and "JEDEC-compliant DRAM."

Subject to and without waiving any objections, Rambus responds as follows:

After having made reasonable inquiry, the information known to or readily obtainable by Rambus is insufficient for Rambus to admit or deny the request.

**REQUEST FOR ADMISSION NO. 704:**

Admit that over 90%, by the volume of bits shipped, of all DRAM sold in 2002 was JEDEC-compliant DRAM.

**RESPONSE TO REQUEST FOR ADMISSION NO. 704:**

Rambus objects to the request as vague and ambiguous, at least with respect to the term "JEDEC-compliant DRAM."

Subject to and without waiving any objections, Rambus responds as follows:

After having made reasonable inquiry, the information known to or readily obtainable by Rambus is insufficient for Rambus to admit or deny the request.

**REQUEST FOR ADMISSION NO. 705:**

Admit that over 90%, by revenue, of all DRAM sold between 1994 and 2002 was JEDEC-compliant DRAM.

**RESPONSE TO REQUEST FOR ADMISSION NO. 705:**

Rambus objects to the request as vague and ambiguous, at least with respect to the term "JEDEC-compliant DRAM."

Subject to and without waiving any objections, Rambus responds as follows:

After having made reasonable inquiry, the information known to or readily obtainable by Rambus is insufficient for Rambus to admit or deny the request.

**REQUEST FOR ADMISSION NO. 706:**

Admit that over 90%, by units shipped, of all DRAM sold between 1994 and 2002 was JEDEC-compliant DRAM.

**RESPONSE TO REQUEST FOR ADMISSION NO. 706:**

Rambus objects to the request as vague and ambiguous, at least with respect to the terms "units" and "JEDEC-compliant DRAM."

Subject to and without waiving any objections, Rambus responds as follows:

After having made reasonable inquiry, the information known to or readily obtainable by Rambus is insufficient for Rambus to admit or deny the request.

**REQUEST FOR ADMISSION NO. 707:**

Admit that over 90%, by the volume of bits shipped, of all DRAM sold between 1994 and 2002 was JEDEC-compliant DRAM.

**RESPONSE TO REQUEST FOR ADMISSION NO. 707:**

Rambus objects to the request as vague and ambiguous, at least with respect to the term "JEDEC-compliant DRAM."

Subject to and without waiving any objections, Rambus responds as follows:

After having made reasonable inquiry, the information known to or readily obtainable by Rambus is insufficient for Rambus to admit or deny the request.

**REQUEST FOR ADMISSION NO. 708:**

Admit that Rambus bases business decisions on the projection that over 90%, by revenue, of all DRAM sold in 2003 will be JEDEC-compliant DRAM.

**RESPONSE TO REQUEST FOR ADMISSION NO. 708:**

Rambus objects to this request as vague and ambiguous, at least with respect to the terms "bases," "business decisions," and "projection."

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 709:**

Admit that Rambus bases business decisions on the projection that over 80%, by revenue, of all DRAM sold in 2004 will be JEDEC-compliant DRAM.

**RESPONSE TO REQUEST FOR ADMISSION NO. 709:**

Rambus objects to this request as vague and ambiguous, at least with respect to the terms

"bases," "business decisions," and "projection."

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 710:**

Admit that Rambus bases business decisions on the projection that over 80%, by revenue, of all DRAM sold in 2005 will be JEDEC-compliant DRAM.

**RESPONSE TO REQUEST FOR ADMISSION NO. 710:**

Rambus objects to this request as vague and ambiguous, at least with respect to the terms "bases," "business decisions," and "projection."

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 711:**

Admit that the 5,243,703 patent does not cover presentations made by various JEDEC 42.3 Subcommittee members between December 1991 through June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 711:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "cover" and "presentations." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee. In any event, to the extent that "cover" is intended to be interpreted as "infringed by," Rambus objects to the request on the ground that a patent claim cannot be infringed by a presentation.

**REQUEST FOR ADMISSION NO. 712:**

Admit that the 5,319,755 patent does not cover presentations made by various JEDEC 42.3 Subcommittee members between December 1991 through June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 712:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "cover" and "presentations." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee. In any event, to the extent that "cover" is intended to be interpreted as "infringed by," Rambus objects to the request on the ground that a patent claim cannot be infringed by a presentation.

**REQUEST FOR ADMISSION NO. 713:**

Admit that Rambus' Israeli patent does not cover presentations made by various JEDEC 42.3 Subcommittee members between December 1991 through June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 713:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "cover" and "presentations." Rambus further objects that the request is vague and ambiguous with respect to the term "Rambus' Israeli patent" since Rambus has multiple Israeli patents. Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee. In any event, to the extent that "cover" is intended to be interpreted as "infringed by," Rambus objects to the request on the ground that a patent claim cannot be infringed by a presentation.

**REQUEST FOR ADMISSION NO. 714:**

Admit that the 5,268,639 patent does not cover presentations made by various JEDEC 42.3 Subcommittee members between December 1991 through June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 714:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "cover" and "presentations." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee. In any event, to the extent that "cover" is intended to be interpreted as "infringed by," Rambus objects to the request on the ground that a patent claim cannot be infringed by a presentation.

**REQUEST FOR ADMISSION NO. 715:**

Admit that the 5,357,195 patent does not cover presentations made by various JEDEC 42.3 Subcommittee members between December 1991 through June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 715:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "cover" and "presentations." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee. In any event, to the extent that "cover" is intended to be interpreted as "infringed by," Rambus objects to the request on the ground that a patent claim cannot be infringed by a presentation.

**REQUEST FOR ADMISSION NO. 716:**

Admit that the 5,325,053 patent does not cover presentations made by various JEDEC 42.3 Subcommittee members between December 1991 through June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 716:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "cover" and "presentations." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee. In any event, to the extent that "cover" is intended to be interpreted as "infringed by," Rambus objects to the request on the ground that a patent claim cannot be infringed by a presentation.

**REQUEST FOR ADMISSION NO. 717:**

Admit that the 5,422,529 patent does not cover presentations made by various JEDEC 42.3 Subcommittee members between December 1991 through June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 717:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "cover" and "presentations." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee. In any event, to the extent that "cover" is intended to be interpreted as "infringed by," Rambus objects to the request on the ground that a patent claim cannot be infringed by a presentation.

**REQUEST FOR ADMISSION NO. 718:**

Admit that the 5,451,898 patent does not cover presentations made by various JEDEC 42.3 Subcommittee members between December 1991 through June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 718:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "cover" and "presentations." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee. In any event, to the extent that "cover" is intended to be interpreted as "infringed by," Rambus objects to the request on the ground that a patent claim cannot be infringed by a presentation.

**REQUEST FOR ADMISSION NO. 719:**

Admit that the 5,337,285 patent does not cover presentations made by various JEDEC 42.3 Subcommittee members between December 1991 through June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 719:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "cover" and "presentations." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee. In any event, to the extent that "cover" is intended to be interpreted as "infringed by," Rambus objects to the request on the ground that a patent claim cannot be infringed by a presentation.

**REQUEST FOR ADMISSION NO. 720:**

Admit that the 5,488,321 patent does not cover presentations made by various JEDEC 42.3 Subcommittee members between December 1991 through June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 720:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "cover" and "presentations." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee. In any event, to the extent that "cover" is intended to be interpreted as "infringed by," Rambus objects to the request on the ground that a patent claim cannot be infringed by a presentation.

**REQUEST FOR ADMISSION NO. 721:**

Admit that the 5,499,355 patent does not cover presentations made by various JEDEC 42.3 Subcommittee members between December 1991 through June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 721:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "cover" and "presentations." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee. In any event, to the extent that "cover" is intended to be interpreted as "infringed by," Rambus objects to the request on the ground that a patent claim cannot be infringed by a presentation.

**REQUEST FOR ADMISSION NO. 722:**

Admit that the 5,355,391 patent does not cover presentations made by various JEDEC 42.3 Subcommittee members between December 1991 through June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 722:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "cover" and "presentations." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee. In any event, to the extent that "cover" is intended to be interpreted as "infringed by," Rambus objects to the request on the ground that a patent claim cannot be infringed by a presentation.

**REQUEST FOR ADMISSION NO. 723:**

Admit that the 5,408,129 patent does not cover presentations made by various JEDEC 42.3 Subcommittee members between December 1991 through June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 723:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "cover" and "presentations." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee. In any event, to the extent that "cover" is intended to be interpreted as "infringed by," Rambus objects to the request on the ground that a patent claim cannot be infringed by a presentation.

**REQUEST FOR ADMISSION NO. 724:**

Admit that the 5,473,575 patent does not cover presentations made by various JEDEC 42.3 Subcommittee members between December 1991 through June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 724:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "cover" and "presentations." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee. In any event, to the extent that "cover" is intended to be interpreted as "infringed by," Rambus objects to the request on the ground that a patent claim cannot be infringed by a presentation.

**REQUEST FOR ADMISSION NO. 725:**

Admit that the 5,254,883 patent does not cover presentations made by various JEDEC 42.3 Subcommittee members between December 1991 through June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 725:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "cover" and "presentations." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee. In any event, to the extent that "cover" is intended to be interpreted as "infringed by," Rambus objects to the request on the ground that a patent claim cannot be infringed by a presentation.

**REQUEST FOR ADMISSION NO. 726:**

Admit that the 5,390,308 patent does not cover presentations made by various JEDEC 42.3 Subcommittee members between December 1991 through June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 726:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "cover" and "presentations." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee. In any event, to the extent that "cover" is intended to be interpreted as "infringed by," Rambus objects to the request on the ground that a patent claim cannot be infringed by a presentation.

**REQUEST FOR ADMISSION NO. 727:**

Admit that the 5,446,696 patent does not cover presentations made by various JEDEC 42.3 Subcommittee members between December 1991 through June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 727:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "cover" and "presentations." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee. In any event, to the extent that "cover" is intended to be interpreted as "infringed by," Rambus objects to the request on the ground that a patent claim cannot be infringed by a presentation.

**REQUEST FOR ADMISSION NO. 728:**

Admit that the 5,434,817 patent does not cover presentations made by various JEDEC 42.3 Subcommittee members between December 1991 through June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 728:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "cover" and "presentations." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee. In any event, to the extent that "cover" is intended to be interpreted as "infringed by," Rambus objects to the request on the ground that a patent claim cannot be infringed by a presentation.

**REQUEST FOR ADMISSION NO. 729:**

Admit that the 5,434,817 patent does not cover presentations made by various JEDEC 42.3 Subcommittee members between December 1991 through June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 729:**

Rambus objects to this request as duplicative of Request No. 728, and incorporates its objections and response thereto.

**REQUEST FOR ADMISSION NO. 730:**

Admit that the 5,430,676 patent does not cover presentations made by various JEDEC 42.3 Subcommittee members between December 1991 through June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 730:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "cover" and "presentations." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between

December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee. In any event, to the extent that "cover" is intended to be interpreted as "infringed by," Rambus objects to the request on the ground that a patent claim cannot be infringed by a presentation.

**REQUEST FOR ADMISSION NO. 731:**

Admit that the 5,485,490 patent does not cover presentations made by various JEDEC 42.3 Subcommittee members between December 1991 through June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 731:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "cover" and "presentations." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee. In any event, to the extent that "cover" is intended to be interpreted as "infringed by," Rambus objects to the request on the ground that a patent claim cannot be infringed by a presentation.

**REQUEST FOR ADMISSION NO. 732:**

Admit that Rambus' Taiwanese patent does not cover presentations made by various JEDEC 42.3 Subcommittee members between December 1991 through June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 732:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "cover" and "presentations." Rambus further objects that the request is vague and ambiguous with respect to the term "Rambus' Taiwanese patent" since Rambus has multiple Taiwanese patent certificates. Rambus further objects on the ground that it is not

familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee. In any event, to the extent that "cover" is intended to be interpreted as "infringed by," Rambus objects to the request on the ground that a patent claim cannot be infringed by a presentation.

**REQUEST FOR ADMISSION NO. 733:**

Admit that the 5,243,703 patent does not relate to the presentations made by various JEDEC 42.3 Subcommittee members between December 1991 through June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 733:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "relate to" and "presentations." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 734:**

Admit that the 5,319,755 patent does not relate to presentations made by various JEDEC 42.3 Subcommittee members between December 1991 through June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 734:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "relate to" and "presentations." Rambus further objects on the ground

that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 735:**

Admit that Rambus' Israeli patent does not relate to presentations made by various JEDEC 42.3 Subcommittee members between December 1991 through June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 735:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "relate to" and "presentations." Rambus further objects that the request is vague and ambiguous with respect to the term "Rambus' Israeli patent" since Rambus has multiple Israeli patents. Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 736:**

Admit that the 5,268,639 patent does not relate to presentations made by various JEDEC 42.3 Subcommittee members between December 1991 through June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 736:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "relate to" and "presentations." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 737:**

Admit that the 5,357,195 patent does not relate to presentations made by various JEDEC 42.3 Subcommittee members between December 1991 through June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 737:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "relate to" and "presentations." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 738:**

Admit that the 5,325,053 patent does not relate to presentations made by various JEDEC

42.3 Subcommittee members between December 1991 through June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 738:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "relate to" and "presentations." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 739:**

Admit that the 5,422,529 patent does not relate to presentations made by various JEDEC 42.3 Subcommittee members between December 1991 through June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 739:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "relate to" and "presentations." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 740:**

Admit that the 5,451,898 patent does not relate to presentations made by various JEDEC 42.3 Subcommittee members between December 1991 through June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 740:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "relate to" and "presentations." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 741:**

Admit that the 5,337,285 patent does not relate to presentations made by various JEDEC 42.3 Subcommittee members between December 1991 through June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 741:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "relate to" and "presentations." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 742:**

Admit that the 5,488,321 patent does not relate to presentations made by various JEDEC 42.3 Subcommittee members between December 1991 through June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 742:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "relate to" and "presentations." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 743:**

Admit that the 5,499,355 patent does not relate to presentations made by various JEDEC 42.3 Subcommittee members between December 1991 through June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 743:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "relate to" and "presentations." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

After having made reasonable inquiry, the information known to or readily obtainable by Rambus is insufficient for Rambus to admit or deny the request.

**REQUEST FOR ADMISSION NO. 744:**

Admit that the 5,355,391 patent does not relate to presentations made by various JEDEC 42.3 Subcommittee members between December 1991 through June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 744:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "relate to" and "presentations." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 745:**

Admit that the 5,408,129 patent does not relate to presentations made by various JEDEC 42.3 Subcommittee members between December 1991 through June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 745:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "relate to" and "presentations." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3

Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 746:**

Admit that the 5,473,575 patent does not relate to presentations made by various JEDEC 42.3 Subcommittee members between December 1991 through June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 746:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "relate to" and "presentations." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 747:**

Admit that the 5,254,883 patent does not relate to presentations made by various JEDEC 42.3 Subcommittee members between December 1991 through June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 747:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "relate to" and "presentations." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is

intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 748:**

Admit that the 5,390,308 patent does not relate to presentations made by various JEDEC 42.3 Subcommittee members between December 1991 through June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 748:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "relate to" and "presentations." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 749:**

Admit that the 5,446,696 patent does not relate to presentations made by various JEDEC 42.3 Subcommittee members between December 1991 through June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 749:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "relate to" and "presentations." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such

presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 750:**

Admit that the 5,434,817 patent does not relate to presentations made by various JEDEC 42.3 Subcommittee members between December 1991 through June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 750:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "relate to" and "presentations." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 751:**

Admit that the 5,434,817 patent does not relate to presentations made by various JEDEC 42.3 Subcommittee members between December 1991 through June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 751:**

Rambus objects to this request as duplicative of Request No. 750, and incorporates its objections and response thereto.

**REQUEST FOR ADMISSION NO. 752:**

Admit that the 5,430,676 patent does not relate to presentations made by various JEDEC 42.3 Subcommittee members between December 1991 through June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 752:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "relate to" and "presentations." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 753:**

Admit that the 5,485,490 patent does not relate to presentations made by various JEDEC 42.3 Subcommittee members between December 1991 through June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 753:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "relate to" and "presentations." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 754:**

Admit that Rambus' Taiwanese patent does not relate to presentations made by various JEDEC 42.3 Subcommittee members between December 1991 through June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 754:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "relate to" and "presentations." Rambus further objects that the request is vague and ambiguous with respect to the term "Rambus' Taiwanese patent" since Rambus has multiple Taiwanese patent certificates. Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 755:**

Admit that the 5,243,703 patent was not involved in to the presentations made by various JEDEC 42.3 Subcommittee members between December 1991 through June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 755:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "involved in" and "presentations." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 756:**

Admit that the 5,319,755 patent was not involved in presentations made by various JEDEC 42.3 Subcommittee members between December 1991 through June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 756:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "involved in" and "presentations." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 757:**

Admit that Rambus' Israeli patent was not involved in presentations made by various JEDEC 42.3 Subcommittee members between December 1991 through June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 757:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "involved in" and "presentations." Rambus further objects that the request is vague and ambiguous with respect to the term "Rambus' Israeli patent" since Rambus has multiple Israeli patents. Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable

inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 758:**

Admit that the 5,268,639 patent was not involved in presentations made by various JEDEC 42.3 Subcommittee members between December 1991 through June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 758:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "involved in" and "presentations." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 759:**

Admit that the 5,357,195 patent was not involved in presentations made by various JEDEC 42.3 Subcommittee members between December 1991 through June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 759:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "involved in" and "presentations." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such

presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 760:**

Admit that the 5,325,053 patent was not involved in presentations made by various JEDEC 42.3 Subcommittee members between December 1991 through June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 760:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "involved in" and "presentations." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 761:**

Admit that the 5,422,529 patent was not involved in presentations made by various JEDEC 42.3 Subcommittee members between December 1991 through June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 761:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "involved in" and "presentations." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members

between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 762:**

Admit that the 5,451,898 patent was not involved in presentations made by various JEDEC 42.3 Subcommittee members between December 1991 through June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 762:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "involved in" and "presentations." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 763:**

Admit that the 5,337,285 patent was not involved in presentations made by various JEDEC 42.3 Subcommittee members between December 1991 through June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 763:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "involved in" and "presentations." Rambus further objects on the

ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 764:**

Admit that the 5,488,321 patent was not involved in presentations made by various JEDEC 42.3 Subcommittee members between December 1991 through June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 764:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "involved in" and "presentations." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 765:**

Admit that the 5,499,355 patent was not involved in presentations made by various JEDEC 42.3 Subcommittee members between December 1991 through June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 765:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least

with respect to the terms "involved in" and "presentations." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

After having made reasonable inquiry, the information known to or readily obtainable by Rambus is insufficient for Rambus to admit or deny the request.

**REQUEST FOR ADMISSION NO. 766:**

Admit that the 5,355,391 patent was not involved in presentations made by various JEDEC 42.3 Subcommittee members between December 1991 through June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 766:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "involved in" and "presentations." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 767:**

Admit that the 5,408,129 patent was not involved in presentations made by various JEDEC 42.3 Subcommittee members between December 1991 through June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 767:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "involved in" and "presentations." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 768:**

Admit that the 5,473,575 patent was not involved in presentations made by various JEDEC 42.3 Subcommittee members between December 1991 through June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 768:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "involved in" and "presentations." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 769:**

Admit that the 5,254,883 patent was not involved in presentations made by various

JEDEC 42.3 Subcommittee members between December 1991 through June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 769:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "involved in" and "presentations." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 770:**

Admit that the 5,390,308 patent was not involved in presentations made by various JEDEC 42.3 Subcommittee members between December 1991 through June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 770:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "involved in" and "presentations." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 771:**

Admit that the 5,446,696 patent was not involved in presentations made by various JEDEC 42.3 Subcommittee members between December 1991 through June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 771:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "involved in" and "presentations." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 772:**

Admit that the 5,434,817 patent was not involved in presentations made by various JEDEC 42.3 Subcommittee members between December 1991 through June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 772:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "involved in" and "presentations." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 773:**

Admit that the 5,434,817 patent was not involved in presentations made by various JEDEC 42.3 Subcommittee members between December 1991 through June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 773:**

Rambus objects to this request as duplicative or Request No. 772, and incorporates its objections and response thereto.

**REQUEST FOR ADMISSION NO. 774:**

Admit that the 5,430,676 patent was not involved in presentations made by various JEDEC 42.3 Subcommittee members between December 1991 through June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 774:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "involved in" and "presentations." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 775:**

Admit that the 5,485,490 patent was not involved in presentations made by various JEDEC 42.3 Subcommittee members between December 1991 through June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 775:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least

with respect to the terms "involved in" and "presentations." Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

**REQUEST FOR ADMISSION NO. 776:**

Admit that Rambus' Taiwanese patent was not involved in presentations made by various JEDEC 42.3 Subcommittee members between December 1991 through June 1996.

**RESPONSE TO REQUEST FOR ADMISSION NO. 776:**

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "involved in" and "presentations." Rambus further objects that the request is vague and ambiguous with respect to the term "Rambus' Taiwanese patent" since Rambus has multiple Taiwanese patent certificates. Rambus further objects on the ground that it is not familiar with all presentations made by JEDEC 42.3 Subcommittee members between December 1991 through June 1996, and is unable to become familiar with all such presentations through reasonable inquiry even if, for purposes of this request, "presentations" is intended to be restricted to presentations made during meetings of the JEDEC 42.3 Subcommittee.

Subject to and without waiving any objections, Rambus responds as follows:

Denied.

DATED: February 6, 2003 Respectfully submitted,

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VERIFICATION

I, Robert K. Eulau, declare:

I am Senior Vice President - Finance of Rambus Inc., which is the Respondent in the above-entitled action, and I have been authorized to make this verification on its behalf.

I have read the foregoing document entitled Respondent Rambus Inc.'s Responses to Complaint Counsel's First Request for Admissions and know the contents thereof. I am informed and believe that the information contained therein is accurate and true.

I declare under penalty of perjury under the laws of the State of California that the foregoing is true and correct.

Executed at Los Altos, California on February 6, 2002.

_____

Robert K. Eulau