LAUR-06-0322

Licensable Technologies

Superthin SOI

Applications:

- Semiconductor manufacturing
- Wafer fabrication

Benefits:

- More transistors can fit on a chip
- Higher performance
- Fewer silicon defects — less damage
- Higher reliability and reproducibility
- Lower power consumption

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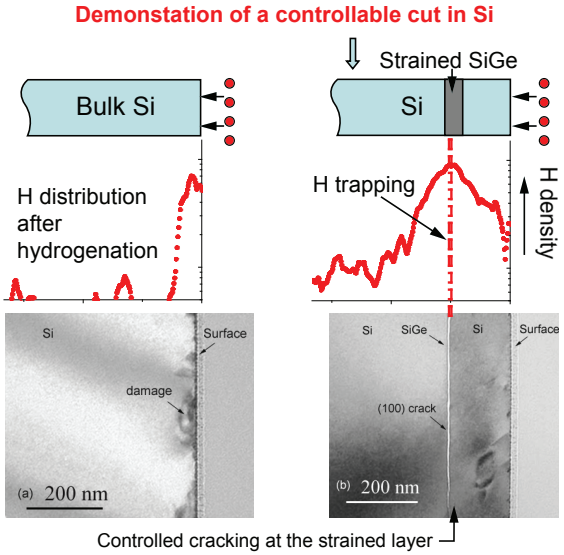
Technology Transfer Division

Summary:

The Problem: Moore's Law*

The Solution: Los Alamos' Superthin Silicon-on-Insulator (SOI) technology



Heterogeneous material integration for future devices

Semiconductor designers are constantly shrinking the size of transistors in order to fit more devices in less space. SOI has been used to tackle issues of device shrinking. SOI introduces a layer of insulating material between the top face of the silicon layer (where semiconductor chips are fabricated) and the supporting base silicon to produce faster devices that consume significantly less power than those made with traditional bulk silicon. While the industry once thought that device integration on SOI wafers would provide a sustainable method to solve transistor scaling barriers, its progress has been hindered by the difficulty in producing highly demanded, top-quality SOI wafers with existing techniques. In sum, industry is having trouble producing a high-crystalline-quality top Si layer with a thickness less than 50 nanometers.

Los Alamos National Laboratory has invented a way to overcome the 50 nanometer barrier to allow the industry to continue its "Moore's Law" trajectory to reduce size and power consumption. Specifically, the Laboratory has developed three revolutionary methods for transferring an ultrathin layer of silicon with high crystalline quality to an insulating substrate:

- Method One: Introduces a thin strained layer.
- Method Two: Uses a doped layering technique to induce cracking.
- Method Three: Employs an interface defect layer to induce cracking.

All three methods result in the transfer of an ultrathin (sub 20 nm) layer of a monocrystalline layer of silicon to an insulating substrate.

Development Stage:

This technology has been reduced to practice in the laboratory.

Patent Status: Patents are pending for each method.

Licensing Status:

The technology is ready and available for non-exclusive licensing. The Laboratory welcomes development partners to help mature the technology to product readiness.

*Moore's Law says that the total number of transistors on the cheapest CPU will grow exponentially at a constant rate and that this constant rate produces a doubling every 12 (or 18, or 24) months.

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