PUBLIC

UNITED STATES OF AMERICA
BEFORE THE FEDERAL TRADE COMMISSION

In the Matter of **RAMBUS INC.,** **a corporation.**	**Docket No. 9302**

RAMBUS INC.'S RESPONSES TO COMPLAINT COUNSEL'S PROPOSED FINDINGS OF FACT

VOLUME II

VI. Rambus Participation in JEDEC.

A. Beginning In Early 1992, and Continuing Throughout the Entire Time It Was a Member of JEDEC and Thereafter, Rambus Intended to Use Its Patents To Monopolize the Technologies Incorporated In the JEDEC Standards.

1. Throughout The Time It Was a Member of JEDEC and Thereafter, Rambus Acted With Knowledge and Intent to Monopolize.

800. From the outset, Rambus planned to obtain monopoly power in the market for technologies used in synchronous DRAMs. (CCFF 708, 709, 732-35; *see also* CX0543A at 7 ("Rambus's objective is to establish Rambus Technology as the new high volume standard in the 90's. Our target is to achieve penetration of 50% of DRAMs (and the associated logic ICs) by 1997.")).

Rambus's Response to Finding No. 800:

The cited findings and evidence support no conclusion about "monopoly power." They instead reflect a start-up company's desire to succeed by offering substantial improvements in performance to the DRAM industry.

801. Rambus originally planned lawfully to obtain monopoly power in the market for technologies used in synchronous DRAMs by persuading the market to adopt and license its RDRAM technology. (CCFF 736-45).

Rambus's Response to Finding No. 801:

For the reasons set out in RRFF 800, the cited findings and evidence support no conclusion about "monopoly power."

802. Throughout its entire time at JEDEC, Rambus continued to intend lawfully to obtain monopoly power in the market for technologies used in synchronous DRAMs by persuading the market to adopt and license its RDRAM technology. (CCFF 746-56, 1238-53.)

Rambus's Response to Finding No. 802:

For the reasons set out in RRFF 800, the cited findings and evidence support no conclusion about "monopoly power."

803. Beginning in 1992, Rambus developed a second plan to monopolize the market for technologies used in synchronous DRAMs, one that did not depend on the market adopting RDRAMs. This second plan was to obtain and later enforce patents covering technologies used in SDRAMs, including JEDEC-compliant SDRAMs. (CCFF 757-66, 911-18, 937-38; *see also* CX0543A at 16-17 (Draft Business Plan: "Our #1 strategy to counter Sync DRAMs therefore is to get our [RDRAM] parts proven and in the market. . . . Finally, we believe that Sync DRAMs infringe on some claims in our filed patents; and that there are additional claims we can file for our patents that cover features of Sync DRAMs. Then we will be in position to request patent licensing (fees and royalties) from any manufacturer of Sync DRAMs. Our action plan is to determine the exact claims and file the additional claims by the end of Q3/92."); CX1941 at 1 (Vincent notes: "Need preplanning before accuse others of infringement"); CX1949 at 1 (Vincent notes: "what to include in divisional applications . . . so cause problems with synch DRAM..."); CX0702 at 1 (Ware e-mail: "This claim has been written up and filed. This is directed against SDRAMs."); CX1970 at 1 (Vincent notes: "Enforcement; Sync DRAMS."); CX0763 at 1 (Crisp e-mail: "I would hope we sue other companies, in particular those that are not licensed."); CX0831 (Tate e-mail: "tony's #1 objective right now is to . . . determine what should proactively be done to strengthen our IP position relative to competition." and requesting staff to forward e-mail talking about "competitive technology developments/directions (e.g. JEDEC meeting reports, etc.)"); CX1730 at 1 (Tate notes: "SDRAM – now – next . . . 1. Understand our IP . . . 3. Assess our current patents – what claims/strength do we have vs. competition 4. What can we do? . . . 5. Plan of action 6. Implement")).

Rambus's Response to Finding No. 803:

The cited findings and evidence do not support the conclusory assertion contained in this finding. The cited exhibits are mischaracterized and taken out of context, as demonstrated in connection with those individual findings in this section where the particular exhibits are discussed. As an example, Complaint Counsel cite an early *draft* of a Rambus business plan for the proposition that Rambus believed its patent applications covered "Sync DRAMs," without disclosing that the phrase was omitted from the final version of the business plan after Mr. Tate learned that the statement was inaccurate. *See* RRFF 765 and evidence cited therein.

Because each of the other exhibits is addressed in connection with specific findings to which they are supposedly relevant, Rambus will discuss those exhibits at that point.

804. SDRAM and DDR SDRAM were sources of competition for RDRAM. (Crisp, Tr.

2932 ("Q: . . . you understood that certain people at Rambus believed that DDR SDRAMs could be a potential threat to Rambus' business, right? A: Yes, that's correct."); CX0606 at 2 ("Mr. Mooring then spoke on Rambus vs. Sync. positioning, potential competition from IEEE Ramlink strategy, staffing, marketing communications."); CX0831 (Tate e-mail citing "JEDEC meeting reports" as an example of "competitive technology developments/directions"); CX0837 at 1 (Crisp e-mail: "At the time we began attending JEDEC we did so to learn what the competition was working on . . ."); CX2069 at 654 (Crisp, Infineon Dep.) ("Q. And DDR was perceived to be a potential threat; right? . . . THE WITNESS: It had that potential, yes."); CX2073 at 212 (Tate, Micron Dep.) (Tate "understood [SDRAMs] were something that customers were talking about as a competitive alternative.")).

Rambus's Response to Finding No. 804:

Rambus has no specific response, except to note that the proposed finding is vague as to time.

805. From the time that Rambus first developed its plan, Rambus focused on SDRAMs, and on the SDRAM standard being developed in JEDEC. (CX0606 at 2 (Board of Directors Minutes: "Mr. Crisp reported on the SDRAM status at JEDEC, the Rambus patent strategy and system level difficulties with SDRAMs."); CX0543A at 16-17 (Draft Business Plan: "Our #1 strategy to counter Sync DRAMs . . ."); CX1949 at 1 (Vincent notes: "what to include in divisional applications . . . so cause problems with synch DRAM..."); CX0702 at 1 (Ware e-mail: "This claim has been written up and filed. This is directed against SDRAMs."); CX1970 at 1 (Vincent notes: "Enforcement; Sync DRAMS."); CX0745 at 1 (Roberts note: "This is Lester's attempt to write the claims for the MOST/SDRAM defense."); CX0831 (Tate e-mail: "tony's #1 objective right now is to . . . determine what should proactively be done to strengthen our IP position relative to competition." and requesting staff to forward e-mail talking about "competitive technology developments/directions (e.g. JEDEC meeting reports, etc.)").

Rambus's Response to Finding No. 805:

The cited exhibits do not support the conclusory assertion contained in this finding. Because the particular cited exhibits are addressed individually in connection with the particular findings in this section to which they are supposedly relevant, they will not be addressed here.

806. From the time that Rambus first developed this plan, Rambus intended to obtain patents with claims covering SDRAMs, including SDRAMs that complied with the SDRAM and DDR SDRAM standards being developed by JEDEC. (CCFF 885-92, 900-01, 910, 917, 918, 932-36, 937, 939, 945, 948, 958, 962-67, 981, 987-93, 100-03, 1004-08, 1018-24, 1028-29, 1040, 1049, 1069, 1074-77, 1089, 1098-99; *see also* CX0543A at 17 (Draft Business Plan: ". . .

there are additional claims we can file for our patents that cover features of Sync DRAMs. . . . Our action plan is to determine the exact claims and file the additional claims by the end of Q3/92."); CX0606 at 2 (Board of Director Minutes: "Mr. Crisp reported on the SDRAM status at JEDEC, the Rambus patent strategy and system level difficulties with SDRAMs."); CX0831 (Tate e-mail: "tony's #1 objective right now is to . . . determine what should proactively be done to strengthen our IP position relative to competition." and requesting staff to forward e-mail talking about "competitive technology developments/directions (e.g. JEDEC meeting reports, etc.)"); CX0738 (Dillon e-mail: "We may be able to make a broader claim for auto-precharge for *any* DRAM and therefore gain leverage over SDRAM and MOST."); CX0740 (Tate e-mail: "this stuff is real critical – I'd like a list of which claims we are making that read directly on current/planned sdrams . . . so i can track progress from lester's periodic status lists."); CX1730 at 1 (Tate notes: "SDRAM – now – next . . . 1. Understand our IP . . . 3. Assess our current patents – what claims/strength do we have vs. competition 4. What can we do? . . . 5. Plan of action").

Rambus's Response to Finding No. 806:

This conclusory finding misstates the evidence and is false. The particular exhibits are described elsewhere in this section; that discussion will not be repeated here. It is clear, however, from the weight of the evidence, that:

1. Rambus did not violate any EIA or JEDEC rules that governed its conduct while it was a JEDEC member. *See* RPF 318-463.

2. The governing EIA and JEDEC rules encouraged but did not require the disclosure of intellectual property interests while Rambus was a member. *See* RPF 128–185.

3. Rambus had no patents or patent applications while it was a JEDEC member that read on or were essential to the use of any JEDEC standard or even to the use of any technology *proposed* for standardization while it was a member. *See* RPF 327-396.

4. Rambus had no intent to violate any EIA or JEDEC rule relating to

intellectual property disclosure. *See* RPF 444-463.

5. Rambus did nothing to lull any JEDEC member into believing that it would not have or would not enforce its intellectual property. *See* RPF 464-595.

The proposed conclusory finding is, therefore, contrary to the weight of the evidence.

807. Rambus intentionally joined JEDEC and renewed its membership. (CX0602 at 2 (Rambus's application for membership) and 6-7, 10-12 (its payment of dues); CCFF 878-79, 954, 982, 1039).

Rambus's Response to Finding No. 807:

This finding's reference to "intent" is peculiar; it adds nothing to the finding, which should be rephrased simply to state the fact that Rambus joined JEDEC in early 1992 and subsequently paid the required dues for calendar years 1993, 1994 and 1995.

808. Rambus intentionally followed the proceedings of JEDEC. (CCFF 871-77, 880-84, 893-98, 902-09, 921-27, 929-31, 940-45, 950-53, 959-61, 968-76, 978-80, 983-86, 996-99, 1009-17, 1026-27, 1031-38, 1041-48, 1062-68, 1070-73, 1078-82, 1096-99.)

Rambus's Response to Finding No. 808:

The "intent" phrasing is again peculiar. Rambus agrees that after it joined JEDEC, its JEDEC representative attended JEDEC meetings between early 1992 and December 1995. Rambus's primary JEDEC representative, Mr. Crisp, testified that between 1993 and 1995, he spent only 5-10% of his time on JEDEC-related matters. (Crisp, Tr. 3522).

809. From the time that Rambus first developed this plan, Rambus intentionally took specific action to obtain patents with claims covering SDRAMs, including SDRAMs that complied with the SDRAM and DDR SDRAM standards being developed by JEDEC. (CCFF 885-92, 900-01, 910, 917, 918, 932-36, 937, 939, 945, 948, 958, 962-67, 981, 987-93, 100-03, 1004-08, 1018-24, 1028-29, 1040, 1049, 1069, 1074-77, 1089, 1098-99; *see also* CX1949 at 1 (Vincent notes: "what to include in divisional applications . . . so cause problems with synch DRAM..."); CX0702 at 1 (Ware e-mail: "This claim has been written up and filed. This is

directed against SDRAMs."); CX0745 at 1 (Roberts note: "This is Lester's attempt to write the claims for the MOST/SDRAM defense."); CX0831 (Tate e-mail: "tony's #1 objective right now is to . . . determine what should proactively be done to strengthen our IP position relative to competition." and requesting staff to forward e-mail talking about "competitive technology developments/directions (e.g. JEDEC meeting reports, etc.)"); CX2092 at 192 (Crisp, Infineon Trial Tr.) ("Q: Am I right, sir, that Rambus was intentionally drafting claims to intentionally cover JEDEC SDRAMs? A: Partially true, yes.")).

Rambus's Response to Finding No. 809:

The cited findings and exhibits do not support this conclusory finding. The particular exhibits are discussed in connection with the individual findings in this section to which they are supposedly relevant; that discussion will not be repeated here. In response to the finding itself, Rambus states that the evidence supports only a finding that Rambus intended to obtain broad patent protection for its inventions and that it told the world it would do so. (RX 81 at 3 – March 1992 Corporate Backgrounder: "Rambus Inc. is fully protecting the intellectual property rights of its technology by filing basic, broad patents in all major industrial nations around the world.").

The parties have also stipulated that:

(1) Prior to the adoption of the JEDEC SDRAM standard in 1993, Rambus had no claims in any pending patent application that, if issued, would have necessarily been infringed by the manufacture or use of any device manufactured in accordance with the 1993 JEDEC SDRAM standard; and

(2) As of January 1996, Rambus held no issued U.S. patents that were essential to the manufacture or use of any device manufactured in compliance with any JEDEC standard.

(The Parties' First Set of Stipulations, entered April 24, 2003, p. 2).

Finally, the evidence supports a finding that even if Rambus had filed patent applications while it was a JEDEC member that covered features being considered for standardization by JEDEC, it would have violated no rule or policy by doing so, because there was no rule or policy against such efforts, because the governing Legal Guides stated that "[s]tandards are proposed or adopted by EIA without regard to whether their proposal or adoption may in any way involve patents on articles, materials or processes," (CX 204 at 4), and because the EIA formally stated to the FTC in January 1996 that its policy was that "[a]llowing patented technology in standards is procompetitive." (RX 669 at 2). *See* RPF 432-443.

810. Rambus intentionally took information learned at JEDEC and used it to help obtain patents with claims covering SDRAMs, including SDRAMs that complied with the SDRAM and DDR SDRAM standards being developed by JEDEC. (CCFF 885-92, 900-01, 910, 917, 918, 932-36, 937, 939, 945, 948, 958, 962-67, 981, 987-93, 100-03, 1004-08, 1018-24, 1028-29, 1040, 1049, 1069, 1074-77, 1089, 1098-99; *see also* CX2092 at 192 (Crisp, Infineon Trial Tr.) ("Q: Am I right, sir, that Rambus was intentionally drafting claims to intentionally cover JEDEC SDRAMs? A: Partially true, yes."); *id*. at 132 ("Q: And the ideas that you had to add claims to the Rambus patent applications for the mode register and for programmable CAS latency, those were ideas that were spurred on by your attendance at the JEDEC meeting in April and May and participating in this SDRAM standardization effort, right? A: Yeah. Those were our inventions. We had invented those for the RDRAM.")).

Rambus's Response to Finding No. 810:

The proposed finding is not supported by the findings and evidence that it cites. The cited exhibits and testimony are addressed in connection with the particular individual findings to which they are supposedly relevant; that discussion will not be repeated here.[1]

This finding is also irrelevant, for the reasons explained by Complaint Counsel in his Opening Statement:

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[1]For example, the proposed finding appears to assume that Rambus did, during the relevant timeframe, file claims that, if granted by the PTO, would have required a license to practice a JEDEC standard. This is contrary to the evidence. *See* RPF 334-383.

> "[L]et me be very clear about something. It is *not* complaint counsel's contention that the act of amending one's patent applications to cover a competitive product is in itself a wrongful act, nor do we claim that Rambus' use of information obtained from attending JEDEC meetings amounts to misappropriation or somehow renders Rambus' patents invalid."

(Opening Statement, Tr. 49-50) (emphasis added).

Having taking the misappropriation issue off of the table at the outset, Complaint Counsel may not now bring it to the fore. It is, in any event, not an issue at all, as JEDEC Council and JC 42.3B Chairman Gordon Kelley testified:

> "I did not understand that the use of JEDEC confidential information was an abuse as long as the people using the information were members."

(Kelley, Tr. 2626).

811. Various Rambus JEDEC representatives believed Rambus had pending patent applications that, if issued, would likely cover SDRAMs that complied with the JEDEC SDRAM and DDR SDRAM standards. (CCFF 884, 887, 892, 900-01, 910, 917, 918, 932-36, 937, 938, 939, 948, 958, 962-67, 987-93, 7000-03, 1004-08, 1009-17, 1018-25, 1028-30, 1040, 1049, 1057-58, 1069, 1073, 1077, 1089, 1098; *see also* CX0543A at 17 (Draft Rambus Business Plan: " . . . we believe that Sync DRAMs infringe on some claims in our filed patents; . . ."); CX2070 at 97 (Harmon, Micron Dep.) (Harmon heard "from various people that Rambus' patents were so fundamental and so broad that they likely covered technology that was being used by any other high-speed DRAM."); CX2073 at 221-22 (Tate, Micron Dep.) ("I recall that our feeling [in 1992] was that synchronous DRAMS sure looked like they were stemming from inventions that we had done first, and that our understanding is that patents are supposed to protect your inventions, and we assumed that our patents had been filed to do so. And that led us to a conclusion that, hey, we must have some claims they are infringing. . ."). Farmwald, Tr. 8208 ("We certainly in general thought that we had pretty broad claims and that they certainly might cover synchronous DRAMs").

Rambus's Response to Finding No. 811:

The proposed finding is not supported by the findings and evidence that it cites. For example, Complaint Counsel cite only the initial part of Mr. Tate's deposition testimony regarding the 1992 draft business plan, without revealing that Mr. Tate at the same time and on the same page testified that after the draft had been prepared, an employee was assigned to review the pending claims to see if they did, in fact, cover SDRAM, and that after hearing his report, Tate concluded that the claims were not broad enough to do so. (CX 2073, Tate Micron Depo. at 222-24; *see also* CX 2088, Tate Infineon Trial Testimony at 57-8). *See* RPF 423-24.

The remaining evidence cited in this conclusory finding will be addressed when it is cited in connection with the particular findings in this section to which it is supposedly relevant.

812. From the time that Rambus first developed this plan, Rambus intended to enforce its patents against SDRAMs, including SDRAMs that complied with the SDRAM and DDR SDRAM standards being developed by JEDEC, if necessary to monopolize the market for technology used in DRAMs. (CCFF 887, 889-91, 917, 918, 938, 948, 955-57, 981, 997, 1002, 1018-24, 1037, 1059-60, 1069, 1083-87; *see also* CX0543A at 17-18 (Draft Rambus Business Plan: ". . . we will be in position to request patent licensing (fees and royalties) from any manufacturer of Sync DRAMs."); CX1941 at 1 (Vincent notes, "Need preplanning before accuse others of infringement"); CX1970 at 1 (Vincent notes: "Enforcement; Sync DRAMS."); CX0763 at 1 (Crisp e-mail: "I would hope we sue other companies, in particular those that are not licensed."); CX1730 at 1 (Tate notes: "SDRAM – now – next . . . 3. Assess our current patents – what claims/strength do we have vs. competition 4. What can we do? . . . 5. Plan of action 6. Implement")).

Rambus's Response to Finding No. 812:

The proposed conclusory finding is not supported by the individual findings and evidence that it cites. The 1992 draft business plan is discussed above; it and the other exhibits cited in this finding will be addressed in connection with the particular findings to which they are supposedly relevant. Rambus's direct responses to the conclusory allegations contained in this

finding are as follows:

(1) The evidence demonstrates that Rambus violated no rules that governed its conduct as a JEDEC member. RPF 318-463.

(2) The evidence establishes that Rambus did nothing to lull any JEDEC member into believing that it would not assert whatever intellectual property rights it might have. RPF 464-595.

(3) The evidence establishes that Rambus had no patent or patent applications while it was a JEDEC member whose claims would be infringed by a memory device built in compliance with a JEDEC standard. RPF 327-396.

(4) The evidence establishes that there was no rule prohibiting Rambus from obtaining valid patents for the features or technologies invented by Drs. Farmwald or Horowitz, regardless of whether those technologies were discussed at JEDEC meetings as possible candidates for standardization. Instead, it was JEDEC's policy and practice that "JEDEC standards are adopted without regard to whether or not their adoption may involve patents [on] articles, materials or processes." (CX 205A at 11). Moreover, as the EIA told the FTC in January 1996, "[a]llowing patented technology in standards is procompetitive" because "[b]y allowing standards based on patents, American consumers are assured of standards that reflect the latest innovation and high technology the great technical minds of this country can deliver." (RX 669 at 2-3).

These are not just words. They represent official EIA policy; they are found in official EIA and JEDEC manuals and formal comment letters to United States government officials; and

they reflect a "basic objective" of "all EIA engineering standardization and related programs." (CX 204 at 4).

813. Rambus intentionally did not inform others in the industry about the content of its pending patent applications. (CCFF 909 927, 931, 944, 953, 961, 974, 976, 980, 986, 999, 1017, 1027, 1033, 1038, 1048, 1063, 1067, 1082, 1098-99, 1111, 1238-59, 1676-1700).

Rambus's Response to Finding No. 813:

This statement is both false and misleading, as demonstrated in Rambus's responses to the cited findings and as demonstrated at RPF 606-719.

814. Rambus intentionally did not inform JEDEC about any of its pending patent applications. (CCFF 909 927, 931, 944, 953, 961, 974, 976, 980, 986, 999, 1017, 1027, 1033, 1038, 1048, 1063, 1067, 1082, 1098-99, 1111; CX0837 at 2 (Crisp e-mail: "We decided [during the beginning of the period after we joined JEDEC] that we really could not be expected to talk about potential infringement for patent that had not issued . . ."); *id.* (" . . . we should re-evaluate our position relative to what we decide to keep quiet about, and what we say we have."); CX0711 at 68, 73 (Crisp e-mail: in response to Mr. Kelley's request to inform JEDEC of whether Rambus knows of any patents that may read on SyncLink, "I think it makes no sense to alert them to a potential problem they can easily work around. . . . We may not want to make it easy for all to figure out what we have especially if nothing looks really strong."); CX0673 (Crisp e-mail: "Siemens expressed concern over potential Rambus Patents covering 2 bank designs. Gordon Kelley of IBM asked me if we would comment which I declined."); Crisp, Tr. 3174-75 (Mr. Crisp did not say anything about patent applications at the time he disclosed Rambus's '703 patent; Vice President Mooring chastised Mr. Crisp after disclosing the '703 patent.)).

Rambus's Response to Finding No. 814:

The proposed finding and its citations to evidence are misleading and incomplete. For example, Complaint Counsel interrupt Mr. Crisp in mid-sentence when quoting from CX 837 at 2, in a manner that omits the legitimate business reasons for non-disclosure that Mr. Crisp sets out in his e-mail. Here is the full sentence, with the portion omitted by Complaint Counsel in italics.

> "We decided that we really could not be expected to talk about potential

> infringement for patents that had not issued *both from the perspective of not knowing what would wind up being acceptable to the examiner, and from the perspective of not disclosing our trade secrets any earlier than we are forced to*."

(CX 837 at 2).

Complaint Counsel omit this language because it is entirely inconsistent with the Complaint's core allegations and with Complaint Counsel's theory that Rambus's decision to maintain its patent applications in confidence was part of some grandiose and unlawful "plan." Fortunately, the record contains the unexpurgated document.

The evidence also shows that numerous JEDEC members and their lawyers were aware of and reviewed one or more of Rambus's patent applications while Rambus was a JEDEC member, *see* RPF 516-535; 692-702, and that Rambus's patent applications were discussed at JEDEC meetings on at least two occasions.

It is true that Rambus did not, at JEDEC meetings, describe the contents of its pending patent applications. It was *not* silent, however. Rambus's refusals to comment at both the May 1992 JEDEC meeting and the September 1995 meeting were openly stated and were known to all. Rambus's September 1995 statement could not have been clearer:

> "Our presence or silence at committee meetings does not constitute an endorsement of any proposal under the committee's consideration nor does it make any statement regarding potential infringement of Rambus intellectual property."

(JX 27 at 26). The committee chair, Mr. Kelley, considered this statement to be a "notification to

the Committee that there should be a concern" about intellectual property issues. (Kelley, Tr. 2579).

815. After it withdrew from JEDEC, Rambus intentionally took specific action to obtain patents with claims covering SDRAMs, including SDRAMs that complied with the SDRAM and DDR SDRAM standards being developed by JEDEC. (CCFF 1625-75).

Rambus's Response to Finding No. 815:

The conclusory finding is misleading, ambiguous and irrelevant to any issue in the case. *See* RRFF 1625-75.

816. After it withdrew from JEDEC, Rambus intentionally did not inform others in the industry about the content of its pending patent applications. (CCFF 1676-1700; *see also* CX0919 at 1 (Tate e-mail: "2. do *NOT* tell customers/partners that we feel DDR may infringe–our leverage is better to wait"); CX0942 ("Our policy so far has been NOT to publicize our patents and I think we should continue with this."); CX1075 at 2 "We've made no comment on whether DDR infringes our patents. . . . Our position is there is insufficient data."); Hampel, Tr. 8731-33 (Hampel had contacts with Rambus customers "15 to 40 times a month" and he testified that he was not aware of "any instance in which Rambus representatives told the DRAM manufacturers which features of RDRAM were protected by Rambus patents or patent applications")).

Rambus's Response to Finding No. 816:

The proposed finding is misleading, contrary to the evidence, and irrelevant. *See* RRFF 1676-1700.

817. Beginning in late 1999, Rambus intentionally began threatening to enforce its patents against manufacturers of SDRAMs and DDR SDRAMs and manufacturers of controllers and graphics controllers that interface with SDRAMs and DDR SDRAMs. Rambus intentionally sent letters and made presentations to companies stating that their products infringed Rambus patents. Rambus intentionally sued two DRAM manufacturers in U.S. federal courts, filed counterclaims against two DRAM manufacturers in U.S. federal courts, and sued three DRAM manufacturers in various foreign courts, in all cases alleging infringement of Rambus patents. (CCFF 1950-2032) .

Rambus's Response to Finding No. 817:

The proposed finding is misleading, contrary to the evidence, and irrelevant. *See*

RRFF 1950-2032.

818. Rambus acted with knowledge that the purpose of JEDEC was to develop open standards. (CCFF 318, 320, 371, 383-85, 418, 430, 823, 871-85, 880, 902-906, 921, 929, 940, 942-43, 950, 959, 968-69, 978-79, 983-85, 994-95, 996, 1009, 1026, 1034-36, 1041-42, 1062-66, 1078, 1080, 1601-02; *see also* CX0903 at 2 (Crisp e-mail: "The job of JEDEC is to create standards which steer clear of patents which must be used in compliance with the standard whenever possible.").

Rambus's Response to Finding No. 818:

Rambus has responded to each one of the dozens of individual findings cited in support of this conclusory finding; it will not repeat those responses here. The proposed finding is misleading in many respects. The quoted e-mail was written *after* Rambus withdrew from JEDEC; the incomplete snippet that it is quoted has no probative value. Moreover, if the finding is intended to suggest that "open standards" are those that are free of any patented technologies, it is flatly contrary to the great weight of the evidence and, in particular, to the governing EIA Legal Guides (CX 204) and the EIA's January 1996 comment letter to the FTC. (RX 669 at 2-3: ("[a]llowing patented technology in standards is procompetitive . . . . By allowing standards based on patents, American consumers are assured of standards that reflect the latest innovation and high technology [that] the great technical minds of this country can deliver.").

819. Rambus acted with knowledge that JEDEC and its members were concerned about a company enforcing patents against companies practicing a JEDEC standard. (CCFF 318, 320, 371, 383-85, 418, 430, 823, 871-85, 880, 902-906, 921, 929, 940, 942-43, 950, 959, 968-69, 978-79, 983-85, 994-95, 996, 1009, 1026, 1034-36, 1041-42, 1062-66, 1078, 1080, 1601-02).

Rambus's Response to Finding No. 819:

Rambus has responded to each one of the dozens of individual findings cited in this conclusory finding; it will not repeat those responses here. The proposed finding is false.

820. Rambus acted with knowledge that JEDEC had a disclosure policy requiring

disclosure of patents and patent applications. (CX0672 at 1 (Garrett email: "Fujitsu indicated that they do have patents applied for, but that they will comply with the JEDEC requirements to make it a standard!!!"); CX685 at 1 (Mooring e-mail: "IBM raised the issue that they were aware that some "voting" JEDEC attendees have patents pending on SDRAMs that they have not made the committee aware of. They will come to the next meeting with a list of the offenders."); CX2092 at 60 (Crisp, Infineon Tr.) ("Sometime in 1995 I received a copy of the patent policy as part of the users in the manual that they had that was to be used to tell people what the rules were. And I read in there that it applied to patent policies. Q: Patent applications? A: Patent applications, that's right."); CX2104 at 950-51 (Crisp, Micron Dep.) ("Q And when you got it [JEDEC manual 21-I] and read it, then it was clear that the manual required disclosure of both patents and patent applications, wasn't it? A Yes, if they related to the work of the committee."); CX2104 at 851-52 (Crisp, Dep.) (Crisp's understanding of JEDEC's written patent policy was that JEDEC members "wanted to know about both patents and patent application that might relate to the works that were going on within JEDEC.")).

Rambus's Response to Finding No. 820:

The proposed finding is false. JEDEC had no such policy, as thoroughly demonstrated at RPF 108-317. Complaint Counsel's truncated excerpts from Mr. Crisp's testimony and the other cited documents are just as thoroughly misleading. Mr. Crisp understood that any disclosure obligations were borne by *presenters*, not by those merely in attendance. (CX 842 at 1-2; Crisp, Tr. 3484, 3511). And as Complaint Counsel are well aware, the "list of offenders" that Mr. Mooring understood Mr. Kelley would be bringing to the next JEDEC meeting never materialized; it was replaced by a very different statement from Mr. Kelley: "IBM noted that their view has been to ignore [the] patent disclosure rule because their attorneys have advised them that if they do then a listing may be construed as complete." (JX 15 at 6).

821. Rambus representatives acted with knowledge that Rambus's membership in and attendance at JEDEC meetings gave rise to a risk of equitable estoppel, which might prevent Rambus from enforcing its patents against JEDEC members in the future. (CX1942 at 1 (Vincent Notes: "I said there could be equitable estoppel problem if Rambus creates impression on JEDEC that it would not its patent or patent appl[icatio]n"); CX3125 at 321 (Vincent, Infineon Dep.) ("The downside risk was that somebody was going to raise the issue of equitably estoppel if Rambus attended JEDEC"); CX1958 at 1, 15-16 ("Stambler v. Diebold, Inc. . . . Plaintiff's claim is estopped. 'Plaintiff had a duty to speak out and his silence was affirmatively misleading.

Plaintiff could not remain silent while an entire industry implemented the proposed standard and then when the standards were adopted assert that his patents covered what manufacturers believed to be an open and available standard.'"); Diepenbrock, Tr. 6214-17 (Diepenbrock told "Mr. Crisp that he was running a risk that equitable estoppel might apply to his actions at JEDEC." ". . . [T]his risk to Rambus was that some of its patents could be rendered unenforceable").

Rambus's Response to Finding No. 821:

The proposed finding is pure argument. Mr. Vincent's notes and his testimony reflect that he advised Rambus to weigh the "downside risk and the upside potential" and to take steps to avoid misleading JEDEC. (Vincent, Tr. 7995-96). (*See also* Vincent, Tr. 7998) ("I talked about the downside – balancing the downside risk versus the upside potential. That was my analysis."). Rambus followed that advice and did not promote its technology and did not mislead JEDEC members about its intentions. The fact that some litigant in some future lawsuit "could" raise an issue of equitable estoppel, as the proposed finding states, is neither surprising nor controversial. *Each* of the participants at JEDEC took on that risk. The evidence shows that Rambus, by not promoting its technology for standardization, by openly declining to respond to questions about its intellectual property, and by expressly warning JEDEC *not* to rely on its "presence or silence" at JEDEC meetings, avoided that risk. RPF 318-463; 491-515; 544-48.

2. Rambus Understood That Its Interests And Actions as a JEDEC Member Were Contrary to the Purposes and Rules of JEDEC, and It Participated in JEDEC in Bad Faith.

822. Rambus did not participate in JEDEC in good faith. (Sussman, Tr. 1460-61 (Rambus did not comply with "the good faith requirements set forth [in the EIA Legal Guides]"); Kelley, Tr. 2745-46 (Richard Crisp "was not dealing in good faith with me."); Appleton, Tr. 6396 (Micron is asserting its complaint that Rambus was "in violation of antitrust laws, that there was fraud and bad faith."); CCFF 803-821).

Rambus's Response to Finding No. 822:

The proposed finding is false, and the testimony which it cites is irrelevant and unreliable. Mr. Appleton's description of the allegations in Micron's lawsuit against Rambus is not evidence of anything. The other two conclusory charges of bad faith, made by financially interested witnesses, are of no probative value.

Rambus acted at all times in good faith. It did not at any time encourage or push JEDEC to adopt any feature or technology. When it was asked on two occasions at JEDEC meetings if it would care to comment about its intellectual property rights, it declined to do so. *See* RPF 491-515; 544-48. It did not lie and say that it had no such rights; it did not lie and say that it would not assert whatever rights it had. Instead, it openly and publicly declined to comment, and all present understood that it had declined to comment. (*Id.*) Indeed, JEDEC Council and 42.3B Chairman Gordon Kelley testified that Rambus's comment of no comment was "unusual" and "surprising" and constituted "notification to the committee that there should be a concern" about intellectual property issues. (Kelley, Tr. 2579).

This conduct represents the definition of good faith. Rambus misled no one. It lulled no one. It chose, for legitimate business reasons and on the advice of counsel, to keep its patent applications confidential. It had undertaken no duty, and had assumed no obligation, to act otherwise. If it *had* had such a duty, *if* it *had* assumed such an obligation, surely someone at the JEDEC meetings where Rambus declined to comment would have said: "no, you must comment," or "you have agreed to comment," or "the rules require you to comment." No such words were spoken. (*Id.*)

Complaint Counsel have not met their burden of proving that Rambus acted in bad faith

while a JEDEC member.

823. Richard Crisp, the JEDEC representative for Rambus beginning in May 1992, understood that the job of JEDEC was to create, whenever possible, standards that steer clear of patents that must be used in compliance with the standards. (CX0903 at 1; Crisp, Tr. 2941).

Rambus's Response to Finding No. 823:

The proposed finding fails to reveal that the document in question was written *after* Rambus withdrew from JEDEC; it says nothing about Mr. Crisp's state of mind when he was attending JEDEC. The document also says nothing about disclosure obligations. The contemporaneous documents show that Mr. Crisp understood by the fall of 1995 that only *presenters* were expected to disclose patent applications. (CX 842 at 1-2; Crisp, Tr. 3484, 3511).

824. Mr. Crisp believed that the most valuable patents are ones that must be used to be in compliance with the standard. The reason is that such patents cannot be avoided. (CX0903 at 1; Crisp, Tr. 2941 ("Q: And the reason they're valuable is that such patents cannot be avoided. Is that right? A: Well, in the situation to where you want to build a device that's compliant with the standard, whatever the standard is.")).

Rambus's Response to Finding No. 824:

As noted at RRFF 823, the cited document was created after Rambus left JEDEC. The document carries with it no suggestion of wrongdoing in any event, for JEDEC's policy and practice show clearly that it had no qualms about including essential patents in its standards. When the SDRAM standard was balloted for approval in 1993, for example, JEDEC was aware that JEDEC member Hitachi had obtained what could be a "very powerful patent," because it "cover[s] the basic specification for SDRAM." (JX 16 at 26). JEDEC knew at the same time that Motorola had obtained a patent that was "general enough to cover almost any SDRAM design." (JX 16 at 27). The 42.3 committee and the JEDEC council passed the standard anyway. (JX 16 at 5; CX 54 at 8-10).

JEDEC passed the SDRAM standard not just in the face of these powerful, basic patents, but with the knowledge that there might be numerous other patents affecting it. Just before the 42.3 committee voted to send the standard on to the JEDEC council for approval, the official minutes reflect that "IBM noted that their view has been to ignore the patent disclosure rule because their attorneys have advised them that if they do then a listing may be construed as complete." (JX 15 at 6).

None of this evidence should be surprising, for the JEDEC Manual in effect when the SDRAM standard was passed in the spring of 1993 was very clear:

> "JEDEC standards are adopted without regard to whether or not their adoption may involve patents [on] articles, materials or processes."

(CX 205A at 11).

In short, the proposed finding is irrelevant and is not indicative of any wrongdoing or unlawful intent in light of the evidence in the record regarding JEDEC's policies and practices.

825. Rambus pursued interests contrary to those of JEDEC and its members. Rambus never had any plans to manufacture, use or support products that conformed to the JEDEC SDRAM or DDR SDRAM standards. (Crisp, Tr. 2931). Rather, Rambus was promoting its RDRAM architecture. (Crisp, Tr. 2931)

Rambus's Response to Finding No. 825:

The first sentence of the finding does not cite to, and is not supported by, any evidence. It is unrelated to the second and third sentences, which are themselves unobjectionable.

826. Individuals at Rambus, including Mr. Crisp, believed that JEDEC-compliant DDR SDRAMs could be a potential threat to Rambus business. (Crisp, Tr. 2931-32; *see also* CX0831 (Tate identified JEDEC as an example of a competitive DRAM); *see also* CCFF 918, 1089, 1616-24, 1626, 1676-78, 1685, 1687, 1690-95).

Rambus's Response to Finding No. 826:

Rambus has no specific response, except to note that the views ascribed to "individuals at Rambus" did not arise while Rambus was at JEDEC.

827. Mr. Crisp, Billy Garrett, and others at Rambus hoped that JEDEC would fail to develop a widely used standard for SDRAM and DDR SDRAM, as they did not want to see potential competitive devices appear on the market. (CX0672 at 1 (Garrett e-mail: "SDRAMs will happen. They may happen sooner than we want, and they may become quite standardized and highly multi-sourced."); CX1708 at 3 ("It really looks like there is a lot of momentum against us in the main memory arena. It seems like the group is pretty set on using the SDRAMs for memory."); Crisp, Tr. 2933 ("Q: You didn't have any particular interest in seeing JEDEC succeed in developing a widely used standard for SDRAM, did you? A: I think that answer is correct, yes. Q: You also didn't have any interest in seeing JEDEC succeed in developing a widely used standard for DDR SDRAM, did you? A: I was not interested in seeing potential competitive devices appear on the market.")).

Rambus's Response to Finding No. 827:

Rambus agrees that it did not advocate, promote or vote in favor of the standardization of the SDRAM device.

828. Mr. Crisp withheld technical information that might have helped JEDEC. (CX0711 at 23 (Crisp May 1994 email: "The key thing everyone is missing is the failure to appreciate that the pinouts set over a year ago eliminate the possibility of routing the clocks in a way that naturally avoids the problems of clock skew"); CX0711 at 169 (Crisp September 1995 email: "Another thing they are going to do is have VTT track Vref, which Srinivas tells me is something we have determined to be a no-no based on our work in the lab").").

Rambus's Response to Finding No. 828:

Complaint Counsel do not suggest that Rambus or Mr. Crisp were required to assist in the development of the SDRAM device. Indeed, it is likely that if Mr. Crisp *had* been offering technical advice to JEDEC on how to improve its SDRAM devices, instead of simply sitting quietly during the meetings, Complaint Counsel would now be arguing that Rambus's active involvement in the development of the standard caused it to take on disclosure obligations with

respect to intellectual property.

829. Rambus voted "no" on four ballots relating to technologies proposed for the SDRAM standard. (CCFF 921-27). As least some JEDEC members believed that Rambus was voting "no" in an attempt to delay completion of a standard that would compete with RDRAM. (Sussman, Tr. 1395 (" . . . the activity of Rambus was more to delay the standardization process as this was basically a competing option for the Rambus DRAM, so not assisting in the standards.")).

Rambus's Response to Finding No. 829:

Rambus agrees that it did not promote, urge the adoption of, or assist in the development of the SDRAM standard, and that JEDEC members were aware of these facts.

830. At the very first JEDEC meeting he attended for Rambus, Mr. Crisp witnesses some dissension among some JEDEC members at the meeting, and suggested to Rambus colleagues that word of the dissension be leaked to the press to the competitive advantage of Rambus. (CCFF 893-99; Crisp, Tr. 2934-35; CX1708 at 5). Mr. Crisp told his colleagues that such an action could lead to censure by JEDEC but "should help our air war." (CX1708 at 5; Crisp, Tr. 2935 (the term "air war" referred to the desire of Rambus to have people use the proprietary RDRAM architecture)).

Rambus's Response to Finding No. 830:

The proposed finding is irrelevant, because there is no evidence that the referenced conduct occurred.

831. Gordon Kelley identified a proposal to plant a story with the press about dissension within JEDEC as "an example of not having good faith or not showing good faith" because it could "undermine the JEDEC process." (G. Kelley, Tr. 2523-24).

Rambus's Response to Finding No. 831:

The proposed finding is irrelevant, because there is no evidence that the referenced conduct occurred.

832. Knowing that JEDEC's purpose was to develop open standards, Rambus, without informing JEDEC, nevertheless used information obtained from JEDEC to ensure that it developed patents with claims that covered the JEDEC standards. (CCFF 885-92, 900-01, 910, 917, 918, 932-36, 937, 939, 945, 948, 958, 962-67, 981, 987-93, 100-03, 1004-08, 1018-24,

1028-29, 1040, 1049, 1069, 1074-77, 1089, 1098-99).

Rambus's Response to Finding No. 832:

The proposed finding presents several issues. First, the definition of "open standard" that comports with the weight of the evidence is a definition that *allows* patented technologies to be incorporated within the standard, as long as the relevant patents are available "to all parties on reasonable, non-discriminatory terms." (RX 669 at 4). (*See also* Kelly, Tr. 2072, CX 419 at 1; RX 669 at 2, 4). Rambus's royalty terms and rates fully comply with this definition. *See* RPF 1361-1422.

Second, Complaint Counsel do not and cannot contend that Rambus's patents claim inventions that Rambus's founders did not, in fact, invent. Because Complaint Counsel have said repeatedly that they will not challenge in this case the determination by the Patent and Trademark Office that Drs. Farmwald and Horowitz invented the subject matters claimed in the patents, they cannot contend that Rambus "stole" its inventions from JEDEC. Complaint Counsel also stated "very clear[ly]" in their opening statement that they "do *not* claim that Rambus's use of information obtained from attending JEDEC meetings amounts to misappropriation or somehow renders Rambus's patents invalid." (Opening Statement, Tr. 49-50) (emphasis added).

In addition, JEDEC Council Chairman Gordon Kelley testified without qualification that he "did not understand that the use of JEDEC confidential information was an abuse as long as the people using the information were members." (Kelley, Tr. 2626).

833. One of the reasons why Rambus began attending JEDEC meetings was to learn what its competition was working on. (CX0837 at 1-2) (Crisp 1995 email: "At the time we began attending JEDEC we did so to learn what the competition was working on and what sort of

performance systems using that technology would be able to achieve and what sorts of issues would arise when designing with the devices (primarily SDRAM/SGRAM).").

Rambus's Response to Finding No. 833:

The finding is irrelevant and, if it is intended to suggest that Rambus's motivation was inappropriate, misguided. For example, JEDEC Council and 42.3B Chairman Gordon Kelley testified that he and Siemens' JEDEC representative Willi Meyer were *each* reporting on JEDEC activities to a joint DRAM development team that IBM and Siemens had created. (Kelley, Tr. 2621-22). Mr. Kelley testified that he "did not understand that the use of JEDEC confidential information was an abuse as long as the people using the information were members." (Kelley, Tr. 2626).

Even today, JEDEC tries to drum up new members by pointing to the competitive advantages of membership, or perhaps the *dis*advantages of *non*-membership. (CX 302 at 17 – Rhoden presentation entitled "A Look Inside JEDEC" points to "[p]rivate web access for ongoing work" and warns that "[i]f you are not there, your competition may be deciding your future."). Dr. Oh was even more blunt when describing why Hyundai joined JEDEC:

> "We wanted to propose things to be adopted at the JEDEC meeting. That means if our proposal is – is adopted, that means we are ahead of our competitors, so we actively decided to attend and join the JEDEC committee."

(CX 2108, Oh Depo. at 23:24-24:5).

834. Rambus used the information it obtained at JEDEC to help refine the claims in its pending patent applications to ensure that its claims would cover the JEDEC standards. (CX2092 at 192 (Crisp, Infineon Tr.) ("Q: Am I right, sir, that Rambus was intentionally drafting claims to intentionally cover JEDEC SDRAMs? A: Partially true, yes."); CX0831 (Tate e-mail:

"tony's #1 objective right now is to understand competitive technology, get up to speed on all of our patents filed, assess how many and how strong our current patents /claims are vs. competition, and determine what should proactively be done to strengthen our IP position relative to competition"; and requesting staff to forward to him copies of JEDEC meeting reports).

Rambus's Response to Finding No. 834:

Complaint Counsel do not and cannot contend that Rambus's patents claim inventions that it did not, in fact, invent and that were instead developed at JEDEC meetings. Complaint Counsel have said repeatedly that they do not and will not challenge in this case the determination by the Patent and Trademark Office that Drs. Farmwald and Horowitz invented the subject matters claimed in the patents, and that they do not claim that Rambus misappropriated information from JEDEC meetings. (Opening Statement, Tr. 49-50). (*See also* Kelley, Tr. 2626 (members may use JEDEC confidential information)).

835. During his time as JEDEC representative for Rambus, Mr. Crisp learned that meetings of JEDEC committees and subcommittees were conducted in accordance with the EIA Legal Guides. (Crisp, Tr. 2945).

Rambus's Response to Finding No. 835:

Rambus has no specific response.

836. Mr. Crisp was aware that the EIA Legal Guides provided that all EIA standardization programs shall be carried on in good faith. (Crisp, Tr. 2946-47).

Rambus's Response to Finding No. 836:

Rambus has no specific response.

837. Mr. Crisp was aware that JEDEC was controlled by EIA rules regarding use of patents. (Crisp, Tr. 2947-48). Mr. Crisp understood that the EIA rules stated that requirements in EIA standards which called for the use of patented items should be avoided. (Crisp, Tr. 2948). Mr. Crisp understood that the EIA rules provided that no program of standardization

should refer to a product on which there is a known patent unless all the technical information covered by the patent was known to the standards committee. (Crisp, Tr. 2948).

Rambus's Response to Finding No. 837:

Complaint Counsel did not ask Mr. Crisp whether he had the referenced understanding while he was a JEDEC representative. (Crisp, Tr. 2947-48). The evidence does not, therefore, support the proposed finding.

838. Mr. Crisp understood that the purpose of JEDEC was to develop open standards. (CX0903 at 2 (Crisp e-mail: "The job of JEDEC is to create standards which steer clear of patents which must be used in compliance with the standard whenever possible.")).

Rambus's Response to Finding No. 838:

The finding is vague as to time; the e-mail was written after Rambus stopped attending JEDEC meetings.

839. Mr. Crisp understood that JEDEC and its members were concerned about a company enforcing patents against companies practicing a JEDEC standard. (CX0711 at 1 (Crisp e-mail: "TI was chastized for not informing JEDEC that it had a 1987 patent on quad CAS devices . . . The bottom line is that all quad CAS devices will be removed from standard 21C."); CX0711 at 16 (Crisp e-mail: "The whole [quad CAS] issue got pretty nasty . . . Sussman . . . made a motion that TI withdraw from JEDEC pending resolution of the patent issue!"); CX0903 at 2 (Crisp e-mail: "The job of JEDEC is to create standards which steer clear of patents which must be used in compliance with the standard whenever possible.")).

Rambus's Response to Finding No. 839:

The Texas Instruments "Quad Cas" issue does not support the finding. Once TI promised to license its patents on "RAND" terms, the dispute ended and all ballots seeking to withdraw the Quad Cas feature were themselves withdrawn. (JX 25 at 5; Kellogg, Tr. 5022-26). The other cited exhibit, CX 903, was prepared after Rambus left JEDEC. Moreover, the EIA in 1996 informed the FTC, on behalf of JEDEC and its other standards activities, that "[a]llowing patented technologies in standards is procompetitive" and that "the important issue is the license

availability to all parties on reasonable, non-discriminatory terms." (RX 669 at 2, 4).

840. Mr. Crisp, during the time he was the primary JEDEC representative for Rambus, understood that there was a patent policy at JEDEC. (Crisp, Tr. 2949). One of the ways that Mr. Crisp learned of the patent policy was because at the meetings of the JC42.3 Committee that Mr. Crisp attended, Jim Townsend generally started the meeting with a discussion of the patent policy. (Crisp, Tr. 2949).

Rambus's Response to Finding No. 840:

The finding mischaracterizes the examination. Counsel's question asked Mr. Crisp if he "came to understand" that there was a patent policy at JEDEC at some point while he was attending meetings.

841. Mr. Crisp was aware that JEDEC had a disclosure policy requiring disclosure of patents and patent applications. (CX2104 at 851-52 (Crisp, Micron Dep.) (Crisp's understanding of JEDEC's written patent policy was that JEDEC members "wanted to know about both patents and patent application that might relate to the works that were going on within JEDEC."); CX2092 at 168 (Crisp, Infineon Tr.) ("Q: And what [the slide] said and what [Mr. Townsend] said to everyone in the committee is that the policy applied equally to patent applications as it did to patents, right? A: I think he said that. I don't remember it very clearly, but I think he said that.")).

Rambus's Response to Finding No. 841:

Mr. Crisp testified that *presenters* were expected to disclose applications. (Crisp, Tr. 3474-78; 3484-85).

842. Mr. Crisp and other Rambus representatives knew that certain JEDEC members disclosed patent applications at JEDEC. (Crisp, Tr. 2950-51) ("Q: And you recall that that [patent tracking list] includes not just patents, but also patent applications? A: I think it included a few patent applications from my recollection."); CX2104 at 851-52 (Crisp, Micron Dep.) (Crisp's understanding of JEDEC's written patent policy was that JEDEC members "wanted to know about both patents and patent application that might relate to the works that were going on within JEDEC."); CX0672 at 1 (Garrett email: "Fujitsu indicated that they do have patents applied for, but that they will comply with the JEDEC requirements to make it a standard!!!"); CX685 at 1 (Mooring e-mail: "IBM raised the issue that they were aware that some "voting" JEDEC attendees have patents pending on SDRAMs that they have not made the committee aware of. They will come to the next meeting with a list of the offenders.")).

Rambus's Response to Finding No. 842:

Mr. Crisp testified that he understood from the subcommittee chairman's statements that disclosures involving patent applications were not required:

> "Q: What do you remember Gordon Kelley saying about the disclosure of patents or patent applications?
>
> A: He said he wasn't going to do it.
>
> Q: Wasn't going to do what?
>
> A: Disclose patent applications.
>
> Q: What do you remember him saying?
>
> A: I remember him saying that IBM was not going to disclose patent applications at the – at the JEDEC meetings.
>
> Q: Did you – did you reach any conclusion from hearing that?
>
> A: Yes, I did.
>
> Q: What was your conclusion?
>
> A: The disclosure of patent applications was not a requirement.
>
> Q: After that meeting in December 1993, did you ever see any IBM representative disclose a patent application at a JEDEC meeting?
>
> A: No, sir."

(Crisp, Tr. 3503-04).

843. Throughout the period when Rambus participated in JEDEC, Mr. Garrett and Mr. Crisp informed executives and others at Rambus that JEDEC members disclosed pending patent applications that pertained to the work at JEDEC. (E.g. CCFF 882-83, 1080; CX0672 at 1 (Garrett email reporting February 1992 disclosure of Fujitsu patent application); CX0711 at 169 (Crisp September 1995 email: "Fujitsu stated yesterday that they have patents pending on

SSTL"); CX0711 at 192 (Crisp December 1995 email: "MOSAID has a pending patent application for PLL/DLL on SDRAMs . . . they will be in compliance with the JEDEC patent policy."); *see also* CX0685 at 1 (Mooring December 1992 email noting IBM comment that some "JEDEC attendees have patents pending on SDRAMs")).

Rambus's Response to Finding No. 843:

See RRFF 842.

844. Mr. Crisp was aware of the patent tracking lists shown by Mr. Townsend, which included both patents and patent applications. (Crisp, Tr. 2950). Mr. Crisp received minutes from JEDEC meetings, which generally included the slides from Mr. Townsend's presentations concerning the patent policy. (Crisp, Tr. 2951).

Rambus's Response to Finding No. 844:

Rambus has no specific response.

845. As of mid-1995, Rambus representative Mr. Crisp knew that JEDEC manual 21-I called for the disclosure of patent applications. (CX2092 at 60 (Crisp, Infineon Tr.) ("Sometime in 1995 I received a copy of the patent policy as part of the users in the manual that they had that was to be used to tell people what the rules were. And I read in there that it applied to patent policies. Q: Patent applications? A: Patent applications, that's right."); CX2104 at 950-51 (Crisp, Micron Dep.) ("Q And when you got it [JEDEC manual 21-I] and read it, then it was clear that the manual required disclosure of both patents and patent applications, wasn't it? A Yes, if they related to the work of the committee.")).

Rambus's Response to Finding No. 845:

The proposed finding is incomplete and misleading because it does not distinguish between presenters and non-presenters. Mr. Crisp testified that as a result of his review of the JC 42 members' manual, and as a result of his attendance at meetings where Mr. Kelley stated that IBM would not disclose its patent applications, he understood that only *presenters* were expected to disclose patent applications. (Crisp, Tr. 3474-78; 3484-85). This same understanding was expressed by the JEDEC representative form Molex, Jim McGrath. (McGrath, Tr. 9273-74).

846. During the period when Rambus participated in JEDEC, Mr. Crisp spoke with Desi Rhoden, longtime member of JEDEC and later Chairman of JEDEC (Rhoden, Tr. 283, 284-85), to inquire about the JEDEC patent disclosure policy. (Rhoden, Tr. 518-19). Mr. Crisp inquired specifically about the application of the policy to patent applications; Mr. Rhoden informed Mr. Crisp that in the patent disclosure policy, the word patent applied to everything that was in the patent process, and necessarily included patents and patent applications. (Rhoden, Tr. 519).

Rambus's Response to Finding No. 846:

Mr. Rhoden's testimony is not corroborated by any written evidence and is not credible. Mr. Rhoden has a strong financial interest in the outcome of the matter; his sole employment income over the past four years has come from his position at AMI2, which is funded and controlled by DRAM manufacturers. (Rhoden, Tr. 287-88; 699). Moreover, Mr. Rhoden's testimony is inconsistent with his own conduct in failing to disclose a patent application *on which he was a named inventor* that covered the precise specification for the SLDRAM pinout that was standardized by JEDEC. (RX 2086 at 1; Rhoden, Tr. 1206-1211, 1219).

Mr. Rhoden also testified that as he understood the JEDEC patent policy, disclosure was not required if the patent application had been filed after the standard had passed. (Rhoden, Tr. 1211-12). It is safe to presume that *if* Mr. Rhoden spoke to Mr. Crisp about the JEDEC patent policy, as he claims, he would have informed Mr. Crisp of this same understanding. Mr. Crisp would have therefore understood that Rambus had nothing to disclose, for as the parties have stipulated, "Prior to the adoption of the JEDEC SDRAM standard in 1993, Rambus had no claims in any pending patent application that, if issued, would have necessarily been infringed by the manufacture or use of any device manufactured in accordance with the 1993 JEDEC SDRAM standard." (The Parties' First Set of Stipulations, entered April 24, 2003, p. 2).

847. Mr. Rhoden told Mr. Crisp that if he would like to have a legal opinion, he could contact John Kelly. (Rhoden, Tr. 519). During the time that Rambus was a member of JEDEC,

Rambus never contacted John Kelly, the legal counsel for JEDEC, with any questions about EIA's or JEDEC's rules. (J. Kelly, Tr. 2057).

Rambus's Response to Finding No. 847:

Rambus has no specific response.

848. On at least two separate occasions, Mr. Crisp refused to respond to questions from Mr. Gordon Kelley, the Subcommittee Chairman, regarding the possible existence of Rambus patents relating to a presentation at JEDEC. (May 1992: CCFF 902-909, 1247-48; CX0673 at 1 ("Gordon Kelley of IBM asked me if we would comment which I declined."); CX2089 at 130-131, 136-137 (Meyer, Infineon Trial Tr.); September 1995: CCFF 1044, 1062-68; JX0027 at 26 ("At this time, Rambus elects to not make a specific comment on our intellectual property position relative to the Synclink proposal.")).

Rambus's Response to Finding No. 848:

Rambus has prepared extensive findings regarding the two referenced meetings. *See* RPF 466-529, 544-548.

849. Rambus knew that its failure to disclose the existence of its issued '327 patent and its pending patent applications to JEDEC could serve to equitably estop Rambus from enforcing its patents as to JEDEC participants. (Order, February 26, 2003 at 9; Order, February 27, 2003; *see also* CCFF 885-91, 955-57, 1056-61, 1083-87, 1090).

Rambus's Response to Finding No. 849:

Neither the cited Orders nor the referenced findings have any application to the '327 patent. Rambus has never asserted the '327 patent against any device built in compliance with a JEDEC standard, and the '327 patent does not cover any device built in compliance with a JEDEC standard. *See* RPF 354-56.

In addition, Rambus had no undisclosed claims in any pending patent applications while it was a JEDEC member that, if issued, would have necessarily been infringed by the manufacture or use of any device manufactured in accordance with JEDEC's SDRAM standard. Thus, the cited Orders and findings do not support the conclusion stated in the finding. In

addition, Complaint Counsel have not met their burden of proving that Rambus's JEDEC representative, Richard Crisp, had actual knowledge of any claim that Complaint Counsel assert should have been disclosed.

850. Rambus representatives understood that Rambus's membership in and attendance at JEDEC meetings gave rise to a risk of equitable estoppel. Rambus representatives understood that risk to be that the doctrine of equitable estoppel might prevent Rambus from enforcing its patents against JEDEC members in the future. (CCFF 885-91, 955-57, 1056-61, 1083-87, 1090; CX1942 at 1 (Vincent notes: "I said there could be equitable estoppel problem if Rambus creates impression on JEDEC that it would not its patent or patent appl[icatio]n"); CX3125 at 321 (Vincent, Infineon Dep.) ("The downside risk was that somebody was going to raise the issue of equitably estoppel if Rambus attended JEDEC"); CX1958 at 1, 15-16 ("Stambler v. Diebold, Inc. . . . Plaintiff's claim is estopped. 'Plaintiff had a duty to speak out and his silence was affirmatively misleading. Plaintiff could not remain silent while an entire industry implemented the proposed standard and then when the standards were adopted assert that his patents covered what manufacturers believed to be an open and available standard.'"); Diepenbrock, Tr. 6214-17 (Diepenbrock told "Mr. Crisp that he was running a risk that equitable estoppel might apply to his actions at JEDEC." ". . . [T]his risk to Rambus was that some of its patents could be rendered unenforceable")).

Rambus's Response to Finding No. 850:

Rambus agrees that it sought and obtained the advice of counsel regarding its participation in JEDEC and that counsel discussed the doctrine of equitable estoppel with Rambus employees and provided guidelines as to permissible conduct. Rambus followed that advice. *See* RPF 446-459.

851. On at least seven separate occasions, Rambus in-house or outside legal counsel informed Rambus representatives, including Rambus CEO Geoff Tate, Rambus Vice President Allen Roberts, and Rambus's primary JEDEC representative Richard Crisp, that they faced a risk that, based on Rambus's participation in JEDEC, the doctrine of equitable estoppel might preclude Rambus from enforcing its patents against JEDEC members. (CCFF 885-91, 955-57, 1056-61, 1083-87, 1090; CX1942 (Vincent notes, 3/27/92: "I said there could be equitable estoppel problem"); CX1958 at 1, 12 (Vincent letter and attachment, 5/5/93: "Two possible legal theories for non-enforcement: 1) estoppel? 2) antitrust?"); CX3126 at 552-54 (Vincent, Dep.) (at some point in time, Vincent talked with Crisp about the upside potential versus downside risk of participating in standard setting bodies); CX0837 at 1 (Crisp e-mail, 9/23/95: "Tony's worst case scenario regarding estoppel"); CX1990 at 1 (Vincent letter, 12/19/95 ("the [FTC] charged that

Dell restricted competition in the personal computer industry and undermined the standard-setting process by threatening to exercise undisclosed patent rights against computer companies adopting the VL-Bus standard."); CX3124 at 190-94 (Vincent, Dep.) (describing meeting over lunch with Geoff Tate and Maria Sobrino at which they discussed the Dell consent order); CX3126 at 537-40 (Vincent, Dep.) (describing 1/11/96 meeting at Rambus to discuss the Dell consent order and the IEEE letter); *see also* CX3126 at 554 (Vincent, Dep.) (Vincent may have had another conversation with Crisp and Tony Diepenbrock); CX3127 at 113-14 (Vincent, Dep.) (same)).

Rambus's Response to Finding No. 851:

Rambus agrees that it sought and obtained the advice of counsel regarding its participation in JEDEC and that counsel discussed the doctrine of equitable estoppel with Rambus employees and provided guidelines as to permissible conduct. Rambus followed that advice. *See* RPF 446-459.

852. Lester Vincent does not recall being aware of the EIA Legal Guides, the JEDEC Manual 21-I, the Townsend presentations at the JC-42.3 meetings, the patent tracking list, the JEDEC sign-in sheet, internal Rambus emails discussing disclosures within JEDEC, specific requests made to Rambus regarding Rambus patents, any specific presentations made within JEDEC, or emails within Rambus commenting on whether presentations at JEDEC would be covered by Rambus patent rights. (Vincent, Tr. 7996-98). Yet, he still advised Rambus that there was a downside risk that somebody could raise the issue of equitable estoppel. (CX3126 (Vincent Dep. at 191, 197, 320); CX3127 (Vincent Dep. at 114-115); *see also* CX1928 (Vincent notes, undated: ("– No further participation in any standards body (if there has been any) – do not even get close!!")).

Rambus's Response to Finding No. 852:

The proposed finding is pure argument. Mr. Vincent's notes and his testimony reflect that he advised Rambus to weigh the "downside risk and the upside potential" and to take steps to avoid misleading JEDEC. (Vincent, Tr. 7995-96). (*See also* Vincent, Tr. 7998) ("I talked about the downside – balancing the downside risk versus the upside potential. That was my analysis."). Rambus followed that advice and did not promote its technology and did not mislead JEDEC members about its intentions. The fact that some litigant in some future lawsuit "could"

raise an issue of equitable estoppel, as the proposed finding states, is neither surprising nor controversial. *Each* of the participants at JEDEC took on that risk. The evidence shows that Rambus, by not promoting its technology for standardization, openly declining to respond to questions about its intellectual property, and by expressly warning JEDEC *not* to rely on its "presence or silence" at JEDEC meetings, avoided that risk. *See* RPF 318-463; 491-515; 544-48.

853. Rambus knew or should have known from its pre-1996 participation in JEDEC that developing JEDEC standards would require the use of patents held or applied for by Rambus. (See Order, February 26, 2003 at 9; *see also* CCFF 884, 887, 892, 900-01, 910, 917, 918, 932-36, 937, 938, 939, 948, 958, 962-67, 987-93, 7000-03, 1004-08, 1009-17, 1018-25, 1028-30, 1040, 1049, 1057-58, 1069, 1073, 1077, 1089, 1098).

Rambus's Response to Finding No. 853:

Complaint Counsel's reliance on the first rebuttable presumption set forth in Judge Timony's February 26, 2003 Order is misplaced. Rambus has rebutted that presumption, and each of the presumptions, imposed on it by that Order.

Under settled law, in order to rebut these presumptions, Rambus was required only to produce evidence that would be sufficient to support a finding contrary to the presumed fact. In other words, the effect of the presumption was to shift the burden of going forward to Rambus, but ultimately to leave the burden of proof – a burden of proof that must be borne by Complaint Counsel – intact. *See* 21 Wright and Graham, Fed. Prac. & Proc. § 5122 at 571 (explaining that the quantum of evidence that one must produce to rebut the facts inferred or presumed from one's document destruction is, at most, the burden of producing evidence "sufficient to support a finding of non-existence of the presumed fact.") *See also A.C. Aukerman Co. v. R.L. Chaides Constr. Co.*, 960 F.2d 1020, 1037 (Fed. Cir. 1992); *In the Matter of Novartis Corp.*, 1999 FTC

LEXIS 63 at *26 (1999).[2]

Judge Timony's first rebuttable adverse presumption was that "Rambus knew or should have known from its pre-1996 participation in JEDEC that developing JEDEC standards would require the use of *patents held or applied for* by Rambus." As discussed elsewhere, Rambus has rebutted this presumption by establishing the following propositions: (1) Rambus did not have any issued patents or claims in any pending patent applications prior to June 1996 that "read on" any so-called "developing JEDEC standards" that were then in effect or that had been proposed during that time frame (*e.g.,* RPF 318-416; RIB 49-63); (2) although there were short periods of time when some at Rambus believed that it was seeking patent coverage over certain features that were then being considered for inclusion in future products, analysis in each instance corrected this mistaken belief and clarified that in fact Rambus had filed no such patent claims (RPFF 417-31); and (3) at no time did Richard Crisp or any other Rambus officer or employee believe that Rambus possessed any patents or patent applications that Rambus was required to disclose to JEDEC. (*Id.*). Thus, this inference has been fully rebutted.

Moreover, a portion of this inference is that Rambus "should have known" that it had patent claims or claims in patent applications that covered "developing JEDEC standards." The record evidence has established beyond question that what someone "should have known" is not a relevant or material fact in this proceeding; the only knowledge that matters with respect to any JEDEC disclosure is the *actual* knowledge, not of the company, but of the JEDEC representative. (Rhoden, Tr. 624 (disclosure obligation "triggered by the actual knowledge of the people that

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[2] To impose any higher burden on Rambus would improperly shift the burden of proof that must be borne by Complaint Counsel. *See, e.g., United States v. Baker Hughes, Inc.*, 908 F.2d 981, 983 (D.C. Cir. 1990).

were involved"); Kelly, Tr. 1970 (any obligation applied only "to [] participants with actual knowledge")). Complaint Counsel have not met their burden of proving that Mr. Crisp had actual knowledge that the claims contained in any Rambus patent or patent application covered or read on any of the technology or features proposed for standardization while Rambus was a JEDEC member. *See* RPF 417-431; Crisp, Tr. 3464-66; 3540-43.

854. Mr. Crisp admitted that he went to JEDEC meetings and saw proposals for standardization for SDRAM; that following the presentations he or others met with the Rambus's outside patent lawyer to work on claims for pending Rambus patent applications; and that the intent was to make the claims broad enough that they would cover an SDRAM using the features that Mr. Crisp had seen at the JEDEC meetings. (CX2092 at 70-72 (Crisp, Infineon Trial Tr.) ("Q: And what you did in those meetings [with the Rambus patent lawyer] was work on new claims for the Rambus pending patent applications, and your intent was to make them broad enough that they would cover an SDRAM using the features you had seen at the prior [JEDEC] meetings. Isn't that right? A: In some cases that was true."); *id*. at 134 (". . . Rambus was adding claims, in Rambus' words, specifically directed to the SDRAM; isn't that right? . . . A: I believe that there were some people at Rambus that were attempting to do that."); *id*. at 139-40 (after the July 1992 JEDEC meeting, he had conversations with Mr. Vincent about amending or adding claims to the original 1990 application); *id*. at 132 ("Q: And the ideas that you had to add claims to the Rambus patent applications for the mode register and for programmable CAS latency, those were ideas that were spurred on by your attendance at the JEDEC meeting in April and May and participating in this SDRAM effort, right? A: Yeah. Those were our inventions. We had invented those for the RDRAM."); *id*. at 192 ("Q: Am I right, sir, that Rambus was intentionally drafting claims to intentionally cover JEDEC SDRAMs? A: Partially true, yes.")).

Rambus's Response to Finding No. 854:

The proposed finding is compound, ambiguous as to time frame, and relies upon misleading and truncated snippets of testimony. Moreover, it omits Mr. Crisp's testimony that he was unaware while attending JEDEC meetings of whether or not Rambus had filed any applications with claims over any features found in SDRAMs, and it omits his testimony that upon reviewing a collection of Rambus's patents and patent applications in the summer of 1995, he saw no Rambus patent or application that had claims that "applied to SDRAM." (Crisp,

Tr. 3464-66; 3540-43).

855. Programmable CAS latency, programmable burst, double edge data transfer and PLL/DLL, as related to the patents asserted against Infineon by Rambus, were all technologies that Mr. Crisp saw discussed at JEDEC and for which Rambus had patent applications that covered aspects of the technologies. (CX2092 at 258-59 (Crisp, Infineon Trial Tr.) ("Q: And those are the very features that you saw at JEDEC and that you met with your lawyer about and that Rambus' patent applications ultimately changed into; isn't that right? A: I think those issues were discussed there in some form or another, and we certainly had patent applications that covered aspects of those, of those technologies.")).

Rambus's Response to Finding No. 855:

The cited testimony does not support the finding; the finding is inconsistent with the Parties' First Set of Stipulations, item 9, with the weight of the evidence in this case, and with the Federal Circuit's opinion in the *Infineon* case. *See* RPF 361-396.

856. While Rambus was a member of JEDEC, Mr. Garrett or Mr. Crisp saw JEDEC members propose to incorporate into a JEDEC standard:

1. low voltage swing signaling,
2. programmable CAS latency,
3. programmable burst/wrap length,
4. externally supplied reference voltage,
5. two banks,
6. dual edge output/input,
7. source synchronous clocking,
8. auto-precharge, and
9. on-chip PLL or DLL.

(Crisp, Tr. 3024, 3035-45, 3052-53; 3107-08, 3165, 3200-3201; *see also* DX0028; CX0670 at 1 (programmable latency and wrap length, single clock edge); CX0672 at 1 (two banks, reduced voltage swing parts); CX1708 at 2 (source synchronous clocking); CX0680 at 1-2 (programmable latency, programmable burst length, two banks, auto-precharge); CX0711 at 25, 31 (externally supplied reference voltage); CX0711 at 52, 54 (externally bussed reference voltage); CX0711 at 36-37 (on-chip PLL); CX0711 at 56, 58 (source synchronous clocking); CX1320 (double edge clocking); CX0905 (CX1320 contained confidential JEDEC material); *See also* CCFF 876, 894, 901, 919, 925, 926, 930, 933, 937, 939, 948, 960, 962-65, 989-93, 997-98, 1000-03, 1004-06, 1010-16, 1032, 1037, 1045, 1070-73, 1078-81, 1098).

Rambus's Response to Finding No. 856:

The proposed finding is vague and irrelevant. All of the nine technologies listed in the proposed finding are vague terms that can each cover a host of different implementations. Absent some detail of what was actually being proposed and how it related to, if at all, to Rambus's intellectual property, the proposed finding is irrelevant.

Moreover, even assuming that JEDEC members were obligated to disclose some intellectual property interests at JEDEC meetings while Rambus was a member, the evidence shows that that obligation was not triggered until the time that a proposal was balloted for approval. (RPF 296-300). Absent some indication of whether any of the "proposals" referenced was actually balloted approval, the proposed finding is irrelevant.

Finally, with respect to five of the nine technologies listed, low voltage swing signaling, externally supplied reference voltage, two banks, source synchronous clocking, and auto-precharge, Complaint Counsel have not even attempted to make a showing that any implementation of the technology discussed at JEDEC was covered by any pending Rambus patent claims.

Complaint Counsel cite as support for this proposed finding numerous other proposed findings; Rambus responds to each of those proposed findings below and will not repeat the responses here.

857. While Rambus was a member of JEDEC, Mr. Garrett or Mr. Crisp believed that Rambus might have pending applications containing claims covering, or be able to obtain – based on its April 1990 application – patent rights covering:

1. low voltage swing signaling,
2. programmable CAS latency,
3. programmable burst/wrap length,
4. externally supplied reference voltage,

5. two banks,
6. dual edge output/input,
7. source synchronous clocking,
8. auto-precharge, and
9. on-chip PLL or DLL.

(Crisp, Tr. 3027-3028, 3060-64, 3104-08, 3164-71, 3178-80; CX1949 at 1 (Vincent notes: "*1) DRAM – multiple open row addresses 2) DRAM – programmable latency via control reg . . . 4) using phase lock loop on DRAM . . ."); *id*. at 5 ("must claim source synch clocking"); CX0672 (regarding reduced voltage-swing parts: " . . . we could use our patents to keep current-mode interfaces off of DRAMs . . ."); CX0702 (identifying programmable CAS latency, DRAM with PLL clock generation, DRAM with multiple open rows, DRAM with externally supplied reference voltage, and DRAM using low-voltage-swing signal levels); CX0738 ("We may be able to make a broader claim on auto-precharge for any DRAM . . ."); CX0734 (Roberts believed that, based on the teachings of the '898 application, Rambus could enhance its claim coverage with respect to, *inter alia*, "Use of both edges of the clock," "Multiple . . . internal DRAM memory regions (banks)," "selective precharging of banks" and "Use of control registers . . . which control RAS and CAS access timing"); CX1949; CX0711 at 25, 31 (regarding externally supplied reference voltage: "(Allen, I believe this was one of the claims you, Lester, Tracy and I wrote up in late '91, right?"); CX0711 at 36-37 ("What is the exact status of the patent with the PLL claim?****"); CX0711 at 56, 58 (regarding source synchronous clocking: "Of course they may get in to patent trouble if they do this"); *see also* CCFF 876, 894, 901, 919, 925, 926, 930, 933, 937, 939, 948, 960, 962-65, 989-93, 997-98, 1000-03, 1004-06, 1010-16, 1032, 1037, 1045, 1070-73, 1078-81, 1098).

Rambus's Response to Finding No. 857:

The proposed finding is vague and irrelevant. All of the nine technologies listed in the proposed finding are vague terms that can each cover a host of different implementations. Without some detail of what Mr. Crisp or Mr. Garrett believed Rambus might have pending applications or patent rights covering, and how it related to, if at all, JEDEC work, the proposed finding is irrelevant.

Moreover, the evidence shows that, even if JEDEC members were obligated to disclose some intellectual property interests at JEDEC meetings while Rambus was a member, that obligation was triggered by the "actual knowledge" of the JEDEC representative of the

intellectual property and its relationship to a standard; a question as to whether the representative's company might have intellectual property is not sufficient. (RPF 288-95). Absent some indication that either Mr. Crisp or Mr. Garret had such actual knowledge, the proposed finding is irrelevant.

Finally, with respect to five of the nine technologies listed, low voltage swing signaling, externally supplied reference voltage, two banks, source synchronous clocking, and auto-precharge, Complaint Counsel have not even attempted to make a showing that any implementation of the technology discussed at JEDEC was covered by any pending Rambus patent claims.

Complaint Counsel cite as support for this proposed finding numerous other proposed findings; Rambus responds to each of those proposed findings below and will not repeat the responses here.

858. Every patent that Rambus has asserted in patent litigation involving the SDRAM and DDR standards can trace its lineage to one of two patent applications in the '898 family: either the 08/222,646 ("'646") or the 07/847,961 ("'961"). (First Stipulations, No. 22; Exhibit A to First Stipulations, No. 22; Nusbaum Tr. 1506-1508; see also DX0014). The '646 and '961 applications, as well as the '490 application which was a continuation of the '961 application, and the '327 patent which issued from the '646 application, were pending while Rambus was a member of JEDEC (CCFF 1008, 1028, 1049, 1076-77, 1092-95) and contained claims that related to ongoing work at JEDEC (CCFF 1028, 1049, 1125-63, 1164-82, 1199-1215, 1216-37). Rambus never disclosed to other JEDEC participants the existence of its patent or pending patent applications that were required for use of the developing JEDEC standards. (Order, February 26, 2003 at 9; Order, February 27, 2003; *see also* CCFF 909, 927, 931, 944, 953, 961, 974, 976, 980, 986, 999, 1017, 1027, 1033, 1038, 1048, 1063, 1067, 1082, 1098-99, 1111).

Rambus's Response to Finding No. 858:

The proposed finding is misleading. The fact that a patent application traces its lineage back to another patent application does not in any way suggest that the subject matter of its

claims is related to the subject matter of the claims of the prior patent application, except that both must be supported by the same written description. (See RPF 78, 83-85). The proposed finding is also misleading to the extent that it suggests that the '646 and '961 applications are unique in this respect. In fact, every patent that Rambus has asserted in patent litigation can trace its lineage to various other combinations of two patents applications, such as, for example, applications 08/798,525 and 07/954,945. (*See* Stipulated Patent Tree).

Complaint Counsel cite as support for this proposed finding numerous other proposed findings; Rambus responds to each of those proposed findings below and will not repeat the responses here.

859. At no time while Rambus was a member of JEDEC did it inform JEDEC of the existence of its issued U.S. patent no. 5,513,327. At the time of its withdrawal from JEDEC, Rambus did not inform JEDEC of the existence of its issued U.S. patent no. 5,513,327. (Crisp, Tr. 3381, 3384; CX0887; CCFF 1092-95, 1109-14).

Rambus's Response to Finding No. 859:

Rambus has no specific response.

860. At no time while Rambus was a member of JEDEC did it inform JEDEC of the subject matter of any of its pending patent applications. At the time of its withdrawal from JEDEC, Rambus did not inform JEDEC of the subject matter of any of its pending patent applications. (Crisp, Tr. 3386-87; CX0887 (Rambus's withdrawal letter from JEDEC: "Rambus has also applied for a number of additional patents in order to protect Rambus technology."); *See also* CCFF 909, 927, 931, 944, 953, 961, 974, 976, 980, 986, 999, 1017, 1027, 1033, 1038, 1048, 1063, 1067, 1082, 1098-99, 1111).

Rambus's Response to Finding No. 860:

The proposed finding is misleading because it suggests that there existed a Rambus patent application for Mr. Crisp to disclose. Complaint Counsel have stipulated that, prior to the adoption of the JEDEC SDRAM standard in 1993, Rambus had no claims in any pending patent

application that, if issued, would have necessarily been infringed by the manufacture or use of any device manufactured in accordance with the 1993 JEDEC SDRAM standard. (Parties' First Set of Stipulations, No. 9.) The evidence also shows that Rambus had no undisclosed claims in any pending patent applications while it was a JEDEC member that, if issued, would have necessarily been infringed by the manufacture or use of any device manufactured in accordance with JEDEC SDRAM standard. *See* RPF 327-396. The proposed finding is also misleading because it suggests that Mr. Crisp should have disclosed some inventions in connection with SDRAM standardization that he believed were owned by Rambus. Even if, contrary to the weight of the evidence and the holding of the Federal Circuit, a JEDEC representative's beliefs could trigger a disclosure obligation, Complaint Counsel did not meet their burden of proving that Richard Crisp held such a belief at the time. (RPF 418-22).

861. At no time while Rambus was a member of JEDEC did it inform JEDEC that it had pending patent applications containing claims that related to the on-going work of JEDEC. (CX2092 at 148 (Crisp, Infineon Tr.) ("Q: Did you ever stand up in JEDEC in the four years that you attended meetings and watch the SDRAM standardization, did you ever stand up and say, Stop doing this; I own it? A: No, I never said that."); Crisp, Tr. 3176 ("Q: Between the time that you disclosed the '703 patent [in September 1993] and the time that you submitted the withdrawal letter to JEDEC, you did not disclose any Rambus patent applications at JEDEC, did you? A: That's correct."); CX0887 (Rambus's withdrawal letter from JEDEC); *See also* CCFF 909, 927, 931, 944, 953, 961, 974, 976, 980, 986, 999, 1017, 1027, 1033, 1038, 1048, 1063, 1067, 1082, 1098-99, 1111).

Rambus's Response to Finding No. 861:

The proposed finding is misleading because it suggests that there existed a Rambus patent application for Mr. Crisp to disclose. Complaint Counsel have stipulated that, prior to the adoption of the JEDEC SDRAM standard in 1993, Rambus had no claims in any pending patent application that, if issued, would have necessarily been infringed by the manufacture or use of

any device manufactured in accordance with the 1993 JEDEC SDRAM standard. (Parties' First Set of Stipulations, No. 9.) The evidence also shows that Rambus had no undisclosed claims in any pending patent applications while it was a JEDEC member that, if issued, would have necessarily been infringed by the manufacture or use of any device manufactured in accordance with JEDEC SDRAM standard. *See* RPF 327-396. The proposed finding is also misleading because it suggests that Mr. Crisp should have disclosed some inventions in connection with SDRAM standardization that he believed were owned by Rambus. Even if, contrary to the weight of the evidence and the holding of the Federal Circuit, a JEDEC representative's beliefs could trigger a disclosure obligation, Complaint Counsel did not meet their burden of proving that Richard Crisp held such a belief at this time. (RPF 418-22).

862. At no time while Rambus was a member of JEDEC did it inform JEDEC that it believed it had pending patent applications containing claims that related to the on-going work of JEDEC. (Crisp, Tr. 3084 ("Q. My question is you did not say anything with respect to Rambus – potential Rambus patents. Isn't that right? A. Yes, that's correct"); Crisp, Tr. 3064 ("Q. So you just sat there in silence and watched these presentations go forward. Isn't that right? A. Yes, that's correct"); *see also* Crisp, Tr. 3066, 3067-68 ("Q. And at this meeting, Mr. Sussman said that he didn't think that that foreign Rambus patent application would be a concern for the JEDEC SDRAM standardization effort. . . And you didn't say anything at that time to contradict Mr. Sussman, did you? A. I think that's correct, yes."); *See also* CCFF 909, 927, 931, 944, 953, 961, 974, 976, 980, 986, 999, 1017, 1027, 1033, 1038, 1048, 1063, 1067, 1082, 1098-99, 1111)

Rambus's Response to Finding No. 862:

The proposed finding is misleading because it suggests that there existed a Rambus patent application for Mr. Crisp to disclose. Complaint Counsel have stipulated that, prior to the adoption of the JEDEC SDRAM standard in 1993, Rambus had no claims in any pending patent application that, if issued, would have necessarily been infringed by the manufacture or use of any device manufactured in accordance with the 1993 JEDEC SDRAM standard. (Parties' First

Set of Stipulations, No. 9.) The evidence also shows that Rambus had no undisclosed claims in any pending patent applications while it was a JEDEC member that, if issued, would have necessarily been infringed by the manufacture or use of any device manufactured in accordance with JEDEC SDRAM standard. *See* RPF 327-396. It *cannot* be Complaint Counsel's theory that Your Honor should find that Rambus was required to provide *false* information to JEDEC, and to *falsely* state that its pending applications read on SDRAMs, in order to avoid antitrust liability.

The proposed finding is also misleading because it suggests that Mr. Crisp should have disclosed some "belief" regarding its patent applications. Even if, contrary to the weight of the evidence and the holding of the Federal Circuit, a JEDEC representative's beliefs could trigger a disclosure obligation, Complaint Counsel did not meet their burden of proving that Mr. Crisp held such a belief at the time. (RPF 418-22).

863. At no time while Rambus was a member of JEDEC did it inform JEDEC that it believed it could easily amend its pending patent applications to add claims that related to the on-going work of JEDEC. (CCFF 909, 927, 931, 944, 953, 961, 974, 976, 980, 986, 999, 1017, 1027, 1033, 1038, 1048, 1063, 1067, 1082, 1098-99, 1111).

Rambus's Response to Finding No. 863:

The proposed finding is misleading because it suggests that Mr. Crisp should have disclosed some belief regarding its prospects of success in amending its patent applications. Even if, contrary to the weight of the evidence and the holding of the Federal Circuit, a JEDEC representative's beliefs could trigger a disclosure obligation, Complaint Counsel did not meet their burden of proving that Richard Crisp held any such belief at the time. (RPF 418-22).

864. At no time while Rambus was a member of JEDEC did it inform JEDEC that it planned to amend its pending patent applications to add claims that related to the on-going work of JEDEC. (CCFF 909, 927, 931, 944, 953, 961, 974, 976, 980, 986, 999, 1017, 1027, 1033, 1038, 1048, 1063, 1067, 1082, 1098-99, 1111).

Rambus's Response to Finding No. 864:

The proposed finding is misleading because it suggests that Mr. Crisp should have disclosed some "plan" in connection with Rambus's patent applications. Even if, contrary to the weight of the evidence and the holding of the Federal Circuit, a JEDEC representative's knowledge about "plans" could trigger a disclosure obligation, Complaint Counsel did not meet their burden of proving that Richard Crisp had such knowledge at the time. (RPF 418-22).

865. At no time while Rambus was a member of JEDEC did it inform JEDEC that it was working with its patent counsel for the purpose of amending its pending patent applications to add claims that would relate to the on-going work of JEDEC.(CCFF 909, 927, 931, 944, 953, 961, 974, 976, 980, 986, 999, 1017, 1027, 1033, 1038, 1048, 1063, 1067, 1082, 1098-99, 1111).

Rambus's Response to Finding No. 865:

The proposed finding is misleading because it suggests that Mr. Crisp should have disclosed some "purpose" relating to Rambus's patent applications. Even if, contrary to the weight of the evidence and the holding of the Federal Circuit, a JEDEC representative's knowledge of such a "purpose" could trigger a disclosure obligation, Complaint Counsel did not meet their burden of proving that Richard Crisp had such knowledge at the time. (RPF 418-22).

866. Never once did Mr. Crisp inform JEDEC that Rambus believed it had invented, and could claim patent rights to, technologies being discussed at JEDEC. (CX2092 at 148, 150 ("Q. But you never once in four years of attending JEDEC meetings told JEDEC what they were doing was stealing Rambus' designs, did you? A. That's correct, I never once did say that."); *id.* at 187 ("Q. [N]ever once in four years did you stand up and say, I own that; you can't have it, right? A. That's correct").

Rambus's Response to Finding No. 866:

The proposed finding is misleading because it suggests that Mr. Crisp should have disclosed some inventions in connection with SDRAM standardization that he believed were owned by Rambus. Even if, contrary to the weight of the evidence and the holding of the Federal

Circuit, a JEDEC representative's beliefs could trigger a disclosure obligation, Complaint Counsel did not meet their burden of proving that Richard Crisp held such a belief at the time. (RPF 418-22).

B. As A JEDEC Member, Rambus Simultaneously Pursued Patent Applications Covering JEDEC Work While Withholding From JEDEC Any Meaningful Information Concerning Rambus Intellectual Property Rights.

867. The first Rambus employee to attend a JEDEC meeting on behalf of the company was William ("Billy") Garrett, who first attended a meeting in early December 1991. (CX0670 at 1). Mr. Garrett was later replaced as the Rambus primary representative at the JC 42.3 Committee by Richard Crisp, who served as primary representative from May 1992 until Rambus withdrew from JEDEC. (Crisp, Tr. 2929). Rambus submitted a letter withdrawing as a member of JEDEC in June 1996. (CX0602 at 8; CX0887; CX0888).

Rambus's Response to Finding No. 867:

The proposed finding is misleading and incomplete in its characterization of Rambus's submission of a letter in June 1996 as "withdrawing as a member of JEDEC." Rambus attended its last JEDEC meeting in December 1995. (CCFF 1088). Rambus did not pay the 1996 invoice for renewing its membership. (*Id.*). The June 1996 letter merely formalized Rambus's separation from JEDEC. (CX0887).

868. For a brief period of time, Rambus considered presenting its proprietary RDRAM design to JEDEC for evaluation as a standard. (CX0671 at 1 (Tate email in Dec. 1991 referring to "develop[ing] a plan . . . to take Rambus to JEDEC"); CX1705 at 30 (Roberts handwritten notes: "12/18 Board Meeting . . . JEDEC submission. talk to Richard about creating a plan for JEDEC")). Rambus co-founder Horowitz testified that one of the reasons Rambus initially joined JEDEC was its desire to have RDRAM adopted as an industry standard. (Horowitz, Tr. 8588-89; see also CX2101 at 279 (Horowitz, Micron Dep.)). Rambus was invited to attend its first JEDEC meeting as a guest of Toshiba, in part because Toshiba suggested Rambus consider taking the RDRAM to JEDEC. (CX2054 at 43-44 (Mooring, Infineon Dep.)).

Rambus's Response to Finding No. 868:

The proposed finding is not supported by the evidence. The December 1991 email from

Mr. Tate cited by Complaint Counsel does not reflect Rambus's consideration of presenting RDRAM to JEDEC but simply states that a Toshiba representative "[t]hinks we should develop a plan . . . to take Rambus to JEDEC." (CX0671 at 1.) Mr. Roberts' notes stating to a "12/18 Board Meeting . . . JEDEC submission" likely referred to Rambus's submission of a JEDEC application which had taken place earlier that month. (CX0602 at 2-3.) Dr. Horowitz did not testify that Rambus was considering presenting RDRAM to JEDEC for standardization. Rather, Dr. Horowitz testified that once RDRAM became a de facto standard through wide adoption, it might ultimately be standardized by JEDEC and Rambus believed it might be useful to understand JEDEC procedures prior to that time. (Horowitz, Tr. 8589-90).

869. However, while Rambus perceived its technology as revolutionary (Farmwald, Tr. 8304-8305), it came to recognize that customers would not move to Rambus unless their applications required the added performance (Farmwald, Tr. 8334). (See also CX2106 at 73 (Farmwald, Dep.) ("[T]he main feedback was that it was considered too big a leap. That it was too revolutionary. That they wanted evolutionary approaches, and that SDRAMs were perfectly fine for the next generation."); Horowitz, Tr. 8571, 8577, 8579-8582 (although Rambus' technology was revolutionary, customers chose the least-risk solution that met their needs and not necessarily the "best" solution); CX1322 at 15).

Rambus's Response to Finding No. 869:

The proposed finding is misleading and incomplete. During the 1990s, there was widespread recognition that Rambus technology would be necessary to achieve the performance demanded by customers. As Siemens' JEDEC representative, Willi Meyer, wrote in 1994, "[a]ll computers will (have to be) built like this some day, but hopefully without royalty to Rambus." (RX 488A at 1). JEDEC Council and 42.3B Committee chairman Gordon Kelley came to a similar conclusion in April 1992, when he warned his superiors at IBM about the potential for a "future Intel memory strategy to marry [a] 586/686 processor with Rambus protocol to corner

PC/notebook market with *state of the art performance*." (RX 279 at 4) (emphasis added).

870. Shortly after its representatives began attending JEDEC meetings, Rambus recognized that it might be able to assert patent rights over technologies under consideration at JEDEC in connection with a proposed synchronous DRAM standard and future generations of DRAM technology. (CCFF 884, 885-92, 911-20, 937-38). While it publicly promoted its proprietary RDRAM technology as the solution for computer memory technology, Rambus secretly sought to gain advantage over the competing technological standards under development at JEDEC. (See, e.g., CCFF 885-92, 900-01, 910, 917, 918, 932-36, 937, 939, 945, 948, 958, 962-67, 981, 987-93, 100-03, 1004-08, 1018-24, 1028-29, 1040, 1049, 1069, 1074-77, 1089, 1098-99). Over the course of its participation as a JEDEC member, Rambus secretly pursued steps to confirm and enhance its patent rights over JEDEC standard technologies, while withholding from JEDEC any meaningful information concerning its intellectual property rights. (See, e.g. CCFF 909, 927, 931, 944, 953, 961, 974, 976, 980, 986, 999, 1017, 1027, 1033, 1038, 1048, 1063, 1067, 1082, 1098-99, 1111).

Rambus's Response to Finding No. 870:

This conclusory finding is contradicted by the weight of the evidence. The finding cites no evidence itself and instead relies solely on individual findings. Rambus will not restate here all of its responses to those individual findings, which are instead incorporated by this reference.

December 1991 - JEDEC Committee Meeting

871. In December 1991 William Garrett was present for Rambus at the JEDEC JC-42.3 Committee meeting in Maui, Hawaii, participating as a non-member. (JX0010 at 2). Jim Townsend of Toshiba made a presentation concerning the JEDEC patent policy and showed the patent tracking list. (JX0010 at 11). Rambus was a guest at the invitation of Toshiba. (Rambus Answer at 20, ¶ 40).

Rambus's Response to Finding No. 871:

Rambus has no specific response.

872. Among the matters discussed at the December 1991 meeting were a variety of patent-related matters, including separate patent disclosures by IBM, DEC, Siemens, and TI; a response to patent-related questions by TI and Motorola; clarifications of patent licensing policies by Siemens and Hitachi; and expressions of patent-related concerns on proposals by Fujitsu and Samsung. (JX0010 at 3, 5, 8-11; G. Kelley, Tr. 2437-45). In particular, in response to an inquiry by Texas Instruments (TI), the purpose of the patent tracking list was explained as a means to track and identify patented items pertaining to Committee proposals. (*Id.*). Several

members provided clarifications, updates or corrections pertaining to identified patents. (*Id.;* G. Kelley, Tr. 2438-39). Hitachi provided a written statement of its general policy to license its patents on reasonable and non-discriminatory terms. (JX0010 at 11, 139).

Rambus's Response to Finding No. 872:

The proposed finding is inaccurate and incomplete. First, there is no evidence that DEC disclosed a patent (as opposed to another party raising a DEC patent). (JX0010 at 3). Second, the cited pages contain no evidence of a patent-related question raised by Motorola or of Siemens clarifying its patent licensing policy. Third, the purpose of the patent tracking list was identified in the minutes as "only to track and identify *patented* items of Committee proposals" (JX0010 at 11) (emphasis added). This shows that only issued patents that read on proposed items were under discussion, not all patents "pertaining to" such proposals, as stated in the proposed finding. Fourth, the minutes state that "companies who hold patents identified can respond to Committee, *if they wish.* (JX 10 at 11) (emphasis added). This shows the voluntary nature of patent-related disclosure. Fifth, while Hitachi's statement does begin by stating that its "general policy" is to license patents on RAND terms, the remainder of the statement indicates that Hitachi evaluates requests for licenses on "a case-by-case basis." (JX 10 at 139). Hitachi's statement goes on to say that it may only license its patents in the event that its negotiating partner is prepared to enter into a cross-license. (JX0010 at 139). The complete statement reads:

> "It is Hitachi's general policy to license its patents on reasonable and non-discriminatory terms. Requests for licenses generally are evaluated on a case-by-case basis, taking into consideration other Hitachi patents that may be applicable as well as patents of the party requesting a license. Typically, the resulting license encompasses the applicable patents of both

parties."

(*Id.*) The minutes reflect no objection to Hitachi's policy. (*Id.*)

873. One specific area where patent issues arose at the December 1991 Committee meeting concerned a proposed standard for a packaging technology known as V-PACK. (JX10 at 8-9 (Items 329.1 and 329.2, JEDEC Ballot JC-42.3-91-66A); Williams, Tr. 779-782; CX2114 at 31 (Karp, Dep.)). The balloted proposal for incorporating VPACK as a JEDEC standard failed due to patent issues. (JX10 at 8-9; Williams, Tr. 781-782; CX2114 at 31).

Rambus's Response to Finding No. 873:

The proposed finding is incomplete. The "patent issues" involving the V-PACK ballot related to three separate companies, Texas Instruments, Micron and Fujitsu, asserting that they had patent rights over the technology. (CX2114, Karp FTC Depo. at 31-32). There was also a concern whether companies already paying royalties to Texas Instruments on DRAM-related patents would have to pay an additional royalty for the V-PACK technology. (*Id.*)

874. Joel Karp, who at the time represented Samsung on the Committee, recalled that the patent holder, Texas Instruments ("TI"), offered to license at a 1% royalty. (CX2114 at 32; *see also* CX2078 at 139-140 (Karp, Dep.)). The 1% royalty rate is not referenced in the JEDEC minutes, but is based on Mr. Karp's own recollection of the event. (CX2114 at 41). Mr. Mooring of Rambus recalls seeing a letter indicating TI was willing to license its patents on VPACK at a "reasonable royalty rate," in the one percent range. (CX2112 at 88 (Mooring, FTC Dep.)). Mr. Karp's experience, based on the V-PACK events, was that members of JEDEC balked at paying even a 1% royalty. (CX2078 at 139, 141-42).

Rambus's Response to Finding No. 874:

The proposed finding is misleading and incomplete. Mr. Karp testified that, at the time of the V-PACK ballot, Samsung was already paying Texas Instruments "significantly more than 1%" on their patents and felt that it would be unreasonable to pay an additional 1% for Texas Instruments' V-PACK patent. (CX2078, Karp Micron Depo. at 140-42). In fact, in that time frame, Texas Instruments was charging royalties in the range of 5-10% for their DRAM patent

portfolio, varying from company to company depending on cross-licensing arrangements. (CX 2106, Farmwald, FTC depo. at 124-25.) Moreover, there was a concern that additional royalties would have to be paid to other companies claiming to have patent rights over the technology. (CX2114, Karp FTC Depo. at 31-32). Despite these concerns, only five JEDEC members voted no on the V-PACK ballot, as opposed to ten who voted yes. (CX2080, Karp Micron Depo. at 228). Thus, the proposed finding that "members of JEDEC balked at paying even a 1% royalty" is grossly misleading; in fact, a *minority* of JEDEC members balked at paying an *additional* 1% royalty to Texas Instruments over the 5-10% royalty they were already paying, as well as potential royalties to other companies.

875. Mr. Karp's handwritten notes from the Decembeer 1991 JEDEC meeting confirm that other manufacturers opposed the standardization of V-PACK because they did not want to pay royalties. (CX2080 at 228-229 (Karp, Dep.)). As Mr. Karp testified, "I think they [the DRAM producers] are saying they won't pay anything." (*Id.* at 229).

Rambus's Response to Finding No. 875:

The proposed finding is misleading, incomplete, and misrepresents the evidence. As discussed above, the evidence indicates that a minority of DRAM manufacturers opposed the standardization of V-PACK because they did not want to pay an additional 1% royalty to Texas Instruments over the 5-10% royalty they were already paying, as well as potential royalties to other companies. (*See* RRFF 874).

876. Mr. Garrett prepared a report of the December 1991 Committee meeting that he circulated to Rambus colleagues. (CX0670 at 1). The report stated that there were "several synchronous presentations" and outlined the important points of each. (*Id.*). Mr. Garrett specifically noted that both Howard Sussman and Texas Instruments proposed to use programmable CAS latency and programmable burst length. (CX0670 at 1 ("NEC .....2) Latency should be Programmable. (This would be accomplished with a WCBR cycle . ... 1 ..... 51 Burst sequence and wrap length should be programmable .... TI - most important points ... Programmable WCBR cycle for Wrap or Burst note, length, sequence and clock Latency ...

Their proposal seems to be well though[t] out."); see also Crisp, Tr. 3037-38 (Mr. Garrett's e-mail described CAS latency and programmable wrap length, which sometimes is used interchangeably with burst length)). Mr. Garrett's e-mail also noted that Mitsubishi proposed to use pins for wrap note and wrap type which would allow changes on the fly. (CX0670 at 1).

Rambus's Response to Finding No. 876:

The proposed finding is incomplete and misleading in suggesting that Mitsubishi's proposal, which would have used pins to set burst length and burst type, would have allowed changes on the fly as opposed to the other proposals. In fact, Mr. Garrett wrote that the Mitsubishi proposal would use pins to "allow changes on the fly while all other proposals are being set once (*or on the fly*) through the use of a WCBR cycles [sic]." (CX0670 at 1 (emphasis added)). Mr. Garrett also noted that Mitsubishi was "considering eliminating" the additional pins for setting burst length and burst type. (*Id.*)

877. According to Mr. Garrett, all of the companies making proposals were currently working on their own solutions and were committed to meeting their customers' needs; the Committee was trying to get some agreement to reduce the proliferation of different parts. (*Id.*). Most proposals, he said, were incremental additions to existing DRAMs. (*Id.* at 2).

Rambus's Response to Finding No. 877:

The proposed finding is incomplete. Mr. Garrett stated that the companies were "committed to meeting their customers needs, even if it does not become a JEDEC standard." (CX0670 at 1).

December 1991 - Rambus Applies for JEDEC Membership

878. Within days after returning from the December 1991 Committee meeting, Mr. Garrett submitted for Rambus an official membership application to JEDEC and paid the company's membership dues. (CX0602 at 2-3). On its membership application Mr. Garrett noted that Rambus "agree[d] to participate in the activities of" the JC-42.3 Committee, which was charged with overseeing the development of JEDEC Synchronous DRAM standards. (*Id*. at 3).

Rambus's Response to Finding No. 878:

Rambus has no specific response, other than to note that the application form says nothing about the disclosure of intellectual property interests.

879. On January 12, 1992, Rambus CEO and President Tate circulated a draft business plan. The draft business plan made no mention of patent rights applicable to competing DRAM technologies. (CX0542). Several day later, handwritten notes from Rambus Vice President Allen Roberts' personal notebook suggest - discussion with "Richard" about creating a plan for JEDEC. (CX1705 at 30 ("Board meeting ... JEDEC submission. Talk to Richard about creating a plan for JEDEC.")).

Rambus's Response to Finding No. 879:

The proposed finding is misleading to the extent that it suggests a connection between circulation of the draft business plan and Mr. Roberts' notes. There is no evidence to suggest such a connection.

February 1992 - JEDEC Committee Meeting

880. In February 1992 the JEDEC JC-42.3 Committee met in Seattle, Washington. (JX0012 at 1). The Chairman Mr. Townsend made a presentation concerning the patent policy and showed the patent tracking list. (JX0012 at 5, 28-29).

Rambus's Response to Finding No. 880:

Rambus has no specific response.

881. Among the matters discussed at the February 1992 meeting were several patent-related matters. (JX0012 at 5). These included clarifications by Texas Instruments (TI) concerning patents that it had previously disclosed to the Committee. (*Id.*). Siemens provided clarifications on several previously identified patents, and provided a written statement of its intent to license two specified patents on reasonable and non-discriminatory terms. (*Id.* at 5, 30).

Rambus's Response to Finding No. 881:

The proposed finding is inaccurate. Texas Instruments clarified that it made "no LOC patent claims" and "sync DRAM patent claims" (JX0012 at 5), but the patent tracking list

indicates that this did not relate to patents that Texas Instruments had previously disclosed to the Committee, but rather to patent issues raised by others. (JX0012 at 29).

882. Mr. Garrett prepared a detailed report of the discussions at the meeting for his Rambus colleagues that stated he was in attendance. (CX0672 at 1).

Rambus's Response to Finding No. 882:

The proposed finding is misleading in stating that Mr. Garrett's report was "detailed." In fact, the cited report summarizing the two-day meeting was slightly over one page long. (CX0672).

883. The first item that Mr. Garrett reported to his Rambus colleagues was a presentation by Fujitsu concerning a new generation of DRAMs; the presentation was reported by Mr. Garrett to be "particularly good and well thought of." (CX0672 at 1). In connection with the presentation, Fujitsu discussed its intellectual property claims – specifically, its rights under pending patent applications: Mr. Garrett reported "Fujitsu indicated that they do have patents applied for, but that they will comply with the JEDEC requirements to make it a standard!!!" (*Id.*, emphasis in original).

Rambus's Response to Finding No. 883:

The proposed finding is inaccurate. The Fujitsu presentation referred to in the proposed finding did not concern a "new generation of DRAMs," but rather a new type of DRAM packaging known as a "VSMP" or "Vertical Surface Mount Package." (CX0672 at 1; JX0012 at 11, 137-39). Mr. Garrett's comment regarding a Fujitsu presentation that was "particularly good and well thought of," did not relate to this packaging presentation but, rather, to a different Fujitsu presentation on synchronous DRAM. (CX0672 at 1; JX0012 at 9, 75-92).

884. In contrast to the statement made to JEDEC by Fujitsu, Mr. Garrett's report noted to his colleagues the possibility that Rambus might be in a position to assert patent claims over aspects of JEDEC work on SDRAM standards. (CX0672 at 1 (Rambus "could influence the voltage standard if we want, or we could use our patents to keep current-mode interfaces off of DRAMs")).

Rambus's Response to Finding No. 884:

The proposed finding is incomplete, misleading and not supported by the evidence. First, the quoted language from Mr. Garrett's report does not refer to asserting patent claims. Second, the quote from Mr. Garrett's report *omits* Mr. Garrett's comment that Rambus might influence these features "assuming that it is what we patented." (CX 672 at 1). In fact, Rambus had no patents in February 1992, and there is no evidence that Rambus had any patent claims involving low voltage interfaces or current-mode interfaces that were pending at that time. Third, Complaint Counsel has introduced no evidence that current mode interfaces were being discussed at JEDEC at that time. Fourth, the proposed finding purports to contrast Fujitsu's behavior with Rambus's, while ignoring the differences between their two positions. Fujitsu was *proposing* standardization of certain technology at JEDEC that it was currently patenting, while Rambus was not proposing that JEDEC adopt any technology and did not have filed patent claims covering the technology being discussed at JEDEC.

Spring 1992 - Rambus Consultations With Patent Counsel

885. By late 1991 Rambus was represented by an outside patent attorney, Lester Vincent, of the firm Blakely, Sokoloff, Taylor & Zafman, in connection with patent matters, including the preparation and revision of its patent applications. (*See, e.g.,* CX3125 at 279-80 (Vincent, Dep.); CX1932). Mr. Vincent's work for Rambus over the years included patent prosecution and offensive and defensive work regarding patents. (CX3123 at 9 (Vincent, Dep.)).

Rambus's Response to Finding No. 885:

Rambus has no specific response.

886. In late 1991, prior to the March 1992 meeting between Mr. Vincent and Messrs. Roberts and Crisp, Mr. Crisp had consulted with Rambus concerning Rambus patent applications and the use of "low swing signals on DRAM." (CX1932; CX3125 at 279-80 (Vincent, Dep.)).

Rambus's Response to Finding No. 886:

The proposed finding is not supported by the evidence. The cited document, Mr. Vincent's notes of a conversation with Jim Gasbarro of Rambus, states "Allen Roberts – Low swing signals on DRAM." (CX1932). There is no mention of Mr. Crisp in the document or in the cited Vincent deposition testimony.

887. By March 1992, Rambus began to consult with Lester Vincent concerning JEDEC (CX3123 at 62 (Vincent, Dep.)). In a March 25, 1992, teleconference, Lester Vincent and Rambus Vice President of Engineering, Allen Roberts, discussed the possibility of Rambus asserting patents over SDRAMs, as well as the potential legal implications of such a strategy. (CX3125 at 296-98, 299-302 (Vincent, Dep.); CX1941 at 1). Among other things, Mr. Vincent's handwritten notes record that the conversation concerned "Jedec" and the "need [for] pre planning before accuse others of infringement." (CX1941 at 1). The notes contain the reference "Jedec Committee => Standards for DRAMs" and reflect discussion of "Advising JEDEC of patent applications." (*Id.*). The notes state "Allen will get JEDEC bylaws re patents." (*Id.*).

Rambus's Response to Finding No. 887:

The proposed finding is inaccurate, misleading, and not supported by the evidence. The proposed finding that "[b]y March 1992, Rambus began to consult with Lester Vincent concerning JEDEC issues" is misleading, because it suggests on-going consultation when, in fact, the record shows only a few discussions concerning JEDEC over several years. The evidence also does not support a finding that in the March 25, 1992 teleconference, there was a discussion of "the possibility of Rambus asserting patents over SDRAMs, as well as the potential legal implications of such a strategy." The sum total of Complaint Counsel's support for this proposition is the line in Mr. Vincent's notes which states: "Said need preplanning before accuse others of infringement." (CX 1941 at 1.) As Mr. Vincent explained, this means that you cannot just "run into Federal Court or write letters threatening people with infringement; it requires some preparation work." (CX 3125, Vincent Infineon Depo. at 299.) There is no indication in

the notes or the related Vincent deposition testimony of what specific technology, if any, was under discussion; nor is there any indication of the discussion of "potential legal implications." (CX 1941 at 1; CX 3125, Vincent Depo. at 301).

888. Two days later, on March 27, 1992, Mr. Vincent met with Rambus employees Allen Roberts and Richard Crisp and continued this discussion. (CX3125 at 310, 311-313 (Vincent, Dep.); CX1942). At this meeting Mr. Vincent was informed that Rambus was a member of JEDEC (CX3125 at 311-312 (Vincent, Dep.); CX1942 at 1) and that "Rambus attended [a] meeting with a hundred others where JEDEC's proposal to establish [a] standard for small swing signals for sync DRAM was discussed."(CX1942 at 1; CX3125 at 312-313 (Vincent, Dep.)).

Rambus's Response to Finding No. 888:

Rambus has no specific response.

889. The issue that Rambus wanted to talk about with Mr. Vincent in late March 1992 was whether attending JEDEC was a problem. Mr. Vincent warned that there could be an "equitable estoppel problem" in connection with the enforcement of Rambus patents if Rambus created an impression on JEDEC that it would not enforce its patents or patent applications. (CX3125 at 317-18 (Vincent, Dep.); CX1942 at 1). Mr. Crisp advised that the "strongest case of equitable estoppel is when you say you will not enforce your patent" and that the issue was "less clear-cut if Rambus is merely silent." (*Id.*). He cautioned that Rambus "cannot mislead JEDEC into thinking that Rambus will not enforce its patent." (*Id.*).

Rambus's Response to Finding No. 889:

The proposed finding is inaccurate and not supported by the evidence. First, the evidence does not indicate whether the discussion relating to equitable estoppel was initiated by Rambus or by Mr.Vincent. Second, the statement regarding equitable estoppel were made by Mr. Vincent, not Mr. Crisp. Third, the finding omits the last line of the notes, which states: "possibly abstain from voting." (CX 1942 at 1).

890. Mr. Crisp recalled that in this meeting Mr. Vincent advised Messrs. Roberts and Crisp that even if Rambus did go to JEDEC meetings, stayed silent and didn't do anything else, there was still a risk that Rambus patents might be unenforceable. (CX2092 at 98 (Crisp, Infineon Trial Tr.)). Mr. Vincent was trying to tell Messrs. Roberts and Crisp that if Rambus insisted on going, the least it should do is don't do anything to mislead anybody. (*Id.*).

Rambus's Response to Finding No. 890:

The proposed finding is misleading. Mr. Vincent's notes and Mr. Crisp's testimony make clear that any risk that Mr. Crisp recalls of staying silent at JEDEC meetings was only in the event that that silence misled others into thinking that Rambus would not enforce its patents. (CX 1942; CX 2092, Crisp Infineon Trial Tr. at 98; Crisp, Tr. at 3469-70). It is undisputed that Mr. Crisp informed JEDEC openly in both May of 1992 and in September of 1995 that he would not disclose information about Rambus's pending patent applications at JEDEC meetings and that Rambus's "presence or silence at committee meetings does not constitute an endorsement of any proposal under the committee's consideration nor does it make any statement regarding potential infringement of Rambus intellectual property." (JX 27 at 26). *See* RPF 466-561. It is also undisputed that no one who testified at trial and who had been at either meeting testified that he had been led by these statements to believe that Rambus would not seek or enforce intellectual property relating to JEDEC standards. Instead, every witness understood Rambus's messages as a warning. (RX 290 at 3; Kelley, Tr. 2579; Kellogg, Tr. 5055-56, 5322; Calvin, Tr. 1066-1070). *See* RPF 493-548.

891. In the same time period, Mr. Vincent advised Mr. Crisp and Mr. Roberts that he "didn't think it was a good idea" for Rambus to continue participating in JEDEC, given the downside risk associated with potential equitable estoppel claims that might prevent enforcement of Rambus patents. (CX3125 at 320-21 (Vincent, Dep.) ("Q. Did you tell Richard Crisp and Allen Roberts that at this March 27th, 1992, meeting, that they should not participate in JEDEC? . . . A. . . . I believe at some point early on . . . I believe I said I didn't think it was a good idea"; "Q. The downside risk was that someone was going to raise the issue of equitable estoppel if Rambus attended JEDEC? A. Right. . . .")).

Rambus's Response to Finding No. 891:

The proposed finding is not supported by the evidence. Complaint Counsel cites

deposition testimony from Mr. Vincent that was corrected by Mr. Vincent a few minutes later when he realized that he was confused about the time frame, and that his statement that it was not a "good idea" that Rambus participate in JEDEC meetings may have been made as late as 1996. (CX3125, Vincent Depo. at 326.) Mr. Vincent has since testified that he does not recall making any such statement in the 1992 time frame. (Vincent, Tr. 7906). Indeed, the available evidence indicates that Mr. Vincent did not advise Rambus that it was not a "good idea" to participate in JEDEC until after the Dell proposed consent order was released in late 1995 or early 1996. (Crisp, Tr. 3470 (Mr. Vincent did not advise Rambus in March 1992 not to go to JEDEC meetings); RRFF 1084-85.).

892. In late March and early April 1992, Mr. Vincent conferred further with Rambus. A handwritten note of Mr. Vincent of a teleconference with Rambus CEO Geoffrey Tate on March 30, 1992, makes reference to "possible infringer" and obtaining copies of Rambus patent applications; the note states "we [sic] call me if he wants to go over the claim coverage." (CX1943; CX1325 at 321-22 (Vincent, Dep.)). On April 1, 1992, Mr. Crisp asked Mr. Vincent to fax him abstracts of Rambus patent applications (CX1944; CX3125 at 322 (Vincent, Dep.)), which Mr. Vincent did several days later. (CX1945 at 1). Later in April, Mr. Vincent's time records indicate he reviewed JEDEC publications. (CX3128 at 185-86 (Vincent, Dep.); CX1933 at 20).

Rambus's Response to Finding No. 892:

The proposed finding is incomplete. Lester Vincent's time entries indicate that he reviewed JEDEC publications in April 1992 for only .25 hours (fifteen minutes). (CX 1933 at 20). Moreover, the only JEDEC publications that contained in Blakely, Sokoloff's files were the Style Manual for Standards and Publications of EIA, TIA, and JEDEC, EP-7-A, (July 1990), the Manual for Committee, Subcommittee, and Working Group Chairmen and Secretaries, Engineering Publication EP-3-F (October 1981), the Manual of Organization and Procedure EP-1-J (June 1989), JEDEC Manual of Organization and Procedure JEP21-H (July 1988), and the

EIA Legal Guides (March, 1983). (CX 3128, Vincent Micron Depo. at 186-89; Vincent deposition reading, Tr. 2215-16; CX 207A; RX 9; CX 206; CX 205A; CX 202).

There is thus no evidence that Mr. Vincent reviewed JEDEC Manual of Organization and Procedure JEP21-I, which was not even published as of April 1992. The 21-H manual, which *was* located in Blakeley, Sokoloff's files, and which *was* in force in April 1992 when Mr. Vincent reviewed JEDEC publications, contains only one statement about intellectual property:

> "JEDEC standards are adopted without regard to whether or not their adoption may involve patents [on] articles, materials or processes."

(CX 205A at 11).

April 1992 - JEDEC Task Group Meeting

893. In April 1992, Richard Crisp attended a JEDEC Synchronous DRAM Task Group meeting in Dallas, Texas. (Crisp, Tr. 2933-34; CX1708).

Rambus's Response to Finding No. 893:

Rambus has no specific response.

894. At the April 1992 task group meeting, Mr. Crisp learned that there was "a lot of momentum against" the RDRAM technology and that the group was "pretty set on using the SDRAMs for memory" in the new standard under consideration. (CX1708 at 3). He observed presentations involving a programmable mode register, including programmable burst length. (Crisp, Tr. 3054-55).

Rambus's Response to Finding No. 894:

The proposed finding is incomplete and not supported by the evidence. Mr. Crisp's notes state that there was "a lot of momentum against us in the main memory arena," but not for other purposes, such as graphics, as the proposing finding suggests. (CX1708 at 3) Moreover, Mr.

Crisp's statement that "the group is pretty set on using the SDRAMs for memory" was not referring to what was to be standardized, as the proposing finding suggests, but rather what was to be used in the marketplace. (CX1708 at 3).

895. Mr. Crisp reported to Rambus colleagues that there was intense focus by JEDEC members on minimizing the costs associated with SDRAMs. (CX1708 at 1 (IBM "cited pricing as being the driving force."; *id*. at 2 ("Compaq (Dave Wooton), like the others stressed that price was the major concern for all their systems."); id. ("Sun echoed the concerns about low cost. They really hammered on that point.")).

Rambus's Response to Finding No. 895:

The proposed finding is not supported by the evidence. Mr. Crisp's report does not indicate an "intense focus" on minimizing costs, but rather that JEDEC members discussed a number of topics, including SDRAM pricing, at the task group meeting. (CX1708 at 1-7). The evidence cited indicates that three particular DRAM customers were concerned about the price they would have to pay for SDRAMs, not about the costs associated with SDRAMs. (CX1708 at 1-2).

896. Mr. Crisp concluded that SDRAMs were likely to be significantly lower-priced items as compared to RDRAM devices. (CX1708 at 3). Mr. Crisp attributed this price difference, in large degree, to the fact that makers of RDRAMs would be forced to pay license fees and royalties to Rambus. (*Id.* ("it seems unlikely that we are going to be able to do better on price than the SDRAMs (license fees in need of recapture, royalties to be paid, bigger die size).").

Rambus's Response to Finding No. 896:

The proposed finding is not supported by the evidence. Mr. Crisp's report states only that "[i]t seems unlikely that we are going to be able to do better on price than the SDRAMs." (CX1708 at 3). This hardly supports a finding that Mr. Crisp concluded that SDRAMs were likely to be *significantly* lower-priced than RDRAMs. Nor does the evidence support the

proposed finding that Mr. Crisp attributed any price difference *in large degree* to license fees and royalties; Mr. Crisp also mentioned die size and did not attempt to apportion any price differential among these factors. (CX1708 at 3).

897. Mr. Crisp believed there was dissension among some JEDEC members at the meetings, and in the aftermath of the meeting suggested to Rambus colleagues that this be leaked to the press to the competitive advantage of Rambus. (Crisp, Tr. 2934-35; CX1708 at 5). In an email to colleagues, Mr. Crisp suggested a headline to be carried on trade publications EETimes and Nikkei Electronics. (CX1708 at 5 ("RIFT forms in JEDEC SDRAM working group: major system houses now leaning away from JC42 committee recommendation.")). Mr. Crisp suggested specific trade press journalists who might be willing to help with the story. (*Id.*).

Rambus's Response to Finding No. 897:

The proposed finding is incomplete and irrelevant. There is no evidence that any such information was ever leaked to the press.

898. Mr. Crisp recognized that one downside of the idea was that the JEDEC discussions were confidential and a leak could lead to censure by JEDEC "if we weren't tossed out." (CX1708 at 5; see also CCFF 830-31). But getting the story in industry publications "should help our air war." (*Id.*). This referred to the desire of Rambus to have people use the proprietary RDRAM architecture. (Crisp, Tr. 2935).

Rambus's Response to Finding No. 898:

The proposed finding is incomplete and irrelevant. There is no evidence that any such information was ever leaked to the press.

899. Gordon Kelley of IBM wrote a letter to Ken McGhee of JEDEC following the April 1992 Committee meeting expressing concern with possible leaks to the press. (CX0035 at 16; G. Kelley, Tr. 2516-19). Mr. Kelley testified that Mr. Crisp's suggestion that Rambus leak information from the April 1992 meeting was "an example of not having good faith or not showing good faith." (G. Kelley, Tr. 2523-24).

Rambus's Response to Finding No. 899:

The proposed finding is incomplete and irrelevant. First, there is no evidence that Rambus ever leaked any information to the press. Second, as Mr. Kelley's letter following the

April 1992 Task Group meeting indicates, leaks to the press from JEDEC members were not an uncommon occurrence. (CX0035 at 16).

Early May 1992 - Discussion With Patent Counsel

900. In early May 1992, within weeks after the April 1992 SDRAM Task Group meeting, Rambus was once again consulting with its outside patent counsel, Lester Vincent, concerning the possibility of asserting patent claims against the SDRAM standard under consideration. In his notes from a May 2, 1992, teleconference, Mr. Vincent wrote that "Richard Crisp wants to add claims to the original application" and referred specifically to "claims to mode register to control latency output timing depending upon clock cycle." (CX1946 at 1).

Rambus's Response to Finding No. 900:

The proposed finding is inaccurate and not supported by the evidence. First, Mr. Vincent's notes say nothing about asserting patent claims against SDRAMs (one cannot assert a patent against a standard), but simply discuss a desire on Mr. Crisp's part to obtain claims covering certain technology. (CX 1946 at 1). Second, the reference to Rambus "once again" consulting with Mr. Vincent suggests, contrary to the evidence, that Rambus had previously consulted with Mr. Vincent about asserting patent claims against SDRAMs. There is no such evidence. (See RRFF 887). Finally, the proposed finding misquotes Mr. Vincent's notes, which actually state: "Add claims to mode register to control latency output timing depending upon clock – specify clock cycle." (CX1946 at 1).

901. Each of the items mentioned as those for which Mr. Crisp desired to add new patent claims had, by this point in time, been proposed for inclusion in the SDRAM specifications during JEDEC meetings attended by Mr. Garrett or Mr. Crisp. (CX0670 at 1 (Garrett email describing "the definition of synchronous DRAMs" as including the following, among other features: "Fully Synchronous DRAM with all signals referenced to a single (positive) clock edge. . . . Latency should be Programmable. . . . Burst sequence and wrap length should be programmable")).

Rambus's Response to Finding No. 901:

The proposed finding is misleading in its reference to "[e]ach of the items," since Mr. Crisp was only proposing adding new patent claims with respect to a single item – a "mode register to control latency output timing depending upon clock." (CX 1946 at 1).

May 1992 - JEDEC meeting - Crisp declines to comment

902. In May 1992 Richard Crisp was present for Rambus at the JEDEC JC-42.3 Committee meeting in New Orleans, Louisiana. (CX0034A at 1). The Chairman Mr. Townsend made a presentation concerning the patent policy and tracking list, and secretary Ken McGhee spoke concerning the EIA patent policies. (CX0034A at 4, 7).

Rambus's Response to Finding No. 902:

The proposed finding is incomplete. According to the meeting minutes, Mr. McGhee "showed a copy of the new ANSI patent policy implementation guide." (CX 34 at 3, 10-11). As EIA General Counsel John Kelly has testified, the ANSI patent policy does not require the disclosure of patent applications. (Kelly, Tr. 1958, 2074).

903. By May of 1992 there were concerns by some members of the JC-42.3 Committee that a particular aspect of JEDEC's work on SDRAM standards might implicate Rambus patents. Siemens and IBM, which had been working on a joint project relating to the development of next-generation memories, had noted similarities between SDRAM and the two-bank design used in proprietary RDRAM, and had learned of rumors that Rambus had demanded royalties from Samsung. (CX2088 at 317-319, CX2089 at 41-43 (Meyer, Infineon Trial Tr.); RX0286A at 2; RX0289 at 1).

Rambus's Response to Finding No. 903:

The proposed finding is misleading and not supported by the evidence. While the evidence does show that Siemens and IBM were concerned that "2-bank sync may fall under Rambus patents" (RX0289 at 1), the evidence does not support a finding that JEDEC members' concerns were limited to this "particular aspect" of JEDEC's work on SDRAM standards. Willi

Meyer of Siemens wrote a memorandum dated April 30, 1992 that stated in part that "[t]he original idea behind the SDRAM is based on the basic principle of a simple pulse input (IBM toggle pin) and the complex RAMBUS structure." (RX 285A at 5). The memorandum does not indicate that the only similarity between SDRAM and "the complex Rambus structure" was 2-bank design. (RX 285A at 5). Also on April 30, 1992, Mr. Meyer wrote in another memorandum that "Rambus has announced a claim against Samsung for USD 10 million due to the similarity of the SDRAM with the Rambus storage device architecture." (RX0286A at 2). Mr. Meyer testified that he had received this information from Gordon Kelley of IBM. (CX2088, Meyer Infineon Trial Tr. at 317-18.) There is no indication in the document that the "similarity" was limited to 2-bank design. There is also no evidence to support the characterization in the proposed finding of the information relating to a Rambus claim against Samsung as "rumors."

Moreover, a week later, at the May 1992 JC 42.3 meeting, IBM JEDEC representative Mark Kellogg prepared handwritten notes reflecting a concern that Mr. Meyer had raised during the meeting:

> "Siemens: kernal of chip similar to Rambus. Patent concerns? (No Rambus coments)."

(RX 290 at 3). Mr. Kellogg testified that when he used the phrase "kernel of the chip" in his notes, he was referring to Mr. Meyer's concern that "the fundamental architecture of the SDRAM device" was "similar to Rambus." (Kellogg, Tr. 5324).

Mr. Kellogg testified that he considered the discussion a "flag" because JEDEC members were "describing possible intellectual property concerns which may affect our decision process for synchronous DRAM." He testified that "[t]hat is a concern" and that "[t]he lack of response

by Rambus is also a concern." (Kellogg, Tr. 5323 (quoting deposition testimony, which Mr. Kellogg agreed was truthful)).

904. During the May 1992 Committee meeting there was discussion that made reference to Motorola and Rambus as firms about which there were possible patent issues pertaining to the dual bank design. The Chairman Mr. Kelley of IBM, prompted by Willi Meyer of Siemens, asked Mr. Crisp whether he would like to comment on the issue. Mr. Crisp gave no verbal response, but rather shook his head. Mr. Kelley then commented to the group that "they don't have anything to say about that." (CX2089 at 130-131, 136-137 (Meyer, Infineon Trial Tr.)).

Rambus's Response to Finding No. 904:

The proposed finding is incorrect, misleading and not supported by the evidence. The proposing finding alters the question that Mr. Kelley asked Mr. Crisp to make it appear that, by shaking his head, Mr. Crisp was denying that Rambus might have relevant patent claims. To the contrary, as Mr. Meyer makes clear in the very testimony cited by Complaint Counsel: "The way how Mr. Kelley formulated the question was: Do you want to give a comment on this?" (CX2089, Meyer Infineon Trial Tr., at 136). Thus, Mr. Meyer's testimony that Mr. Crisp shook his head in response shows that Mr. Crisp was declining to comment on Rambus's patent position.

Complaint Counsel's description of the question supposedly asked to Mr. Crisp is especially misleading given that every witness who testified about the May 1992 exchange between Crisp and Kelley, and every contemporaneous document that describes it, states that Crisp had declined to comment about Rambus's intellectual property. (*See, e.g.*, RX 290 at 3 – notes of 5/92 meeting taken by IBM's Mark Kellogg say "Siemens: kernel of chip similar to Rambus. Patent concerns? (No Rambus comments)". This evidence is set out in more detail at RPF 493-511.

905. Mr. Crisp reported to his Rambus colleagues that at the May 1992 Committee meeting Siemens and Philips had expressed concern over potential Rambus patents covering two-bank designs. (CX0673 at 1). According to Mr. Crisp, "Gordon Kelley of IBM asked me if we would comment which I declined." (*Id.*).

Rambus's Response to Finding No. 905:

Rambus has no specific response.

906. At the May 1992 Committee meeting, Howard Sussman of NEC commented to the group that he had seen a copy of a Rambus foreign patent application. (CX2092 at 128 (Crisp, Infineon Trial Tr.). According to Mr. Crisp, the essence of the comment was that Mr. Sussman had obtained a copy of the application from the foreign patent office, had read it and it should not be a concern for the JEDEC standardization effort. (CX2092 at 129 (Crisp, Infineon Trial Tr.). Mr. Crisp was there, heard the comment, and didn't say anything different. (CX2092 at 130 (Crisp, Infineon Trial Tr.)).

Rambus's Response to Finding No. 906:

The proposed finding is misleading and incomplete. Mr. Sussman indicated that Rambus's foreign patent application, the PCT application, should not be a concern because, according to Sussman, "many, many claims . . . are anticipated by prior art." (CX0673 at 1; *see* RPF 516-22.) The contemporaneous notes of Mark Kellogg, IBM's JEDEC representative, confirm that Sussman stated that, in Sussman's view, the Rambus claims were not valid. (RX0290 at 3 ("NEC: Rambus International Patent 150 pages, Motorola patents/Rambus patents – suspect claims won't hold.").

907. The chairman of the meeting, Gordon Kelley, testified that prior to the May 1992 meeting Mr. Crisp had spoken to him about the possibility of Rambus scheduling a presentation concerning DRAM design. Concerned about the rumors of possible patent issues with Rambus, Mr. Kelley asked Mr. Crisp if he was aware if there were patents or patent issues relating to the possible presentation, and asked if Rambus agreed with the JEDEC policy on patent disclosure and licensing. Mr. Crisp told Mr. Kelley that he could not agree for Rambus on the policy for licensing; Mr. Kelley responded that if Rambus agreed with the patent policy, he could make a presentation. (G. Kelley, Tr. 2486-87). Mr. Kelley testified that Mr. Crisp never said anything that made Kelly believe that Rambus would not comply with the JEDEC patent disclosure policy. (G. Kelley, Tr. 2488-89).

Rambus's Response to Finding No. 907:

The proposed finding is inaccurate and incomplete. First, the proposed findings summary of Mr. Kelley's testimony contains a number of inaccuracies. For example, Mr. Kelley did not testify that the possible patent issues with JEDEC could be characterized as "rumors;" Mr. Kelley did not testify that he asked Mr. Crisp whether there were "patents or patent issues relating to" Mr. Crisp's proposal, but rather whether there "patent or patent applications that applied" to the proposal. Second, the proposed finding is incomplete. Mr. Kelley also testified that he had refused to allow Rambus present its technology for standardization at JEDEC on this and another occasion, even though he had never barred any other company from making a presentation. (Kelley, Tr. 2649-58; RPF 181). Mr. Kelley further testified that he was only empowered to do so with respect to Rambus by virtue of a completely undocumented "hand vote" at the May 1991 JC 42.3 meeting. (*Id.*). Mr. Kelley had a clear conflict of interest, however: he made and enforced his unilateral decision to bar Rambus from presenting its technology *two weeks* after he wrote in an internal company document that his company's interests were threatened by the Rambus technology and were best served if Rambus "fails to become standard." (RX 279 at 7). He did not disclose this conflict to Mr. Crisp or to anyone else. (Kelley, Tr. 2656-57).

908. At the May 1992 Committee meeting, after "lengthy discussion," the Committee agreed to issue ballots on several items, including the SDRAM Truth Table and Test Mode Entry. (CX0034A at 3).

Rambus's Response to Finding No. 908:

Rambus has no specific response.

909. At the May 1992 Committee meeting Mr. Crisp did not make any disclosure to the Committee concerning any Rambus patent or patent application. (Crisp, Tr. 3316). Mr. Crisp did not inform the Committee that the matters under discussion in connection with SDRAM

standardization involved inventions that Rambus believed it owned. (CX2092 at 148, 150).

Rambus's Response to Finding No. 909:

The proposed finding is misleading because it suggests that Mr. Crisp had a Rambus patent or patent application to disclose. In fact, Complaint Counsel have stipulated that, prior to the adoption of the JEDEC SDRAM standard in 1993, Rambus had no claims in any pending patent application that, if issued, would have necessarily been infringed by the manufacture or use of any device manufactured in accordance with the 1993 JEDEC SDRAM standard. (Parties' First Set of Stipulations, No. 9.) The proposed finding is also misleading because it suggests that Mr. Crisp should have disclosed some inventions in connection with SDRAM standardization that he believed were owned by Rambus. Even if, contrary to the weight of the evidence and the holding of the Federal Circuit, a JEDEC representative's beliefs could trigger a disclosure obligation, Complaint Counsel did not meet their burden of proving that Richard Crisp held such a belief at any relevant time. (RPF 418-22). Moreover, Mr. Crisp's open refusal to comment in response to a question regarding Rambus's potential intellectual property interests constituted notice to JEDEC that Rambus might have such interests and was not going to inform the committee about them, as Gordon Kelley testified. (Kelley, Tr. 2579) ("[a] comment of no comment is notification to the committee that there should be a concern" about intellectual property issues). Kelley's fellow IBM representative, Mark Kellogg, held the same view; he recorded Mr. Crisp's refusal to comment in his meeting notes because it "would have been a flag." (Kellogg, Tr. 5322).

Late May 1992 - Discussion With Patent Counsel

910. In late May 1992, Rambus patent counsel Lester Vincent communicated with

Richard Crisp of Rambus concerning further proposed amendments to Rambus pending patent applications. (CX1947; CX3125 at 330-31 (Vincent, Dep.); Crisp, Tr. 3068-69). According to Mr. Vincent's notes, Mr. Roberts told him "Richard has claims for cases we have filed plus claims for divisionals," including adding claims to "mode register and control latency." (*Id.*).

Rambus's Response to Finding No. 910:

The proposed finding is not supported by the evidence. The notes cited do not refer to Mr. Roberts, but only to a conversation with Richard Crisp. (CX1947). While the notes do state that "Richard has claims for cases we have filed plus claims for divisionals," they do not discuss claims to "mode register and control latency." (*Id.*). The proposed finding appears to be a muddle of two exhibits – CX1947 and CX1946. However, CX1946 likewise does not refer to claims to "mode register *and* control latency," suggesting two separate features, but rather to claims to "mode register *to* control latency." (CX1946; Response to Finding No. 900).

Rambus June 1992 Business Plan

911. In June 1992, Rambus CEO Geoffrey Tate transmitted to the Rambus Board of Directors a comprehensive five-year business plan, which, he explained, was based on "inputs from all of the executives." (CX0543A at 1). The minutes of the Board's June 25, 1992 meeting reflect that this "5-Year Business Plan" was discussed. (CX0604 at 2).

Rambus's Response to Finding No. 911:

Rambus has no specific response.

912. As reflected in the "Executive Summary" of this June 1992 Business Plan, Rambus remained committed to:

> "establish[ing] strong intellectual property barriers";
> "establish[ing] Rambus as the new interface standard"; and
> "establish[ing] a very high profit stream of technology royalties."

(CX0543A at 3).

Rambus's Response to Finding No. 912:

This proposed finding is misleading because it omits relevant evidence. The three

quotations contained in the proposed finding are from a lengthy list of bullet points set forth in the Executive Summary portion of the cited document. Not only does the proposed finding omit six of the nine bullet points entirely, it also omits portions of the bullet points from which it does quote. The omitted bullet points include:

"develop a breakthrough technology with high value added in a large percentage of computer, communications, and consumer digital systems products;"

"to license the technology for integration onto high volume ICs of all major IC companies and to have license fees cover the costs of technology and market development;"

"to establish Rambus as the new interface standard for systems requiring high performance at low cost;" (underlined portion omitted in proposed finding);

"to continually improve on Rambus Technology through minor and major enhancements" (CX0543A at 3).

Moreover, Mr. Tate did not describe his "draft" June 1992 business plan as "comprehensive." Rather, he expressly stated that it was prepared for the limited purpose of acquiring additional funding. (CX 0543A at 1) ("The 'spur' to do this is the Lease Line we are arranging with Phoenix.").

913. The June 1992 Business Plan reported that Rambus was making good progress in obtaining patents over its inventions. It reported that "Rambus Technology is currently covered by 18 [filed] patents, with over 300 claims, filed in the United States. Most of the patents have been or will be filed in other major countries in Europe and Asia." (CX0543A at 5). The Plan stated that the filed patents were "extensive and fundamental" and said that "[i]t is Rambus' opinion . . . that companies will not be able to develop Rambus-compatible technology or Rambus-like technology without infringing on multiple fundamental claims of the patents." (*Id.* at 9).

Rambus's Response to Finding No. 913:

Rambus has no specific response.

914. With respect to the key goals of establishing Rambus as the new interface standard and establishing a high profit stream of technology royalties (CX0543A at 3), the June 1992 Business Plan acknowledged that Rambus faced two principal impediments: "Resistance to Business Model" and "Competitive Solutions." *(Id.* at 14). Regarding the former, The Plan reported that some firms "have had a very negative reaction to our business model" including resistance to paying royalties to Rambus and fear that the royalties would make chips containing the Rambus technology "too expensive. (*Id.* (emphasis added)).

Rambus's Response to Finding No. 914:

The proposed finding misrepresents the evidence. Although the "draft" business plan has subsections headed "Resistance to Business Model" and "Competitive Solutions," these are not "acknowledged" as "principal impediments. To the contrary, the draft dismisses "Competitive Solutions" as any impediment at all, noting that "[t]here is no technology that is a breakthrough technology similar to Rambus." (CX0543A at 14). With respect to "Resistance to Business Model," while acknowledging that "a few" companies "have had a very negative reaction to our business model," the draft goes on to point out that "[m]ost systems customers" agree that the key is whether Rambus is better than an alternative solution on "performance, price, features." (*Id.*). The draft also noted that Rambus should explain that "our royalties are in line with IC industry traditional royalty levels of 1-5%." (*Id.*).

915. According to the 1992 Business Plan, the principal competitive threat to RDRAM at this time continued to be JEDEC's emerging standards for "Synchronous DRAMs" which did not suffer from the same "price negative and risk negative associated with Rambus." (CX0543A at 17; see also *id.* at 16 ("many system customers perceive . . . that Sync DRAMs will be sourced more broadly and more quickly," and hence "will be much cheaper," than RDRAMs)).

Rambus's Response to Finding No. 915:

The proposed finding is misleading. The draft referred to a "price negative and risk

negative associated with Rambus" only in terms of what "many system customers perceive." (CX0543A at 16-17). Thus, the draft indicated that this perception could be removed by proving RDRAM in non-main memory markets, such as graphics. (*Id*. at 17). The last sentence of the finding also omits the very next sentence in the document, which sheds a very different light on the discussion:

> "Reality is that 18 Mbits, Sync and RDRAMs will have the same die size – and Rambus already has 3 fully-compatible sources, whereas no two SyncDRAMs in development are pin-compatible!"

(CX 543A at 16).

916. The June 1992 Business Plan outlined multiple alternative strategies for responding to the competitive threat posed by Synchronous DRAMs. According to the Plan, "Our #1 strategy to counter Sync DRAMs is to get our parts proven and in the market." (CX0543A at 16). In addition, the Plan contemplated that Rambus would seek "to gain momentum rapidly in non-main-memory markets where Sync DRAMs are NOT an issue." (*Id.* at 17).

Rambus's Response to Finding No. 916:

The proposed finding misrepresents the evidence. There is nothing in the draft to suggest that the strategies described are "alternative," rather than complementary, strategies. (CX0543A at 16-17).

917. In addition to these strategies, the June 1992 Business Plan stated a patent-based strategy for attacking SDRAMs:

> Finally, we believe that Sync DRAMs infringe on some claims in our filed patents; and that there are additional claims we can file for our patents that cover features of Sync DRAMs. Then we will be in a position to request patent licensing (fees and royalties) from any manufacturer of Sync DRAMs.

(CX0543A at 17). The Plan referred to an "action plan" pursuant to which Rambus would identify and file additional patent claims and thereafter inform SDRAM manufacturers, all during

1992. (*Id.*) The disclosure portion of this action plan was not executed, however. During the time that Rambus was a member of JEDEC, its representative Mr. Crisp did not disclose any Rambus patent applications or patents to JEDEC, except for the '703 patent disclosed in September 1993. (Crisp, Tr. 3316, 3176).

Rambus's Response to Finding No. 917:

The proposed finding is inaccurate, misleading, and incomplete in a number of ways. First, by asserting that "[t]he disclosure portion of this action plan was not executed," the proposed finding implies that the part of the "draft" plan relating to filing claims covering SDRAMs *was* executed. This is false. Indeed, Complaint Counsel have stipulated that Rambus had no claims pending that would cover SDRAMs prior to the adoption of the SDRAM standard in 1993. (Parties' First Set of Stipulations, no. 9). In fact, Rambus had no claims that would necessarily read on JEDEC-compliant SDRAMs prior to mid-1999. (*See* Stipulated Patent Tree (earliest patent asserted by Rambus against DRAM manufacturers issued in June 1999))**.** The proposed finding is also misleading because, by stating that Mr. Crisp did not disclose any patent applications or patents to JEDEC other than the '703 patent, the proposed finding implies that were patents or applications that should have been disclosed. There were not. RPF 327-396. It is also incorrect to say that Mr. Crisp did not disclose any patent applications to JEDEC because, in fact, the '703 patent, which was disclosed, lists 9 other pending applications. (RX 425 at 11).

This proposed finding is also misleading because it implies that a plan to "attack" SDRAMs was complete and ready to be implemented. Rambus CEO Geoff Tate testified instead that the statement in the June 1992 draft plan that "we believe that Sync DRAMs infringe on some claims in our filed patents"was based on a "feeling" that "synchronous DRAMs sure looked like they stem[med] from [our] inventions." (CX 2073, Tate *Micron* Depo. at 221-22).

Mr. Tate had "assumed" that broad patent applications had been filed to protect all of Rambus's inventions. (CX 2073, Tate *Micron* Depo. at 222; CX 2088, Tate *Infineon* Trial Testimony at 57). At the time that he wrote the June 1992 draft, Mr. Tate did not know of any particular claim that might be infringed by SDRAMs. (*Id.*).

After the June 1992 draft was prepared, a Rambus employee was assigned the task of determining what filed claims would be infringed by SDRAMs. (CX 2073, Tate Micron Depo. at 222-3). After hearing the employee's report, Mr. Tate concluded that the filed claims were not as broad as previously thought and did not cover SDRAMs. (CX 2073, Tate Micron Depo. at 222-24; CX 2088, Tate Infineon Trial Testimony at 57-58). (*See* RPF 423-424).

918. The belief that Rambus had intellectual property claims to JEDEC SDRAM technology was widespread at Rambus. Vice-President Mooring could not recall any Rambus executive having a belief different than that expressed in the June 1992 business plan concerning Rambus patent coverage over SDRAM technology. (CX2079 at 155-56 (Mooring, Micron Dep.)) (Note; pending R objection] Former Rambus Chief Financial Officer Gary Harmon testified that from the time he started at Rambus in 1993, he heard "from various people that Rambus' patents were so fundamental and so broad that they likely covered technology that was being used by any other high-speed DRAM." (CX2070 at 97 (Harmon, Micron Dep.)). The source of this information was Mr. Tate, Mr. Mooring and others "who just gave the general impression that Rambus technology was broad." (CX2070 at 98 (Harmon, Micron Dep.)). This view extended to DDR when it was discussed in later years. (CX2070 at 100-01 (Harmon, Micron Dep.)).

Rambus's Response to Finding No. 918:

The proposed finding is misleading and incomplete. Mr. Mooring testified that what the June 1992 draft described as a "belief" that SDRAMs might infringe Rambus's patent claims was equally well characterized as a "*hope* that synchronous DRAMs infringe on some claims." (CX2079, Mooring Micron Depo., at 155). Mr. Harmon confirmed that "it was generally *speculated* at Rambus" that they might have claims to more than just RDRAMs. (CX2070,

Harmon Micron Depo., at 96). The "speculat[ion]" and "general feeling" that Rambus might have claims to SDRAM or DDR SDRAM did not become a more specific belief until well after Joel Karp came to Rambus to take charge of its intellectual property portfolio. (*Id.* at 95-96, 101).

919. On June 11, 1992, the JC-42.3 Committee issued a series of four ballots. (CX252A; CX253; CX254). One of the four ballots, item 3763, proposed to include with the SDRAM standard a programmable mode register incorporating programmable CAS latency and burst length. (CX0252A at 3; Crisp, Tr. 3075-76; Rhoden, Tr. 448; Willliams, Tr. 811-812; Sussman, Tr. 1390-1391)). The ballot directed: "If anyone receiving this ballot is aware of patents involving this ballot, please alert the Committee accordingly during your voting response. (CX252A at 2).

Rambus's Response to Finding No. 919:

The ballot did not "direct" anything, as this finding asserts. When the ballot language regarding patents was first added to JEDEC ballots, a JEDEC member asked during a JEDEC meeting about the purpose of the new language. The minutes of the JC 42.1 meeting held on September 13, 1989 state that:

> "Council discussed patent issue at their June meeting at the request of JC-42.3. The result was not to change EIA legal requirements as outlined in document EP-7, but to add some wording on JEDEC ballot voting sheets about informing the Committee if any patent covers the balloted material. TI was concerned that Committee members could be held liable if they didn't inform Committee members correctly on patent matters. Committee responded that the question was added on ballot voting sheets for information only and was not going to be checked to see who said what."

(CX 3 at 6).

The statements in the official JEDEC meeting minutes that the patent-related question on the ballot was added "for information only" and that the ballots were "not going to be checked to see who said what" are inconsistent with the proposition that the ballot language was intended to, or did, express any mandatory disclosure obligation. (CX 3 at 6).

920. On June 22, 1992, Mr. Crisp spoke to Mr. Lester Vincent regarding pending Rambus divisional patent applications. (CX3125 at 332-33 (Vincent Dep.); Crisp, Tr. 3076-79). Mr. Crisp wanted to file a preliminary amendment soon, but Mr. Vincent recommended waiting a few months because Rambus was not losing any rights. (CX3130 at 81-82 (Vincent, Dep.)).

Rambus's Response to Finding No. 920:

The proposed finding is incomplete. Mr. Vincent recommended waiting not just because Rambus was not losing any rights but because waiting would allow Rambus to see what office actions might be forthcoming from the PTO prior to filing an amendment. (CX3130, Vincent Depo., at 82-83).

July 1992 - Committee Meeting and Vote on Elements of the SDRAM Standard

921. In July 1992 Richard Crisp and David Mooring were present for Rambus at the JEDEC JC-42.3 Committee meeting in Denver, Colorado. (JX0013 at 1-2). The Chairman Mr. Townsend showed the patent policy and tracking list. (JX0013 at 4).

Rambus's Response to Finding No. 921:

Rambus has no specific response.

922. At the July 1992 meeting, the Committee tabulated and discussed the results of the four ballots that had been approved at the June 1992 meeting of the Committee. (JX0013 at 9-10). The proposals that had been circulated for a vote included one concerning the use of a mode register for programming CAS latency. (JX0013 at 10).

Rambus's Response to Finding No. 922:

The proposed finding is inaccurate. There is no evidence of a Committee meeting in June

1992; the four ballots were issued in June. (CCFF 919).

923. The proposals carried by more than the two-thirds required by the Committee rules. (JX0013 at 9-10; Rhoden, Tr. 451-52). Pursuant to the established procedures of the Committee, comments were made by members concerning the proposals and addressed in open discussion by the Committee. (JX0013 at 9-10; Rhoden, Tr. 452).

Rambus's Response to Finding No. 923:

Rambus has no specific response.

924. Among the matters discussed at the July 1992 Committee meeting were concerns by IBM over patent issues. (JX0013 at 9 ("Patent issues must be cleaned up before we proceed.")). During the meeting the Motorola representative received a letter from the company legal staff concerning a Motorola patent; the letter was shown by the Committee chairman and accepted by the Committee as complying with the JEDEC patent policy. (*Id.* at 9, 136).

Rambus's Response to Finding No. 924:

The proposed finding is incomplete and misleading. The minutes state that the letter from Motorola was accepted by the Committee as complying with the JEDEC patent policy because the "Committee agreed that it met the EIA patent requirements." (JX0013 at 9).

925. Richard Crisp was present at the July 1992 meeting of the Committee and participated for Rambus in the discussion and the vote on the proposals, including the mode register proposal. (JX0013 at 1, 9-10). David Mooring of Rambus also was present. (JX0013 at 2). Rambus voted "no" to the proposals. (*Id.* at 9-10; CX2112 at 78-79 (Mooring, Dep.)).

Rambus's Response to Finding No. 925:

Rambus has no specific response.

926. Mr. Mooring, who was present for Rambus at this Committee meeting, was aware as of early 1991 that programmable CAS latency and programmable burst length either surely or likely were Rambus inventions. (CX2054 at 84-85 (Mooring, Infineon Dep.)) Mr. Mooring recalled that in the 1992-93 time period there was "some belief we [Rambus] actually had patent applications on SDRAM." (CX2054 at 89-90 (Mooring, Infineon Dep.)). Rambus CEO Tate and Richard Crisp were individuals within Rambus who held or professed such beliefs. (CX2056 at 252 (Mooring, Infineon Dep.)).

Rambus's Response to Finding No. 926:

The proposed finding is inaccurate and misrepresents the evidence. Mr. Mooring was *not* aware as of early 1991 that programmable CAS latency and programmable burst length either "surely or likely" were Rambus inventions, as the testimony cited by Complaint Counsel for the contrary proposition makes clear. Rather, Mr. Mooring testified to his belief that "some, if not all" of the four features – programmable CAS latency, programmable burst length, on-chip DLL or PLL, and dual-edge clocking – were "surely or likely" Rambus inventions. (CX2054, Mooring Infineon Depo., at 84-85). Of these four, Mr. Mooring believed that it was more likely that the *latter* two, i.e. *not* programmable CAS latency and burst length, were Rambus inventions. (*Id.* at 85).

Mr. Mooring's testimony as to the beliefs of others at Rambus regarding coverage over SDRAM was based on just "two memories, one of Richard Crisp investigating that at one point and once when we were doing our business plan late in '92." (*Id.* at 91). With respect to Mr. Crisp's investigation, Mr. Mooring recalls that Mr. Crisp determined that the pending patent claims were *not* broad enough to cover SDRAM. (*Id.* at 94.) With respect to the draft business plan, Mr. Mooring testified that it basically expressed the "hope" that Rambus might have claims that covered SDRAMs. (*See* Response to Finding No. 918). In any case, soon after the draft plan was circulated, Mr. Tate concluded that Rambus did not, in fact, have claims pending that were sufficiently broad to cover SDRAM. (CX 2073, Tate Micron Depo. at 222-24; CX 2088, Tate Infineon Trial Testimony at 57-58). *See also* RPF 423-24; RRFF 765.

927. Mr. Crisp cast the vote for Rambus and made technical comments concerning the proposals, but despite the discussion of patent issues at the meeting did not say anything concerning Rambus patents or patent applications. (Crisp, Tr. 3082-84, 3087; Rhoden, Tr. 453-

54; Williams, Tr. 816-20; (CX2056 at 236, CX2112 at 78 (Mooring, Dep.)). Mr. Crisp did not inform the Committee that the matters under discussion in connection with SDRAM standardization involved inventions that Rambus believed it owned. (CX2092 at 148, 150).

Rambus's Response to Finding No. 927:

The proposed finding is misleading because it suggests that there existed a Rambus patent or patent application for Mr. Crisp to disclose. In fact, Rambus had no issued patents at this time. Moreover, Complaint Counsel have stipulated that, prior to the adoption of the JEDEC SDRAM standard in 1993, Rambus had no claims in any pending patent application that, if issued, would have necessarily been infringed by the manufacture or use of any device manufactured in accordance with the 1993 JEDEC SDRAM standard. (Parties' First Set of Stipulations, No. 9.) The proposed finding is also misleading because it suggests that Mr. Crisp should have disclosed some inventions in connection with SDRAM standardization that he believed were owned by Rambus. Even if, contrary to the weight of the evidence and the holding of the Federal Circuit, a JEDEC representative's beliefs could trigger a disclosure obligation, Complaint Counsel did not meet their burden of proving that Richard Crisp held such a belief at this time. (RPF 418-22).

August 1992 - Conference with Patent Counsel

928. Rambus patent counsel Lester Vincent conferred by telephone with Richard Crisp in late August 1992 concerning amendment of Rambus patent claims. (CX3130 at 99-100 (Vincent, Dep.); CX1930 at 42).

Rambus's Response to Finding No. 928:

Rambus has no specific response.

September 1992 - Committee Meeting

929. In September 1992 Richard Crisp and Billy Garrett were present for Rambus at the

JEDEC JC-42.3 Committee meeting in Crystal City, Virginia. (CX0042A at 1; Crisp, Tr. 3093-3096). The Chairman Mr. Townsend reported on the patent policies and showed the patent tracking list. (CX0042A at 2).

Rambus's Response to Finding No. 929:

Rambus has no specific response.

930. Mr. Garrett and Mr. Crisp reported to senior executives of Rambus, including CEO Tate, Vice-President Roberts and board member Farmwald, concerning the matters under discussion at the meeting; among the matters discussed and reported were the inclusion of programmable CAS latency and programmable burst length in the SDRAM standard under discussion by the Committee. (CX0680 at 1, 2; Crisp, Tr. 3094-95).

Rambus's Response to Finding No. 930:

The proposed finding is not supported by the evidence. Mr. Garrett sent an e-mail regarding the September 1992 JEDEC meeting to certain Rambus personnel, including Messrs. Tate, Roberts and Farmwald. (CX0680). The cited evidence does not suggest that Mr. Crisp reported on the meeting.

931. Notwithstanding these discussions at the September 1992 meeting of the Committee, Mr. Crisp did not inform the Committee in September 1992 of the Rambus efforts to seek claims in its patent applications pertaining to SDRAM features. (Crisp, Tr. 3316). Mr. Crisp did not inform the Committee that the matters under discussion in connection with SDRAM standardization involved inventions that Rambus believed it owned. (CX2092 at 148, 150).

Rambus's Response to Finding No. 931:

The proposed finding is misleading. Even if, contrary to the holding of the Federal Circuit and the weight of the evidence, "efforts to seek claims" were subject to a JEDEC disclosure duty, Complaint Counsel have not met their burden of showing that there were such efforts at this time. Complaint Counsel have stipulated that, prior to the adoption of the JEDEC SDRAM standard in 1993, Rambus had no claims in any pending patent application that, if

issued, would have necessarily been infringed by the manufacture or use of any device manufactured in accordance with the 1993 JEDEC SDRAM standard. (Parties' First Set of Stipulations, No. 9.) The proposed finding is also misleading because it suggests that Mr. Crisp should have disclosed some inventions in connection with SDRAM standardization that he believed were owned by Rambus. Even if, contrary to the holding of the Federal Circuit and the weight of the evidence, a JEDEC representative's beliefs could trigger a disclosure obligation, Complaint Counsel did not meet their burden of proving that Richard Crisp held such a belief at this time. (RPF 418-22).

September 1992 - Conference With Patent Counsel

932. In September 1992, approximately a week after the JEDEC Committee meeting, Mr. Crisp had a face-to-face meeting with Lester Vincent about further pursuit of divisional patent applications on behalf of Rambus. (CX1949).

Rambus's Response to Finding No. 932:

Rambus has no specific response.

933. Mr. Vincent's notes of his September 1992 meeting with Mr. Crisp reflect detailed discussion of a number of additional areas suggested by Mr. Crisp for coverage under patent claims by Rambus; these included programmable CAS latency, multiple open rows (or banks), source synchronous clocking and other concepts that had been under discussion at the most recent and past JEDEC meetings and reported to Rambus management by Messrs. Crisp and Garrett. (Crisp, Tr. 3097-3105; CX1949 at 1,2,5,7; CX3125 at 337-38, 338-340, 348-49 (Vincent, Dep.)). Mr. Vincent's notes make specific reference to "caus[ing] problems with Sync DRAM" and "SDRAM stuff worried about." (CX1949 at 1, 7; CX3125 at 339, 349 (Vincent, Dep.)).

Rambus's Response to Finding No. 933:

The proposed finding is inaccurate, misleading and incomplete. Mr. Vincent's notes do not reflect that "programmable CAS latency" was discussed, but, rather, the more general concept of "programmable latency." (CX1949 at 1). Mr. Vincent's notes do not reflect that

multiple "banks" were discussed, but, rather, the more general concept of "multiple open rows." (*Id*.; Crisp, Tr. 3098). This indicates that the discussion was not specifically directed at SDRAMs.

There is no mention of SDRAM in connection with programmable latency or multiple open rows. The notes refer to "cause problems with synch DRAM and Ramlink" under the heading of "packet-oriented comm. [communication]." (CX1949 at 1). This indicates that the reference was not to SDRAM, which is not "packet-oriented." (CCPF 1306). The notes refer to "SDRAM stuff worried about" under "source synch clocking." (CX1949 at 7). There is no evidence that source synchronous clocking was being considered in connection with SDRAM at this time.

934. Mr Vincent's notes of his September 1992 meeting with Mr. Crisp indicate, with respect to access time, that a broad independent claim was desired. (CX1949 at 2 ("make Indep. Claim => broad") (emphasis in original); CX3128 at 235-36 (Vincent, Dep.)).

Rambus's Response to Finding No. 934:

Rambus has no specific response.

935. Mr. Vincent's notes of his September 1992 meeting with Mr. Crisp reflect a desire to include claims covering use of phase lock loops, or PLLs, on DRAMs, (CX1949 at 1, 5, 7; CX3125 at 338-40, 345, 346-47 (Vincent, Dep.)). Mr. Vincent's notes indicate, with respect to PLLs on DRAMs, that they wanted to cover the concept of using PLLs or DRAMs, not just specific PLL circuits. (CX1949 at 5 ("=> many different ways of designing PLL – want to cover concept of .... deskewing input"); *id.* at 7 ("=> claim usage of such circuit on a DRAM – not particular PLL") (emphasis in original); CX3125 at 346-47 (Vincent, Dep.)).

Rambus's Response to Finding No. 935:

Rambus has no specific response.

937. Mr. Vincent's notes of his September 1992 meeting with Mr. Crisp discuss including coverage of packet-oriented commands. (CX1949 at 1 ("DRAM-packet oriented comm."); *id.* at 4 ("=>Rambus=> wants to claim memory device that receives commands via

packets"); CX3125 at 338-40 (Vincent Dep.)). Mr. Vincent's notes state "so cause problems w/ . . . Ramlink," and "Richard => will get me copy of the Ramlink spec." (CX1949 at 4; CX3125 at 342, 343 (Vincent, Dep.)).

Rambus's Response to Finding No. 936:

The proposed finding is inaccurate. The discussion between Mr. Vincent and Mr. Crisp involved "packet-oriented communication" not "packet-oriented commands." (CX3125, Vincent Depo., at 338-39).

September 1992 - Rambus Business Plan

937. In September 1992, Rambus CEO and President Geoffrey Tate circulated a revised business plan. (CX0545; CX2061 at 229 (Tate, Dep.)). That document stated: "Sync DRAMs infringe claims of Rambus filed patents and other claims that Rambus will file in updates later in 1992." (CX0545 at 21).

Rambus's Response to Finding No. 937:

The proposed finding is incomplete. Mr. Tate's statement regarding "Sync DRAMs infring[ing] claims of Rambus filed patents" was based on an assumption that Mr. Tate subsequently learned was incorrect. (RPF 423-24; RRFF 765). Moreover, Rambus did not file any patent claims in 1992 that covered SDRAMs. (Parties First Set of Stipulations, No. 9).

October 1992 - Rambus Board Briefing

938. In October 1992 Mr. Crisp and Mr. Mooring made presentations to the Rambus Board of Directors concerning among other things the status of SDRAM activity at JEDEC and the Rambus patent strategy. (CX0606 at 2; Crisp, Tr. 3108-09). Mr. Crisp made a presentation to the board concerning the status of SDRAM at JEDEC, and thereafter told the Board that Rambus was making efforts to broaden the Rambus patent applications to cover SDRAMs. (CX2092 at 162-63 (Crisp, Infineon Trial Tr.); CX2082 at 752 (Crisp, Dep.)). The issue of whether Rambus patents cover JEDEC standards was discussed at a Rambus Board meeting in 1992. (CX2054 at 62 (Mooring, Dep.)).

Rambus's Response to Finding No. 938:

The proposed finding is inaccurate and misleading. First, while Mr. Crisp made

presentations to the Board regarding the status of SDRAM at JEDEC and Rambus's patent strategy, Mr. Mooring's presentations were on different topics. (CX0606 at 2). Second, the cited evidence does *not* show that Mr. Crisp "told the Board that Rambus was making efforts to broaden the Rambus patent applications to cover SDRAMs." Mr. Crisp testified that he told the Board that part of Rambus's patent strategy was to try to broaden its claims, possibly including covering SDRAMs, but he did not testify that he told them that efforts along those lines were actually being made. (CX2092, Crisp, Infineon Trial Tr., at 162-63; CX2082, Crisp Infineon Depo., at 751-52). In fact, Rambus had no pending patent claims that covered SDRAMs until long after 1992. (Parties First Set of Stipulations, No. 9 (no pending claims prior to SDRAM standardization; RPF 327-396 (no pending claims prior to withdrawal from JEDEC))). The evidence does not support the proposed finding that the issue of whether Rambus patents cover JEDEC standards was discussed at a Rambus board meeting in 1992. The only evidence cited for this proposition by Complaint Counsel is Mr. Mooring's testimony; Mr. Mooring, however, made clear that he had no recollection of such a discussion and that his testimony was based solely on his recollection of recently reviewing the early board minutes, which referred to a presentation by Richard Crisp on this topic. (CX2054, Mooring Infineon Depo. at 62). Mr. Mooring was incorrect: the board minutes do not say that Mr. Crisp's presentation involved the issue of whether Rambus patents cover JEDEC standards. (CX0606 at 2).

November 1992 - Conference with Patent Counsel

939. In November 1992, after first informing CEO Tate and Vice-President Roberts, Richard Crisp and Michael Farmwald of Rambus met with Mr. Vincent, the Rambus patent counsel, to discuss Rambus patent claims. (CX682; CX1930 at 59; CX3130 at 107-08 (Vincent, Dep.); Crisp, Tr. 3109-11). The purpose of the meeting was to discuss claims to be added to Rambus patent applications (CX682); the topics discussed included multiple row addresses and

synchronization (CX1930 at 59). The concept of multiple row addresses was broad enough to embrace the two bank design feature that had been discussed at JEDEC in connection with the SDRAM standard. (Crisp, Tr. 3097-98, 3110).

Rambus's Response to Finding No. 939:

Rambus has no specific response.

December 1992 - Committee Meeting

940. In December 1992 Richard Crisp and David Mooring were present for Rambus at the JEDEC JC-42.3 Committee meeting in Fort Lauderdale, Florida. (JX0014; CX0042A at 1-2; Crisp, Tr. 3113-14).

Rambus's Response to Finding No. 940:

Rambus has no specific response.

941. Mr. Mooring reported to various Rambus executives, including CEO Tate, that views on the on the SDRAM features had "almost consolidated," and predicted that consensus on the standard would be reached by March 1993. (CX0685 at 1; CX2055 at 103 (Mooring, Dep.)). Mr. Mooring also reported that, at the December 1992 meeting, IBM had stated that it was aware that some voting attendees at the Committee meetings had "patents pending on SDRAMs" that they had not made the Committee aware of. (*Id.*) Mr. Mooring's report reflects his recollection of the JEDEC meeting from the following day; he was merely reporting what IBM had said at the meeting. (CX2112 at 105, CX2055 at 100 (Mooring, Dep.)).

Rambus's Response to Finding No. 941:

Rambus has no specific response.

942. During the course of the December 1992 meeting, Committee chairman Jim Townsend made a presentation concerning the EIA patent policy and draft revisions to the JEDEC manual pertaining to the patent policy. (JX0014 at 3, 25; Crisp, Tr. 2984-86). Among other things, the language contained in the presentation materials stated that the patent policy applied to situations involving the discovery of patents that may be required for the use of a patent subsequent to its adoption. (JX0014 at 21). The presentation materials also made repeated reference to the need to make disclosure of "patented or patentable items," and stated that the term "patented" also included "pending patents on items and processes under consideration." (JX0014 at 25; Crisp, Tr. 2986-88).

Rambus's Response to Finding No. 942:

The proposed finding is inaccurate and incomplete. The minutes of the December 1992 meeting expressly identify the presentation materials quoted in the proposed finding as a "draft." (JX0014 at 3). Moreover, contrary to the proposed finding, the draft does not contain any language whatsoever referring to a "need to make disclosure" of any intellectual property on the part of JEDEC members, whether patents or pending patents. (JX0014 at 21-28).

943. These revisions were later embodied in the next version of the JEDEC manual. (CX208A at 19).

Rambus's Response to Finding No. 943:

The proposed finding is inaccurate, incomplete and misleading. First, the relevant sections of JEDEC manual 21-I were substantially different from the "draft" that was presented at the December 1992 meeting. (JX0014 at 25; CX0208A at 19). In addition, Complaint Counsel did not meet their burden of establishing that the 21-I manual ever received the approval from EIA's Engineering Department Executive Council that was necessary to make it effective. (See RPF 165-70).

944. Notwithstanding these discussions at the December 1992 meeting of the Committee, Mr. Crisp did not inform the Committee in December 1992 of the Rambus efforts to seek claims in its patent applications pertaining to SDRAM features. (Crisp, Tr. 3316).

Rambus's Response to Finding No. 944:

The proposed finding is misleading. First, the proposed finding seems to suggest that discussions of draft revisions to the JEDEC patent policy somehow imposed disclosure obligations on JEDEC members. They did not. Second, the draft revisions themselves did not contain any disclosure duty. Third, the draft revisions made no reference to "efforts to seek

claims." Fourth, even if, contrary to the holding of the Federal Circuit and the weight of the evidence, "efforts to seek claims" were subject to a JEDEC disclosure duty, Complaint Counsel have not met their burden of showing that there were such efforts by Rambus at this time. Complaint Counsel have stipulated that, prior to the adoption of the JEDEC SDRAM standard in 1993, Rambus had no claims in any pending patent application that, if issued, would have necessarily been infringed by the manufacture or use of any device manufactured in accordance with the 1993 JEDEC SDRAM standard. (Parties' First Set of Stipulations, No. 9.)

945. An internal Rambus document entitled "Architectural Issues" and dated approximately one week after the December 1992 Committee meeting among other things states a plan to "get a copy of the SDRAM spec and check it for features we need to cover as well as features which violate our patents." (CX1821 at 24).

Rambus's Response to Finding No. 945:

Rambus has no specific response.

February 1993 - Work on Rambus Patent Applications

946. In February 1993, Rambus CEO and President Geoffrey Tate sent an email to all Rambus staff noting that NEC, Toshiba, Fujitsu, Hitachi, Mitsubishi and Micron all had announced that in the second half of 1993 they would introduce samples of synchronous DRAMs that lined up with the anticipated JEDEC standard. (CX0688).

Rambus's Response to Finding No. 946:

Rambus has no specific response.

947. In early 1993 Rambus employee Fred Ware began to work with Rambus patent counsel Mr. Vincent in connection with the Rambus pending patent applications. Mr. Ware was an engineer in the "architecture group" inside Rambus and was in a reporting chain that reported to Vice-President Allen Roberts. (Crisp, Tr. 3119-20).

Rambus's Response to Finding No. 947:

Rambus has no specific response.

948. In February 1993 Mr. Ware asked Mr. Crisp for a list of claims under consideration for addition to the original Rambus patent. (CX0686). Mr. Crisp's email response identified several items, including "DRAM with programmable access latency," a broad concept that included programmable CAS latency as discussed earlier at JEDEC. (CX0686; Crisp, Tr. 3121-22). Mr. Crisp also identified "DRAM with multiple open rows," a technology related to but broader than the two bank feature discussed within JEDEC. (CX0686, Crisp, Tr. 3122). Mr. Crisp also identified "DRAM using PLL/DLL circuit to reduce input buffer skews." (CX0686; Crisp, Tr. 3122). In a follow-on communication a few days later Mr. Crisp also identified external reference voltage, a technology similar if not the same as had been discussed at JEDEC; his response to Mr. Ware indicated that adding such a claim to Rambus's patent protection "should help confound the . . . effort" to develop industry standard technology. (CX691; Crisp, Tr. 3123-24).

Rambus's Response to Finding No. 948:

The proposed finding is incomplete and misleading. Mr. Crisp's first e-mail also identified "DRAM with packet oriented communication protocol" as an item under consideration. (CX0686). The follow-on communication states that adding a claim "where the voltage reference is provided to a dynamic memory chip for setting the input receiver's thresholds . . . should help confound the GTL effort." (CX0691). Complaint Counsel have introduced no evidence about the GTL standardization effort or of any obligations of Rambus with respect to it.

949. By February 1993, Rambus was aware that major DRAM manufacturers had announced their intention to line up with the JEDEC SDRAM standard under development. CEO Tate sent an email to Rambus staff that made reference to press reports indicating that NEC, Toshiba, Fujitsu, Mitsubishi and Micron had all indicated their intention to align themselves with the JEDEC standard. (CX0688; Crisp, Tr. 3125-26).

Rambus's Response to Finding No. 949:

The proposed finding is misleading. In context, the statements in the e-mail indicate not that the DRAM manufacturers intended to "line up" with the JEDEC SDRAM standard, but that they intended to manufacture products that lined up with that standard. (See CCPF 946).

March 1993 - JEDEC Committee Meeting

950. In March 1993 William ("Billy") Garrett was present for Rambus at the JEDEC JC-42.3 Committee meeting in Scottsdale, Arizona. (JX0015 at 2). The Chairman Mr. Townsend presented the patent policies and showed the patent tracking list, and there was discussion by members concerning patent issues. (JX0015 at 4).

Rambus's Response to Finding No. 950:

Rambus has no specific response.

951. Among the patent matters discussed at the March 1993 Committee meeting was an inquiry made to IBM concerning whether IBM would disclose to the Committee all patents and patent applications held by the company worldwide. (G. Kelley, Tr. 2449-50; JX0015 at 6). Because of the breadth and difficulty of the company-wide search that would be required for such a listing, there was a risk that any such listing would be incomplete and misleading, and so IBM stated that it would not undertake such a listing. (G. Kelley, Tr. 2450-51). However, the IBM representative did assure the Committee that he would alert the group to any patent information known to him, and would provide a response to any patent question raised by Committee members. (G. Kelley, Tr. 2451-52).

Rambus's Response to Finding No. 951:

The proposed finding is against the weight of the evidence. The official minutes reflect no inquiry to IBM about a list of all of its patents and applications. Instead, the minutes record that IBM stated that its "view has been to ignore [the] patent disclosure rule because their attorneys have advised them that if they do then a listing may be construed as complete." (JX0015 at 6). IBM made its position even more clear in December 1993, noting "that in the future they will not come to the committee with a list of applicable patents on standards proposals. It is up to the user of the standard to discover which patents apply." (JX0018 at 8).

Contrary to Mr. Kelley's testimony that he assured the committee that he would alert the committee to any patent information known to him, there were no IBM patents or patent applications added to the "patent tracking list" maintained by JC 42 Chairman Jim Townsend

between December 1993 and December 1995. (RPF 196).

Contrary to Mr. Kelley's trial testimony that he agreed to provide a response to any patent question raised by Committee members, Mr. Kelley refused to do just that with respect to IBM's BGA patents in August 1993, writing:

> "IBM Intellectual Property Law attorneys have informed me that we will not use JEDEC as a forum for discussing this subject. It is the responsibility of the producer to evaluate the subject and to work out the proper use of rights. So, I can not confirm or deny any IPL rights."

(RX 420 at 2).

952. At the March 1993 meeting, the Committee passed the last of the ballots that made up the SDRAM standard, and approved the issuance of a press release announcing that the Committee had approved the SDRAM standard. (JX0015 at 14, 99).

Rambus's Response to Finding No. 952:

Rambus has no specific response.

953. Notwithstanding these developments at the March 1993 meeting of the Committee, Mr. Garrett did not inform the Committee in March 1993 of the Rambus efforts to seek claims in its patent applications pertaining to SDRAM features. (CCFF 863-65).

Rambus's Response to Finding No. 953:

The proposed finding is misleading. Even if, contrary to the holding of the Federal Circuit and the weight of the evidence, "efforts to seek claims" were subject to a JEDEC disclosure duty, Complaint Counsel have not met their burden of showing that there were such efforts at this time. Complaint Counsel have not asserted that Rambus had any claims pending prior to January 1995 that would cover JEDEC-compliant SDRAMs. Complaint Counsel have also *stipulated* that, prior to the adoption of the JEDEC SDRAM standard in 1993, Rambus had

no claims in any pending patent application that, if issued, would have necessarily been infringed by the manufacture or use of any device manufactured in accordance with the 1993 JEDEC SDRAM standard. (Parties' First Set of Stipulations, No. 9.) There is also no evidence that Mr. Garrett was aware of the progress of Rambus's patent prosecution efforts.

April 1993 - Rambus Renews Its JEDEC Membership

954. In April 1993 Rambus paid its dues to renew its JEDEC membership for the 1993 calendar year. (CX602 at 11; Stipulation, Tr. 3143-44).

Rambus's Response to Finding No. 954:

Rambus has no specific response.

April-May 1993 - Consultations with Patent Counsel and Pursuit of Claims

955. In late April 1993 Lester Vincent, patent counsel for Rambus, sent to Messrs. Farmwald, Roberts and Crisp of Rambus proposed preliminary amendments to pending Rambus patent applications. (CX1957; CX1457; Crisp, Tr. 3145-48).

Rambus's Response to Finding No. 955:

Rambus has no specific response.

956. On May 4, 1993, Mr. Lester Vincent apparently sent Mr. Crisp a presentation regarding industry standards that said, "Two possible legal theories for non-enforcement [of patents]: 1) Estoppel? 2) Antitrust?" (CX1958 at 12). Mr. Vincent thought that Mr. Crisp might be interested in the presentation handout because of Mr. Vincent's March 1992 meeting in which he discussed the issue of equitable estoppel with Mr. Crisp and Mr. Roberts of Rambus. (CX3126 at 397 (Vincent, Dep.)). The materials included as pages 2-22 of CX1958 were produced from Mr. Vincent's files and are the only presentation relating to industry standards that were found in his files. (CX3126 at 396-97, CX3128 at 255-56 (Vincent, Dep.)).

Rambus's Response to Finding No. 956:

Rambus has no specific response.

957. The presentation summarized the Stambler v. Diebold decision as specific example of equitable estoppel as a defense to a claim of patent infringement. (CX1958 at 15, 16 ("Plaintiff could not remain silent while an entire industry implemented the proposed standard

and then when the standards were adopted assert that his patents covered what manufacturers believed to be an open and available standard." (*quoting* Stambler v. Diebold, 11 USPO 2d 1709, 1715 (E.D.N.Y. 1988), aff'd, 11 USPO 2d 1715 (Fed. Cir. 1989)).

Rambus's Response to Finding No. 957:

The proposed finding is incomplete and misleading. *Stambler* is only one of several cases cited, and the presentation notes that it is "only a District Court case." (CX 1958 at 15). It involved an *issued* patent and *actual* knowledge of infringement by the patentee. (*Id.*). Moreover, the presentation also lists the elements required for estoppel and notes that one required element is "affirmative conduct by the patentee inducing the belief that it had abandoned its claims against the alleged infringer." (CX1958 at 13). The presentation states that in order to satisfy this element, you "need affirmative conduct," because "silence alone is not sufficient," although there is "some authority for applying equitable estoppel where there has been 'intentionally misleading silence' (i.e., a duty to speak)." (CX1958 at 14). The presentation also states that "estoppel cannot arise out of unilateral expectations or even reasonable hopes of one party." (*Id*.) In any case, the cited evidence does not show that Richard Crisp ever reviewed the presentation, and Mr. Crisp does not recall receiving it. (Crisp, Tr. 3001).

958. On May 13, 1993, Mr. Vincent conferred with Messrs. Farmwald and Crisp concerning the draft amendments to Rambus pending patent applications that were sent to Rambus in April. (CX1930 at 83). On May 17, Mr. Vincent's firm filed the preliminary amendments with the Patent and Trademark Office. (CX1458; CX3129 at 412-14 (Vincent, Dep.)). One of the preliminary amendments filed on May 17 added language to the pending Rambus '651 patent application describing a claim for programmable CAS latency. (CX1458 at 5 (claim 151(D), adding claim for circuitry "for storing a value corresponding to a predetermined time period during which the interfacing circuitry must wait before transmitting reply information")). Mr. Crisp and others at Rambus understood the amendment to the '651 application to be "directed against SDRAMs." (CX0702; CX1959; CX0703; Crisp, Tr. 3153-57).

Rambus's Response to Finding No. 958:

The proposed finding is inaccurate, incomplete and misleading. Claim 151 of the '651 application did not "describ[e] a claim for programmable CAS latency;" rather claim 151 included numerous limitations, one of which involved storing a latency value. (CX1458 at 5). Another limitation, required that data, address, and control information be "in the form of packets." (*Id.*) This limitation plainly excluded SDRAMs from coverage. (CCFF 1306).

May 1993 - JEDEC Committee Meeting

959. On May 19-20,1993, Richard Crisp was present for Rambus at the JEDEC JC-42.3 Committee meeting in Chicago, Illinois. (JX0016 at 1; Crisp, Tr. 3158). The Chairman Mr. Townsend presented the patent policies and showed the patent tracking list, and there was discussion by members concerning patent issues. (JX0016 at 5).

Rambus's Response to Finding No. 959:

Rambus has no specific response.

960. At the May 19-20, 1993, JEDEC JC42.3 Committee meeting Gordon Kelley gave a report on the status of the packet of fourteen SDRAM ballots that had been sent to the JEDEC council. Mr. Kelley announced that there was only one no vote, from AT&T, and distributed copies of the SDRAM ballots. (JX0016 at 5). Mr. Crisp informed Rambus management by email from the meeting that the SDRAM standard was likely to be adopted at the next JEDEC council meeting. (CX0700 at 1). Rambus CEO Tate responded by asking Mr. Crisp to brief him and other members of management when Mr. Crisp returned. (CX0711 at 8 ("Sounds like lots of interesting activities - please arrange to debrief me, Allen [Roberts]. Dave [Mooring] when you are back and Mike [Farmwald] if he's interested.")).

Rambus's Response to Finding No. 960:

Rambus has no specific response.

961. At the meeting Mr. Crisp did not make any disclosure of any Rambus patent or patent application that might relate to these SDRAM ballots. (Crisp, Tr. 3160-61). Mr. Crisp did not inform the Committee that the matters under discussion in connection with SDRAM standardization involved inventions that Rambus believed it owned. (CX2092 at 148, 150).

Rambus's Response to Finding No. 961:

The proposed finding is misleading because it suggests that Mr. Crisp had a Rambus patent or patent application to disclose. In fact, Complaint Counsel have stipulated that, prior to the adoption of the JEDEC SDRAM standard, Rambus had no claims in any pending patent application that, if issued, would have necessarily been infringed by the manufacture or use of any device manufactured in accordance with the 1993 JEDEC SDRAM standard. (Parties' First Set of Stipulations, No. 9.) Complaint Counsel has not introduced evidence of any claims that were pending prior to January 1995 that Complaint Counsel assert cover SDRAMs. The proposed finding is also misleading because it suggests that Mr. Crisp should have disclosed some inventions in connection with SDRAM standardization that he believed were owned by Rambus. Even if, contrary to the holding of the Federal Circuit and the weight of the evidence, a JEDEC representative's beliefs could trigger a disclosure obligation, Complaint Counsel did not meet their burden of proving that Richard Crisp held such a belief at any relevant time. (RPF 418-22).

June 1993 - Rambus Patent Activity

962. In June 1993, Fred Ware of Rambus sent an email to various Rambus employees, including Messrs. Farmwald, Roberts and Crisp, reporting on a conversation with Mr. Vincent and the "current status of the additional claims we wanted to file on the original . . . patent." (CX1959; see also CX3130 at 129 (Vincent, Dep.)). Mr. Ware reported that a claim pertaining to "writable configuration register permitting programmable CAS latency" had been "written up and filed" and remarked that the claim was "directed against SDRAMs." (CX1959).

Rambus's Response to Finding No. 962:

The proposed finding is incomplete and misleading. The claim that Mr. Ware identified as "directed against SDRAMs," claim 151 of the '651 application, contained a limitation

requiring that data, address, and control information be "in the form of packets," indicating that the claim clearly was not directed against SDRAMs. (Response to Finding No. 958; RPF 426).

963. Mr. Ware also identified several other patent claims that were being written up or considered by Mr. Vincent but had not yet been filed. These included a claim for "DRAM with PLL clock generation" that was "directed against future SDRAMs," and a claim for "DRAM with multiple open rows" that was "directed against SDRAMs." (CX1959). Mr. Ware also identified claims relating to DRAM, with externally supplied reference voltage and DRAMs using low-voltage-swing signal levels. He described these claims as directed against CTT technology and GTL technology respectively. (CX1959).

Rambus's Response to Finding No. 963:

The proposed finding is incomplete and misleading. First, Mr. Ware's e-mail states that the claim for DRAM with PLL clock generation is directed not only against future SDRAMs, but also against Ramlink. (CX1959). Second, with respect to a claim for DRAM with multiple open rows, Mr. Ware notes that "Lester [Vincent] is doubtful whether we can extract this claim from the teachings of [the '898 application]." (*Id.*). Complaint Counsel have introduced no evidence that a claim going to a DRAM with multiple open rows was ever filed by Rambus.

964. A reply email from Mr. Crisp the same day stated that the claims for low voltage swing signals already had been done. He otherwise confirmed the accuracy of Mr. Ware's report. (CX703; Crisp, Tr. 3156-57, 3163; CX2082 at 772-74 (Crisp, Dep.); CX2092 at 189-93 (Crisp, Infineon Trial Tr.)).

Rambus's Response to Finding No. 964:

The proposed finding mischaracterizes the evidence. The reply e-mail from Mr. Crisp did not "otherwise confirm[] the accuracy of Mr. Ware's report."

965. On June 20, 1993, Mr. Vincent filed an amendment to an existing Rambus patent application seeking to add a claim for externally supplied reference voltage, another topic that had been discussed at JEDEC. (Crisp, Tr. 3164-3171; CX1959; CX1459; CX1961; CX1963 at 4).

Rambus's Response to Finding No. 965:

The proposed finding is not supported by the evidence. In the testimony of Mr. Crisp cited by Complaint Counsel, Mr. Crisp stated only that "Rambus had given some consideration to requesting that our patent lawyer look to see if such claims [involving externally supplied reference voltage] existed or if they didn't if they could have been created and added to our existing applications." (Crisp, Tr. 3164). Complaint Counsel also cite to certain e-mails and notes that are consistent with Mr. Crisp's testimony that Mr. Vincent had been asked to consider claims involving an externally supplied reference voltage, but do not indicate that such claims had been filed. (CX1959, CX1963 at 4). Finally, Complaint Counsel cite to an amendment to the '692 application, as well as a cover letter enclosing that amendment, which Complaint Counsel elsewhere assert added claims relating to on-chip PLL and do not contain claims involving an externally supplied reference voltage. (CX1459; CX1961).

966. On June 28, 1993, Mr. Vincent's firm filed on behalf of Rambus an amendment that cancelled the claims in the pending Rambus patent application 07/847,692 (the '692 application) and inserted new claims. (CX1502 at 208, 212). The new claims contained in this amendment included claims pertaining to the use of on-chip PLL circuitry. (CX1502 at 204, 208 (claim 151); Nusbaum, Tr. 1583-85; Jacob, Tr. 5533-41; CCFF 1103 et seq.).

Rambus's Response to Finding No. 966:

The proposed finding is incomplete and misleading. One of the independent claims added in the amendment to the '692 application does recite a "phase locked loop (PLL)" in one of the limitations, but only together with a number of other limitations. Moreover, although the claim refers to a "PLL," it actually describes a different type of circuit known as a "DLL." (Jacob, Tr. 5634).

967. Two days later, on June 30, 1993, Mr. Vincent sent Mr. Crisp a copy of the

preliminary amendment to the '692 application. (CX1961). On July 9, 1993, Mr. Vincent met with Mr. Crisp and Mr. Ware and discussed, among other topics, claims relating to low voltage swing signals and externally supplied reference voltage. (CX1963 at 3,4; CX3126 at 447-48, 449-52 (Vincent, Dep.)).

Rambus's Response to Finding No. 967:

Rambus has no specific response.

September 1993 - JEDEC Committee Meeting & Disclosure of '703 Patent

968. In September 1993 Richard Crisp was present for Rambus at the JEDEC JC-42.3 Committee meeting in Boston, Massachusetts. (JX0017 at 1; Crisp, Tr. 3171-73). The Chairman Mr. Townsend presented the patent policies and showed the patent tracking list. (JX0017 at 3). Mr. Townsend also showed a draft of portions of the revised 21-I Manual (JX0017 at 12 ("Standards that call for the use of a patented item or process may not be considered by a JEDEC committee unless all of the relevant technical information covered by the patent or pending patent is known to the committee, subcommittee or working group") (emphasis added); *id.* at 14 (regarding discussion of "pending or existing patents" and applicability of patent policy after adoption of a standard); see also CX2092 at 63-64 (Crisp, Infineon Trial Tr.)).

Rambus's Response to Finding No. 968:

The proposed finding is incomplete. The viewgraph of the draft portions of the JEP 21-I manual was expressly marked "DRAFT" and contained a footnote stating that the "material is a proposed revision" that "has not been approved by JEDEC." (JX0017 at 12). The "draft" viewgraph does not contain language requiring intellectual property disclosures by JEDEC members. (*Id.*). Complaint Counsel did not establish that the 21-I manual ever received the EDEC approval that it needed to become effective. (Kelly, Tr. 2105).

969. At the September 1993 Committee meeting there was discussion concerning the discovery by Committee members that Texas Instruments (TI) had a patent covering so-called Quad CAS technology. (JX0017 at 6; Crisp, Tr. 2960-62). Mr. Crisp reported to Rambus CEO Tate and Vice-President Mooring that at the meeting "TI was chastized [sic] for not informing JEDEC that it had a 1987 patent on Quad CAS devices" and reported that the Committee had determined to remove Quad CAS technology from the pertinent JEDEC standard. (CX0711 at 1 ("The bottom line is that all Quad CAS devices will be removed from standard 21C.")). Tempers flared at the meeting, and Mr. Crisp believed that the action was a way that the group sent a

strong message to TI that they did not appreciate what TI had done. (CX2086 at 165, 168 (Crisp, Dep.)).

Rambus's Response to Finding No. 969:

The proposed finding is misleading and incomplete. In fact, the Committee did not decide to remove Quad CAS technology from the JEDEC standards at the September 1993 meeting, but only issued a ballot on that issue and asked TI to respond to the concerns raised by the next meeting. (JX0017 at 7). Mr. Crisp's recollection of the incident is that Micron and TI were in litigation "and that Micron, I believe, brought this issue up in the meeting in an attempt to get the committee to be swayed by their position on this and to support them on taking some sort of action against TI." (Crisp, Micron Depo., at 164). However, once TI gave a RAND letter for its Quad-CAS technology (RX 562 at 13), the debate within JEDEC about TI's patents instantly subsided, the issue was resolved, and the JEDEC committee voted unanimously to remove the hold on the Quad CAS standards and to revoke the ballot to rescind the standard. (JX 25 at 5).

970. About three weeks after the September 1993 Committee meeting, Mr. Crisp requested that Mr. Vincent obtain copies of six TI patents as well as copies of the complaints in pending litigation between TI and Micron in Texas and Idaho. (CX1967; Crisp, Tr. 2963-64; CX1955 at 46; *see also* CX1971 at 1).

Rambus's Response to Finding No. 970:

The proposed finding is incomplete. Mr. Crisp testified that his request for these materials was unrelated to the patent disclosure issue at JEDEC. (Crisp, Tr. 2962). Mr. Crisp explained:

"I remember asking Mr. Vincent for him to tell me about the complaints in the TI

versus Micron case in Marshall, Texas, because I had a business interest in what the products were that were under suit, because I was interested in using that to help me with my marketing with Micron."

(Crisp, Tr. 2964).

971. At the September 1993 meeting of the Committee Mr. Crisp disclosed to the Committee the issuance to Rambus on September 7, 1993, of United States Patent Number 5,243,703. (CX1460; Crisp, Tr. 3173; Stipulation No. 11). The '703 patent was the first Rambus patent and had issued shortly before the meeting. *Id.* The '703 patent resulted from a divisional application of an original application, Serial No. 07/510,898 ('898 application), filed in April 1990. (First Stipulations, No. 11).

Rambus's Response to Finding No. 971:

Rambus has no specific response.

972. The '703 patent asserted claims over a U-shaped or reflected clock technology; neither the claims or the specification of the '703 patent would have alerted an engineer at the time it was issued that Rambus might seek to obtain patent rights over features contained the JEDEC SDRAM standard. (CX1460; Jacob, Tr. 5498-5501). The claims of the '703 patent did not read on anything other than Rambus-compatible devices. (CX2102 at 321 (Karp, Dep.)).

Rambus's Response to Finding No. 972:

The proposed finding is not supported by the weight of the evidence.

The specification and drawings of the '703 patent are substantially the same as the specification and drawings of the '898 specification and drawings. (CCFF 1269). An engineer reviewing that specification would have realized that Rambus could seek claims regarding numerous inventions, including features contained in the JEDEC SDRAM standard. (*See* RPF 689-713, 716). Indeed, the specification of the '703 patent discloses the fact that Rambus was pursuing numerous other divisional applications claiming priority to the '898 application with claims directed at inventions other than the invention claimed in the '703 patent. (RX0425 at 11;

RPF 717).

Complaint Counsel cite Mr. Karp for the proposition that the claims of the '703 patent did not read on anything other than Rambus-compatible devices. Mr. Karp is clearly incorrect: while the claims of the '703 patent are directed at the clocking scheme described in the '898 specification, the claims do not include limitations relating to other features of the preferred embodiment (such as the bus architecture, packetized protocol, etc.). (RX0425 at 24-25). The citation to Mr. Karp is also misleading to the extent that it suggests that Mr. Karp is of the opinion that the '703 patent did not disclose the range of Rambus's potential patent claims. Mr. Karp's testified as follows:

> "Well, let's separate the '703 out into the specification and the claims. In the specification -- the specification is the same as the specification that was in the laid open European application, so it was kind of the master Rambus specification. And so all of the technology that was the subject of their initial inventions was contained in that specification. The claims of the '703, in my opinion, did not read on anything other than potentially Rambus-type devices. But it was clear to me from my experience that if the inventions were there, that they were ultimately going to be claimed. It was clear that there was additional prosecution going on."

973. Mr. Crisp did not provide any information about the subject matter of the '703 patent or how, if at all, it related to JEDEC work. (CX2087 at 248-49 (Crisp, Dep.)). The '703 patent was unrelated to ongoing JEDEC work. (CX2092 at 197-99 (Crisp, Infineon Trial Tr.); CX1801 at 3 ("The '703 patent and the WIPO application did not relate to JEDEC's SDRAM work, but were directed to the implementation of Rambus' RDRAM products.")).

Rambus's Response to Finding No. 973:

The proposed finding that the '703 patent was unrelated to ongoing JEDEC work is misleading and not supported by the evidence. The evidence cited by Complaint Counsel in support of this proposition is referring to the claims of the '703 patent. The specification of the '703 patent is substantially the same as the specification of the '898 application and disclosed all of the inventions that Rambus could claim from that application. (RPF 689-713, 716-17; RRFF 972).

974. At the September 1993 meeting of the Committee, Mr. Crisp did not say anything about any of the pending patent applications of Rambus. (Crisp, Tr. 3174). Mr. Crisp did not inform the Committee that the matters under discussion in connection with SDRAM standardization involved inventions that Rambus believed it owned. (CX2092 at 148, 150).

Rambus's Response to Finding No. 974:

The proposed finding is misleading because the existence of some of Rambus's pending patent applications were disclosed in the '703 patent itself, which was disclosed by Mr. Crisp. (RX0425 at 11).

The proposed finding is also misleading because it suggests that Mr. Crisp should have disclosed some inventions in connection with SDRAM standardization that he believed were owned by Rambus. Even if, contrary to the holding of the Federal Circuit and the weight of the evidence, a JEDEC representative's beliefs could trigger a disclosure obligation, Complaint Counsel did not meet their burden of proving that Richard Crisp held such a belief at this time. (RPF 418-22).

975. David Mooring, who was Mr. Crisp's supervisor at the time, gave Mr. Crisp the impression that he was "annoyed" when he learned about the disclosure of the '703 patent at JEDEC. (Crisp, Tr. 3174-75; CX2054 at 189-90 (Mooring, Dep.)). In an email two years later, Mr. Crisp recalled that he had been "castigated" for disclosing the '703 patent to JEDEC.

(CX0837 at 2; Crisp, Tr. 3175 ("chastised")).

Rambus's Response to Finding No. 975:

The proposed finding is incomplete and misleading. As Mr. Mooring made clear, he was annoyed not about the disclosure itself but about the fact that Mr. Crisp had not consulted with him prior to disclosing the '703 patent. (CX2054, Mooring Infineon Depo., at 189-90). As JEDEC Secretary Ken McGhee observed some seven years later, "[d]isclosure of patents is a very big issue for Committee members. . . ." (RX 1582 at 1).

976. Except for the '703 patent, Mr. Crisp did not disclose any Rambus patent applications or patents to JEDEC during the time he was a member. (Crisp, Tr. 3316, 3176).

Rambus's Response to Finding No. 976:

The proposed finding is misleading because the existence of some of Rambus's pending patent applications were disclosed in the '703 patent itself. (RX0425 at 11).

November 1993 - JEDEC publishes SDRAM standard

977. JEDEC published its standard for SDRAM as part of Release 4 of JEDEC Standard 21-C in November 1993. (First Stipulations, No. 19). Since 1993, JEDEC has published several revisions of the JEDEC standard governing SDRAMs, JEDEC Standard 21-C. (First Stipulations, No. 20).

Rambus's Response to Finding No. 977:

Rambus has no specific response.

December 1993 - JEDEC Committee Meeting

978. In December 1993 Richard Crisp was present for Rambus at the JEDEC JC-42.3 Committee meeting in San Diego, California. (JX0018 at 1). The Chairman Mr. Townsend presented the patent policies and the patent tracking list was updated. (JX0018 at 3, 15-18).

Rambus's Response to Finding No. 978:

Rambus has no specific response.

979. At the December 1993 Committee meeting, the Committee considered and voted to adopt a ballot to rescind previously-approved portions of JEDEC standards pertaining to Quad CAS, in light of the patent issues that had been discussed at the September 1993 Committee meeting. (JX0018 at 7; G. Kelley, Tr. 2467-69). The Committee, after discussion, voted to send the ballot to rescind the previously-approved portions of the standards to the JEDEC Council. (JX0018 at 9).

Rambus's Response to Finding No. 979:

The proposed finding is misleading and incomplete. Once TI gave a RAND letter for its Quad-CAS technology (RX 562 at 13), the debate within JEDEC about TI's patents instantly subsided, the issue was resolved, and the JEDEC committee voted unanimously to remove the hold on the Quad CAS-related standards and to revoke the ballot to rescind those standards. (JX 25 at 5; Kellogg, Tr. 5220-26).

980. At the December 1993 Committee meeting Mr. Crisp did not make any disclosure to the Committee concerning any Rambus patent or patent application. (Crisp, Tr. 3316). Mr. Crisp did not inform the Committee that the matters under discussion in connection with SDRAM standardization involved inventions that Rambus believed it owned. (CX2092 at 148, 150).

Rambus's Response to Finding No. 980:

The proposed finding is misleading because it suggests that Mr. Crisp had a Rambus patent or patent application to disclose. In fact, Complaint Counsel have stipulated that, prior to the adoption of the JEDEC SDRAM standard, Rambus had no claims in any pending patent application that, if issued, would have necessarily been infringed by the manufacture or use of any device manufactured in accordance with the 1993 JEDEC SDRAM standard. (Parties' First Set of Stipulations, No. 9.) Complaint Counsel have not introduced evidence of any claims that were pending prior to January 1995 that, Complaint Counsel assert, cover SDRAMs. The proposed finding is also misleading because it suggests that Mr. Crisp should have disclosed

some inventions in connection with SDRAM standardization that he believed were owned by Rambus. Even if, contrary to the holding of the Federal Circuit and the weight of the evidence, a JEDEC representative's beliefs could trigger a disclosure obligation, Complaint Counsel did not meet their burden of proving that Richard Crisp held such a belief at this time. (RPF 418-22).

January 1994 - Consultation With Rambus Patent Counsel

981. On January 10, 1994, Mr. Vincent met with Rambus CEO Tate, CFO Gary Harmon and Vice-President Roberts to discuss enforcement of Rambus patents against synchronous DRAM, with particular reference to low voltage swing, configurable mode register (including programmable CAS latency) and on-chip PLLs. (CX1970 at 1 ("Enforcement: Sink DRAM, . . . low swing signals . . . config registers . . . programmable latency . . . PLLs"); CX3126 at 461-62, 463-65 (Vincent, Dep.)). Mr. Vincent noted that there were five Fred Ware applications, and he needed to file all five. (CX1970 at 2).

Rambus's Response to Finding No. 981:

The proposed finding is not supported by the weight of the evidence. Rambus had no issued patents on January 10, 1994 other than the '703 patent. The claims of the '703 patent did not, as Complaint Counsel acknowledge, cover SDRAMs. (Parties First Set of Stipulations, Exh. A; CCFF 972). Indeed, the only Rambus patent that issued prior to June 1996 that Complaint Counsel assert covered any JEDEC-compliant, the '327 patent, is alleged to read on DDR SDRAMs, not SDRAMs. (CCFF 1632, 1635). DDR SDRAM standard setting work did not begin until late 1996. (RPF 399-413).

The SDRAM standard does not include an on-chip PLL, and the first JEDEC presentation relating to PLLs on SDRAMs that Complaint Counsel raise is a September 1994 NEC presentation. (CCFF 604). The SDRAM standard did not include any form of low voltage swing signaling. (RRFF 564). Whatever the stray notes from Mr. Vincent that Complaint Counsel cite mean, they cannot plausibly be interpreted, as the proposed finding suggests, as referring to the

enforcement against SDRAMs of non-existent patents over features that are not in SDRAMs.

The proposed finding also misrepresents the evidence. The evidence cited refers to "config registers," not "configurable mode register[s]." (CX1970 at 1). The evidence cited refers to "programmable latency," not "programmable CAS latency." (*Id*.) The proposed finding takes general terms used in the notes and replaces them with terms specific to SDRAMs to make it appear that SDRAMs were being discussed in a way not supported by the evidence.

Finally, the proposed finding regarding "Fred Ware applications" is irrelevant. It is true that Mr. Ware was an inventor on numerous Rambus patent applications, many filed after the date of Mr. Vincent's notes. (See CX 1984 (Rambus patent status report) at 25, 28, 31, 32, 37-42, 46). These patents do not claim priority to the '898 application, and there was no trial testimony about them in this case.

February 1994 - Rambus Renews Its JEDEC Membership

982. In February 1994 Rambus renewed its JEDEC membership for the 1994 calendar year, increasing its dues to reflect participation in an additional JEDEC committee. (CX0602 at 7; Stipulation, Tr. 3176; Crisp, Tr. 3176).

Rambus's Response to Finding No. 982:

The proposed finding that Rambus joined an additional JEDEC committee is not supported by the weight of the evidence. Complaint Counsel base this finding on Mr. Crisp's speculation at trial and the fact that Rambus's dues of $4,000 were crossed out on the invoice and $5,000 written in. (CX0602 at 7; Crisp, Tr. 3177-78). However, the evidence suggests that this reflected nothing more than an increase in the dues. The invoice indicates that Rambus was to be a member of the JC-15, JC-16, and various subcommittees of JC-42. Rambus was already a member of these three committees in 1993. (CX0602 at 5). JEDEC's 1992 price list shows that

the maximum dues were $4,000 for joining more than two committees. (CX0602 at 2). It is likely that this figure was raised to $5,000 in 1994.

March 1994 - JEDEC Committee Meeting

983. In March 1994 Richard Crisp was present for Rambus at the JEDEC JC-42.3 Committee meeting in Orlando, Florida. (JX0019 at 1). The Chairman Mr. Townsend presented the patent policies and showed the patent tracking list. (JX0019 at 4).

Rambus's Response to Finding No. 983:

Rambus has no specific response.

984. Among the patent issues discussed at the March 1994 Committee meeting was the disclosure by Philips of two patents, and its statement of willingness to license on reasonable and non-discriminatory terms. (JX0019 at 25). Micron and TI also disclosed several patents at the meeting. (CX0711 at 16-17).

Rambus's Response to Finding No. 984:

The proposed finding is misleading and incomplete. Philips disclosed a single United States patent and its Taiwanese counterpart. (JX0019 at 25). Micron did not disclose any of its own patents, but disclosed several TI patents. (CX0711 at 16). There is no evidence that any patent applications were disclosed.

985. At the March 1994 Committee meeting there was extensive discussion among Committee members concerning the continuing Quad CAS controversy and the patent disclosure policy. (JX0019 at 4-5). Mr. Crisp reported to his Rambus colleagues that "the meeting opened with a lot of controversy regarding patents" having to do with the ongoing lawsuit in which TI and Micron were "embroiled." (CX0711 at 16). Mr. Crisp reported to his colleagues that TI sought to have the Committee interpret the disclosure duty as "limited" to two scenarios. (*Id.*) He also reported Micron's statement that the JEDEC patent policy existed "due to anti-trust concerns" so that companies could not keep out competition. (*Id.*) Mr. Crisp reported that discussion on this and other related topics "got pretty nasty and was finally squelched" by the Chairman who asked successfully for a motion to cut off discussion. (*Id.*). At the close of the discussion on this topic, those present in the room were asked to indicate by hand vote whether there was any confusion on the basic patent policy – the need and obligation to disclose patent activity. By unanimous vote, the Committee confirmed that the patent policy was clear. (Kellogg, Tr. 5028-30; JX0019 at 4-5 ("The Committee was asked if the policy is clear. The

Committee felt it was clear.")).

Rambus's Response to Finding No. 985:

The proposed finding omits several relevant passages from Mr. Crisp's e-mail about the meeting. (CX 711 at 16). First, the "antitrust concerns" that Micron reportedly expressed related to the availability of patent licenses and a concern that companies might "agree amongst themselves" not to license other companies "that they do not want to compete with." (*Id.*) Second, *both* of the "two scenarios" referenced by the proposed finding refer to disclosure of "patents"; neither refers to patent applications. (*Id.*)

As Mr. Crisp's e-mail suggests, and as confirmed by other contemporaneous documents, the "Quad Cas controversy" involved the disclosure of issued patents, not the disclosure of patent applications or of a member's "beliefs" or "intentions".

986. Despite the various discussions pertaining to patent disclosure at the March 1994 Committee meeting, Mr. Crisp did not make any disclosure to the Committee concerning any Rambus patent or patent application. (Crisp, Tr. 3316). Mr. Crisp did not inform the Committee that the matters under discussion in connection with SDRAM standardization involved inventions that Rambus believed it owned. (CX2092 at 148, 150).

Rambus's Response to Finding No. 986:

The proposed finding is misleading because it suggests that Mr. Crisp had a Rambus patent or patent application to disclose. In fact, Complaint Counsel have stipulated that, prior to the adoption of the JEDEC SDRAM standard, Rambus had no claims in any pending patent application that, if issued, would have necessarily been infringed by the manufacture or use of any device manufactured in accordance with the 1993 JEDEC SDRAM standard. (Parties' First Set of Stipulations, No. 9.) Complaint Counsel have not introduced evidence of any claims that were pending prior to January 1995 that Complaint Counsel assert cover SDRAMs.

The proposed finding is also misleading because it suggests that Mr. Crisp should have disclosed some inventions in connection with SDRAM standardization that he believed were owned by Rambus. Even if, contrary to the holding of the Federal Circuit, and the weight of the evidence, a JEDEC representative's beliefs could trigger a disclosure obligation, Complaint Counsel did not meet their burden of proving that Richard Crisp held such a belief at this time. (RPF 418-22).

March-May 1994 - More Rambus Patent Strategy

987. On March 15, 1994, Rambus Vice President David Mooring proposed to CEO Geoff Tate, Vice-President Allen Roberts and CFO Gary Harmon that Rambus "kick-off another patenting spree." (CX0726). Mr. Mooring noted that Rambus still had "a window of opportunity left while we still have confidential information." (*Id.*) He suggested that it would help the Rambus scenario against competitive memories such as RamLink and SyncLink if they had patents that would be infringed by memory controllers produced by companies such as ATI. (*Id.*)

Rambus's Response to Finding No. 987:

The proposed finding is irrelevant. Mr. Mooring refers to scouring certain listed "confidential but detailed information" for "patentable fundamental stuff." (CX0726). Thus the patents that Mr. Mooring was hoping to apply for would have been new patents, not additional patents based on the '898 application (which was not listed, and had not been confidential since the publication of the PCT application in October 1992 (CX1454 at 1)). Complaint Counsel have introduced no testimony about patents outside the '898 family; the potential patent applications mentioned in Mr. Mooring's e-mail are unrelated to this case

988. On April 29, 1994, Rambus Vice-President Roberts requested a meeting with Rambus employees Fred Ware, Rick Barth and John Dillon to discuss "what new claims for our existing patents we dream up which might block MOST." (CX0730). One idea that Mr. Roberts proposed was "clocking data on moth edges of the clock on a DRAM."). (*Id.*).

Rambus's Response to Finding No. 988:

The proposed finding is incomplete. The history of Rambus's patent claims against MOST, also known as Mosys, underscores two important points: 1) that Rambus did not indulge in detailed infringement analysis until a patent that was arguably infringed had actually issued, because until then it is not clear what claims will issue, and 2) that Rambus did not bring accusations of infringement until there was an actual infringing product that could be analyzed to make sure that it met all the limitations of the patent claims.

Lester Vincent was asked by Rambus to look into the question of whether Mosys products infringed the '327 patent only after the '327 patent had issued on April 30, 1996. (CX 3129, Vincent Micron depo. at 380-82.) In order to perform this analysis, Mr. Vincent was sent an actual Mosys DRAM, as well as a Mosys data sheet. (*Id*. at 397-99.)

Rambus did not form a conclusion about infringement of the '327 patent by Mosys DRAMs until the Mosys DRAM had been reverse-engineered and the infringement analysis completed. (Diepenbrock, Tr. 6209.) Mosys was contacted about possible infringement only after the reverse engineering was done. (Diepenbrock, Tr, 6205-06.)

989. In May 1994, Allen Roberts, Rambus Vice-President of Engineering, sent a letter to Rambus patent counsel Lester Vincent further discussing enhancements to the coverage of the original Rambus patent application and identifying various ideas to be pursued as claims in the various pending patent applications or in newly filed applications. The letter stated that "it is possible that some of these enhancements are already in the existing applications, but we would like to re-assess the strength of those claims." (CX0734).

Rambus's Response to Finding No. 989:

The proposed finding is misleading to the extent that it suggests that patent claims in all the areas listed in Mr. Roberts' letter were filed by Rambus. The letter asks Mr. Vincent to

"consider" the areas identified. (CX0734).

990. Among the enhancements described in the May 1994 letter were "[m]ultiple and independently controlled and addressed DRAM memory regions (banks)." (CX0734). Two bank design had previously been discussed on multiple occasions at JEDEC. (Crisp, Tr. 3180).

Rambus's Response to Finding No. 990:

The proposed finding is irrelevant. There is no evidence that Rambus ever filed or obtained claims to two bank design. (RRFF 549).

991. Among the enhancements described in the May 1994 letter was "[u]se [of] control registers to contain values which control RAS or CAS access timing." (CX0734 at 2). Use of control registers to enable programmable CAS latency had previously been discussed on multiple occasions at JEDEC. (Crisp, Tr. 3181-82).

Rambus's Response to Finding No. 991:

Rambus has no specific response.

992. Among the enhancements described in the May 1994 letter was "[u]se of both edges of the clock for transmission of address, commands or data (or any combination) on DRAM device to increase effective bandwidth/pin." (CX0734 at 1).

Rambus's Response to Finding No. 992:

Rambus has no specific response.

993. In July 1994 Mr. Roberts apparently informed Rambus CEO Tate that { } (CX1715 at 56 (*in camera*) ("{ })).

Rambus's Response to Finding No. 993:

The proposed finding is not supported by the evidence. {

}

May 1994 - Clarification of JEDEC Patent Policy

994. In May 1994, the secretary of the JEDEC Council distributed to all members of JC-42 Committees copies of a memorandum prepared by John Kelly, the JEDEC legal counsel. (CX0355 at 1). The memorandum had been prepared by Mr. Kelly in response to a white paper that had been submitted to the JEDEC council in March 1994 by TI in connection with the ongoing dispute concerning Quad CAS technology arising from the work of the JEDEC JC42.3 Committee. (J. Kelly, Tr. 1940-41; CX0353 at 2-5).

Rambus's Response to Finding No. 994:

Rambus has no specific response, except to note that Mr. Kelley's title was EIA General Counsel.

995. In the memorandum, Mr. Kelly, who was responsible for interpreting JEDEC rules (J. Kelly, Tr. 1821-22), clarified the JEDEC patent policy and rejected an interpretation that had been argued by TI in its white paper submitted to the JEDEC Council. (J. Kelly, Tr. 1942-47). In the memorandum, Mr. Kelly made clear that under the JEDEC patent disclosure policy written assurances with respect to patent licensing must be provided by a patent holder where a standard under consideration "may require" the use of a patented invention. (CX0355 at 2). The memorandum contradicted the position of TI, which was that no assurances were required unless it was absolutely clear that use of the patent was required to comply with the standard. (J. Kelly, Tr. 1943-44). Consistent with longstanding practice, the use of the term "patented" in the memo referred to either patents or patent applications. (J. Kelly, Tr. 1945-46).

Rambus's Response to Finding No. 995:

This finding improperly inserts the word "disclosure" into its description of Mr. Kelly's memorandum. The memorandum does not mention either the word or the subject matter. (CX 355 at 2). Instead, the question presented involved the circumstances under which the 42.3 committee could request "RAND" assurances from a patent holder. (*Id.*)

It is also important to note that Mr. Kelly circulated not just his one-page memorandum, but *also* circulated (or caused Mr. McGhee to circulate), a copy of the ANSI Patent Policy Guidelines. (CX 355 at 1, 3-9). Kelly caused these guidelines to be circulated to all JC 42.3

members because he "thought they provided insight into the proper interpretation of the EIA and JEDEC patent policy." (Kelly, Tr. 1950). It is undisputed that the ANSI Patent Policy encourages, but does not require, disclosure of intellectual property interests by members of standards-setting organizations. (Kelly, Tr. 1961). It is also undisputed that at the time Mr. Kelly caused the ANSI Patent Policy Guidelines to be circulated to all JC 42.3 members, he:

(1) understood that the ANSI Patent Policy did not require the disclosure of patent applications (Kelly, Tr. 2075);

(2) knew that the ANSI Guidelines that he was circulating were one basis for his own understanding that the ANSI Patent Policy did not require the disclosure of patent applications (Kelly, Tr. 2077);

(3) knew that the language of the EIA patent policy and the ANSI Patent Policy was essentially identical (Kelly, Tr. 2077-78); and

(4) said nothing to the JC 42.3 members who would be receiving the ANSI Patent Policy Guidelines to suggest that the EIA or JEDEC, unlike ANSI, supposedly required disclosure of patent applications. (CX 355 at 1-2).

May 1994 - JEDEC Committee Meeting

996. In May 1994 Richard Crisp was present for Rambus at the JEDEC JC-42.3 Committee meeting in New York City. (JX0020 at 1; Crisp, Tr. 3188). The Chairman Mr. Townsend presented the patent policies and showed the patent tracking list. (JX0020 at 4, 15-18).

Rambus's Response to Finding No. 996:

Rambus has no specific response.

997. During the course of the May 1994 meeting Mr. Crisp prepared a lengthy email to colleagues at Rambus reporting and commenting on the discussions occurring at the meeting.

(Crisp, Tr. 3193-94; CX711 at 26-30). In the text of the email, Mr. Crisp noted that one of the topics addressed in the discussions was the use of externally-supplied reference voltage in later-generation SDRAM design. (CX711 at 27, 31). His comments (including one directed to Rambus Vice-President Allen Roberts) made reference to this technology as one that Rambus had been pursuing through patent filings by Rambus patent attorney at its request. *(Id.*; see also Crisp, Tr. 3193-94). Mr. Crisp commented that "we may be able to slow down or stop (or at least collect from) [devices embodying the technology] if the claim is allowed.." (CX711 at 31).

Rambus's Response to Finding No. 997:

The proposed finding is irrelevant. Complaint Counsel have made no showing that Rambus had any claims relating to an externally supplied reference voltage that should have been disclosed. (RRFF 555, 564).

998. In fact, the topic of external reference voltage had been discussed by the Committee and noted by Rambus representative Billy Garrett as early as February 1992. (CX672 at 1; Crisp, Tr. 3042-44). In February 1993 Richard Crisp had sent an email to other Rambus executives discussing pursuit of a patent claim relating to external reference voltage. (CX691; Crisp, Tr. 3123-24).

Rambus's Response to Finding No. 998:

The proposed finding is irrelevant. Complaint Counsel have made no showing that Rambus had any claims relating to an externally supplied reference voltage that should have been disclosed. (RRFF 555, 564).

999. Mr. Crisp did not inform the Committee that he had worked on a patent claim relating to externally supplied reference voltage, or that Rambus might be able to slow down or stop or at least collect royalties from various devices relating to externally supplied reference voltage if the claim was allowed. (Crisp, Tr. 3194). Mr. Crisp did not inform the Committee that the matters under discussion in connection with SDRAM standardization involved inventions that Rambus believed it owned. (CX2092 at 148, 150).

Rambus's Response to Finding No. 999:

The proposed finding is irrelevant. Complaint Counsel have made no showing that Rambus had any claims relating to an externally supplied reference voltage that should have been

disclosed. (RRFF 555, 564). Moreover, even if, contrary to the holding of the Federal Circuit and the weight of the evidence, a JEDEC representative's beliefs could trigger a disclosure obligation, Complaint Counsel did not meet their burden of proving that Richard Crisp held such a belief with respect to an externally supplied reference voltage. Mr. Crisp's e-mail states only that the "we need to check claims." (CX0711 at 31). As noted above, there is no evidence that Rambus had such claims pending; a "check" by Mr. Crisp would have turned up nothing.

June 1994 - Internal Rambus Communication

1000. On June 16, 1994, John Dillon, the head of the architecture group inside Rambus and Rambus representative at the JEDEC JC 15 Committee (CX0602 at 5), sent an email to various other Rambus executives, including CEO Geoffrey Tate, Vice-President David Mooring, Vice-President Allen Roberts and Fred Ware. (CX0738; Crisp, Tr. 3185-86). The email was entitled "an overlooked patent claim?" and discussed the "auto-precharge feature." (CX0738).

Rambus's Response to Finding No. 1000:

The proposed finding is irrelevant. Complaint Counsel have made no showing that Rambus had any claims relating to an auto-precharge feature that should have been disclosed. (RRFF 552, 564).

1001. The auto-precharge feature had previously been discussed at JEDEC on at least two occasions in 1992 in connection with the SDRAM standard. (CX1708 at 5; CX0680 at 2; Crisp, Tr. 3183-85). Auto-precharge had been incorporated as a feature in the JEDEC SDRAM 21-C standard, issued in November 1993. (JX0056 at 115).

Rambus's Response to Finding No. 1001:

The proposed finding is irrelevant. Complaint Counsel have made no showing that Rambus had any claims relating to an auto-precharge feature that should have been disclosed. (RRFF 552, 564).

1002. The June 1994 email by Mr. Dillon stated that Rambus "may be able to make a . . .

claim on auto precharge for *any* DRAM and therefore gain leverage over SDRAM" and certain DRAMs produced by the firm Mosys. (CX0738). Mr. Dillon stated that the feature was not fundamental to the performance of SDRAM, but said that "patenting this feature would have high harassment value, especially to the extent that third-party SDRAM controllers depend on it." *Id*.

Rambus's Response to Finding No. 1002:

The proposed finding is irrelevant. Complaint Counsel have made no showing that Rambus had any claims relating to an auto-precharge feature that should have been disclosed. (RRFF 552, 564).

1003. The following day, CEO Geoff Tate sent an e-mail to Vice President Roberts on the subject at "sdram and most patent claims." (CX0740). Mr. Tate wrote "this stuff is real critical," and requested "a list of which claims we are making that read directly on current/planned sdrams" so that he could track progress from Mr. Vincent's periodic status reports. (*Id.*)

Rambus's Response to Finding No. 1003:

The proposed finding is misleading to the extent that it suggests that Rambus had undisclosed pending claims that would "read directly" on SDRAMs in June 1994. To the contrary, Rambus did not file any such claims while it was a member of JEDEC (RPF 361-70), and even Complaint Counsel do not allege that Rambus had filed such claims prior to January 1995.

August-September 1994 - Communication and Action by Patent Counsel

1004. On August 1, 1994, an attorney with the firm of Lester Vincent, the Rambus patent counsel, transmitted to Rambus Vice-President Allen Roberts a draft preliminary amendment to a pending Rambus patent application that included claims pertaining to dual-edge clock technology. (CX0746 at 2; id. at 4-5 (claim 151, referring to information transmission "in response to a rising edge of the clock signal and a falling edge of the clock signal.")).

Rambus's Response to Finding No. 1004:

The proposed finding is misleading. The draft claim did not pertain to any type of "dual edge clocking technology," but only to devices that would meet each and every limitation in the claim. (CX 746 at 2-5).

1005. The draft application also contained claims relating to multibank design (CX0746 at 9-10 (claim 167, referring to an array of memory cells that is "subdivided into a plurality of memory sections, each of the memory sections being assigned a portion of the range of addresses")) and to auto-precharge (CX0746 at 10 (claim 171, a dependent claim of claim 167 also referring to sense amps "for selectively pre charging the columns of the first `memory section")).

Rambus's Response to Finding No. 1005:

The proposed finding is irrelevant. Claim 167 in the draft amendment is similar in pertinent respects to claim 182 filed in the '646 application and is irrelevant to the issues in this case, as set forth in RRFF 549.

1006. A handwritten note attached to this letter and attachment in Rambus files signed by "Allen" sought comments from others at Rambus and noted that "this is Lester's attempt to work the claims for the MOST/SDRAM defense." (CX0746 at 1).

Rambus's Response to Finding No. 1006:

Rambus has no specific response.

1007. On August 31, 1994, Rambus employee Fred Ware responded to Allen Roberts, with copies to John Dillon and Rick Barth of Rambus, stating that the biggest omission in the claims was the lack of a normal access or a page mode access with auto-precharge. (CX0755). He added that the issue "may need some quick attention, since it's a fairly important concept."). (*Id.*).

Rambus's Response to Finding No. 1007:

The proposed finding is irrelevant. Complaint Counsel have made no showing that Rambus had any claims relating to an auto-precharge feature that should have been disclosed.

(RRFF 552, 564). Moreover, Complaint Counsel have made no showing that a "normal access or a page mode access with auto-precharge" is relevant to SDRAM.

1008. On September 6, 1994, Mr. Vincent's firm filed on behalf of Rambus an amendment to the pending Rambus patent application 08/222,646 (the '646 application); this application later resulted in the issuance of the Rambus '327 patent. (CX1493 at 1, 183). The new claims contained in the September 1994 amendment included a claim pertaining to a dual-edge clocking feature for use in DRAMs. (CX1493 at 183-201; Nusbaum, Tr. 1595-1603; Jacob, Tr. 5549-50; see CX1244 at 1).

Rambus's Response to Finding No. 1008:

The proposed finding is misleading. While the September 1994 amendment included a claim pertaining to a particular type of dual edge clocking, it did not cover SDRAMs or DDR SDRAMs. (*See* RRFF 1199-1215).

September 1994 Committee Meeting - Presentation on PLL/DLL

1009. In September1994 Richard Crisp was present for Rambus at the JEDEC JC-42.3 Committee meeting in Albuquerque, New Mexico. (JX0021 at 1; Crisp, Tr. 3199). The Chairman Mr. Townsend presented the patent policies and showed the patent tracking list. (JX0021 at 4, 14-18).

Rambus's Response to Finding No. 1009:

Rambus has no specifice response.

1010. During the course of the September 1994 Committee meeting Mr. Crisp observed a presentation by NEC pertaining to a proposal for the use of an on-chip PLL circuit in future-generation SDRAM technology. (JX0021 at 91; Crisp, Tr. 3200-01). The proposal contrasted the potential use of PLL circuitry versus not using on-chip PLL circuitry. (JX0021 at 91; G. Kelley, Tr. 2570; Rhoden, Tr. 466; *see also* CX0711 at 36).

Rambus's Response to Finding No. 1010:

The proposed finding is incorrect and incomplete. The September 14, 1994 NEC presentation was not for "the use of an on-chip PLL" but rather for a "PLL enable mode"

according to which a PLL on an SDRAM chip could be enabled or disabled depending on a bit in the mode register. (JX0021 at 87, 91-92.) The NEC presentation did not relate to "future-generation SDRAM technology," but rather to the current generation of 16 Megabit SDRAMs. (JX0021 at 87). The NEC presentation did not propose that the standard incorporate this PLL enable mode, but only that it be available as an "option." (JX0021 at 87.) The NEC presentation was a "first showing" (JX0021 at 11), which never proceeded to a second showing or to balloting.

1011. In September 1994, the pending Rambus '692 patent application contained claims that a reasonable engineer would believe covered the on-chip PLL circuitry shown in NEC's proposal. (CCFF 1183 et seq.).

Rambus's Response to Finding No. 1011:

The proposed finding is not supported by the weight of the evidence. (See RRFF 1186-95).

1012. Mr. Crisp immediately informed executive group and marketing group colleagues at Rambus, including CEO Tate, Vice-President Roberts and Vice-President Mooring. (CX711 at 36; Crisp, Tr. 3201-02). The subject line of Mr. Crisp's email read "NEC PROPOSES PLL ON SDRAM!!!" (CX0711 at 36 (emphasis in original)).

Rambus's Response to Finding No. 1012:

Rambus has no specific response.

1013. In the email Mr. Crisp reported the NEC presentation and stated that "they plan on putting a PLL on board their SDRAMs." (CX0711 at 36). In the email, Mr. Crisp said that "we need to think about our position on this for potential discussion with NEC regarding patent issues." He concluded by stating: "**** I believe we have now seen that others are seriously planning inclusion of PLLs on board SDRAMs," and asking, "what is the exact status of the patent with the PLL claim?****" (CX0711 at 36, 37 (emphasis in original)).

Rambus's Response to Finding No. 1013:

Rambus has no specific response.

1014. Also on September 14, 1994, Vice-President Roberts replied to Mr. Crisp's e-mail. Although most of his e-mail apparently has been lost or destroyed, a portion remains as embedded text in an e-mail sent by Mr. Crisp. (CX0757 at 1; Crisp, Tr. 3208-11). Mr. Roberts apparently contemplated that Rambus might have to litigate to enforce patent claims covering PLL on a DRAM (CX0757 at 1("so if we want to fight this one (after the claim is issued), we better stock up our legal warchest.")).

Rambus's Response to Finding No. 1014:

Rambus has no specific response.

1015. Still on September 14, 1994, Mr. Crisp replied to Mr. Roberts and the rest of the Rambus executive group. He agreed that litigation appeared likely not only regarding "PLL on a DRAM" and "PLL/DLL circuit implementations," but also with respect to other areas such as "programmable access latencies." (CX0757 at 1 ("It seems likely we will have to fight litigation at some point in the future.")). Mr. Crisp recognized that could involve JEDEC members. (Crisp, Tr. 3215 ("Q: .... Litigation might involve some of the other companies sitting in the very JEDEC room that day, wouldn't it? A: That's certainly a possibility.")). Mr. Crisp concluded by suggesting to the Rambus executive group that, if Rambus could get NEC to agree to a deal to "belly up some dollars," then Rambus could disclose the existence of its pending '651 patent application at JEDEC. (CX0757 at 1 ("I think if we can get them to agree to such a deal that the patent issue could be brought up in JEDEC ...")).

Rambus's Response to Finding No. 1015:

The proposed finding is incomplete. Mr. Crisp explained in his e-mail that he believed that litigation appeared likely "at some point in the future," because, while Rambus "anticipated the need to use advanced technniques to attain high clock rates and solved the problem before anyone else felt there was a need," Mr. Crisp "expect[ed] that we will be hit from a lot of copycats in one aspect or another." (CX0757 at 1).

The proposed finding is also misleading and incorrect in part. Mr. Crisp did not "suggest[]" entering into licensing negotiations with NEC, but was simply tossing out an idea for discussion. (CX0757 at 1 ("I wonder if . . . .")). Moreover, there is no support whatsover for the proposed finding tht Mr. Crisp's idea involved potentially disclosing the existence of the '651

patent application at JEDEC. In fact, the existence of the '651 application had been disclosed to JEDEC *a year earlier* – the '651 application is listed as the ninth "related application" in the '703 patent which had been disclosed to JEDEC in September 1993. (RX0425 at 11; CCFF 971). To the extent that Complaint Counsel intended to refer to a disclosure not of the existence of the '651 application, but of its *claims*, no such inference can be drawn from Mr. Crisp's e-mail. Mr. Crisp states only that "the patent issue could be brought up at JEDEC," which does not relate to the claims of any specific application. Moreover, the claims of the '651 application are not related to JEDEC work. (CCFF 958).

1016. In the 1994 time frame, Mr. Mooring believed that putting a PLL on a DRAM was an invention of Rambus. (CX2098 at 397-98 (Mooring, Micron Dep.)). Gary Harmon, Rambus CFO, also testified that "I believe that we have or felt we had a patent on using PLLs on a DRAM" at the time. (CX2070 at 138-39 (Harmon, Micron Dep.)).

Rambus's Response to Finding No. 1016:

The proposed finding is irrelevant. The evidence shows that, even if there was an obligation at JEDEC to disclose intellectual property under certain circumstances, the obligation was triggered only by the actual knowledge of the JEDEC representative. (RPF 288-95). The beliefs of other Rambus personnel are not relevant. (*Id.*)

In addition, the proposed finding about "putting a PLL on a DRAM" is vague and misleading since this can be done in various ways. Rambus did have a filed claim in 1994 (in the '692 application) that involved putting a PLL on a DRAM, but with various limitations that were not met, for example, by the PLL on a DRAM shown in the September 1994 NEC presentation. (*See* RRFF 1186-95).

Mr. Harmon's testimony is not probative. Mr. Harmon explained that he was simply

speculating and does not "know the specifics of our patents." (CX2070 at 138-39, Harmon, Micron Depo., at 138-39).

1017. Mr. Crisp never informed the Committee concerning his discussions with Rambus patent counsel or disclosed whether Rambus had a patent application on file pertaining to the use of on-chip PLL circuitry. (Crisp, Tr. 3207-08, 3451-52). At the September 1994 Committee meeting Mr. Crisp did not make any disclosure to the Committee concerning any Rambus patent or patent application. (Crisp, Tr. 3316). Mr. Crisp did not inform the Committee that the matters under discussion in connection with SDRAM standardization involved inventions that Rambus believed it owned. (CX2092 at 148, 150).

Rambus's Response to Finding No. 1017:

The proposed finding is misleading because it suggests that Mr. Crisp had a Rambus patent or patent application to disclose. In fact, Rambus had no patents or patent applications in during the time that it was a member of JEDEC that would cover the September 1994 NEC presentation. (See RRFF 1186-95).

The proposed finding is also misleading because it suggests that Mr. Crisp should have disclosed some belief regarding inventions that were owned by Rambus. Even if, contrary to the holding of the Federal Circuit and the weight of the evidence, a JEDEC representative's beliefs could trigger a disclosure obligation, Complaint Counsel did not meet their burden of proving that Richard Crisp held a belief that Rambus had pending claims that covered the NEC presentation. Mr. Crisp's e-mail regarding the NEC presentation asked "[w]hat is the exact status of the patent with the PLL claim?" No witness testified that when a JEDEC representative has a *question* in his own mind about whether or not his company might have relevant claims in a pending application, the representative must reveal to the committee that he has a *question*. (*See* Rhoden, Tr. 624-5) (Mr. Rhoden had no opinion about whether a representative with "a question" about possible patent coverage had to disclose, and he testified that there is no

obligation to ask your company's patent counsel about "what was in the patent process".). Moreover, if Mr. Crisp had checked on the status of the '692 patent application, he would have discovered that it did not contain claims covering the NEC presentation. (*See* RRFF 1186-95).

The proposed finding is also irrelevant because JEDEC members were aware of Rambus's potential claims on PLLs on DRAMs, but believed that any issued claims would not be valid. (CX0711 at 37) ("Proebsting of Hyundai told me that he can put one [a PLL] on-board too and that he doubted any claim we may have made would be valid if challenged.").

October 1994 - Rambus Contemplates Litigation

1018. In late October 1994, Mr. Crisp and Rambus executives again discussed the possibility of suing other companies for using PLLs on SDRAMs. At that time, Rambus was negotiating a potential license agreement with Samsung. Samsung wanted a license agreement that was broader than just RDRAMs, so if they manufactured other types of DRAMs that happened to use Rambus technology, they wouldn't be sued. (Crisp, Tr. 3220-21). Although Rambus wanted to limit the agreement to "compatible uses," *i.e.*, to use in RDRAMs (Crisp. Tr. 3220-21), Samsung "made it abundantly clear" that, unless they got broader protection, "there will be no deal." (CX0767).

Rambus's Response to Finding No. 1018:

The proposed finding is misleading and not supported by the evidence. The evidence shows only that Rambus executives were discussing the licensing negotiations with Samsung and Samsung's desire to obtain a license to Rambus's intellectual property that was not limited to RDRAM. The fact that Rambus executives may have noted that the consequence of granting Samsung such a license would be that Samsung could use aspects of Rambus's intellectual property, such as on-chip PLLs, in an SDRAM with impunity (CCFF 1019), is not properly characterized as a discussion "of the possibility of suing oher companies for using PLLs on SDRAMs."

The proposed finding is also incomplete. The fact that Samsung was intent on a broader license to Rambus's intellectual property indicates their knowledge that Rambus had important intellectual property extending beyond RDRAM. (*See also* RPF 687-88).

1019. On October 25, 1994, CEO Geoff Tate summarized the Samsung "deal details" in an e-mail to Rambus executives and Mr. Crisp. (CX0762). Mr. Tate wrote that pursuant to the negotiated terms, Rambus could not see Samsung unless Samsung intentionally used Rambus technology in a DRAM that competed with RDRAM. (*Id.* at 1). Mr. Tate described this as "the big issue." (*Id.*) As an example, Mr. Tate explained that Rambus could not sue Samsung for putting a PLL on an SDRAM. (*Id.* ("So if they put for example a PLL on an SDRAM we can't sue them")). In a separate e-mail, Mr. Tate explained that he didn't like the terms, but they were the best that Rambus could get. (CX0765 ("we cannot get a Samsung deal without something like the If compromise we gave them. . . . I don't like the compromise but it's what we can get")).

Rambus's Response to Finding No. 1019:

The proposed finding is incomplete. The fact that Samsung was intent on a broader license to Rambus's intellectual property that would allow them, for example, to put a PLL on an SDRAM, indicates their knowledge that Rambus had important intellectual property extending beyond RDRAM. (*See also* RPF 687-88).

1020. Vice-President Allen Roberts replied to Mr. Tate in an e-mail that apparently was lost or destroyed. A portion remains, however, embedded in an e-mail from Richard Crisp. (CX0763; Crisp, Tr. 3221-22). Mr. Roberts wrote: "Is the following a mistype on your part?? Why can't we sue for using a PLL on an SDRAM if we granted [sic] that patent? This is going to be an important point." (CX0763).

Rambus's Response to Finding No. 1020:

The proposed finding is incomplete. Mr. Roberts explained that an on-chip PLL was "going to be an important point" because "Samsung engineers explained that the major reason for not being able to exceed speeds of 70-80 MHz for SDRAM type products was because of I/O timing constraints. They could solve this problem by using our IP." (CX0763).

1021. Mr. Crisp responded to Mr. Roberts and the entire Rambus executive group that Rambus needed to hold, and to be able to collect royalties on, its patent relating to on-chip PLLs. (CX0763 ("I've felt for some time that we need to hold this as one of or key technology patents. If it is allowed, we need to be able to collect on it."; see also Crisp, Tr. 3223-24 (Crisp wanted to collect "whatever monies [Rambus] could get" for the patent)). Mr. Crisp added that he hoped Rambus would sue other companies, particularly those that did not have a RDRAM license, and collect a royalty similar to that for RDRAM. (*Id.*)

Rambus's Response to Finding No. 1021:

The proposed finding is incomplete and misleading. As the quoted language from Mr. Crisp's e-mail indicates, Mr. Crisp's hopes of collecting royalties were conditional and based on a sufficiently broad patent being allowed. Mr. Crisp's statement that he hoped that Rambus would sue companies that did not take a license was made in the context of a possible scenario where Rambus *did* get such a broad patent allowed, and that patent was "a key to permitting SDRAMs to run at Rambus like speeds." (CX0763).

1022. In a separate e-mail sent the same day, Mr. Crisp replied to an e-mail from Vice-President Roberts (also apparently lost or destroyed) regarding Mr. Roberts' explanation of use of a "DLL or PLL." (CX0764). Mr. Crisp emphasized again, "we worked hard to get the claims we did in the original patent filings (really the divisionals). I hate to see us not get the full benefit from them." (*Id.*)

Rambus's Response to Finding No. 1022:

The proposed finding is incomplete and misleading. Mr. Roberts' "explanation of use of a 'DLL or PLL'" was made to Samsung in the context of explaining how Rambus solved the problem that Samsung was just now struggling with of obtaining a good yield of SDRAMs that were capable of high speed performance. (CX0764). Mr. Crisp, in response, while wanting to get the "full benefit" of claims that Rambus may be granted, acknowledged the uncertainty that sufficiently broad claims "may not issue." (*Id.*).

1023. In an e-mail sent the following day, on October 26, 1994, Mr. Crisp emphasized to

CEO Geoff Tate and the Rambus executive group his belief that PLLs or DLLs on SDRAM could be the key to SDRAM reaching speeds of 150 MHz or 200 MHz. CX0766 at 1 (PLLs/DLLs on SDRAMs "may be the key to the 150-200 mhz clock puzzle for the SDRAM boys")). Mr. Crisp emphasized the need to keep proper perspective on "the significance of a PLL on a DRAM." (*Id.*) Mr. Crisp added that the license agreement with Samsung might be good because, as Samsung pulled the market along in the direction of using PLLs or DLLs on SDRAMs, Rambus would "get opportunities to sue" other companies that followed Samsung's lead. (*Id.*)

Rambus's Response to Finding No. 1023:

The proposed finding is incomplete. Once again, Mr. Crisp noted that his scenario "assumes that the patent issues."

1024. CFO Gary Harmon disagreed with the assessment of CEO Geoff Tate, opining that Rambus could still sue Samsung for using PLLs on SDRAMs despite the terms of the agreement.. (CX0767 ("And I don't agree that we can't sue [Samsung] for infringement if they put a PLL on a SDRAM.")). When Vice President Roberts asked whether Rambus should inform Samsung that Rambus considered the idea of clock compensation on the DRAM to correct date timing to be a Rambus invention, CFO Harmon responded that Rambus should "not rock the boat until the money is in the bank." (CX0770).

Rambus's Response to Finding No. 1024:

The proposed finding is incomplete and misleading. Mr. Harmon explained that it was his opinion that, under the terms of the potential Samsung agreement, whether Rambus could sue Samsung for infringement relating to putting a PLL on an SDRAM would depend on whether Samsung was appropriating other Rambus intellectual property and whether it was intentional. (CX0767).

1025. In late November 1994, Vice President Allen Roberts spoke to Mr. Lester Vincent and requested a copy of the PLL and DLL claims. (CX3126 at 495 (Vincent, Dep.)).

Rambus's Response to Finding No. 1025:

The proposed finding is not supported by the evidence. Mr. Vincent testified that his

notes of the conversation with Mr. Roberts stated: "MOST claims P001C2-send copy PLL and DLL." Apparently, Mr. Roberts had requested a copy of the patent application with internal reference number P001C2. This corresponds to the '646 application, which does contain claims related to a form of dual-edge clocking that could apply to the MOST or Mosys products. (RRFF 988, 1008). The reference to "PLL and DLL" appears to be unrelated.

December 1994 - JEDEC Committee Meeting

1026. In December 1994 Richard Crisp was present for Rambus at the JEDEC JC-42.3 Committee meeting in Maui, Hawaii. (JX0022 at 1). The Chairman Mr. Townsend presented the patent policies and showed the patent tracking list. (JX0022 at 3, 12-16).

Rambus's Response to Finding No. 1026:

Rambus has no specific response.

1027. At the December 1994 Committee meeting Mr. Crisp did not make any disclosure to the Committee concerning any Rambus patent or patent application. (Crisp, Tr. 3316). Mr. Crisp did not inform the Committee that the matters under discussion in connection with SDRAM standardization involved inventions that Rambus believed it owned. (CX2092 at 148, 150).

Rambus's Response to Finding No. 1027:

As an initial matter, the proposed finding is irrelevant because Complaint Counsel has not identified any "discussion in connection with SDRAM standardization" at the December 1994 committee meeting that allegedly triggered some disclosure duty on Rambus's part.

Moreover, the proposed finding is misleading because it suggests that Mr. Crisp had a Rambus patent or patent application to disclose in connection with SDRAM standardization. Complaint Counsel has not alleged that Rambus had any patents or patent applications with claims covering SDRAMs until January 1995 at the earliest.

The proposed finding is also misleading because it suggests that Mr. Crisp should have disclosed some inventions in connection with SDRAM standardization that he believed were owned by Rambus. Even if, contrary to the holding of the Federal Circuit and the weight of the eivdence, a JEDEC representative's beliefs could trigger a disclosure obligation, Complaint Counsel did not meet their burden of proving that Richard Crisp held such a belief at this time. (RPF 418-22).

January-February 1995 - Rambus Patent Activity

1028. On January 6, 1995, Rambus filed a preliminary amendment to its pending '961 patent application cancelling the original claims and adding new ones. (Nusbaum, Tr. 1543-44; CX1504-216). Rambus had filed the '961 application in March 1992. (Nusbaum, Tr. 1542; CX1504-019). The preliminary amendment to the '961 application contained claims that a reasonable engineer could construe to cover use of programmable burst length and programmable CAS latency in synchronous DRAMs. (Nusbaum, Tr. 1540-72; Jacob, Tr. 5507-28; see CCFF 1125 et seq.).

Rambus's Response to Finding No. 1028:

The proposed finding that the preliminary amendment to the '961 application contained claims that a reasonable engineer could construe to cover use of programmable burst length and programmable CAS latency in synchronous DRAMs is incorrect. (RRFF 1125-63).

1029. On February 2, 1995, Rambus engineer Richard Barth met with Rambus outside patent counsel Maria Sobrino, a partner in Mr. Vincent;'s law firm. (CX1978; Second Stipulations, No. 1, 2). Ms. Sobrino's notes indicate that she and Mr. Barth discussed claims to directed against synchronous DRAM manufacturers, including claims relating to PLLs/DLLs on DRAMs. (CX1978 at 1 ("Claims to prevent Synch DRAM mftgrs [sic]. Where do we claim using PLL/DLL on DRAMs for phase compensation for DRAMs."); Second Stipulations, No. 1, 3).

Rambus's Response to Finding No. 1029:

The proposed finding mischaracterizes the evidence. Ms. Sobrino's notes state, as indicated: "Claims to prevent Synch DRAM mftgrs [sic]. Where do we claim using PLL/DLL

on DRAMs for phase compensation for DRAMs." The meaning is unclear. For example, "claims to prevent Synch DRAM mftgrs." could refer to claims to future Rambus technology that might prevent synchronous DRAM manufacturers from proceeding in a certain direction, rather than claims to be directed at synchronous DRAM manufacturers.

1030. In late February, 1995, Mr. Crisp informed Rambus executives and the business development group that Mr. Farhad Tabrizi of Hyundai announced at a RamLink meeting that he wanted to make a first showing of RamLink/SyncLink at the May 1995 JEDEC meeting (CX0783 at 1). Mr. Crisp suggested that one angle Rambus could take was to tell the Hyundai representatives in Korea that RamLink/SyncLink involved difficult problems and they were embarking on a very risky path, and that when they were finished they would probably have to pay Rambus higher royalties than they would pay for RDRAM. (CX0783 at 1-2 ("And then tell them that when they get finished they will probably find themselves mired in a big intellectual property trap which may result in higher royalties being paid to Rambus than if they simply license the [Rambus] technology and use it for 100% compatible [RDRAM] products.")) However, Mr. Crisp was reluctant to inform Hyundai of this intellectual property issue because of concern that it would become known at JEDEC. (CX0783 at 2 ("I certainly do not want to bring this intellectual property issue up without careful consideration. I especially do not want it all over JEDEC ...")).

Rambus's Response to Finding No. 1030:

The proposed finding is misleading and incomplete. Mr. Crisp suggested that "one angle we can take" is to:

> "Emphasize the immensly difficult problem that will have to be solved tehcnically to make this proposal work, point out that the skills required to solve the circuit, signalling, clocking, packaging and architectural problems are not fond [sic] in the typcial DRAM organization. That the track record of the standards organizations such as JEDEC . . . are poor; most or the products have not enjoyed widespread market success . . ., and that they are embarking on a very risky path with no system company support."

(CX0783 at 1-2). After having made these points, Mr. Crisp suggested that Hyundai might be told that Rambus had intellectual property that could result in royalties to Rambus.

Complaint Counsel neglect to tell Your Honor that less than two months later, Mr. Crisp *did* warn Hyundai. In an April 12, 1995 letter to K.H. Ho, the Director of Hyundai's Memory Business Division in Seoul, Mr. Crisp wrote:

> "Furthermore since Rambus was the first low pincount high bandwidth DRAM and since Rambus has filed and had issued a number of very fundamental patents, it seems unlikely a device such a Ramlink could avoid infringing one or more Rambus patents."

(RX 555 at 5).

In addition, about six months later, in August 1995, the minutes of the August 21, 1995 meeting of the SyncLink working group stated that:

> "Richard Crisp, of Rambus, informed us that in their opinion both RamLink and SyncLink may violate Rambus patents that date back as far as 1989."

(RX 592 at 2). A Hyundai representative was present at the meeting. (RX 592 at 1).

March 1995 - JEDEC Committee Meetings

1031. In March 1995, Richard Crisp was present for Rambus at a meeting of the JEDEC JC-16 Committee meeting in Las Vegas, Nevada. (CX0082 at 1).

Rambus's Response to Finding No. 1031:

Rambus has no specific response.

1032. During the course of this March 1995 Committee meeting Mr. Crisp observed a presentation by Fujitsu pertaining to a proposal for a technology for high-speed bus transceiver

logic known as STBUS. (CX0082 at 3, 12-16; CX0711 at 52-54). Mr. Crisp reported by email concerning the presentation to Rambus executives. (CX0711 at 52-54). In his report Mr. Crisp stated that the Fujitsu proposal relied on externally bussed reference voltage (CX0711 at 54; Crisp, Tr. 3241) and observed that because of this aspect of the technology, the proposal "may well infringe our work." (CX0711 at 54).

Rambus's Response to Finding No. 1032:

The proposed finding is irrelevant. (*See* RRFF 555, 557).

1033. Mr. Crisp did not tell anyone at JEDEC that he thought that the Fujitsu proposal might well infringe Rambus patents. (Crisp, Tr. 3242).

Rambus's Response to Finding No. 1033:

The proposed finding is irrelevant. (*See* RRFF 555, 557).

1034. In March 1995 Richard Crisp also was present for Rambus at the JEDEC JC-42.3 Committee meeting in Las Vegas. (JX0025 at 1). The Chairman Mr. Townsend presented the patent policies and showed the patent tracking list. (JX0025 at 3, 18-26).

Rambus's Response to Finding No. 1034:

Rambus has no specific response.

1035. In the course of this March 1995 Committee meeting, there was continued discussion among Committee members concerning TI patent coverage of the Quad CAS technology. (JX0025 at 5). TI submitted to JEDEC a letter complying with the EIA patent policy (JX0025 at 5); this was the basis for a unanimous vote by the Committee resolving the issue. (*Id.*).

Rambus's Response to Finding No. 1035:

The proposed finding is incomplete. The resolution of the Quad CAS issue was that the committee voted unanimously to remove the hold on the Quad CAS standards and to revoke the ballot to rescind earlier standards. (JX 25 at 5; Kellogg, Tr. 5022-26). Thus, even where a member fails to disclose an *issued* patent at the time of *balloting*, it is the *licensing* issue, not the disclosure issue, that matters. This is consistent with the EIA's 1/22/96 comment letter to the

FTC, which states that ". . . the important issue is the license availability to all parties on reasonable, non-discriminatory terms." (RX 669 at 4).

1036. In the course of this March 1995 Committee meeting, Mr. Crisp observed and later reported to Rambus executives that there was discussion during the "patent review session" of the meeting that AT&T was reported to have a patent on EDO technology, and that efforts were being made to determine what the patent covered and what position AT&T would adopt concerning licensing. (CX0711 at 57).

Rambus's Response to Finding No. 1036:

Rambus has no specific response.

1037. In the course of this March 1995 Committee meeting, Mr. Crisp observed and later reported to Rambus executives that there was discussion by a Fujitsu representative concerning the use of synchronous clocking in high-speed operation. (CX0711 at 56). Mr. Crisp remarked to his Rambus colleagues that "[i]t appears they are starting to figure out that we have a very good idea with respect to synchronous source clocking. Of course they may get into patent trouble if they do this." *Id.* at 58. Mr. Crisp had in mind patent trouble with Rambus patents. (Crisp, Tr. 3248).

Rambus's Response to Finding No. 1037:

The proposed finding is irrelevant; the claims in this case do not involve synchronous source clocking. (*See* RRFF 554, 564).

1038. Mr. Crisp did not tell anyone at the Committee meeting that he thought that Fujitsu might get into trouble with Rambus patents if it went ahead with its proposal. (Crisp, Tr. 3248). Despite the various patent-related discussions that occurred at the March 1995 Committee meeting, Mr. Crisp did not make any disclosure to the Committee concerning any Rambus patent or patent application. (Crisp, Tr. 3316). Mr. Crisp did not inform the Committee that the matters under discussion in connection with SDRAM standardization involved inventions that Rambus believed it owned. (CX2092 at 148, 150).

Rambus's Response to Finding No. 1038:

The proposed finding is irrelevant. Complaint Counsel have made no showing that Rambus had any claims relating to synchronous source clocking that should have been disclosed, (RRFF 554, 564), or that a comment at a JEDEC meeting could trigger a disclosure obligation.

Moreover, even if, contrary to the holding of the Federal Circuit and the weight of the evidence, a JEDEC representative's beliefs could trigger a disclosure obligation, Complaint Counsel did not meet their burden of proving that Richard Crisp held such a belief with respect to sychronous source clocking. Mr. Crisp's e-mail states only that they "may" get into "patent trouble." (CX 711 at 58). This hardly represents a firm belief that Rambus actually owned intellectual property that covered synchronous source clocking.

April 1995 - Rambus Renews Its JEDEC Membership

1039. In April 1995 Rambus paid its dues to renew its JEDEC membership. (CX0602 at 6).

Rambus's Response to Finding No. 1039:

Rambus has no specific response.

April 1995 - Rambus Strategic Query

1040. In April 1995, Rambus CEO Geoff Tate wrote a follow-up email to John Dillon's June 1994 message suggesting that Rambus might be able to make a broader patent claims on auto-precharge, which would "have high harassment value" with respect to SDRAMs and third-party SDRAM controllers. (CX0791). Mr. Tate asked, "what did we end up doing about this idea?" (*Id.*). Any response to Mr. Tate's question was apparently lost or destroyed.

Rambus's Response to Finding No. 1040:

The proposed finding is wholly speculative. There is no evidence that there ever was a written response to Mr. Tate's e-mail, and Complaint Counsel did not attempt to show that any response was "lost or destroyed."

May 1995 - JEDEC Committee Meeting

1041. In May 1995 Richard Crisp was present for Rambus at the JEDEC JC-42.3 Committee meeting in New Orleans, Louisiana. (CX0088A at 1; Crisp, Tr. 3250). The Chairman Mr. Townsend presented the patent policies and showed the patent tracking list. (CX0088A at 2).

Rambus's Response to Finding No. 1041:

Rambus has no specific response.

1042. During the course of the meeting there were discussions concerning a variety of patent-related issues, including: the showing of a letter from TI concerning the patent policy (CX0088A at 2, 13); the showing of a new Hitachi patent on SIMM mounting (CX0088A at 2, 13); the showing of a letter from Sun clarifying their compliance with the patent policy (CX0088A at 2, 14); and a report from Intel that the EDO patent issue was being worked internally towards a solution (CX0088A at 2).

Rambus's Response to Finding No. 1042:

The proposed finding is misleading and incomplete. The minutes show that the Hitachi patent had been applied for more than three years earlier and the patent policy is described only as requiring an agreement to license on RAND terms.

1043. In the course of the May 1995 Committee meeting, Mr. Crisp observed three different presentations relating to SyncLink architecture. (Crisp, Tr. 3252, 3259). The SyncLink design was being developed by a group working under the auspices of the IEEE; the technology involved a packetized system and was similar to the proprietary Rambus architecture in a number of ways. (Crisp, Tr. 3254-55; see CCFF 1504). Among other things, the SyncLink technology presented at the May 1995 Committee meeting involved the use of both the rising and falling edge of the clock for data input. (CX0088A at 58 ("Reference clock, both edge for input, positive edge for output"); Crisp, Tr. 3261-63; CX0711 at 156).

Rambus's Response to Finding No. 1043:

The proposed finding is misleading. As explained in the JEDEC minutes, the Synclink technology was being standardized under the auspices of the IEEE, not JEDEC, and was being brought to JEDEC simply to standardize the pinout. (CX0088A at 5; JX0026 at 10).

1044. At the May 1995 Committee meeting, there were inquiries about possible patent issues pertaining to the SyncLink technology. Gordon Kelley of IBM asked whether or not HP, Hyundai, Mitsubishi or TI had any patents covering any of the matters being presented; all of these companies stated that they did not. (CX0711 at 72; Crisp, Tr. 3264-65). Sam Calvin of Intel and Gordon Kelley of IBM also inquired whether there were any Rambus patents covering the SyncLink technology. (CX0711 at 73; Crisp, Tr. 3266-67). When Mr. Crisp did not respond to this inquiry at the May 1995 meeting, Mr. Kelley asked Mr. Crisp to go back to Rambus and

then report back to the Committee whether Rambus knew of any patents, especially Rambus patents, that may read on the SyncLink technology. (CX0711 at 73; CX0794 at 4; Crisp, Tr. 3267-68).

Rambus's Response to Finding No. 1044:

The proposed finding is incomplete.

First, although the Synclink technology was being brought to JEDEC to standardize the pinout and although HP, Hyundai, Mitsubishi and TI stated that they did not have patents covering any of the matters presented, a patent application claiming the Synclink pinout was later filed. (RPF 245). Among the named inventors who were present at the JEDEC meeting were Desi Rhoden of VLSI and Hans Wiggers of HP. For a review of the evidence regarding the lengthy e-mail discussion of patent-related issues between Mr. Wiggers and Mr. Crisp, see RPF 537-541.

Second, Mr. Crisp did respond to Mr. Calvin of Intel, and to his colleague, Mr. Lai. As they were walking out of the May 1995 meeting, Mr. Crisp told these Intel representatives that my personal opinion was that it would be virtually impossible for them [Synclink] to not infringe some aspect of what we had done."

In addition, about six months later, in August 1995, the minutes of the August 21, 1995 meeting of the SyncLink working group stated that:

> "Richard Crisp, of Rambus, informed us that in their opinion both RamLink and SyncLink may violate Rambus patents that date back as far as 1989."

(RX 592 at 2). A Hyundai representative was present at the meeting. (RX 592 at 1).

1045. In his e-mail informing the Rambus executives, engineering managers and

business development and marketing groups of this development, Mr. Crisp listed a few ideas he had of Rambus intellectual property issues regarding SyncLink (CX0711 at 68, 73). His list included:

"1. DRAM on a packet oriented bus
2. DRAM with low swing signaling
*. . . .
4. DRAM with programmable access latency"

(CX0711 at 68, 73).

Rambus's Response to Finding No. 1045:

Rambus has no specific respnose.

1046. Mr. Crisp offered his suggestion of how to respond to the JEDEC request as well as what Rambus might want to mention to Hyundai in their attempts to restart negotiations. He suggested that Rambus "review our current issued patents and see what we have that may work against them." (CX0711 at 68, 73). He recommended that Rambus consider "simply provid[ing] a list of patent members which have issued" and telling JEDEC members to "decide for yourselves what does and does not infringe." (*Id.*) Mr. Crisp added, however, that if the Rambus patents were "not a really key issue . . . then it makes no sense to alert them to a potential problem they can easily work around," and that "we may not want to make it easy for all to figure out what we have especially if nothing looks really strong." (*Id.*)

Rambus's Response to Finding No. 1046:

The proposed finding is misleading because it changes the order of various statements in Mr. Crisp's e-mail to confuse Mr. Crisp's suggestions of what Rambus may want to tell Hyundai with his suggestions of what Rambus may want to state at the next JEDEC meeting. For example, the final sentence of proposed finding suggests that all of the language quoted was directed at JEDEC when, in fact, the first quote in the sentence comes from a different paragraph directed at Hyundai. (CX 711 at 73).

1047. Following receipt of Mr. Crisp's e-mail, Rambus CEO Tate wrote in his personal notebook, {

} (CX1723 at 138 (*in camera*).

Rambus's Response to Finding No. 1047:

Rambus has no specific response.

1048. Despite the various patent-related discussions that occurred at the May 1995 Committee meeting and the specific inquiry concerning Rambus patents on SyncLink technology, Mr. Crisp did not make any disclosure to the Committee concerning any Rambus patent or patent application. (Crisp, Tr. 3316). Mr. Crisp did not inform the Committee that the matters under discussion in connection with SDRAM standardization involved inventions that Rambus believed it owned. (CX2092 at 148, 150).

Rambus's Response to Finding No. 1048:

The proposed finding is misleading and incomplete with respect to Synclink. Shortly after the meeting, Mr. Crisp informed various JEDEC members that it was his opinion that Synclink would likely violate Rambus's intellectual property. (CX0711 at 73; RPF 537-41). Then, in August 1995, the minutes of the Synclink working group, whose members were mostly JEDEC representatives, state that Crisp had informed it that "SyncLink may violate RamBus patents that date back as far as 1989." (RX0592 at 2; RPF 542-43; Parties First Set of Stipulations, p. 3).

At the next JEDEC meeting in September 1995, Mr. Crisp presented a statement of Rambus's position. That statement made clear that Rambus believed that its work predated Synclink and then stated:

> "At this time, Rambus elects to not make a specific comment on our intellectual property position relative to the Synclink proposal. *Our presence or silence at committee meetings does not constitute an endorsement of any proposal under the committee's consideration nor does it make any statement regarding potential infringement of Rambus intellectual property.*"

(JX0027 at 26) (emphasis added). Rambus's statement was taken by JEDEC members as a warning that Rambus may have intellectual property relating to Synclink. (RPF 545-48).

The proposed finding with respect to SDRAM standardization is irrelevant because Complaint Counsel has not identified any SDRAM standardization work in May 1995 that allegedly triggered some disclosure duty on Rambus's part. Moreover, the proposed finding is misleading because it suggests that Mr. Crisp had a Rambus patent or patent application to disclose in connection with SDRAM standardization. The only patent application that Complaint Counsel has raised in this regard, the '961 application, did not contain claims covering SDRAM. (RRFF 1125-63).

The proposed finding with respect to SDRAM standardization is also misleading because it suggests that Mr. Crisp should have disclosed some inventions in connection with SDRAM standardization that he believed were owned by Rambus. Even if, contrary to the holding of the Federal Circuit and the weight of the evidence, a JEDEC representative's beliefs could trigger a disclosure obligation, Complaint Counsel did not meet their burden of proving that Richard Crisp held such a belief at any relevant time. (RPF 418-22). In fact, after Mr. Crisp conducted a review of Rambus patent and patent applications in the summer of 1995, he concluded that "we didn't have any patents or pending patents that I could find that were required for the SyncLink proposal as I saw it at that point. I also didn't see that we had anything that applied to SDRAM at that time either." (Crisp, Tr. 3542-43).

June 1995 - Rambus Patent Activity

1049. On June 6, 1995, Rambus filed its patent application no. 08/469,490 (the '490 application). (CX1504-246; Nusbaum, Tr. 1572). The '490 application was a continuation of the '961 application. (Nusbaum, Tr. 1572). The '490 application contained claims covering a

JEDEC-compliant SDRAM, the use of such an SDRAM, and a computer system incorporating a JEDEC-compliant SDRAM. (Nusbaum, Tr. 1573-1578; Jacob, Tr. 5528-32; see CCFF 1164 et seq.).

Rambus's Response to Finding No. 1049:

The proposed finding that the '490 application contained claims covering a JEDEC-compliant SDRAM, the use of such an SDRAM, and a computer system incorporating a JEDEC-compliant SDRAM is incorrect. (RRFF 1164-82).

Summer 1995 - Rambus Patent Efforts Directed at SyncLink

1050. After the May 1995 Committee meeting, Mr. Crisp did a "general sort of read" of Rambus intellectual property. (Crisp, Tr. 3274). Mr. Crisp had access to the entire set of Rambus patent files; he doesn't recall which of those materials he actually reviewed at the time. (CX0798; Crisp, Tr. 3585-86).

Rambus's Response to Finding No. 1050:

The cited testimony does not refer to the review of Rambus patents and patent applications that Mr. Crisp undertook in connection with Mr. Kelley's request at the May 1995 JEDEC meeting. That testimony is set out below:

> "Q: Well, did he ask Rambus – did he ask you as the representative –
>
> A: He asked me – he asked me as the Rambus JEDEC representative.
>
> Q: To go back and research your company's patents?
>
> A: He asked me to state whether we would make a comment on our intellectual property position on SyncLink or whether we had any patents that would apply to it.
>
> Q: Okay, all right. And as a result of that, did you do anything?
>
> A: Yes, I did.

Q: What did you do?

A: I first found out what I could find out about what the JEDEC patent policy was to find out what my obligation was. Then I also talked with some people internally to find out which patents and patent applications would be the best ones to look at to see if we had anything that might already exist that covered the SyncLink spec as we understood it to be, and I took that information with me on a trip that I made to Asia and spent basically the whole plane flight on the way to I think it was Taiwan reading this material.

Q: How long was that flight back then?

A: Oh, it was probably a 12 or 13-hour-flight from San Francisco to Taipei. I'm not going to say I read it for the whole flight but, you know, a good portion of the flight.

Q: And you took both patents and patent applications?

A: That's what I remember.

. . .

Q: And did you reach any conclusions – after reviewing the patents and patent applications that you took with you on this trip and looked through, did you reach any conclusions about the scope of Rambus's patents and patent applications?

A: Yes, I did.

Q: What were those conclusions?

A: Well, I reached the conclusion that we didn't have any patents or pending patents that I could find that were required for the SyncLink proposal as I saw it at that point. I also didn't see that we had anything that applied to SDRAM at the time either."

(Crisp, Tr. 3540-43). The proposed finding is thus inaccurate and fails to reflect the extent of Mr. Crisp's efforts.

1051. Mr. Crisp focused on a particular patent application that had been earlier filed for Rambus by patent counsel Lester Vincent. (Crisp, Tr. 3274, 3274-76). A discussion between Mr. Crisp and colleagues including Vice-President Allen Roberts concluded that the particular patent application had legal problems and could only be salvaged by filing a new divisional patent application. (CX0796; Crisp, Tr. 3276-77).

Rambus's Response to Finding No. 1051:

The proposed finding that Mr. Crisp focused on a particular application is not supported by the evidence to the extent that it suggests exclusion of other patent applications. *See* RRFF 1050.

1052. Mr. Crisp informed Vice-President Roberts, Vice-President Mooring, and Rick Barth that the patent application Rambus had filed in 1990 should allow Rambus to block SyncLink; Rambus just needed to "sweat through the details" of ensuring that Rambus obtained the appropriate claims. (CX0797; Crisp, Tr. 3279). Mr. Crisp stated his view that if it was necessary to do so, a new divisional application should be filed. (CX0797 ("if it is possible to salvage and get anything that helps us get a claim to shoot SyncLink in the head, we should do it")). Mr. Crisp volunteered to take ownership of this task. (*Id.*).

Rambus's Response to Finding No. 1052:

The e-mail was prepared before Mr. Crisp conducted the review described in RRFF 1050.

1053. On July 21, 1995, Don Stark, and engineer at Rambus, circulated an e-mail to all Rambus staff calling specific attention to the SyncLink clocking scheme, and the fact that SyncLink used both edges of the clock to input data. (CX0711 at 156, 157; Crisp, Tr. 3261-62).

Rambus's Response to Finding No. 1053:

The proposed finding is misleading and incomplete. Mr. Stark listed numerous Synclink features, beginning with features that Synclink shared with Rambus technology. (CX0711 at 157). The clocking scheme was not listed among the similarities between Synclink and Rambus, presumably because only the rising edge of the clock is used for data output. (*Id.*)

1054. By July 1995 Mr. Crisp reported to Vice-President Roberts and CEO Geoffrey Tate that he had done a review of Rambus intellectual property and wanted to talk with Lester Vincent about adding claims to Rambus patent applications in order to better describe Rambus inventions. (CX0824; Crisp, Tr. 3300). Mr. Roberts authorized Mr. Crisp and Rick Barth of Rambus to speak with Mr. Vincent, and they did so in early August 1995. (CX0825; CX2000 at 12 (Vincent time record entry for August 2, 1995)).

Rambus's Response to Finding No. 1054:

The proposed finding mischaracterizes the evidence. Mr. Roberts did not authorize Mr. Crisp and Mr. Barth to speak with Mr. Vincent, but, rather, told Mr. Crisp to consult with Mr. Barth as to how to proceed. (CX0825).

1055. During the later part of 1995, Rambus apparently provided Mr. Vincent with a copy of a SyncLink standard or data sheet, and as of December Mr. Vincent was engaged in preparing a preliminary patent application amendment based on his review of the SyncLink proposed standard. (CX2000 at 13 (Vincent time record entries for Dec. 5, 14 and 15, 1995); CX3130 at 166-68 (Vincent, Dep.)).

Rambus's Response to Finding No. 1055:

The proposed finding is not supported by the evidence. There is no indication of how Mr. Vincent obtained the "Synclink disclosure" referenced in his time record entries.

August-September 1995 - Renewed Estoppel Concerns

1056. In August 1995, Rambus hired Anthony Diepenbrock as Intellectual Property Manager for Rambus. (CX0827). The internal announcement by Rambus CEO Geoffrey Tate stated that a reason for hiring Mr. Diepenbrock, who was trained as an engineer and an attorney, was to have someone who would "focus[] full time on our strategy for protecting IP, analyzing

our IP position vs competitive technologies, etc." (*Id.*). Among the competitive technologies that Mr. Tate wanted Mr. Diepenbrock to focus on were SDRAM and SyncLink. (Diepenbrock, Tr. 6111-12).

Rambus's Response to Finding No. 1056:

Rambus has no specific response.

1057. On September 12, 1995, Rambus CEO Tate sent an e-mail to all Rambus executives, engineering managers, and members of the business development group reminding them that Mr. Diepenbrock's "number 1 objective" was to "understand competitive technology" and "determine what should be done to strengthen [the Rambus] IP position relative to competition." (CX0832). Mr. Tate requested that the recipients forward to Mr. Diepenbrock any e-mails they received talking about competitive technology developments and directions, such as "JEDEC meeting reports." (*Id.*)

Rambus's Response to Finding No. 1057:

Rambus has no specific response, except to note that the exhibit in question is CX0831 rather than CX0832.

1058. Also on September 12, 1995, Rambus CEO Tate began a series of weekly one-on-one meetings with Mr. Diepenbrock. Mr. Tate's notes from the September 12 meeting indicate that Mr. Tate instructed Mr. Diepenbrock, "cover: SDRAM -Now-Next SyncLink Mosys" and "steps: 1. Understand our IP; 2. Understand competitive Tech. And Directions; 3. Assess or current Patents - what claims/strength (?) Do we have vs. competition and what can we do? . . . .5. Plan of Action; 6. Implement." (CX1730 at 1). Mr. Tate's notes from his September 19, 1995 meeting with Mr. Diepenbrock indicate that they discussed, "Claims in issued patents that read on current SDRAMs/Mosys/SyncLink." (C's 1731 at 1).

Rambus's Response to Finding No. 1058:

The proposed finding that, on September 19, 1995, Mr. Tate and Mr. Diepenbrock discussed "Claims in issued patents that read on current SDRAMs/Mosys/SyncLink" is not supported by the evidence. As an initial matter, Rambus had no claims in issued patents that read on current SDRAMs at that time, and Complaint Counsel do not contend otherwise. (Parties' First Set of Stipulations, No. 10). Moreover, Mr. Tate's notes demonstrate a practice of

taking notes on the left hand side and writing action items to himself in circles on the right. For example, on September 12, 1995, the direction "Fed-X video to Tony H." appears in a circle on the right. (CX 1730 at 1). Similarly, on September 19, 1995, the notes contain the circled direction to "Give my correct [illegible]" in a circle on the right. The note "Claims in issued patents that read on current SDRAMs/Mosys/SyncLink" thus probably does not represent a note taken during the meeting with Mr. Diepenbrock, as the finding states.

1059. Shortly after Mr. Diepenbrock was hired at Rambus, Rambus patent counsel Lester Vincent spoke with Mr. Diepenbrock concerning the issue of equitable estoppel. (Diepenbrock, Tr. 6216-17). Mr. Vincent told Mr. Diepenbrock that he had a concern that Rambus employees attending standards bodies meetings in some capacity could raise an equitable estoppel issue regarding patents that Rambus had or was seeking. (Diepenbrock, Tr. 6217-18). After studying the issue himself, Mr. Diepenbrock came to agree with Mr. Vincent about the risk of Rambus employees, including Richard Crisp, attending such meetings. (Diepenbrock, Tr. 6218-19).

Rambus's Response to Finding No. 1059:

Rambus has no specific response.

1060. Mr. Diepenbrock conveyed the shared concerns of himself and Mr. Vincent concerning equitable estoppel risks to Mr. Crisp, who at the time did not perceive the risk. (Diepenbrock, Tr. 6219; *see* Crisp, Tr. 3005-06). Mr. Vincent told Mr. Diepenbrock he had raised the issue before Mr. Diepenbrock joined Rambus. (Diepenbrock, Tr. 6219; *see* CX3127 at 114, CX3126 at 553 (Vincent, Dep.) (hallway conversation between Mr. Diepenbrock and Mr. Crisp)). Mr. Diepenbrock talked with Mr. Crisp about these concerns. (CX2082 at 804-06 (Crisp, Dep.)).

Rambus's Response to Finding No. 1060:

The first sentence of the proposed finding misstates the question that Complaint Counsel asked of Mr. Diepenbrock, which was whether Mr. Crisp had "initially" perceived a risk. (Diepenbrock, Tr. 6219).

1061. In late September, Mr. Crisp wrote an email to Rambus executives that referred to "Tony's worst case scenario regarding estoppel" and stated that "the only thing lost is the ability to enforce our rights against those that can prove estoppel applies. . . . We do not have our patent

invalidated." (CX0837 at 1; Crisp, Tr. 3005-06). Mr. Crisp reminded Rambus executives that when Rambus joined JEDEC, a group of individuals within Rambus decided that Rambus would not talk about potential for patent infringement. (Crisp, Tr. 3325). He suggested that Rambus re-evaluate its position relative to what it decided to disclose and what to keep quiet about. He also suggested that they "redouble [their] efforts" to get the necessary amendments completed and new claims added to its pending patent applications in order to "make damn sure this ship is watertight before we get too far out to sea." (CX0837 at 2; Crisp, Tr. 3325-26).

Rambus's Response to Finding No. 1061:

Complaint Counsel's proposed finding omits very relevant passages from Mr. Crisp's e-mail in an effort to change its meaning, as described below:

- Immediately after the first portion quoted in the finding, Mr. Crisp says "[o]f course I am not convinced that estoppel applies either. . . ." (CX 837 at 1).
- The second reference to the e-mail in the proposed finding says that the e-mail states that Rambus had decided after joining JEDEC that it would not talk about potential for patent infringement. In fact, the e-mail talks about what Rambus "was expected" to disclose, and it gives legitimate business justifications for the decision not to disclose patent *applications*:

  "We decided that we really could not be expected to talk about potential infringement for patents that had not issued both from the perspective of not knowing what would wind up being acceptable to the examiner, and from the perspective of not disclosing our trade secrets any earlier than we are forced to."

(CX 837 at 2).

Mr. Crisp testified that he had learned this information primarily from outside counsel, Lester Vincent. (Crisp, Tr. 3473).

September 1995 - JEDEC Committee Meeting

1062. In September 1995 Richard Crisp was present for Rambus at the JEDEC JC-42.3 Committee meeting in Crystal City, Virginia. (JX0027 at 1; Crisp, Tr. 3305). The Chairman Mr. Townsend presented the patent policies and showed the patent tracking list. (JX0027 at 4, 20-25; Crisp, Tr. 3306).

Rambus's Response to Finding No. 1062:

Rambus has no specific response.

1063. Among the patent matters discussed at the September 1995 Committee meeting was the response of Rambus to the inquiry made at the May 1995 Committee meeting concerning patents on SyncLink. (Crisp, Tr. 3306-08). Mr. Crisp provided the Committee a letter from Rambus in which Rambus refused to provide any information concerning whether there were Rambus patents or patent applications that might apply to SyncLink. (CX0829; JX0027 at 26 ("Rambus elects not to make a specific comment on our intellectual property position relative to the Synclink proposal.")). The letter included other recitations, including the observation that it would be several years before there was a finalized SyncLink specification to analyze for possible infringement, and that SyncLink was being developed under the auspices of IEEE, which had "a less stringent patent policy than JEDEC." (*Id.*).

Rambus's Response to Finding No. 1063:

The finding is incomplete and misleading. The letter, which was shown and read to the JC 42 committee, and which was attached to the JC 42.3 meeting minutes, included the following language:

> "At this time, Rambus elects to not make a specific comment on our intellectual property position relative to the Synclink proposal. *Our presence or silence at committee meetings does not constitute an endorsement of any proposal under the committee's consideration nor does it make any statement regarding potential infringement of Rambus intellectual property*."

(JX 27 at 26) (emphasis added). The letter also stated Rambus's view that its DRAM design efforts began well before the Ramlink and SyncLink efforts. (*Id.*)

1064. Rambus Vice-President Mooring, as Mr. Crisp's supervisor, worked with Mr. Crisp and approved the language in the letter stating that "Rambus elects not to make a specific comment on our intellectual property position" on the SyncLink proposal. (CX2112 at 206-07 (Mooring, Dep.)). There is nothing in the letter informing the Committee that Rambus had pending patent applications relating to specific SDRAM technologies of programmable CAS latency, programmable burst length, on-chip PLL or DLL, and dual edge clocking. (CX2056 at 274 (Mooring, Dep.)).

Rambus's Response to Finding No. 1064:

The finding is misleading in that it implies that the letter was insufficient to put the JC 42.3 committee on notice that Rambus might have intellectual property relevant to the work of the committee. The letter did *not* limit itself just to the SyncLink proposal and instead stated that Rambus's "presence or silence at committee meetings" did not "constitute an endorsement of *any* proposal under the committee's consideration" or make "*any* statement" about potential infringement. (JX 27 at 26) (emphasis added).

In addition, JEDEC 42.3B Chairman Gordon Kelley testified that the letter *did* constitute a warning to the committee. (Kelley, Tr. 2579) (explaining that "[a] comment of no comment is a notification to the committee that there should be a concern" about intellectual property issues).

1065. At the September 1995 Committee meeting Mr. Crisp read the Rambus letter to the JEDEC Committee electing to make no comment on the Rambus intellectual property position (JX0027 at 26). The letter generated discussion. (CX0711 at 66). Mr. Crisp reported to his Rambus colleagues that Gordon Kelley of IBM commented at the meeting that "he heard a lot of words but did not hear anything said." (*Id.*).

Rambus's Response to Finding No. 1065:

Rambus has no specific response.

1066. In the course of the discussion of the Rambus letter at the September 1995 Committee meeting, Mr. Crisp reminded the Committee that Rambus in the past had reported a Rambus patent to the Committee. (Crisp, Tr. 3312). This was a reference to the disclosure to the Committee of the Rambus '703 patent in September 1993. (*Id.*). Mr. Crisp was saying that Rambus was in the category of JEDEC members that had disclosed patents. (Crisp, Tr. at 3313).

Rambus's Response to Finding No. 1066:

The finding is incomplete; it omits Mr. Crisp's statement that he "reminded them of the 14 patents relating to SDRAM, *and that our silence was not an agreement that we have no IP related to SycLink, . . .* [and I] reminded them that the member companies are constantly receiving patents on things they are standardizing and that they seldom report the patents." (CX 711 at 167) (emphasis added).

1067. Mr. Crisp did not tell the Committee that he was working to draft claims to shoot SyncLink in the head (Crisp, Tr. 3316) or that he believed that SyncLink would violate Rambus patents (Crisp, Tr. 3316). Mr. Crisp did not identify what particular aspects of the SyncLink technology might infringe Rambus intellectual property. (Crisp, Tr. 3317). He did not identify the SyncLink dual edge clocking feature as a feature that might violate Rambus intellectual property. (Crisp, Tr. 3317). Mr. Crisp did not inform the Committee that the matters under discussion in connection with SDRAM standardization involved inventions that Rambus believed it owned. (CX2092 at 148, 150).

Rambus's Response to Finding No. 1067:

The statement that was read to the meeting attendees and placed in the minutes speaks for itself. It constituted "a notification to the committee that there should be a concern" about intellectual property issues. (Kelley, Tr. 2579).

1068. Mr. Crisp reported to his Rambus colleagues that there would be no second showings of the SyncLink material at the September 1995 Committee meeting. (CX0711 at 171). Mr. Crisp reported that one of the meeting participants told Mr. Crisp that he thought the reason there would be no second showings of the SyncLink technology at JEDEC was that "we [Rambus] have cast doubt over the patent issue." (*Id.*).

Rambus's Response to Finding No. 1068:

The proposed finding is misleading and incomplete. At a JEDEC meeting on December 9-10, 1997, the SLDRAM pinout standard ballot was approved by the JC-42.3 subcommittee. (JX 41 at 22, 24; RX 1114 at 1; Rhoden, Tr. 1206-08). Complaint Counsel have

never suggested that Rambus's patents cover the pinout. In contrast, JEDEC President Desi Rhoden and several other JEDEC representatives are named inventors on a patent that claims the precise specifications of the pinout standardized by JEDDEC. (Rhoden, Tr. 1209-11).

Fall 1995 – Rambus Strategy Presentation

1069. In the fall of 1995, Rambus Intellectual Property Manager gave a presentation to Rambus employees on "Rambus IP strategy." (CX1267; Diepenbrock, Tr. 6129-30). The slides included discussion of "Offensive" and "Defensive" strategies. (CX1267; Diepenbrock, Tr. 6130). The "Offensive" patent strategy, according to Mr. Diepenbrock, meant "finding key or essential areas of Rambus intellectual property and claiming them as broadly as possible." (Diepenbrock, Tr. 6131). The first example of the "Offensive" strategy relates to DLLs, or delay locked loops. (CX1267; Diepenbrock, Tr. 6131-32). The second example given relates to dual edge clocking technology, or transmitting or receiving data on both edges of the clock. (C's 1267; Diepenbrock, Tr. 6132-33). At the time this presentation was given, Rambus had pending patent applications relating to both these features. (Diepenbrock, Tr. 6133).

Rambus's Response to Finding No. 1069:

The proposed finding that Rambus had patent applications "relating" to DLLS and dual edge clocking in the Fall of 1995 is vague and misleading. It is true that Rambus had a claim pending at the time that included a limitation describing a DLL (CCFF 1185; RRFF 1191-92); likewise, Rambus had a claim pending that included a dual edge clocking limitation (CCFF 1206). These claims, however, contained other limitations as well and did not read on the presentations and/or standards that Complaint Counsel assert triggered a disclosure duty on Rambus's part. (See generally RRFF 1183-1215).

Fall 1995 - SDRAM Lite and Next Generation SDRAM Ballots

1070. Among the topics discussed at the September 1995 JC-42.3 Committee meeting was NEC's SDRAM Lite proposal. (JX0027 at 13). NEC proposed a reduced-feature version of the SDRAM in order to reduce costs. NEC proposed to use a single CAS latency value and burst length value. (CCFF 572). The Committee decided to issue a survey ballot to its members regarding the SDRAM Lite proposal. (CCFF 573). Mr. Crisp received this ballot by e-mail. (CX0711 at 196-99).

Rambus's Response to Finding No. 1070:

The proposed finding is not supported by the weight of the evidence. The NEC SDRAM lite presentation did not include a single fixed burst length, but rather two burst lengths of 1 and 4. (RRFF 572).

The proposed finding is also misleading in referring to the survey ballot as "regarding the SDRAM Lite proposal." The survey ballot was not directed at any particular proposal but, rather was gauging interest in various ways the SDRAM feature set might be reduced. (CX0711 at 196-99; *see* RRFF 573).

1071. Also among the topics discussed at the September 1995 JEDEC JC-42.3 Committee meeting was the preparation and distribution of a survey ballot to obtain Committee members' views concerning various features in connection with "next generation" SDRAM standard technology. (JX0027 at 14; Crisp, Tr. 3323-24). In the aftermath of that meeting, a survey ballot dated October 30, 1995, was prepared and distributed to JC-42.3 Committee members including Rambus. (Crisp, Tr. 3328-29; CX0260 at 1).

Rambus's Response to Finding No. 1071:

Rambus has no specific response.

1072. Among the issues inquired about in the next generation SDRAM survey ballot was whether Committee members believed that it was important to standardize CAS latency beyond the values permitted under the existing SDRAM standard. (CX0260 at 9). The ballot also asked members to state whether they believed that on-chip PLL or DLL was important to reduce the access time from the clock for future generations of SDRAM (CX0260 at 12), and whether they believed future generations of SDRAM could benefit from using both edges of the clock for sampling inputs (*id.*).

Rambus's Response to Finding No. 1072:

Rambus has no specific response.

1073. The survey ballot was received by Rambus and distributed to the business development and marketing groups of Rambus. (Crisp, Tr. 3329; CX2056 at 264 (Mooring, Dep.)). Mr. Mooring summarized the reaction at Rambus: "We [Rambus] believe we invented key aspects of several of the things on this list." (CX2056 at 268 (Mooring, Infineon Dep.)).

Rambus's Response to Finding No. 1073:

Rambus has no specific response.

Fall 1995 - Rambus Patent Activity

1074. During October 1995, Anthony Diepenbrock of Rambus met with outside Rambus patent attorney Lester Vincent concerning pursuit by Rambus of patents pertaining to DLL technology. (CX1988 at 2).

Rambus's Response to Finding No. 1074:

Rambus has no specific response.

1075. In October 1995, Mr. Vincent's firm filed on behalf of Rambus an amendment to the pending Rambus '692 patent application. (CX1483 at 1, 8; see also CX1502 at 233, 241). This amendment modified an earlier amendment of the application, filed in June 1993, that contained claims pertaining to the use of PLL circuitry. (CX1502 at 208; Nusbaum, Tr. 1583-85). The '692 application as amended in October 1995 contained multiple claims addressing on-chip PLL technology. (Nusbaum, Tr. 1584; CX1502 at 233-35 (claims 151, 152, 166, 167)).

Rambus's Response to Finding No. 1075:

The proposed finding is not supported by the weight of the evidence. Although the claims of the '692 application refer to a "PLL," the reference is a misnomer since the claims actually describe a "DLL." (RRFF 1191).

The proposed finding is also vague in its reference to "the use of PLL circuitry" and "on-chip PLL technology." The claims of the '692 application contain various limitations which limit them to a particular implementation of on-chip PLL technology. (CX1483 at 1-3).

1076. The United States Patent and Trademark Office sent Mr. Vincent's firm a Notice of Allowance of claims with respect to the '646 application on October 6, 1995. (CX1482; Diepenbrock, Tr. 6190). A Notice of Allowance occurs when the patent office has reason to believe that claims in a particular application should be issued. (Diepenbrock, Tr. 6151). A Notice of Allowance means that "other than the actual publication of the patent, it's essentially a done deal." (CX2114 at 23 (Karp, Dep.)).

Rambus's Response to Finding No. 1076:

The proposed fiding is misleading and incomplete. Complaint Counsel cite the testimony of Mr. Karp, who is not a patent lawyer. In fact, a Notice of Allowance does not necessarily represent a "done deal." As Mr. Diepenbrock explained:

> "Well, after a notice of allowance is issued, Blakely Sokoloff had a policy of reviewing the file for the receipt of post cards for transmittals to the patent office and other documents to make sure that everything was in order before they paid the issue fee, and if something wasn't in order, the issue fee wouldn't be paid, and it would be put back in the prosecution."

(Diepenbrock, Tr. 6190-91).

1077. The '646 patent application, which later resulted in the issuance to Rambus of its '327 patent, contained claims related to moving input or output data on the rising and the falling edges of the clock. (Diepenbrock, Tr. 6144-46; Nusbaum, Tr. 1597, 1601-1603; see also Jacob, Tr. 5550-5551 (technical expert opinion that claim describes the general concept of dual edge clocking technology)). Internal Rambus documents refer to the '646 application , also known internally as the P 001C2 application, as "the clocking patent." (CX0871 at 1; Diepenbrock, Tr. 6168). Anthony Diepenbrock, the patent attorney who was employed starting in the fall of 1995 to manage Rambus' intellectual property portfolio (Diepenbrock, Tr. 6099, 6106-6107), testified that the P 001C2 application "included claims having qualifiers that related to moving data on the rising and the falling edges of the clock." (Diepenbrock, Tr. 6145). (See also CX2114 at 212 (Karp, Dep.)).

Rambus's Response to Finding No. 1077:

The proposed finding is misleading. Although certain claims of the '646 application did have limitations related to inputting or outputting data on the rising and falling edges of the clock, they contained other limitations as well. (CX1493 at 184-85).

December 1995 - JEDEC Committee Meeting

1078. In December 1995 Richard Crisp was present for Rambus at the JEDEC JC-42.3 Committee meeting in Dallas, Texas. (JX0028 at 1; Crisp, Tr. 3337). The JEDEC patent policies had been the subject of a presentation in a plenary session of JEDEC prior to this Committee meeting; those presentation materials including the patent tracking list are an attachment to the minutes. (JX0028 at 3, 12-23).

Rambus's Response to Finding No. 1078:

Rambus has no specific response.

1079. Among the topics discussed at the Committee meeting were the responses to the future SDRAM features survey ballots that had been distributed to Committee members in October 1995. (JX0028 at 6, 36). The Representative from Mosaid, the Committee member that had conducted the survey for the Committee, made a presentation concerning the results of the survey. (JX0028 at 6). Among the survey results was a tally showing that most responding Committee members believed that it was important to standardize CAS latency beyond the values permitted under the existing SDRAM standard. (JX0028 at 42). The tallied results showed that most responding Committee members believed that on-chip PLL or DLL was important to reduce the access time from the clock for future generations of SDRAM. (JX0028 at 45). The tallied results showed that the majority of the responding Committee members did not believe future generations of SDRAM could benefit from using both edges of the clock for sampling inputs. (JX0028 at 45).

Rambus's Response to Finding No. 1079:

Rambus has no specific response.

1080. During the course of the December 1995 discussion of the survey ballot results, the representative of Mosaid disclosed that Mosaid had a patent pending on DLL technology, but stated that the patent pertained to a particular implementation and may not be required to use the standard. (JX0028 at 6; Crisp, Tr. 3342). Mr. Crisp reported to his colleagues at Rambus that Mosaid had reported the existence of a "pending patent application for PLL/DLL on SDRAMs" and repeated the characterization of the application as an implementation patent. Mr. Crisp reported that if the patent is a "concept patent," Mosaid would comply with the JEDEC patent policy. (CX0711 at 191-92).

Rambus's Response to Finding No. 1080:

The proposed finding is incomplete and misleading in suggesting that Mosaid made a voluntary disclosure of a patent application. To the contrary, Mosaid's comment was in response to a specific question from Hyundai. (JX0028 at 45 ("Wondering DLL may be Mosaid

patent.")). The exchange does confirm that, to the extent that there was any disclosure duty, it applied only to essential patents, that is patents that are "neccessary to use a standard." (See generally RPF 274-85).

1081. Mr. Crisp also reported: "The momentum is building for getting a new SDRAM standard kicked off. Kelly [sic] of IBM is saying that they need to do it right, to it to stand the test of time. He admits that the current devices will not run over 100mhz. They all say that it must change." (CX0843 at 1). This report indicates that JEDEC was looking to the future and interested in developing a more high performance or high speed product. (CX2112 at 249 (Mooring, FTC Dep.)).

Rambus's Response to Finding No. 1081:

Rambus has no specific response.

1082. Despite the discussion at the December 1995 JC 42.3 Committee meeting concerning CAS latency, on-chip PLL/DLL technology and dual-edge clocking, and despite the disclosure by Mosaid of a possibly relevant patent application, Mr. Crisp did not make any disclosure to the Committee concerning any Rambus patent or patent application. (Crisp, Tr. 3316). At the meeting Mr. Crisp did not say anything at all with respect to any Rambus patent applications that might relate to CAS latency (Crisp, Tr. 3341); did not make any statements at all with respect to any pending patent applications that might relate to the use of on-chip PLL or DLL (Crisp, Tr. 3341, -44); and made no statement at all with respect to any patent applications that might relate to the use of a dual edge clock (Crisp, Tr. 3341). Mr. Crisp did not inform the Committee that the matters under discussion in connection with SDRAM standardization involved inventions that Rambus believed it owned. (CX2092 at 148, 150).

Rambus's Response to Finding No. 1082:

This proposed finding is misleading and incomplete for several reasons. First, it suggests, incorrectly, that there was some disclosure obligation in connection with survey ballots. Unlike other ballot forms, survey ballots contained no language requesting the voluntary disclosure of patent information. Rhoden, Tr. 480. Several witnesses testified that in their understanding, survey ballots were for information only and did not trigger any disclosure requirement. (Rhoden, Tr. 480, 587; Kelley, Tr. 2701; Crisp, Tr. 3517).

Second, the finding omits to note that at the JEDEC meeting just prior to the December 1995 meeting, Rambus had very clearly, and in writing, warned the committee that:

> "Our presence or silence at committee meetings does not constitute an endorsement of any proposal under the committee's consideration nor does it make any statement regarding potential infringement of Rambus intellectual property."

(RX 602 at 1; JX 27 at 4, 26). As a consequence, there could have been no reasonable or legitimate expectations on the part of JEDEC members that Rambus would disclose its intellectual property interests, if any, in response to the survey ballot and related discussions. Finally, Complaint Counsel have not met their burden of proving that Rambus had any pending patent applications that would necessarily have been infringed by any proposal being considered at the December 1995 meeting, nor have they proven that Mr. Crisp had "actual knowledge" of such applications. *See* RPF 327-396.

December 1995/January 1996 - The FTC Dell Consent And Rambus Decision to Withdraw From JEDEC

1083. In December 1995, Mr. Vincent sent Mr. Diepenbrock of Rambus materials relating to a proposed FTC consent order involving Dell Computer. (CX1990 at 1; Diepenbrock, Tr. 6222; see Rambus Answer at 34, ¶ 81). Mr. Vincent described the case as involving charges that Dell restricted competition in the personal computer industry and undermined the standard-setting process by threatening to exercise undisclosed patent rights against computer companies adopting standard technology. (CX1990 at 1).

Rambus's Response to Finding No. 1083:

Rambus has no specific response.

1084. Shortly after he forwarded to Rambus a copy of the Dell decision, Mr. Vincent and his partner, Maria Sobrino, had a luncheon meeting with Rambus CEO Tate at which they discussed the FTC's proposed consent order in the Dell matter and the downside risk of

participating in JEDEC. (CX3124 at 190-94 (Vincent, Dep.)). The downside risk was that somebody could raise the issue of equitable estoppel and argue that Rambus patents should not be enforceable. (*Id.* at 196-98). At the time Mr. Vincent discussed this downside risk, he did not know the facts as to what was going on with respect to JEDEC, and did not know the JEDEC disclosure policy. (CX3124 at 193-94 (Vincent, Dep.)).

Rambus's Response to Finding No. 1084:

The proposed finding is not supported by the weight of the evidence. First, there is no "Dell decision;" the matter was resolved through a consent order. Second, although Mr. Vincent did testify to a luncheon meeting with Mr. Tate and Ms. Sobrino, he was uncertain whether it occured before or after June 1996 and he was unsure whether the downside risk of participating in JEDEC was discussed. (CX3126, Vincent Infineon Depo., at 556).

Third, while Rambus agrees that Mr. Vincent was unaware at the time of "what was going on with respect to JEDEC," as the finding states, Rambus views that as favorable to *its* position, not that of Complaint Counsel. If Mr. Vincent had known then what the record now shows, he would likely have heavily *discounted* any "downside risk" of participating in JEDEC. He was unaware, for example, that the EIA, on behalf of JEDEC and the other EIA standards activities, had sent a letter to the FTC commenting on the *Dell* order in which it said that patent disclosures within the EIA were "encourage[d] and "voluntary," not mandatory, and that the EIA felt that "[a]llowing patented technologies in standards is procompetitive." (RX 669 at 2). Mr. Vincent would also have been interested to know that the FTC itself acknowledged the critical difference between the EIA's patent policy and that of the organization involved in the *Dell* case, for only the *latter* required a certification by participants regarding "potentially conflicting patent interests." (RX 740 at 2). The FTC explained that this difference in the patent policies meant that the "expectations of participants in the two standards-setting processes

differ." (*Id.*)

1085. In January 1996, Mr. Vincent and others from his firm met with Rambus executives to discuss the Dell decision and other matters. (CX3126 at 537 (Vincent, Dep.); Crisp, Tr. 3357; CX2082 at 807-10 (Crisp, Dep.)). Among those attending from Rambus were CEO Tate, David Mooring, Tony Diepenbrock and Richard Crisp. (CX3126 at 537 (Vincent, Dep.)). The discussion at the meeting addressed the downside risk of the Dell case, which included the risk that a patent might be held unenforceable. (*Id*. at 538-39). Attorneys for Rambus advised Rambus that it should no longer participate in any standards bodies, in part because the risks associated with such participation outweighed any benefits. (Rambus Answer at 34, ¶ 81).

Rambus's Response to Finding No. 1085:

Rambus has no specific response.

1086. Handwritten notes of Mr. Vincent from this time period (CX3126 at 543-44 (Vincent, Dep.)) reflect among a "to do" list of Rambus-related items the following notation: "No further participation in any standards body (if there has been any) – do not even get close!!" (CX1928 (emphasis in original)).

Rambus's Response to Finding No. 1086:

See RRFF 1084.

1087. Mr. Crisp recalled that the result of the meeting was a decision that Rambus should discontinue attendance at JEDEC meetings. (CX2082 at 809 (Crisp, Dep.)). An email from Mr. Crisp to CEO Tate and others at Rambus in late January 1996 stated: "So, in the future, the current plan is to go to no more JEDEC meetings due to fear that we have exposure in some possible future litigation." (CX0858 at 2; Crisp, Tr. 3358).

Rambus's Response to Finding No. 1087:

The proposed finding is incomplete and misleading. Mr. Crisp also states in the e-mail cited that "I understand the concerns about the patent policy and some potential exposure we could have in future litigation. However, court opinions I have read on the subject of Equitable Estoppel and Laches give me the feeling that these issues can be avoided by careful planning . . . ." (CX0858 at 2). This indicates that Mr. Crisp did not feel that Rambus had done

anything up to that point that might result in equitable estoppel and simply needed to engage in "careful planning" to make sure that it did not do so in the future. He also recounts in the e-mail that another conclusion from the meeting in question was that "we haven't done anything wrong . . . ." (*Id.*). This is consistent with an e-mail that Mr. Crisp wrote the previous month, in December 1995, in which he stated that he understood the conduct that could be deemed "inequitable behavior" and he was "unaware of us doing any of this or of any plans to do this." (*Id*.).

1088. The final JEDEC meeting attended by Rambus was the meeting in December 1995. (Rambus Answer at 20, ¶ 41). Thereafter Rambus continued to receive certain JEDEC mailings for some time. (*Id.*). Rambus did not pay in response to a dues invoice sent by JEDEC in January 1996. (*Id.*). Rambus responded to the dues invoice by a letter dated June 17, 1996, in which it informed JEDEC that it was not renewing its membership in the organization. (*Id.*).

Rambus's Response to Finding No. 1088:

Rambus has no specific response.

1089. One of the reasons Rambus left JEDEC was because it believed the items being discussed there looked more and more like Rambus products. (CX2112 at 202 (Mooring, FTC Dep.)). One of the features that Rambus saw involved dual edge clocking, such as was seen in the SyncLink proposal and what would eventually become DDR. (CX2112 at 205, C's 2056 at 190 (Mooring, Dep.)).

Rambus's Response to Finding No. 1089:

The proposed finding is misleading and incomplete. Mr. Mooring testified that the discussions he was referring to had not yet even reached the "first showing" stage. (CX2056, Mooring Infineon Depo., at 190). Rambus's founders believed from its inception that the techniques that they had invented would inevitably have to be used to improve DRAM performance in the future. (Farmwald, Tr. 8466; Horowitz, Tr. 8487).

1090. Equitable estoppel was another consideration in Rambus' decision to leave

JEDEC. (CX2112 at 222 (Mooring, FTC Dep.)).

Rambus's Response to Finding No. 1090:

The proposed finding is misleading and incomplete. With respect to equitable estoppel, Mr. Mooring testified only that "legal guidance not to attend JEDEC escalated" after the "situation with DELL." (CX2112, Mooring FTC Depo., at 222). The evidence shows that Rambus's lawyers felt that, although Rambus's situation was not the same as the situation in the Dell case, the risk that an equitable estoppel defense might be *raised* justified withdrawing from JEDEC, assuming that the benefits of attendance did not outweigh the risks. (CX3124, Vincent Infineon Depo. at 196-97).

As Mr. Crisp described it, Ed Taylor of the Blakeley Sokoloff firm advised Rambus that "if we could get the information we got in the JEDEC meetings and the contacts that we had there other ways, that that would be probably advisable to do that . . . [even though] we haven't done anything wrong from our discussion that we had in the room. . . . so, he recommended that, you know, unless there was a real compelling reason for us to continue staying within JEDEC, that we should get out." (Crisp, Tr. 3558-59).

1091. Another factor in the Rambus decision to leave JEDEC was its unwillingness to license its technology on RAND terms. In responding to a letter from Cheryl Rowden of the IEEE in February 1996, Rambus in-house counsel Anthony Diepenbrock stated that Rambus "had already licensed its technology and would continue to license its technology in accordance with its existing business practices. " (CX0869 at 1, responding to CX0490; Diepenbrock, Tr. 6223-6224). Mr. Diepenbrock did not agree with Ms. Rowden's interpretation of an earlier letter as suggesting that Rambus would be willing to license applicants on reasonable and non-discriminatory ("RAND") terms. (Diepenbrock, Tr. 6223-6224; CX0490 at 1). Mr. Diepenbrock testified that his view was that agreeing to RAND terms was inconsistent with Rambus' business practices. (Diepenbrock Tr. 6228) Mr. Diepenbrock also testified that one of the reasons for taking this position was because he was uncertain that every contract Rambus had signed up to that point would meet a RAND standard. (Diepenbrock, Tr. 6228). Mr. Diepenbrock also testified that, to the best of his knowledge, Rambus has never submitted a RAND letter to any

standard-setting organization, including JEDEC. (Diepenbrock, Tr. 6228-6229).

Rambus's Response to Finding No. 1091:

The proposed finding is misleading and incomplete. Mr. Diepenbrock testified that he was uncertain that every contract that Rambus had signed would meet a RAND standard simply because he had not had the opportunity to review all the contracts. (Diepenbrock, Tr. 6227 ("Well, I generally knew some of the terms in existing contracts and contracts that were being worked on that were similar, and without studying -- there were a lot of them. Without studying them, there was no way for me to be certain that all of the terms met RAND.").

Early 1996 - Rambus Obtains Its '327 Patent

1092. In the late 1995-early 1996 time period, the then-extant rule at the United States Patent Office was that applicants had 90 days after receiving a Notice of Allowability of Claims to pay the fees for the issuance of the patent or the patent application could be deemed abandoned. (Diepenbrock, Tr. 6191-6192). On January 5, 1996, Rambus outside patent counsel sent a check for $1,250.00 to the United States Patent and Trademark office for payment of issue fees relating to the '646 application, also known internally as the P001C2 application. (CX1487; Diepenbrock, Tr. 6192).

Rambus's Response to Finding No. 1092:

Rambus has no specific response.

1093. By December 1995, Rambus in-house attorney Mr. Diepenbrock, had put in place a protocol with Rambus' outside patent counsel that required that he be notified prior after the Notice of Allowance and before the payment of any issue fees. (Diepenbrock, Tr. 6192-6194) (witness acknowledges accuracy of prior deposition testimony used to refresh recollection). Mr. Diepenbrock also testified that he passed on information that claims had been allowed to Geoffrey Tate, the CEO of Rambus. (Diepenbrock, Tr. 6191).

Rambus's Response to Finding No. 1093:

Rambus has no specific response.

1094. On April 9, 1996, Rambus' outside patent counsel prepared a tracking report noting the issue date and patent number three weeks in advance of its issuance. (CX2008 at 3;

see also CX3127 at 75 (Vincent, Dep.). It is not uncommon for the patent office to provide advance notice of the issue date and patent number to parties seeking patents after a Notice of Allowance had been issued. (Diepenbrock, Tr. 6150). The '327 patent issued to Rambus on April 30, 1996. (CX1494).

Rambus's Response to Finding No. 1094:

Rambus has no specific response.

1095. The issuance of the '327 patent was a noteworthy event at Rambus. (Diepenbrock, Tr. 6194). Mr. Diepenbrock discussed the fact that the '327 patent had issued with others in Rambus, including CEO Tate, prior to June of 1996. (Diepenbrock, Tr. 6194-95).

Rambus's Response to Finding No. 1095:

Rambus has no specific response.

January 1996 - JEDEC Committee Meeting

1096. In January of 1996, the JEDEC JC-42.3 Committee held an interim meeting in Sunnyvale, California. (JX0029 at 1; Rhoden, Tr. 484). At that meeting there was additional discussion about Future SDRAM, and Micron submitted a first presentation for the use of echo clocks on the next generation of DRAMs. (JX0029 at 17-22; Lee, Tr. 6655-66).

Rambus's Response to Finding No. 1096:

Rambus has no specific response.

1097. Desi Rhoden, currently the Chairman of JEDEC, testified that the Micron presentation at the January 1996 interim meeting would trigger a disclosure obligation under the JEDEC patent disclosure policy. (Rhoden, Tr. 488-489, referencing JX0029 at 17-22).

Rambus's Response to Finding No. 1097:

The proposed finding is irrelevant. Complaint Counsel have made no showing that Rambus had any patents or patent applications relating to the Micron presentation to disclose. Moreover, the proposed finding is not supported by the weight of the evidence which shows that if any disclosure of intellectual property interests was required at JEDEC, it was required only at the time of balloting. (RPF 296-300).

1098. Mr. Crisp of Rambus did not attend this Committee meeting, but received the minutes and circulated copies to others at Rambus (Crisp, Tr. 3561) with the following observation:

> I have put copies of the JC42.3 meeting minutes in each of your mail slots. Notice the Micron presentation especially the part about the separate transmit and receive clocks. I think we should have a long hard look at our IP and if there is a problem, I believe we should tell JEDEC that there is a problem.

(CX0868 at 1). This email was sent to Rambus CEO Tate, Vice Presidents Mooring and Roberts, Intellectual Property Manager Diepenbrock, and others. (*Id.*) Mr. Crisp testified at trial that he suggested telling JEDEC if there was an IP problem raised by the Micron presentation. (Crisp, Tr. 3367). Mr. Crisp further testified that he had no information that Rambus ever told Micron or JEDEC that there was an IP problem. (Crisp, Tr. 3367-3368).

Rambus's Response to Finding No. 1098:

The proposed finding is irrelevant. As Complaint Counsel note, Mr. Crisp suggested telling JEDEC *if* there was an IP problem raised by the Micron presentation. He has testified that he did not know whether there were any Rambus intellectual property interests relating to the presentation. (Crisp, Tr. 3561-62). Complaint Counsel have introduced no evidence as to whether Rambus ever did reach the conclusion that there was a "problem" with respect to Micron's presentation and Rambus's intellectual property and, if so, whether Mr. Crisp knew it. Likewise, Complaint Counsel have introduced no evidence of a Rambus patent or patent application with claims covering the Micron presentation.

1099. Despite Mr. Crisp's suggestion that Rambus tell JEDEC if there was an IP problem raised by the Micron presentation (Crisp, Tr. 3367), Rambus never informed JEDEC of any problems relating to the Micron presentation in January 1996. (Crisp, Tr. 3367-3368; CX2112 at 255-56 (Mooring, FTC Dep.)) By January 1996, Mr. Mooring believed there was a general trend toward more Rambus "inventions" being incorporated into JEDEC presentations. (CX2112 at 256 (Mooring, FTC Dep.)).

Rambus's Response to Finding No. 1099:

The proposed finding is irrelevant for the reasons stated in RRFF 1098. Mr. Mooring's vague testimony is also irrelevant. Mr. Mooring testified that "I don't have definitive memories,but the general trend toward more of our inventions filtering their way into JEDEC presentations was a problem." (CX2112, Mooring FTC Depo. at 256). Mr. Mooring's testimony does not support the conclusion that Rambus had any patents or patent applications while it was a JEDEC member with claims covering any presentation made at JEDEC.

June 1996 - Rambus Seeks Enforcement Readiness Opinion on '327 Patent

1100. On June 17, 1996, Rambus' Mr. Diepenbrock forwarded a request for an enforcement readiness opinion to Rambus outside patent counsel Lester Vincent with respect to the '327 patent. (CX0889; Diepenbrock, Tr. 6195-6196) (enforcement readiness means an independent review of the file wrapper to determine if it was sufficient to assert claims against a possible infringer). This was the only occasion during his tenure at Rambus where Mr. Diepenbrock could recall requesting an outside opinion on the enforcement readiness of an issued Rambus patent. (Diepenbrock, Tr. 6198-6199).

Rambus's Response to Finding No. 1100:

The proposed finding is incomplete. The request for an enforcement readiness opinion related to Rambus's potential claims against Mosys. (Diepenbrock, Tr. 6202-04).

1101. In the same letter, Rambus also sought the opinion of Mr. Vincent's firm regarding whether this patent would be infringed by a device that had been described in an earlier communication with the firm. (CX0889 at 2). The prior communication sent by Mr. Diepenbrock to Mr. Vincent involved a company called Mosys, about whom Rambus was concerned with possible infringement of the '327 patent. (Diepenbrock, Tr. 6203).

Rambus's Response to Finding No. 1101:

The proposed finding is incomplete. Lester Vincent was asked by Rambus to look into the question of whether Mosys products infringed the '327 patent only after the '327 patent had

issued on April 30, 1996. (CX 3129, Vincent Micron depo. at 380-82.) In order to perform this analysis, Mr. Vincent was sent an actual Mosys DRAM, as wll as a Mosys data sheet. (*Id*. at 397-99.)

1102. Rambus documents suggest that a "competitive analysis" of the Mosys device had been prepared in January of 1996 (CX1316) and again in March of 1996 (CX1319). Richard Crisp, Rambus' JEDEC representative, attended meetings in the 1996 time frame involving representatives of Rambus and Mosys where the alleged infringement of Rambus patents by Mosys was discussed. (Crisp, Tr. 3368-3369). These discussions related, in part, to a particular implementation of dual edge clocking technology contained in a Rambus patent. (*Id.*)

Rambus's Response to Finding No. 1102:

Rambus has no specific response.

1103. Rambus CEO Tate was the person who directed Mr. Diepenbrock to study the Mosys device for possible infringement, and who sought the opinion from Mr. Vincent's firm in June 1996. (Diepenbrock, Tr. 6202, 6204). At the time Mr. Diepenbrock requested the enforcement readiness opinion of outside counsel in June of 1996, Rambus had only a data sheet and no silicon from the Mosys device but considered that to be sufficient information to seek the enforcement readiness opinion. (Diepenbrock, Tr. 6204).

Rambus's Response to Finding No. 1103:

The proposed finding is misleading and incomplete. Rambus did not form a conclusion about infringement of the '327 patent by Mosys DRAMs until an actual Mosys DRAM had been reverse-engineered and the infringement analysis completed. (Diepenbrock, Tr. 6209.) Mosys was contacted about possible infringement only after the reverse engineering was done. (Diepenbrock, Tr, 6205-06.)

1104. A facsimile sent by Mr. Diepenbrock to Mike Mallie of Mr. Vincent's firm included a diagram of the Mosys device and described the device as operating on "both edges of the clock." (CX0891 at 1). Mr. Mallie met with Mr. Diepenbrock and later advised him that him saw no problem with the enforceability of the '327 patent. (Diepenbrock, Tr. at 6205).

Rambus's Response to Finding No. 1104:

Rambus has no specific response.

1105. By mid-August 1996, Rambus informed Mosys about its infringement concerns with respect to the '327 patent. (CX0901) (correspondence between the CEO of Mosys and the CEO of Rambus, Mr. Tate, referencing a August 16, 1996 letter from Rambus to Mosys). Mosys and Rambus eventually entered into licensing negotiations that concluded with Mosys paying Rambus a royalty rate of one percent of sales. (CX0927) (royalty of $56,000 based on sales of $5.6 million).

Rambus's Response to Finding No. 1105:

The proposed finding is incomplete. Mosys was contacted about possible infringement only after (1) the '327 patent had issued, (2) a Mosys part had been reverse engineered, and (3) an infringement analysis had been completed. (RRFF 1101, 1103).

1106. Also in August 1996, shortly after having withdrawn from JEDEC, Mr. Crisp shared with others at Rambus a presentation, based in part on confidential JEDEC material, about SDRAM using double clocked data. (CCFF 1107-08).

Rambus's Response to Finding No. 1106:

The proposed finding is irrelevant and misleading. Mr. Crisp apparently shared some confidential JEDEC material, obtained while Rambus was a JEDEC member, with other Rambus personnel. To the extent that Complaint Counsel imply that this was in some way improper, they have failed to indicate how.

The proposed finding is also incomplete and misleading in stating that Rambus had withdrawn from JEDEC "shortly" before August 1996. In fact, Rambus attended its last JEDEC meeting in December 1995. (CCFF 1088). Rambus did not pay the January 1996 invoice for renewing its membership. (*Id.*). In June 1996 Rambus sent JEDEC a letter merely formalizing Rambus's separation from JEDEC. (CX0887).

1107. Mr. Crisp gave a presentation on SDRAM at a lunchtime meeting at Rambus called "the Rambler." (Crisp, Tr. 3393-95; CX1320 at 1-5; CX0905 at 1). Crisp reminded his co-workers that his Rambler presentation contained confidential JEDEC material. (Crisp, Tr. 3395; CX0905 at 1 (September 1996 email from Crisp to all Rambus staff: "One more time so that all hear: the material I presented in my Rambler contained some JEDEC material which is not permitted to be shared with any company who is not a member of JEDEC.")).

Rambus's Response to Finding No. 1107:

The proposed finding is irrelevant and misleading. (*See* RRFF 1106).

1108. Mr. Crisp's presentation discussed SDRAM using double clocked data. (CX1320 at 4 ("What about double clocked Data?" with a timing diagram referencing the rising and falling edges of a clock signal); *id*. at 5 ("Double Clocked Data (read case)" and "Double Clocked Data (write case)")).

Rambus's Response to Finding No. 1108:

The proposed finding is irrelevant and misleading. (*See* RRFF 1106).

June 1996 - Rambus Withdraws from JEDEC

1109. On June 17, 1996, Richard Crisp of Rambus sent a letter to JEDEC secretary Ken McGhee formally withdrawing from JEDEC. (CX0887 at 1; CX0888 at 1).

Rambus's Response to Finding No. 1109:

The proposed finding is incomplete and misleading. Rambus attended its last JEDEC meeting in December 1995. (CCFF 1088). Rambus did not pay the January 1996 invoice for renewing its membership. (*Id.*). In June 1996 Rambus sent JEDEC a letter merely formalizing Rambus's separation from JEDEC. (CX0887).

1110. The June 17, 1996, withdrawal letter signed by Mr. Crisp states in part:

> To the extent that anyone is interested in the patents of Rambus, I have enclosed a list of Rambus U.S. and foreign patents. Rambus has also applied for a number of additional patents in order to protect Rambus technology.

(CX0887 at 1; CX0888 at 1).

Rambus's Response to Finding No. 1110:

Rambus has no specific response.

1111. Attached to the June 17, 1996 withdrawal letter was a list of patents issued or assigned to Rambus. (CX0887 at 2; CX0888 at 2). The list contained no references to patent applications, and was not a complete list of issued patents because the '327 patent was not on the list. (CX0888 at 2; Crisp, Tr. 3381, 3384; Diepenbrock, Tr. 6200). No one at Rambus informed JEDEC about the '327 patent, either before or after it issued on April 30, 1996. (Diepenbrock, Tr. 6201-6202; Crisp, Tr. 3316).

Rambus's Response to Finding No. 1111:

The proposed finding is misleading to the extent that it suggests that the '327 patent was intentionally omitted from the list. The only evidence presented at trial on this issue showed that the '327 patent was omitted from the list by mistake. (RPF 561). The proposed finding is also irrelevant because, upon issuance, the '327 was publicly available and the evidence shows that JEDEC members were aware of it. (RX1214 at 1 (July 1998 e-mail circulating list of Rambus patents, including the '327 patent, to numerous JEDEC representatives); RX2216 at 3 (Mitsubishi chart of Rambus patents including the '327 patent)).

The proposed finding is also misleading in noting that the list contained no reference to patent applications. As Complaint Counsel have admitted, the cover letter made clear that "Rambus has also applied for a number of additional patents in order to protect Rambus technology." (CCFF1110).

1112. The date of the Rambus letter withdrawing from JEDEC, which omitted the '327 patent pertaining to dual-edge clock technology (CX0887; CX0888) is the same as the Rambus letter to outside patent counsel Lester Vincent seeking an enforcement readiness opinion with respect to the '327 patent. (CX0889 at 2).

Rambus's Response to Finding No. 1112:

The proposed finding is incomplete and misleading. The letter to JEDEC was signed by

Richard Crisp, while the letter to Lester Vincent was signed by Anthony Diepenbrock; there is no evidence of any connection between the letters.

1113. Earlier drafts of the JEDEC withdrawal letter contained language suggesting that the attached list of issued Rambus patents was complete, including the following statements: "In the spirit of full disclosure, Rambus Inc would like to bring to the attention of JEDEC all issued U. S. patents held by Rambus Inc." (CX0873 at 1) and "This list [of patents] is complete as of this writing and follows below." (CX0873 at 1; CX0874 at 1; Crisp, Tr. 3382-3383). The final June 17, 1996, withdrawal letter that was actually sent to JEDEC contained no such language. (CX0887 at 1; CX0888 at 1; Crisp, Tr. 3383-3384).

Rambus's Response to Finding No. 1113:

The proposed finding is irrelevant. (*See* RRFF 1111).

1114. None of the patents listed in the attachment to the June17, 1996, withdrawal letter (CX0888 at 2) related to JEDEC work. (CX0887 at 2; Jacob, Tr. 5365-5366, 5501-5502). The '327 patent, which was not included in the list, did relate to JEDEC work on dual-edge clocking technology. (Jacob, Tr. 5366-5367, 5545-5549, 5551-5555).

Rambus's Response to Finding No. 1114:

The proposed finding that none of the patents listed in the June 17, 1996 attachment related to JEDEC work is contradicted by more reliable evidence and is misleading for the reasons stated in RRFF 1272. The proposed finding that the '327 patent related to JEDEC work is not supported by the weight of the evidence which shows that the claims of the '327 patent did not necessarily cover either the presentations raised by Complaint Counsel or JEDEC-compliant devices. (*See* RRFF 1216-37).

Rambus Foreign Patent Activity

1115. From the earliest days of the company, Rambus planned to pursue intellectual property claims not only in the United States but in other countries as well. (CX0535 at 1 (1990 Rambus Business Plan: file a broad patent "in all major industrial nations"); *id*. at 4 ("The base patent is being filed over the next several months in the European Patent Office, Israel, Korea, Taiwan, Japan, India and Canada.")).

Rambus's Response to Finding No. 1115:

The proposed finding is irrelevant. (*See* RRFF 3183).

1116. During the time that Rambus was a JEDEC member, part of the work by Rambus patent counsel Lester Vincent on behalf of Rambus involved work on foreign patent filings, including counseling Rambus representatives with respect to the countries in which they should file patent applications. (Vincent, Tr. 7878-79; see CX1937 at 28). This included providing Rambus with a chart listing countries currently or in the future expected to be involved in semiconductor manufacturing, packaging and assembly and computer production, to help Rambus in making foreign patent filing decisions. (CX1972 at 1, 2).

Rambus's Response to Finding No. 1116:

The proposed finding is irrelevant. (*See* RRFF 3183).

1117. Rambus filed an International Patent Application under the Patent Cooperation Treaty (the PCT application) on April 16, 1991. (CX1454 at 1). The PCT application claimed priority based on the Rambus '898 U.S. application. (CX1454 at 1). A PCT application is a mechanism that permits an applicant to file with the World Intellectual Property Organization ("WIPO") an application based on a United States patent application, and thereafter enter the patent registration process in various foreign countries within a specified period. (Vincent, Tr. 7883; see CX1948).

Rambus's Response to Finding No. 1117:

The proposed finding is irrelevant. (*See* RRFF 3183).

1118. Rambus also filed an application with the European Patent Office ("EPO"). The EPO is administrative mechanism for centralized examination of patent applications for various European countries. (Vincent, Tr. 7885-86, 7894-97). Rambus pursued examination of patent applications in this fashion in the United Kingdom, France, Germany and Italy. (Vincent, Tr. 7897; RX335).

Rambus's Response to Finding No. 1118:

The proposed finding is irrelevant. (*See* RRFF 3183).

1119. Rambus attempted to conform certain independent claims in the EPO application to the amended claims being prosecuted in the United States. (Vincent, Tr. 7899).

Rambus's Response to Finding No. 1119:

The proposed finding is irrelevant. (*See* RRFF 3183). The proposed finding is also unsupported by the cited evidence and vague. The proposed finding is vague in that it is unclear as to which European application is referred to as "the EPO application." The proposed finding is also unsupported by the cited evidence, which does not establish that any modifications to any claims in the EPO were made. (Vincent, Tr. 7899-7900 ("Well, I was asking a question. I don't recall what I actually ended up doing.")).

1120. As of approximately 1995, there were Rambus patent applications based on the original Rambus '898 patent application pending with the EPO (Vincent, Tr. 7885-86), the WIPO (Vincent, Tr. 7883), India (Vincent, Tr. 7882), Israel (Vincent, Tr. 7885), Japan (Vincent, Tr. 7886-87) and Korea (Vincent, Tr. 7887). As of that time, Rambus had also been issued a patent in Taiwan based on the specification contained in the original Rambus '898 patent application. (Vincent, Tr. 7883-85). (See also CX1982).

Rambus's Response to Finding No. 1120:

The proposed finding is irrelevant. (*See* RRFF 3183). Moreover, the WIPO application filed in 1991 was no longer pending in 1995 as it expired at the end of the "waiting period" at which time you "enter various foreign countries at the end of the period." (Vincent, Tr. 7883).

1121. Complaint Counsel has limited information regarding the prosecution of Rambus's foreign patents because Respondent has asserted attorney-client privilege with respect to work involving foreign patent filings. (Vincent, Tr. 7879). There are over fifty communications regarding Rambus's foreign patent filings between 1991 and 1996 that were not produced to Complaint Counsel because Respondent asserted the attorney-client privilege. (Steinberg Motion *In Limine*, Attachment 9, Rambus Privilege Log Entries 114, 116-27, 129, 138-48, 150-51, 174-76, 187-89, 239-47, 260-64, 619, 623, 631-32, 759, 1120, 1122-24, 1126-27, 1177).

Rambus's Response to Finding No. 1121:

The proposed finding is irrelevant. (*See* RRFF 3183).

C. During the Time That It Was A JEDEC Member, Rambus Possessed United States Patents Or Patent Applications That Read On The Four Relevant

JEDEC Standard Technologies At Issue In This Case.

1122. Every patent that Rambus has asserted against SDRAM and DDR SDRAM products in patent litigation resulted from continuation or divisional patent applications flowing from the original '898 application. The asserted patents claim the benefit of the '898 application's April 18, 1990 filing date. (First Stipulation, no. 22; Exhibit A to First Stipulation, no. 22; Nusbaum Tr. 1506-1508; *see also* DX0014).

Rambus's Response to Finding No. 1122:

Rambus has no specific response.

1123. Moreover, every patent that Rambus has asserted in patent litigation can trace its lineage to one of two patent applications in the '898 family: either the 08/222,646 ("'646") or the 07/847,961 ("'961"). (First Stipulations, No. 22; Exhibit A to First Stipulations, No. 22; Nusbaum Tr. 1506-1508; *see also* DX0014).

Rambus's Response to Finding No. 1123:

The proposed finding is misleading. The fact that a patent application traces its lineage back to another patent application does not in any way suggest that the subject matter of its claims is related to the subject matter of the claims of the prior patent application, except that both must be supported by the same written description. (See RPF 78, 83-85). The proposed finding is also misleading to the extent that it suggests that the '646 and '961 applications are unique in this respect. In fact, every patent that Rambus has asserted in patent litigation can trace its lineage to various other combinations of two patents applications, such as, for example, applications 08/798,525 and 07/954,945. (*See* Stipulated Patent Tree).

1124. Rambus was a member of JEDEC from December 1991 until June 1996. (CCFF 878, 1109). The '898, '646 and '961 applications were pending while Rambus was a member of JEDEC. (First Stipulations, No. 22; Exhibit A to First Stipulations, No. 22; *see also* DX0014).

Rambus's Response to Finding No. 1124:

The proposed finding is misleading and incomplete. Rambus attended its last JEDEC

meeting in December 1995 and did not pay the January 1996 invoice for renewing its membership. (CCFF 1088). In June 1996, Rambus sent a letter to JEDEC simply formalizing its separation from JEDEC. (CX0887).

1. The Rambus '961 Patent Application Contained Claims Covering Programmable CAS Latency and Programmable Burst Length.

1125. Rambus patent application 07/847,961 (the '961 application) contained claims covering, or that a reasonable engineer could interpret as covering, the programmable burst length and programmable CAS latency features of JEDEC-compliant SDRAMs. (Nusbaum, Tr. 1540-72; Jacob, Tr. 5507-28).

Rambus's Response to Finding No. 1125:

The proposed finding is incorrect. The Federal Circuit, the appellate court charged with interpreting patent claims, expressly considered the claims of the '961 application and held:

> This court has examined the claims of the cited applications [which include the '961 application] as well as the relevant portions of the SDRAM standard. Based on this review, this court has determined that substantial evidence does not support the finding that these applications had claims that read on the SDRAM standard.

Rambus Inc. v. Infineon Technologies AG, 318 F.3d 1081, 1103 (Fed. Cir. 2003). The court went on to hold that a license under the claims of the '961 application "would not be necessary to practice the SDRAM standard." (*Id.*) It follows that a reasonable engineer would not interpret the claims of the '961 application as covering JEDEC-compliant SDRAMs. The Federal Circuit interprets claims from the viewpoint of a person of ordinary skill in the art to which the patent application pertains, such as an engineer. (*Id.* at 1088 ("a claim term means 'what one of ordinary skill in the art at the time of the invention would have understood the term to mean.'")

Thus, the Federal Circuit has held that a person of ordinary skill, such as an engineer, would not interpret the claims of the '961 application as reading on the SDRAM standard. As set forth in Rambus's Initial Post-Trial Brief, this Court is bound by the Federal Circuit's opinion regarding the scope of claims in the '961 application. (Rambus's Initial Post-Trial Brief at 55-57).

1126. Rambus filed the '961 application in the PTO on March 5, 1992. (Nusbaum, Tr. 1542; CX1504-019). As filed, the '961 application contained claims 95-105 of the original 150 claims submitted with the '898 parent patent application. (Nusbaum, Tr. 1542-43; CX1504-173-175).

Rambus's Response to Finding No. 1126:

Rambus has no specific response.

1127. The patent examiner issued a first Office Action in the '961 application on September 6, 1994. (Nusbaum, Tr. 1544; CX1504-208). In response to that Office Action, Rambus submitted an Amendment on January 6, 1995, cancelling the original claims and adding new ones. (Nusbaum, Tr. 1543-44; CX1504-216). The January 6, 1995, Amendment was Rambus's first change to the '961 application. (Nusbaum, Tr. 1544).

Rambus's Response to Finding No. 1127:

The proposed finding is incomplete. The claims relied on by Complaint Counsel that were added to the '961 application on January 6, 1995 were cancelled on June 23, 1995. (CX1504 at 258; Fliesler, Tr. 8847-48).

(A) Claim 160 of the '961 Application

1128. Claim 160 of the '961 application recites:

> [1] In a memory storage system including a bus, a semiconductor device
>
> [2] having that [sic] is configurable by a device that is external to the semiconductor device, comprising:
>
> [3] at least one pin for coupling the semiconductor device to the

bus; and

[4] at least one register operative to store information

[5] specifying a manner in which the semiconductor device is to respond to transaction requests received from the bus,

[6] . . .wherein the information is received by the semiconductor device from the bus when the semiconductor device is configured, the semiconductor device storing the information received from the bus lines in the register during configuration of the semiconductor device

[7] and thereafter responding to transaction requests in the manner specified by the information stored in the register.

(CX1504 at -221-22) (numbering added).

Rambus's Response to Finding No. 1128:

Rambus has no specific response.

1129. An SDRAM compliant with Release 4 of the JEDEC SDRAM standard (JX0056) contains each limitation of claim 160 of the '961 application. (Nusbaum, Tr. 1550-55).

Rambus's Response to Finding No. 1129:

The proposed finding is incorrect. As discussed above, this Court is bound by the Federal Circuit's determination that substantial evidence does not support the proposition that the '961 application had claims reading on the SDRAM standard, that is, each claim of the '961 application, including claim 160, has limitations that are not contained in SDRAM. (*See* RRFF 1125).

1130. A reasonable engineer could construe claim 160 to cover both the programmable CAS latency and the programable burst length features of an SDRAM compliant with Release 4 of the JEDEC SDRAM standard. (Jacob, Tr. 5507-17).

Rambus's Response to Finding No. 1130:

The proposed finding is inaccurate. As discussed above, this Court is bound by the Federal Circuit's determination that, as understood by a person of ordinary skill in the art, such as an engineer, the claims of the '961 application would not read on the SDRAM standard. (*See* RRFF 1125).

1131. A JEDEC-compliant SDRAM is a semiconductor device operating in a memory storage system including a bus. Therefore, it satisfies element [1] of claim 160. (JX0056at 1, 103, 134, 141; (Nusbaum, Tr. 1551; Jacob, Tr. 5509).

Rambus's Response to Finding No. 1131:

As set forth above, this Court is bound by the Federal Circuit's determination of the scope of claim 160 and should not accept Complaint Counsel's invitation to reinterpret that claim. (*See* RRFF 1125).

1132. A JEDEC-compliant SDRAM is configured by an external bus controller, such as a central processing unit (CPU). Therefore, it satisfies element [2] of claim 160. (JX0056 at 114-16; Nusbaum, Tr. 1552; Jacob, Tr. 5510).

Rambus's Response to Finding No. 1132:

As set forth above, this Court is bound by the Federal Circuit's determination of the scope of claim 160 and should not accept Complaint Counsel's invitation to reinterpret that claim. (*See* RRFF 1125).

1133. A JEDEC-compliant SDRAM has pins for connecting the SDRAM to the bus. Therefore, it satisfies element [3] of claim 160. (JX0056 at 106, 141; Nusbaum, Tr. 1552; Jacob, Tr. 5510).

Rambus's Response to Finding No. 1133:

As set forth above, this Court is bound by the Federal Circuit's determination of the scope

of claim 160 and should not accept Complaint Counsel's invitation to reinterpret that claim. (*See* RRFF 1125).

1134. A JEDEC-compliant SDRAM contains a mode register that stores information. Therefore, it satisfies element [4] of claim 160. (JX0056 at 114; (Nusbaum, Tr. 1552-53; Jacob, Tr. 5510-11).

Rambus's Response to Finding No. 1134:

As set forth above, this Court is bound by the Federal Circuit's determination of the scope of claim 160 and should not accept Complaint Counsel's invitation to reinterpret that claim. (*See* RRFF 1125).

1135. The information stored in a JEDEC-compliant SDRAM's mode register specifies burst length, burst type and latency mode. (JX0056 at 114). The burst length, burst type and latency mode specify the manner in which the SDRAM responds to transaction requests, i.e., read and write requests. (JX0056 at 114-16, 120, 121). Therefore, a JEDEC-compliant SDRAM satisfies element [5] of claim 160. (Nusbaum, Tr. 1553; Jacob, Tr. 5511-12).

Rambus's Response to Finding No. 1135:

As set forth above, this Court is bound by the Federal Circuit's determination of the scope of claim 160 and should not accept Complaint Counsel's invitation to reinterpret that claim. (*See* RRFF 1125).

1136. A JEDEC-compliant SDRAM receives burst length, burst type and latency information from the bus and stores it in the mode register "after power-on and before normal operation," when the SDRAM is configured. (J00X56 at 114). Therefore, it satisfies element [6] of claim 160. (Nusbaum, Tr. 1543-54; Jacob, Tr. 5512).

Rambus's Response to Finding No. 1136:

As set forth above, this Court is bound by the Federal Circuit's determination of the scope of claim 160 and should not accept Complaint Counsel's invitation to reinterpret that claim. (*See* RRFF 1125).

1137. A JEDEC-compliant SDRAM responds to transaction requests (read and write requests) in the manner specified by the burst type, burst length and latency information stored in its mode register. (JX0056 at 114, 120, 121). Therefore, it satisfies element [7] of claim 160. (JX0056 at 114; Nusbaum, Tr. 1554-55; Jacob, Tr. 5512-13).

Rambus's Response to Finding No. 1137:

As set forth above, this Court is bound by the Federal Circuit's determination of the scope of claim 160 and should not accept Complaint Counsel's invitation to reinterpret that claim. (*See* RRFF 1125).

1138. Claim 160 of the '961 application contains no language requiring a device identifier feature. (Nusbaum, Tr. 1561; Jacob, Tr. 5523).

Rambus's Response to Finding No. 1138:

The proposed finding is incorrect. The Federal Circuit has held that "claims in the '961 application were limited to the device identifier feature" that is not "present in the SDRAM standard." (*Rambus Inc. v. Infineon Technologies AG*, 318 F.3d 1081, 1103 (Fed. Cir. 2003)).

1139. The '961 application does contain claims that recite a device identifier feature. (CX1504 at 219-223; Nusbaum, Tr. 1562). For example, claim 161 recites "an identification register" which stores "an identification number that uniquely identifies the semiconductor device." (CX1504 at 222). The fact that claim 161 contains this limitation suggests that claim 160 should not be interpreted to require a device identifier feature because proper dependant claims (i.e., claim 161) should be understood as adding limitations to their independent claims (i.e., claim 160). (Nusbaum, Tr. 1562; Fliesler, Tr. 8941).

Rambus's Response to Finding No. 1139:

As set forth above, this Court is bound by the Federal Circuit's determination of the scope of claim 160 and should not accept Complaint Counsel's invitation to reinterpret that claim. (*See* RRFF 1125, 1138).

(B) Claim 164 of the '961 Application

1140. Claim 164 of the '961 application recites:

[1] The semiconductor device of 160,

[2] wherein the register is an access-time register and the information is a value indicative of an access time for the semiconductor device, the semiconductor device being operative to wait for the access time before using the bus

[3] in response to a transaction request specifying the semiconductor device.

(CX1504-223) (numbering added).

Rambus's Response to Finding No. 1140:

Rambus has no specific response.

1141. An SDRAM compliant with Release 4 of the JEDEC SDRAM standard (JX0056) contains each limitation of claim 164 of the '961 application. (Nusbaum, Tr. 1555).

Rambus's Response to Finding No. 1141:

The proposed finding is incorrect. As discussed above, this Court is bound by the Federal Circuit's determination that substantial evidence does not support the proposition that the '961 application had claims reading on the SDRAM standard, that is, each claim of the '961 application, including claim 164, has limitations that are not contained in SDRAM. (*See* RRFF 1125).

1142. A reasonable engineer could construe claim 164 to cover the programmable CAS latency features of an SDRAM compliant with Release 4 of the JEDEC SDRAM standard. (Jacob, Tr. 5523-25).

Rambus's Response to Finding No. 1142:

The proposed finding is incorrect. As discussed above, this Court is bound by the Federal Circuit's determination that, as understood by a person of ordinary skill in the art, such as an engineer, the claims of the '961 application would not read on the SDRAM standard. (*See* RRFF

1125).

1143. Because claim 164 is dependant upon claim 160, it includes the limitations of claim 160. (Nusbaum, Tr. 1555). An SDRAM compliant with JEDEC release 4 satisfies the limitations of claim 160, as explained above, and therefore satisfies element [1] of claim 164. (Nusbaum, Tr. 1555).

Rambus's Response to Finding No. 1143:

As set forth above, this Court is bound by the Federal Circuit's determination of the scope of claim 164 and should not accept Complaint Counsel's invitation to reinterpret that claim. (*See* RRFF 1125).

1144. Paragraph 1144 is unused.

1145. A JEDEC-compliant SDRAM contains a mode register that specifies the CAS latency, which satisfies claim 164's requirement for an "access-time register" and "a value indicative of an access time." (JX0056 at 114). Therefore, the SDRAM satisfies element [2] of claim 164. (Nusbaum, Tr. 1555; Jacob, Tr. 5524).

Rambus's Response to Finding No. 1145:

As set forth above, this Court is bound by the Federal Circuit's determination of the scope of claim 164 and should not accept Complaint Counsel's invitation to reinterpret that claim. (*See* RRFF 1125).

1146. A JEDEC-compliant SDRAM outputs data in response to a transaction request (a read request) after waiting a time specified by the CAS latency. (JX0056 at 114, 121). A read request specifies the SDRAM through the chip select line. (JX0056 at 21, 121). Therefore, the SDRAM satisfies element [3] of claim 164. (Nusbaum, Tr. 1559-60; Jacob, Tr. 5524-25).

Rambus's Response to Finding No. 1146:

As set forth above, this Court is bound by the Federal Circuit's determination of the scope of claim 164 and should not accept Complaint Counsel's invitation to reinterpret that claim. (*See* RRFF 1125).

1147. Claim 164 of the '961 application contains no language requiring a device identifier feature. (Nusbaum, Tr. 1562; Jacob, Tr. 5525).

Rambus's Response to Finding No. 1147:

The proposed finding is incorrect. The Federal Circuit has held that "claims in the '961 application were limited to the device identifier feature" that is not "present in the SDRAM standard." (*Rambus Inc. v. Infineon Technologies AG*, 318 F.3d 1081, 1103 (Fed. Cir. 2003)).

(C) Claim 151 of the '961 Application

1148. Claim 151 of the '961 application recites:

> A computer system comprising:
>
> a bus including bus lines for carrying data;
>
> a bus master coupled to the bus; and
>
> a plurality of semiconductor devices coupled to the bus, each semiconductor device comprising:
>
> at least one register operative to store information specifying a manner in which the semiconductor device is to respond to transaction requests received from the bus,
>
> wherein the bus master transmits the information to the semiconductor device via the bus lines of the bus when the bus is configured,
>
> the semiconductor device storing the information received from the bus lines in the register during bus configuration and thereafter responding to transaction requests according to the information stored in the register.

(CX1504 at 218-19).

Rambus's Response to Finding No. 1148:

Rambus has no specific response.

1149. A reasonable engineer could construe claim 151 of the '961 application to cover a computer system incorporating an SDRAM that complied with Release 4 of the JEDEC SDRAM standard (JX0056). (Jacob, Tr. 5526).

Rambus's Response to Finding No. 1149:

The proposed finding is incorrect. As discussed above, this Court is bound by the Federal Circuit's determination that, as understood by a person of ordinary skill in the art, such as an engineer, the claims of the '961 application would not read on the SDRAM standard. (*See* RRFF 1125).

1150. A computer system incorporating an SDRAM that complied with Release 4 of the JEDEC SDRAM standard (JX56) would contain every limitation of claim 151 of the '961 patent. (Nusbaum, Tr. 1565-68).

Rambus's Response to Finding No. 1150:

The proposed finding is incorrect. As discussed above, this Court is bound by the Federal Circuit's determination that substantial evidence does not support the proposition that the '961 application had claims reading on the SDRAM standard, that is, each claim of the '961 application, including claim 151, has limitations that would not be contained in an SDRAM. (*See* RRFF 1125).

1151. The limitation of claim 151 "at least one register operative to store information specifying a manner in which the semiconductor device is to respond to transaction requests ..." is similar to limitations of claim 160. A JEDEC compliant SDRAM would satisfy this limitation in claim 151 for the same reasons it satisfies the similar limitation of claim 160. (Nusbaum, Tr. 1567-68).

Rambus's Response to Finding No. 1151:

As set forth above, this Court is bound by the Federal Circuit's determination of the scope of claim 151 and should not accept Complaint Counsel's invitation to reinterpret that claim. (*See* RRFF 1125).

1152. The scope of claim 151 is similar to the scope of claim 160 of the '961 application in that claim 151 covers a computer system incorporating a memory storage system similar to that recited in claim 160. (Jacob, Tr. 5526).

Rambus's Response to Finding No. 1152:

Rambus has no specific response.

1153. Claim 151 contains no language referring to a device identifier feature. (CX1504-218-19).

Rambus's Response to Finding No. 1153:

The proposed finding is incorrect. The Federal Circuit has held that "claims in the '961 application were limited to the device identifier feature" that is not "present in the SDRAM standard." (*Rambus Inc. v. Infineon Technologies AG*, 318 F.3d 1081, 1103 (Fed. Cir. 2003)).

(D) Claim 159 of the '961 Application

1154. Claim 159 of the '961 application recites:

> The computer system of 151, wherein the register is an access-time register operative to store a value indicative of an access time for the semiconductor device, the semiconductor device being operative to wait for the access time before using the bus in response to a request specifying the semiconductor device.

(CX1504 at 221).

Rambus's Response to Finding No. 1154:

Rambus has no specific response.

1155. Claim 159 covers a JEDEC-compliant SDRAM used in a computer system. (Nusbaum, Tr. 1570).

Rambus's Response to Finding No. 1155:

The proposed finding is incorrect. As discussed above, this Court is bound by the Federal Circuit's determination that substantial evidence does not support the proposition that the

‘961 application had claims reading on the SDRAM standard. (See RRFF 1125).

1156. The limitation of claim 159 requiring “an access-time register operative to store a value indicative of an access time for the semiconductor device” is similar to a limitation in claim 164 of the ‘961 application. (Nusbaum, Tr. 1569-70). A JEDEC-compliant SDRAM having a mode register which stores CAS latency information satisfies this limitation. (Nusbaum, Tr. 1570).

Rambus’s Response to Finding No. 1156:

As set forth above, this Court is bound by the Federal Circuit’s determination of the scope of claim 159 and should not accept Complaint Counsel’s invitation to reinterpret that claim. (*See* RRFF 1125).

1157. Claim 159 contains no language referring to a device identifier feature. (CX1504 at 221).

Rambus’s Response to Finding No. 1157:

The proposed finding is incorrect. The Federal Circuit has held that “claims in the ’961 application were limited to the device identifier feature” that is not “present in the SDRAM standard.” (*Rambus Inc. v. Infineon Technologies AG*, 318 F.3d 1081, 1103 (Fed. Cir. 2003)).

(E) Claim 165 of the ‘961 Application

1158. Claim 165 of the ‘961 application recites:

> In computer system, a method for configuring operation of a semiconductor device coupled to the bus,
>
> coupling a value to the bus by a bus master that it coupled to the bus, the value specifying a manner in which the semiconductor device is to respond to transaction requests after the semiconductor device is configured; and
>
> writing the value to a register of the semiconductor device by the semiconductor device.

(CX1504 at 223).

Rambus's Response to Finding No. 1158:

Rambus has no specific response.

1159. Claim 165 of the '961 application covers the method by which a computer system's bus master stores information in the mode register of a JEDEC-compliant SDRAM that specifies the manner in which the SDRAM responds to transaction requests. (Nusbaum, Tr. 1570-71).

Rambus's Response to Finding No. 1159:

The proposed finding is incorrect. As discussed above, this Court is bound by the Federal Circuit's determination that substantial evidence does not support the proposition that the '961 application had claims reading on the SDRAM standard. (See RRFF 1125).

1160. A reasonable engineer could conclude that claim 165 covers the method of storing CAS latency information in the mode register of an SDRAM, as described Release 4 of the JEDEC SDRAM standard. (Jacob, Tr. 5527).

Rambus's Response to Finding No. 1160:

The proposed finding is incorrect. As discussed above, this Court is bound by the Federal Circuit's determination that, as understood by a person of ordinary skill in the art, such as an engineer, the claims of the '961 application would not read on the SDRAM standard. (*See* RRFF 1125).

1161. A reasonable engineer would conclude that claim 165 covers the method of programming burst length as described Release 4 of the JEDEC SDRAM standard. (Jacob, Tr. 5527-28).

Rambus's Response to Finding No. 1161:

The proposed finding is incorrect. As discussed above, this Court is bound by the Federal Circuit's determination that, as understood by a person of ordinary skill in the art, such as

an engineer, the claims of the '961 application would not read on the SDRAM standard. (*See* RRFF 1125).

(F) Claim 168 of the '961 Application

1162. Claim 168 of the '961 Application recites:

> The method of claim 165, wherein the value specifies value specifies [sic] an access time for the semiconductor device, the method comprising the further step of the semiconductor device waiting for the access time before using the bus to respond to a transaction request that specifies the semiconductor device.

(CX1504 at 224).

Rambus's Response to Finding No. 1162:

Rambus has no specific response.

1163. Claim 168 covers the method used with a JEDEC-complaint SDRAM of programming the CAS latency value in the SDRAM's mode register and having the SDRAM wait the CAS latency period before using the bus. (Nusbaum, Tr. 1571-72).

Rambus's Response to Finding No. 1163:

The proposed finding is incorrect. As discussed above, this Court is bound by the Federal Circuit's determination that substantial evidence does not support the proposition that the '961 application had claims reading on the SDRAM standard. (See RRFF 1125).

2. The Rambus '490 Patent Application Contained Claims Covering JEDEC-Compliant SDRAM.

1164. Rambus patent application no. 08/469,490 (the '490 application) contained claims covering, or that a reasonable engineer could interpret as covering, a JEDEC-compliant SDRAM, the use of such an SDRAM, and a computer system incorporating a JEDEC-compliant SDRAM. (Nusbaum, Tr. 1573-1578; Jacob, Tr. 5528-32).

Rambus's Response to Finding No. 1164:

The proposed finding is incorrect. Claim analysis is done from the perspective of a

person of ordinary skill in the art. (Fliesler, Tr. 8778). In this case, a person of ordinary skill in the art would be an engineer. (Fliesler, Tr. 8778-79; Nusbaum, Tr. 1613). Complaint Counsel's expert agrees with Rambus's expert that the claims of the '490 application are similar to the claims of the '961 application that the Federal Circuit held did not read on the SDRAM standard from the persepective of a person of ordinary skill in the art. (Fliesler, Tr. 8855; Nusbaum, Tr. 1572, 1630; RPF 364). Moreover, as set forth below, from the perspective of a person of ordinary skill in the art, each of the claims is limited to devices containing a device identifier feature not found in SDRAMs. (Fliesler, Tr. 8943-44).

1165. Rambus filed the '490 application on June 6, 1995. (CX1504 at 246; Nusbaum, Tr. 1572). The '490 application is a continuation of the '961 application. (Nusbaum, Tr. 1572). Rambus filed claims 183-185 in the '490 application on June 23, 1995. (CX1504 at 258-271; Nusbaum, Tr. 1572-73).

Rambus's Response to Finding No. 1165:

The proposed finding is incomplete. Claims 183-185 were withdrawn from further consideration as of November 27, 1995 pursuant to a PTO restriction requirement. (CX1504 at 274-75; Fliesler, Tr. 8853-54).

(A) Claim 183 of the '490 Application

1166. Claim 183 of the '490 patent recites:

> [1] A computer system comprising:
> a bus; a semiconductor device coupled to the bus,
>
> [2] the semiconductor device comprising an access-time register operative to store a value indicative of an access time for the semiconductor device;
>
> [3] a bus master coupled to the bus, the bus master transmitting the value to the semiconductor device via the bus, the semiconductor device storing the value in the access-time register,

[4] the semiconductor device thereafter being operative to wait for the access time before using the bus in response to a request specifying the semiconductor device.

(CX1504 at 264-65) (numbering added).

Rambus's Response to Finding No. 1166:

Rambus has no specific response.

1167. Claim 183 covers a computer system incorporating a JEDEC-compliant SDRAM having programmable CAS latency. (Nusbaum, Tr. 1580-81). A reasonable engineer could construe claim 183 of the '490 patent to cover a computer system using a JEDEC-compliant SDRAM. (Jacob, Tr. 5528-30).

Rambus's Response to Finding No. 1167:

The proposed finding is incorrect for the reasons set forth in RRFF 1164 and 1171.

1168. A JEDEC-compliant SDRAM operates in a computer system having a bus. Therefore a computer system incorporating a JEDEC-compliant SDRAM satisfies element [1] of claim 183. (JX56 at 164; Jacob, Tr. 5529).

Rambus's Response to Finding No. 1168:

Rambus has no specific response.

1169. A JEDEC-compliant SDRAM has a mode register which stores CAS latency (access time) information. Therefore a computer system incorporating a JEDEC-compliant SDRAM satisfies element [2] of claim 183. (JX56 at 114; Jacob, Tr. 5529).

Rambus's Response to Finding No. 1169:

Rambus has no specific response.

1170. A JEDEC-compliant SDRAM has a mode register which stores CAS latency (access time) information which it receives from a bus master over the bus. Therefore a computer system incorporating a JEDEC-compliant SDRAM satisfies element [3] of claim 183. (JX56 at 114; Jacob, Tr. 5529-30).

Rambus's Response to Finding No. 1170:

Rambus has no specific response.

1171. A JEDEC-compliant SDRAM waits for the CAS latency time before using the bus in response to a read request. Therefore a computer system incorporating a JEDEC-compliant SDRAM satisfies element [4] of claim 183. (JX56 at 114; Jacob, Tr. 5530).

Rambus's Response to Finding No. 1171:

The proposed finding is incorrect. The '898 application teaches that semiconductor devices are specified using device identification information incorporated in a request. (*See* CCPF 1296 ("The invention described in the '898 specification has 'no need for separate device-select lines since device-select information for each device on the bus is carried over the bus.' (CX1451 at 14)"). According to Complaint Counsel's technical expert, this indicates that the bus system described in the '898 specification does not have a chip select network for indicating which chips should respond to commands. (Jacob, Tr. 5495-96). Element [4] of the claim requires that the semiconductor device respond "to a request specifying the semiconductor device," which restricts the claim in a way that teaches away from separate chip select lines that can be used to specify a semiconductor device in a manner separate from the request itself.

Claim terms are not to be interpreted in a vacuum, but in light of the specification. (Nusbaum, Tr. 1517). The limitation of claim 183, that the semiconductor device "respond to a request specifying" it, when read in light of the specification as required, limits the claim to devices having a device identifier feature with no separate chip select network. SDRAMs do have such a "separate chip-select network" (CCPF 1297), and, therefore do not satisfy element [4] of claim 183. (*See* Fliesler, Tr. 8943-44 (testifying that claim 183 is limited to devices with Rambus's device identifier feature)).

1172. Claim 183 contains no limitation requiring a device identification feature. (CX1504 at 264-65; Nusbaum, Tr. 1575-77; Jacob, Tr. 5530-31).

Rambus's Response to Finding No. 1172:

The proposed finding is incorrect. The limitation that the semiconductor device "respond to a request specifying the semiconductor device," read in light of the specification, requires a device identification feature. (RRFF 1171).

(B) Claim 184 of the '490 Application

1173. Claim 184 of the '490 application recites:

> [1] A semiconductor device having an access time that is programable, comprising:
>
> [2] at least one pin for coupling the semiconductor device to a bus; and
>
> [3] at least one access-time register operative to store a value indicative of the access time for the semiconductor device, wherein the value is received by the memory device from the bus, the semiconductor device storing the value in the access-time register,
>
> [4] the semiconductor device thereafter being operative to wait for the access time before using the bus in response to a request specifying the semiconductor device.

(CX1504 at 265) (numbering added).

Rambus's Response to Finding No. 1173:

Rambus has no specific response.

1174. An SDRAM compliant with Release 4 of the JEDEC SDRAM standard (JX56) contains each limitation of claim 184 of the '490 application. (Nusbaum, Tr. 1574-75). A reasonable engineer could construe claim 184 to cover the programmable CAS latency feature of an SDRAM compliant with Release 4 of the JEDEC SDRAM standard. (Jacob, Tr. 5531).

Rambus's Response to Finding No. 1174:

The proposed finding is incorrect for the reasons set forth in RRFF 1164 and 1178.

1175. A JEDEC-compliant SDRAM is a semiconductor device having an access time, CAS latency, that is programable. Therefore, it satisfies element [1] of claim 184. (JX56 at 114; (Nusbaum, Tr. 1574; Jacob, Tr. 5531).

Rambus's Response to Finding No. 1175:

Rambus has no specific response.

1176. A JEDEC-compliant SDRAM has pins for connecting to the bus. Therefore, it satisfies element [2] of claim 184. (JX56 at 141; Nusbaum, Tr. 1574).

Rambus's Response to Finding No. 1176:

Rambus has no specific response.

1177. A JEDEC-compliant SDRAM has a mode register which stores a CAS latency value received from the bus. Therefore, it satisfies element [3] of claim 184. (JX56 at 114; Nusbaum, Tr. 1574-75).

Rambus's Response to Finding No. 1177:

Rambus has no specific response.

1178. The CAS latency (access time) causes a JEDEC-compliant SDRAM to wait a specified time before using the bus in response to a read request. Therefore, the SDRAM satisfies element [4] of claim 184. (JX56 at 114; Nusbaum, Tr. 1574-75).

Rambus's Response to Finding No. 1178:

The proposed finding is incorrect. Element [4] of claim 184, like claim 183, requires that the semiconductor device respond "to a request specifying the semiconductor device." Therefore, claim 184 is limited to devices containing a device identifier feature not found in SDRAMs for the same reasons as claim 183. (RRFF 1171.)

1179. Claim 184 contains no limitation requiring a device identification feature. (CX1504 at 265; Nusbaum, Tr. 1577; Jacob, Tr. 5530-31).

Rambus's Response to Finding No. 1179:

The proposed finding is incorrect. The limitation that the semiconductor device "respond to a request specifying the semiconductor device," read in light of the specification, requires a device identification feature. (RRFF 1171, 1178).

(C) Claim 185 of the '490 Application

1180. Claim 185 of the '490 application recites:

> A method for programming an access time of a semiconductor device, comprising:
>
> coupling a value to a bus by a bus master that is coupled to the bus, the value specifying an access time for the semiconductor device;
>
> the semiconductor device receiving the value from the bus;
>
> writing the value to an access-time register of the semiconductor device; and
>
> the semiconductor device thereafter responding to transaction request that specify the semiconductor device by waiting the access time before using the bus.

(CX1504 at 265-66).

Rambus's Response to Finding No. 1180:

Rambus has no specific response.

1181. Claim 185 covers the method of programming the CAS latency value in the mode register of a JEDEC-compliant SDRAM that is inherent in the operation of the SDRAM. Therefore, claim 185 cover the use of an SDRAM compliant with Release 4 of the JEDEC SDRAM standard. (Nusbaum, Tr. 1576-77). A reasonable engineer could construe claim 185 to cover the use of the programmable CAS latency feature of a JEDEC-compliant SDRAM. (Jacob, Tr. 5531-32).

Rambus's Response to Finding No. 1181:

The proposed finding is incorrect for the reasons set forth in Responses to Findings Nos.

1164. Claim 185, like claim 183, requires that the semiconductor device respond to requests "that specify the semiconductor device." Therefore, claim 185 is limited to devices containing a device identifier feature not found in SDRAMs for the same reasons as claim 183. (RRFF 1171.)

1182. Claim 185 contains no limitation requiring a device identification feature. (CX1504 at 265-66; Nusbaum, Tr. 1576-77; Jacob, Tr. 5530-31).

Rambus's Response to Finding No. 1182:

The proposed finding is incorrect. The limitation that the semiconductor device respond to requests that "specify the semiconductor device," read in light of the specification, requires a device identification feature. (RRFF 1171, 1181).

3. The Rambus '692 Patent Application Contained Claims Covering A Phase-Lock Loop Incorporated Into JEDEC-Compliant SDRAM.

1183. Rambus patent application 07/847,692 (the '692 application) contained claims covering, or that a reasonable engineer could interpret as covering, a phase lock loop (PLL) incorporated into a JEDEC-complaint SDRAM. (Nusbaum, Tr. 1582-95; Jacob, Tr. 5533-41).

Rambus's Response to Finding No. 1183:

The proposed finding is incorrect and not supported by the evidence. Neither Mr. Nusbaum nor Dr. Jacob testified that the '692 application contained claims covering a PLL incorporated into a JEDEC-compliant SDRAM in general. Rather, each testified only that the '692 application contained certain claims that would cover a particular implementation of a PLL incorporated into a JEDEC-compliant SDRAM as purportedly set forth in a September 1994 NEC presentation. (As set forth below, Mr. Nusbaum and Dr. Jacob are incorrect even as to this more limited conclusion.)

1184. Rambus filed the '692 application in the PTO on March 5, 1992 as a divisional application of the '898 application. (CX1502-177; Nusbaum, Tr. 1582). As filed, the '692 application contained claims 73-81 of the original 150 claims submitted with the '898 parent

patent application. (CX1502 at 194; Nusbaum, Tr. 1583). However, on June 28, 1993, Rambus filed a Preliminary Amendment in which it canceled claims 73-81 and added new claims 151-165. (CX1504 at 205-213; Nusbaum, Tr. 1584).

Rambus's Response to Finding No. 1184:

Rambus has no specific response.

(A) Claim 151 of the '692 Application

1185. Claim 151 of the '692 application, as submitted on June 28, 1993, recited:

> [1] A memory device residing on a single substrate, comprising:
>
> [2] (A) a memory array for storing data at addresses;
>
> [3] (B) a clock signal receiving circuit coupled to receive an external clock signal for generating a local clock signal for performing memory operations with respect to the memory array;
>
> [4] (C) a phase locked loop (PLL) coupled to the clock signal receiving circuit and the memory array for providing a variable delay to the local clock signal such that the delayed local clock signal is synchronized with the external clock signal received by the clock signal receiving circuit.

(CX1502 at 208) (numbering added).

Rambus's Response to Finding No. 1185:

Rambus has no specific response.

1186. On September 14, 1994, NEC Corporation made a proposal to JEDEC Committee 42.3 that the SDRAM standard incorporate an on-chip PLL. (JX0021 at 1, 91). The proposal demonstrates the use of a PLL on an SDRAM chip to synchronize an external clock (indicated as CLK) and the internal clock (indicated as ICLK). (JX0021 at 91; Nusbaum, Tr. 1587-88; Jacob, Tr. 5533-34).

Rambus's Response to Finding No. 1186:

The proposed Finding is incorrect and incomplete. The September 14, 1994 NEC presentation included a "PLL Enable Mode" according to which a PLL on an SDRAM chip

could be enabled or disabled depending on a bit in the mode register. (JX0021 at 87, 91-92.) The NEC presentation did not propose that the SDRAM standard incorporate this PLL enable mode, but only that it be available as an "option." (JX0021 at 87.) The NEC presentation was a "first showing" (JX0021 at 11), which never proceeded to a second showing or to balloting. The presentation indicates that, in the event the PLL is enabled, its purpose is to generate an internal clock (ICLK) that is aligned with an external clock (CLK) to drive an output buffer. (JX0021 at 91; Nusbaum, Tr. 1632-33; Jacob, Tr. 5533-34, 5635).

1187. A JEDEC-compliant SDRAM that incorporated the NEC on-chip PLL proposal would contain each limitation of claim 151 of the '692 application as set forth in the June 23, 1993 amendment. (Nusbaum, Tr. 1589-93). A reasonable engineer could construe the June 1993 version of claim 151 to cover a JEDEC-compliant SDRAM including a PLL circuit as set forth in the September 1994 NEC proposal. (Jacob, Tr. 5535).

Rambus's Response to Finding No. 1187:

The finding is incorrect. As set forth below, the NEC proposal does not contain each limitation of claim 151 of the '692 application and a reasonable engineer would not construe claim 151 as covering a JEDEC compliant SDRAM including a PLL circuit as set forth in the September 1994 NEC proposal.

1188. A JEDEC-compliant SDRAM is a memory device residing on a single substrate. Therefore it satisfies element [1] of claim 151. (Jacob, Tr. 5536; Nusbaum, Tr. 1590).

Rambus's Response to Finding No. 1188:

Rambus has no specific response.

1189. A JEDEC-compliant SDRAM includes a memory array for storing data at addresses. Therefore, it satisfies element [2] of claim 151. (Jacob, Tr. 5536-37; Nusbaum, Tr. 1590).

Rambus's Response to Finding No. 1189:

Rambus has no specific response.

1190. A JEDEC-compliant SDRAM including a PLL circuit as set forth in the September 1994 NEC proposal will include "a clock signal receiving circuit" as indicated by the triangle labeled "receiver" in the proposal. The receiver circuit generates a local, internal clock signal, ICLK. (JX0021 at 91; Jacob, Tr. 5537-38). The local clock signal is coupled to the memory array through the output driver that drives data onto the bus, thereby performing memory operations. (JX0021 at 91; Jacob, Tr. 5538). Therefore, a JEDEC-compliant SDRAM including a PLL circuit as set forth in the September 1994 NEC proposal satisfies element [3] of claim 151. (Jacob, Tr. 5538; Nusbaum, Tr. 1590-91).

Rambus's Response to Finding No. 1190:

The proposed finding is incorrect. The local clock signal is not "coupled to the memory array through the output driver." As clearly indicated in the proposal, ICLK is coupled to the output driver, not to the memory array. (JX0021 at 91). Moreover, the connection between the memory array and the output driver is for data to be transferred out of the array; as shown in the diagram, ICLK cannot affect the timing of any operations in the memory array itself. (JX0021 at 91; Nusbaum, Tr. 1632-33; Jacob, Tr. 5635; Fliesler, Tr. 8872.) It follows that ICLK does not "perform[] memory operations with respect to the memory array" as required by claim 151. (Fliesler, Tr. 8872).

1191. A JEDEC-compliant SDRAM including a PLL circuit as set forth in the September 1994 NEC proposal will include a PLL which is coupled to the clock signal and to the memory array through the output driver. The PLL delays the local clock signal in order to synchronize it with the external clock signal. Therefore, an SDRAM including the PLL proposal satisfies element [4] of claim 151. (JX0021 at 91; Jacob, Tr. 5538-39; Nusbaum, Tr. 1591-92).

Rambus's Response to Finding No. 1191:

The proposed finding is incorrect. The PLL in the NEC presentation is not coupled to the memory array, as required by the claim, but rather to the output driver. (JX0021 at 91;

Nusbaum, Tr. 1632-33; Jacob, Tr. 5635; Fliesler, Tr. 8872.). Furthermore, the PLL in the NEC presentation does not delay the local signal in order to synchronize it with the external clock signal; a PLL, as the term is generally used, uses a voltage controlled oscillator rather than a variable delay to synchronize two signals. (RRFF 595). The reference in Claim 151 to a "PLL" is a misnomer, since the claim actually describes a DLL. (Jacob, Tr. 5634).

1192. On October 23, 1995, Rambus submitted an amendment to the PTO making minor changes to claim 151, including adding a limitation to the end of claim 151 reciting "wherein the memory array, the clock signal receiving circuit and the PLL all reside on a single semiconductor substrate." (CX1502 at 233-34; Nusbaum, Tr. 1585-86). The amendments to claim 151 did not significantly change the meaning of the claim. (Jacob, Tr. 5540-41; Nusbaum, Tr. 1593).

Rambus's Response to Finding No. 1192:

The proposed finding is misleading because the limitation added to claim 151, that the memory array, the clock signal receiving circuit and the PLL all reside on a single substrate, is significant. Rambus agrees, however, that the amendment did not materially change the meaning of the claim in any way relevant to the 1994 NEC presentation. Claim 151, as amended, does not cover the NEC presentation for the same reasons that it failed to do so prior to amendment. (RRFF 1190-91).

1193. A JEDEC-compliant SDRAM that incorporated the September 1994 NEC on-chip PLL proposal would contain each limitation of claim 151 of the '692 application as set forth in the October 23, 1995 amendment. (Nusbaum, Tr. 1589-92). An engineer could reasonably construe the October 1995 version of claim 151 to cover a JEDEC-compliant SDRAM including a PLL circuit as set forth in the September 1994 NEC proposal. (Jacob, Tr. 5540-41).

Rambus's Response to Finding No. 1193:

The proposed finding is irrelevant. The October 1995 amendment was not filed until over a year after the September 1994 NEC presentation.

The proposed finding is also incorrect. The September 1994 NEC presentation did not contain each limitation of claim 151 of the '692 application, as amended, for the same reasons that it did not contain each limitation of claim 151 prior to amendment. (RRFF 1190-91).

(B) Claim 152 of the '692 Application

1194. Rambus submitted claim 152 of the '692 application to the PTO on June 23, 1993. Claim 152, which is dependent on claim 151 adds the limitation that "the memory array is a dynamic random access memory (DRAM)." (CX1502 at 208).

Rambus's Response to Finding No. 1194:

Rambus has no specific response.

1195. Because a JEDEC-compliant SDRAM is a DRAM, claim 152 covers an SDRAM incorporating the NEC on-chip PLL proposal. (Nusbaum, Tr. 1592).

Rambus's Response to Finding No. 1195:

The proposed finding is incorrect. Since claim 152 is dependent on claim 151, it incorporates all of the limitations of claim 151 and fails to cover an SDRAM for the same reasons as claim 151. (*See* RRFF 1190-91).

(C) Claim 166 and 167 of the '692 Application

1196. In the October 23, 1995 amendment, Rambus added claims 166 and 167 to the '692 application. (CX1502 at 233-34). Claim 166 recites "a computer system, comprising: (A) a bus; (B) a bus master coupled to the bus" and a "memory device" having the same features as recited in claim 151 of the '692 application. (CX1502 at 234).

Rambus's Response to Finding No. 1196:

Rambus has no specific response.

1197. Claim 167 is dependent on claim 166. Claim 167 requires that the memory array be "a dynamic random access memory (DRAM)." (CX1502 at 235).

Rambus's Response to Finding No. 1197:

Rambus has no specific response.

1198. Claims 166 and 167 cover a computer system using a JEDEC-compliant SDRAM incorporating the September 1994 NEC on-chip PLL proposal. (Nusbaum, Tr. 1593-1594).

Rambus's Response to Finding No. 1198:

The proposed finding is irrelevant. The October 1995 amendment was not filed until over a year after the September 1994 NEC presentation.

The proposed finding is also incorrect. Claims 166 and 167 fail to cover a device built according to the NEC presentation for the same reasons as claims 151 and 152. (*See* RRFF 1190-91, 1195; Fliesler, Tr. 8875).

4. The Rambus '646 Patent Application Contained Claims Covering A JEDEC-Compliant SDRAM Incorporating A Proposed Dual-Edge Clocking Feature.

1199. Rambus patent application 08/222,646 (the '646 application) contained claims that covered a JEDEC-compliant SDRAM incorporating a proposed dual-edged clocking feature. (Nusbaum, Tr. 1595-1603; Jacob, Tr. 5549-50).

Rambus's Response to Finding No. 1199:

The proposed finding is incorrect for the reasons set forth in the responses below with respect to various proposals purportedly relating to dual-edged clocking.

1200. A proposal for a dual-edged clocking scheme appears in JEDEC 42.3 Committee minutes from May 1992. (CX0034 at 32; Jacob, Tr. 5542-43).

Rambus's Response to Finding No. 1200:

The proposed finding is misleading and incomplete. (*See* RRFF 1207).

1201. The minutes of the December 6, 1995 JEDEC 42.3 Committee meeting report the results of a "SDRAM Feature Survey Ballot." (JX0028 at 1, 35, 45). Under the heading "Issues with Mixed Support," the minutes list "Using both edges of the clock for sampling inputs."

(JX0028 at 35). This is a reference to dual-edged clocking. (Jacob, Tr. 5543-44). The minutes also report the results of voting on the question, "Does your company believe that future generations of SDRAM could benefit from BOTH edges of the clock for sampling input?" (JX0028 at 45).

Rambus's Response to Finding No. 1201:

The proposed finding is misleading and incomplete. (*See* RRFF 1207).

1202. At a March 20, 1996 meeting of JEDEC Committee 42.3, Samsung Corporation made a presentation entitled "Future SDRAM." (JX0031 at 68-72). The "Proposed Clocking Scheme" of the presentation included the feature "Data in sampled at both edge [sic] of Clock into memory." (JX0031 at 71). This is a reference to dual-edged clocking. (Jacob, Tr. 5554-45).

Rambus's Response to Finding No. 1202:

The proposed finding is misleading and incomplete. (*See* RRFF 1207).

1203. The May 1992, December 1995 and March 1996 proposals for dual edge clocking require controlling memory operations (read and write operations) in an SDRAM, in response to both the rising edge and the falling edge of a clock signal. (Nusbaum, Tr. 1595-96).

Rambus's Response to Finding No. 1203:

The proposed finding is incorrect. The March 1996 Samsung presentation called for "Data in sampled at both edge of Clock." At most this could refer to some form of dual edge clocking with respect to write operations (data in), not "read and write operations" as the proposed finding suggests. The other two presentations offer even less detail than the Samsung presentation (*see* RRFF 1207); it is impossible to determine what form of dual edge clocking they might have had in mind.

1204. Rambus filed the '646 application on March 31, 1994. The '646 application is a continuation of application number 07/954,945, which is a continuation of the '898 application. (CX1493 at 002; Nusbaum, Tr. 1596).

Rambus's Response to Finding No. 1204:

Rambus has no specific response.

1205. On September 6, 1994, Rambus filed a preliminary amendment in the '646 application that canceled the original claims and added new claims 151 and 152, among others. (CX1493 at 183-201; Nusbaum, Tr. 1597).

Rambus's Response to Finding No. 1205:

Rambus has no specific response.

(A) Claim 151 of the '646 Application

1206. Claim 151 of the '646 application, as submitted to the PTO on September 6, 1994, recites:

> [1] A dynamic random access memory (DRAM) capable of being coupled to a bus, the DRAM comprising:
>
> [2] a first circuit for providing a clock signal;
>
> [3] a conductor for coupling the DRAM to a bus; and
>
> [4] a receiver circuit coupled to the conductor and the first circuit, the receiver circuit for latching information received from the conductor in response to a rising edge of the clock signal and a falling edge of the clock signal.

(CX1493 at 184-85) (numbering added).

Rambus's Response to Finding No. 1206:

The proposed finding is incomplete. In an office action dated January 24, 1995, the patent examiner rejected claim 151 for, among other reasons, being indefinite. (CX 1493 at 212, 215). Claim 151 of the '646 application was cancelled by Rambus on September 14, 1995. (CX1493 at 243; Fliesler Tr. 8856-57).

1207. Claim 151 of the '646 application covers a JEDEC-compliant SDRAM incorporating the dual edge clocking proposals made to JEDEC in May 1992, December 1995,

March 1996. (Nusbaum, Tr. 1595-1603; Jacob, Tr. 5549-50).

Rambus's Response to Finding No. 1207:

The proposed finding is irrelevant: Since claim 151 was filed in September 1994 and cancelled in September 1995 (CCFF 1206; Response to Finding No. 1206), it was not pending in May 1992, December 1995, or March 1996.

Moreover, it is misleading to describe the mentions of dual edge clocking on those dates as "proposals." Attached to the May 1992 JEDEC meeting minutes was a memorandum summarizing presentations made at a task group meeting in April 1992. One presentation, by IBM, related to an asynchronous DRAM and stated "dual clock edge" without any further detail about that feature. (CX0034 at 32). There is no indication in the minutes that this presentation was repeated in the May 1992 Committee meeting. (CX0034 at 4-5).

At the December 1995 JEDEC meeting, the results of a survey ballot, one of whose questions related to dual-edge clocking, were presented. With respect to dual-edge clocking, the result of the survey ballot was that there was "mixed support" for "using both edges of the clock for sampling inputs," with seven respondents indicating support for the feature and nine opposed to it. (JX0028 at 35, 45). The survey ballot provided no further details of the implementation of dual-edge clocking.

At the March 1996 JEDEC meeting, Samsung gave a presentation regarding "Future SDRAM Concepts." (JX0031 at 9). With respect to dual-edge clocking, the Samsung presentation stated only that "Data in sampled at both edge of Clock into memory." (*Id.* at 71). No further details of the implementation of dual edge clocking were provided. There is no evidence that the Samsung presentation was ever pursued further at JEDEC, and, indeed, even

the initial presentation was characterized in the minutes simply as a "presentation," rather than a "first showing." (*Id*. at 9).

In any case, claim 151 would not cover the presentations raised by Complaint Counsel because they contain no implementation details and thus do not contain the implementation details that are *required* by claim 151 of the '646 application. (CCFF 1206; CX 1493 at 184-85).

1208. An SDRAM is coupled to a bus. Therefore, a JEDEC-compliant SDRAM that incorporated the dual-edge clocking feature proposed in March 96 would satisfy element [1] of claim 151 of the '646 application. (Nusbaum, Tr. 1602; Jacob, Tr. 5550-51). A JEDEC-compliant SDRAM that incorporated the dual-edge clocking feature proposed in May 1992 or December 1995 would also satisfy element [1]. (Nusbaum, Tr. 1598, 1602, 1617; Jacob, Tr. 5550-51).

Rambus's Response to Finding No. 1208:

As discussed above, it is misleading to characterize the mentions of dual edge clocking in May 1992, December 1995 and March 1996 as "proposals." (RRFF 1207). In May 1992, dual edge clocking was mentioned in an attachment to the minutes, not in a presentation actually made at the meeting; in December 1995, a survey ballot indicated that a majority of respondents did not want dual edge clocking; in March 1996, Samsung made a presentation, not even characterized as a "first showing," that mentioned dual edge clocking. (Response to Finding No. 1207). Moreover, it makes no sense to refer to a "JEDEC-compliant SDRAM that incorporated the dual-edge clocking feature" in the IBM presentation summarized in the attachment to the May 1992 minutes; JEDEC-compliant SDRAMs are synchronous DRAMs with synchronous RAS and CAS signals, while the IBM presentation described an asynchronous DRAM with an asynchronous RAS/CAS interface. (CX 34 at 30-32). Indeed, although the

IBM presentation does state "dual clock edge," this is loose terminology since the IBM technology that was the subject of the presentation did not transfer data on both edges of a "clock," but rather used both edges of a separate "toggle" signal. (*See* RRFF 510).

1209. An SDRAM receives an external clock signal through a circuit that provides an internal clock signal. Therefore, a JEDEC-compliant SDRAM that incorporated the dual-edge clocking feature proposed in March 96 would satisfy element [2] of claim 151 of the '646 application. (Nusbaum, Tr. 1602; Jacob, Tr. 5551). A JEDEC-compliant SDRAM that incorporated the dual-edge clocking feature proposed in May 1992 or December 1995 would also satisfy element [2]. (Nusbaum, Tr. 1598, 1602, 1617; Jacob, Tr. 5551-52).

Rambus's Response to Finding No. 1209:

The proposed finding is irrelevant and misleading. (*See* RRFF 1207, 1208.)

1210. An SDRAM will have pins that couple it a bus. Therefore, a JEDEC-compliant SDRAM that incorporated the dual-edge clocking feature proposed in March 96 would satisfy element [3] of claim 151 of the '646 application. (Nusbaum, Tr. 1602; Jacob, Tr. 5551). A JEDEC-compliant SDRAM that incorporated the dual-edge clocking feature proposed in May 1992 or December 1995 would also satisfy element [3]. (Nusbaum, Tr. 1598, 1602, 1617; Jacob, Tr. 5551-54).

Rambus's Response to Finding No. 1210:

The proposed finding is irrelevant and misleading. (*See* RRFF 1207, 1208.)

1211. An SDRAM that samples input data in response to the rising and falling edges of a clock signal must have a receiver circuit that latches data in response to the rising and falling edges of a clock signal. Therefore, a JEDEC-compliant SDRAM that incorporated the dual-edge clocking feature proposed in March 96 would satisfy element [4] of claim 151 of the '646 application. (Nusbaum, Tr. 1602-03; Jacob, Tr. 5551). A JEDEC-compliant SDRAM that incorporated the dual-edge clocking feature proposed in May 1992 or December 1995 would also satisfy element [4]. (Nusbaum, Tr. 1598, 1602-03, 1617; Jacob, Tr. 5554-55).

Rambus's Response to Finding No. 1211:

The proposed finding is irrelevant and misleading. (*See* RRFF 1207, 1208.) Moreover, Complaint Counsel have not shown that to implement dual edge clocking an SDRAM "must have a receiver circuit that latches data in response to the rising and falling edges of a clock

signal."

(B) Claim 152 of the '646 Application

1212. Claim 152 of the '646 application, as submitted on September 6, 1994, was dependant on claim 151 and added limitations to "a first input receiver" and "a second input receiver". (CX1493 at 185).

Rambus's Response to Finding No. 1212:

Rambus has no specific response.

1213. On April 21, 1995, Rambus submitted to the PTO an amendment to the '646 application, which made a minor wording change to claim 151 and added the language of claim 151 to claim 152 so that it claim 152 was no longer dependant on claim 151. (CX1493 at 223-24). Rambus canceled claim 151 on September 14, 1995. (CX1493 at 243). On October 6, 1995, the examiner issued a notice of allowance for the '646 application, which indicated that he had allowed claim 152, among others. (CX1493 at 249).

Rambus's Response to Finding No. 1213:

Rambus has no specific response.

1214. The '646 application issued as Patent No. 5,513,327 (the '327 patent) to Rambus on April 30, 1996. (CX1494 at 1). Claim 152 of the '646 application issued as claim 1 of the '327 patent. (CX1493 at 223-24; CX1494 at 23).

Rambus's Response to Finding No. 1214:

Rambus has no specific response.

1215. Claim 152 of the of the '646 application covered the most feasible way to implement a JEDEC-compliant SDRAM that incorporated the dual-edged clocking feature proposed in May 1992, December 1995 and March 1996. (Jacob, Tr. 5545-47).

Rambus's Response to Finding No. 1215:

It is misleading to refer to the mentions of dual-edge clocking in May 1992, December 1995, and March 1996 as "propos[als]"; moreover, it makes no sense to refer to "a JEDEC-compliant SDRAM that incorporated the dual-edge clocking feature" mentioned in the summary

of a presentation about an asynchronous DRAM in an attachment to the May 1992 minutes. (*See* RRFF 1207, 1208). In addition, the proposed finding is incomplete. Professor Jacob also testified that the using two input receivers as described in claim 152 of the '646 application was "sort of an implementation detail." (Jacob, Tr. 5546-47). Moreover, despite Professor Jacob's testimony, when dual edge clocking *was* implemented in DDR SDRAM it was *not* implemented according to claim 152 of the '646 application: claim 152 of the '646 patent describes latching information in response to a clock signal to write data to the DRAM, while the DDR SDRAM standard uses a different signal, the DQS strobe signal, for that purpose. (RPF 354 (referring to claim 1 of the '327 patent which, as noted in CCFF 1214, corresponds to claim 152 of the '646 application)).

5. The Rambus '327 Patent Contains Claims Covering Implementation of A Dual-Edge Clocking Feature in JEDEC-Compliant SDRAM .

1216. Rambus Patent No. 5,513,327 (the '327 patent) contains claims covering the most feasible way to implement the dual-edged clocking feature proposed to JEDEC in May 1992, December 1995 and March 1996 in a JEDEC-compliant SDRAM. (Jacob, Tr. 5545-49; see CX1244 at 1).

Rambus's Response to Finding No. 1216:

The proposed finding is irrelevant: The '327 patent issued in April 30, 1996, after all of the presentations cited by Complaint Counsel.

The proposed finding is also misleading in referring to the mentions of dual-edge clocking in May 1992, December 1995, and March 1996 as "propos[als]"; moreover, it makes no sense to refer to "a JEDEC-compliant SDRAM that incorporated the dual-edge clocking feature" mentioned in the summary of a presentation about an asynchronous DRAM in an attachment to the May 1992 minutes. (*See* RRFF 1207 and 1208). In addition, the proposed

finding is incomplete. Professor Jacob also testified that the using two input receivers as described in claim 1 of the '327 patent was "sort of an implementation detail." (Jacob, Tr. 5546-47). Moreover, despite Professor Jacob's testimony, when dual edge clocking *was* implemented in DDR SDRAM it was *not* implemented according to claim 1 of the '327 patent: claim 1 of the '327 patent describes latching information in response to a clock signal to write data to the DRAM, while the DDR SDRAM standard uses a different signal, the DQS strobe signal, for that purpose. (RPF 354).

1217. The '327 patent also contains claims covering DDR SDRAM as described in JEDEC Specification JESD 79 (June 2000). (Jacob, Tr. 5550-60).

Rambus's Response to Finding No. 1217:

The proposed finding is irrelevant: Rambus withdrew from JEDEC over 4 years before JESD 79 was published. The proposed finding is also incorrect as set forth in Rambus's Responses to Findings Nos. 1224-28 and 1234-37.

(A) Claim 1 of the '327 Patent Compared to JEDEC Dual-Edged Clocking Proposals

1218. Claim 1 of the '327 patent recites:

> [1] A dynamic random access memory (DRAM), comprising; a first circuit for providing a clock signal;
>
> [2] a conductor for coupling the DRAM to a bus; and a receiver circuit coupled to the conductor and the first circuit,
>
> [3] the receiver circuit for latching information received from the conductor in response to a rising edge of the clock signal and a falling edge of the clock signal,
>
> [4] wherein the receiver circuit comprises:
>
> a first input receiver coupled to the conductor and the first

> circuit, the first input receiver for latching information provided by the bus via the conductor in response to the rising edge of the clock signal; and
>
> a second input receiver coupled to the conductor and the first circuit, the second input receiver for latching information frm the bus in response to the falling edge of the clock signal.

(CX1494 at 23) (numbering added).

Rambus's Response to Finding No. 1218:

Rambus has no specific response.

1219. An engineer could reasonablely construe claim 1 of the '327 patent to cover a JEDEC-compliant SDRAM that incorporated the dual-edged clocking feature of the May 1992 (CX0034 at 32) and March 1996 (JX0031 at 71) proposals or the December 1995 survey ballot (JX0028 at 35). (Jacob, Tr. 5545).

Rambus's Response to Finding No. 1219:

The proposed finding is irrelevant: The '327 patent issued in April 30, 1996, after all of the presentations cited by Complaint Counsel.

The proposed finding is also misleading in referring to the mentions of dual-edge clocking in May 1992 and March 1996 as "proposals"; moreover, it makes no sense to refer to "a JEDEC-compliant SDRAM that incorporated the dual-edge clocking feature" mentioned in the summary of a presentation about an asynchronous DRAM in an attachment to the May 1992 minutes. (*See* RRFF 1207, 1208).

The proposed finding is also incomplete. The '327 patent issued on April 30, 1996 (CCFF 1214), after all three of the presentations raised by Complaint Counsel.

The proposed finding is also incorrect. Complaint Counsel's expert, Professor Jacob, concedes that claim 1 of the '327 patent is implementation-specific. (Jacob, Tr. 5546-47). It

follows that a reasonable engineer could not reasonably construe claim 1 of the '327 patent as covering presentations, like the ones raised by Complaint Counsel, that provided no implementation details whatsoever. (*See* RRFF 1207).

1220. An SDRAM uses an external clock signal for generating an internal clock signal. Therefore, a JEDEC-compliant SDRAM that incorporated the dual-edge clocking feature proposed in May 1992, December 1995 or March 1996 would satisfy element [1] of claim 1 of the '327 patent. (Jacob, Tr. 5545-46; JX0056 at 124).

Rambus's Response to Finding No. 1220:

The proposed finding is irrelevant, misleading, incomplete and incorrect. (*See* RRFF 1219).

1221. An SDRAM uses a pin for connecting to a bus and has a clock pin coupled to a clock receiver circuit. Therefore, a JEDEC-compliant SDRAM that incorporated the dual-edge clocking feature proposed in May 1992, December 1995 or March 1996 would satisfy element [2] of claim 1 of the '327 patent. (Jacob, Tr. 5545-46; JX0056 at 106).

Rambus's Response to Finding No. 1221:

The proposed finding is irrelevant, misleading, incomplete and incorrect. (*See* RRFF 1219).

1222. An SDRAM having a dual-edged clocking feature will latch data in response to the rising edge and falling edge of a clock. Therefore, a JEDEC-compliant SDRAM that incorporated the dual-edge clocking feature proposed in May 1992, December 1995 or March 1996 would satisfy element [3] of claim 1 of the '327 patent. (Jacob, Tr. 5546).

Rambus's Response to Finding No. 1222:

The proposed finding is irrelevant, misleading, incomplete and incorrect. (*See* RRFF 1219). Moreover, Complaint Counsel have not shown that to implement dual edge clocking an SDRAM must have "a receiver circuit for latching information in response to a rising edge of the clock signal and a falling edge of the clock signal" as required by claim 1.

1223. The only way for an SDRAM having a dual-edged clocking feature that latches data in response to the rising edge and the falling edge of a clock is to use two receivers, one which latches data in response to a rising edge and one which latches data in response to a falling edge. Therefore, a JEDEC-compliant SDRAM that incorporated the dual-edged clocking feature proposed in May 1992, December 1995 or March 1996 would satisfy element [4] of claim 1 of the '327 patent. (Jacob, Tr. 5546-47).

Rambus's Response to Finding No. 1223:

The proposed finding is not supported by the evidence. Professor Jacob described the use of two input receivers that latch data in response to the rising edge and falling edge of the clock as "sort of an implementation detail" (Jacob, Tr. 5546-47), indicating that other implementations were possible. Moreover, when dual edge clocking *was* implemented in DDR SDRAM it was *not* implemented according to claim 1 of the '327 patent: claim 1 of the '327 patent describes latching information in response to a clock signal to write data to the DRAM, while the DDR SDRAM standard uses a different signal, the DQS strobe signal, for that purpose. (RPF 354).

(B) Claim 1 of the '327 Patent Compared to the JEDEC DDR SDRAM Standard

1224. An engineer could reasonablely construe claim 1 of the '327 patent to cover a DDR SDRAM as described in the JESD 79 specification dated June 2000 (JX57). (Jacob, Tr. 5551-52).

Rambus's Response to Finding No. 1224:

The proposed finding is irrelevant: Rambus withdrew from JEDEC over 4 years before JESD 79 was published.

The proposed finding is also incorrect. Claim 1 of the '327 patent calls for the use of a clock signal to write data to the DRAM, while JESD 79 describes the use of a different signal, the DQS strobe signal, for that purpose. (JX0057 at 5; Fliesler, Tr. at 8861; Jacob, Tr. 5641-42).

A clock signal and a strobe signal are different: a clock is a "free-running" signal, that is running all the time, while the strobe in DDR SDRAMs is not free-running. (Macri, Tr. 4634).

1225. Circuits on DDR SDRAM provide clock signals. Therefore a DDR SDRAM satisfies element [1] of claim 1 of the '327 patent (Jacob, Tr. 5552-53; JX0057 at 8).

Rambus's Response to Finding No. 1225:

Rambus has no specific response.

1226. A DDR SDRAM includes pins to couple the DRAM to a bus. The DDR SDRAM has a circuit including two input registers that acts as the receiver circuit for data. Therefore a DDR SDRAM satisfies element [2] of claim 1 of the '327 patent (Jacob, Tr. 5552-53; JX0057 at 8).

Rambus's Response to Finding No. 1226:

The proposed finding is incorrect. Element [2] of claim 1 requires that the receiver circuit be coupled to the "conductor for coupling the DRAM to a bus," namely to the data pins. (Jacob, Tr. 5553). However, the input registers that the proposed finding identifies with the receiver circuit are not coupled to the data pins; rather, the data pins are coupled to a box marked "RCVRS," which is in turn coupled to the input registers. (JX0057 at 8). Moreover, the functional block diagram in JESD79 on which this proposed finding depends is not properly considered a part of the DDR SDRAM standard. (*See* RRFF 1237).

1227. A DDR SDRAM will latch data for inputs (writes) in response to the rising edge and falling edge of the data strobe (DQS), which is a clock signal. Therefore a DDR SDRAM satisfies element [3] of claim 1 of the '327 patent (Jacob, Tr. 5553-54; JX0057 at 32).

Rambus's Response to Finding No. 1227:

The proposed finding is incorrect. The data strobe (DQS) is not a clock signal within the meaning of the '327 patent and, therefore, a DDR SDRAM does not satisfy element [3] of claim 1 of the '327 patent. (*See* RRFF 1224). Indeed, Professor Jacob conceded that, in DDR

SDRAMs, "the system clock is all but ignored" in write operations, where a separate data strobe signal is used. (Jacob, Tr. 5642).

1228. A DDR SDRAM includes two input registers, which are input receivers, one of which latches data in response to the rising edge of DQS, and one of which latches data in response to the falling edge of (DQS, which is a clock signal. Therefore a DDR SDRAM satisfies element [4] of the '327 patent (Jacob, Tr. 5554-55; JX0057 at 8).

Rambus's Response to Finding No. 1228:

The proposed finding is incorrect. The data strobe (DQS) is not a clock signal within the meaning of the '327 patent and, therefore, a DDR SDRAM does not satisfy element [4] of claim 1 of the '327 patent. (*See* RRFF 1224). In addition, the "input registers" cannot be identified with the input receivers required by claim 1 because the input registers do not latch data in response to the DQS signal; rather a separate component marked "RCVRS" latches the data. (JX0057 at 8). Moreover, the functional block diagram in JESD79 on which this proposed finding depends is not properly considered a part of the DDR SDRAM standard. (*See* RRFF 1237).

(C) Claim 7 of the '327 Patent Compared to JEDEC Dual-Edged Clocking Proposals

1229. Claim 7 of the '327 patent recites:

> [1] A dynamic random access memory (DRAM), comprising;
>
> a first circuit for providing a clock signal;
>
> [2] a conductor for coupling the DRAM to a bus; and
>
> [3] a multiplexer coupled to the first circuit, the multiplexer having an output, a first input, and a second input;
>
> a first output line coupled to the first input of the multiplexer, wherein the multiplexer couples the first

output line to the output of the multiplexer in response to a rising edge of the clock signal; and

a second output line coupled to the second input of the multiplexer, wherein the multiplexer couples to the second output line to the output of the multiplexer in response to a falling edge of the clock signal.

(CX1494 at 23) (numbering added).

Rambus's Response to Finding No. 1229:

Rambus has no specific response.

1230. An engineer could reasonablely construe claim 7 of the '327 patent to cover a JEDEC-compliant SDRAM that also incorporated the dual-edged clocking feature of the May 1992 (CX0034 at 32) and March 1996 (JX0031 at 71) proposals or the December 1995 survey ballot (JX0028 at 35). (Jacob, Tr. 5547-48).

Rambus's Response to Finding No. 1230:

The proposed finding is irrelevant: The '327 patent issued in April 30, 1996, after all of the presentations cited by Complaint Counsel.

The proposed finding is also misleading in referring to the mentions of dual-edge clocking in May 1992 and March 1996 as "proposals"; moreover, it makes no sense to refer to "a JEDEC-compliant SDRAM that incorporated the dual-edge clocking feature" mentioned in the summary of a presentation about an asynchronous DRAM in an attachment to the May 1992 minutes. (*See* RRFF 1207, 1208).

The proposed finding is also incomplete. The '327 patent issued on April 30, 1996 (CCFF 1214), after all three of the presentations raised by Complaint Counsel.

The proposed finding is also inaccurate. Complaint Counsel's expert, Professor Jacob, concedes that claim 7 of the '327 patent is implementation-specific. (Jacob, Tr. 5548 ("Element

3 describes an implementation of dual-edged clocking for driving data out onto a bus and which you toggle between two output drivers through a multiplexer."). It follows that a reasonable engineer could not reasonably construe claim 7 of the '327 patent as covering presentations, like the ones raised by Complaint Counsel, that provided no implementation details whatsoever. (*See* RRFF 1207).

1231. An SDRAM uses an external clock signal for generating an internal clock signal. Therefore, a JEDEC-compliant SDRAM that incorporated the dual-edge clocking feature proposed in May 1992, December 1995 or March 1996 would satisfy element [1] of claim 7 of the '327 patent. (Jacob, Tr. 5548; JX0056 at 124)).

Rambus's Response to Finding No. 1231:

The proposed finding is irrelevant, misleading, incomplete and inaccurate. (*See* RRFF 1230).

1232. An SDRAM uses a pin for connecting to a bus. Therefore, a JEDEC-compliant SDRAM that incorporated the dual-edge clocking feature proposed to in May 1992, December 1995 or March 1996 would satisfy element [2] of claim 7 of the '327 patent. (Jacob, Tr. 5548; JX0056 at 106).

Rambus's Response to Finding No. 1232:

The proposed finding is irrelevant, misleading, incomplete and inaccurate. (*See* RRFF 1230).

1233. The most reasonable way for an SDRAM having a dual-edged clocking feature to output data on the rising and falling edge of a clock signal is to toggle between two output drivers using a multiplexer. Therefore, a JEDEC-compliant SDRAM that used the most reasonable method to incorporate the dual-edge clocking feature proposed in May 1992, December 1995 or March 1996 would satisfy element [3] of claim 7 of the '327 patent. (Jacob, Tr. 5548-49).

Rambus's Response to Finding No. 1233:

The proposed finding is irrelevant, misleading, incomplete and inaccurate. (*See* RRFF

1230). Moreover, Professor Jacob's testimony that the use of a multiplexer as described is the "most reasonable implementation" of dual edge clocking for output data in an SDRAM concedes that this is simply one of a number of implementations. (Jacob, Tr. 5548-49).

(D) Claim 7 of the '327 Patent Compared to the JEDEC DDR SDRAM Standard

1234. An engineer could reasonablely construe claim 7 of the '327 patent to cover a DDR SDRAM as described in the JESD 79 specification dated June 2000 (JX57). (Jacob, Tr. 5556-60).

Rambus's Response to Finding No. 1234:

The proposed finding is irrelevant: Rambus withdrew from JEDEC over 4 years before JESD 79 was published.

The proposed finding is also incorrect. An engineer could not reasonably construe claim 7 o f the '327 patent as necessarily covering a DDR SDRAM as described in JESD 79, because devices could be built according to JESD 79 without infringing claim 7 of the '327 patent. (Fliesler, Tr. 8861-2). Claim 7 calls for a multiplexer in the DRAM output path while the DDR SDRAM standard does not require the use of a multiplexer. (Fliesler, Tr. 8863; Jacob, Tr. 5642-43).

1235. Circuits on DDR SDRAMs provide clock signals. Therefore a DDR SDRAM satisfies element [1] of claim 7 of the '327 patent (Jacob, Tr. 5557; JX0057 at 8).

Rambus's Response to Finding No. 1235:

Rambus has no specific response.

1236. A DDR SDRAM includes pins to couple the DRAM to a bus. Therefore a DDR SDRAM satisfies element [2] of claim 7 of the '327 patent (Jacob, Tr. 5557-58; JX0057 at 8).

Rambus's Response to Finding No. 1236:

Rambus has no specific response.

1237. A DDR SDRAM has a multiplexer that is coupled to a clock. The multiplexer has two output lines which allows the DDR SDRAM to output data in response to the rising edge and the falling edge of a clock signal. Therefore a DDR SDRAM satisfies element [3] of claim 7 of the '327 patent. (Jacob, Tr. 5558-60; JX0057 at 08, 22).

Rambus's Response to Finding No. 1237:

The proposed finding is incorrect because the DDR SDRAM standard does not require the use of a multiplexer. Release 9 of JEDEC Standard 21-C, in which the DDR SDRAM standard was first published, does not mention a multiplexer. (CX0234 at 143-207). Complaint Counsel rely on a "Functional Block Diagram" in a follow on publication, JESD 79, which shows a multiplexer. (JX0057 at 8). However, JESD 79 makes clear that the Functional Block Diagram "does not represent an actual circuit implementation." (*Id.*) That the multiplexer is just shown in an example of a possible implementation and is not actually part of the standard also follows from the relationship between Standard 21-C and JESD 79. The latter was simply intended to be an "extraction" from the former. (Rhoden, Tr. 1293-94). It was not intended to add any new material. (Rhoden, Tr. 1294 ("Q. Comparing JX-57 [JESD 79] to CX-234 [Standard 21-C], what new material, if any, was added to JX-57 at the time it was published? A. It shouldn't have been any new material necessarily, except for whatever cleanup was necessary at the time. The fact that there's some time between here, there's a possibility that things were -- that maybe JESD79 is slightly more updated, but it should be the same thing.")).

In addition, claim 7 of the '327 patent requires that the mutliplexer respond to rising and falling edges of a clock signal. (CCFF 1229). Professor Jacob's identification of the least

significant bit output of a counter (Col 0) as the corresponding clock signal in the block diagram of JESD 79 (JX0057 at 8) is vague and misleading. (*See* Jacob, Tr. 5558). Indeed, even Professor Jacob seemed to concede that this purported correspondence was far from clear, testifying that there is an "*implicit* clock going into this circuit even though it's not showed" and therefore Col 0 "starts to look *a lot like* a clock." (Jacob, Tr. 5558 (emphasis added)).

D. Rambus Was Successful In Concealing Its Claim To Intellectual Property Rights To JEDEC Standard Technology.

1. During the Time It was a Member of JEDEC and Thereafter, Rambus Promoted Its Proprietary RDRAM Technology And Concealed Its Intellectual Property Claims to JEDEC Standard Technology.

1238. Throughout the period of its membership in JEDEC and thereafter, Rambus pursued a strategy of actively promoting its proprietary RDRAM technology to companies who were in a position to manufacture memory chips or related chipsets. (See Crisp, Tr. 2931; CX0543A at 7-8).

Rambus's Response to Finding No. 1238:

The proposed finding is incomplete. Rambus also promoted its RDRAM technology to others, including systems companies. (CX0543A at 1, 3).

1239. Rambus efforts to promote adoption of its proprietary RDRAM technology included making presentations concerning the proprietary technology to memory chip manufacturers and other firms. (E.g. CX2107 at 63 (Oh, Dep.); Bechtelsheim, Tr. 5818-19; G. Kelley, Tr. 2537; Kellogg, Tr. 5052-53). In connection with such efforts, Rambus commonly entered into non-disclosure agreements ("NDAs") that prohibited the firms from disclosing information concerning the proprietary Rambus technology to others without the consent of Rambus. (E.g. Bechtelsheim, Tr. 5818-19; Rhoden, Tr. 521; Kellogg, Tr. 5052-53).

Rambus's Response to Finding No. 1239:

The proposed finding omits relevant evidence. Rambus's presentations often included a discussion of the patent protection Rambus was seeking for its inventions; after Rambus's

original patent application was made public through the publication of the corresponding PCT application in October 1991, Rambus did disclose non-detailed descriptions of its inventions in various other public documents. (See RRFF 747).

1240. The focus of these presentations was on the advantages Rambus saw of the proprietary RDRAM technology and the unique characteristics of that technology, including its unique bus architecture. (E.g., G. Kelley, Tr. 2533-34; Sussman, Tr. 1429-31). Rambus' presentations of the RDRAM technology in the 1992-93 time frame involved a DRAM with a multiplexed bus, meaning that various signals were combined on a single line. (CX2114 at 61-62 (Karp, Dep.)). Joel Karp, who was with Samsung at the time, viewed the Rambus RDRAM as "more revolutionary than evolutionary." (CX2114 at 63 (Karp, Dep.)). Craig Hampel, Rambus technical director who since 1993 participated in numerous meetings and presentations with DRAM manufacturers and other firms to discuss Rambus technology (Hampel, Tr. 8672, 8729-31), was not aware of any instance in which Rambus representatives told the DRAM manufacturers which aspects of RDRAM were Rambus inventions, or were protected by Rambus patents or patent applications. (Hampel, Tr. 8732-33).

Rambus's Response to Finding No. 1240:

This proposed finding is vague in its reference to "these presentations," and contradicted by other evidence. Notably, the evidence does not support the finding that Rambus's "unique bus architectecture" was a "*focus*" of the numerous presentations made by Rambus. (See RRFF 748).

The definition of multiplexing in the proposed finding as referring to "various signals . . . combined on a single line," is also vague. According to the Federal Circuit, "Multiplexing refers to the sharing of a single set of lines to send multiple types of information." (*Rambus Inc. v. Infineon Technologies AG*, 318 F.3d 1081, 1094 (Fed. Cir. 2003)).

Mr. Hampel's testimony is mischaracterized in the proposed finding and, to the exent that the reference to Mr. Hampel's testimony is meant to imply that Rambus did not inform DRAM manufacturers that its intellectutal property might cover non-RDRAM devices, the

proposed finding is contradicted by the weight of the evidence. (*See* RRFF 749).

1241. Rambus President David Mooring testified that the first time Rambus ever advised any SDRAM manufacturer that Rambus had claims covering features of SDRAMs was Hitachi in late 1999 or early 2000. (CX2079 at 157-58; see also CX2098 at 442-43 (Mooring, Dep.); see also CX2112 at 171-72 (Mooring, FTC Depo.)). Slides used by Rambus in presentations to Rambus customers would "definitely not have put anybody on notice" of the coverage of patents but would only have generic information about aggregate numbers of Rambus patents and/or patent applications. (CX2112 at 180 (Mooring, Dep.)).

Rambus's Response to Finding No. 1241:

This proposed finding is incomplete and misleading. While the slides used by Rambus may only have listed aggregate numbers of Rambus patents and/or applications, Mr. Mooring testified that Rambus's RDRAM licensees were explicitly told that Rambus had pending or issued patents that would cover the use of pieces of the Rambus technology. (CX 2079, Mooring Micron Depo., at 83-84). The weight of the evidence demonstrates that the industry was made aware that Rambus might have patents that covered more than RDRAMs. (See RRFF 749).

1242. Gary Harmon, former Rambus Chief Financial Officer, was involved in negotiating RDRAM licenses for Rambus in the 1993-96 time frame. (CX2070 at 42 (Harmon, Dep.)). Mr. Harmon recalled being involved in discussions with Oki, Fujitsu, Toshiba and NEC from Japan; LG, Hyundai and Samsung from Korea; and Intel, LSI Logic, IBM, Texas Instruments, and Cirrus Logic from the United States, among others. (CX2070 at 42-43 (Harmon, Dep.)). Mr. Harmon did not recall any discussions on the scope or extent of Rambus patents during these negotiations. (CX2070 at 42 (Harmon, Dep.)).

Rambus's Response to Finding No. 1242:

This proposed finding is contradicted by the evidence. (*See* RRFF 750).

1243. When asked, Mr. Harmon did not tell any of these companies that Rambus might have patents extending beyond RDRAM. (CX2070 at 45-46 (Harmon, Micron Dep.)). Specifically, Mr. Harmon testified that:

> I don't believe we ever specifically stated that we had intellectual property that applied to – outside of the Rambus-compatible area.

(CX2070 at 47 (Harmon, Dep.)). Mr. Harmon also was unaware from discussions with others at Rambus (excluding any privileged communications with counsel) that others had discussions with potential licensees that Rambus technologies might cover SDRAM as well as RDRAM. (CX2070 at 60-61 (Harmon, Dep.)).

Rambus's Response to Finding No. 1243:

The proposed finding is misleading and mischaracterizes the evidence. The testimony of Mr. Harmon quoted by Complaint Counsel did not relate to his licensing discussions generally, but to those involving one particular company. (CX2070, Harmon Depo., at 47). Moreover, Mr. Harmon testified that a license for uses of Rambus technology outside the RDRAM context was discussed with that company. (CX2070, Harmon Depo., at 46). Thus, while Mr. Harmon may not have "specifically stated" that Rambus's intellectual property applied outside the Rambus-compatible area, that would have been the assumption on which the non-Rambus-compatible license was based. Moreover, there is no support in Mr. Harmon's testimony that for the proposed finding's implication that Mr. Harmon was "asked" whether Rambus might have patents extending beyond RDRAM. The proposed finding is also contradicted by other evidence. (*See* RRFF 750).

1244. Howard Sussman, who participated in JEDEC since 1979 as representative for NEC and later Sanyo Semiconductor (Sussman, Tr. 1321-22), first learned about Rambus through a presentation made by a Rambus employee in 1991. (Sussman, Tr. 1429). The content of the presentation focused on what were portrayed as the key features of the Rambus RDRAM, which included the use of a low-voltage CMOS driver and packetized input/output (*Id.* at 1430-31). The presentation did not discuss PLL/DLL, programmable mode register, programmable CAS latency or burst length, or dual edge clock technology. (*Id.* at 1431, 1435-36).

Rambus's Response to Finding No. 1244:

This proposed finding is misleading, not supported by the evidence cited, and

contradicted by the weight of the evidence. The evidence is clear that Mr. Sussman was well aware of Rambus technology prior to Mr. Garrett's presentation in December 1991. (*See* RRFF 751).

1245. No one from Rambus ever suggested to Mr. Sussman that the SDRAM that he and others were standardizing at JEDEC used proprietary Rambus technology, or that Rambus intellectual property rights extended outside the RDRAM architecture. (Sussman, Tr. 1454-55). Mr. Sussman first learned that Rambus was taking the position that its technology covered products outside the RDRAM architecture in late 1999 when news of Rambus patent litigation started to show up in the trade press. (Sussman, Tr. 1455).

Rambus's Response to Finding No. 1245:

This proposed finding is not supported by the evidence. (*See* RRFF 751). Additionally, Mr. Sussman was in attendance for the following events – all of which suggested that Rambus's intellectual property might extend beyond the RDRAM: First, Mr. Sussman was aware as early as 1992 that Rambus might obtain patent rights with respect to features being considered for incorporation into JEDEC Standards, and Rambus did nothing to dispel those concerns. Mr. Sussman was in attendance at the May 1992 JEDEC 42.3 meeting when Richard Crisp declined to comment on Rambus's patent position in response to Gordon Kelley's "point blank" question as to whether Rambus had anything to disclose relating to two-bank design of an SDRAM. (CX0034 at 1; RPF 492; *see* RPF 493-515). Mr. Sussman also was present at a JEDEC 42.3 meeting in September 1995 when Richard Crisp expressly informed the committee that "Rambus elects not to make a specific comment on [Rambus's] intellectual property position relative to the Synclink proposal. Our presence or silence at committee meetings does not constitute an endorsement of any proposal under the committee's consideration nor does it make any statement regarding potential infringement of Rambus intellectual property."

(JX0027 at 26. RPF 536, 544-546). Mr. Sussman was also present in March 1997 when Terry Lee of Micron, and others, indicated that Rambus "had a patent" on the clocking scheme described in an NEC DDR SDRAM presentation. (JX0036 at 1, 7; *see* RPF 567-569.)

1246. In April 1992, Gordon Kelley of IBM attended a presentation by Rambus at IBM comparing the proprietary Rambus RDRAM technology with SDRAM. (G. Kelley, Tr. 2537). Following that presentation, Mr. Kelley believed that the Rambus RDRAM was fundamentally different from the SDRAM technology under discussion at JEDEC and that no intellectual property rights that Rambus had on RDRAM could be applicable to SDRAM or JEDEC. (G. Kelley, Tr. 2537-38, 2546).

Rambus's Response to Finding No. 1246:

The proposed finding is contradicted by more reliable evidence. Contemporaneous documents demonstrate that in June of 1992, Gordon Kelly was concerned about potential Rambus "patent problems" relating to SDRAMs and that he presented those concerns to a meeting of 30 engineers from Siemens and IBM. (RRFF 752).

1247. Prior to the May 1992 JEDEC 42.3 Committee meeting, Mr. Crisp of Rambus had a conversation with Gordon Kelley of IBM about the possibility of Rambus making a presentation at a JEDEC committee meeting, in which Mr. Kelly explained the JEDEC patent disclosure and licensing policies. (See CCFF 907). On the basis of that conversation, Mr. Kelly understood that there was intellectual property on the Rambus proprietary RDRAM technology that he believed Rambus wished to present to JEDEC; Mr. Kelly's understanding was that the intellectual property in issue applied only to the Rambus RDRAM technology. (G. Kelley, Tr. 2504).

Rambus's Response to Finding No. 1247:

The proposed finding is contradicted by other evidence. (*See* RRFF 752).

1248. Through the time that he left JEDEC in 1998 (Kelley, Tr. 2383), Rambus never indicated to Gordon Kelley of IBM that it might have patent rights over on-chip PLL/DLL or dual edge clock technology. (G. Kelley, Tr. 2593).

Rambus's Response to Finding No. 1248:

This proposed finding is incomplete and misleading. Gordon Kelley was aware, based

in part on statements from Rambus, that Rambus might have intellectual property broad enough to cover JEDEC-compliant SDRAM. (*See* RRFF 752.)

1249. Desi Rhoden was employed at Hewlett Packard when he began to learn about the Rambus technology in the early 90's. (Rhoden, Tr. 396). Rambus came to HP to give a presentation about their new memory that they were developing. (*Id.*). The presentation was made pursuant to a non-disclosure agreement between Rambus and HP. (Rhoden, Tr. 521). Although Rambus did not say anything at that presentation about pending Rambus patent applications, though Rhoden assumed that Rambus probably did have patent applications. (Rhoden, Tr. 521). Rambus never suggested that its proprietary technology extended outside the RDRAM architecture, and did not make any statement to suggest that the SDRAM technology being standardized by JEDEC used Rambus intellectual property. (Rhoden, Tr. 521-22).

Rambus's Response to Finding No. 1249:

The proposed finding is misleading because it omits relevant evidence; the implication of the proposed finding that Mr. Rhoden was unaware of the potential scope of Rambus's intellectual property is contradicted by the weight of the evidence. (*See* RRFF 753).

1250. Andreas Bechtelsheim, who at the time was Vice-President for technology at Sun (Bechtelsheim, Tr. 5752), participated in the development of the SDRAM standard before and during the time that Sun was a member of JEDEC. (*Id.* at 5779). At the time the SDRAM standard was developed, Mr. Bechtelsheim had no understanding that there would be a royalty associated with the programmable CAS latency or programmable burst length features. (Bechtelsheim, Tr. 5813-14). Mr. Bechtelsheim's understanding, based on presentations and discussions with Rambus, was that Rambus had patent rights that covered its proprietary RDRAM technology; Rambus did not suggest that their patents extended to SDRAM or other memory architectures. (Bechtelsheim, Tr. 5828-29; 5841-42).

Rambus's Response to Finding No. 1250:

This proposed finding is misleading because it omits relevant evidence. Mr. Bechtolsheim testified not only that he understood Rambus' patent rights to cover its proprietary RDRAM technology, but also that, "[Rambus] made clear is that they were going to protect any patent on their memory technology because that was their business model." (Bechtolsheim, Tr. 5829).

1251. Andreas Bechtelsheim, who had participated in the development of the SDRAM standard as an executive of Sun, learned from press reports in 2000, when he was an employee of Cisco Systems, that Rambus had begun to enforce patents against SDRAM and DDR products. (Bechtelsheim, Tr. 5880). Mr. Bechtelsheim was surprised at the news, because the JEDEC standards had been developed in an open standards process that had a history of making choices that were not encumbered by proprietary patents or royalties. (*Id.*). Before learning of this through press reports in 2000, Mr. Bechtelsheim had not heard any rumor or suggestion that Rambus might have patents that would extend to SDRAM or DDR. (Id. at 5880-81).

Rambus's Response to Finding No. 1251:

This proposed finding is not supported by the evidence. The overwhelming weight of the evidence demonstrates that the definition of an "open standard" as used by JEDEC members did not mean royalty free. (*See* RRFF 1255).

1252. Thomas Landgraf was JEDEC representative for Hewlett Packard at the time that JEDEC was considering the JEDEC DDR standard. (Landgraf, Tr. 1708). At the time he was participating in JEDEC and considering the DDR standard, Mr. Landgraf was unaware of any patents or patent applications on the on-chip PLL or dual-edge clock features. (Landgraf, Tr. 1710-11). As Hewlett Packard's representative at JEDEC, Mr. Landgraf had an expectation that the DDR standards on which he was voting for Hewlett Packard would be free of undisclosed patents. (Landgraf, Tr. 1712). Mark Kellogg, who served as an alternate and later principal representative for IBM to the JEDEC 42.3 Committee (Kellogg, Tr. 5017), first learned about Rambus technology through a presentation by Rambus to IBM in the early 1990's. (Kellogg, Tr. 5052-53). At that time, Mr. Kellogg expected that any Rambus patent activity would be associated with the Rambus proprietary RDRAM product that they were showing to IBM, which was a narrow I/O, high-bandwidth, packetized memory device or card with a loop-back structure and a few other elements. (Kellogg, Tr. 5053). At the presentations by Rambus to IBM, no one from Rambus ever suggested that the Rambus proprietary technology extended outside the RDRAM architecture. (Kellogg, Tr. 5054).

Rambus's Response to Finding No. 1252:

This proposed finding is contradicted by more reliable contemporaneous evidence. Mr. Kellogg's notes of the May 1992 JEDEC meeting clearly indicated that he was concerned about Rambus' patents that may apply to SDRAMs. (Kellogg, Tr. 5319-5324). Mr. Kellogg explained that concerns about Rambus' intellectual property expressed by other companies

raised a "flag" because, "between Siemens and NEC, companies are describing possible intellectual property concerns which may affect our decision process for synchronous DRAM. That is a concern. The lack of response by Rambus is also a concern." (Kellogg, Tr. 5323).

1253. Rambus made a presentation to representatives of Micron in 1995 in connection with discussions between Micron and Rambus about licensing the RDRAM technology. (Lee, Tr. 6605). In preparation for that 1995 meeting, Micron employee Terry Lee reviewed with other Micron employees abstracts of the patents that Rambus had been granted to that time. (Lee, Tr. 6605-08). The intended scope of the review included any prior art pertaining to the patent, as well as the breadth of the patent – that is, whether the patent applied to more than just Rambus. (Lee, Tr. 6608-09; CX0629). In some instances, including the Rambus '703 patent, the text of the patent itself was reviewed. (Lee, Tr. 6609). Based on his review of Rambus patents in 1995, Mr. Lee and his Micron colleagues concluded that the Rambus patents applied specifically to the RDRAM bus architecture, and reported this conclusion to their supervisor at Micron. (Lee, Tr. 6610-11). Micron chose not to take a license from Rambus in 1995. (Lee, Tr. 6613).

Rambus's Response to Finding No. 1253:

The proposed finding is misleading because it omits relevant information. Mr. Lee's conclusions were unreliable because they were based primarily on a review of selected patent abstracts and not on a review of the entire patent including specifications, drawings and claims. (Lee, Tr. 6608).

The proposed finding also is contradicted by more reliable evidence. In March of 1997 Mr. Lee expressed concerns to the JEDEC JC 42.3 committee that a DDR SDRAM presentation "looked like" one of the Rambus patents he had reviewed in 1995. (Lee, Tr. 6956-59). Mr. Lee's contemporaneous "concerns" that a DDR SDRAM presentation looked like a Rambus patent contradicts the proposed factual finding that Lee previously had concluded that the Rambus patents applied specifically to the Rambus bus structure. If Mr. Lee actually had concluded that the Rambus patents were limited to the Rambus bus structure, he should not

have been concerned in 1997.

1254. Officials of AMD only learned in 2000 that Rambus claimed patent rights in the JEDEC standard memory technology used by AMD. (Polzin, Tr. 3987; Heye, Tr. 3730).

Rambus's Response to Finding No. 1254:

This proposed finding is irrelevant. Rambus does not dispute that it first asserted patents against SDRAMs and DDR SDRAMs in late 1999, based on patents that had issued in June 1999 and later. (Stipulated Patent Tree).

1255. Through the 1990's, firms in the computer memory industry continued to believe that the JEDEC standards for SDRAM and DDR were open standards that could be used free of royalty payments to Rambus or anyone else. (See, e.g., CCFF 1256-58).

Rambus's Response to Finding No. 1255:

The proposed finding is contradicted by the weight of the evidence. According to EIA General Counsel and JEDEC President John Kelly, "open standards" did not mean royalty-free. Mr. Kelly testified:

> "Q. And you say, 'open standards by definition are free of restrictive intellectual property or IP rights,' correct?
>
> A. Yes, sir.
>
> Q. And by 'restricted' you mean that there's no objection to having features [in] standards that are protected by valid patents as long as they're available to all comers on reasonable and non-discriminatory terms?
>
> A. Yes, sir."

(Kelly, Tr. 2072).

Numerous contemporaneous documents, and the evidence of JEDEC's actual practice, also make clear that "open" standards may, and often do, include patented features or technologies. As Mr. Kelly explained in a May 2000 letter to a prospective member, "JEDEC standards are open (in terms of IP *licensing*). . . ." (CX0419 at 1) (emphasis added). The EIA's January 1996 letter to the FTC confirms that an "open" standard is one where necessary patent licenses are available to all comers on reasonable terms. (See RX0669 at 4 (. . . "the important issue is the license availability to all parties on reasonable, non-discriminatory terms")). The EIA Legal Guides, which were required to be followed by JEDEC members (Kelly, Tr. 1829-30; CX0206 at 6), similarly provide that it is a "basic objective" of standards-setting that "[s]tandards are proposed or adopted by EIA without regard to whether their proposal or adoption may in any way involve patents on articles, materials, or processes." (CX0204 at 4).

1256. An internal strategic document of Infineon from 1999, comparing the advantages and disadvantages of the RDRAM, SDRAM and DDR memory architectures, describes Rambus with the notation "proprietary standard of Rambus/Intel=>payment of royalties" and shows opposite that a notation for "Double Data Rate" that states "Open standard=>no royalties." (CX2451 at 9; see also *id.* at 13 (table listing DRAM as SDRAM and DDR as "open standards" in contrast to RDRAM); Peisl, Tr. 4430-31). (See also CX2435 at 23; CX2442 at 36).

Rambus's Response to Finding No. 1256:

The proposed finding is contradicted by more reliable evidence. Internal Siemens (now Infineon) documents demonstrate that Siemens was aware, as early as 1992, that evolving SDRAM standards might be covered by Rambus patents. (RPF 469-501). Moreover, the minutes of the March 1997 JC 42.3 meeting, attended by Siemens, reflect that during a presentation regarding an NEC proposal involving DDR SDRAM, a representative stated that "[s]ome on the committee felt that Rambus had a patent on that type of clock design." (JX0036

at 7).

1257. An internal strategic document of Hyundai from 1997 lists as one of the "Strong Points" for DDR SDRAM that it is the "most cost effective next generation DRAM" in part because of its "open architecture without royalties or fees." (CX2294 at 15; *see also id.* at 16 (listing a disadvantage of Rambus "cost due to proprietary design"). (See also CX2297 at 79, 80 (Hyundai, August 1997); CX2264 at 42 (Hyundai, Nov. 1997) ("open standard spec: Direct RDRAM poor, DDR good"); CX2303 at 16, 18 (Hyundai, Feb. 1998) ("Direct Rambus Royalty," DDR SDRAM: "Open Standard (JEDEC)"); CX2334 at 10, 25, 27 (Hyundai, April 1999) (advantages of DDR SDRAM include "open industry spec")).

Rambus's Response to Finding No. 1257:

Rambus does not dispute that the document includes the quoted text. Rambus does dispute that JEDEC members (including Hyundai) equated "open" with royalty-free. (*See* RRFF 1255).

1258. An internal strategic document of Micron from May 1999 compared RDRAM with SDRAM architecture and concluded "Rambus Cost Remains An Issue" in part because of "Extra royalty cost vs. SDRAM." (CX2737 at 56).

Rambus's Response to Finding No. 1258:

This proposed finding is vague and ambiguous. If anything, this proposed finding demonstrates that Micron acknowledged that there would be some royalties on SDRAM – hence the use of the word "extra".

1259. As late as December 1999, Rambus refused to state publicly whether JEDEC standard technology infringed its intellectual property. In an internal email at that time, Rambus CEO Tate noted that Rambus representatives, in a securities analyst conference call, had been asked directly "does DDR infringe your IP?" (CX1089). In response, the company had said that it was analyzing actual memory chip parts to make that determination, and expected to release the results in the first fiscal quarter. (*Id.*) Mr. Tate directed employees who were asked the same question to confine themselves to the same response, and stated "it's important NOT to indicate/hint/wink/etc what we expect the results of our analysis to be!!!" (*Id.*).

Rambus's Response to Finding No. 1259:

This proposed finding is incomplete and misleading. In an August 1997 email Mr. Tate explained that Rambus could not be sure whether DDR SDRAMs/SGRAMs infringed Rambus patents was because there "was so little hard data and no silicon" to examine. (CX0919 at 1). At that point in time Mr. Tate had concluded that "there are no patents we can definitely say are infringed." (*Id.*). Moreover, DDR products did not begin shipping in volume until the year 2000, at the earliest. (Peisl, Tr. 4386; Gross, Tr. 2354 (Compaq first started using DDR SDRAM parts in 2001).

Mr. Tate testified that "we would not want to tell customers that there was possibility of infringement and then find out that there was not infringement. That would be embarrassing ... I think the intent is clear that we would not want to go tell somebody you infringed without being able to back that up. We would not want somebody to tell us that, and vice versa. So we wanted to do some further research." (CX 2074 at 347 (Tate Depo.)). Mr. Tate's decision to wait until Rambus could confirm infringement reflects sound business judgment.

2. Firms With Concerns About Rambus Intellectual Property Claims Came to Believe That Their Suspicions Were Unfounded.

1260. IBM and Siemens in early 1992 had concerns that Rambus might have intellectual property rights with respect to the dual-bank design that was then under consideration by JEDEC in connection with the proposed SDRAM standard. (See CCFF 903-04). However, by the time of the July 1992 meeting of the Committee, at which votes were taken on a number of ballots pertaining to the SDRAM standard, Mr. Kelly of IBM did not understand that Rambus might have any patent rights related to the ballots under consideration. (G. Kelley, Tr. 2562).

Rambus's Response to Finding No. 1260:

The proposed finding is contradicted by contemporaneous evidence. Gordon Kelley was aware that Rambus might have patents, or might be able to acquire patents, that could pertain to

the SDRAM standard. (See RPF 524-26).

1261. Willi Meyer of Siemens was a JEDEC member who in early 1992 had concerns that Rambus might have intellectual property rights with respect to the dual-bank design that was then under consideration by JEDEC in connection with the proposed SDRAM standard. (See CCFF 903-904). However, in late 1993, after reviewing the Rambus WIPO patent application and witnessing Mr. Crisp's disclosure of the Rambus '703 patent to JEDEC in September 1993, Mr. Meyer of Siemens made an internal report to colleagues at Siemens concerning the status of the JEDEC SDRAM efforts in which he stated that by adopting the SDRAM standard JEDEC had managed to define a public domain version of an improved next generation DRAM – that is, a standard in which nothing was covered by someone's intellectual property. (CX2089 at 151-52 (Meyer, Infineon Trial Tr.)).

Rambus's Response to Finding No. 1261:

The proposed finding is inaccurate contradicted by contemporaneous evidence. Mr. Meyer did not testify that the he reviewed Rambus's WIPO (PCT) patent application before his internal report. Moreover, there is ample evidence in the record demonstrating that Siemens believed Rambus had patents that might cover non-RDRAM products, including SDRAMs. (RX0269; RX0286A; RX0289; RX0321; RX0488A (March 1994 memo from Mr. Meyer including the following statement "One day all computers will (have to) be built like this, but hopefully without the royalties going to Rambus.")).

1262. Rambus email traffic in 1997 confirms that Siemens continued to believe that the JEDEC standards were free of patent claims. (CX0939 at 1 (Mooring: "We have not told Siemens that we think SLDRAM and SDRAM-DDR infringe our patents. We think that will just irritate them."); see also CX0939 at 1("We are hoping that they will either drop their competitive efforts or discover for themselves that they have violated Rambus patents ...")).

Rambus's Response to Finding No. 1262:

This proposed finding is not supported by the evidence. This Rambus email does not and cannot confirm *Siemens'* beliefs. Regardless of what Rambus did or did not tell Siemens, it is clear that Siemens suspected that Rambus might, one day, have patents that covered JEDEC-

compliant products. (*See* RRFF 1261). Additionally, Mr. Mooring's email is entirely consistent with the fact that Rambus did not assert any patents against SDRAMs or DDR SDRAMs until 1999. (*See* Stipulated Patent Tree).

1263. Rambus CEO Tate confirmed in sworn testimony in 2001 that at no time from 1990 until 2000 did Rambus tell Siemens or Infineon that Rambus patents covered their SDRAM products or their DDR products. (CX2088 at 75-77 (Tate, Infineon Trial Tr.)). Rambus in June 2000 accused Infineon of patent infringement in connection with its production of SDRAM and DDR products. (CX1127).

Rambus's Response to Finding No. 1263:

Mr. Tate's testimony is entirely consistent with the fact that Rambus did not assert any patents against JEDEC-compliant SDRAM or DDR SDRAM parts until late 1999, and the first of those asserted patents had issued in mid-1999. (*See* Stipulated Patent Tree). After the patents issued, Rambus contacted Infineon with the desire to reach "an amicable solution." (CX1127).

1264. Hyundai entered into a license agreement with Rambus in December 1995. (CX1589 (letter of intent); CX1599, CX1600 (license agreement); CX2107 at 65-66 (Oh, Dep.)). At the time that Hyundai negotiated its license with Rambus in 1995, Hyundai did not believe that Rambus might have patents or patent applications that extended outside the scope of RDRAM. (CX2107 at 69 (Oh, Dep.)). However, Hyundai negotiated a provision in its 1995 license agreement with Rambus that would have permitted Hyundai to use the licensed Rambus intellectual property rights in connection with "Other DRAM, " that is, DRAM chips other than Rambus proprietary RDRAM. (CX1599 at 3, 12). The reason for this provision was to provide an "insurance program" for concerns by Hyundai that Rambus might have intellectual property claims pertaining to the SyncLink technology, which was being developed by a group in which Hyundai was participating. (CX2107 at 75-77, 94-96, 99, CX2108 at 274-78 (Oh, Dep.)). At the time, Hyundai did not know what patent rights Rambus might have, and the general terms of the provision were acceptable to Hyundai as a way of providing for the possibility that Rambus might assert intellectual property claims against SyncLink. (CX2107 at 75-77 (Oh, Dep.)).

Rambus's Response to Finding No. 1264:

This proposed finding is internally inconsistent and supports Rambus's position that

members of the DRAM industry were aware that Rambus had broad inventions that likely extended beyond the RDRAM. If Hyundai truly believed that Rambus's inventions were limited to the RDRAM architecture there was no reason for Hyundai to "negotiate" a license to non-RDRAM products. Moreover, a draft amendment to the license agreement was sent by Rambus to Hyundai in 1998 and expressly listed SDRAM and DDR SDRAM as examples of "Other DRAM" under the agreement. (RX2275 at 1; CX2108, Oh Depo., at 286).

1265. Despite the existence of a provision in its Rambus license agreement that would have given it the general right to use Rambus technology for a specified royalty rate in connection with non-RDRAM compatible products, Hyundai's strategic documents continuing until at least 1999 show that Hyundai believed that JEDEC standard SDRAM and DDR technologies were open and not subject to royalty payment. (CX2294 at 15, 16; CX2297 at 79, 80; CX2264 at 2; CX2303 at 16, 18; CX2334 at 10, 25, 27). Rambus in June 2000 accused Hyundai of patent infringement in connection with its production of SDRAM and DDR products. (CX1129).

Rambus's Response to Finding No. 1265:

This proposed finding is incomplete and misleading. (*See* RRFF 1264).

3. Review Of Public Patent Documents Known to JEDEC Members Would Not Have Placed A Reasonable Practitioner on Notice of Claims by Rambus to JEDEC Standard Technology.

(A) The Original Rambus '898 Patent Application, Which Described The Basic Rambus Invention, Was the Basis for Several Rambus Patents or Applications That Became Matters of Public Record.

1266. The description of the basic Rambus invention contained in the specification portion of the original '898 patent application was the basis for several documents that were publicly available and known to JEDEC members during the time that Rambus was a JEDEC member. (See CCFF 1267). However, JEDEC members who reviewed these documents did not conclude that Rambus claimed or could claim intellectual property rights to the JEDEC standards. (CCFF 1273-76). Moreover, a reasonable engineer reviewing public patent documents in the early to mid-1990's would not have understood that Rambus claimed or could claim rights to the JEDEC Standards**.** (CCFF 1266 et seq.).

Rambus's Response to Finding No. 1266:

The proposed finding is misleading and not supported by the weight of the evidence. The specification portion of the original '898 patent application described a plurality of inventions; therefore, referring to the "basic Rambus invention" is misleading. (See *Rambus Inc. v. Infineon Techs. AG*, 318 F.3d 1081, 1095 (Fed. Cir. 2003) ("[A] multiplexing bus is only one of many inventions disclosed in the '898 application.")).

The evidence, including written, contemporaneous evidence from the early 1990s, shows that JEDEC members that reviewed the PCT application, whose specification is identical in all material respects to the specification of the '898 application, concluded that Rambus claimed or could claim intellectual property rights to features that were eventually included in the JEDEC SDRAM and DDR SDRAM standards. (*See generally* RPF 655-706).

Similarly, the evidence, including written, contemporaneous evidence from the early 1990s, shows that reasonable engineers that reviewed the PCT application, which shares the same specification as the '898 application, did understand that Rambus claimed or could claim intellectual property rights to features that were eventually included in the JEDEC SDRAM and DDR SDRAM standards. (*Id.*).

Furthermore, the four features at issue were clearly disclosed in presentations and detailed technical descriptions given to DRAM companies and systems manufactures in the early 1990s. (RPF 610-637). At least Siemens responded to one of these overviews with detailed questions, some of which were directly related to the four features. (RPF 626-632).

1267. Rambus filed an International Patent Application under the Patent Cooperation Treaty (the PCT application) on April 16, 1991. (CX1454 at 1). The PCT application claimed priority based on Rambus' '898 U.S. application. (CX1454 at 1). The PCT application has the

legal effective filing date of the '898 application, April 18, 1990. (CX1454 at 1; Fliesler, Tr. 8884). The PCT application was published on about October 31, 1991, and thereafter available to the public. (CX1454 at 1). It contains the original text, drawings and 150 original claims of the '898 U.S. application. (CX1454; CX1451).

Rambus's Response to Finding No. 1267:

Rambus has no specific response.

1268. The PCT application would not have alerted a reasonable engineer that Rambus claimed or could claim patent rights over features in JEDEC-compliant SDRAMs and DDR SDRAMs because language in that application, deriving from the Rambus United States '898 application, described a bus architecture that is narrow, multiplexed, packetized and lacking a chip-select network. The bus architecture of a JEDEC-compliant SDRAM does not meet any of these criteria. (Jacob, Tr. 5460-5501; see CCFF 1283 et. seq.).

Rambus's Response to Finding No. 1268:

The proposed finding is contradicted by more reliable evidence. A reasonable engineer reviewing the PCT application would not have understood that Rambus would be restricted to claiming patent rights to inventions limited by a particular bus architecture. (RPF 665-672). For example, documents from the early 1990's produced by Mitsubishi indicate that engineers at Mitsubishi reviewed the PCT application and understood that the inventions disclosed therein could be used independently of each other and the particular bus architectures described therein. (RPF 666, 670-672, 696)

Professor Jacob's testimony is unreliable with respect to what patent rights a reasonable engineer would have understood could be claimed based on the PCT application. Professor Jacob has very little experience with patents, he has never worked as an engineer in the DRAM industry, his opinions in this area are inconsistent, and, in generating his opinions in this area, he failed to consider contemporaneous evidence as to what engineers actually thought when reviewing the PCT application. (See RPF 707-713).

The proposed finding is also inaccurate in stating that the bus architecture of JEDEC-compliant SDRAM is not multiplexed. While the degree of multiplexing in SDRAM is more limited than that described for certain embodiments of the Rambus system described in the '898 application, some multiplexing does occur in the SDRAM bus architecture. (Jacob, Tr. 5465 (acknowledging that there is some "little" multiplexing in the SDRAM bus architecture)). According to Professor Jacob, "multiplexing" simply means that:

> "at different times different information, different classes of information, are transmitted over the same wire. So for example, the main classes of information would be control information, address information, and data, and in a multiplexed bus, for example, if you transmit data and/or address and/or control over the same wire at different points in time, then that would be a multiplexed wire."

(Jacob, Tr. 5464). This is done in SDRAMs. For example, the lines that carry address information also carry control information, namely the values to be programmed into the mode register, at other times. (JX0056 at 116 (during a "Mode Register Set Cycle," "[t]he address lines . . . contain the mode register set opcode and the valid mode information to be written into the mode register.")). As another example, the particular signal line designated "A10" carries address information at certain times and other control information (specifically, information indicating whether the active bank should be precharged) at other times. (JX0056 at 115 ("The user may specify that the bank currently being accessed precharge itself as soon as the burst is completed. This is done by using address bit A10 during the column address cycle.")).

1269. Rambus patent 5,243,703 (the '703 patent) issued September 7, 1993. (CX1460

at 1). The '703 patent claims priority to the '898 application. The '703 patent issued from a divisional application of the '898 application. (CX1460 at 1). The specification and drawings of the '703 patent are substantially the same as the specification and drawings of the '898 specification and drawings. (CX1460; CX1451; Jacob, Tr. 5500-01). In September 1993, Rambus JEDEC representative Richard Crisp notified the JEDEC JC 42.3 Committee that the '703 patent had issued to Rambus. (CCFF 971-73).

Rambus's Response to Finding No. 1269:

Rambus has no specific response.

1270. The '703 patent would not have alerted a reasonable engineer that Rambus claimed or could claim patent rights over features in JEDEC-compliant SDRAMs and DDR SDRAM because language in that issued patent, deriving from the Rambus United States '898 application, described a bus architecture that is narrow, multiplexed, packetized and lacking a chip-select network. The bus architecture of a JEDEC-compliant SDRAM does not meet any of these criteria. (Jacob, Tr. 5460-5501). Moreover, the claims contained in the '703 patent recite particular features that are not contained in the JEDEC standards. (Jacob, Tr. 5492-93, 5497, 5498-99; see CCFF 1351-55).

Rambus's Response to Finding No. 1270:

The proposed finding of fact is incomplete and is contradicted by more reliable evidence. The proposed finding of fact is incomplete because it omits the fact that the '703 patent revealed the existence of 9 additional pending divisional applications that claimed priority to the '898 application, indicating that Rambus was pursuing numerous other inventions based on that application. (CX1460 at 11, RPF 717). Moreover, because the written description and drawings of the '703 patent are substantially the same as the written description and drawings of the '898 application (CCFF 1269), the '703 patent would have alerted a reasonable engineer that Rambus could claim patent rights over features that were included in the JEDEC SDRAM standard for the same reasons that they would have understood that such patent rights could be obtained based on the PCT application. (*See* RRFF 1268).

Professor Jacob's testimony is unreliable with respect to what patent rights a reasonable

engineer would have understood could be claimed based on the '703 patent. Professor Jacob's testimony is unreliable in this area because he has very little experience with patents, he has never worked as an engineer in the DRAM industry, his opinions in this area are inconsistent, and, in generating his opinions in this area, he failed to consider contemporaneous evidence as to what engineers actually thought when reviewing the PCT application, which has the same written description and drawings as the '703 patent. (See RPF 707-713).

1271. At the time that Rambus withdrew from membership from JEDEC, it submitted with its withdrawal letter dated June 17, 1996, a list of issued patents. (CX0887 at 2; CCFF 1109-14). The list was not a complete list of issued patents because the '327 patent was not on the list. (CX0888 at 2; Crisp, Tr. 3381, 3384; Diepenbrock, Tr. 6200).

Rambus's Response to Finding No. 1271:

The proposed finding is incomplete and misleading. Rambus stopped attending JEDEC meetings in December of 1995, and did not pay its January 1996 dues invoice. (RPF 6-7, 414) The June 17, 1996 letter to JEDEC simply formalized Rambus's separation from JEDEC.

Furthermore, the proposed finding is misleading to the extent that it suggests that the '327 patent was intentionally omitted from the list. The only evidence presented at trial on this issue showed that the '327 patent was omitted from the list by mistake. (RPF 561). The proposed finding is also irrelevant because, upon issuance, the '327 was publicly available and the evidence shows that JEDEC members were aware of it. (RX1214 at 1 (July 1998 e-mail circulating list of Rambus patents, including the '327 patent, to numerous JEDEC representatives); RX2216 at 3 (Mitsubishi chart of Rambus patents including the '327 patent)).

1272. None of the patents listed in the Rambus JEDEC withdrawal letter would have alerted a reasonable engineer in the 1990s that Rambus might be able to obtain patent rights over features incorporated in the JEDEC SDRAM or DDR SDRAM standards. (Jacob, Tr. 5502). Each patent on the list is either restricted to a narrow, packetized, multiplexed bus

architecture, addresses topics outside the scope of the JEDEC 42.3 committee, or relates to only minor implementation details of material that could have been within the scope of the 42.3 committee. (Jacob, Tr. 5502; see CCFF 1356-57).

Rambus's Response to Finding No. 1272:

The proposed finding is contradicted by more reliable evidence and is misleading. For reasons stated in response 1271 above, referring to the June 17, 1996 letter to JEDEC as a "withdrawal letter" is misleading.

The proposed finding is contradicted by the fact that some of the patents identified in the list that accompanied the June 17, 1996 letter to JEDEC claim priority to the '898 application, including the '703 patent. (CX0887 at 2). Patents that claim priority to the '898 application have essentially the same specification and drawings at the '898 and PCT applications. (CCFF 1269). Therefore, JEDEC members reviewing the specification and drawings of those patents would have understood that Rambus might be able to obtain patent rights over features in SDRAM for the same reasons set forth in the responses to 1268 and 1270 above.

Even if one considers only the claims of the patents disclosed, the proposed finding contradicts other findings sought by Complaint Counsel. Although Rambus disagrees, Complaint Counsel assert that the SDRAM standard includes low voltage swing signaling. (CCFF 564). However, Professor Jacob has testified that one of the patents on the list accompanying the June 17, 1996 letter was directed at low voltage swing signaling. (Jacob, Tr. 5647).

(B) JEDEC Members Who Reviewed Publicly Available Rambus Patent Documents Did Not Conclude That Rambus Claimed Rights To the SDRAM or DDR Technologies Under Discussion at JEDEC.

1273. Howard Sussman, who participated in JEDEC since 1979 as representative for NEC and later Sanyo Semiconductor (Sussman, Tr. 1321-22), reviewed the European patent application of Rambus in 1992 or 1993. (Sussman, Tr. 1445). His review, which consisted in large part of flipping through the document and looking over the diagrams, led him to conclude that the application resembled the presentation that he had earlier received from Rambus concerning proprietary RDRAM technology. (Sussman, Tr. 1450-51). At the time of his review in 1992 or 1993, Mr. Sussman did not see anything that he believed put him on notice that Rambus might have intellectual property claims on programmable burst length, programmable CAS latency, on-chip PLL or DLL, or dual edge clock technology. (Sussman, Tr. 1451-54).

Rambus's Response to Finding No. 1273:

The proposed finding is misleading because it leaves out relevant information. At the May 1992 JEDEC meeting, Mr. Sussman stated that he had reviewed the PCT application and that he believed that many of the 150 claims contained in the application were barred by prior art. (RPF 769-771). There was no evidence presented that Mr. Sussman made any mention at a JEDEC meeting that he did not feel Rambus might have intellectual property claims on features considered by JEDEC, including programmable burst length, programmable CAS latency, on-chip PLL or DLL, or dual edge clock technology.

The proposed finding is also misleading because it omits the fact that Mr. Sussman testified that, while reviewing the PCT application during his testimony, he recognized that the PCT application disclosed dual edge clock technology. Mr. Sussman testified that Figure 13 of the PCT application shows "input being sampled on the high and low edge of the clock" and that is "double data rate input." (Sussman, Tr. 1322, 1467-68).

1274. According to the Rambus JEDEC representative Richard Crisp, at the May 1992 JC 42.3 Committee meeting, Howard Sussman of NEC commented to the group that he had seen a copy of a Rambus international patent application. (CX2092 at 128 (Crisp, Infineon Trial Tr.). The essence of the comment was that Mr. Sussman had obtained a copy of the application from the foreign patent office, had read it, and said it should not be a concern for the JEDEC standardization effort. (CX2092 at 129 (Crisp, Infineon Trial Tr.)). Mr. Crisp was there, heard the comment, and didn't say anything different. (CX2092 at 130 (Crisp, Infineon Trial Tr.)).

Rambus's Response to Finding No. 1274:

The proposed finding is incomplete and misleading. At the May 1992 JEDEC meeting, Mr. Sussman stated that he had reviewed the PCT application and that he believed that many of the 150 claims contained in the application were barred by prior art. (RPF 769-771). The proposed finding is misleading to the extent that it implies that Mr. Sussman was indicating that the application was not a concern because it was not relevant to the work at JEDEC. To the contrary, the fact that Mr. Sussman expressed his belief that the teachings of the PCT were anticipated by prior art indicates that there would be concern if the claims were not anticipated by prior art – if the technology were not being used, whether or not it was anticipated by prior art would not be relevant.

The proposed finding also is misleading to the extent that it implies that Mr. Crisp had a duty to respond to Sussman's comment or that Mr Crisp had knowledge of any facts that would cause him to have an understanding that conflicted with Mr. Sussman's comment. Complaint Counsel have not satisfied their burden of establishing that Crisp had such knowledge or duty.

1275. Willi Meyer of Siemens was a JEDEC member who in early 1992 had concerns that Rambus might have intellectual property rights with respect to the dual-bank design that was then under consideration by JEDEC in connection with the proposed SDRAM standard. (See CCFF 903-04). However, in late 1993, after reviewing the Rambus international patent application and witnessing Mr. Crisp's disclosure of the Rambus '703 patent to JEDEC in September 1993, Mr. Meyer of Siemens made an internal report to colleagues at Siemens concerning the status of the JEDEC SDRAM efforts in which he stated that by adopting the SDRAM standard JEDEC had managed to define a public domain version of an improved next generation DRAM – that is, a standard in which nothing was covered by someone's intellectual property. (CX2089 at 151-52 (Meyer, Infineon Trial Tr.)).

Rambus's Response to Finding No. 1275:

The proposed finding is incomplete, misleading, and mischaracterizes the evidence. In

the cited testimony, Mr. Meyer did *not* testify that he he had reached his conclusions "after reviewing the Rambus international patent application." To the extent that Mr. Meyer actually was unconcerned about Rambus's intellectual property, the evidence shows that such a lack of concern would likely have been based on the comments Mr. Meyer heard at the September 1993 JEDEC meeting that Rambus's patent applications were "stuck in the patent office" and invalid because they were "a collection of prior art". (RPF 773, CX2057, Meyer Depo., at 300).

The proposed finding is also incomplete and misleading because it fails to mention that in early 1994, Mr. Meyer prepared a memorandum about Rambus which states "[a]ll computers will (have to be) built like this some day, but hopefully without royalties to Rambus." (RPF 534; RX0488A at 1; CX2088, Meyer Infineon Trial Tr., at 124).

The proposed finding is also incomplete because it fails to note that two Siemens engineers were present at the June 1998 meeting of JEDEC's "Future DRAM Task Group," where a guest speaker told the assembled JEDEC members that:

> "Rambus and DDR are *mirror images* of each other when compared."

(CX 132 at 1) (emphasis added).

1276. In connection with discussions between Micron and Rambus about licensing the RDRAM technology in 1995 (Lee, Tr. 6605-05), Micron employees reviewed abstracts of the patents that Rambus had been granted to that time. (Lee, Tr. 6606-08). The intended scope of the review included any prior art pertaining to the patent, as well as the breadth of the patent – that is, whether the patent applied to more than just Rambus. (Lee, Tr. 6609; CX0629). In some instances, including the Rambus '703 patent, the text of the patent itself was reviewed. (Lee, Tr. 6609). Based on this review of Rambus patents, the Micron employees concluded that the Rambus patents applied specifically to the RDRAM bus architecture, and reported this conclusion to their supervisor at Micron. (Lee, Tr. 6610-11).

Rambus's Response to Finding No. 1276:

The proposed finding is misleading and leaves out relevant information. The Micron

employees that reviewed the patent abstracts, and in some cases, the patents, did so in response to a November 7, 1995 memorandum from Jeff Mailloux that included the abstracts of the Rambus patents "granted to Rambus, Inc. so far." (RX0629). One of the many recipients of the memorandum was Terry Walther, a JEDEC representative for Micron. (RX0629).

The proposed finding is misleading to the extent that it implies that Micron performed a complete review of Rambus's patents and was convinced that the patents were limited to only applying to Rambus's proprietary memory architectures. There is a great deal of evidence showing that Micron continued to monitor Rambus's patent portfolio and was fully aware that Rambus had patents that covered more than just Rambus proprietary designs. (RPF 564-86). For example, by March 1997, Terry Lee, who was then a JEDEC representative for Micron and who had participated in the patent review discussed in this proposed finding (Lee, Tr. 6607-09), thought that Rambus might have intellectual property claims relating not just to RDRAMs but to the work of the JC 42.3 committee as well. (RPF 566-72; Lee, Tr. 6961-62). As another example, an April 1997 e-mail responding to a question from Mr. Walther and copying Mr. Lee and others, stated: "Yes, Rambus feels that DDR for any memory is under their patent coverage." (RX0920 at 1).

(C) A Reasonable Engineer Reviewing Public Patent Documents in the Early to Mid-1990's Would Not Have Understood that Rambus Claimed Rights to JEDEC-Standard Technology.

1277. The main parts of a patent or patent application are the specification, which is the written description of the claimed invention, and the claims, which are statements that define the boundaries of an applicant's right to exclude others from making, using or selling. (Nusbaum, Tr. 1496-97).

Rambus's Response to Finding No. 1277:

The proposed finding is vague, misleading and incomplete, for at least the reason that the specification and the written description are not coextensive. A patent or patent application is set forth in a specification. The specification has a written description setting forth a legally sufficient description of the claimed invention. The specification also has claims that define (or will define if issued without revision) the boundaries of the patentee's right to exclude others from making, using, selling, or offering to sell the claimed invention for a limited period of time. (*See* 35 U.S.C. § 112, ¶ 2 ("The specification shall conclude with one or more claims . . . .")).

1278. The content of claims in a pending patent application can provide information beyond that provided by the application's specification. (Fliesler, Tr. 8894-96, 8900-01). There can be a gap between all the claims that a patent application could support, on the one hand, and the claims that the patent applicant actually files, on the other hand. (Fliesler, Tr. 8897-90). There are many reasons that a patent applicant might not pursue all the claims that a patent specification hypothetically could support. (Fliesler, Tr. 8901). Moreover, information as to how a patent applicant interprets its claims in pending applications is valuable information to a competitor that is not available from the application's specification or the claims themselves. (Fliesler, Tr. 8901-02).

Rambus's Response to Finding No. 1278:

Rambus has no specific response.

1279. Rambus filed patent application serial no. 07/510,898 (the '898 application) in the U.S. Patent and Trademark Office (PTO) on April 18, 1990. (CX1451 at 001-02; Nusbaum, Tr. 1507; see DX0014). Various patents or patent applications, some known to JEDEC members during the time Rambus was a JEDEC member or at the time Rambus withdrew from its membership in JEDEC, contained the specification of the original '898 application. (CCFF 730-31, 1342-43, 1351-52). However, as discussed below, the claims in each of these patents or patent applications differed from each other.

Rambus's Response to Finding No. 1279:

The proposed finding leaves out relevant information in that numerous JEDEC members

continued to monitor Rambus's patent portfolio after Rambus sent in a letter confirming its withdrawal from JEDEC. (*See* RPF 562-95).

1280. An engineer or patent lawyer could not have known for certain what claims Rambus would pursue in the '898 family from reading the '898 application, or the identical PCT application. (Fliesler, Tr. 8902).

Rambus's Response to Finding No. 1280:

The proposed finding is incomplete and misleading to the extent that it implies that an engineer or patent lawyer would not have some understanding of what claims Rambus could pursue in the '898 family. An engineer or patent lawyer would have understood that any claims that Rambus could obtain in the '898 family would have to meet the various requirements of the patent laws, including the written description, the enablement requirement, and the best mode requirement. (RPF 78, 86-89). The written description requirement requires that the originally filed application has to clearly disclose to one of ordinary skill in the art to which the patent pertains that the applicant was in possession of the later claimed invention as of the original filing date. (RPF 87).

Furthermore the proposed finding fails to recognize that the '898 application included 150 claims, including claims related to block size (e.g. claims 38-40) and a modifiable access-time register (e.g. claim 103) that would have indicated to an engineer or patent lawyer that these were technologies for which Rambus might seek further patent coverage. (CX1451 at 75, 104). For example, Mitsubishi recognized that claim 103 was directed to programmable latency which was a feature that was being used in SDRAM. (RPF 676-677).

1281. For the reasons set forth below, the description of the inventions contained in the specification set forth in the basis '898 application and reproduced in substance as the specification in each of the patents or patent applications deriving from the '898 application

would not have alerted a reasonable engineer that Rambus claimed patent rights over features in JEDEC-compliant SDRAMs and DDR SDRAMs. (CCFF 1283 et seq.).

Rambus's Response to Finding No. 1281:

The proposed finding is contradicted by more reliable evidence. (*See* RRFF 1282-1340).

1282. For the reasons set forth below, the claims contained in each of the Rambus patents or patent applications known to JEDEC members during and immediately after Rambus was a member of JEDEC would not have alerted a reasonable engineer that Rambus claimed patent rights over features in JEDEC-compliant SDRAMs and DDR SDRAMs. (CCFF 1341 et seq.).

Rambus's Response to Finding No. 1282:

The proposed finding is misleading and contradicted by more reliable evidence. The proposed finding is misleading because it suggests that "Rambus claimed patent-rights over features in JEDEC-compliant SDRAMs and DDR SDRAMs" "during and immediately after Rambus was a member of JEDEC." However, Rambus had no filed claims that would have necessarily read on JEDEC-compliant SDRAMs and DDR SDRAMs until well after it left JEDEC. (RPF 361-96; Stipulated Patent Tree (showing that applications leading to patents that Rambus has asserted against DRAM manufacturers were filed in late 1997 or later)).

Furthermore, much of the evidence upon which Complaint Counsel rely for its proposed findings relating to what a reasonable engineer would have understood in the early 1990's is testimony from complaint counsel's technical expert Prof. Jacob. Professor Jacob's testimony is unreliable in this area because he has very little experience with patents, he has never worked as an engineer in the DRAM industry, his opinions in this area are inconsistent, and, in generating his opinions in this area, he failed to consider contemporaneous evidence as to what engineers actually thought when reviewing patents or patent applications known to JEDEC members

during and immediately after Rambus was a member of JEDEC. (See RPF 707-713).

Finally, if the proposed finding is meant to indicate what reasonable engineers understood about what Rambus *could* claim as opposed to what actually had been claimed, then the proposed finding is contradicted by more reliable evidence, including contemporaneous documents from Mitsubishi. (*See* RRFF 1268, 1270, 1272 above; RPF 669-72, 676-77, 693-702).

(1) The Patent Specification Describing the Basic Rambus Inventions.

1283. The '898 patent application included a descriptive portion, called the "specification," that was 62 pages long and included 15 original drawings. (CX1451 at 3-63, 140-150; Nusbaum, Tr. 1496-97).

Rambus's Response to Finding No. 1283:

The proposed finding is inaccurate and incomplete in that it purports to limit the "specification" of the '898 application to the drawings and 62-page description. The '898 patent specification also included an additional 62 pages that listed 150 claims. (RRFF 1277; CX1451 at 64-125).

The Narrow, Multiplexed Bus of the '898 Specification

1284. The '898 specification describes a narrow, multiplexed bus structure having no chip-select line as the "present invention." (CX1451 at 9-10, 14; Jacob, Tr. 5461-63; Nusbaum, Tr. 1642-43).

Rambus's Response to Finding No. 1284:

The proposed finding is incomplete, misleading, and not supported by the evidence. The proposed finding is misleading in that it implies that a single invention is disclosed in the '898 specification. It is undisputed that multiple inventions were disclosed in the '898 specification.

Rambus Inc. v. Infineon Technologies AG, 318 F.3d 1081, 1095 (Fed. Cir. 2003) ("[A] multiplexing bus is only one of many inventions disclosed in the '898 application."); Stipulated Patent Tree). The proposed finding is also misleading because the cited evidence does not support that "a narrow, multiplexed bus structure having no chip-select line" is described in the specification as "the present invention".

The proposed finding is also misleading to the extent that it implies that all inventions described in the '898 application would be limited to a particular bus structure. Although the specification describes particular embodiments of one of the many inventions as including or working with a particular bus architecture, a reasonable engineer or patent attorney would not have understood that all inventions disclosed in the '898 specification would be limited to such a bus architecture. (RPF 34-39) For example, the experts at Mitsubishi that reviewed the PCT application recognized that various inventions could be separated from the bus. (RPF 666, 669-671).

Furthermore, the proposed finding is incomplete in that it fails to mention the holding of the Federal Circuit that while "clear language characterizing 'the present invention' may limit the ordinary meaning of claim terms, … such language must be read in context of the entire specification and the prosecution history." The Federal Circuit went on to indicate that when taken as a whole, the specification of the '898 application did not limit inventions that could be claimed to those involving a "bus" to a "multiplexing bus". (*Rambus Inc. v. Infineon Technologies AG*, 318 F.3d 1081, 1094-95 (Fed. Cir. 2003)).

1285. The first paragraph of the "Summary of Invention" section of the '898 specification characterizes the "present invention" as having a bus that includes:

> a plurality of bus lines for carrying substantially all address, data and control information needed by said memory devices, where the control information includes device-select information and the bus has substantially fewer bus lines than the number of bits in a single address, and the bus carries device-select information without the need for separate device-select lines connected directly to individual devices.

(CX1451 at 9).

Rambus's Response to Finding No. 1285:

The proposed finding is incomplete and misleading. While the "Summary of the Invention" does contain the language quoted, the proposed finding is misleading to the extent that it implies that a single invention is disclosed in the '898 specification and that the "Summary of the Invention" somehow limits that invention to a bus with specific characteristics. It cannot be disputed that multiple inventions were disclosed in the '898 specification. (*Rambus Inc. v. Infineon Technologies AG*, 318 F.3d 1081, 1095 (Fed. Cir. 2003) ("[A] multiplexing bus is only one of many inventions disclosed in the '898 application"); Stipulated Patent Tree, attached to Parties' First Set of Stipulations). Indeed, the precise language in the "Summary of the Invention" quoted in the proposed finding was considered by the Federal Circuit which held that it did not limit the scope of the inventions that could be claimed based on the '898 application to a particular bus structure. (*Id*. at 1094-95).

The proposed finding is also misleading and incomplete to the extent that it implies that all of the inventions disclosed in the '898 specification are limited to a particular bus structure. (*See* RRFF 1284).

1286. The "Summary of Invention" section also describes the bus: "[i]n the system of this invention, DRAMs and other devices receive address and control information over the bus and transmit or receive requested data over the same bus." (CX1451 at 10).

Rambus's Response to Finding No. 1286:

While the "Summary of the Invention" does contain the quoted text, the proposed finding is incomplete and misleading to the extent that it implies that all of the inventions disclosed in the '898 specification are limited to a particular bus structure. (*See* RRFF 1284).

1287. The specification describes Figure 2 (CX1451 at 130) in the "Summary of Invention" section and states, "[t]he new bus includes clock signals, power and multiplexed address, data and control signals." (CX1451 at 9-10). Figure 2 of the '898 specification depicts the bus organization described in the specification. (Jacob, Tr. 5470).

Rambus's Response to Finding No. 1287:

While the "Summary of the Invention" does contain the quoted text, the proposed finding is incomplete and misleading to the extent it attempts to limit all of the inventions disclosed in the '898 specification to a particular bus structure. (*See* RRFF 1284).

Furthermore, the proposed finding is vague as it is unclear what is meant by "the bus organization described in the specification." The proposed finding is also misleading in that Figure 2 does not in any way indicate that any lines of the bus organization depicted are multiplexed, which is implied by the proposed finding. (CX1451 at 130).

1288. Figure 2 (CX1451 at 130) shows eight multiplexed bus lines that each carry address, control and data information. (Jacob, Tr. 5471). Figure 2 shows that all components in the system share the bus lines. There are no point-to-point connections traveling from the bus master to only one component. (Jacob, Tr. 5471). Figure 2 does not show a chip-select line. (Jacob, Tr. 5472).

Rambus's Response to Finding No. 1288:

The proposed finding is incorrect, not supported by the evidence cited, and contradicted by more reliable evidence. While Figure 2 does not show a chip-select line, and does show all illustrated components in the system sharing some bus lines, Figure 2 does not illustrate "eight

multiplexed bus lines that each carry address, control, and data information." (CX1451 at 130) Further, Prof. Jacob's testimony does not support that "There are no point-to-point connections traveling from the bus master to only one component."

Furthermore, the proposed finding is incomplete and misleading to the extent it implies that all of the inventions disclosed in the '898 specification are limited to a particular bus structure. (*See* RRFF 1284).

1289. The "Summary of Invention" section of the '898 specification states, "[p]ersons skilled in the art will recognize that 16 bus data lines or other numbers of bus data lines can be used to implement the teaching of this invention. (CX1451 at 10). The specification does not state that a bus having more bus lines than the number of bits in an address may be used to implement the teaching of the invention. (CX1451). The specification does not state that a bus having dedicated address, control and data lines may be used to implement the teaching of the invention. (CX1451).

Rambus's Response to Finding No. 1289:

While the "Summary of the Invention" section does include the quoted language, the proposed finding is incomplete and misleading to the extent it implies that all of the inventions disclosed in the '898 specification are limited to a particular bus structure. (*See* RRFF 1284).

Furthermore, the proposed finding is irrelevant in that the specification is not required to disclose every potential embodiment of an invention, such as the specific bus configurations "more bus lines than the number of bits in an address" or "dedicated address, control and data lines." (*See*, *e.g.*, *Gart v. Logitech*, 254 F.3d 1334, 1343 (Fed. Cir. 2001) ("[I]t is well established, however, that broad claims supported by the written description should not be limited in their interpretation to a preferred embodiment.")).

1290. The first paragraph of the "Detailed Description" section of the '898 specification states:

> The present invention is designed to provide a high speed, multiplexed bus for communication between processing devices and memory devices and to provide devices adapted for use in the bus system. . . . The bus carries substantially all address, data and control information needed by devices for communication with other devices on the bus. In many systems using the present invention, the bus carries almost every signal between every device in the entire system. There is no need for separate device-select lines since device-select information for each device on the bus is carried over the bus. There is no need for separate address and data lines because address and data information can be sent over the same lines. Using the organization described herein, very large addresses (40 bits in the preferred implementation) and large data blocks (1024) bytes) can be sent over a small number of bus lines (8 plus one control line in the preferred implementation).

(CX1451 at 13-14).

Rambus's Response to Finding No. 1290:

While the "Detailed Description" section does include the quoted language, the proposed finding is incomplete and misleading to the extent it implies that all of the inventions disclosed in the '898 specification are limited to a particular bus structure. (*See* RRFF 1284). Indeed, the precise language in the "Detailed Description" quoted in the proposed finding was considered by the Federal Circuit which held that it did not limit the scope of the inventions that could be claimed based on the '898 application to a particular bus structure. (*Rambus Inc. v. Infineon Technologies AG*, 318 F.3d 1081, 1094-95 (Fed. Cir. 2003)).

1291. The description of the bus in the '898 specification as having "substantially fewer bus lines than the number of bits in a single address" indicates that the bus will have relatively few lines and be narrow. For instance, if an address requires 24 bits, the bus will have substantially fewer lines than 24. (Jacob, Tr. 5463-64).

Rambus's Response to Finding No. 1291:

The proposed finding is vague in that it is unclear what is meant by "relatively few lines"

and "narrow".

The proposed finding is incomplete and misleading to the extent it implies that all of the inventions disclosed in the '898 specification are limited to a particular bus structure. (*See* RRFF 1284).

1292. The bus used with a JEDEC-compliant SDRAM does not have "substantially fewer bus lines than the bits in a single address." A typical SDRAM bus has over 100 lines and is wider than the number of bits in the address. (Rhoden, Tr. 401; Jacob, Tr. 5464).

Rambus's Response to Finding No. 1292:

The proposed finding is contradicted by more reliable evidence. The JEDEC SDRAM standard as originally published showed no SDRAM configuration with more than 26 bus lines. (RRFF 718).

1293. The term "multiplexed" means that at different times different classes of information are transmitted over the same wires. The bus lines described in the '898 specification are multiplexed because each can carry address, data and control signals at different times. (Jacob, Tr. 5464-65).

Rambus's Response to Finding No. 1293:

The proposed finding is misleading and vague. The proposed finding is vague in that it is unclear as to what is meant by "the bus lines described in the '898 specification." It is true that the BusData lines used with a preferred embodiment described in the '898 application are multiplexed to carry address, data, and control information. According to the Federal Circuit, "Multiplexing refers to the sharing of a single set of lines to send multiple types of information." (*Rambus Inc. v. Infineon Technologies AG*, 318 F.3d 1081, 1094 (Fed. Cir. 2003)). The Federal Circuit further held that a person of ordinary skill in the art would interpret "bus" as used in the claims of Rambus's asserted patents simply as "a set of signal lines to which a number of

devices are connected, and over which information is transferred between devices" (*id*. at 1095), without any "multiplexed" limitation.

The proposed finding is misleading because a bus line does not need to carry all three (or even two) of address, data, and control information in order to be considered a multiplexed line. For example, a prior art patent that is acknowledged in the background section of the '898 application is described "as the current state-of-the-art interface" in which "[t]he address is two-way multiplexed, and there are separate pins for data and control…" (CX1451 at 6). Furthermore, some multiplexing occurs in JEDEC-compliant SDRAM bus structures, as Professor Jacob has conceded. (RRFF 1268).

1294. The subsection of the "Detailed Description" section of the '898 specification entitled "Bus" describes a bus architecture having eight "BusData" lines that are multiplexed to carry address, control and data information. This subsection describes no other bus architecture. (CX1451 at 20-21).

Rambus's Response to Finding No. 1294:

The proposed finding is misleading to the extent it implies that all of the inventions disclosed in the '898 specification are limited to a particular bus structure. (*See* RRFF 1284).

1295. The bus used with a JEDEC-compliant SDRAM has dedicated address lines, dedicated data lines and dedicated control lines. The dedicated lines carry only one type of information. The bus lines used with a JEDEC-compliant SDRAM are not multiplexed to carry address, data and control information. (Rhoden, Tr. 401; Jacob, Tr. 5465).

Rambus's Response to Finding No. 1295:

The proposed finding is not supported by the weight of the evidence. Some multiplexing occurs in JEDEC-compliant SDRAM bus structures, as Professor Jacob has conceded. (RRFF 1268).

1296. The invention described in the '898 specification has "no need for separate

device-select lines since device-select information for each device on the bus is carried over the bus." (CX1451 at 14). This indicates that the bus system described in the '898 specification does not have a chip select network for indicating which chips should respond to commands. (Jacob, Tr. 5495-96).

Rambus's Response to Finding No. 1296:

The proposed finding is misleading to the extent it implies that all of the inventions disclosed in the '898 specification are limited to a particular bus structure. (*See* RRFF 1284). The proposed finding is also misleading because a statement that a bus architecture has "no need" for separate device-select lines, does not require an absence of such lines. (CX1451 at 14).

1297. A JEDEC-compliant SDRAM uses a separate chip-select network. (Jacob, Tr. 5465). A chip-select line is a wire in JEDEC architecture that is used to identify a "rank" or module of DRAMs for responding to commands. (Jacob, Tr. 5471-72).

Rambus's Response to Finding No. 1297:

The proposed finding is incorrect and vague. A JEDEC-compliant SDRAM only has one chip select input, and therefore the concept of a "chip select network" for a single SDRAM device does not make sense. (JX0056 at 21 (noting that S\ denotes chip select), 108 (showing a single S\ input at pin 15)). Furthermore, the proposed finding is vague as to "JEDEC architecture."

The Packetized System of the '898 Specification

1298. The '898 specification describes a packetized system. (Jacob, Tr. 5466). A packet is a bundle of information that is sent over a bus in multiple cycles of time. (Jacob, Tr. 5466).

Rambus's Response to Finding No. 1298:

The '898 specification does describe embodiments that utilize packets to transmit

information between devices. However, the proposed finding is misleading to the extent that it implies that all of the inventions disclosed in the '898 specification are limited to a particular bus structure or packetized system. (See RRFF 1284).

1299. Because the system described in the '898 specification sends addresses, control signals and data blocks over a small number of bus lines (relative to the number of bits in the address), that information is sent over the bus in multiple cycles of time, which together are a packet. (CX1451 at 17; Jacob, Tr. 5466).

Rambus's Response to Finding No. 1299:

The proposed finding is not supported by the cited evidence and is also misleading and vague. The cited testimony and portion of the '898 specification do not indicate the causality implied by the proposed finding, namely that a packet results from sending "address, control signals, and data blocks over a small number of bus lines (relative to the number of bits in a single address)."

The proposed finding is vague because the description of a "packet" as "that information [which] is sent over the bus in multiple cycles of time" is confusing and unclear.

In addition, the proposed finding is incomplete and misleading to the extent that it implies that all of the inventions disclosed in the '898 specification are limited to a particular bus structure. (*See* RRFF 1284).

1300. The "Detailed Description" section of the '898 specification contains a subsection entitled "Protocol and Bus Operation" at pages 19-28. (CX1451at 21-30). That subsection includes a description of Figure 4 (CX1451 at 131) starting on page 21. (CX1451at 23).

Rambus's Response to Finding No. 1300:

Rambus has no specific response.

1301. Figure 4 of the '898 specification illustrates a preferred implementation of the invention in which a request packet is transmitted over nine bus lines over six bus cycles.

(CX1451 at 23-24, 131; Jacob, Tr. 5474-75). Each of the bus lines in Figure 4 is multiplexed to carry data, address or control information. (Fliesler, Tr. 8911-12).

Rambus's Response to Finding No. 1301:

The proposed finding is misleading in that it implies that only a single invention is disclosed in the '898 application. It cannot be disputed that multiple inventions were disclosed in the '898 specification. (*Rambus Inc. v. Infineon Technologies AG*, 318 F.3d at 1095) ("[A] multiplexing bus is only one of many inventions disclosed in the '898 application."); Stipulated Patent Tree, attached to Parties' First Set of Stipulations). The proposed finding is also misleading to the extent that it implies that "the invention" is somehow limited to the particular packet structure shown in Figure 4. (*See*, *e.g.*, *Gart v. Logitech*, 254 F.3d 1334, 1343 (Fed. Cir. 2001) ("[I]t is well established, however, that broad claims supported by the written description should not be limited in their interpretation to a preferred embodiment.")).

1302. The first bus cycle of the packet shown in Figure 4 indicates four bits to specify "access type." (CX1451 at 131; Jacob, Tr. 5475; Fliesler, Tr. 8912). The access type information indicates whether the memory should perform a read or write, the type of access, and the timing (access time) of the response. (CX1451 at 24-25, 27; Jacob, Tr. 5475; Fliesler, Tr. 8912-13).

Rambus's Response to Finding No. 1302:

The proposed finding is misleading and leaves out relevant information. In a preferred embodiment discussed in the '898 application the four "access type" bits do indicate the type of operation to perform. However, the proposed finding is misleading because it omits that the timing of the response is determined by a value stored in an access time register. (CX 1451 at 25 ("AccessType[1:2] preferably indicates the timing of the response, which is stored in an access-time register.")).

The proposed finding is also misleading to the extent that it implies that the inventions disclosed in the '898 application would be limited to the particular packet structure shown in Figure 4. (*See* RRFF 1301).

1303. The last four bits of information transmitted in the sixth bus cycle shown in the packet of Figure 4 give block size information. The block size information specifies the size of the data block to be transferred. (CX1451 at 29-30, 131; Jacob, Tr. 5475-76).

Rambus's Response to Finding No. 1303:

Four bits of information in the packet of Figure 4 do indicate block size information, which specifies the size of the data block to be transferred. However, the proposed finding is misleading to the extent that it implies that the inventions disclosed in the '898 application, and particularly inventions relating to block size, would be limited to the particular packet structure shown in Figure 4. (*See* RRFF 1301).

1304. The '898 specification does not describe the implementation of a request packet, other than that of Figure 4. (CX1451 at 23-24). The specification does not describe transmission of a read or write request in a non-packetized system. (CX1451; Jacob, Tr. 5476-77).

Rambus's Response to Finding No. 1304:

The proposed finding is misleading to the extent that it implies that the inventions disclosed in the '898 application would be limited to the particular packet structure shown in Figure 4. (*See* RRFF 1301).

1305. The specification does not describe transmission of a read or write request over any bus other than one having substantially fewer bus lines than bits in a single address and having multiplexed lines for carrying address, control and data information. (CX1451; Jacob, Tr. 5476-77).

Rambus's Response to Finding No. 1305:

The proposed finding is misleading to the extent that it implies that all the inventions

disclosed in the '898 application are limited to a particular bus structure. (*See* RRFF 1284).

1306. JEDEC-compliant SDRAM does not operate as a packetized system such as that described in the '898 specification. (Jacob, Tr. 5467). The JEDEC SDRAM architecture does not transmit request information over a small number of multiplexed bus wires over multiple bus cycles. (Jacob, Tr. 5476). The JEDEC SDRAM architecture transmits request information over dedicated bus wires over one bus cycle for the column address and one bus cycle for the row address. (Rhoden, Tr. 402-04; Jacob, Tr. 5477).

Rambus's Response to Finding No. 1306:

The proposed finding is misleading and not supported by the evidence cited. That "[t]he JEDEC SDRAM architecture transmits request information over dedicated bus wires over one bus cycle for the column address and one bus cycle for the row address." is not supported by the cited testimony. Indeed, SDRAMs do not use "dedicated" bus lines – some multiplexing occurs, as Professor Jacob has conceded. (RRFF 1268).

The proposed finding is also misleading to the extent that it implies that the inventions disclosed in the '898 application would be limited to a particular packet structure or a particular bus structure. (*See* RRFF 1284, 1301).

1307. Because the system described in the '898 specification does not include a chip-select line, it encodes information for designating a particular DRAM to respond to a request in a packet. (Jacob, Tr. 5472). When the bus master sends a packet to the memory system, every DRAM in the system must decode that packet and determine from the identification information in the packet if the packet is designated for that particular DRAM, or some other DRAM in the system. (CX1451 at 22-23; Jacob, Tr. 5472).

Rambus's Response to Finding No. 1307:

The proposed finding is misleading to the extent that it implies that the inventions disclosed in the '898 application would be limited to a particular embodiment disclosed therein. (*See* RRFF 1284, 1301).

1308. JEDEC-compliant SDRAM use a separate chip-select network. They do not

receive identification information in request packets. (Jacob, Tr., 5465, 5471-72).

Rambus's Response to Finding No. 1308:

The proposed finding is vague and not supported by the cited evidence. A JEDEC-compliant SDRAM only has one chip select input, and therefore the concept of a "chip select network" for a single SDRAM device does not make sense. (RRFF 1297).

Description of Block Size in the '898 Specification

1309. The '898 specification describes the operation of the block size feature at pages 27 and 28. (CX1451 at 29-30). This portion of the specification includes a table illustrating that the block size can be varied from 0 to 1024 bytes. (CX1451 at 30; Jacob, Tr. 5477-78).

Rambus's Response to Finding No. 1309:

The proposed finding is misleading and omits relevant information. While it is true that a block size discussion is present in the '898 application at pages 27 and 28 and includes a table, the proposed finding omits the language directly below the table: "Persons skilled in the art will recognize that other block size encoding schemes or values can be used." (CX1451 at 30). The table referred to in this proposed finding is also present in claim 40 of the original 150 claims filed with the '898 application. (CX1451 at 75).

The proposed finding is also misleading to the extent that it implies that the inventions disclosed in the '898 application are limited to a particular embodiment disclosed therein. (*See* RRFF 1284, 1301).

1310. The last four bits of information transmitted in the sixth bus cycle shown in the packet of Figure 4 (CX1451 at 131) in the '898 specification give block size information. The block size information specifies the size of the data block to be transferred. (CX1451 at 29-30, 131; Jacob, Tr. 5475-77; Fliesler, Tr. 8918).

Rambus's Response to Finding No. 1310:

The proposed finding is misleading to the extent that it implies that the inventions disclosed in the '898 application would be limited to a particular embodiment disclosed therein. (*See* RRFF 1284, 1301).

1311. Because, in the system described in the '898 specification, the block size information is transmitted with each request packet, the block size information can be easily and efficiently changed with each new request. (Jacob, Tr. 5479; Fliesler, Tr. 8919).

Rambus's Response to Finding No. 1311:

The proposed finding is misleading to the extent that it implies that the inventions disclosed in the '898 application would be limited to a particular embodiment disclosed therein. (*See* RRFF 1284, 1301).

1312. In a JEDEC-compliant SDRAM, the burst length feature is programmed during initialization. (JX0056 at 114; Fliesler, Tr. 8920). The burst length is typically set once at system start-up and never changed again. The burst length cannot be easily and efficiently changed with each new request. (Jacob, Tr. 5479).

Rambus's Response to Finding No. 1312:

The proposed finding is misleading and leaves out relevant information. In fact, the mode register in JEDEC-compliant SDRAM can be reprogrammed during regular operation, and the setting of the burst length feature by changing that register is not restricted to system initialization. This is made clear in the section of the JEDEC SDRAM standard relating to the mode register which states: "During operation, this register (and therefore operation of the chip) may be changed, according to the requirements of the Mode-Register-Write Timing diagram. So, while operating in one mode, for example Burst of 4 in sequential addresses; it can change to Burst of 8 in interleaved address mode." (JX0056 at 114).

1313. The JEDEC SDRAM standard requires only two possible values for the burst length, four and eight. (JX0056 at 114).

Rambus's Response to Finding No. 1313:

The proposed finding is vague, misleading, and incomplete. The proposed finding is vague in that it does not specify to which revision of the JEDEC SDRAM standard it is referring. The proposed finding is also misleading and incomplete because it fails to mention that revision 4 of the 21-C JEDEC SDRAM standard uses three bits to specify the burst length, thus allowing for eight different possible burst length values. (JX0056 at 114). The table shown in revision 4 of the 21-C standard under the title "SDRAM Mode Register" also shows three specifically contemplated optional burst length values, 1, 2 and full page. (*Id.*). The remaining burst length encodings are "reserved" for future use. (*Id.*).

1314. The variable block size feature described in the '898 specification addresses a scheduling problem inherent in the narrow, multiplexed, packetized bus system of the '898 specification. An inefficiency results from the data and address information sharing relatively few bus lines. The variable block size feature increases efficiency by maximizing the amount of data that can be transferred in response to a request as needed. (Jacob, Tr. 5479-80). The description and use of the variable block size feature described in the '898 specification in inherently tied to the narrow, multiplexed bus architecture and packetized system. (Jacob, Tr. 5479-81).

Rambus's Response to Finding No. 1314:

The proposed finding is incorrect and misleading. The variable block size feature described in the '898 specification is not "inherently tied to the narrow, multiplex bus architecture and packetized system." Rambus has obtained broad patents based on the '898 application that encompass the use of variable burst in SDRAM devices (*see, e.g.*, CCFF 1666-68); thus, the PTO has determined that the concept of variable block size is not "inherently tied" to any preferred bus architecture disclosed in the '898 application.

The proposed finding is also misleading to the extent that it implies that the inventions disclosed in the '898 application are limited to a particular embodiment disclosed therein. (*See* RRFF 1284, 1301).

1315. The '898 specification explains, "[t]ransfers of long blocks of data use the bus efficiently even without overlap because the overhead due to bus address, control and access times is small compared to the total time to request and transfer the block. (CX1451 at 18).

Rambus's Response to Finding No. 1315:

Although the '898 specification does include the quoted language, the proposed finding is misleading to the extent that it implies that the inventions disclosed in the '898 application are limited to a particular embodiment disclosed therein. (*See* RRFF 1284, 1301).

1316. The '898 specification describes the use of a variable block size feature only in the context of a narrow, multiplexed bus architecture and a packetized system. (Jacob, Tr. 5478). The '898 specification does not describe the use of a variable block size feature in any other context, including in the context of a DRAM generally. (Jacob, Tr. 5478).

Rambus's Response to Finding No. 1316:

The proposed finding is misleading to the extent that it implies that the inventions disclosed in the '898 application would be limited to a particular embodiment disclosed therein. (*See* RRFF 1284, 1301).

1317. In a JEDEC-compliant SDRAM, the programmable burst length feature is present as a convenience. It is not needed to address the bus scheduling and inefficiency concerns generated by the use of a narrow, multiplexed bus. (Jacob, Tr. 5480).

Rambus's Response to Finding No. 1317:

The proposed finding is misleading in describing the programmable burst length feature in SDRAMs as merely a "convenience." Indeed, JEDEC chose to retain the programmable burst length feature in DDR SDRAMs despite undisputed knowledge of Rambus's patent

claims. (RPF 754-58).

1318. An engineer reading the '898 specification in the early to mid-1990s would not have thought that Rambus could obtain patent rights over the programmable burst length feature as it is used in JEDEC SDRAM due to the difference between the JEDEC system and the system described in the '898 specification. (Jacob, Tr. 5480-81).

Rambus's Response to Finding No. 1318:

The proposed finding is incorrect and not supported by contemporaneous evidence. The evidence upon which Complaint Counsel rely for its proposed findings relating to what a reasonable engineer would have understood in the early 1990's is testimony from complaint counsel's technical expert Professor Jacob. Professor Jacob's testimony is unreliable in this area because he has very little experience with patents, he has never worked as an engineer in the DRAM industry, his opinions in this area are inconsistent, and, in generating his opinions in this area, he failed to consider contemporaneous evidence as to what engineers actually thought when reviewing patents or patent applications known to JEDEC members during and immediately after Rambus was a member of JEDEC. (See RPF 707-713).

The proposed finding is also misleading to the extent that it implies that all inventions described in the '898 application are limited to the particular embodiments disclosed therein. Although the specification describes a particular embodiment of one of the many inventions as including or working with a particular bus architecture, a particular packet structure, etc., a reasonable engineer or patent attorney would not have understood that all inventions disclosed in the '898 specification would be limited to such specific embodiments. (RPF 34-39; *see*, *e.g.*, *Gart v. Logitech*, 254 F.3d 1334, 1343 (Fed. Cir. 2001) ("[I]t is well established, however, that broad claims supported by the written description should not be limited in their interpretation to

a preferred embodiment.")). More reliable contemporaneous evidence also illustrates that the experts at Mitsubishi that reviewed the PCT application in the early 1990s recognized that various inventions could be separated from any particular bus architecture disclosed therein. (RPF 666, 669-671).

The proposed finding is also incomplete in failing to mention the holding of the Federal Circuit that, from the standpoint of a person of skill the art, the specification of the '898 application did not limit the inventions disclosed therein to a "multiplexing bus." (*Rambus Inc. v. Infineon Technologies AG*, 318 F.3d at 1094-95).

Description of Access Time in the '898 Specification

1319. In the system described in the '898 specification, the memory device responds to a read request packet or a write request after waiting the specified access time. (CX1451 at 17; Jacob, Tr. 5481).

Rambus's Response to Finding No. 1319:

The proposed finding is misleading to the extent that it implies that a read request must be received in the form of a packet. The cited testimony of Professor Jacob states that "[a]ccess time refers to the transpiring of time between … the receiving of a request and the response to that request."

1320. As described in the '898 specification, each request packet contains information that specifies the access time. (CX1451 at 23, 25, 29; Jacob, Tr. 5482). This allows the bus master to efficiently change the access time with each new request packet. (CX1451 at 29, Jacob, Tr. 5483).

Rambus's Response to Finding No. 1320:

The proposed finding is misleading and incomplete. The proposed finding is misleading to the extent that it implies that the inventions disclosed in the '898 application would be limited

to a particular embodiment disclosed therein. (*See* RRFF 1284, 1301).

The proposed finding is also misleading and incomplete in implying that the '898 specification does not teach that a value representing the access time is stored in a register, but instead is received with each request. The '898 application clearly describes the use of a register to store a value that represents the amount of time to transpire between receipt of a request and the appropriate response. (CX1451 at 16 ("In a preferred implementation, semiconductor devices…contain access time registers which store a set of one or more delay times at which the device can or should be available to send or receive data."); CX1451 at 25 ("AccessType[1:2] preferably indicates the timing of the response, which is stored in an access-time register.")).

1321. In a JEDEC SDRAM, the CAS latency is programed at system start-up. The CAS latency is not changed during operation. The CAS latency cannot be changed with each request. (JX0056 at 114; Jacob, Tr. 5483; Fliesler, Tr. 8920).

Rambus's Response to Finding No. 1321:

The proposed finding is misleading and leaves out relevant information.

The proposed finding is misleading because it implies that the fact that CAS latency is programmed at system start-up in an SDRAM distinguishes it from the preferred embodiment described in the '898 application. In fact, the '898 application states that the access time registers are "preferably are set as part of an initialization sequence that occurs when the system is powered up or reset." (CX1451 at 16).

The proposed finding also fails to indicate that the mode register in JEDEC-compliant SDRAM can be reprogrammed during regular operation, and the setting of the CAS latency feature by changing that register is not restricted to only occurring at initialization. The 21-C standard states that "During operation, this register (and therefore operation of the chip) may be

changed, according to the requirements of the Mode-Register-Write Timing diagram. So, while operating in one mode, for example Burst of 4 in sequential addresses; it can chance to Burst of 8 in interleaved address mode." (JX0056 at 114).

The proposed finding is also misleading in its characterization of the cited testimony. Professor Jacob testified that "…in the JEDEC mechanism you have to change the programmable CAS latency value through a special initialization or a special command…and you can't change it on a request-by-request basis without going through that special command." (Jacob, Tr. 5483).

1322. The implementation of the access time feature described in the '898 specification is inherently tied to narrow, multiplexed bus and packetized system described in the specification. (Jacob, Tr. 5483-84). By allowing changes to the access time on a request-by-request basis, the system described in the '898 specification resolves inefficiencies that result from the use of a narrow, multiplexed, packetized bus in which address and control information must share lines with data. (Jacob, Tr. 5484).

Rambus's Response to Finding No. 1322:

The proposed finding is incomplete and misleading. The programmable access time feature described in the '898 specification is not "inherently tied to the narrow, multiplex bus architecture and packetized system." Rambus has obtained broad patents based on the '898 application that encompass the use of programmable access time (CAS latency) in SDRAM devices (see, e.g., CCFF 1661-62); thus, the PTO has determined that the concept of programmable access time is not "inherently tied" to any preferred bus architecture disclosed in the '898 application.

The proposed finding is also misleading to the extent that it implies that the inventions disclosed in the '898 application are limited to a particular embodiment disclosed therein. (*See*

RRFF 1284, 1301).

Furthermore, the proposed finding is incomplete in neglecting to mention that the '898 application contemplates a device in which a single access time register is used, thus removing the ability to change the access time on a request-by-request basis. (CX1451 at 16-17 ("Each slave may have one or several access-time registers (four in a preferred embodiment). In a preferred embodiment, one access-time register in each slave is permanently or semi-permanently programmed with a fixed value to facilitate certain control functions.")). As Professor Jacob explained, the '898 application describes an embodiment in which an "AccessType" field in a request packet can select different access times by specifying different access time registers containing different values (CX1451 at 29; Jacob, Tr. 5481-82). This cannot be done when there is only a single access time register.

1323. The specification explains that the access time allows the shared bus to be used for other requests during the access time: "The bus to be used in the intervening bus cycles [between request and response] by the same or other masters for additional requests or brief bus accesses. Thus, multiple, independent accesses are permitted, allowing maximum utilization of the bus for transfer of short blocks of data." (CX1451 at 17-18).

Rambus's Response to Finding No. 1323:

The proposed finding is misleading because it implies that the only use of the access time register in the embodiments described in the '898 application is to allow multiple independent access to coexist in the bus architecture. As set forth in the application, another advantage of the access time register is to ensure that the speed of the memory device is coordinated with the clock speed. (CX1451 at 22 ("To reduce the complexity of the slaves, a slave should preferably respond to a request in a specified time, sufficient to allow the slave to begin or possibly complete a device-internal phase including any internal actions that must

precede the subsequent bus access phase.")).

The proposed finding is also misleading to the extent that it implies that the inventions disclosed in the '898 application are limited to a particular embodiment disclosed therein. (*See* RRFF 1284, 1301).

1324. The '898 specification does not describe the use of access time in any context other than the context of a narrow, multiplexed bus operating in a packetized system. (Jacob, Tr. 5476-77).

Rambus's Response to Finding No. 1324:

The proposed finding is vague and misleading. The proposed finding is vague as it is unclear whether the reference to "access time" is meant to refer to "programmable access time" or "programmable latency" that can be accomplished through the use of an access-time register. The proposed finding is also misleading to the extent that it implies that the inventions disclosed in the '898 application would be limited to a particular embodiment disclosed therein. (*See* RRFF 1284, 1301).

1325. In a JEDEC SDRAM, programmable CAS latency is used as a convenience to allow parts that have different performance to exist in the same system. (Jacob, Tr. 5484).

Rambus's Response to Finding No. 1325:

The proposed finding is not supported by the weight of the evidence. Professor Jacob did not attempt to quantify the cost that would be involved in dispensing with programmable CAS latency. (Jacob, Tr. 5643-44). The evidence shows that programmable latency is much more than a "convenience" to DRAM manufacturers because of the costs that would be incurred in producing multiple fixed latency parts instead. (RPF 810-39).

1326. Because of the difference between the implementation and function of access time in the '898 specification and programable CAS latency as used in the JEDEC SDRAM

standard, an engineer reading the '898 application in the early to mid-1990s would not have understood that Rambus might obtain patent rights over programmable CAS latency as that feature was used in the JEDEC SDRAM standard. (Jacob, Tr. 5484-85).

Rambus's Response to Finding No. 1326:

The proposed finding is incomplete, misleading and contradicted by more reliable evidence. Documents from the early to mid-1990s produced by Mitsubishi indicate that engineers at Mitsubishi reviewed the PCT application (which included the same written description and 150 claims as the '898 application) and understood that the inventions disclosed therein could be used independently of each other and the particular bus architectures described therein. (RPF 666, 670-672, 696). Mitsubishi recognized that claim 103 was directed to programmable latency which was a feature that was being used in SDRAM. (RPF 676-677).

The evidence upon which Complaint Counsel rely for its proposed findings relating to what a reasonable engineer would have understood in the early 1990's is testimony from complaint counsel's technical expert Professor Jacob. Professor Jacob's testimony is unreliable in this area because he has very little experience with patents, he has never worked as an engineer in the DRAM industry, his opinions in this area are inconsistent, and, in generating his opinions in this area, he failed to consider contemporaneous evidence as to what engineers actually thought when reviewing patents or patent applications known to JEDEC members during and immediately after Rambus was a member of JEDEC. (See RPF 707-713).

The proposed finding is also misleading to the extent that it implies that all inventions described in the '898 application are limited to the particular embodiments disclosed therein. Although the specification describes a particular embodiment of one of the many inventions as including or working with a particular bus architecture, a particular packet structure, etc., a

reasonable engineer or patent attorney would not have understood that all inventions disclosed in the '898 specification would be limited to such specific embodiments. (RPF 34-39; *see Gart v. Logitech*, 254 F.3d 1334, 1343 (Fed. Cir. 2001) ("[I]t is well established, however, that broad claims supported by the written description should not be limited in their interpretation to a preferred embodiment.")).

The proposed finding is also incomplete in failing to mention the holding of the Federal Circuit that, from the standpoint of a person of skill the art, the specification of the '898 application did not limit the inventions disclosed therein to a "multiplexing bus." (*Rambus Inc. v. Infineon Technologies AG*, 318 F.3d at 1094-95).

Description of the Clocking Scheme in the '898 Specification

1327. In the "Background of the Invention" section, the '898 specification states "The clocking scheme used in this invention has not been used before . . .". (CX1451 at 7).

Rambus's Response to Finding No. 1327:

The proposed finding is incorrect and misleading. The quoted language does not appear in the "Background of the Invention" section of the '898 application. The quoted language appears in the "Comparison with Prior Art" section (CX1451 at 5-7). The proposed finding is also misleading to the extent that it implies that the inventions described in the '898 application are limited to a particular clocking scheme disclosed therein. (*See* RRFF 1284, 1301).

1328. According to the "Brief Description of the Drawings" section of the '898 specification, "Figures 8a and 8b show the connection and timing between bus clocks and devices on the bus." (CX1451 at 12). Figure 8a (CX1451 at 145) depicts the U-shaped clock organization described in the specification at pages 46-48. (CX1451 at 47-49, 145; Jacob, Tr. 5485).

Rambus's Response to Finding No. 1328:

The proposed finding is misleading to the extent that it implies that the inventions described in the '898 application are limited to a particular clocking scheme disclosed therein. (*See* RRFF 1284, 1301).

1329. In Figure 8a (CX1451 at 145), the clock (labeled CLK) sends a clock signal, clock 1, along a wire. Each chip in the system connects to the wire and receives an "early bus clock signal." At the end of the system, the clock wire turns, are returns to the clock. On the return, the wire transmits the clock 2 signal to each chip, which receives a "late clock signal. (CX1451 at 47-48; Jacob, Tr. 5485-86).

Rambus's Response to Finding No. 1329:

The proposed finding is inaccurate and misleading. The block numbered 50 and labeled CLK in Figure 8a is described in the specification as a "bus clock generator" and was described by Professor Jacob as a "clock chip" and therefore referring to it as a "clock" is inaccurate and misleading. Furthermore the language of the proposed finding "At the end of the system, the clock wire turns, are returns to the clock" is nonsensical. In any case, the proposed finding is also misleading to the extent that it implies that the inventions described in the '898 application are limited to a particular clocking scheme disclosed therein. (*See* RRFF 1284, 1301).

1330. In the clocking system described in the '898 specification, each DRAM has circuitry that synthesizes an internal, midpoint clock signal from the early clock and the late clock signals. (CX1451 at 48-49; Jacob, Tr. 5467-69; see DX0096). Figure 13 of the '898 specification is a timing diagram showing the early clock, late clock and internal clock signal that represents the time average, or midpoint, between the early and late clock. The internal midpoint clock is not in synch with either of the external clocks (early and late clock). (CX1451 at 149; Jacob, Tr. 5491; Fliesler, Tr. 8922).

Rambus's Response to Finding No. 1330:

The proposed finding is misleading and not supported by the cited evidence. While it is true that the '898 specification describes a clocking system in some detail that is used with

particular embodiments of the inventions described therein, the proposed finding is misleading to the extent that it characterizes the '898 specification as being restricted to and only describing a single clocking system. (*See* RRFF 1284, 1301). Furthermore, there is no support in the cited evidence for the proposition that "The internal midpoint clock is not in synch with either of the external clocks (early and late clock)."

1331. In the clocking scheme described in the '898 specification, a DRAM latches data in sync with the internal, time average, midpoint, clock and not any external clock. (CX1451 at 149; Jacob, Tr. 5492).

Rambus's Response to Finding No. 1331:

The proposed finding is vague and misleading. While it is true that the '898 specification describes a clocking system in some detail that is used with particular embodiments of the inventions described therein, the proposed finding is misleading to the extent that it characterizes the '898 specification as being restricted to and only describing a single clocking system. (*See* RRFF 1284, 1301). The reference to an "internal, time average, midpoint, clock" is vague, misleading, and not supported by the evidence cited.

1332. A JEDEC-compliant DDR SDRAM does not generate an internal, time average, midpoint clock from external clock signals. (Jacob, Tr. 5492-93).

Rambus's Response to Finding No. 1332:

The proposed finding is vague and unclear in its reference to an "internal, time average, midpoint clock." Moreover, the proposed finding is not supported by the cited evidence in which Professor Jacob testifies only about what a DDR SDRAM does, not what it does not do. In fact, DDR SDRAMs use a so-called "differential clock" consisting of two external clock signals, CK and CK\, which are generally complements of one another (i.e., when CK is high,

CK\ is low, and vice versa). (JX0057 at 5, 15). Events are timed using the crossing points of the two signals, which occur at roughly the average of the high and low levels of each. (*Id.*).

1333. A JEDEC-compliant DDR SDRAM latches (inputs) data in sync with an external clock, DQS. (Jacob, Tr. 5493; JX0057 at 32). A JEDEC-compliant DDR SDRAM outputs data in sync with the external clock signals, CLK and CLK bar. (Jacob, Tr. 5557-60; 5493, JX0057 at 32).

Rambus's Response to Finding No. 1333:

The proposed finding is inaccurate and misleading. While it is true that JEDEC-compliant DDR SDRAMs latch input data in response to the DQS strobe signal, the DQS strobe signal is not a clock signal. ((Macri, Tr. 4634).

1334. The clocking scheme described in the '898 application differs from the clocking scheme used in the JEDEC DDR SDRAM standard because the application's clocking scheme uses one wire to transmit two clock signals (the early and late signals) whereas the standard uses two wires (clock and clock bar) to transmit one, differential clock signal. (Jacob, Tr. 5492-93; JX0057 at). (A differential clock signal, consisting of the signal and its inverse, is, by definition, one clock signal. (Jacob, Tr. 5493). An engineer reading the '898 patent application during the 1990s would not have thought that Rambus could obtain patent rights over the dual-edged clocking feature as it was proposed for and used in the JEDEC DDR SDRAM standard because of the difference between the two clocking schemes. (Jacob, Tr. 5493).

Rambus's Response to Finding No. 1334:

The proposed finding is misleading and not supported by the weight of the evidence. The proposed finding is misleading to the extent it characterizes the '898 application as only disclosing one clocking scheme. Although the '898 application does contemplate that a single clock line can be used to transmit two clock signals, it describes the embodiment illustrated in Figure 8 as using two clock lines. ((CX1451 at 48 ("Referring to FIG. 8, in the preferred implementation, a bus clock generator 50 at one end of the bus propagates an early bus clock signal in one direction along the bus, for example on line 53 from left to right, to the far end of

the bus. The same clock signal then is passed through the direct connection shown to a second line 54, and returns as a late bus clock signal along the bus from the far end to the origin, propagating from right to left. A single bus clock line can be used if it is left unterminated at the far end of the bus, allowing the early bus clock signal to reflect back along the same line as a late bus clock signal.")). The proposed finding is misleading to the extent that it implies that the inventions described in the '898 application are limited to a particular clocking scheme disclosed therein. (*See* RRFF 1284, 1301). Furthermore, the evidence shows that a reasonable engineer reading the '898 application during the 1990s would have thought that Rambus could obtain patent rights over the dual edged clocking feature as used in DDR SDRAMs. (RPF 681-84).

Description of Figure 12 in the '898 Specification

1335. According to the "Brief Description of the Drawings" Section of the '898 specification, "Figure 12 is a block diagram showing how the internal device clock is generated from two bus clock signals using a set of adjustable delay lines." (CX1451 at 13). The specification describes Figure 12 (CX1451 at 148) at pages 57-58 (CX1451 at 58-59).

Rambus's Response to Finding No. 1335:

The proposed finding is misleading to the extent that it implies that the inventions described in the '898 application are limited to a particular clocking scheme disclosed therein. (*See* RRFF 1284, 1301).

1336. Figure 12 of the '898 specification depicts the circuit located on each chip in the described system generates the time averaged, midpoint internal clock signal. (CX1451 at 13). The circuit of figure 12 uses the early clock signal (56) and late clock signal (57) shown in Figure 8a as inputs and generates the mid-point clock signal (73) as its output. (CX1451 at 58-59; Jacob, Tr. 5487; Fliesler, Tr. 8926-27). The only output of the circuit in Figure 12 is the time averaged, mid-point internal clock signal (73). (Fliesler, Tr. at 8927).

Rambus's Response to Finding No. 1336:

The proposed finding is vague and unclear in referring to a "time averaged, midpoint internal clock signal." The proposed finding is also misleading to the extent that it implies that the inventions described in the '898 application are limited to a particular clocking scheme disclosed therein. (*See* RRFF 1284, 1301).

1337. Figure 12 does not show a phase lock loop (PLL). (Jacob, Tr. 5487-88). The '898 application never refers to a phase-locked loop or a PLL. (Jacob, Tr. 5489-90).

Rambus's Response to Finding No. 1337:

Rambus has no specific response.

1338. Figure 12 does not show a delay lock loop (DLL). (Jacob, Tr. 5488). A comparison of a DLL circuit and the circuit of Figure 12 indicates that they have different structures. (Jacob, Tr. 5488-89, see DX0097). The '898 application never refers to a delay-locked loop or DLL. (Jacob, Tr. 5489-90; Geilhufe, Tr. 9663).

Rambus's Response to Finding No. 1338:

The proposed finding is misleading and not supported by the weight of the evidence. Although the terms "delay locked loop" or "DLL" never appear in the '898 application, the evidence presented at the hearing shows that Figure 12 and its accompanying description disclose, and therefore "refer to" a delay locked loop. (See RPF 685-688). Moreover, the PTO has determined that Rambus's claims to memory devices with DLLs are supported by the specification of the '898 application. (*See* CCFF 1647-49).

1339. The circuit of Figure 12 performs a different function than a DLL. The circuit of Figure 12 uses two clock signals to generate a third signal that is the midpoint, time-average of the two original clock signals. A DLL delays one input signal so that it will be synchronized with a second signal. (Jacob, Tr. 5488-89).

Rambus's Response to Finding No. 1339:

The proposed finding is misleading and irrelevant. The circuit of Figure 12 includes two delay locked loops. (Horowitz, Tr. 8647-48). Hence, comparing the entire circuit of Figure 12 with a single delay locked loop circuit is not probative.

1340. An engineer reading the '898 application in the mid to late 1990s would not have thought that Rambus might obtain patent rights to on-chip DLL as it was used in the JEDEC DDR SDRAM standard due to differences between the implementation, circuit structure and function of the circuit in Figure 12 compared to a DLL circuit. (Jacob, Tr. 5490).

Rambus's Response to Finding No. 1340:

The proposed finding is incomplete, misleading and contradicted by more reliable evidence. The evidence upon which Complaint Counsel rely for the proposed finding relating to what a reasonable engineer would have understood in the mid to late 1990s is testimony from complaint counsel's technical expert Professor Jacob. Professor Jacob's testimony is unreliable in this area because he has very little experience with patents, he has never worked as an engineer in the DRAM industry, his opinions in this area are inconsistent, and, in generating his opinions in this area, he failed to consider contemporaneous evidence as to what engineers actually thought when reviewing patents or patent applications known to JEDEC members. (See RPF 707-713).

The proposed finding is also misleading to the extent that it implies that all inventions described in the '898 application are limited to the particular embodiments disclosed therein. Although the specification describes a particular embodiment of one of the many inventions as including or working with a particular bus architecture, a particular packet structure, etc., a reasonable engineer or patent attorney would not have understood that all inventions disclosed

in the '898 specification would be limited to such specific embodiments. (RPF 34-39; *see Gart v. Logitech*, 254 F.3d 1334, 1343 (Fed. Cir. 2001) ("[I]t is well established, however, that broad claims supported by the written description should not be limited in their interpretation to a preferred embodiment.")).

Documents from the early to mid-1990s produced by Mitsubishi indicate that engineers at Mitsubishi reviewed the PCT application (which included the same written description and 150 claims as the '898 application) and understood that the inventions disclosed therein could be used independently of each other and the particular bus architectures described therein. (RPF 666, 670-672, 696). Moreover, when Joel Karp, then of Samsung, reviewed Rambus's PCT application in 1991, Figure 12 "jumped out" at him as evidencing a DLL. (CX 2078, Karp Micron Depo. at 119; CX 2114, Karp FTC Depo. at 276-77). Thus, the evidence shows that an engineer reading the '898 application in the mid to late 1990s would have thought that Rambus might obtain patent rights to on-chip DLL as it was used in the JEDEC DDR SDRAM. (*See* RPF 685-688).

(2) The Claims Contained in the Publicly Available Patent Application and Patents Known to JEDEC Members.

1341. In addition to the limited language of the specification, discussed above, each of the publicly available patent application or patents known to JEDEC members during and immediately following the withdrawal of Rambus as a JEDEC member contained limitations in its respective patent claims that would not have placed a reasonable engineer on notice of claims by Rambus to JEDEC-standard technology. (CCFF 1342-57).

Rambus's Response to Finding No. 1341:

The proposed finding is misleading and not supported by the weight of the evidence. The proposed finding is misleading to the extent that it implies Rambus had claims covering

features in the JEDEC SDRAM standard "during and immediately following" its withdrawal. However, Rambus had no filed claims that would have necessarily covered JEDEC-compliant SDRAMs and DDR SDRAMs until well after it left JEDEC. (RPF 361-96; Stipulated Patent Tree (showing that applications leading to patents that Rambus has asserted against DRAM manufacturers were filed in late 1997 or later)).

To the extent that the proposed finding suggests that a reasonable engineer would not have been placed on notice that Rambus could seek claims to features that had been incorporated or were eventually incorporated into SDRAMs or DDR SDRAMs based on the patents and patent applications that were known to JEDEC members by mid-1996, the weight of the evidence does not support the proposed finding. A reasonable engineer reviewing the patents and applciations known or available to JEDEC members would have understood that Rambus would be able to get patent claims broad enough to read on features incorporated or discussed for incorporation in JEDEC DRAM standards. (*See* RRFF 1342-57).

The Rambus International Patent Application

1342. Rambus filed its International Patent Application under the Patent Cooperation Treaty (the PCT application) on April 16, 1991. (CX1454 at 1). The PCT application was published on about October 31, 1991, and contains the original text, drawings and 150 original claims of the '898 U.S. application. (CX1454; CX1451)

Rambus's Response to Finding No. 1342:

Rambus has no specific response.

1343. The '898 patent application, as first filed in the PTO, contained 150 original claims. (Nusbaum, Tr. 1515). None of the original 150 claims cover JEDEC-compliant SDRAM. (Nusbaum, Tr. 1526). None of the original 150 claims would have alerted an engineer in the 1990s that Rambus might seek to obtain patent rights over features proposed for use or used in the JEDEC SDRAM or DDR SDRAM standards. (Jacob, Tr. 5494-98).

Rambus's Response to Finding No. 1343:

The proposed finding is contradicted by more reliable evidence. Experts at Mitsubishi that studied the PCT application recognized that at least claim 103 of the original 150 claims was directed to a feature that was included in SDRAM. (RX 2213A at 25, 27 ("Modifiable Access Time Register (Similar to SDRAM latency control)."); RPF 676, 695-96). Claim 103 received an "A" grade from those studying the original claims, thus indicating that it was an important concept. (See RX 2213A at 7, RPF 677). The evidence shows that engineers would likewise have been alerted to the possibility that Rambus could seek claims covering other features of SDRAMs and DDR SDRAMs as well. (*See generally* RPF 655-706).

Professor Jacob's testimony is unreliable with respect to what patent rights a reasonable engineer in the 1990s would have understood could be claimed based on original 150 claims of the '898 application. Professor Jacob's testimony is unreliable in this area because he has very little experience with patents, he has never worked as an engineer in the DRAM industry, his opinions in this area are inconsistent, and, in generating his opinions in this area, he failed to consider contemporaneous evidence as to what engineers actually thought when reviewing patents or patent applications known to JEDEC members during and immediately after Rambus was a member of JEDEC. (See RPF 707-713).

1344. Two limitations of the '898 application, "said bus containing substantially fewer bus lines than the number of bits in a single address," and "said bus carrying device-select information without the need for separate device-select lines connected directly to individual memory devices" can be characterized as multiplexed bus limitations. (Nusbaum, Tr. 1527; Jacob, Tr. 5494-96). Of twenty independent claims in the original group of 150, only two, claims 73 and 91, lack both of these limitations. (Nusbaum, Tr. 1520).

Rambus's Response to Finding No. 1344:

The proposed finding is misleading in that it fails to mention that claims 103 and 121 do not include the "said bus carrying device-select information…" limitation. Claim 103 was recognized by Mitsubishi as being related to features included in SDRAM. (*See* RRFF 1343).

1345. A majority of the 150 original claims contain the limitation "said bus containing substantially fewer bus lines than the number of bits in a single address." (CX1451 at 64-125; Nusbaum, Tr. 1519; Jacob, Tr. 5495). A JEDEC-compliant SDRAM does not satisfy this limitation because it uses more bus lines than the number of bits in a single address. (Nusbaum, Tr. 1527-28; Jacob, Tr. 5495; see Rhoden, Tr. 401).

Rambus's Response to Finding No. 1345:

The proposed finding is misleading and incomplete. Both Mr. Rhoden and Professor Jacob based their testimony on the incorrect premise that a typical SDRAM bus contains over 100 bus lines, while Mr. Nusbaum simply relied on Mr. Rhoden. (Jacob, Tr. 5464; Rhoden, Tr. 401; Nusbaum, Tr. 1527). However, the JEDEC SDRAM standard as originally published showed no SDRAM configuration with more than 26 bus lines. (RRFF 718). Therefore, the cited testimony does not support a contention that all "SDRAM buses" would not have met the "said bus containing substantially fewer bus lines than the number of bits in a single address" limitation.

1346. A majority of the 150 original claims also contain the limitation "said bus carrying device-select information without the need for separate device-select lines connected directly to individual memory devices." (CX1451 at 64-125; Nusbaum, Tr. 1519; Jacob, Tr. 5495). A JEDEC-compliant SDRAM system does not satisfy this limitation because it includes a chip-select line that is directly connected to individual memory devices. (Nusbaum, Tr. 1528; Jacob, Tr. 5465, 5495-96).

Rambus's Response to Finding No. 1346:

The proposed finding is misleading and incomplete in failing to mention that original

claim 103, which includes a programmable access-time register and was recognized as relating to SDRAM latency by Mitsubishi experts, does not contain the limitation. (CX1451 at 104; See RPF 676-77, 695-96).

1347. Claim 73 is directed to a "loop clocking system," also called the U-shaped clocking scheme, having an "early bus clock" and a "late bus clock." (CX1451 at 089-90; Nusbaum, Tr. 1523-24; Jacob, Tr. 5497). A JEDEC-compliant SDRAM does not use the clocking scheme recited in claim 73 (Nusbaum, Tr. 1528; Jacob, Tr. 5492-93, 5497).

Rambus's Response to Finding No. 1347:

The proposed finding is misleading in that claim 73 is directed to a "bus subsystem" that includes two semiconductor devices. (CX1451 at 89-90, Nusbaum, Tr. 1523). Because the claim is not directed to an individual DRAM device, stating that "[a] JEDEC-compliant SDRAM does not use the clocking scheme recited in claim 73" is uninformative.

1348. Claim 91 requires "bus connection means" (i.e., pins) that are "positioned along a single side of the package." (CX1451 at 099; Nusbaum, Tr. 1524). The narrow bus described in the '898 specification allows for a small number of connecting pins that can be positioned along a single side of the chip's package. (Nusbaum, Tr. 1528-29). JEDEC-compliant SDRAM do not use connection means along only one side of a package. The pins are along at least two sides of chip's package. (Nusbaum, Tr. 1529; Jacob, Tr. 5497-98).

Rambus's Response to Finding No. 1348:

Rambus has no specific response, except to point out that the term "narrow bus" is vague.

1349. A reasonable patent practitioner reviewing the '898 application would not have assumed that the original 150 claims contained limitations that were unnecessary to distinguish the prior art because of the massive effort that he would have presumed to have gone into drafting the relatively large number of claims and the relatively lengthy specification. (Nusbaum, Tr. 1537-40).

Rambus's Response to Finding No. 1349:

The proposed finding is misleading and not supported by the weight of the evidence. The evidence upon which Complaint Counsel rely for its proposed finding relating to what a reasonable patent practitioner would have understood in the early 1990's is testimony from complaint counsel's patent expert Mr. Nusbaum. Mr. Nusbaum's testimony is unreliable in this area because he failed to consider contemporaneous evidence as to what people actually thought when reviewing the original 150 claims. (Nusbaum, Tr. 1641). For example, documents from the early 1990's produced by Mitsubishi indicate that engineers at Mitsubishi reviewed the 150 claims of the PCT application and understood that the inventions disclosed therein could be used independently of each other and the particular bus architectures described therein. (RPF 666, 670-672, 696). Furthermore, Mr. Nusbaum acknowledged that a reasonable practitioner would understand that the original 150 claims could be broadened. (Nusbaum, Tr. 1638-1640).

The proposed finding is also not supported by the testimony cited as Mr. Nusbaum does not describe the specification as "relatively lengthy". (Nusbaum, Tr. 1537-40).

1350. A reasonable patent practitioner would have presumed that the multiplexed bus limitations, which appear in the majority of the 150 claims, were necessary to define the invention because the first paragraph of the Summary of the Invention section of the application characterizes the two limitations as features of the "present invention." (Nusbaum, Tr.1539-40).

Rambus's Response to Finding No. 1350:

The proposed finding is incomplete, misleading, and not supported by the evidence. The proposed finding is misleading in that it implies that a single invention is disclosed in the '898 specification. It cannot be disputed that multiple inventions were disclosed in the '898 specification. (*Rambus Inc. v. Infineon Technologies AG*, 318 F.3d at 1095 ("[A] multiplexing

bus is only one of many inventions disclosed in the '898 application."); Stipulated Patent Tree, attached to Parties' First Set of Stipulations)).

The proposed finding is also misleading to the extent that it implies that all inventions described in the '898 application would be limited to a particular bus structure. Although the specification describes particular embodiments of one of the many inventions as including or working with a particular bus architecture, a reasonable engineer or patent attorney would not have understood that all inventions disclosed in the '898 specification would be limited to such a bus architecture. For example, the experts at Mitsubishi that reviewed the PCT application recognized that various inventions could be separated from the bus. (RPF 666, 669-671).

Furthermore, the proposed finding is incomplete in that it fails to mention the holding of the Federal Circuit that while "clear language characterizing "the present invention" may limit the ordinary meaning of claim terms, … such language must be read in context of the entire specification and the prosecution history." The Federal Circuit went on to indicate that when taken as a whole, the specification did not limit inventions involving a "bus" to a "multiplexing bus." (*Rambus Inc. v. Infineon Technologies AG*, 318 F.3d at 1094-95).

The '703 Patent

1351. Rambus patent 5,243,703 (the '703 patent) issued September 7, 1993. (CX1460 at 1). The '703 patent claims priority to the '898 application. The '703 patent issued from a divisional application of the '898 application. (CX1460 at 1).

Rambus's Response to Finding No. 1351:

Rambus has no specific response.

1352. The specification and drawings of the '703 patent are substantially the same as the specification and drawings of the '898 specification and drawings. (CX1460; CX1451; Jacob, Tr. 5500-01).

Rambus's Response to Finding No. 1352:

Rambus has no specific response.

1353. The claims of the '703 patent recite a "U-shaped clocking scheme" having an early clock and a late clock signal and generating the time average of those two clock signals. (CX1460 at 24; Jacob, Tr. at 5499-5500). The JEDEC SDRAM and DDR SDRAM standards do not use the "U-shaped clocking scheme." (Jacob, Tr. 5492-93, 5497).

Rambus's Response to Finding No. 1353:

The proposed finding is incorrect in stating that claims of the '703 patent recite a "U-shaped clocking scheme". None of the claims of the '703 patent include such language. Only claim 2 of the patent mentions a "U-shaped transmission line".

1354. The '703 patent would not have alerted an engineer during the 1990s that Rambus might seek to obtain patent rights over features contained in the JEDEC SDRAM or DDR SDRAM standards because the claims of the '703 patent recite the U-shaped clocking scheme. (Jacob, Tr. 5498-99).

Rambus's Response to Finding No. 1354:

The proposed finding of fact is incomplete and is contradicted by more reliable evidence. (*See* RRFF 1270).

1355. The '703 patent would not have alerted an engineer during the 1990s that Rambus might seek to obtain patent rights over features contained in the JEDEC SDRAM or DDR SDRAM standards because its specification and drawings, which are substantially the same as those of the '898 application, do not relate to the standard. (Jacob, Tr. 5460-5501).

Rambus's Response to Finding No. 1355:

The proposed response is misleading and contradicted by more reliable evidence. (*See* RRFF 1270).

The Patents Identified in the Rambus Withdrawal Letter

1356. At the time that Rambus withdrew from membership from JEDEC, it submitted with its withdrawal letter dated June 17, 1996, a list of issued patents. (CX0887 at 2). The list

was not a complete list of issued patents because the '327 patent was not on the list. (CX0888 at 2; Crisp, Tr. 3381, 3384; Diepenbrock, Tr. 6200).

Rambus's Response to Finding No. 1356:

The proposed finding is incomplete and misleading. (*See* RRFF 1271).

1357. None of the listed patents would have alerted an engineer in the 1990s that Rambus might be able to obtain patent rights over features incorporated in the JEDEC SDRAM or DDR SDRAM standards. (Jacob, Tr. 5502). Each patent on the list dated June 17, 1996 (CX0887 at 2) is either restricted to a narrow, packetized, multiplexed bus architecture, addresses topics outside the scope of the JEDEC 42.3 committee, or relates to only minor implementation details of material that could have been within the scope of the 42.3 committee. (Jacob, Tr. 5502).

Rambus's Response to Finding No. 1357:

The proposed finding is contradicted by more reliable evidence and misleading. (*See* RRFF 1272).

1358. Paragraphs 1358 - 1499 are unused.

VII. RamLink, Synclink and the SyncLink Consortium.

1500. In addition to the Rambus and JEDEC efforts to develop standards for next-generation DRAM technology, there were other similar efforts during the 1990's. Among these were the Ramlink, Synclink and SyncLink Consortium efforts, which did not result in commercially viable DRAM standards. (CCFF following).

Rambus's Response to Finding No. 1500:

Rambus has no specific response to this introductory finding, which cites to no evidence.

A. The IEEE RamLink and SyncLink Working Groups.

1. The IEEE Had Rules Substantially Different From Those of JEDEC.

1501. The IEEE was a professional organization that engaged in various activities, including standard-setting activities. (Tabrizi, Tr. 9116; *see also* Prince, Tr. 8972-73).

Rambus's Response to Finding No. 1501:

Two formal submissions to the FTC by the IEEE Standards Association were admitted at trial; they describe the organization in a more complete and accurate fashion than the cited testimony. (RX 668 at 2; RX 2011 at 1).

1502. Membership in the IEEE was not by company; rather, individuals belonged to IEEE in their individual capacity. (Tabrizi, Tr. 9117; *see also* RX0579 (" . . . [M]embership and participation is by the individual person, as a professional, rather than by a company with the person being merely the company's representative, as is the case for ANSI and JEDEC projects.")).

Rambus's Response to Finding No. 1502:

Rambus has no specific response.

1503. The IEEE procedures, unlike those of JEDEC, did not impose any obligation on companies with respect to patent disclosure. (Tabrizi, Tr. 9122 ("Again, the IEEE policy, since the individual participants were representing themselves, they were not representing any company, they had no obligation to, in terms of patent disclosure. It was kind of vague enough. It wasn't like JEDEC, very solid patent disclosure."); Crisp, Tr. 3283-84; CX0711 at 128, 129-30 ("The talk moved temporarily to patents, and Walther was adamant in pointing out that the bylaws permit the member companies to retain their own intellectual property."); JX0027 at 26

("Additionally, SyncLink is being sponsored by an organization with a less stringent patent policy than JEDEC. Under the bylaws of the IEEE working groups, attendees represent themselves only, not their employers. Furthermore, they are free to patent whatever they desire, and are not bound to relinquish any of their rights to their patents by presenting their ideas for standardization.")).

Rambus's Response to Finding No. 1503:

Rambus does not dispute this finding's statements regarding the IEEE. Complaint Counsel have not, however, met their burden of establishing that the EIA imposed "obligations" regarding patent disclosure, as this finding suggests. (*See* RX 669 at 3 – ½2/96 EIA letter to FTC stating that the EIA "encourage[s]" the "voluntary" disclosure of patents).

2. RamLink Was Developed By Supercomputer Scientists to Standardize a New Future Memory Bus.

1504. RamLink was a specification for a packet-based memory. (Tabrizi, Tr. 9116). RamLink was being developed by the 1596.4 working group within the IEEE. (Gustavson, Tr. 9280).

Rambus's Response to Finding No. 1504:

The phrase "packet -based memory" is ambiguous. According to a trip report regarding the February 22, 1995 Ramlink II Working Group, "[t]he Ramlink concept is to use super high speed serial link to transfer the memory (not necessary DRAM) data to processor." (RX 535 at 1).

1505. RamLink developed as an effort to standardize a new future bus. (Tabrizi, Tr. 9117 ("RamLink was a generic bus that you could connect any kind of memory to it."); Prince, 9018 (" . . . [T]he IEEE had been engaged for a considerable period of time in standardizing the scalable coherent interface as a replacement for the future bus backplane. . . . The future bus was getting old.")).

Rambus's Response to Finding No. 1505:

The evidence shows that "FutureBus" was a name for a particular "bus-related project, "

rather than a generic description of bus designs intended to be used in the future, as this finding states. (RX 465 at 4; RX 576 at 19; RX 579 at 1; RX 940 at 6).

1506. RamLink developed from work of supercomputer scientists on the so-called scalable coherent interface, an effort to develop an entire backplane, or an entire set of components for a high-speed system. (Prince, 9018-19 (" . . . [T]he IEEE had been engaged for a considerable period of time in standardizing the scalable coherent interface as a replacement for the future bus backplane. . . . [T]he people involved in the scalable coherent interface were the supercomputer scientists of the industry from IBM, Hewlett-Packard, CDC, Apple. . . . [T]hey were defining an entire backplane, an entire set of components . . .")).

Rambus's Response to Finding No. 1506:

Rambus has no specific response.

1507. RamLink consisted of a high speed bus protocol that permitted access, based on scheduling of events, to the bandwidth that already existed inside DRAMs. (JX0026 at 95 ("What is RamLink? – High performance protocol that permits access to the large bandwidth already available inside DRAM chips – The basic protocol concepts are based on the scheduling of events")).

Rambus's Response to Finding No. 1507:

Rambus has no specific response.

1508. The RamLink bus was fully multiplexed; command, address and data information were all sent on a single bus. (Tabrizi, Tr, 9119).

Rambus's Response to Finding No. 1508:

Rambus has no specific response.

1509. RamLink members sought to cooperate with Rambus in order to come up with a better standard. Wiggers, Tr. 10,596-97; CX0681 at 1 ("Wigger[s] says Ramlink wants to cooperate with us.")).

Rambus's Response to Finding No. 1509:

The cited testimony says nothing about "Ramlink members" and refers to Mr. Wiggers' views.

1510. Rambus regarded RamLink as a source of potential competition. (Farmwald, Tr. 8369; CX0681 (". . . [O]ur decision options [with respect to RamLink] are (1) Decide they are the enemy and do one or more of: (a) Kill them ourselves (b) Convince them to kill themselves (c) Convince their management to kill them . . .")).

Rambus's Response to Finding No. 1510:

Rambus has no specific response.

1511. Richard Crisp attended meetings of the IEEE P1596.4 RamLink/SyncLink working group in early to mid-1995. (Crisp, Tr. 3528; RX-0579 at 6 ("Attendees . . . Richard D. Crisp"); CX0711 at 81-82 ("As a regular attendee of the Ramlink working group you contributed to the standard and by IEEE rules you were and are a voting member of the working group.")).

Rambus's Response to Finding No. 1511:

Rambus has no specific response.

1512. IEEE was balloting the RamLink proposal for standardization as of June 1995. (Gustavson, Tr. 9282; Gustavson, Tr. 9283).

Rambus's Response to Finding No. 1512:

Rambus has no specific response.

3. The IEEE SyncLink Project Grew Out of, and Modified, the Proposed RamLink Standard.

1513. SyncLink developed as a subset of RamLink (Tabrizi, Tr. 9117 ("SyncLink was a subset of RamLink."); Gustavson, Tr. 9280 (SyncLink was "an off-shoot of Ramlink"); Gustavson, Tr. 9282 (SyncLink was "something that grew out of RamLink"); JX0026 at 98 ("– RamLink supports a rich set of transactions and features – SyncLink uses a subset of those features . . . – Uses existing DRAM technology"). Whereas Ramlink was intended to be a generic bus to which one could connect any kind of memory, SyncLink was intended to be specific to synchronous DRAMs. (Tabrizi, Tr. 9117).

Rambus's Response to Finding No. 1513:

Rambus has no specific response.

1514. The purpose of SyncLink was to create an open standard for the next generation memory system, in which everybody would be able to develop products compatible with the

standard free of blocking patents. (Tabrizi, Tr. 9117-18; *see also* JX0026 at 10 ("It was intended to be an open standard.").

Rambus's Response to Finding No. 1514:

This proposed finding is inaccurate. Although the SyncLink Consortium represented to the public that there would be "no royalties" associated with the SyncLink technology, the Consortium members had secretly agreed among themselves that the SyncLink-related patents would *only* be freely available to members of the Consortium and its corporate successors, SLDRAM Inc. and AMI2. (*See* RX 591 at 2 – 9/22/95 SyncLink minutes – patents will be "freely available to *Consortium members*" (emphasis added); RX 779 at 1 – 10/1/96 SyncLink trip report – "Patents allow *members* use. That is what the press announcement was about when it relayed 'Royalty Free'") (emphasis added).

The SyncLink Consortium members used the patents to encourage companies to join the Consortium (and its successor, AMI2) and to discourage members from resigning from the Consortium. (*See* RX 1001 at 3 – 9/18/97 SyncLink minutes – statement by Tabrizi that "IP" should "stay with the corporation, and members can use it while still members. Otherwise nothing will hold the corporation together;" RX 1100 at 2 – 2/11/98 IBM e-mail stating that Consortium membership "would guarantee our access to any 'blocking' patents. . . ;"

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}; RX 1406 at 2 – 3/16/99 AMI2 Board of Directors meeting minutes stating that "memory manufacturers will need to be full members in order to . . . retain rights to all Patent properties."

The Consortium members also agreed to limit the use of the SyncLink patents to the particular DRAM devices they favored: the SLDRAM and DDR SDRAM devices. (*See* CX 2722 at 1 - 8/7/98 Micron e-mail explaining that SyncLink-related patents can only be "used in SLDRAM or DDR SDRAM based systems. We would not want to allow a situation where an outside developer of the core could use the IP in non-SLDRAM non-DDR systems. . . .").

Your Honor may also recall that the SyncLink Consortium received a patent on the SyncLink pinout itself – *the very specification that had been standardized by JEDEC.* (RX 2086; Rhoden, Tr. 1211: "Q. Well, this patent claims the SLDRAM pinout that was standardized at JEDEC, doesn't it? A. It does."). Finally, Your Honor may recall the testimony of AMI2 Chairman and JEDEC President Desi Rhoden, who is a named inventor on the SyncLink "pinout patent," when he was asked whether the SyncLink Consortium had told the world that the SyncLink device would be "royalty-free:"

> "Q. Weren't you telling the world in 1997 there would be no royalties associated with an SLDRAM?
>
> A. That was the statement that I was making, yes.
>
> Q. And that would mean that any intellectual property held by SDRAM, Inc. would be free for everyone to use? Is that what you were telling the world?
>
> A. I'm not sure that no royalties necessarily means free, sir, okay?"

(Rhoden, Tr. 1214). In fact, the Consortium's corporate successor has offered to license the patents at "reasonable" royalty rates. (RX 1858 at 1).

In short, Complaint Counsel's proposed finding – that the intent was for "everyone" to

be able to develop SyncLink-related products "free of blocking patents" – is inconsistent with the evidence showing the true intentions and actions of the SyncLink Consortium and its corporate successor, AMI2.

1515. SyncLink was the subject of development within the IEEE P1596.7 working group. (RX0940 at 7, 9).

Rambus's Response to Finding No. 1515:

This statement is true only prior to the formation of the SyncLink Consortium in August 1995, at which point the development moved outside of the IEEE working group. (RX 591 at 1-2).

1516. As with RamLink, SyncLink focused on the bus and system protocol; it consisted of an entire system. (JX0026 at 96 (What is a SyncLink? – Implementation of a subset of the RamLink Protocol for high-performance memory systems . . . – Typically a SyncLink memory system consists of a Link Controller, a number of memory devices or modules called SLDRAMs, and the interconnect, all on a single board."); Tabrizi, Tr. 9118 ("JEDEC was working on the core DRAM project and the SyncLink was working on the kind of overall – the component plus the bus that link them together.")).

Rambus's Response to Finding No. 1516:

This proposed finding is too vague to permit any specific response.

1517. The SyncLink project modified the RamLink protocol. (Gustavson, Tr. 9284; *see also* RX0589 at 1 ("The main question was how much to modify the RamLink protocol to optimize for SyncLink.")). The resulting SyncLink architecture was partially multiplexed; command and address information were sent on a single bus, but data was sent on a separate bus. (Tabrizi, Tr, 9119).

Rambus's Response to Finding No. 1517:

Rambus has no specific response.

1518. The SyncLink project had just begun as of May-June 1995. (Gustavson, Tr. 9283).

Rambus's Response to Finding No. 1518:

The evidence show the SyncLink project had begun by January 1995, under the aegis of a "Ramlink II Workgroup." (RX 535 at 1-2).

1519. Richard Crisp attended meetings of the IEEE RamLink and SyncLink working groups. (Crisp, Tr. 3528; Tabrizi, Tr. 9033; RX-0579 at 6 ("Attendees . . . Richard D. Crisp"); RX-0590 at 3 ("Attendees . . . Richard D. Crisp")).

Rambus's Response to Finding No. 1519:

Mr. Crisp attended some of the IEEE meetings on these subjects. (*Id.*).

1520. Rambus regarded SyncLink as a potential threat to Rambus. Crisp, Tr. 3255 (SyncLink could potentially be a threat to Rambus); Crisp, Tr. 3528-29 (Crisp viewed SyncLink as a potential competitor to RDRAM); *see also* Farmwald, Tr. 8369-70 (RamLink or SyncLink was a marketing concern to Rambus); CX0911 ("Competitive Alternatives . . . SyncLink; is it real or is it memorex?").

Rambus's Response to Finding No. 1520:

Rambus has no specific response.

4. The IEEE RamLink/SyncLink Project Was Presented At the JEDEC JC-42.3 Committee, But Rambus Refused to Disclose Whether It Had Any Patents or Patent Applications Relating To It.

1521. In May 1995, Hyundai, Texas Instruments and Mitsubishi presented the RamLink and Synclink architectures at JEDEC. (JX0026 at 10-11, 95-113). The Mitsubishi presentation of SyncLink included a description of dual edge clocking. (JX0026 at 112 ("Strobe In Reference Clock both edge for input, positive edge for output"; *see also* timing diagram at bottom of page 112); Rhoden, Tr. 471-72; Kelley, Tr. 2574-75; Sussman, Tr. 1408-09).

Rambus's Response to Finding No. 1521:

Rambus has no specific response.

1522. Gordon Kelley asked whether any companies had patent issues regarding SyncLink. (CX0711 at 72 ("Gordon Kelley asked whether or not any companies have patent issues with the material.")). Hyundai, Texas Instruments, Mitsubishi and Hewlett Packard all stated that they did not have patents covering SyncLink, and Farhad Tabrizi stated that SyncLink was intended to be an open system. (CX0711 at 72; JX0026 at 10 ("It was stated that no known

patents exist on this proposal. It was intended to be an open standard."); Rhoden, Tr. 474). When Mr. Crisp, the Rambus JEDEC representative, did not respond to this inquiry at the May 1995 meeting, Mr. Kelley asked Mr. Crisp to go back to Rambus and then report back to the Committee whether Rambus knew of any patents, especially Rambus patents, that may read on the SyncLink technology. (CX0711 at 73; CX0794 at 4; Crisp, Tr. 3267-68).

Rambus's Response to Finding No. 1522:

As this finding demonstrates, SyncLink Consortium members represented (falsely) to JEDEC at the May 1995 meeting that they would not have patents relating to the SyncLink technology they were proposing. In contrast, Rambus deceived no one: it openly stated at the September 1995 JEDEC meeting that it would *not* comment on its "intellectual property position relative to the SyncLink proposal," it stated that its design work predated the Ramlink/SyncLink efforts, and it warned JEDEC that its presence or silence at committee meetings made no statement "regarding potential infringement of Rambus intellectual property." (JX 27 at 26).

1523. After substantial internal discussion and efforts at Rambus over several months (CCFF 1050-55), at the September 1995 meeting of the JEDEC Committee, Mr. Crisp provided a response of Rambus to the inquiry made at the May 1995 Committee meeting concerning patents on SyncLink. (Crisp, Tr. 3306-08). Mr. Crisp provided the Committee a letter from Rambus in which Rambus refused to provide any information concerning whether there were Rambus patents or patent applications that might apply to SyncLink. (CX0829; JX0027 at 26 ("Rambus elects not to make a specific comment on our intellectual property position relative to the Synclink proposal.")). The letter included other recitations, including the observation that it would be several years before there was a finalized SyncLink specification to analyze for possible infringement, and that SyncLink was being developed under the auspices of IEEE, which had "a less stringent patent policy than JEDEC." (*Id.*). (See CCFF 1062-68).

Rambus's Response to Finding No. 1523:

Rambus's September 1995 letter to JEDEC, which this finding paraphrases, also includes this statement:

> "Our presence or silence at committee meetings does not constitute an

endorsement of *any* proposal under the committee's consideration nor does it make *any* statement regarding potential infringement of Rambus intellectual property."

(JX 27 at 26) (emphasis added).

1524. Mr. Crisp reported to his Rambus colleagues that there would be no second showings of the SyncLink material at the September 1995 Committee meeting. (CX0711 at 171). Mr. Crisp reported that one of the meeting participants told Mr. Crisp that he thought the reason there would be no second showings of the SyncLink technology at JEDEC was that "we [Rambus] have cast doubt over the patent issue." (*Id.*).

Rambus's Response to Finding No. 1524:

This finding is incomplete, for the evidence shows that despite Rambus's statement, and despite the views expressed by SyncLink members at the time that "there were very likely patents violated by their proposal" (RX 615 at 1 – Motorola trip report), the SyncLink Consortium proceeded to seek and obtain JEDEC standardization of the SLDRAM pinout. (RX 1114 at 1 - 3/4/98 press release announcing JEDEC approval of the SLDRAM pinout specification).

5. Although Mr. Crisp of Rambus Inadvertently Disclosed Limited Information to the IEEE Working Group Regarding the Potential Coverage of Rambus Patents, Rambus Refused to Provide a RAND Letter and No Product Implementing the RamLink Standard Ever Came to Market.

1525. In June 1995, Reese Brown posted a copy of the ballot for the proposed IEEE RamLink standard on the JEDEC reflector. (CX0711 at 76-77 ("I am posting this notice at the request of Ken McGhee: The JEDEC Office has received a copy of a ballot of a proposed IEEE Standard . . . (RAMLINK)."; Crisp, Tr. 3280-82).

Rambus's Response to Finding No. 1525:

Rambus has no specific response.

1526. Richard Crisp took exception to the posting of RamLink information on the JEDEC reflector. (Crisp, Tr. 3282). Without planning to do so beforehand, Mr. Crisp wrote in an e-mail to Mr. Brown stating in part that the proposed IEEE standard was not real and had patent issues associated with it. (CX0711 at 79-80; Crisp, Tr. 3282-83). Mr. Brown forwarded Mr. Crisp's e-mail to Mr. Hans Wiggers. (Crisp, Tr. 3283).

Rambus's Response to Finding No. 1526:

Rambus has no specific response.

1527. Hans Wiggers was the Chairman of the RamLink working group as of mid-1995. (Gustavson, Tr. 9282).

Rambus's Response to Finding No. 1527:

Rambus has no specific response.

1528. Mr. Wiggers wrote to Mr. Crisp because, as Chairman of the RamLink working group, he took Mr. Crisp's comment about patent issues "very seriously." (CX0711 at 90-91; Wiggers, Tr. 10,595 (" . . . because I was the chair, I had to take serious any claims of patents by anybody."). Mr. Wiggers stated that he assumed Mr. Crisp had attended the IEEE working group meetings in "good faith," and if Mr. Crisp knew of any way in which the proposed RamLink standard violated patents held by Rambus or others, he though Mr. Crisp had a "moral obligation" to bring to his attention information about which patents were being violated. (CX0711 at 90-91; Crisp, Tr. 3284-86).

Rambus's Response to Finding No. 1528:

Rambus has no specific response.

1529. Mr. Crisp replied to Mr. Wiggers that his personal opinion was that the RamLink/SyncLink proposals will have a number of problems with Rambus intellectual property. He stated that he planned to make an official statement at the September 1995 JEDEC meeting, and in the meantime he had nothing else to say about Rambus's patent position. He further stated that Rambus would not make any comment with respect to pending material until it issued. (CX0711 at 103, 104-05; Crisp, Tr. 3287-89).

Rambus's Response to Finding No. 1529:

Rather than inaptly paraphrasing Mr. Crisp's e-mail, the finding should quote it:

> "Regarding patents, I have stated to several persons that my personal

> opinion is that the Ramlink/Synclink proposals will have a number of problems with Rambus intellectual property. We were the first out there with high bandwidth, low pincount, DRAMs, our founders were busily at work on their original concept before the first Ramlink meeting was held, and their work was documented, dated and filed properly with the US patent office.
>
> . . .
>
> If you want to search for issued patents held by Rambus, then you may learn something about what we clearly have covered and what we do not. But I must caution you that there is a lot of material that is currently pending and we will not make any comment at all about it until it issues."

(CX 711 at 104-05).

1530. Mr. Crisp sought to prevent Mr. Wiggers from passing this information on to others. He stated in his e-mail that he claimed and withheld all copyrights for the material in his e-mail, and asked Mr. Wiggers to respect his request not to copy and distribute his e-mail to others. (CX0711 at 103, 107; Crisp, Tr. 3289-90). Mr. Wiggers agreed. *Id.*

Rambus's Response to Finding No. 1530:

In order to comport with the evidence, the word "information" must be changed to "e-mail," and the phrase "without his permission" must be added to each sentence of this finding. (CX 711 at 107; Crisp, Tr. 3289).

1531. Mr. Wiggers wrote to Mr. Crisp again in July 1995, stating that as part of submitting the RamLink standard to the IEEE Standards Board, he had to certify that there were no patent issues outstanding. He stated that he had to report his previous communications with Mr. Crisp. (CX0711 at 130, 131; Crisp, Tr. At 3291-92). Mr. Crisp responded that he had

nothing to say to the IEEE working group regarding Rambus's patent position, and that anything he had said in private correspondence was not to be construed as an official position of the company. (CX0711 at 136-37; Crisp, Tr. 3293-94).

Rambus's Response to Finding No. 1531:

If Complaint Counsel are suggesting that Mr. Crisp was trying to hide information by asking that his remarks be attributed to himself rather than to his company, this finding is inaccurate and misleading. Mr. Crisp was not part of Rambus's management (Crisp, Tr. 3498), and as JEDEC's own documents show, engineers were not usually authorized to make representations about their companies' intellectual property. (RX 486 at 1 – 3/94 McGhee memo stating that JEDEC's "legal counsel" had said that engineers should not be asked to provide assurances about "patent rights" in part because such assurances "need to come from a VP or higher within the company – engineers can't sign such documents.").

1532. Mr. Wiggers offered to summarize in his words the earlier correspondence with Mr. Crisp. Crisp, Tr. 3294. Mr. Crisp responded, "Not acceptable!", and asserted that he had "no obligation under any agreements [he had] made with anyone to report anything to anyone relative to the Rambus intellectual property . ..." (CX0711 at 142, 145; *see also* Crisp, Tr. 3294-96). Mr. Wiggers then agreed to pass on only a short statement to the effect that Mr. Crisp expressed a personal opinion that the SyncLink proposal may infringe Rambus patents. (CX0711 at 146; *see also* Crisp, Tr. 3296-97).

Rambus's Response to Finding No. 1532:

Mr. Crisp testified that he did not have a problem with the idea of a summary, but he "wanted it to be factual rather than editorial in nature." (Crisp, Tr. 3295). He and Mr. Wiggers eventually agreed upon the summary statement that "Mr. Crisp has expressed a personal opinion that the SyncLink proposal may infringe Rambus patents." (CX 711 at 146).

Although Complaint Counsel seem to be suggesting that Mr. Crisp was trying to be evasive or misleading in making sure that his remarks were attributed to himself rather than to

his company, the contemporaneous evidence shows that both JEDEC and leading JEDEC members were well aware that engineers like Mr. Crisp were not in a position to speak on behalf of their companies about patent matters and should not be asked to do so. In March 1994, for example, JEDEC Secretary Ken McGhee sent a memorandum to JC 42 Chairman Jim Townsend. (RX 486 at 1). The memorandum reported that JEDEC's "legal counsel" had said that "he didn't think it was a good idea to require people at JEDEC standards meetings to sign a document assuring anything about their company's patent rights," in part because such an assurance "needs to come from a VP or higher within the company – engineers can't sign such documents." (*Id.*). Six years later, JEDEC Secretary McGhee made the same point in a February 11, 2000 e-mail to JC 42.4 members:

> "Disclosure of patents is a very big issue for Committee members and cannot be required of members at meetings."

(RX 1582 at 1).

IBM took the same approach in its "IBM Industry Standards Participation Guide:"

> "In general, patent considerations should not be discussed in technical committees but should be taken up only at the highest committee level in the standards organization."

(RX 653 at 121).

It is thus not at all surprising that Mr. Crisp, who was not part of Rambus management (Crisp, Tr. 3498), would take the steps necessary to ensure that his personal opinions were characterized as such. Complaint Counsel's insinuations in this regard are no substitute for evidence.

1533. At the next meeting of the IEEE working group, it was announced that Mr. Crisp informed the group that, in Rambus's opinion, both RamLink and SyncLink "may" violate Rambus patents that date back as far as 1989. (RX0590 at 2). The statement did not provide any details about Rambus's issued patents or pending patent applications, or about what aspects of the RamLink or SyncLink work might infringe Rambus patent rights. (RX0590 at 2; Crisp, Tr. 3299). The working group concluded that resolution of the issues of whether early public work might invalidate such patents or whether the patents appear to be violated was not a feasible task for the working group, so it decided to continue with the technical work at hand. (RX0590 at 2).

Rambus's Response to Finding No. 1533:

The last sentence of this proposed finding attempts to limit the import of a statement in the SyncLink minutes; the statement should be included in full. (*See* RX 590 at 2). Moreover, as Complaint Counsel concede in their proposed finding no. 1541, the Secretary of the SyncLink Consortium, Dr. Gustavson, and two other engineers *did* undertake to review the claims in Rambus's pending patent applications and *did* come to the conclusion that the SyncLink device would infringe those patents, if they issued. (Gustavson, Tr. 9286-87). The SyncLink Consortium nevertheless continued to develop the device for several more years. *See* CCFF 1566 (proposed finding by Complaint Counsel that the SLDRAM design work *alone* cost at least $2,500,000 in 1997, long after Dr. Gustavson had concluded that Rambus's patent applications covered the device).

1534. Despite Mr. Crisp's statement to the IEEE working group, Rambus declined to comment at JEDEC with respect to its intellectual property position relative to the SyncLink proposal at JEDEC. (JX0027 at 26).

Rambus's Response to Finding No. 1534:

To be complete, this finding should quote, rather than incorrectly paraphrase, the statement that Rambus made and that was attached to the September 1995 JC 42 meeting minutes:

"The first Rambus patents were filed more than five years ago, with development starting years before. We have confirmed that the first Ramlink and Synclink committee meetings and draft proposals occurred years after Rambus began development.

. . .

At this time, Rambus elects to not make a specific comment on our intellectual property position relative to the Synclink proposal. Our presence or silence at committee meetings does not constitute an endorsement of any proposal under the committee's consideration nor does it make any statement regarding potential infringement of Rambus intellectual property."

(JX 27 at 26).

1535. In December 1995, Ms. Cheryl Rowden, Administrator - Intellectual Property of the IEEE, wrote to Rambus asking Rambus to advise the IEEE whether Rambus's patent or patents applied to information contained in the IEEE P1596.4 working group's draft RamLink standard and, if so, whether Rambus would issue a letter of assurance that it would make a non-discriminatory license to its technology available under reasonable rates, terms and conditions. (CX0487).

Rambus's Response to Finding No. 1535:

Rambus has no specific response.

1536. On Rambus's behalf, Lester Vincent prepared draft responses to the IEEE indicating that Rambus had patent rights that covered the draft RamLink standard and that Rambus would not agree to be bound by the IEEE's licensing terms. Mr. Vincent prepared a draft dated January 11, 1996 stating that Rambus patent rights "do cover information found in the draft IEEE P1596.4 document." (CX0853 at 2). The draft letter further stated, however, that Rambus was under "no obligation" to any standards body "to license its intellectual property" or "to disclose its intellectual property in order to retain the right to enforce" it, that Rambus reserved the sole right to decide whether and at what rate or rates to license intellectual

property, that Rambus's intellectual property rights were "not limited by the policy of any standards body," and that Rambus "will not . . . issue the letter of assurance that you have requested regarding a non-discriminatory license." (*Id*. at 1-2). Mr. Vincent prepared a draft dated January 15, 1996 stating that Rambus wished to continue to license its technology on terms that are "consistent with Rambus's own business plan and that are not set by any standards body," and that Rambus therefore was "unable" to provide the IEEE with the letter of assurance that the IEEE sought. (CX0856 at 1). The draft letter further stated that Rambus had applied for a number of additional patents, but that those patent applications remained confidential. (*Id*. at 2).

Rambus's Response to Finding No. 1536:

This finding lacks support on the issue of who drafted the documents in question. In any event, the proposed finding is irrelevant for the reasons set out in RRFF 1533 and 1537.

1537. On January 15, 1996, Mr. Anthony Diepenbrock sent a letter to Ms. Rowden of the IEEE omitting many of the statements from Mr. Vincent's drafts. (CX0855). Mr. Diepenbrock's letter stated that Rambus "cannot comment" on the proposed RamLink standard, containing a list of issued Rambus patents, and stating that Rambus would continue to license its technology "in accordance with its existing business practices." (CX0855 at 2).

Rambus's Response to Finding No. 1537:

This proposed finding is incomplete and misleading, for it fails to mention that Rambus's letter to the IEEE refers to patent applications as well as patents: "Rambus has developed a very high bandwidth memory solution and has many issued patents and *filed patent applications* relevant to high memory bandwidth products." (CX 855 at 2) (emphasis added). In addition, the reference to "Mr. Vincent's drafts" is not supported by the evidence. Complaint Counsel chose not to ask Mr. Vincent about the documents; the evidence does not support a finding that he prepared them.

1538. On February 16, 1996, Ms. Rowden wrote to Mr. Diepenbrock stating that, from Mr. Diepenbrock's letter of January 15, 1996, it was the understanding of the IEEE that Rambus was willing to license applicants "on a nondiscriminatory basis under reasonable terms and conditions" for the purpose of implementing the IEEE RamLink standard. (CX0490).

Rambus's Response to Finding No. 1538:

This proposed finding is incomplete; Mr. Rowden's letter also stated that "[i]t is our understanding from your letter that the patents cited in your letter apply to the draft document. . . ." (CX 490 at 1).

1539. Mr. Diepenbrock disagreed with Ms. Rowden's interpretation of his January 15, 1996 letter because he found that agreeing to reasonable and non-discriminatory terms to be inconsistent with Rambus's existing business practices. (Diepenbrock, Tr. 6223-24, 6228). On February 21, 1996, he wrote a reply letter to Ms. Rowden repeating his earlier statement that Rambus would continue to license its technology "in accordance with its existing business practices." (CX0869).

Rambus's Response to Finding No. 1539:

The proposed finding takes Mr. Diepenbrock's testimony out of context and misstates it. Mr. Diepenbrock testified that he:

> "generally knew some of the terms in existing contracts and contracts that were being worked on that were similar, and without studying – there were a lot of them. Without studying them, there was no way for me to be certain that all of the terms met RAND."

(Diepenbrock, Tr. 6227).

1540. The IEEE requested that the 1596.4 working group redesign the RamLink standard so that it wouldn't violate any Rambus patent claims. (Gustavson, Tr. 9296-97).

Rambus's Response to Finding No. 1540:

Rambus has no specific response.

1541. Mr. Gustavson reviewed the claims of certain of Rambus's pending patent applications. (Gustavson, Tr. 9286). His background was that of a system architect; he was interested in the bus and the system architecture, not the DRAMs. (Gustavson, Tr. 9313-14). He concluded that there was no way to work around the claims that he saw, since they related to things that the working group had been doing for ten years or so. (Gustavson, Tr. 9287). Mr.

Gustavson thought the Rambus patent claims should not block the balloting of the proposed RamLink standard. (Gustavson, Tr. 9294).

Rambus's Response to Finding No. 1541:

This finding improperly attempts to limit the scope of Dr. Gustavson's testimony. He did not limit his description of Rambus's patent applications to "system architecture:"

"Q. And when you reviewed those Rambus patent applications with Mr. Stone and Mr. James, you concluded that Rambus's claims were so broad that you could not send signals on wires in a memory device without violating those claims, right?

A. That's the conclusion I recall reaching, yes.

. . .

Q. And at the time you also concluded that Rambus wouldn't get that very broad coverage, right?

A. I assumed that it would not."

(Gustavson, Tr. 9288).

1542. Also in February 1996, Mr. Crisp called Mr. Gustavson because he believed that Mr. Gustavson "was misinterpreting Rambus's position relative to Ramlink etc." (RX0593 at 1.) Mr. Crisp reported that Rambus was "not able to determine at this time" whether there was a conflict between the RamLink standard and Rambus's patents. (*Id*. at 1-2). Mr. Gustavson concluded, "I expect they won't try to interfere with the standardization process." (*Id*. At 2.)

Rambus's Response to Finding No. 1542:

The second sentence of this proposed finding misstates the document in question, which is an e-mail from Dr. Gustavson to JEDEC representatives Hans Wiggers and Farhad Tabrizi, among others. The e-mail stated that "Crisp explained that they did respond, but their response

was basically to the effect that they were not able to determine at this time whether there was a conflict." Complaint Counsel offered no evidence at trial to show that this contemporaneous written statement by Mr. Crisp was not truthful.

The third sentence of the finding quotes only a portion of a sentence from the document, and the fragment quoted should be placed in context:

> "We discussed the situation re patents in general, and seem to be in agreement that standards ought to make no assurance to the eventual user that no patent conflicts are involved, . . . because that is impossible. Firstly, the writers may not become aware of conflicting patents until long after the standard is finished, due to the various pipeline delays and imperfect communication.
>
> As far as I could tell, Crisp and Rambus's positions were entirely reasonable in this regard, and so I expect they won't try to interfere with the standardization process (they are going to great lengths to separate themselves from it now. . . ."

(RX 593 at 2).

1543. Although the IEEE later issued the proposed RamLink standard, no product implementing the RamLink standard ever came to market. (Prince, Tr. 9012).

Rambus's Response to Finding No. 1543:

Rambus has no specific response.

6. In Response to the Possibility That Rambus Patents Might Cover SyncLink, Hyundai Negotiated an "Other DRAM" Provision As Part of Its RDRAM License To Provide Rights To Use Rambus Technology In Non-Rambus DRAMs.

1544. After Hyundai became aware that Rambus might have patents covering aspects of SyncLink, it negotiated an "Other DRAM" provision in its license agreement with Rambus as a kind of "insurance program." This "Other DRAM" provision permitted Hyundai to use Rambus technology in DRAMs other than RDRAMs. (CCFF 1264-65).

Rambus's Response to Finding No. 1544:

The proposed finding is misleading because it implies that Hyundai negotiated the "Other DRAM" provision solely due to a concern that Rambus might have intellectual property covering aspects of SyncLink. In fact, Hyundai was well aware of Rambus's position that it might have intellectual property coverage with respect to SDRAMs and, later, DDR SDRAMs. For example, a draft amendment to the license agreement was sent by Rambus to Hyundai in 1998 and expressly listed SDRAM and DDR SDRAM as examples of "Other DRAM" under the agreement. (RX 2275 at 1; CX 2108, Oh Depo., at 286). The proposed finding is also misleading by stating, without more, that Hyundai was "permitted" to use Rambus technology. Instead, a condition to such ongoing use was Hyundai's compliance with its contractual obligations, including an itemization of all products subject to royalties, the marking of all such products with Rambus proprietary markings, providing royalty reports showing shipments of all such products each quarter, and ongoing payments of royalties for such products. (CX 1599 at 12-14, ¶¶ 5.3, 5.5).

1545. During the course of 1995, Hyundai was in negotiations with Rambus for a license permitting use of Rambus technology in connection with RDRAMs. (CX0783; CX0711 at 61; CX0711 at 64).

Rambus's Response to Finding No. 1545:

Rambus has no specific response.

1546. In 1995, Dr. Oh was the Senior Vice President in charge of Hyundai's Sales and Marketing Division. (CX2107 at 11 (Oh, Dep.)).

Rambus's Response to Finding No. 1546:

Rambus has no specific response.

1547. At the time that Hyundai began license negotiations with Rambus, Dr. Oh was unaware that Rambus might have patents that extended outside the scope of RDRAM. (CX2107 at 69 (Oh, Dep.)).

Rambus's Response to Finding No. 1547:

This finding misstates Dr. Oh's testimony. He did not testify, as the finding suggests, that he believed that Rambus's intellectual property rights would be limited to the RDRAM device. Instead, the best that can be said of the testimony is that it appears that he had not considered the question. (CX 2107 at 69 (Oh FTC Dep.).

It is, in any event, undisputed that others at Hyundai were aware that Rambus might have intellectual property rights with respect to memory devices other than RDRAM. Mr. Crisp reported, for example, that at the September 1994 JEDEC meeting, a Hyundai engineer named Proebsting stated that Hyundai could put a PLL "on board" an SDRAM and that "he doubted any claim we may have made would be valid if challenged." (CX 711 at 37). It is obvious that Hyundai, like other JEDEC members, knew of the risk that Rambus's intellectual property rights might extend beyond the RDRAM device and chose to ignore that risk because of its views on the validity question. *See* RPF 530-559; 764-784.

1548. By the latter half of 1995, Dr. Oh and others at Hyundai were aware of the possibility that some aspect of SyncLink interface technology might be covered by Rambus

patents. (CX2290 at 13; CX2107 at 72 (Oh, Dep.)). However, Hyundai representatives did not have sufficient information to determine whether Rambus patents would cover SyncLink. (CX2107 at 72-73, 75-76 (Oh, Dep.)).

Rambus's Response to Finding No. 1548:

The proposed finding misstates the evidence it cites. The cited page of CC 2290 says nothing about patents or patent applications. Dr. Oh's testimony about what other people at Hyundai may or may not have known is purely speculative; he even starts his testimony with "I don't *think* any Hyundai people knew what that was about." Dr. Oh's "thoughts" about what others knew or didn't know are not probative on any issue.

1549. In order to protect against the possibility that Rambus might have patents relating to SyncLink, Hyundai sought to include a statement in the Hyundai-Rambus license agreement covering SyncLink. (CX2107 at 73 (Oh, Dep.)). Hyundai viewed this as "an anticipatory move" or an "insurance program" in case it turned out that Rambus had patents relating to SyncLink. (CX2290 at 4 ("This is an anticipatory move, in view of the possibility that a patent dispute could potentially arise concerning the SyncLink Consortium, which the Company is actively working on right now."); CX2107 at 75, 99 (Oh, Dep.)).

Rambus's Response to Finding No. 1549:

As stated in RRFF 1548, Hyundai was aware of the risk that Rambus's intellectual property rights might extend beyond RDRAM and beyon SyncLink. Moreover, the statement in the license agreement that the finding refers to, but it does not quote, is not limited to SyncLink. It reads:

> "'Other DRAM' means that each DRAM which incorporates part of the Rambus Interface Technology but is not Compatible with the Rambus Interface Specification."

(CX 1599 at 3).

1550. Hyundai and Rambus signed a license agreement in December 1995. Hyundai

succeeded in having included in the Hyundai-Rambus license agreement an "Other DRAM" provision that granted Hyundai the right to use Rambus technology in DRAMs other than RDRAMs, subject to payment of a 2.5% royalty. (CX1599 at 3 (Paragraph 1.5, "Other DRAM"), 12 (Paragraph 5.3(a)(ii)); *see also* CX2107 at 84-85, 91-92 (Oh, Dep.); Crisp, Tr. at 3320-22).

Rambus's Response to Finding No. 1550:

The proposed finding is inaccurate and incomplete. Hyundai's right to use Rambus technology in "Other DRAMs" was subject to a number of contractual conditions in addition to the payment of royalties. *See* RRFF 1544.

1551. Although the "Other DRAM" provision in the Hyundai-Rambus license agreement permitted Hyundai to use Rambus technology in all DRAMs other than RDRAMs, Hyundai was only thinking in terms of SyncLink at the time. (CX2107 at 94-96 (Oh, Dep.)).

Rambus's Response to Finding No. 1551:

Dr. Oh has no foundation for opining about what "Hyundai" was "thinking."

1552. Dr. Oh regarded 2.5% as a high royalty rate, but he did not think that Hyundai would actually have to pay that rate. He regarded it as an "insurance program" in case it turned out that SyncLink violated Rambus patents and Hyundai had no alternatives. (CX2107 at 99 (Oh, Dep.)).

Rambus's Response to Finding No. 1552:

This finding misstates Dr. Oh's testimony. Although Complaint Counsel *asked* if Oh thought that Hyundai would have to pay the rate, Oh did not answer the question. Dr. Oh also conceded that no one at Hyundai ever reported to him that they had actually *reviewed* Rambus's patents, nor could he recall if he had ever asked anyone to do so. (CX 2108 at 275-77 (Oh, Dep.)).

1553. Certain Rambus executives stated internally within Rambus that Hyundai would owe Rambus royalties under the Rambus Hyundai license agreement on sales of synchronous DRAMs. (CX1074 at 1.) Rambus never informed Dr. Oh that Hyundai owed Rambus royalties pursuant to this agreement for sales of synchronous DRAMs. (CX2108 at 229 (Oh, Dep.)

(Dr. Oh first learned in 2002 that Rambus was asserting that SDRAM and DDR SDRAM produced by Hyundai infringed Rambus's patents).

Rambus's Response to Finding No. 1553:

This proposed finding is misleading because it fails to mention that the Rambus e-mail it cites about Hyundai owing royalties was written in *August 1999*, at the time when Rambus's first patents covering features used in DDR SDRAMs began to issue. Even more egregious is Complaint Counsel's failure to tell the Court that Dr. Oh *retired* from Hyundai in 1999! (CX 2108 at 11-12 (Oh Dep.)). Complaint Counsel obviously would not suggest that after Rambus's patents issued in 1999, it should have searched throughout South Korea to find the retired Dr. Oh and tell him that Rambus had obtained patents.

B. The SyncLink Consortium.

1. The SyncLink Consortium Was Formed To Permit Joint Funding and Sharing of Various Development Tasks In Order to Create the Next Generation Open Standard.

1554. The SyncLink architecture was first developed within the IEEE working group as an off-shoot of RamLink. (Gustavson, Tr. 9280 (SyncLink was "an off-shoot of Ramlink"); Gustavson, Tr. 9282 (SyncLink was "something that grew out of RamLink")). The SyncLink working group modified the RamLink protocol. (Gustavson, Tr. 9284; see also RX0589 at 1 ("The main question was how much to modify the RamLink protocol to optimize for SyncLink.")). The resulting SyncLink architecture was partially multiplexed; command and address information were sent on a single bus, but data was sent on a separate bus. (Tabrizi, Tr, 9119).

Rambus's Response to Finding No. 1554:

Rambus has no specific response.

1555. In August 1995, Hyundai, Mitsubishi, Mosaid and Texas Instruments formed the SyncLink Consortium. (RX0591 at 1). Companies joining later or sending attendees included Micron, Hitachi, Samsung, Fujitsu, NEC, Hewlett-Packard, IBM, Panasonic, Molex, VIS, AMP and Vanguard International. (RX2090 at 7-8). Members included not only DRAM suppliers, but also customers and other companies. (CX2303 at 21 (identifying "users" and "others");

Tabrizi, Tr. 9177-78).

Rambus's Response to Finding No. 1555:

The SyncLink Consortium minutes suggest that Micron, Samsung and Apple were also "founding members" of the Consortium. (RX 610 at 1-2).

1556. The purpose of the SyncLink Consortium was to develop the next generation open standard, royalty-free standard that could meet customer requirements. (Tabrizi, Tr. 9121; *see also* RX0849 at 5 ("Consortium Mission Provide an Open Industry Standard Solutions That Meets Performance Requirements of Future Memory Systems"); RX0940 at 3 (same)). The SyncLink Consortium was intending to develop the next-generation main memory architecture that could be used in various applications, including personal computers, servers, workstations and various other segments of the market. (Tabrizi, Tr. 9126-27; see also RX0591 at 2 ("We all agreed that we are optimizing for PCs, the high volume market, though we want to perform well for multiple-processor systems and for graphics too.")).

Rambus's Response to Finding No. 1556:

This proposed finding is inaccurate. Although the SyncLink Consortium represented to the public that it was "developing an open, royalty-free industry standard" (RX 765 at 1), the Consortium members had secretly agreed among themselves that the SyncLink-related patents would *only* be freely available to members of the Consortium and its corporate successors, SLDRAM Inc. and AMI2. (*Compare* RX 765 at 1 (9/9/96 press release referencing a "royalty-free standard"), with RX 591 at 2 (8/22/95 SyncLink minutes stating that patents will be "freely available to *Consortium members*") (emphasis added), and RX 779 at 1 (trip report from the October 1996 Consortium meeting stating that: "Patents allow members use. That is what the press announcement was about when it relayed 'Royalty Free'")) (emphasis added).

By restricting the patents to "members' use," (*id.*), the Consortium members could and did use the patents to encourage companies to join the Consortium (and its successor, AMI2) and to discourage members from resigning from the Consortium. (*See* RX 1001 at 3 (9/18/97

SyncLink minutes with statement by Tabrizi that "IP" should "stay with the corporation, and members can use it while still members. Otherwise nothing will hold the corporation together"); RX 1100 at 2 (2/11/98 IBM e-mail stating that Consortium membership "would guarantee our access to any 'blocking' patents. . ."); {

} **(in camera)**; RX 1406 at 2 – 3/16/99 AMI2 Board of Directors meeting minutes stating that "memory manufacturers will need to be full members in order to . . . retain rights to all Patent properties."

The Consortium members also agreed to limit the use of the SyncLink patents to the particular DRAM devices they favored: the SLDRAM and DDR SDRAM devices. (*See* CX 2722 at 1 (8/7/98 Micron e-mail explaining that SyncLink-related patents can only be "used in SLDRAM or DDR SDRAM based systems. We would not want to allow a situation where an outside developer of the core could use the IP in non-SLDRAM (non-DDR systems. . . .")).

In the peculiar lexicon of AMI2 Chairman and JEDEC President Desi Rhoden, who is a named inventor on at least one of the SyncLink patents, the SyncLink Consortium had not made any misrepresentation to the public when it said that the SyncLink device would be "royalty-free:"

> "Q. Weren't you telling the world in 1997 there would be no royalties associated with an SLDRAM?
>
> A. That was the statement that I was making, yes.
>
> Q. And that would mean that any intellectual property held by SDRAM,

Inc. would be free for everyone to use? Is that what you were telling the world?

A. I'm not sure that no royalties necessarily means free, sir, okay?"

(Rhoden, Tr. 1214). In fact, the Consortium's corporate successor subsequently offered to license the patents at "reasonable" royalty rates. (RX 1858 at 1).

Complaint Counsel's proposed finding – that the Consortium's "purpose" was to develop a "royalty-free standard" – is truthful only if one disregards all of the contemporaneous documents to the contrary and accepts Mr. Rhoden's testimony that "royalty-free" means "reasonable royalties." (Rhoden, Tr. 1214).

1557. The SyncLink Consortium was formed as a consortium outside of the IEEE in part to fund development of an actual prototype test chip and to work with users to develop and test a board. (Tabrizi, Tr. 9122; *see also* RX0591 at 1 ("The Consortium intends to contract with Mosaid to provide the circuit-level feasibility analysis and design support for SyncLink development.").

Rambus's Response to Finding No. 1557:

The SyncLink Consortium was clearly formed as a means to exclude Rambus. Mr. Tabrizi conceded at trial that "[w]e created the consortium as a result of Rambus wanting to attend the [IEEE] meeting, and it was their right to attend [that] meeting. IEEE meeting was an open meeting to any individual." (Tabrizi, Tr. 9033-34).

1558. The SyncLink Consortium was formed as a consortium outside of the IEEE in part because the Consortium members did not consider the IEEE rules regarding disclosure of patents to be satisfactory. Because individual members in the IEEE represented only themselves and not any company, there was no obligation of patent disclosure. (Tabrizi, Tr. 9120, 9122).

Rambus's Response to Finding No. 1558:

As noted in Rambus's response to proposed finding no. 1557, the Consortium was

formed as a means to exclude Rambus from being present at the meetings. (Tabrizi, Tr. 9033-34).

1559. The SyncLink Consortium was formed as a consortium outside of the IEEE in part to permit cross-licensing among members with respect to any technology utilized in the standard. (Tabrizi, Tr. 9122).

Rambus's Response to Finding No. 1559:

This finding demonstrates – if there were still any doubt – that Complaint Counsel's proposed finding that the SyncLink standard was intended to be "royalty-free" (CCFF 1556) is false. There would be no need to have "cross-licensing" of intellectual property among members if the patents were free to all. This finding – and other evidence in the record – show that the standard was never intended to be "royalty-free" and that the Consortium made that misrepresentation in an effort to compete with the Rambus device. (*See* RRFF 1514 and evidence cited therein).

1560. The SyncLink Consortium was open to any company that wanted to join. (Gustavson, Tr. 9316; RX0591 at 1 ("The Consortium will be open to additional Founding Members that declare their intention to join by September 21, 1995, and complete the financial transaction by October 21, 1995. Other companies can join later, but at a price determined at that time by negotiation."); CX0488 at 4 ("The chair actively encourages all members to actively solicit memberships from any and all companies that may be interested in this work.")).

Rambus's Response to Finding No. 1560:

Rambus has no specific response.

1561. Rambus was invited to join the SyncLink Consortium, but did not. (Gustavson, Tr. 9316; *see also* CX0488 at 4 ("SyncLink secretary should write Rambus, HP, IBM, etc. to specifically invite them to join, and keep copies.")).

Rambus's Response to Finding No. 1561:

The purported letter to Rambus inviting it to join was not introduced at trial. It is likely,

given Mr. Tabrizi's testimony that the Consortium was formed to keep Rambus from attending the meetings, that the letter was never written. Dr. Gustavson's testimony to the contrary is not credible in light of Mr. Tabrizi's testimony and in light of the absence of such a letter.

1562. The SyncLink Consortium formed a corporation known as SLDRAM Inc. (Tabrizi, Tr. 9124).

Rambus's Response to Finding No. 1562:

Rambus has no specific response.

1563. The SyncLink Consortium divided the various infrastructure tasks necessary for the development of the standard among member companies. Hyundai and Mitsubishi developed an initial test chip. IBM developed a motherboard. Micron performed simulation analysis. Hewlett Packard performed an environmental analysis. IBM and Teradyne performed testing. A packaging company worked on defining the next generation package. (Tabrizi, Tr. 9127-30).

Rambus's Response to Finding No. 1563:

Rambus has no specific response.

1564. The SyncLink Consortium members shared know-how and design experience relating to the SyncLink architecture. (Tabrizi, Tr. 9128-29).

Rambus's Response to Finding No. 1564:

Rambus has no specific response.

1565. The SyncLink Consortium members shared the cost of development of the first chip and the expenses associated with other projects. SLDRAM Inc. levied special assessments of its members as needed for different projects. (Tabrizi, Tr. 9128).

Rambus's Response to Finding No. 1565:

Rambus has no specific response.

1566. SLDRAM Inc. contracted with Mosaid to develop a 64-meg prototype chip on behalf of the Consortium. (RX0785 at 1 ("MOSAID is prepared to begin development of a 64M SL-DRAM beginning as soon as we can formalize a business relationship with the SyncLink Consortium.")). The design work cost between $2 million and $3 million. (Tabrizi, Tr. 9129-30; RX0882 at 2 ("MOSAID agrees to our offered $2.5M total, if Consortium provides 4

experienced engineers for the duration, to be under direction of MOSAID project leader, and members of the core design team.")). The Mosaid contract was paid for by means of a special assessment in the amount of approximately $170,000 per member company. (Tabrizi, Tr. 9178).

Rambus's Response to Finding No. 1566:

Rambus has no specific response.

2. The SyncLink Consortium Sought To Avoid Patented Technologies, Including Technologies that Members Thought Might Be Covered By Rambus Patents.

1567. Members of the SyncLink Consortium were concerned about patents of non-members that might cover the work of SyncLink. The SyncLink Consortium applied for and held patents in its own name. (Tabrizi, 9124-25; Gustavson, Tr. 9314).

Rambus's Response to Finding No. 1567:

Rambus has no specific response.

1568. The SyncLink Consortium's purpose in applying for and holding patents was defensive, to prevent other individuals or companies from obtaining patents that would block the SyncLink work. (Tabrizi, Tr. 9125 ("Our patent policy was fully defensive. We just didn't want other people to file patents on our technology."); Gustavson, Tr. 9315-16 ("We had discovered . . . that one had to have patents so that you could be protected so that no one could block you from using your own technology, basically. And the term I heard applied to this was 'defensive patents'."); RX0849 at 6 ("The consortium have filed six patents for members protection against others."); Lee, Tr. 6848-49, 7048 (". . . [W]e were concerned that later on some company might try to assert patents on as far as our innovations, and so the only way to protect ourselves was to file patents.")).

Rambus's Response to Finding No. 1568:

The evidence shows that the SyncLink Consortium's purpose in obtaining patent rights was not merely "defensive," for the Consortium members used the patents to encourage companies to join the Consortium (and its successor, AMI2) and to discourage members from resigning from the Consortium. (*See* RX 1001 - 9/18/97 SyncLink minutes – statement by Tabrizi that "IP" should "stay with the corporation, and members can use it while still members.

Otherwise nothing will hold the corporation together;" RX 1100 at 2 – 2/11/98 IBM e-mail stating that Consortium membership "would guarantee our access to any 'blocking' patents. . . ;" {

}

The Consortium members also agreed to limit the use of the SyncLink patents to the particular DRAM devices they favored: the SLDRAM and DDR SDRAM devices. (*See* CX 2722 at 1 - 8/7/98 Micron e-mail explaining that SyncLink-related patents can only be "used in SLDRAM or DDR SDRAM based systems. We would not want to allow a situation where an outside developer of the core could use the IP in non-SLDRAM (non-DDR systems. . . ."). The Consortium's successor, AMI2, has also announced that the patents are available to be licensed on reasonable terms. (RX 1858 at 1).

None of these actions can be characterized as merely "defensive."

1569. Members of the SyncLink Consortium were particularly concerned about Rambus's patents. (CX0488 at 2 ("Micron is particularly concerned to avoid the Rambus patents, though all of us share this concern."); *see also* Gustavson, Tr. 9303-04).

Rambus's Response to Finding No. 1569:

This finding shows that the Consortium and its members were not "lulled" into believing that Rambus's patents or patent applications were limited to the RDRAM architecture or that Rambus would not assert its patents against others. They nevertheless proceeded with the development of the SyncLink device. *See* RRFF 1533.

1570. The SyncLink Consortium lacked specific information about Rambus's intellectual property rights. Mr. Crisp had informed the IEEE RamLink working group that RamLink and SyncLink "may" violate Rambus patents. (RX0590 at 2). Although Mr.

Vincent's draft letter of January 11, 1996 stated that Rambus patent rights "do cover information found in the draft IEEE P1596.4 document," (CX0853 at 2), Mr. Diepenbrock's final letter of January 15, 1996 to Ms. Rowden of the IEEE stated that Rambus "cannot comment" on the proposed RamLink standard, (CX0855 at 2), and Mr. Crisp subsequently told Mr. Gustavson that Rambus was not able to determine whether there was a conflict between the RamLink standard and Rambus's patents. (RX0593 at 1-2). Mr. Wiggers testified that he never received any clarification of Rambus's patent claims relating to RamLink. (Wiggers, Tr. 10,595-96; see also CX2107 at 76 (Oh, Dep.) ("We did not know exactly what Rambus has – had at that time. If we knew what they had, then it [the Other DRAM provision in the Hyundai-Rambus license agreement] would be more specific than this."); CX2107 at 72-73 (Oh, Dep.) ("No way – no way we can speculate [as to the possibility that Rambus's patents might cover SyncLink] because we don't know what it is.")). Neither Mr. Crisp's statement to the IEEE working group nor Mr. Diepenbrock's letters to the IEEE provided any details about Rambus's issued patents or pending patent applications, or about what aspects of the RamLink or SyncLink work might infringe Rambus patent rights. (RX0590 at 2; CX0855 at 2; Crisp, Tr. 3299).

Rambus's Response to Finding No. 1570:

Rambus has two responses. First, Rambus's statement that it "may" have intellectual property relating to the SyncLink was a "sufficient" disclosure under the patent policy, *according to the President of JEDEC*, Desi Rhoden, who testified that the SyncLink Consortium's own statement at a JEDEC meeting that it "might have IP" relating to the device was "sufficient to comply with the obligations of all [consortium] members with respect to the JEDEC patent policy." (Rhoden, Tr. 1305). Second, the SyncLink Consortium Secretary, Dr. David Gustavson, reviewed Rambus's pending European patent applications along with two other Consortium representatives and determined that the SyncLink device *would* infringe, *if* the applications ever issued as patents (Gustavson, Tr. 9286-87). Gustavson did not, however, believe that the patents would issue, (*id.*), and Hans Wiggers, the chair of the Ramlink Committee, believed that Rambus was simply trying to "torpedo" the Ramlink and SyncLink standards. (Wiggers, Tr. 10589).

In short, the SyncLink story gives Your Honor a very clear insight into what the "but-for" world would look like. If Rambus had stated at a JEDEC meeting, as Complaint Counsel suggests that it should have, that it believed that it could file applications that, if issued, might cover one or more of the four features at issue here, JEDEC members: (1) would have believed that any such applications would not issue, or if issued, would be invalid because of prior art (Gustavson, Tr. 9286-87; RX 829 at 2; RX 966 at 3; RX 880 at 25). and (2) would have dismissed Rambus's statements as an effort to "torpedo" JEDEC's standards. (Wiggers, Tr. 10589). Mr. Wiggers' testimony on the dual edge clocking feature is telling:

> "Q. If you had heard Richard Crisp say in a JEDEC meeting that he believed that Rambus had invented the use of both edges of the clock to transmit data in a memory device, what would your reaction have been?
>
> A. I would have said that that was not something that he could have patented because it was a known technology, so I could not see that as a proprietary technique."

(Wiggers, Tr. 10588).

Similarly, in April 1997, when Micron JEDEC representative and JEDEC Council member Terry Walther learned that Rambus "plans legal action to request royalties on all DDR memory efforts," he responded that he thought "that is old technology." (RX 920 at 1-2). Another Micron JEDEC representative, Terry Lee, testified that when he learned that same information in April 1997, he "didn't believe this was true," and he did nothing to follow up. (Lee, Tr. 6981).

There is also evidence that JEDEC members, especially the leadership of the 42.3

committee, held strongly felt views that the Patent Office often issued patents for "old technology," as Mr. Walther puts it, and the 42.3 committee even considered offering its services as "a source of expert opinions on memories to the patent office." (JX 32 at 2). The "reasoning was that there were a number of claims made on patents that had been prior art for some time and yet patents were still issued . . . . If JEDEC gets involved in reviewing patents then, they might wind up rejecting a large portion of the patents pursued." (*Id.*). It is thus clear that JEDEC 42.3 members were predispositioned to believe that any Rambus patents on features as on-chip PLL or dual edge clocking would be invalid because of prior art. (*See*, *e.g.*, CX 711 at 37 – statement by Hyundai engineer to Richard Crisp that Hyundai "can put [a PLL] on board" a synchronous DRAM and that "he doubted any claim we may have made would be valid if challenged.").

1571. Certain members of the SyncLink Consortium thought that the SyncLink architecture (as opposed to the RamLink architecture) avoided Rambus patents because the SyncLink architecture did not use a triply multiplexed bus structure and did not use other key features of the Rambus architecture. (Lee, Tr. 6623-24 (Rambus used a loop-back clock, whereas SyncLink used a source synchronous design with data strobes; Rambus used an open drain driver, whereas SyncLink used a push/pull driver scheme; "the SyncLink bus structure just had command/address multiplexed. Data was a separate bus."); Lee, Tr. 6610-11 ("The [Rambus] patents – at least the abstracts that I had reviewed seemed to apply kind of specifically to this bus architecture, to this RDRAM product. . . . [By 'this bus' I meant] the narrow bus with the command/address/data multiplexed with this Rambus architecture and Rambus signaling scheme."); see also Tabrizi, Tr. 9118-19 ("At IEEE RamLink, the bus was fully multiplexed. That means address, data, command all on one bus. But the SyncLink was somewhere between the two [RamLink and the JEDEC architecture]. We made the address and command on one bus and data on a separate bus.")).

Rambus's Response to Finding No. 1571:

The weight of the contemporaneous evidence shows that the SyncLink Consortium was well aware that their work could or would violate the claims in Rambus's pending patent

applications if those applications ever issued as patents, that they believed there was prior art that would prevent the issuance of, or invalidate, any such patents, and that they went forward with their development efforts anyway in an effort to thwart customer acceptance of the RDRAM device. RRFF 1533. The evidence on these issues includes the following:

- RX 615 at 1 – a September 1995 trip report by Motorola JEDEC representative Mark Farley stating that "SyncLink told Motorola confidentially that there were very likely patents violated by their proposal;"
- RX 663 at 2 – the January 1996 SyncLink Consortium meeting minutes, which state that "Rambus says their patents may cover our SyncLink approach even though our method came out of early RamLink work;"
- Dr. Gustavson's testimony that in late 1995 or early 1996, he reviewed Rambus's pending European patent applications, determined that they covered everything that the Ramlink and Synclink groups were doing, and concluded that the applications would never issue (Gustavson, Tr. 9286-87);
- RX 829 at 2 – the December 1996 e-mail by Micron DRAM Marketing Manager Jeff Mailloux to Micron CEO Steve Appleton stating that "[f]rom our research, we think many Rambus patents read on prior art or other patents;"
- RX 924 at 1 – Richard Crisp's May 1997 e-mail reporting that a VIA Technologies executive had said that "he thinks that SyncLink is going to

be stepping all over Rambus patents;"

- RX 966 at 3 – the January 1997 SyncLink Consortium meeting minutes, showing a desire to "collect information relevant to prior art and Rambus filings," because of a concern that "Rambus will sue individual companies" for patent infringement;
- RX 1001 at 5 – the September 1997 SyncLink Consortium meeting minutes, stating that it might not be such a wise move to collect information relating to Rambus patents, "because that multiplies the damages," no doubt referring to trebling of damages for willful infringement; and
- CX 1030 at 1 – statement in May 1998 by LG Semicon executive Dr. Jun to Rambus engineers that he had reviewed the "SLDRAM schematics," that "it looks very similar to Rambus," and that "SLDRAM Inc. is violating Rambus patents."

In short, Complaint Counsel's proposed finding, and its suggestion that SyncLink development went forward because the consortium members were unaware of any IP conflicts, are not consistent with the record in this case.

1572. SyncLink Consortium members nevertheless shared a concern to avoid Rambus patents in any future consortium work. (CX0488 at 2 ("Micron is particularly concerned to avoid the Rambus patents, though all of us share this concern.")).

Rambus's Response to Finding No. 1572:

The evidence shows that the Consortium members went forward with SyncLink development because they believed Rambus's patents would not issue or, if issued, would be

invalid because of prior art. *See* RRFF 1571.

3. After Intel Announced That It Would Support Exclusively RDRAM For Future PC Main Memory, The Role Of The SyncLink Consortium Changed to Supporting a Possible Future Memory Standard For Limited Applications Alongside RDRAM and DDR SDRAM.

1573. After Intel announced in late 1996 that it would support exclusively the RDRAM architecture for main memory in future personal computer architectures, the role of the SyncLink Consortium changed from developing a future generation main memory product to developing a future product for certain specific applications, particularly servers. (CCFF following).

Rambus's Response to Finding No. 1573:

The evidence shows that after Intel announced in late 1996 that it would support the RDRAM architecture in future generations of main memory scheduled to be launched in 1999, the DRAM manufacturers used the "corporate shield" of the SyncLink Consortium to facilitate and hide from public view their joint efforts to thwart or slow marketplace acceptance of the RDRAM device. (RRFF following).

1574. At the time it was formed, the SyncLink Consortium was intending to develop the next-generation main memory architecture that could be used in personal computers as well as servers, workstations and various other segments of the market. (Tabrizi, Tr. 9126-27; *see also* RX0591 at 2 ("We all agreed that we are optimizing for PCs, the high volume market, though we want to perform well for multiple-processor systems and for graphics too.")).

Rambus's Response to Finding No. 1574:

Rambus has no specific response.

1575. As of the latter half of 1996, DRAM manufacturers supported three different architectures for the next generation: Rambus's Direct RDRAM, SyncLink (or SLDRAM), and DDR SDRAM. (Tabrizi, Tr. 9131-32; Peisl, Tr. 4533; Appleton, Tr. 6341; CX0711 at 183, 184-85 (Intel "will say internally that they are pushing forward two if not three different potential technologies (R2 [Direct RDRAM], SyncLink, and 200+mhz SDRAM? [DDR SDRAM], are keeping the players 'honest' by playing one off the other . . .")). DRAM manufacturers understood that customers would decide which architecture to buy. (Tabrizi, Tr.

9133-34; Peisl, Tr. 4417 ("Q: Did you ever express any preference to customers toward either SDRAM or RDRAM? A: No. And essentially it's the customer's decision which controller is being designed into a particular motherboard and that dictates the usage of the memory."); *see also* Appleton, Tr. 6317-18 (discussing Micron's support of burst EDO, RamLink and SDRAMs in the early 1990's, "The customer is going to decide what they want to buy, and we needed to make sure that whatever became the customer's choice of product, that we were in a position to be able to supply it.")).

Rambus's Response to Finding No. 1575:

The proposition that DRAM manufacturers were passively waiting for customers to tell them "which architecture" to manufacture is contrary to the trial record. Mr. Tabrizi, for example, whose testimony this finding relies upon, admitted at trial that he had told Sang Park, then the President and Chief Operating Officer of Hyundai, that he wanted to "kill" Rambus and force RDRAM from the market. (Tabrizi, Tr. 9105-07). Tabrizi subsequently testified that he hadn't really meant "killing" when he talked to Park about "killing" Rambus; he really meant that Rambus had committed "suicide, [with] me watching on the sideline." (Tabrizi, Tr. 9109). In his June 2000 email to Mr. Park, however, Mr. Tabrizi had talked only of killing: "[i]f Intel does not invest in us, I really want to ask you to let me go back to my old mode of RDRAM killing. I think we were very close to achieving our goal until you said we are absolutely committed to this baby." (RX 1661 at 2).

Tabrizi was not alone in his efforts to "kill" RDRAM. At a January 1997 meeting of DRAM manufacturer executives, Siemens executive Dr. von Zitzewitz told his fellow executives that he was "disappointed" by statements he had heard from some of them "accepting" Intel's choice of Rambus, and he argued that Rambus's royalty rates were too high and that "Rambus is not acceptable." (CX 2250 at 2). This meeting of manufacturer executives to discuss whether to "accept" Rambus and to discuss the costs they should or should not be

paying for intellectual property is strong evidence of a "buyer's cartel." Complaint Counsel's economic expert acknowledged at trial that the DRAM industry possessed characteristics known to favor the existence of a buyer's cartel. (McAfee, Tr. 7594-95).

There is much additional evidence of cartel activity intended to block marketplace acceptance of RDRAM. The manufacturers monitored each other in 1998 and 1999 to ensure that their counterparts were not "cav[ing] in to the 'dark side'" by producing RDRAM in volume. (RX 1155 at 1) (*see also* RX 1444 at 1 – Micron e-mails complaining that Samsung was planning to produce too much RDRAM and had "broken ranks with the other suppliers" and "sold their soul to the devil;" RX 1487 at 4 - Hynix e-mails noting Samsung's plans to manufacture "significant amounts" of RDRAM and discussing the "need to work with them to limit the supply in the market. . . .").

The manufacturers did not simply talk about defeating "the devil" that was Rambus; they acted. The manufacturers met in October 1998, for example, to discuss a Micron proposal that they agree on a "common roadmap" to present to customers that would, they hoped, remove the "current uncertainty about the supply situation" among the customers by showing a joint commitment "by all or most of the DRAM companies" to support DDR or SLDRAM instead of RDRAM. (RX 2191 at 1; RX 2192 at 3). The manufacturers also formed a consortium known as "MI2" or "MI4," where they agreed: (1) to visit customers "as a group" to persuade them not to use RDRAM; and (2) to "benchmark" the "price" of DDR SDRAM. (RX 1390 at 1-2).

There is substantial additional evidence, describe in Rambus's Proposed Findings 1548-1602, to show that the DRAM manufacturers were not, as Complaint Counsel's proposed finding suggests, passively waiting for their customers to "decide which architecture" they

preferred. The evidence shows instead that they were attempting in concert to "kill" Rambus because it was "unacceptable" and would cause them "to lose control of [their] destiny." (RX 855 at 3; RX 1661 at 2).

1576. Intel played a significant role in selecting among the future architectures. Intel built both microprocessors and chipsets that connected the microprocessors to the system main memory. (Tabrizi, Tr. 9134). At that time, Intel controlled about 80% of the market for microprocessors used in personal computers. (Tabrizi, Tr. 9138-39).

Rambus's Response to Finding No. 1576:

Rambus has no specific response.

1577. In late 1996, Intel announced that its future chipsets for main system memory in personal computers would support exclusively RDRAM. (Tabrizi, Tr. 9134-35). As a result of that decision, DRAM manufacturers expected SyncLink to be relegated to non-PC applications, including servers, Apple-based computers and systems using UNIX-based processors. (Tabrizi, Tr. 9134-35, 9137).

Rambus's Response to Finding No. 1577:

The cited testimony by Mr. Tabrizi is inconsistent with the documents he prepared and sent to his fellow manufacturers at the time, such as this December 1996 e-mail:

> "As I have mentioned many times before, Intel does not make DRAMs, we do. And if all of us put our resources together, we do not have to go on this undesirable path. The path of control and domination by Intel.
>
> . . .
>
> I am asking all of you to stick together on this matter. . . ."

(RX 802 at 3). (*See also* RX 778 at 1 – 9/96 e-mail by Tabrizi urging manufacturers "to please educate others and get their agreement to say 'NO TO RAMBUS AND NO TO INTEL DOMINATION.'") (capitalization in original).

1578. Following Intel's announcement of its decision to support only RDRAMs for main memory in future PC systems, Mr. Tabrizi had to decide whether to stop the SyncLink Consortium work or to get some level of support from DRAM manufacturers to continue the SyncLink Consortium work. (Tabrizi, Tr. 9138-39; *see also* Appleton, Tr. 6382 (with respect to RX0801, his letter to Mr. Tabrizi, ". . . they wanted me to send this letter to Mr. Tabrizi because he was having difficulty even within Hyundai on maintaining support for SyncLink."); Lee, Tr. 6893-94 (". . . the triggering issue is what do we do with the consortium, do we keep going forward or not.")).

Rambus's Response to Finding No. 1578:

Rambus has no specific response.

1579. Mr. Tabrizi organized a meeting of executives representing the SyncLink Consortium members in January 1997 to determine the future of the SyncLink Consortium. (Tabrizi, Tr. 9138-39; RX0808 at 2 ("Propose executive meeting Friday Jan 10, 1997, in Tokyo . . . Goals: exchange ideas on future of SynchLink. Present SynchLink, ask execs for support.")). At the meeting, the level of support for the SyncLink Consortium varied from company to company; the participants agreed to continue at least to support the SyncLink Consortium's development work, but not to commit major resources to it. (Tabrizi, Tr. 9139-40).

Rambus's Response to Finding No. 1579:

Mr. Tabrizi did not alone organize the January 1997 executive meeting. The evidence shows that a senior Mitsubishi executive and Micron CEO Steven Appleton sent e-mails urging their fellow executives to attend. (RX 802 at 2; RX 809 at 1). The finding's further suggestion that the January 1997 meeting of executives had mixed results is inconsistent with the description of the meeting that appeared in the minutes of the very next SyncLink Consortium meeting:

> "Tokyo meeting of executives was very positive.
>
> . . .
>
> Siemens was eloquent. No future RB roadmap. Letting one company control industry is crazy. 0.1% royalty ok, 1-2% ridiculous. RB not

acceptable. . . ."

(RX 855 at 1).

1580. Following the meeting in January 1997, the SyncLink Consortium continued with its development work. By June 1997, the SyncLink Consortium had contracted with Mosaid to design a prototype chip. The SyncLink Consortium agreed to pay $2.5 million for the Mosaid work; members contributed $175,000 each. Hyundai also contributed two engineers and Siemens and Vanguard contributed one engineer each to the design effort. (Tabrizi, Tr. 9178; RX0938 at 1-2).

Rambus's Response to Finding No. 1580:

Rambus has no specific response.

1581. Throughout 1997, 1998 and into 1999, most DRAM manufacturers continued to support three future generation architectures: Direct RDRAM, SyncLink, and DDR SDRAM. (CX2294 at 5, 7, 9 (Hyundai roadmaps for SDRAM, DDR SDRAM, SLDRAM and RDRAM); CX2297 at 3, 25 (Hyundai tables showing RDRAM for PC application, DDR/SLDRAM for server application, and DDR for graphic application); Tabrizi, Tr. 9144-52; CX2718 at 26, 44, 45 (Micron roadmap and tables showing projected availability and positioning of DDR, RDRAM and SLDRAM); CX2728 at 2-3 (Micron table showing projected availability and comparison of SDRAM, DDR, RDRAM and SLDRAM); CX2735 at 24-25 (Micron roadmap for SDRAM, DDR, SLDRAM and RDRAM); Lee, Tr. 6719-29, 6740-44).

Rambus's Response to Finding No. 1581:

See RRFF 1575.

4. After Rambus Pressured Hyundai Into Withdrawing From the SyncLink Consortium, the SyncLink Consortium Was Disbanded.

1582. In late 1998, Rambus CEO Geoff Tate suggested to Hyundai executive Dr. Oh that Hyundai stop participating in the SyncLink Consortium. (CX2107 at 109-110 (Oh, Dep.) ("Rambus claimed that SyncLink is hurting them, and so suggest me to stop SyncLink, ask me to stop, suggest me."); *see also* Tabrizi, Tr. 9183 ("My executives were continuously getting complaint from both Rambus and Intel that Farhad is pushing SLDRAM and they want us to – they want Hyundai to ask Farhad to resign.")). Mr. Tate explained to Dr. Oh that, by playing an active role in the SyncLink Consortium, Hyundai hurt Rambus's business. (CX2107 at 115-16 (Oh, Dep.)).

Rambus's Response to Finding No. 1582:

This proposed finding takes Dr. Oh's testimony out of context. Dr. Oh recalled only that Mr. Tate had "kind of alluded" to the proposition that Hyundai should stop participating in SyncLink meetings. (CX 2107, Oh Dep. Tr., 110:13-19). He later clarified his testimony and stated that the statement by Mr. Tate that he remembers "more clearly" is a request that Mr. Tabrizi not attend a meeting between Rambus and Hyundai to discuss RDRAM development, because of a concern on Mr. Tate's part that Tabrizi might take confidential Rambus information and use it in his SyncLink development efforts. (CX 2107, Oh Dep. Tr., 115:1-9; 116:13-17; 322:7-15). In any event, it is undisputed that Mr. Tabrizi was using the SyncLink Consortium (by then incorporated as SLDRAM, Inc.) as a tool in his efforts to "kill" RDRAM and to prevent "control and domination by Intel." (RX 1661 at 2; RX 802 at 3). Those efforts did, in fact, "hurt Rambus's business," as this finding suggests.

1583. Because Intel supported Rambus at that time, Dr. Oh believed he had no choice but to produce RDRAM. (CX2107 at 117 (Oh, Dep.) ("Intel supported Rambus, so at that time no choice. As a – one of the large manufacturer of DRAM, I had to produce Rambus DRAM . . .")). In order to produce RDRAMs, Dr. Oh believed that Hyundai needed to have support from Rambus. (CX2107 at 118-19 (Oh, Dep.)).

Rambus's Response to Finding No. 1583:

Rambus has no specific response.

1584. Dr. Oh believed that he would not get full support from Rambus unless Hyundai withdrew from the SyncLink Consortium. (CX2107 at 119 (Oh, Dep.)).

Rambus's Response to Finding No. 1584:

This finding is incomplete, for it omits Dr. Oh's testimony that his belief was based only on the fact that Mr. Tate had "kind of alluded" to the proposition that Hyundai stop participating

in SyncLink meetings. (CX 2107, Oh Dep. Tr. 110:13-19).

1585. In order to satisfy Rambus, Dr. Oh instructed Mr. Tabrizi to resign from the SyncLink Consortium. (CX2107 at 117 (Oh, Dep.) (". . . in order to satisfy Mr. Tate and satisfy rambus request, I asked Mr. Tabrizi to resign."); Tabrizi, Tr. 9183-84 ("Q: And did Dr. Oh instruct you to resign from SyncLink? A: Yes, he did.")).

Rambus's Response to Finding No. 1585:

The full testimony by Dr. Oh gives a more complete picture of his reasoning:

> "Q. Why did Hyundai stop participating in the SyncLink Consortium?
>
> A. There were two reasons. The first one was, at least to me as a person who is in charge of total Hyundai memory operation, Rambus now becoming real, real product, and going to market, and, second, Rambus claimed that SyncLink is hurting them, and so suggest we to stop [participating in] SyncLink. . . ."

(CX 2107, Oh Dep. Tr., 109-110).

1586. In 1999, after Mr. Tabrizi resigned, the SyncLink Consortium was disbanded. (Tabrizi, Tr. 9183).

Rambus's Response to Finding No. 1586:

This proposed finding is false. In the fall of 1998, Intel informed Mr. Tabrizi that "they would like to start working on Intel next generation memory solution beyond RDRAM as soon as possible," and that they wanted to develop that post-Rambus device *with the DRAM manufacturers*, instead of continuing to develop further generations of Rambus memory. (RX 1361 at 1). In the same December 1998 e-mail in which he informed Dr. Oh of this news, Mr. Tabrizi said:

> "I am no longer head of SLDRAM Inc. as of 12/17/98, and I believe the

organization will die slowly from here on. Job accomplished."

(RX 1361 at 1).

What did Mr. Tabrizi mean by "job accomplished?" (*Id.*). Since it is undisputed that the SyncLink architecture was "not accepted within the industry and never went into volume production," *see* CCFF 1587, he cannot have meant that the Consortium was successful in a technical or commercial sense. Instead, Tabrizi's "job" had been to work with the other DRAM manufacturers to try to avoid the "undesirable path" of "control and domination by Intel." (RX 802 at 3). Intel's decision to work with the DRAM manufacturers, rather than Rambus, to design the post-RDRAM memory device meant that the manufacturers would not "loose control of [the] specification" and become "foundries" for Intel, as Mr. Tabrizi had feared. (RX 849 at 44). *That* is why Mr. Tabrizi thought his "job" was "accomplished" as of December 1998, and why he believed that SLDRAM Inc. would "die slowly from here on." (RX 1361 at 1).

But SLDRAM Inc. did not die, as Mr. Tabrizi had predicted, nor did it "disband," as Complaint Counsel's proposed finding states. Instead, the manufacturers saw the "corporate shield" offered by SLDRAM Inc. as a facilitating device that would allow them to "co-ordinate" their efforts to block RDRAM's marketplace acceptance in favor of the newly standardized DDR SDRAM device. (RX 1373 at 1; RX 1406 at 3). As Desi Rhoden put it, "[i]n the DRAM industry, we are clearly stronger together than we are individually." (RX 1373 at 1).

As set out in RPF 1585-1602, SLDRAM Inc. quickly became AMI2, and its new head was JEDEC Chairman Desi Rhoden. Mr. Rhoden was obviously aware of the antitrust problems that arise when competitors "co-ordinate" their activities in an effort to be "stronger" market participants. (RX 1373 at 1). In Mr. Rhoden's view, however, the corporate form for

the new organization would "indemnify member companies from anti-trust while still providing a close working environment for all." (*Id.* at 3.). He also suggested that an existing consortium of DRAM manufacturers called "M12" should "be folded under the corporation for anti-trust protection." (RX 1373 at 8).

Secure in the (false) belief that they were protected from antitrust scrutiny by their "corporate shield" (RX 1406 at 3), the manufacturers who controlled AMI2: (1) agreed to, and did, visit customers "as a group to persuade them to utilize DDR instead of RDRAM (RX 1390 at 2-3; (2) agreed to provide production "volume projections" of memory devices to Mr. Rhoden to allow him to produce a joint production forecast; and (3) agreed that "benchmarking" be "done for DDR SDRAM" on the issues of "Price-Cost Availability." (RX 1390 at 2).

1587. The SyncLink architecture was not accepted within the industry and never went into volume production. (Appleton, Tr. 6319; Tabrizi, Tr. 9184 ("Q: Now, did Hyundai ever produce SyncLink in commercial quantities? A: Never."); Peisl, Tr. 4492 ("Q: Did SyncLink ever result in the production of a product? A: Not to my knowledge.")).

Rambus's Response to Finding No. 1587:

As this finding suggests, and as an IBM engineer had pointed out as early as 1996, the SyncLink device was "vaporware compared to Rambus." (RX 839 at 1). ("Vaporware" is a term used to describe promised products that are intended to thwart customer acceptance of competitive products, in this case RDRAM. *See Caldera, Inc. v. Microsoft Corp.*, 72 F.Supp.2d 1295, 1299 (D. Utah 1999)).

1588. Paragraphs 1588 - 1599 are unused.

VIII. After Rambus Withdrew from JEDEC, It Continued to Promote Its Proprietary Technology, While Secretly Preparing to Assert Patent Claims Against JEDEC Standard Technology.

A. Intel's Endorsement of RDRAM in Late 1996 Placed DRAM Manufacturers Under Economic Pressure to Sign Licenses with Rambus and Support RDRAM Technology.

1600. In late 1995, Intel decided it would support the proprietary Rambus RDRAM technology with the next generation of Intel microprocessors. (RX1532 at 1 (Intel timeline: "December '95: chose RDRAM as the direction we would pursue")).

Rambus's Response to Finding No. 1600:

According to the Intel e-mail cited in support of this finding, the December 1995 date was an internal decision about which direction to go, which was followed by a lengthy period of meetings and negotiations with Rambus and with DRAM manufacturers. (RX 1532 at 1-2). The e-mail states that Intel and Rambus signed a contract in November 1996 and that Intel announced "that we had chosen RDRAM" in December 1996. (*Id.*) (*See also* RX 802 at 3-5 (12/17/96 news article describing Intel announcement).

1601. In order to pacify companies that were unhappy with Rambus's exclusive control over the RDRAM architecture, Rambus considered forming a Rambus "standards committee" called REDEC. (Crisp, Tr. 2939-2940; CX0902 at 1 (Garrett August 1996 email: "I have put a strawman proposal in you mailboxes, "High Performance Memory Open Standards Committee"); CX0903 at 1 (Crisp August 1996 email: "This is about pacification of our partners, pure and simple . . . there is a lot of resentment within our DRAM partners")).

Rambus's Response to Finding No. 1601:

This proposed finding is misleading because it relies upon some of Mr. Crisp's reactions to the "REDEC" proposal as if those reactions described the motivation behind the original proposal, which Mr. Crisp did not prepare. The original proposal, prepared not by Mr. Crisp but by Jeff Mitchell, is not in evidence, but we do know from Mitchell's 8/23/96 e-mail that his

proposal was "an attempt to address the concerns our customers and partners have about the proprietary nature of Rambus technology." (CX 902 at 1). It is also important to note that this "strawman" proposal was floated at a time *before* Intel entered into its agreement with Rambus jointly to develop the next-generation memory architecture, (RX 802 at 3-5), an agreement that would have made any such proposal unnecessary.

This proposed finding is also misleading because it quotes only a portion of a sentence from Mr. Crisp's 8/26/96 e-mail and does so *without* indicating that the sentence is really just a fragment. The full sentence, which explains why, in Mr. Crisp's view, the DRAM manufacturers resented Rambus, is as follows:

> "As I have recently stated, my feeling is that there is a lot of resentment within our DRAM partners that they have been caught napping on the job of product definition and that they now need to be wedded permanently to Rambus, being forced into it by the universal bad guys of the semiconductor business: Intel."

(CX 903 at 1).

1602. Richard Crisp, Rambus's primary JEDEC representative, argued against REDEC because if "REDEC was modeled at all like JEDEC, then there would be an expectation" that the organization was developing "standards which steer clear of patents." (CX0903 at 2; Crisp, Tr. 2942). Crisp believed REDEC would be in direct conflict with Rambus's goal of collecting licensing fees and royalties on its intellectual property. (CX0903 at 2-3 (Crisp August 1996 email: REDEC "sounds pretty good on the surface but I see several problems: 1) Open standards seem at odds with our business model . . . I just cannot visualize how it could be turned into anything resembling JEDEC, do meaningful work, and not be in direct conflict with our business model.")). Mr. Crisp acknowledged that "[t]he most valuable patents are ones that must be used in order to be in compliance with a standard." (*Id.* at 2; Crisp, Tr. 2939).

Rambus's Response to Finding No. 1602:

This proposed finding is misleading and incomplete because Complaint Counsel ignore the fundamental difference between the "strawman" proposal about "REDEC" and Rambus's experience at JEDEC. Rambus had never presented its technology for standardization at JEDEC, and as a result, there was no expectation that Rambus would be disclosing, or giving up rights to, its intellectual property. (McGrath, Tr. 9273-74). "REDEC," in contrast, would be entirely centered on the design and implementation of the next generation *Rambus* technology. (CX 902 at 1-2). In that scenario, as Mr. Crisp pointed out, the conflict would be how Rambus would allow the other participants "control" over the design process and yet still retain all patent rights to the developing design. (CX 903 at 2). This is why, for example, Mr. Crisp explained that "we could ask each [participant] to sign over rights etc. to us, but the odds of that happening are dreadfully small. . . ." (*Id.*). In short, the REDEC "strawman" proposal is not relevant here.

1603. In late 1996, Intel announced that its future desktop PC chipsets would only work with RDRAM. (RX1532 at 2 (Intel timeline: "December '96: Communicated that we had chosen RDRAM and signed a license with RamBus to memory vendors"); Hampel, Tr. 8677-78; Tabrizi, Tr. 9135; Crisp, Tr. 3432-33; CX2634 at 1 (Microprocessor Report article from April 1997 noting "Intel's adoption of Rambus's Direct RDRAM as its next-generation main-memory technology for PC's")).

Rambus's Response to Finding No. 1603:

The Microprocessor Report article that this finding cites provides some useful context for this finding, including an explanation for *why* Intel made the choice referenced in the finding. According to the article:

> "Intel's move was motivated by the incessant need to provide more system-level performance.

. . .

> The existing mainstream DRAM architectures cannot deliver the required bandwidth while simultaneously respecting the memory-size and bus-width constraints inherent in the PC platform. Some new high-bandwidth commodity DRAM is needed by 1999 for Intel to reach its larger goal.
>
> . . .
>
> Rambus had a proven track record of delivering cheap, high-bandwidth systems. . . . Rambus's technology also has headroom."

(CX 2634 at 1).

1604. During the beginning of the Rambus-Intel partnership, Intel hoped that Rambus would have a good relationship with the DRAM industry. (MacWilliams, Tr. 4871 ("what we had hoped for and what we had worked for actually in the first few years of this deal was to try and make Rambus a value-added part of this whole industry infrastructure")). Intel envisioned an industry infrastructure where DRAM vendors built DRAMs, Intel built chipsets, and "Rambus provide[d] all of the glue to make the enabling pieces work and therefore [] would be perceived as valuable." (MacWilliams, Tr. 4871).

Rambus's Response to Finding No. 1604:

The proposed finding is vague and not supported by the evidence. The MacWilliams testimony cited by Complaint Counsel does not state that Intel hoped Rambus would have a "good relationship" with the DRAM industry, but states that Rambus would be a "value-added part of this whole industry infrastructure." Nor does the MacWilliams testimony suggest – as Complaint Counsel seems to imply – that Intel envisioned some fundamental change to the industry infrastructure. Together with the preceding portion of Mr. MacWilliams' answer (MacWilliams, Tr. 4870-71), it is clear that Intel hoped that Rambus could enable the industry in the same way that Intel provided "many of the enabling capabilities . . . back in the PC100

days".

1605. Projected demand for RDRAM increased sharply after Intel announced it would produce chipsets that used RDRAM. (Hampel, Tr. 8677-78 (Rambus saw an increase in customer interest after Intel endorsed RDRAM: "There were more customers interested. We did increase kind of the workload . . . to support the effort"); CCFF 1607, 1802, 1806-08)).

Rambus's Response to Finding No. 1605:

Rambus has no specific response.

1606. Because RDRAM was expensive to produce and Rambus demanded high royalty rates, some members of the DRAM industry were surprised and concerned about Intel's decision to endorse Rambus. (Appleton, Tr. 6344 (Micron's Chairman of the Board and CEO Steven Appleton was surprised to learn that Intel had endorsed Rambus's Direct RDRAM technology because "there were better alternatives to pursue" and "it would be a relatively high cost to the DRAM industry to do it."); Tabrizi, Tr. 9044, 9135 (Hynix Vice President Farhad Tabrizi was very concerned about Intel's decision to support RDRAM because he believed in open standards and felt the industry would be stuck with a very costly device to manufacture)).

Rambus's Response to Finding No. 1606:

This proposed finding is not supported by the evidence. It is true that the DRAM manufacturers were very "concerned about Intel's decision to endorse Rambus," as this finding states, but not for the reasons suggested by the finding. The concern over Rambus's royalties that this finding mentions, for example, was not about the *rate* being charged as much as the fact that the *recipient* of the royalty was not a DRAM manufacturer. As the article from Microprocessor Report cited in CCFF 1603 makes clear, Rambus's royalties:

> "are an emotional issue for many in the DRAM industry, yet these royalty relationships are commonplace in the DRAM industry. Texas Instruments, for example, currently derives more income from its DRAM patent portfolio than Rambus can reasonably expect to generate within the next decade. The aggravating issue is not so much royalties *per se*,

but new and blatantly aboveboard royalties. Also, because Rambus is an intellectual-property company, its licensing relationships do not have the same sense of reciprocity and *quid pro quo* as do other licensing arrangements in the industry."

(CX 2634 at 3).

The other concern mentioned in Complaint Counsel's proposed finding is that the RDRAM supposedly would be "expensive to produce." The finding cites testimony by Micron CEO Steve Appleton and Hyundai Vice President Farhad Tabrizi in support of this proposition. The contemporaneous evidence shows, however, that Micron was not at all concerned about the prospect of manufacturing RDRAM, then referred to as "nDRAM." In an official "response script" prepared by Micron at the time of Intel's announcement, Micron explained that it would have little or no difficulty adapting to the new technology:

> "4. What would having to make 'nDRAM' or SyncLink mean to Micron?
>
> Keep in mind that ALL of these DRAM technologies use the same DRAM process, the same DRAM cell, and virtually the same DRAM array. . . .
>
> Switching from one product to another, while still using the same core technology, involves only changing priorities in design and product engineering and may mean some differences in our assembly and test equipment purchases. SDRAM, SLDRAM, nDRAM all use the same fab equipment and core DRAM technology. In short, while the flavors might

change, it's still a DRAM."

(RX 836 at 3).

As for the only other evidence cited by this finding, the testimony of Hyundai's Mr. Tabrizi, the contemporaneous evidence shows *no* concern on his part about RDRAM being "expensive to produce," as this finding states. Instead, Mr. Tabrizi was concerned about the manufacturers' loss of control over future memory design and development, as these contemporaneous documents written by Mr. Tabrizi make clear:

- September 1996 – ". . . the real motive of Intel is to control DRAM manufacturers. . . . We will become a foundry for all Intel activities. . . ." (RX 778 at 1);
- December 1996 – "[m]any suppliers are paranoid over the prospect of a single customer, e.g., Intel, having control of market. We can't resist such a possibility individually. We need some united strategy." (RX 808 at 2);
- December 1996 – ". . . Intel does not make DRAMs, we do. And if all of us put our resources together, we do not have to go on this undesirable path. The path of control and domination by Intel." (RX 802 at 3).

There is substantial additional evidence of the manufacturers' fears of a "loss of control" over their "destiny," which evidence is described and analyzed at RPF 1555-1572.

In short, while this finding correctly states that the DRAM manufacturers were concerned about Intel's decision to endorse Rambus, it is incorrect in identifying the purported reasons for those concerns.

1607. Despite concerns, Intel's support of RDRAM forced Micron to engage in

licensing negotiations with Rambus. (Appleton, Tr. 6345-46 ("once Intel endorsed [] RDRAM, then the probabilities of customers in the marketplace actually using it increased quite a bit, and as a result, we also then believed that some customers would use RDRAM and that we needed to then engage to negotiate for a license.")).

Rambus's Response to Finding No. 1607:

Rambus has no specific response.

1608. In February 1997, Rambus and Samsung narrowed the scope of their prior RDRAM license agreement by eliminating the "other use clause." (CX0914 at 1 (Tate December 1996 email: reporting an "agreement on a much narrow[er] deal," pursuant to which Samsung was forbidden to use Rambus IP for any "competitive DRAMs"); CX0918 at 1 (Tate February 1997 email discussing a meeting with Samsung: "we both signed the contract (finally)"); CCFF 741)).

Rambus's Response to Finding No. 1608:

The proposed finding is incomplete and misleading. The first cited exhibit CX0914 states that the "other use clause" was "a fairly fuzzy clause" and that the agreement would be "modified," not that the clause would be "eliminated."

Nor does the first exhibit state, as Complaint Counsel suggest in their parenthetical, that pursuant to the modification "Samsung was *forbidden* to use Rambus IP for any 'competitive DRAMs,'" (emphasis added), but that Samsung "cannot use our IP for competitive DRAMs which we define as pretty much any dram. *If they do use our IP for a competitive dram* we say *we'll negotiate a license agreement with them in good faith*. . . . [I]f they use our IP in a competitive dram and don't license it, we can't cancel the whole Rambus license but we can sue them (not just arbitrate)." (CX0914 (emphasis added)).

1609. One by one, DRAM manufacturers signed Direct RDRAM license agreements with Rambus. (CCFF 1611-15).

Rambus's Response to Finding No. 1609:

Rambus has no specific response.

1610. { } (CX2699 at 1, *in camera*).

Rambus's Response to Finding No. 1610:

Rambus has no specific response.

1611. In February 1997, Mitsubishi signed a license agreement with Rambus covering Direct RDRAM. (CX1609 at 1-19). The subject matter of the Mitsubishi agreement was limited to Rambus-compatible DRAMs and interfaces. (*Id.* at 1-2).

Rambus's Response to Finding No. 1611:

Rambus has no specific response, unless Complaint Counsel are suggesting that the license does not include "subject matter" broader than just patent rights for the manufacture, use and sale of DRAM. The agreement includes other subject matter such as design and development support. (CX1609).

1612. In March 1997, Hyundai amended its RDRAM license agreement with Rambus to include Direct RDRAM. (CX1612 at 1-7; CX1599 at 1-23; CX1600 at 1-22 (original RDRAM license agreement between Hyundai and Rambus dated December 1995)). Hyundai's new agreement included royalties on Direct RDRAM ranging from 1.5% to 2.0% depending on the sale date. (CX1612 at 5).

Rambus's Response to Finding No. 1612:

The proposed finding is vague and incomplete. The March 1997 agreement includes royalties ranging decreasing from 2.0% to 1.5% of net sales, depending on the sales date *and* the relative revenue for the sales (CX1612 at 5).

1613. In March 1997, Micron signed a license agreement with Rambus covering Direct RDRAM. (CX1646 at 1-20). Micron agreed to pay royalty rate up to 2% on next generation RDRAM. (CX1646 at 11).

Rambus's Response to Finding No. 1613:

The proposed finding is incomplete. Micron's agreement included a provision to buy down the royalty rate. (CX 1646 at 11).

1614. Micron was forced to sign a license agreement for Direct RDRAM under "economic pressure." (Appleton, Tr. 6346-47 ("We felt that with Intel's endorsement, that there would be a customer base that would use the product, and we needed to be in a position to make whatever product that the customer decided that they were going to use for their platforms."); Lee, Tr. 6870, 6615 (Micron was forced to sign a license agreement with Rambus in keep up with Intel's projection of using RDRAM across its product lines)).

Rambus's Response to Finding No. 1614:

This finding is misleading because of its use of quotation marks around the phrase "economic pressure." By placing those quotation marks adjacent to a citation to Mr. Appleton's trial testimony, Complaint Counsel were obviously suggesting that Mr. Appleton had used that phrase in his testimony. He did not. What he said was that he had signed a license because he thought customers would want to buy what he would be manufacturing. (Appleton, Tr. 6346-47). That statement is *no one's* definition of economic pressure.

1615. In July 1997, Siemens AG signed a license agreement with Rambus covering RDRAM. (CX1617 at 1-22; CX2088 at 62 (Tate, Infineon Trial Tr.)).

Rambus's Response to Finding No. 1615:

Rambus has no specific response.

B. Rambus Attempted to Persuade Companies to Stop Developing Alternative Technologies That Competed with RDRAM.

1616. From 1996 through 1998, Rambus attempted to get DRAM manufacturers to agree not to support alternatives to RDRAM. (CCFF 1617-18, 1620, 1623).

Rambus's Response to Finding No. 1616:

The proposed finding is incomplete and misleading. (*See* RRFF 1617-18, 1620 and

1623).

1617. Rambus considered offering Samsung warrants for 250,000 shares of Rambus stock in exchange for working exclusively on RDRAM. (CX0981 at 4 (Tate December 1997 email: "we should offer [Samsung] 250K warrants in return for their commitment NOW to drop ddr"); CX0983 at 1 (Tate December 1997 email: "we give [Samsung] warrants for 250K shares at the market price . . . as long as they have not developed or worked on any competitive memory interface technology")).

Rambus's Response to Finding No. 1617:

This proposed finding is incomplete and misleading. The cited email demonstrates that the idea of Rambus giving Samsung warrants for 250,000 Rambus shares was first proposed *by Samsung*. (CX 981 at 3 ("Finally he [CS Choi of Samsung] talked about intel's warrants of $1MU – they are 90% of MPU's; samsung is 25% of DRAMs, so we should give samsung a pro-rated amount of warrants at least, say 250K-ish").) Mr. Tate's comments reflect his reaction to Samsung's request and his attempt to respond to it.

1618. Rambus offered Micron, Samsung, and Lucky Goldstar ("LG") preferential RDRAM license terms in exchange for "dropping" development work on other DRAMs. (Appleton, Tr. 6342-43; RX0828 at 1 (December 1996 letter from Rambus to Micron: "if Micron wants to increase the commitment a step further to put 'all your wood behind one arrow' with Rambus as your sole effort for high-bandwidth DRAMs . . . then in return we can slash our fee for our license"); CX0956 at 2-3 (Tate September 1997 email: "if samsung was willing to consider dropping ddr, synclink and announcing that after sdram-100 that rambus is their only dram strategy then we could talk about . . . rewards to samsung"); CX0957 at 1-2 (Rambus proposed to Korean DRAM maker LG that if it were to "cancel ddr" and commit to fully support RDRAM, then Rambus "could consider some [RDRAM] royalty breaks for 98 in return."); CX0966 at 1 (Tate November 1997 email considering LG's request to lower RDRAM royalty rates: "tie to agreement to NOT do ddr/sldram and public announcement of this NOW")).

Rambus's Response to Finding No. 1618:

This proposed finding is incomplete and misleading. First, as is clear from the document underlying the cited Appleton testimony, RX0828, Rambus was not requesting that Micron stop

developing non-Rambus DRAM. It was an offer of several licensing options, one of which was that if Micron put all its wood behind RDRAM, then Rambus would reduce both the licensing fee and the royalty rate. (RX0828). Second, the cited Tate email regarding Samsung demonstrates that Rambus did not expect Samsung to drop DDR but wanted to encourage Samsung to promote RDRAM ahead of DDR. (CX0956 at 1 ("make rambus their #1 marketing priority > DDR"). Third, Rambus offered warrants to LG "but since LG [was] already a good partner there were no conditions for them to get the warrant deal – just to meet the milestones." (CX 957 at 1).

1619. Micron "responded negatively" to Rambus's request to stop developing non-Rambus DRAM because Micron CEO Steve Appleton did not want to limit the company to one path. (Appleton, Tr. 6343).

Rambus's Response to Finding No. 1619:

The proposed finding is misleading and irrelevant. As is clear from the document underlying the cited Appleton testimony, RX0828, Rambus was not requesting that Micron stop developing non-Rambus DRAM. It was an offer of several licensing options, one of which was that if Micron put all its wood behind RDRAM, then Rambus would reduce both the licensing fee and the royalty rate. (RX0828). Because it was based on a faulty premise, Micron's response and Mr. Appleton's testimony are irrelevant.

1620. In early 1998, Rambus CEO Geoffrey Tate met with Hyundai senior executive vice president Dr. Oh and suggested that Hyundai stop participating in the SyncLink Consortium. (CX2107 at 110-111 (Oh, Dep.)).

Rambus's Response to Finding No. 1620:

This proposed finding takes Dr. Oh's testimony out of context. Dr. Oh recalled only that Mr. Tate had "kind of alluded" to the proposition that Hyundai stop participating in SyncLink

meetings. (CX 2107, Oh Dep. Tr., 110:13-19). He later clarified his testimony and stated that the statement by Mr. Tate that he remembers "more clearly" is a request that Mr. Tabrizi not attend a meeting between Rambus and Hyundai to discuss RDRAM development, because of a concern on Mr. Tate's part that Tabrizi might take confidential Rambus information and use it in his SyncLink development efforts. (CX 2107, 2108, Oh Dep. Tr., 115:1-9; 116:13-17; 322:7-15).

1621. Dr. Oh wanted to maintain good relations with Rambus because Intel supported Rambus. (CX2107 at 117 (Oh, Dep.) ("Intel supported Rambus, so . . . [as] one of the large manufacturers of DRAM, I had to produce Rambus DRAM")). In order to produce RDRAMs, Hyundai needed support from Rambus. (CX2107 at 119 (Oh, Dep.)).

Rambus's Response to Finding No. 1621:

Rambus has no specific response.

1622. Dr. Oh feared that he would not get full technical support from Rambus unless Hyundai withdrew from the SyncLink Consortium. (CX2107 at 119 (Oh, Dep.)).

Rambus's Response to Finding No. 1622:

This proposed finding is misleading. Dr. Oh did not mention "technical support," and he did not speak of "fear." (CX 2107, Oh Dep. Tr., 119).

1623. In 1998, Hyundai stopped participating in the SyncLink Consortium. (CX2107 at 109 (Oh, Dep.)). Dr. Oh instructed Farhad Tabrizi to resign from SyncLink "in order to satisfy Mr. Tate and satisfy Rambus['s] request." (CX2107 at 117 (Oh, Dep.); Tabrizi, Tr. 9183-84).

Rambus's Response to Finding No. 1623:

The full testimony by Dr. Oh gives a more complete picture of his reasoning:

> "Q. Why did Hyundai stop participating in the SyncLink Consortium?
>
> A. There were two reasons. The first one was, at least to me as a person who is in charge of total Hyundai memory operation, Rambus now

> becoming real, real product, and going to market, and, second, Rambus claimed that SyncLink is hurting them, and so suggest we to stop [participating in] SyncLink. . . ."

(CX 2107, Oh Dep. Tr., 109-110).

1624. Hyundai never commercially produced SyncLink and, after Hyundai withdrew its support, SyncLink "kind of died." (Tabrizi, Tr. 9183-84).

Rambus's Response to Finding No. 1624:

This proposed finding is false. In the fall of 1998, Intel informed Mr. Tabrizi that "they would like to start working on Intel next generation memory solution beyond RDRAM as soon as possible," and that they wanted to develop that post-Rambus device *with the DRAM manufacturers*, instead of continuing to develop further generations of Rambus memory. (RX 1361 at 1). In the same December 1998 e-mail in which he informed Dr. Oh of this news, Mr. Tabrizi said:

> "I am no longer head of SLDRAM Inc. as of 12/17/98, and I believe the organization will die slowly from here on. Job accomplished."

(RX 1361 at 1).

What did Mr. Tabrizi mean by "job accomplished?" (*Id.*). Since the SyncLink architecture was "not accepted within the industry and never went into volume production," *see* CCFF 1587, he cannot have meant that the Consortium was successful in a technical or commercial sense. Instead, Tabrizi's "job" had been to work with the other DRAM manufacturers to try to avoid the "undesirable path" of "control and domination by Intel." (RX 802 at 3). Intel's decision to work with the DRAM manufacturers, rather than Rambus, to

design the post-RDRAM memory device meant that the manufacturers would not "loose control of [the] specification" and become "foundries for Intel," as Mr. Tabrizi had feared. (RX 849 at 44). *That* is why Mr. Tabrizi thought his "job" was "accomplished" as of December 1998, and why he believed that SLDRAM Inc. would "die slowly from here on." (RX 1361 at 1).

But SLDRAM Inc. did not die, as Mr. Tabrizi had predicted, nor did it "disband," as Complaint Counsel's proposed finding states. Instead, the manufacturers saw the "corporate shield" offered by SLDRAM Inc. as a facilitating device that would allow them to "co-ordinate" their efforts to block RDRAM's marketplace acceptance in favor of the newly standardized DDR SDRAM device. (RX 1373 at 1; RX 1406 at 3). As Desi Rhoden put it, "[i]n the DRAM industry, we are clearly stronger together than we are individually." (RX 1373 at 1).

As set out in RPF 1585-1602, SLDRAM Inc. quickly became AMI2, and its new head was JEDEC Chairman Desi Rhoden. Mr. Rhoden was obviously aware of the antitrust problems that arise when competitors "co-ordinate" their activities in an effort to be "stronger" market participants. (RX 1373 at 1). In Mr. Rhoden's view, however, the corporate form for the new organization would "indemnify member companies from anti-trust while still providing a close working environment for all." (RX 1373 at 3). He also suggested that an existing consortium of DRAM manufacturers called "M12" should "be folded under the corporation for anti-trust protection." (RX 1373 at 8).

Secure in the (false) belief that they were protected from antitrust scrutiny by their "corporate shield" (RX 1406 at 3), the manufacturers who controlled AMI2: (1) agreed to, and did, visit customers "as a group" to persuade them to utilize DDR instead of RDRAM (RX 1390 at 2-3; (2) agreed to provide production "volume projections" of memory devices to Mr. Rhoden

to allow him to produce a joint production forecast; and (3) agreed that "benchmarking" be "done for DDR SDRAM" on the issues of "Price," "Cost" and "Availability." (RX 1390 at 2).

C. After its Withdrawal from JEDEC, Rambus Secretly Monitored the Activities at JEDEC and Synclink Even As It Continued To Amend and Prosecute its Patent Applications.

1625. Rambus continued to follow JEDEC's activities after it submitted its withdrawal letter in June 1996. (Crisp, Tr. 3388; CX0888 at 1).

Rambus's Response to Finding No. 1625:

This proposed finding is vague, ambiguous and not supported by the evidence. In the cited testimony Mr. Crisp simply explained that he continued to be "curious" about JEDEC. (Crisp, Tr. 3388). The only other evidence cited to support this proposed finding, Rambus's letter confirming its withdrawal, certainly does not demonstrate that Rambus continued to follow JEDEC's activities after it sent the letter. (CX0888 at 1).

1626. Several sources leaked information to Rambus about JEDEC meetings after Rambus withdrew from JEDEC. (Crisp, Tr. 3413). In 1997 Richard Crisp, Rambus's principal JEDEC representative, received information about JEDEC's activities from a source called "deep throat." (Crisp, Tr. 3414; CX0929 at 1; CX0932 at 1 (Crisp June 1997 email: "My 'deep throat' (DT) source told me that the DDR bandwagon is moving fast within JEDEC with all companies participating.")). Crisp also received information relating to proceedings at JEDEC from an anonymous source called "Mixmaster," a reporter Crisp called the "Carroll contact," and a source known as "Secret Squirrel." (Crisp, Tr. 3414-3417; CX0953 at 1; CX0935 at 1 ("More stuff from the Carroll contact")).

Rambus's Response to Finding No. 1626:

The proposed finding is misleading and is not supported by the evidence. First, there is no evidence that the information referenced in the cited e-mails was confidential, such that its disclosure would constitute a "leak." JC 42.3B chair Gordon Kelley has acknowledged that the minutes of JC 42.3 meetings are publicly available. (Kelley, Tr. 2623). Second, Mr. Crisp

explained that the "Carroll contact" was a reporter, not a JEDEC person. (Crisp, Tr. 3414-3417). Finally, the e-mails Mr. Crisp received from anonymous individuals called "Mixmaster" and "Secret Squirrel" were unsolicited and were sent through an e-mail "anonymizer" by persons unknown to him. (*Id.*).

1627. Mr. Crisp shared JEDEC-related information he received from Deep Throat, the Carroll Contact, Mixmaster, and other sources with Rambus executives and engineers. (Crisp, Tr. 3413-3417; CX0935 at 1 (Crisp email regarding "more stuff on taipei jedec meeting"); CX0929 at 001; CX0932 at 1 (June 1997 email from Crisp to Rambus's entire executive group and others within Rambus entitled "JEDEC G2," referring to a type of intelligence); CX0973 at 1 ("some JEDEC G2"); CX0979 at 1 ("jedec G2 . . . no discussion of any Rambus patents that my source heard either officially or unofficially"); CX1014 at 1 ("other G2 regarding JEDEC . . . I had lunch with a JEDEC guy (frequent source of information)")).

Rambus's Response to Finding No. 1627:

Rambus has no specific response.

1628. After its withdrawal from JEDEC, Rambus used the information that Mr. Crisp gathered in the process of amending the scope of its patent claims. (Crisp, Tr. 3417-18).

Rambus's Response to Finding No. 1628:

This proposed finding is contradicted by the only evidence that it cites. Mr. Crisp testified that it was "not clear" whether information he received after Rambus left JEDEC permitted Rambus to continue the process of amending its patent claims. (Crisp, Tr. 3417-18). Mr. Crisp's testimony does not establish that information he received after Rambus left JEDEC was actually used in Rambus's process of amending its patent claims. In any event, the activity described is lawful under *Kingsdown Medical Consultants, Ltd. v. Hollister, Inc.* , 863 F.2d 867 (Fed. Cir. 1988), as Complaint Counsel have conceded.

1629. After June 1996, Rambus continued to follow SyncLink's activities. (Crisp, Tr. 3388-89; Crisp, Tr. 3395-3396; CX0711 at 183).

Rambus's Response to Finding No. 1629:

The evidence shows that the SyncLink Consortium followed Rambus a lot more closely than Rambus followed SyncLink's activities. *See* RPF 557-59; 589-90; 1555-62; 1570-73.

1630. After June 1996, Rambus continued its efforts to secure patent rights over SyncLink. In August 1996, Mr. Crisp again urged upon Rambus management "the importance that we have our issued patents and any pending claims looked at long and hard" to anticipate the SyncLink standard. (CX0711 at 185). Mr. Crisp stated that it probably would not matter if SyncLink was successful "[a]s long as we collect big royalty checks every quarter." (*Id.*)

Rambus's Response to Finding No. 1630:

The evidence shows that members of the SyncLink Consortium were well aware that their proposed device could or did infringe Rambus's intellectual property. *See* RPF 557-9; 589-90. The law allows an inventor to protect his inventions from misappropriation by amending patent claims to cover such design work, as Complaint Counsel have conceded. See *Kingsdown Medical Consultants, Ltd. v. Hollister, Inc.*, 863 F.2d 867 (Fed. Cir. 1988).

D. Rambus Continued Efforts to Obtain Patents Covering the Technologies Presented at JEDEC.

1631. After withdrawing from JEDEC in June 1996, Rambus continued its efforts to perfect patent rights over the programmable CAS latency, programmable burst length, dual edge clock and on-chip PLL/DLL technologies. (CCFF 1632-1667).

Rambus's Response to Finding No. 1631:

The proposed finding is misleading and incomplete.

With respect to Rambus's withdrawal from JEDEC, Rambus actually attended its last JEDEC meeting in December 1995 and did not pay its January 1996 JEDEC dues invoice. (CCFF 1088). Rambus's June 1996 letter formalized its separation from JEDEC. (RPF 560).

With respect to Rambus's efforts to obtain patent rights over the four technologies listed

in the proposed finding, Rambus actually had no reasoned and considered belief that it could obtain patent claims that covered SDRAMs or DDR SDRAMs incorporating those technologies until late 1998. (RPF 419-31).

1632. At the time Rambus withdrew from JEDEC, it already had an issued patent containing claims covering uses of dual edge clock technology in synchronous DRAMs. After withdrawing from JEDEC, Rambus filed additional applications in order to obtain additional patents with claims relating to use of dual edge clock technology. (CCFF 1216-37, 1634-40).

Rambus's Response to Finding No. 1632:

The proposed finding is not supported by the weight of the evidence. The proposed finding refers to the '327 patent which issued on April 30, 1996 and did not cover the dual edge clock technology in the JEDEC DDR SDRAM standard. (RRFF 1216-37). Rambus did not file applications with claims relating to the use of dual edge clocking in DDR SDRAMs until after March 1998, when Joel Karp informed Rambus's board of directors that Rambus's existing patent claims were narrowly framed, but he believed that he could improve the strength of the patent portfolio. (RPF 429). The proposed finding is also misleading to the extent that it suggests that there were SDRAMs using dual edge clock technology at the time that Rambus withdrew from JEDEC. The first presentation leading to the DDR SDRAM standard did not occur until December 1996. (RPF 402-13).

1633. Rambus filed the '646 application on March 31, 1994. The '646 application is a continuation of application number 07/954,945, which is a continuation of the '898 application. (CX1493 at 2; Nusbaum, Tr. 1596).

Rambus's Response to Finding No. 1633:

Rambus has no specific response.

1634. Rambus patent application 08/222,646 (the '646 application) issued as Rambus patent no. 5,513,327 (the '327 patent) on April 30, 1996. It claims priority based on the original

‘898 application and can trace its lineage through the ‘646 application. (CX1494 at 1; First Stipulation, no. 22; Exhibit A to First Stipulation, no. 22; Nusbaum Tr. 1506-1508; *see also* DX0014).

Rambus’s Response to Finding No. 1634:

Rambus has no specific response.

1635. Rambus’s ‘327 patent contains claims covering the most feasible way to implement the dual-edged clocking feature proposed to JEDEC in May 1992, December 1995 and March 1996 in a JEDEC-compliant SDRAM. (Jacob, Tr. 5545-49; CCFF 1216-23, 1229-33).

Rambus’s Response to Finding No. 1635:

The proposed finding is irrelevant because the ‘327 patent did not issue until after the presentations cited. In addition, the proposed finding is misleading and incomplete as set forth in RRFF 1216.

1636. The ‘327 patent also contains claims covering DDR SDRAM as described in JEDEC Specification JESD 79 (June 2000). (Jacob, Tr. 5550-60; CCFF 1224-28, 1234-37).

Rambus’s Response to Finding No. 1636:

The proposed finding is irrelevant: Rambus withdrew from JEDEC over 4 years before JESD 79 was published. The proposed finding is also incorrect as set forth in RRFF 1217, 1224-28 and 1234-37.

1637. On February 19, 1999, Rambus filed application no. 09/252,998 (“the ‘998 application”), which traced back to the ‘646 application. The ‘327 patent was listed under related U.S. application data. (CX1523 at 1).

Rambus’s Response to Finding No. 1637:

The proposed finding is misleading in noting that ‘998 application traced back to the ‘646 application, which issued as the ‘327 patent, and that the ‘327 patent was listed under

related U.S. application data in the '214 patent which issued from the '998 application. (CX1523 at 1). Presumably, Complaint Counsel include these random facts to suggest that it is evidence of some significant relationship between the claims of the '214 and '327 patents. This suggestion is misleading since the claims of patents that can be traced back to the '646 application may be drawn to entirely different inventions then the claims of the '327 patent. For example, the '918 patent which relates to variable block size (CCFF 1666), not dual edge clocking, likewise can be traced to the '646 application and lists the '327 patent under related U.S. application data. (CX1525 at 1; CCFF 1664).

1638. On February 29, 2000, the '998 application issued as patent no. 6,032,214 ("the '214 patent"). (CX1523).

Rambus's Response to Finding No. 1638:

Rambus has no specific response.

1639. Independent claims 1 and 15 of the '214 patent relate to outputting data with respect to a first and a second clock signal. (CX1523 at 29 (Claim 15 recites: "A method of operation of a synchronous memory device . . . wherein a first portion of the first amount of data is output synchronously with respect to the first external clock signal and a second portion of the first amount of data is output synchronously with respect to the second external clock signal.")).

Rambus's Response to Finding No. 1639:

The proposed finding is misleading because it omits other significant limitations in claims 1 and 15, such as that the memory device receives block size information. (CX1523 at 28-29).

1640. Rambus has taken the position that claims 1 and 15 of the '214 patent cover use of double data rate in combination with variable block or burst size. (CX1371 at 64-70 (comparing claim 1 of the '214 patent to the mode register and timing diagrams of a JEDEC DDR SDRAM data sheet); CX1383 at 60, 63-66 (same); s*ee also* Rambus Brief, *Rambus Inc. v. Infineon Technologies AG*, (Feb. 1, 2001), at 7-8 (Judicial Notice taken, Tr. 1581-82, marked by not admitted as CX1877) (the "double data rate" invention "allow[ed] data to be sent out on

both the tick and the tock (the rising and falling edges) of the clock"; "Claim 15 of the '214 is a representative claim covering the double data rate invention in combination with the variable block size (burst) described above.")).

Rambus's Response to Finding No. 1640:

The proposed finding is misleading. Rambus has taken the position that claim 15 covers certain DDR SDRAMs that Rambus has investigated because the method of operation of those DDR SDRAMs meets each and every limitation of those claims. (*See* Nusbaum, Tr. 1565-66 (A claim covers a device if "each and every limitation in the claim . . .finds a counterpart in [the device]")). Two of those limitations can be described as double data rate and variable block size. The evidence does not support the implication of the proposed finding that Rambus has taken the position that claim 1 of the '214 patent is infringed by any DDR SDRAM device. The presentation that Complaint Counsel cite with respect to claim 1 of the '214 patent concerns graphic chips. (CX1371).

1641. After Rambus withdrew from JEDEC, it continued to prosecute a pending patent application containing claims covering uses of an on-chip phase lock loop circuit in synchronous DRAMs. Rambus also filed additional patent applications containing claims relating to on-chip PLL/DLL technology after it withdrew from JEDEC. (CCFF 1642-48).

Rambus's Response to Finding No. 1641:

The proposed finding is incorrect. The pending patent application cited by Complaint Counsel relates to delay locked loops (DLLs), not phase locked loops (PLLs); moreover there is no evidence to suggest that it covered uses of DLLs in SDRAMs. Rambus did not file applications with claims relating to use of on-chip DLL in DDR SDRAMs until after March 1998, when Joel Karp informed Rambus's board of directors that Rambus's existing patent claims were narrowly framed, but he believed that he could improve the strength of the patent

portfolio. (RPF 429).

1642. Beginning in June 1993 and continuing throughout the time that Rambus was a member of JEDEC, Rambus patent application 07/847,692 (the '692 application) contained claim 151 that a reasonable engineer could interpret as covering, a phase lock loop (PLL) incorporated into a JEDEC-complaint synchronous DRAM. (Nusbaum, Tr. 1582-95; Jacob, Tr. 5533-41).

Rambus's Response to Finding No. 1642:

The proposed finding is incorrect, as set forth in RRFF 1187-93.

1643. Rambus filed application no. 08/749,729 (the '729 application) as a continuation of the '692 application on November 15, 1996. Rambus included claim 151 of the '692 application as claim 151 in the new '729 application. (CX1502 at 305-13, 319; CX1459).

Rambus's Response to Finding No. 1643:

Rambus has no specific response.

1644. The '729 application issued as the 5,657,481 (the '481) patent on August 12, 1997. (CX1503 at 1). Claim 151 of the '729 application became claim 1 of the '481 patent. (CX1503 at 26; CX1502 at 306).

Rambus's Response to Finding No. 1644:

The proposed finding is misleading because, in conjunction with the two previous proposed findings, it suggests that the "claim 151" that issued as claim 1 of the '481 patent was the same as the "claim 151" that was pending while Rambus was a member of JEDEC. In fact, claim 151 was further amended after Rambus left JEDEC. (CX1502 at 306, 313 (amendment of claim 151 in December 1996)).

1645. At the time the '481 patent issued, Rambus described the patent in internal documents as containing an independent claim covering a memory device that includes phase lock loop circuitry. (CX0948 ("The 5 independent claims cover the following: (a) A memory device that . . . includes phase locked loop circuitry which varies the delay of the local clock signal to create an internal, synchronized clock to operate the interface circuitry on the memory device."); *see also* CX1244 at 1 ("pll-on-a-memory-device patents/'481")).

Rambus's Response to Finding No. 1645:

The proposed finding is misleading. The shorthand notation in certain internal documents does not accurately reflect the coverage of the claim. A claim of the '481 patent will only cover a device if each and every limitation of the claim is found in the device. (Nusbaum, Tr. 1565-66). This requires much more than that the claim simply comprised "phase locked loop circuitry." (See CX1503 at 26-27 (claims of the '481 patent)).

The '481 patent has not been asserted against SDRAMs or DDR SDRAMs. (Stipulated Patent Tree).

1646. On February 10, 1997, Rambus filed patent application no. 08/798,525 (the '525 application). This application issued as Rambus patent no. 5,954,804 (the '804 patent) on September 21, 1999. The '804 patent claims a priority date of April 18, 1990 based on the original '898 application and traces its history through the '961 and '490 applications, which it lists as related applications. (CX1518 at 1; First Stipulation, no. 22; Exhibit A to First Stipulation, no. 22; Nusbaum Tr. 1506-1508; *see also* DX0014).

Rambus's Response to Finding No. 1646:

Rambus has no specific response.

1647. Claim 26 of the '804 patent relates to delay lock loop circuitry. (CX1518 at 31 (Claim 26 recites, "An integrated circuit device . . . [that] comprises: . . . delay locked loop circuitry to generate an internal clock signal using the first and second external clock signals . . . .")).

Rambus's Response to Finding No. 1647:

The proposed finding is misleading because it omits other significant limitations in claim 26. (CX1518 at 31).

1648. Rambus has taken the position that the '804 patent covers use of delay lock loop technology in combination with programmable CAS latency. (Rambus Brief, *Rambus Inc. v. Infineon Technologies AG*, (Feb. 1, 2001), at 9 (Judicial Notice taken, Tr. 1581-82, marked but not admitted as CX1877) ("Claim 26 of the '804 patent is a representative claim covering the delay locked loop invention in combination with [programmable CAS] latency . . . .")).

Rambus's Response to Finding No. 1648:

The proposed finding is misleading. Rambus has taken the position that claim 26 covers certain DDR SDRAMs because those DDR SDRAMs meets each and every limitation of that claim. (See Nusbaum, Tr. 1565-66 (A claim covers a device if "each and every limitation in the claim . . .finds a counterpart in [the device]")). Two of those limitations are met by DDR SDRAMs by virtue of their delayed locked loops and their implementation of programmable CAS latency.

1649. From January 1995 until February 1996, Rambus had claims in pending patent applications, the 07/847,961 (the '961 application) and the 08/469,490 (the '490 application), that contained claims covering the programmable CAS latency feature of a JEDEC compliant SDRAM or its use. (CCFF 1127-82).

Rambus's Response to Finding No. 1649:

The proposed finding is misleading. The claims that Complaint Counsel assert covered SDRAMs, claims 183-185, were withdrawn from further consideration as of November 27, 1995 pursuant to a PTO restriction requirement. (CX1504 at 274-75; Fliesler, Tr. 8853-54).

The proposed finding is also incorrect. The claims of the '961 and '490 applications did not cover JEDEC-compliant SDRAMs. (RRFF 1127-82).

1650. Not long after Rambus withdrew from JEDEC, Rambus renewed its attempts to obtain a patent containing claims covering programmable CAS latency in synchronous DRAMs. (CCFF 1651-61).

Rambus's Response to Finding No. 1650:

The proposed finding is misleading. Complaint Counsel do not allege that Rambus filed any claims different from those pending while Rambus was at JEDEC until 1998 when Rambus amended claims in the '520 application. (CCFF 1655). The '520 application issued as the '580

patent (CCFF 1656), which has not been asserted against SDRAMs or DDR SDRAMs (Stipulated Patent Tree).

1651. Claims 183-185 of the '490 application covered a JEDEC-compliant SDRAM having programmable CAS latency, a computer system using that SDRAM, or a method of programming it. (Nusbaum, Tr. 1574-81; Jacob, Tr. 5528-32).

Rambus's Response to Finding No. 1651:

The proposed finding is incorrect, as set forth in RRFF 1164-82.

1652. Rambus cancelled claims 183-185 of the '490 application on February 26, 1996 in response to a restriction requirement by the patent examiner. (CX1504 at 279) ("Please cancel claims . . . 183-185 without prejudice to the filing of continuations or divisionals")). However, Rambus resubmitted those claims to the PTO in application 08/798,520, which also claims priority to the '898 application. (CX1509 at 187-89; CX1504 at 264-266; First Stipulation, no. 22; Exhibit A to First Stipulation, no. 22; *see also* DX0014).

Rambus's Response to Finding No. 1652:

The proposed finding is misleading. Claims 183-185 were withdrawn from further consideration as of November 27, 1995 pursuant to a PTO restriction requirement. (CX1504 at 274-75; Fliesler, Tr. 8853-54).

1653. On February 10, 1997, Rambus filed its 08/798,520 patent application (the '520 application). The '520 application was divisional of the 08/448,657 patent application ("the '657 application"), which in turn was a divisional application of the '646 application. (CX1509 at 184). The '520 application claims priority based on the '898 application. (First Stipulation, no. 22; Exhibit A to First Stipulation, no. 22; Nusbaum Tr. 1506-1508; *see also* DX0014).

Rambus's Response to Finding No. 1653:

Rambus has no specific response.

1654. On February 10, 1997, Rambus submitted to the PTO a Preliminary Amendment to the '520 application adding claims 156-158. (CX1509 at 184). The text of claims 156-158 in the '520 application is identical to the text of claims 183-185 in the '490 application. (CX1504 at 264-266; CX1509 at 187-88, 189 ("This divisional application includes claims 156-158 which correspond to claims 183-185, respectively, from related application Serial No. 08/469, 490 filed June 6, 1995 . . .")).

Rambus's Response to Finding No. 1654:

Rambus has no specific response.

1655. On January 20, 1998, Rambus amended claim 156 of the '520 application. (CX1509 at 227). Rambus did not represent that the amendment changed the scope of claim 156. (CX1509 at 231-35, and specifically at 232 (the purpose of the amendment was "to further prosecution of the claimed invention.")).

Rambus's Response to Finding No. 1655:

The proposed finding is misleading to the extent that it suggests that, absent a statement to that effect by the patent applicant, a claim amendment will not change the scope of a claim. The amendment to claim 156 introduced significant changes (CX1509 at 227), and Complaint Counsel has introduced no evidence to indicate that the scope remained unchanged.

1656. The patent examiner allowed claim 156 of the '520 application in this form. It became claim 1 of Rambus patent 5,841,580, (the '580 patent), which issued on November 24, 1998. (CX1510 at 1, 29).

Rambus's Response to Finding No. 1656:

Rambus has no specific response.

1657. On November 20, 1998, Rambus filed application no. 09/196,200 ("the '200 application"), which was a continuation of the '520 application. (CX1507 at 96).

Rambus's Response to Finding No. 1657:

Rambus has no specific response.

1658. The patent examiner rejected claim 151 of the '200 application because it was not patentably distinct from claim 1 of the '580 patent and thus constituted double patenting. (CX1507 at 88 ("Claim 151 is rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 5,841,540 [5,841,580]. Although the conflicting claims are not identical, they are not patentably distinct from each other because the bus transaction request would include the read request.")).

Rambus's Response to Finding No. 1658:

The proposed finding is misleading and incomplete. There are two kinds of "double patenting" rejections – statutory "same invention" double patenting, and non-statutory "obviousness-type" double patenting. (MPEP § 804). In this case, the rejection was of the second type, meaning that the examiner determined that the two claims at issue were *not* drawn to the same invention.

1659. In order to overcome the patent examiner's double patenting objection, Rambus submitted a terminal disclaimer for the '200 application that disclaimed the term of any patent beyond the expiration date of the '580 patent. (CX1507 at 76).

Rambus's Response to Finding No. 1659:

The proposed finding is misleading and incomplete. The filing of a terminal disclaimer to obviate a rejection based on nonstatutory double patenting is not an admission of the propriety of the rejection. (MPEP § 804 (citing *Quad Environmental Technologies Corp. v. Union Sanitary District*, 946 F.2d 870, 20 USPQ2d 1392 (Fed. Cir. 1991).).

1660. Following the terminal disclaimer, the examiner allowed the '200 application, which issued as Rambus patent 5,953,263 ("the '263 patent") on September 14, 1999. (CX1517 at 1; CX1507 at 32). Claim 151 of the '200 application issued as claim 1 of the '263 patent. (CX1507 at 98; CX1517 at 29).

Rambus's Response to Finding No. 1660:

Rambus has no specific response.

1661. Rambus has taken the position that claims contained in the '263 patent cover use of programmable CAS latency. (CX1383 at 13 (applying elements of claim 18 of the '263 patent to the CAS latency portion of a mode register diagram); CX1371 at 16-18, 21-22, 24 (stating that a programmable mode register that includes bits specifying the read latency infringes the '263 patent); *see also* Rambus Brief, *Rambus Inc. v. Infineon Technologies AG*, (Feb. 1, 2003), at 5-6 (Judicial Notice taken, Tr. 1581-82, marked but not admitted as CX1877) (the '263 patent applies to use of programmable CAS latency because "a programmable register can be added to a DRAM chip to establish a known delay time or latency" and that "Claim 1 of

the ‘263 patent is a representative claim covering this invention.”)).

Rambus’s Response to Finding No. 1661:

The proposed finding is misleading. Rambus has taken the position that claims contained in the ‘263 patent cover certain SDRAMs and DDR SDRAMs because those devices meet each and every limitation of that claim. (See Nusbaum, Tr. 1565-66 (A claim covers a device if “each and every limitation in the claim . . .finds a counterpart in [the device]”)). One of those limitations is met by SDRAMs and DDR SDRAMs by virtue of their implementation of programmable CAS latency.

1662. While a member of JEDEC, Rambus had claims in the ‘961 patent application that covered the programmable burst length feature of a JEDEC compliant SDRAM or its use. (CCFF 1125-39, 1148-53, 1158-61).

Rambus’s Response to Finding No. 1662:

The proposed finding is incorrect. (RRFF 1125-39, 1148-53, 1158-61).

1663. After withdrawing from JEDEC, Rambus renewed its attempts to obtain a patent containing claims covering programmable burst length in synchronous DRAMs. (CCFF 1664-67).

Rambus’s Response to Finding No. 1663:

The proposed finding is misleading. First, it suggests, contrary to the weight of the evidence, that Rambus attempted to obtain a patent covering programmable burst length in synchronous DRAMs prior to withdrawing from JEDEC. The only evidence Complaint Counsel cite in this regard are the claims of the ‘961 application which do not even mention “burst length” or “block size” (CX1504 at 218-24), and which the Federal Circuit has held do not cover the JEDEC SDRAM standard (RRFF 1125). Second, Complaint Counsel do not allege any attempt on Rambus’s part to obtain a patent covering programmable burst length in

synchronous DRAMs after withdrawing from JEDEC until 1999. (CCFF 1664).

1664. On February 19, 1999, Rambus filed patent application no. 09/252/997 ("the '997 application"). The '997 application traced its lineage through the '646 application back to the '898 application. The '327 was listed as related U.S. application data. (CX1525 at 1; *see also* First Stipulation, No. 22; Exhibit A to First Stipulations, No. 22; Nusbaum Tr. 1506-1508; *see also* DX0014)).

Rambus's Response to Finding No. 1664:

Rambus has no specific response.

1665. On March 7, 2000, the '997 application issued a U.S. patent no. 6,034,918 (the '918 patent). (CX1525).

Rambus's Response to Finding No. 1665:

Rambus has no specific response.

1666. Claims 1 and 18 of the '918 patent relate to programmable block size. (CX1525 at 30 (Claim 18 recites: "A method of operation of a synchronous memory device, wherein . . . the method of operation of the memory device comprises: . . . receiving first block size information from a bus controller, wherein the first block size information defines a first amount of data to be output by the memory device onto a bus in response to a read request . . . .")).

Rambus's Response to Finding No. 1666:

The proposed finding is misleading because it omits other significant limitations in claims 1 and 18. (CX1525 at 29-30). The proposed finding is also misleading to the extent that by "programmable" block size it means to suggest storing the block size value in a register. The claims of the '918 patent include limitations concerning a controller "providing" block size information to a memory device, or the memory device "receiving" block size information, but do not require that the value be stored in a register. (*Id.*)

1667. Rambus has taken the position that claims of the '918 patent cover use of programmable burst length. (CX1383 at 36, 43 (applying elements of claims 1 and 8 (a dependent claim of claim 1) of the '918 patent to the burst length portion of a mode register diagram); CX1371 at 91-94, 97 (stating that a programmable mode register that includes bits

specifying the burst length infringes the '918 patent); *see also* Rambus Brief, *Rambus Inc. v. Infineon Technologies AG*, (Feb. 1, 2001), at 5-6 (Judicial Notice taken, Tr. 1581-82, marked but not admitted as CX1877) (stating that claims of the '918 patent cover programmable burst length because "additional circuitry (allowing for a programmable block or burst size) can be added to the prior art DRAM chip so as to allow for the output of a variably sized block of data (or burst of data) . . . " and that "Claim 18 of the '918 patent is a representative claim covering this invention.")).

Rambus's Response to Finding No. 1667:

The proposed finding is misleading. Rambus has taken the position that claims contained in the '918 patent cover certain SDRAMs and DDR SDRAMs because those devices meet each and every limitation of that claim. (See Nusbaum, Tr. 1565-66 (A claim covers a device if "each and every limitation in the claim . . .finds a counterpart in [the device]")). One of those limitations is met by SDRAMs and DDR SDRAMs by virtue of their implementation of programmable burst length since storage of a burst length value in a mode register first requires that it be received.

1668. Complaint Counsel lacks information about Rambus's understanding of any of the above-listed patents and applications, or other patents in the '898 family that Rambus has asserted against SDRAM and DDR SDRAM, because Rambus has asserted attorney-client and work product privileges with respect to all correspondence to, from or among attorneys (other than correspondence to or from the PTO) relating to the prosecution of these patents. (Steinberg Motion *In Limine*, Attachment 9, Rambus Privilege Log Entries).

Rambus's Response to Finding No. 1668:

Rambus has no specific response.

1669. After leaving JEDEC in June 1996, Rambus continued to prosecute patents at foreign patent offices. (CX1496 at 1; CX1499 at 1; CX1506 at 1; CX1511 at 1; CX1515 at 1; CX1519 at 1; CX1527 at 1; CX1529 at 1; CX1533 at 1; CX1535 at 3; CX1536 at 1; Crisp, Tr. 3405).

Rambus's Response to Finding No. 1669:

Rambus has no specific response.

1670. A Korean Patent No. titled, "Integrated Circuit I/O Using a High Performance Bus Interface," was granted in 1999. (CX1515 at 1). That patent claims priority based on Rambus's original U.S. patent application no. 07/510,898, and the benefit of its April 18, 1990 filing date. (*Id.*).

Rambus's Response to Finding No. 1670:

Rambus has no specific response.

1671. German Patent No. 9117296.9 was granted on April 6, 2000. (CX1527 at 1). That patent claims priority based on Rambus's original U.S. patent application no. 07/510,898, and the benefit of its April 18, 1990 filing date. (*Id.*).

Rambus's Response to Finding No. 1671:

The proposed finding is incorrect. The exhibit cited is a German utility model, not a patent, which differs from a patent in various respects.

1672. European Patent No. EP 0525068 B1, entitled "Semiconductor Memory Device," was granted April 19, 2000. (CX1529 at 1). That patent claims priority based on Rambus's original U.S. patent application no. 07/510,898, and the benefit of its April 18, 1990 filing date. (*Id.*).

Rambus's Response to Finding No. 1672:

Rambus has no specific response.

1673. European Patent No. EP 1004956B1, entitled "Method of operating a synchronous memory having a variable data output length," was granted on January 3, 2001. (CX1533 at 2). That patent claims priority based on Rambus's original U.S. patent application no. 07/510,898, and the benefit of its April 18, 1990 filing date. (*Id.*).

Rambus's Response to Finding No. 1673:

Rambus has no specific response.

1674. European Patent No. EP 1022642B1, entitled "Integrated circuit I/O using a high performance bus interface," was granted on September 5, 2001. (CX1536 at 1). That patent claims priority based on Rambus's original U.S. patent application no. 07/510,898, and the benefit of its April 18, 1990 filing date. (*Id.*).

Rambus's Response to Finding No. 1674:

Rambus has no specific response.

1675. Complaint Counsel has limited information regarding the prosecution of all foreign patents because Respondent has asserted attorney-client privilege with respect to work involving foreign filings. (Vincent, Tr. 7879). There are well over one hundred communications regarding Rambus's foreign patent filings between July 1996 and early 2000 that were not produced to Complaint Counsel because Respondent asserted the attorney-client privilege. (Steinberg Motion *In Limine*, Attachment 9, Rambus Privilege Log Entries: 52-100, 105-113, 115, 132-137, 154-156, 158-164, 166-173, 177-180, 206-227, 248-259).

Rambus's Response to Finding No. 1675:

Rambus has no specific response.

E. Rambus Continued to Conceal Its JEDEC-Related Intellectual Property after its Withdrawal from JEDEC.

1676. After its withdrawal from JEDEC, Rambus continued to conceal from the DRAM industry that it believed SyncLink and DDR SDRAM infringed Rambus patents. (CX0939 at 1 (Davidow July 1997 email: "One of the things we have avoided discussing with our partners is intellectual property problem discussed in the fourth paragraph [referring to Rambus's thinking that SLDRAM and SDRAM DDR infringed Rambus's patents]"; CX2109 at 149-50 (Davidow, Dep.); CX0936 at 1 (Davidow July 1997 email: "We have not discussed [possible infringement] with the DRAM manufacturers. We hope we never have to."); CX2109 at 136-138 (Davidow, Dep.); CX0942 at 1 (Tate August 1997 email: "our policy so far has been NOT to publicize our patents and I think we should continue with this.")).

Rambus's Response to Finding No. 1676:

This proposed finding is contradicted by the weight of the evidence. Rambus did not conceal its intellectual property from the DRAM industry – either before or after it left JEDEC. (CX2070 at 43 (Harmon, Dep.)). For example, the SyncLink Consortium minutes and related documents show a profound awareness on the part of DRAM manufacturers that the device they were designing could or would infringe Rambus's intellectual property. A few of the examples are set out below:

- RX 615 at 1 – a September 1995 trip report by Motorola JEDEC representative Mark Farley stating that "SyncLink told Motorola confidentially that there were very likely patents violated by their proposal;"
- RX 663 at 2 – the January 1996 SyncLink Consortium meeting minutes, which state that "Rambus says their patents may cover our SyncLink approach even though our method came out of early RamLink work;"
- Dr. Gustavson's testimony that in late 1995 or early 1996, he reviewed Rambus's pending European patent applications, determined that they covered everything that the Ramlink and Synclink groups were doing, and concluded that the applications would never issue (Gustavson, Tr. 9286-87);
- RX 829 at 2 – the December 1996 e-mail by Micron DRAM Marketing Manager Jeff Mailloux to Micron CEO Steve Appleton stating that "[f]rom our research, we think many Rambus patents read on prior art or other patents;"
- RX 924 at 1 – Richard Crisp's May 1997 e-mail reporting that a VIA Technologies executive had said that "he thinks that SyncLink is going to be stepping all over Rambus patents;"
- RX 966 at 3 – the January 1997 SyncLink Consortium meeting minutes, showing a desire to "collect information relevant to prior art and Rambus filings," because of a concern that "Rambus will sue individual

companies" for patent infringement;"

- RX 1001 at 5 – the September 1997 SyncLink Consortium meeting minutes, stating that it might not be such a wise move to collect information relating to Rambus patents, "because that multiplies the damages," no doubt referring to trebling of damages for willful infringement;
- CX 1030 at 1 – statement in May 1998 by LG Semicon executive Dr. Jun to Rambus engineers that he had reviewed the "SLDRAM schematics," that "it looks very similar to Rambus," and that "SLDRAM Inc. is violating Rambus patents;" and
- CX 132 at 1 – statement in minutes of July 1998 Future DRAM Task Group meeting that "Rambus and DDR are mirror images of each other when compared."

In addition, it is undisputed that Rambus's CEO Geoff Tate and Rambus Vice President Allen Roberts held a series of meetings with DRAM manufacturers in Asia in an effort to convince the manufacturers to become Rambus licensees. Mr. Tate's notes of those meetings reflect that he told DRAM manufacturers LG Semicon, Samsung, NEC, and Oki that Rambus expected to have intellectual property that would read on the SyncLink architecture and on devices manufactured in compliance with the SDRAM standard. (RPF 550-54). Rambus's CFO Gary Harmon also testified that he recalled "a couple of cases" during license negotiations where the issue of "whether the Rambus-issued patents or filed patents would cover SDRAM technologies" was discussed. (CX2070 at 43 (Harmon, Dep.)). Rambus also told Intel that it

might have IP that covered DDR SDRAMs. (MacWilliams, Tr. 4905). Rambus's statements at the September 1995 JEDEC meeting also constituted a "notification to the committee that there should be a concern" about intellectual property issues. (Kelley, Tr. 2579).

Finally, it is undisputed that by March and April 1997, Micron and other JEDEC members knew that Rambus's intellectual property claims likely reached beyond any so-called "packetized," "narrow bus" RDRAM architecture to DDR clocking schemes. (RPF 567-572; 574-582; RX 920 at 2 – Micron 4/16/97 e-mail stating that "Rambus plans legal action to request royalties on all DDR memory efforts.").

1677. In early 1997, Rambus held a DDR threat assessment meeting. (CX0919 at 1; Crisp, Tr. 3403-3404). In an email summarizing the meeting, Rambus CEO Geoffrey Tate stated, "There are many issued and in-process patents that DDR SDRAMs/SGRAMs *might* infringe." (CX0919 at 1 (asterisks in original)).

Rambus's Response to Finding No. 1677:

This proposed finding is incomplete and misleading. In his e-mail Mr. Tate explained that the reason Rambus could not be sure whether DDR SDRAMs/SGRAMs infringed Rambus patents was because there "was so little hard data and no silicon" to examine. (CX0919 at 1). At that point in time, Mr. Tate had concluded that "there are no patents we can definitely say are infringed." (*Id.*).

1678. In response to the DDR threat assessment meeting, Mr. Tate instructed his staff "NOT" to tell people that Rambus felt DDR may infringe its patents. (CX0919 at 1 ("1. keep pushing our patents through the patent office 2. do *NOT* tell customers/partners that we feel DDR may infringe – our leverage is better to wait"); Crisp, Tr. 3408 ("Mr. Tate had explained to people . . . that he didn't want us to make any allegations that there might be some infringement. . . . we were basically told to not be telling customers and partners that we think DDR might infringe our patents.")).

Rambus's Response to Finding No. 1678:

This proposed finding is incomplete and misleading. Because Mr. Tate had concluded that there are "no patents we can definitely say are infringed," his instructions to *NOT* tell customers/partners that DDR may infringe were entirely reasonable and proper. For one thing, assertions of patent infringement can and do draw declaratory relief actions. Two of the three U.S. patent suits that Rambus is currently involved in were initiated by the infringers, not by Rambus. (Appleton, Tr. 6412; RRFF 2019). From a business perspective, as Mr. Tate explained: "we did not want to go out and tell people we thought they were doing something inappropriate without something -- some more specific justification for that." (CX 2074 at 347 (Tate Depo.)). Mr. Tate also noted "we would not want to tell customers that there was possibility of infringement and then find out that there was not infringement. That would be embarrassing . . . I think the intent is clear that we would not want to go tell somebody you infringed without being able to back that up. We would not want somebody to tell us that, and vice versa. So we wanted to do some further research." (*Id.*). Mr. Tate's decision to wait until Rambus could confirm infringement reflects sound business judgment. *See* RRFF 1697, 1708.

1679. During Rambus's licensing negotiations with Micron in early 1997, Rambus never told Micron that its patent rights extended or might extend beyond direct RDRAM. (Appleton, Tr. 6350 ("Never during the discussion that we had with Rambus on the license for RDRAM did they ever indicate, ever say that somehow [] the patents that were part of RDRAM had any application to anything else besides RDRAM")).

Rambus's Response to Finding No. 1679:

This proposed finding is incomplete and misleading. First, the finding is overly broad, for Mr. Appleton did not testify that he had personal knowledge of all of the licensing discussions between the parties. Second, the license negotiations concerned RDRAM. There is

no reason to believe (or evidence to suggest) that the subject of Rambus patents relating to non-RDRAM products were a part of those negotiations. Third, there also is no evidence that Micron asked Rambus if it believed its patents covered non-RDRAM products. Fourth, in early 1997 Micron already was aware that Rambus might have patent coverage that extended beyond RDRAMs. (Lee, Tr. 6962 "Q. So you believed by March 1997 that Rambus might have intellectual property claims to clocking schemes that were not tied to the use o f a narrow bus in a multiplexed, packetized RDRAM architecture; right? A. I had concerns that they had patents to a clocking scheme that may relate to the work of the committee."). Fifth, in April 1997, just a month after the Rambus/Micron license agreement was executed, Micron learned from Intel that "Rambus feels DDR for any memory is under their patent coverage." (RX 920 at 1). Although this e-mail was widely distributed within Micron, and even reached Jeff Mailloux, who was then Micron's DRAM marketing manager, there is no evidence that anyone from Micron contacted Rambus to confirm or deny the information.

1680. During Rambus's licensing negotiations with Micron in early 1997, Rambus never told Micron that Rambus believed it possessed, or would be able to obtain patent rights extending to any aspect of SDRAM. (Appleton, Tr. 6348; Lee, Tr. 6619). In early 1997, Rambus knew that Micron was working on SDRAM. (Appleton, Tr. 6351). During this time period, Micron would have considered it important to know if Rambus believed it possessed patent rights over an aspect of SDRAM. (Appleton, Tr. 6352).

Rambus's Response to Finding No. 1680:

This proposed finding is incomplete and misleading. *See* RRFF 1679.

1681. During Rambus's licensing negotiations with Micron in early 1997, Rambus never told Micron that Rambus believed it possessed, or would be able to obtain patent rights extending to SyncLink DRAM technology. (Appleton, Tr. 6353).

Rambus's Response to Finding No. 1681:

This proposed finding is incomplete and misleading. Micron was well aware of the likelihood that the SyncLink device would infringe Rambus's intellectual property. For example, several Micron representatives were present at the July 1997 SyncLink meeting, the minutes of which state:

> "Consortium should collect information relevant to prior art and Rambus filings. . . . Rambus will sue individual companies instead of Consortium. Companies will then ask Gustavson etc. for prior art info.
>
> . . .
>
> First company to be sued will organize the materials, and ask for help. . . ."

(RX 966 at 3). (*See also* RRFF 1679; RX 1001 at 5).

1682. During Rambus's negotiations with Siemens in 1997, Rambus never told Siemens that it thought DDR SDRAM and SyncLink would infringe Rambus patents. (CX0937 at 1; CX0939 at 1 (Mooring July 1997 email: "We have not yet told Siemens that we think SLDRAM and SDRAM-DDR infringe our patents. We think that will just irritate them. Hopefully, SLDRAM and DDR will die due to their technical/infrastructure faults so we don't have to play that card."); CX2109 at 144 (Davidow, Dep.); CX2088 at 75-77 (Tate, Infineon Trial Tr.)).

Rambus's Response to Finding No. 1682:

This proposed finding is incomplete and misleading. First, the license negotiations concerned RDRAM. There is no reason to believe (or evidence to suggest) that the subject of Rambus patents relating to non-RDRAM products should have been part of those negotiations. Second, there also is no evidence that Siemens asked Rambus if it believed its patents covered non-RDRAM products. Third, there is ample evidence in the record demonstrating that

Siemens already believed Rambus might have patents relating to non-RDRAM devices. As Siemens' JEDEC representative Willi Meyer testified, "[i]f they had invented something then they would get a patent for it. And we were absolutely sure that Rambus was trying to get patents." (CX 2089, Meyer Infineon 4/26/01 Trial Tr. at 75). (*See also* RX-269; RX-286A at 2 (noting "similarity of the SDRAM with the Rambus device architecture"); RX-289; RX-321; RX-488A ("All computers will (have to be) built like this someday, but hopefully without royalties to Rambus."). Fourth, Siemens, like Micron, was present at SyncLink meetings in 1997 where the prospect of patent infringement litigation involving Rambus patents was discussed. (RX 966 at 3; RX 1001 at 5).

1683. During a 1997 meeting between Rambus and Korean DRAM maker LG, an LG executive explained to Mr. Tate that LG's reason for favoring DDR was that it understood DDR to be a "royalty-free . . . open, jedec standard." (CX0957 at 1). It appears that Mr. Tate did nothing to disabuse LG's beliefs regarding the "open" and "royalty-free" nature of JEDEC's DDR SDRAM standard. (*Id.* at 1-2).

Rambus's Response to Finding No. 1683:

This proposed finding is contradicted by the weight of the evidence. During a meeting in Korea in October 1995, Rambus informed LG Semiconductor that Rambus had or might obtain intellectual property rights that might apply to non-RDRAM products. (CX 2111, Tate Depo. at 314-15; CX 1729 at 96). In addition, an LG Semicon executive named Dr. Jun informed Rambus engineers in May 1998 that he had reviewed the "SLDRAM schematics," that they "look very similar to Rambus," and that "SLDRAM Inc. is violating Rambus patents." (CX 1030 at 1).

1684. In August 1997, Rambus believed that people did not understand the significance of the 5,513,327 patent, which included claims related to moving data on the rising and the falling edges of the clock. (CX1494; CX0942 at 1 (Tate August 1997 email: "we already have

the 327 patent but few people are aware of what it means."); Diepenbrock, Tr. 6145-46; Hampel, Tr. 8732-33 (Mr. Hampel could not recall any instance in which Rambus representatives told the DRAM manufacturers which features of RDRAM were protected by Rambus patents or patent applications)). Rambus had omitted the '327 patent from its June 1996 JEDEC withdrawal letter. (CX0888 at 1-2).

Rambus's Response to Finding No. 1684:

This proposed finding is incomplete, misleading and irrelevant. Nothing suggests that Rambus's conduct relating to disclosure of or beliefs about its intellectual property after it withdrew from JEDEC is relevant to the issues presented in this case. Second, Rambus has not asserted the '327 patent against JEDEC-compliant parts. (Parties' First Set of Stipulations, Patent Tree). Third, the '327 patent does not read on DDR SDRAM products. (*See* RPF 354-56). Fourth, there was nothing sinister about Rambus's omission of the '327 patent from its June 1996 letter to JEDEC. It was Lester Vincent's responsibility to compile the list of patents communicated to JEDEC in Rambus's June 1996 letter. (CX 3129, Vincent Dep. Tr., 537-39). Mr. Vincent explained that the '327 was accidentally omitted and that no one at Rambus instructed him to leave the '327 patent off the list. (*Id.*). Finally, the list of Rambus patents e-mailed by a Hynix executive in 1998 to a large group of industry participants included the '327 patent. (RX 1214 at 1). Complaint Counsel's technical expert, Dr. Bruce Jacob, who has testified (contrary to Rambus's expert) that claims contained in the '327 patent are infringed by memory devices that comply with the DDR SDRAM standard, has *also* testified that if the engineers who received this e-mail, were reasonable engineers, *they would have known* from looking at the '327 patent that it covered the DDR SDRAM device they were working on at the time. (Jacob, Tr. 5675).

In light of the foregoing, it is clear that after Rambus left JEDEC, various JEDEC

members were aware of possible Rambus patent claims relating to the work of the JC 42.3 committee. There is no record evidence that any of these members contacted Rambus to make any further inquiry regarding those possible claims or to ask Rambus for "RAND" assurances.

1685. Rambus believed that "competitive solutions" such as DDR SDRAMs and SLDRAMs would likely infringe its '327 and new '481, PLL/DLL on DRAM patent. (CX1503 (Rambus's 5,657,481 patent issued on August 12, 1997); Diepenbrock, Tr. 6183; CX0942 at 1 (Tate August 1997 email: "ddr/sldram are likely to infringe" these two patents)).

Rambus's Response to Finding No. 1685:

This proposed finding is vague and ambiguous as to time frame, incomplete and misleading. The cited evidence is dated after Rambus left JEDEC. There is nothing to suggest that Rambus's conduct relating to disclosure of or beliefs about its intellectual property *after* it withdrew from JEDEC is relevant to the issues presented in this case. This proposed finding is not supported by the evidence. The cited "testimony" from Mr. Diepenbrock consisted of Complaint Counsel reading from a document followed by a privilege objection being sustained. (Diepenbrock, Tr. 6183-84). This is not evidence of anything. Finally, the cited e-mail simply demonstrates a general belief that, upon further research, turned out to be incorrect. (CX 2102 at 304-06 (Karp Depo.); CX 2109 at 27-28 (Davidow Depo.)).

1686. Eight days before the 5,657,481 patent issued, Mr. Tate reminded his staff that Rambus's policy had been "NOT to publicize our patents" and suggested that staff continue this approach. (CX0942 at 1). Mr. Tate further instructed his staff to prepare a position statement in case Rambus received calls from the press when the new patent issued. (*Id.*)

Rambus's Response to Finding No. 1686:

This proposed finding is incomplete and misleading. The references in the cited e-mail to press inquiries shows that when Mr. Tate used the word "publicize," he meant press statements. The e-mail also notes that by August 1997, Rambus already had made "verbal"

statements to Intel suggesting that Rambus might have IP that covered DDR and Synclink. Of course, the weight of the evidence shows that all JEDEC members were aware that Rambus might have patents reading on dual edge clocking schemes. RRFF 1676, 1679-1683. The cited evidence thus supports Rambus' position that the DRAM industry was not misled or lulled by Rambus regarding the possible scope of Rambus patents.

1687. Rambus employees created a "party line" to help address any inquiries about the newly issued 5,657,481 patent, which avoided comment directly on whether SDRAMs or DDR SDRAMs infringed the patent. (CX0948 at 1; CX0947 at 1 ("Q3: Do Double Data Rate (DDR) SDRAMs use this patent? A: We don't know yet. No DDR products exist for us to evaluate.")).

Rambus's Response to Finding No. 1687:

This proposed finding is misleading if it is intended to suggest that the position taken in the e-mail – that Rambus did not at that time know whether or not its patents would be infringed by a DDR SDRAM product – was untrue. As documented in numerous places, Rambus was not able to make a definitive determination regarding DDR SDRAM infringement because there "was so little hard data and no silicon" for DDR SDRAMs to examine. (CX0919 at 1). Any definitive statement from Rambus regarding DDR SDRAM infringement before there were DDR parts to examine would have been premature and risky. *See* RRFF 1697, 1708.

1688. During the same timeframe that Rambus was concealing its JEDEC-related intellectual property from the DRAM industry, Rambus made limited, private disclosures to its partner, Intel. (CCFF 1694-95).

Rambus's Response to Finding No. 1688:

This proposed finding is vague and ambiguous regarding time frame, internally inconsistent and actually supports Rambus' position that the DRAM industry was not lulled into infringing Rambus patents. Complaint Counsel concede in this finding that Rambus was

alerting industry members (here Intel) regarding the possibility that JEDEC-compliant parts might infringe Rambus patents.

1689. In August 1996, Rambus was concerned that Intel might support 200 Mhz SDRAMs. (CX0898 at 1 (Barth August 1996 email discussing concern with Intel supporting 200MHz SDRAMs)). At the time, Rambus CEO Geoffrey Tate suggested that one way to deal with this threat might be to alert Intel that, among other "potential problems," these devices might infringe upon Rambus patents. (CX0897 at1 (Tate August 1996 email: "my gut-level inclinations on an action plan . . . send intel a rambus assessment on 200mhz sdram raising the potential problems we see with feasibility, risk and compatability; *AND* point out that we have issued patents that this proposal could very well infringe")).

Rambus's Response to Finding No. 1689:

The cited evidence and proposed finding supports Rambus' position that the DRAM industry was not lulled into infringing Rambus patents. In August 1996, Rambus was alerting industry members (here Intel) regarding the possibility that JEDEC-compliant parts might infringe Rambus patents.

1690. In the second half of 1997, Rambus was concerned that Intel was considering supporting DDR through a DDR-compatible chipset. (CX0942 at 1). Rambus believed that Intel could be scared into a DDR program because Intel's principal chipset rival – VIA – was itself "aggressively promoting DDR." (CX0968 at 1 (Crisp November 1997 email suggesting that VIA's support for DDR, along with the support of other companies, had Intel worried and could cause Intel to "be scared into doing a DDR program."); *see also* CX0655 at 1 ("certain groups within Intel are supposedly talking about DDR for main memory")).

Rambus's Response to Finding No. 1690:

Rambus has no specific response.

1691. Rambus planned to persuade Intel not to develop a chipset that would support DDR SDRAM memory. Rambus CEO Geoffrey Tate suggested that Rambus "meet with intel . . . to get them aware that IF they were to consider a DDR chipset that there is a minefield of 60+ rambus patents that would have to be avoided – we convince them 2 of the mines are real but not give them a map to the whole minefield." (CX0942 at 1).

Rambus's Response to Finding No. 1691:

This proposed finding supports Rambus's position that it did not attempt to lull the DRAM industry into producing JEDEC-compliant parts that infringed Rambus patents. As this proposed finding demonstrates, Rambus attempted to convince industry members not to produce DDR SDRAM products. This proposed finding also demonstrates that in August 1996, Rambus was alerting industry members (here Intel) regarding the possibility that JEDEC-compliant parts might infringe Rambus patents.

1692. In August 1997, Rambus CEO Geoffrey Tate wrote to his colleague David Mooring laying out strategies for convincing Intel not to develop a DDR chipset. (CX0946 at 1; CX1244 at 1 (Tate August 1997 email titled "parker/gelsinger; ddr crush plan": "i think we need to make it clear to them that we aren't going to make any significant further changes in our business deal with them without their decision they are not doing a ddr backup chipset period.")). Mr. Tate stated, "they need to know that a ddr backup chipset is first real bad for their objectives and second one that we cannot accept under our original make-us-king deal." (*Id.*) Mr. Tate also suggested that Tony Diepenbrock was ready, willing, and able to "educate" Mooring on Rambus's "double-data-rate/327 and pll-on-a-memory-device patents/481." (*Id.*)

Rambus's Response to Finding No. 1692:

This proposed finding supports Rambus's position that it did not attempt to lull the DRAM industry into producing JEDEC-compliant parts that infringed Rambus patents. As this proposed finding demonstrates, Rambus attempted to convince industry members not to produce DDR SDRAM products. This proposed finding also demonstrates that in August 1996, Rambus was alerting industry members (here Intel) regarding the possibility that JEDEC-compliant parts might infringe Rambus patents.

1693. In January 1998, Rambus executives considered telling Intel that they believed DDR and SLDRAM infringed Rambus patents in order to discourage Intel from developing non-Rambus technologies. (CX0984 at 3 (Tate January 1998 email: "should we also disclose our position on patents and that we believe ddr's/sldram/etc will likely infringe our patents? this is to show that whatever path the market takes it infringes our IP. should we tell intel

this?")).

Rambus's Response to Finding No. 1693:

This proposed finding is contradicted by the evidence. As noted in RRFF 1686, Rambus already had informed Intel verbally before August 1997 that it might have IP that JEDEC-compliant parts might infringe. (CX 942 at 1; RX 920 at 1). This proposed finding supports Rambus's position that it did not attempt to lull the DRAM industry into producing JEDEC-compliant parts that infringed Rambus patents.

1694. In late 1997 or early 1998, Rambus informed Intel in general terms that Rambus might have patent applications that would cover DDR SDRAMs, but did not provide any specific details. (MacWilliams, Tr. 4905 ("We were related this notion that [Rambus] might have something, but we were given nothing concrete. We had no specifics on what they had patents applications on. We had no patent applications in-house to look at. So it was kind of a piece of information with no immediate relevance.")).

Rambus's Response to Finding No. 1694:

This proposed finding supports Rambus's position that it did not attempt to lull the DRAM industry into producing JEDEC-compliant parts that infringed Rambus patents. As this proposed finding demonstrates, Rambus was alerting industry members (here Intel) regarding the possibility that JEDEC-compliant parts might infringe Rambus patents. This proposed finding also is misleading to the extent it attempt to fault Rambus for providing only "general" information. As documented in numerous places, Rambus was not able to make a definitive determination regarding DDR SDRAM infringement because there "was so little hard data and no silicon" for DDR SDRAMs to examine. (CX0919 at 1). Any definitive statement from Rambus regarding DDR SDRAM infringement *before* there were DDR parts to examine would have been premature and dangerous.

1695. Intel had non-disclosure agreements with Rambus that prevented it from sharing Rambus confidential information with third parties. (Calvin, Tr. 1018; CX0993 at 1 (Tate January 1998 email: our rdram partners "CANNOT disclose our confidential information to 3rd parties . . .Our partners' employees working on competitive products, e.g. DDR, might have access to our confidential information. they might even go to committees like jedec to discuss DDR. BUT they are obligated as employees of our partners' to keep our confidential information secret")).

Rambus's Response to Finding No. 1695:

This proposed finding is misleading to the extent that it suggests that Intel did not or would not pass along Rambus' views regarding possible infringement to others in the industry. As demonstrated by e-mails from Micron employees, Intel's James Akiyama provided Micron with information in April 1997 about what he understood to be Rambus's belief that "DDR for any memory is under their patent coverage." (RX 920 at 1).

1696. In early 1998, Rambus considered, but rejected, making public statements about DDR infringing Rambus patents. (CX0987 at 4 (Tate January 1998 email: "ddr infringes our patents (question: do we start saying this publicly?)")).

Rambus's Response to Finding No. 1696:

This proposed finding is incomplete and misleading. In an August 1997 e-mail, Mr. Tate explained that Rambus could not be sure whether DDR SDRAMs/SGRAMs infringed Rambus patents was because there "was so little hard data and no silicon" to examine. (CX0919 at 1). At that point in time Mr. Tate had concluded that "there are no patents we can definitely say are infringed." (*Id.*). DDR SDRAM products did not begin shipping in volume until the year 2000, at the very earliest. (Peisl, Tr. 4386; Gross, Tr. 2354) (Compaq first started using DDR SDRAM parts in 2001); (CX 2057, Meyer 12/13/00 Depo. Tr., 289:24-290:5) (Infineon had not released its production version of DDR SDRAM as of December 2000).

1697. Rambus was still concealing its JEDEC-related intellectual property in 1999.

(CX1075 at 2 (interview with Rambus CEO Geoffrey Tate: "We've made no comment on whether DDR infringes our patents. . . . Our position is there is insufficient data."); CX1089 at 1 (in December 1999, Mr. Tate advised his colleagues that, if asked questions about the potential for DDR to infringe Rambus patents, "it's important NOT to indicate/hint/wink/etc what we expect the results of our [infringement] analysis to be!!!")).

Rambus's Response to Finding No. 1697:

This proposed finding is contradicted by the weight of the evidence. The evidence shows that Rambus did not conceal its intellectual property from the DRAM industry – either before or after it left JEDEC. RPF 466-719; RRFF 800-821; 1238-1357; 1676-1696. Rambus had legitimate business justification – and legal barriers – that kept it from making public accusations of infringement. The case law is clear: a company's statements to customers or others that a competitor's products infringes its patents can lead to lawsuits charging the company with state law claims for unfair competition, trade libel or tortious interference with contract, as well as federal Lanham Act claims. *Zenith Elecs. Corp. v. Exzec, Inc.*, 182 F.3d 1340, 1353-55 (Fed. Cir. 1999); *PennPac Int'l, Inc. v. Rotonics Mfg., Inc.*, 2001 U.S. Dist. LEXIS 6842 at *33-34 (E.D. Pa. 2001).

1698. Most people in the DRAM industry believed that RDRAM and DDR SDRAM were very different technologies. (CX2749 at 1-3 (October 1999 article describing the difference between the clocking of DDR SDRAM and the clocking of RDRAM); CCFF 748, 751-53, 1281)).

Rambus's Response to Finding No. 1698:

This proposed finding is irrelevant, and the evidence in the record does not support a finding about what "most people believed. . ." In any event, *all* JEDEC members knew by March 1997 that Rambus's patent claims were likely not to be limited to a "packetized" or "narrow bus" architecture (JX 36 at 7; Lee, Tr. 6957-62; RX 880 at 25), and Micron and Intel, at

least, knew by April 1997 that "Rambus plans legal action to request royalties on all DDR memory efforts" (RX 920 at 2) and that "Rambus feels DDR for *any* memory is under their patent coverage. (RX 920 at 1) (emphasis added).

1699. Before late 1999, most people in the DRAM industry did not believe that Rambus's patents applied to SDRAMs or DDR SDRAMs. (CX2107 at 69 (Oh, Dep.); Bechtelsheim, Tr. 5841-42, 5880-81; Sussman, Tr. 1455; Kellogg, Tr. 5060; CCFF 1698)).

Rambus's Response to Finding No. 1699:

The proposed finding is contradicted by the weight of the evidence. *See* RPF 466-595; 665-706; 714-719.

1700. Rambus Vice President of Intellectual Property Joel Karp even acknowledged that most of the DRAM industry did not think Rambus's patents applied to SDRAMs and DDR SDRAMs. (CX1069 at 1) (Karp May 1999 email: "They probably think they avoid our IP if they don't go 'packetbased'").

Rambus's Response to Finding No. 1700:

This proposed finding is incomplete and misleading and is contradicted by other evidence. In fact, with Mr. Karp directly involved, Samsung participated in the standardization of synchronous DRAMs at JEDEC "*with* the expectation that Rambus held patents on aspects of what was standardized." (CX 2078 at 103 (Karp Depo.)) (emphasis added). Without supporting testimony, it is impossible to discern the precise meaning of the stray comment in the e-mail from Mr Karp cited in the proposed finding. It is likely, however, that Mr. Karp had heard Mr. Sussman, Mr. Rhoden, Mr. Wiggers, Mr. Walther or others in the DRAM industry express their view, as they often did, that any Rambus claims to the various features of Rambus technology, other than the bus architecture and packet-based protocol, would be rendered invalid by prior art. (RPF 530-58, 764-84).

F. Rambus Prepared to Enforce its Strategic Patent Portfolio.

1701. In late May 1997, Rambus CEO Geoffrey Tate considered hiring Joel Karp to coordinate Rambus's strategies for enforcing patent claims against non-Rambus technologies. (CX0928 at 1).

Rambus's Response to Finding No. 1701:

This proposed finding is contradicted by the evidence. The cited email makes clear that Mr. Tate believed that Mr. Karp's "real strength for us is negotiating deals with infringers," and that Mr. Karp would not be well suited to help Rambus with strategy. (CX 0928).

1702. Mr. Tate understood that Mr. Karp was "NOT a technologist" and thus would not be in a position "to determine who infringes [Rambus patents] and how." (CX0928 at 1). Tate expected that Karp's "real strength" would be in "negotiating deals with infringers." (CX0928 at 1).

Rambus's Response to Finding No. 1702:

This finding supports Rambus's position that it is difficult to make judgments about infringement without a thorough analysis, and that the casual beliefs of engineers about the possible scope of his company's intellectual property should not be afforded much weight.

1703. In June 1997, Mr. Tate briefly reconsidered whether Rambus should hire Mr. Karp in light of the fact that DDR devices were not likely to be available until early to mid-1998. (CX0931 at 1 (Tate June 1997 email: "i've decided to NOT make joel an offer and NOT make him a consultant. reasons: . . . DDR is not coming 2H/97 but more like 1H/98, mid-98 . . . if we get surprised and DDR happens sooner we can always . . . try to hire joel later")).

Rambus's Response to Finding No. 1703:

This proposed finding is incomplete and misleading. Mr. Tate listed six different "reasons" why he had decided not to make Mr. Karp a job offer in June 1997. Before noting anything about DDR, Mr. Tate provided his first two reasons: (1) I "suspect we'll be tight on budget q3/q4..."; and (2) "hunch he wants more in the way of title/roel/etc than i think is

productive." (CX 0931 at 1).

1704. In October 1997, Mr. Karp became Vice President of Intellectual Property at Rambus. (CX0960 at 1; CX0963 at 1; Crisp, Tr. 3410; CX2059 at 33 (Karp, Dep.)).

Rambus's Response to Finding No. 1704:

Rambus has no specific response.

1705. Mr. Karp knew from the day he was hired at Rambus that there was a good chance Rambus would end up in litigation with DRAM manufacturers. (CX2102 at 429 (Karp, Dep.)).

Rambus's Response to Finding No. 1705:

This proposed finding is incomplete and is not supported by the weight of the evidence. Mr. Karp did not testify that he "knew" there was a good chance of litigation with DRAM manufacturers. The designated testimony on this issue is instead mixed. Mr. Karp testified at one point that "it's very likely that I knew that, but again, I can't go back to that point and tell you what my mind set was at that point." (CX 2102 at 429 (Karp, Dep.)). As this phrasing suggests, he had been asked nearly the same question earlier in the same deposition and had testified as follows:

> ". . . what you're really asking is for me to go back and visit a state of mind that I might have had, you know, four years ago. And I believe that I could probably say without violating any privilege here that I believe that my job was to -- I believe that a really important part of my job was to help Rambus *avoid* litigation. It was not -- I didn't want to -- litigation was not something that I was -- that I either looked forward to or wanted to see happen."

(CX 2102 at 421 (Karp, Dep.)) (emphasis added).

1706. Rambus hired Mr. Karp to negotiate licensing agreements with manufacturers of non-Rambus DRAMs. (CX2114 at 105 (Karp, Dep.) ("they really hired me to do noncompatible licensing"); CX2059 at 33 (Karp, Dep.) ("I was hired specifically for the noncompatible licensing"); CX0960 at 1 (Karp's role "is to prepare and then to negotiate to license our patents for infringing drams (and potentially other infringing ic's)"); CX2067 at 48-50 (Davidow, Dep.); CX0963 at 1 (Tate October 1997 email announcing that Karp "joined rambus . . . as vice president responsible for assessing our patent portfolio, determining when chips infringe our patent portfolio, setting licensing strategies for infringing chips, and for negotiations with companies that build and sell infringing chips.")).

Rambus's Response to Finding No. 1706:

This proposed finding is incomplete and misleading. As Mr. Tate noted in his October 1997 email, Mr. Karp was to be responsible for several things. Mr. Tate listed those responsibilities in the following order: (1) assessing the Rambus patent portfolio; (2) determining when chips infringe Rambus patents; (3) setting licensing strategies for infringing chips; and (4) negotiating with companies that build and sell infringing chips. (CX 0963 at 1).

1707. Rambus was careful not to make it known externally what Mr. Karp was hired to do. (CX0960 at 1 (Tate October 1997 email: "when joel starts we have to have our spin control ready for partners/etc as to why we are hiring him and what he will be doing. my thought is we say externally that joel is coming on board to help us with contracts and ip licensing."); CX0963 at 1 (Tate October 1997 email to Rambus staff: "joel karp joins rambus **NOTE**: message to outside is only that 'joel is going to help us with contract negotiations'")).

Rambus's Response to Finding No. 1707:

This proposed finding is not supported by the evidence. Mr. Tate explained that Rambus would make it known publicly that Mr. Karp was being hired to help Rambus with "contracts and IP licensing." (CX 0960 at 1). This is exactly what Mr. Karp was hired to do. (CX 0963 at 1).

1708. Rambus wanted to keep Mr. Karp's job responsibilities quiet as part of its "strategy" to "downplay the whole infringement/IP issue." (CX0963 at 1 (Tate October 1997 email to Rambus staff: "currently we expect based on datasheets that both ddr sdram/sgram and sldram will infringe our patents. . . . **NOTE** - we are not making any public statement outside of rambus about joel joining. . . . Our strategy is to downplay the whole infringement/IP issue until there is actual infringement.")).

Rambus's Response to Finding No. 1708:

This proposed finding is incomplete and misleading. Rambus was being appropriately careful to analyze actual DDR parts before reaching any conclusion that they would and did infringe Rambus patents. (CX 0963 at 1 ("we cannot be sure of this [infringement] though till we actually get and examine silicon"). Indeed, any other approach would place the company at risk of defending expensive lawsuits in multiple jurisdictions. The case law is clear: a company's statements to customers or others that a competitor's products infringes its patents can lead to lawsuits charging the company with state law claims for unfair competition, trade libel or tortious interference with contract, as well as federal Lanham Act claims. *Zenith Elecs. Corp. v. Exzec, Inc.*, 182 F.3d 1340, 1353-55 (Fed. Cir. 1999); *PennPac Int'l, Inc. v. Rotonics Mfg., Inc.*, 2001 U.S. Dist. LEXIS 6842 at *33-34 (E.D. Pa. 2001).

1709. Mr. Karp contemplated suing unlicensed companies that used RDRAM. (CX0982 at 1) (Karp December 1997 email: "If unlicensed folks use our IP, we are well protected with patents and must use whatever legal remedies we deem necessary to shut them down or have them take a license from us.").

Rambus's Response to Finding No. 1709:

This proposed finding is not supported by the evidence. The cited e-mail says nothing about RDRAM.

1710. Shortly after joining Rambus, Mr. Karp began planning a campaign to collect royalties from DDR SDRAM and other non-RDRAM products. (Crisp, Tr. 3418).

Rambus's Response to Finding No. 1710:

The term "campaign" in this context is vague and potentially misleading. Rambus does not contest that part of Mr. Karp's job was to work on collecting royalties from non-Rambus compatible products that infringed Rambus's patents. (*See* RRFF 1706; CX0963 (setting forth Mr. Karp's job responsibilities)).

1711. Rambus CEO Geoffrey Tate instructed Mr. Karp not to agree to any "non-compatible" DRAM license unless the royalty rate was greater than the rates Rambus charged for its proprietary RDRAM technology. (CX0960 at 1 (Tate October 1997 email: "i advised clearly that if a chip co wants to license all of our present and future patents for use for any infringing dram, then the only acceptable deal is the royalty on infringing drams must be greater than the royalty on rambus drams.")).

Rambus's Response to Finding No. 1711:

The proposed finding is misleading. The cited evidence makes clear that in the circumstance where a chip company wants to license all of Rambus's present and future patents for use of any infringing DRAM, Mr. Tate advised Mr. Karp to negotiate a deal where the royalty on the non-compatible DRAMs would be greater than the royalty on RDRAMs. However, the very next sentence of the cited evidence also makes clear that for other circumstances, e.g., where the desired license was narrower, Rambus would be willing to agree to less or to a lump sum. ((CX0960) ("if the license was much narrower we could conceivably agree to less or to lump sum – say existing patents for just 66mhz ddr.")). Moreover, the weight of the evidence makes clear that Rambus was willing to negotiate the terms of its licenses, including the royalty term. (*See* RRFF 745; CX0733).

1712. Rambus's strategic objective in charging higher royalties for SDRAM than RDRAM was to promote the adoption of RDRAM by raising the costs of competing technologies. (CX0550 at 1 (January 1998 document setting out Rambus's "Goals for 2002": "Develop and enforce IP, A. Get access time register patent issued that reads on existing

SDRAM . . . C. Get all infringers to license our IP with royalties > RDRAM (if it is a broad license) OR sue"); CX1744A at 150 (Karp's October 1998 handwritten notes regarding a one-on-one meeting with Tate: "SDRAM Royalties – royalty rate dependent on . . . RDRAM -- idea - how to prevent a new competitive device"); CX2114 at 149-150 (Karp, Dep.); CCFF 1977-80)).

Rambus's Response to Finding No. 1712:

This proposed finding is irrelevant and misleading. Rambus does not charge higher royalty rates for SDRAM than for RDRAM, and the cited evidence does not suggest that Rambus had intentions to do so or that it actually did so. (*See* RRFF 1977-80; RPF 1361-1422). In fact, it is difficult to draw any conclusions from the cited evidence, given its fragmented nature.

1713. Mr. Karp thought it best that Rambus not make any public disclosure regarding its belief that DDR infringed Rambus patents. Karp was concerned that a public disclosure would cause DRAM manufacturers to band together to find ways to avoid paying royalties to Rambus. Mr. Karp suggested that the better strategy was to "approach companies individually and without any publicity." (CX0988 at 1 ("I am very uncomfortable with any public statements regarding who or what infringes our patents. . . . Once one or two sign up to strategic licenses it will be much easier to license the others but public pronouncements only stimulate a lot of negative emotions towards Rambus.")).

Rambus's Response to Finding No. 1713:

This proposed finding is not supported by the evidence. First, there is no indication in the cited evidence that Mr. Karp's thoughts were related to DDR. Second, there is no indication that Mr. Karp had any concerns that manufacturers would try to find ways to avoid paying royalties to Rambus. To the extent he had concerns, they were very general in nature, *e.g.*, "stimulat[ing] a lot of negative emotions towards Rambus." (CX0988).

1714. In 1997, Rambus implemented the strategic patent portfolio project. (CX2067 at 103 (Davidow, Dep.)). The term "strategic patent portfolio" "referred to the 1990 patent or continuances to the 1990 patent." (CX2109 at 198-99 (Davidow, Dep.)).

Rambus's Response to Finding No. 1714:

The proposed finding is not supported by the evidence. Mr. Davidow did not testify as asserted in the proposed finding, and his testimony makes clear that he lacked personal knowledge of the issues involved and was making an "*assumption*." (CX 2109 at 198-99 (Davidow, Dep.) (emphasis added)).

The proposed finding is also contradicted by the weight of the evidence. The evidence shows that the "strategic patent portfolio" was the entire set of patents that Neil Steinberg was prosecuting for Rambus in late 1998. (CX 2114 at 154 (Karp Depo.)).

1715. In February 1998, Mr. Karp produced a draft document entitled "Strategic Patent Licensing Program" in which he identified target royalty rates for DDR SDRAM (3.0-4.0%) and SLDRAM (3.5-5.0%). (CX0551 at 1).

Rambus's Response to Finding No. 1715:

The proposed finding omits relevant evidence. The draft document evidences various other royalty arrangements that could be worked out upon request of the licensee. In addition, the draft notes, "These licenses are granted upon reasonable and non-discriminatory terms and conditions to those who respect Rambus intellectual property rights." (CX051 at 1).

1716. In April 1998, Mr. Karp formed an internal "Rambus Patent Council," which was to "meet once a month with the intent of discussing [Rambus's] overall patent strategy/directions from a strategic perspective." (CX1017 at 1).

Rambus's Response to Finding No. 1716:

Rambus has no specific response.

1717. One of Rambus's "key results" for 1998 was securing its strategic patent portfolio. (CX1744A at 161 ("Key result . . IP rights secure strategy portfolio, convince industry that paying royalties to Rambus is a fact of life"); CX2114 at 152-154 (Karp, Dep.)).

Rambus's Response to Finding No. 1717:

Rambus has no specific response.

G. Rambus Destroyed Documents in Anticipation of Patent Enforcement Litigation.

1718. In March 1998, there was "growing worry" within Rambus about "email back-ups as being discoverable information" in future litigation. (CX1005 at 1).

Rambus's Response to Finding No. 1718:

This proposed finding is not supported by the evidence. The cited evidence does not reflect any concern at the company, but rather one employee's belief. Further, Joel Karp, the employee primarily responsible for implementing the document retention policy, testified unequivocally that he did not believe there was a growing concern within Rambus about employee retention of e-mail. (CX 2102 at 346 (Karp Dep. (8/7/01)). Moreover, as the totality of the evidence makes clear, the "worry" – if there was one -- was that Rambus might be subpoenaed in connection with litigation in which it was not a party, not that Rambus itself might be a party to any specific case or type of litigation. (*See* CX 2112 at 159-161 (Karp Dep.)). As Mr. Karp testified:

> "Q Was this slide prepared contemporaneous with the prior document which has a date of July 22nd, 1998?
>
> A Yes.
>
> Q Okay. Taking that then as a given, at that point in time, July 22nd, 1998, was Rambus anticipating potential litigation?
>
> A No."

(*Id*. at 161-62).

1719. In April 1998, Rambus planned to purchase several high volume shredders. (CX1744A at 92 ("Buy shredders for all floors."); CX2114 at 134-35, 123-124 (Karp, Dep.) ("the idea was to put shredders at more convenient locations")).

Rambus's Response to Finding No. 1719:

This proposed finding is incomplete and misleading. The cited evidence makes clear that as the result of a security audit, Rambus determined that it should purchase shredders in order to prevent non-Rambus employees from obtaining confidential Rambus information and/or company trade secrets from documents that could be recovered from Rambus's trash dumpsters. (CX 2114 at 124, 135 (Karp Depo.)).

Complaint Counsel have frequently insinuated that shredders are an inappropriate device to use when destroying confidential material. They have cited no authority for that proposition. Numerous state and federal regulations, for example, have long *required* destruction of confidential business information "by a paper shredder, burning, or other approved method." Department of Agriculture Animal and Plant Health Inspection Service, Policy Statement on the Protection of Privileged or Confidential Business Information, 50 Fed. Reg. 38561 (Sept. 23, 1985). Other companies involved in this case also have regular document retention/document destruction programs. (*See, e.g.*, RX 1724 at 1 (Micron Records Retention Schedule); RX 1102 at 1 (Micron Electronic Records Retention Policy; Chen 1/16/03 Depo. Tr., 81-82 (Mitsubishi policy to "recycle" e-mails after 6 months)). Complaint Counsel have not suggested that any of these companies – or any other company whose records were subpoenaed – were able to produce in discovery as voluminous and complete a record of the relevant years at JEDEC as Rambus has done.

1720. Rambus executives decided to destroy emails archived on the company's backup

system after three months. (CX1744A at 94 ("3 months might be ok"); CX1744A at 104 (May 1998 management staff meeting: "Backups kept for three months); CX2114 at 136-39 (Karp, Dep.) ("the backups would be kept three months")).

Rambus's Response to Finding No. 1720:

This proposed finding is not supported by the evidence. The cited evidence does not refer to destroying anything. Rather, it reflects Rambus's decision to adequately protect itself against the loss of valuable emails in the event of a computer crash by backing up emails on the Company's email server(s). (CX 2114 at 136 (Karp Depo.)). Specifically, Rambus implemented a program such that if and when its computer system crashed, it would be able to restore the previous three months' emails from its email archives. (*Id*.) This program had no effect on the ability of employees to maintain their own email archives for whatever time period they desired. In fact, employees were told to maintain their own archives if they wanted to maintain email files for longer than three months. (*Id*.; *see also* CX1031 (email from Joel Karp informing employees "you can no longer depend on the full system backups for archival purposes. Any valuable data, engineering or otherwise, must be archived separately")); CX 2102 at 343-344 (Karp *Micron* Depo)).

Rambus's JEDEC representative testified that he preserved his JEDEC-related emails pursuant to the document retention policy. (Crisp, Tr. 3576). He also testified that he had gone out of his way to preserve those e-mails, through two computer system changes, even though it meant that he had to use his home computer equipment. (Crisp, Tr. 3572-3). Moreover, after patent litigation commenced, he located his JEDEC-related e-mails in his home computer, and turned them over to Rambus's general counsel. (Crisp, Tr. 3574).

1721. Rambus did not preserve emails from the early 1990's that were stored on

macintosh backup tapes. (CX2114 at 139-140 (Karp, Dep.) ("those were the first tapes that were destroyed")).

Rambus's Response to Finding No. 1721:

This proposed finding is incomplete and misleading. Any Macintosh files Rambus did not retain in its company archives were "useless" because "Rambus didn't have any way to read the things." (CX2114 at 140 (Karp, Dep.)). The evidence also makes clear that Rambus's primary JEDEC representative during the early 1990s, Richard Crisp, had previously converted his Macintosh files containing his JEDEC-related materials to IBM PC files in order to retain them. (Crisp, Tr. 3572-4; 3588-90). *See* RRFF 1720.

1722. Rambus CEO Geoffrey Tate and Mr. Karp had a one-on-one meeting at which they discussed reviewing pre-June 1996 backup tapes. (CX1744A at 136 ("Review backup tapes for pre-June 1996, Check for files"); CX2114 at 144-145 (Karp, Dep.)).

Rambus's Response to Finding No. 1722:

This proposed finding is not supported by the evidence. The cited evidence provides no support that Messrs. Tate and Karp discussed reviewing any tapes. Rather, the cited testimony makes clear that Mr. Karp used the term "review" in the sense of "search for." (CX2114 at 144-45 (Karp Dep.)). Mr. Karp explained that his notes referred to a search he conducted to find a specific back up tape for the pre-June '96 time frame. (*Id.*). This proposed finding also omits relevant evidence. Mr. Karp explained that the only significance to the June 1996 date was that it related to the conception dates of some of the work that was done for Direct Rambus. (*Id*.) The June 1996 date had nothing to do with JEDEC. (*Id*. at 145).

1723. On May 14, 1998, Mr. Karp sent an e-mail to all Rambus engineers and senior managers regarding "Backup Strategy/Document Retention Policy." (CX1031 at 1). He informed them that "[e]very Rambus employee will be involved" in Rambus's document retention policy. (*Id.*) Karp announced that he expected to have "a company meeting in early

June to kick off the program." (*Id.*) He invited questions in face-to-face discussions, but preferred that senders of any emails "keep the distribution narrow." (*Id.*)

Rambus's Response to Finding No. 1723:

The proposed finding omits relevant evidence. The idea of establishing a document retention policy initiated with Rambus's outside counsel from the Cooley Godward firm. (CX 2102 at 329 (Karp Depo.); (CX 2114 at 141-42 (Karp Depo.)).

1724. In June 1998, Mr. Karp was finalizing Rambus's document retention policy and preparing slides to explain the policy to Rambus employees. (CX1744A at 122 ("Doc retention teaching slide next week"); CX2114 at 140-141 (Karp, Dep.) ("we were finalizing the document retention policy . . . I was working on a set of slides that were going to be used as part of the meetings that would be held.")).

Rambus's Response to Finding No. 1724:

The proposed finding omits relevant evidence. The idea of establishing a document retention policy initiated with Rambus's outside counsel from the Cooley Godward law firm. (CX 2102 at 329 (Karp Depo.); *see* CX 2114 at 141-142 (Karp Depo.)). Mr. Karp prepared a policy that was based on the sample policies he had received from the Cooley Godward lawyers. (CX 2102 at 342).

1725. In June 1998, Mr. Karp outlined a plan to implement Rambus's document retention policy. (CX1744A at 126 ("Exec approval of doc. ret. policy, Presentation of details to exec, Presentation to managers and key individuals with outside counsel, Presentation to staff via division meetings, Implementation mid-August"); CX2114 at 141-142 (Karp, Dep.)).

Rambus's Response to Finding No. 1725:

See Rambus's RRFF 1723-24.

1726. Rambus CEO Geoffrey Tate made the final decision to implement the document retention policy at Rambus. (CX2102 at 362 (Karp, Dep.))

Rambus's Response to Finding No. 1726:

This proposed finding is not supported by the evidence it cites. Mr. Karp merely "believed" that Mr. Tate had approved the policy, but he had no specific recollection of such an occurrence. (CX 2102 at 362 (Karp Depo.)).

1727. In July 1998, Karp disseminated Rambus's two-page written document retention policy to all Rambus employees. (CX1040 at 1-2; Diepenbrock, Tr. 6230; CX2114 at 155-56 (Karp, Dep.)).

Rambus's Response to Finding No. 1727:

Rambus has no specific response.

1728. Rambus provided inadequate guidance to its employees as to what documents should be retained and which documents could be purged as part of its corporate document retention program. (February 26, 2003 Order on Complaint Counsel's Motions for Default Judgment and for Oral Argument at 9; CX1040 at 1-2 (policy itself provided little guidance to employees).

Rambus's Response to Finding No. 1728:

This proposed finding is irrelevant and contradicted by the weight of the evidence. Rambus, provided, both in writing and orally at staff meetings, a significant amount of information to its employees regarding the importance of retaining documents. Rambus's document retention policy was provided to all employees in writing and specifically instructed employees to retain various categories of documents. (CX 1040). Those document retention instructions were summarized in slides that Mr. Karp used when he delivered presentations to staff. The slides Mr. Karp presented to all Rambus employees specifically instructed Rambus employees, in bold-faced type, "LOOK FOR THINGS TO KEEP" and "LOOK FOR REASONS TO KEEP IT." (CX 1264 at 4, 7). The slides also provided specific guidance regarding the importance of retaining various kinds of documents, including documents related

to: (1) Intellectual Property ("All Documents Designated As Containing Trade Secret Information Should Be Kept For The Life Of The Trade Secret") (CX 1264 at 5-6); (2) Human Resources ("Most Personnel Records Must Be Kept For 3 Years.") (CX 1264 at 2); (3) Tax/Legal ("Audit Period Is 3 Years," "Inside Counsel Subject To Same Document Retention Policy As Rest of Company") (CX 1264 at 3); (4) Engineering ("LOOK FOR REASONS TO KEEP IT") (CX 1264 at 7); (5) Marketing and Sales ("Generally Kept for 3 Years", "LOOK FOR THINGS TO KEEP") (CX 1264 at 8); and (6) Contracts (If You Feel That A Particular Document Would Aid You In Refreshing Your Recollection – Keep It", "LOOK FOR THINGS TO KEEP") (CX 1264 at 10).

Moreover, Complaint Counsel have conceded that they have not suffered any prejudice as a result of any documents that were not retained by Rambus. Complaint Counsel have not pointed to any particular document or category of documents that they believe were deliberately destroyed. They are as aware as anyone that Mr. Crisp's JEDEC-related e-mails were, in fact, preserved and have, in fact, been introduced as evidence. In fact, Complaint Counsel acknowledged in their opening statement that in light of the massive amount of discovery, including privileged documents, that Rambus and its counsel have produced, they "have an unusual degree of visibility into the precise nature of Rambus' conduct, as well as the underlying motivations for what Rambus did." (Opening Statement, Tr. at 15).

1729. Rambus's corporate document retention program specifically failed to direct its employees to retain documents that could be relevant to any foreseeable litigation. (February 26, 2003, Order on Complaint Counsel's Motions for Default Judgment and for Oral Argument at 9; CX1040 at 1-2; CX1264 at 1; CX2102 at 354 (Karp, Dep.) (Mr. Karp did not recall anyone at Rambus saying documents should be retained because they might be relevant to some future litigation.)).

Rambus's Response to Finding No. 1729:

This proposed finding is not supported by the evidence. The document retention policy, by its nature, recognized the possibility of future disputes and instructed employees to keep documents that would foreseeably be relevant to those potential disputes. For example, employees were specifically instructed employees to keep (1) documents demonstrating that Rambus is entitled to trade secret protection (CX 1264 at 5); (2) documents demonstrating proof of invention dates (CX 1264 at 5); and (3) documents that would aid in refreshing recollection regarding contracts (CX 1264 at 10). Rambus also specifically instructed its employees to maintain their own e-mail archives. (CX 2114 at 136 (Karp Depo.), CX 1031 (e-mail from Joel Karp informing employees "you can no longer depend on the full system backups for archival purposes. Any valuable data, engineering or otherwise, must be archived separately")); CX 2102 at 343-345 (Karp Micron Depo). It is undisputed that the e-mail files of Rambus's JEDEC representative Richard Crisp were archived and produced in discovery. (Crisp, Tr. 3572-76).

1730. Rambus's corporate document retention program specifically failed to require employees to create and maintain a log of the documents purged pursuant to the program. (February 26, 2003, Order on Complaint Counsel's Motions for Default Judgment and for Oral Argument at 9; CX1040 at 1-2; CX2102 at 371 (Karp, Dep.) (Mr. Karp did not recall Rambus keeping any inventory of the items that were destroyed)).

Rambus's Response to Finding No. 1730:

This finding is irrelevant to this case. Moreover, there is no requirement, legal or otherwise, for a corporation to keep a log of documents that are not retained, and the other policies in the record contain no such instruction to employees. (RX 1102; RX 1724).

1731. After distributing the written policy, Karp and an attorney from Cooley Godward

held a meeting with all Rambus employees to "kick off" the document retention policy. (Diepenbrock, Tr. 6230; Crisp, Tr. 3419; CX2102 at 361-62 (Karp, Dep.); CX2114 at 156 (Karp, Dep.)).

Rambus's Response to Finding No. 1731:

Rambus has no specific response.

1732. While explaining the document retention policy to Rambus employees, Mr. Karp told staff to destroy emails because they could be discoverable in litigation. (Diepenbrock, Tr. 6230-32; CX1264 at 1 ("EMAIL – THROW IT AWAY • Email Is Discoverable In Litigation Or Pursuant To A Subpoena • Elimination of email is an integral part of document control • In General, Email Messages Should Be Deleted As Soon As They Are Read"); CX2114 at 161 (Karp, Dep.) ("We know all e-mail is discoverable; there's no question about that. So the real question becomes what are you required to save and what should you not save.")).

Rambus's Response to Finding No. 1732:

This proposed finding is incomplete, misleading and not supported by the evidence. Mr. Karp presented a comprehensive policy, which included guidance as to what should be discarded and what should be kept. The weight of the evidence makes clear that the prevailing message to employees was that they should "LOOK FOR THINGS TO KEEP" and "LOOK FOR REASONS TO KEEP IT," and only to discard a document if there was *no* reason to keep it. (CX 1264 at 4, 7). E-mails were no different. The cited evidence merely points out that e-mails are considered "documents" pursuant to Rambus's document retention policy. Moreover, employees were instructed to maintain their own e-mail archives. (CX 2114 at 136 (Karp Depo.), CX 1031 (email from Joel Karp informing employees "you can no longer depend on the full system backups for archival purposes. Any valuable data, engineering or otherwise, must be archived separately")); CX 2102 at 343-345 (Karp Micron Depo). Indeed, in this case, e-mails relating to JEDEC *were* archived by Richard Crisp. (Crisp, Tr. 3572-76). And as Mr. Karp testified, Rambus was *not* anticipating litigation at the time:

"Q Was this slide prepared contemporaneous with the prior document which has a date of July 22nd, 1998?

A Yes.

Q Okay. Taking that then as a given, at that point in time, July 22nd, 1998, was Rambus anticipating potential litigation?

A No."

(CX 2114, Karp FTC Dep., 161-62).

1733. Rambus's former in-house counsel Anthony Diepenbrock was told that Rambus did not want to keep documents around because they were "[d]iscoverable in a lawsuit." (Diepenbrock, Tr. 6234-35 ("Q. And when you say you were told Rambus didn't want to keep these documents around because they were discoverable, when you say 'discoverable,' you are talking about in a subsequent litigation like we are in right here, right? . . . A. Discoverable in a lawsuit, right")).

Rambus's Response to Finding No. 1733:

This proposed finding is not supported by the evidence. Mr. Diepenbrock did not testify that the motivation for Rambus's document retention policy was to avoid discovery in a lawsuit. Mr. Diepenbrock simply agreed that "generally" he understood the word discoverable to mean discoverable in a "lawsuit." (Diepenbrock, Tr. 6234-35). There is no indication whatsoever that Mr. Diepenbrock understood the hypothetical "lawsuit" referred to a particular type of lawsuit or a lawsuit in which Rambus was a party – as opposed to a lawsuit where Rambus received a third-party subpoena. (*See e.g.*, CX1264). Moreover, the idea of establishing a document retention policy initiated with Rambus's outside counsel from the Cooley Godward firm. (CX 2102 at 329 (Karp Dep.)); *see* CX 2114 at 141-42 (Karp Dep.)).

1734. In the weeks following the initial meeting, Karp held several training sessions regarding the document retention plan. (CX2102 at 361 (Karp, Dep.)).

Rambus's Response to Finding No. 1734:

Rambus has no specific response.

1735. Mr. Karp explained Rambus's document retention policy to all Rambus employees. (CX2102 at 367 (Karp, Dep.)).

Rambus's Response to Finding No. 1735:

Rambus has no specific response.

1736. From 1998 through 2000, Rambus employees destroyed massive amounts of material as part of Rambus's document retention policy. (CX1052 at 1; CX2114 at 165 (Karp, Dep.) ("Q. You testified previously there were a large number of documents discarded or purged or destroyed after this policy was implemented at Rambus? A. Yes."); CCFF 1737-40)).

Rambus's Response to Finding No. 1736:

This proposed finding is vague and ambiguous and is not supported by the evidence. There is no indication of what is meant by "massive," and there is no evidence that "massive" amounts of documents were destroyed. This proposed finding is irrelevant in any event, because there is no showing that the discarding of document pursuant to Rambus's document retention proper was improper or that Complaint Counsel was prejudiced by it. (Opening Statement, Tr. at 15 (statement by Mr. Royall that "we have an unusual degree of visibility into the precise nature of Rambus' conduct, as well as the underlying motivations for what Rambus did.")).

1737. As a result of directives from Mr. Karp, Mr. Diepenbrock, Rambus's in-house counsel, purged his documents and files in the summer on 1998. (Diepenbrock, Tr. 6235-36).

Rambus's Response to Finding No. 1737:

This proposed finding is not supported by the evidence. Mr. Diepenbrock explained his actions in response to Rambus's document retention policy as follows: "I removed some

documents from my work product files that were old, and in some cases I had questions about the retention policy, and I asked Mr. Karp, and documents were not removed if there was any reason to save them." (Diepenbrock, Tr. 6236). Moreover, Mr. Diepenbrock did not even arrive at Rambus until September 1995. (Diepenbrock, Tr. 6099).

1738. In response to Joel Karp's directives regarding the document retention policy, Richard Crisp, Rambus's primary JEDEC representative, cleaned out his files. (Crisp, Tr. 3425; CX2082 at 841-43 (Crisp, Dep.)). Because Crisp was leaving on a business trip to Asia, he did not have a lot of time to sort through all the material in his office. (Crisp, Tr. 3427). As a result, Crisp simply dumped most of the paper in his office, including JEDEC-related material and any paper documents regarding patent prosecution work, into a burlap bag to be shredded. (Crisp, Tr. 3427-30; CX2082 at 841-43 (Crisp, Dep.) ("anything that I had on paper, I basically threw away")).

Rambus's Response to Finding No. 1738:

This proposed finding is irrelevant because Complaint Counsel have conceded that they were not prejudiced. (Opening, Tr. at 15) ("("we have an unusual degree of visibility into the precise nature of Rambus' conduct, as well as the underlying motivations for what Rambus did.")

It is also misleading because it omits related evidence. The cited evidence makes clear that Mr. Crisp discarded most of the paper in his office "because most of the paper I had in my office were things I knew I didn't need to keep. Most of the things I needed to keep were electronic files that I had on my computer." (Crisp, Tr. 3428). Moreover, Mr. Crisp testified that he "gave a great deal of thought to what I needed to keep that was on my computer. The kinds of documents that I had been asked to keep were things that were in electronic form, and I made an attempt to preserve those documents, many of which we have been reviewing in this case." (*Id.*). The paper materials that were in his office and discarded were wholly irrelevant to

this action, such as brochures and duplicates of official publications. (*See id.* (describing the documents as "data books" and "brochures from marketing conferences")).

1739. In September 1998, Rambus celebrated a corporate-wide "Shred Day." (CX1044 at 1; CX1051 at 1 ("Thursday is Shred Day 1998 . . . Please leave your burlap bags in the hallway . . . We will have a Shred Day Celebration in the new 1st floor open area . . . If you have any questions regarding our Document Retention Policy, please see Joel [Karp]"); Crisp, Tr. 3422; CX2102 at 369-370 (Karp, Dep.) ("we had one day where we had kind of a spring cleaning . . . one of the many Valley shredding companies [came] in with their kind of industrial shredders")).

Rambus's Response to Finding No. 1739:

This proposed finding is misleading and omits significant testimony. Mr. Karp explained that the shred day was a "kind of spring cleaning" where "the idea was not destroying, the idea was, you know, culling out the things that needed to be kept, and then the stuff that did not need to be kept could be thrown away." (CX 2102 (Karp Depo. 8/7/01) at 369). As Mr. Karp explained, much of what he discarded consisted of "stacks of magazines" (CX 2144 (Karp FTC Depo.) at 165) and old "phone books." (CX 2102 (Karp Depo. 8/7/01) at 371).

This proposed finding is, in any event, irrelevant because Complaint Counsel have conceded that they were not prejudiced. (Opening Statement, Tr. at 15) ("("we have an unusual degree of visibility into the precise nature of Rambus' conduct, as well as the underlying motivations for what Rambus did.")

The finding is also misleading because it implies that there was something improper about shredding documents pursuant to Rambus's document retention policy. Companies, individuals and government agencies "purge," or to use a more neutral term, "clean," their files constantly. Complaint Counsel have failed to make any showing that Rambus was required to maintain any documents other than those that it *did* retain and *did* produce in discovery.

1740. In one day alone, in the space of five hours, Rambus destroyed as much as 20,000 pounds of business records. (CX2102 at 371 (Karp, Dep.) (Rambus delivered "a lot of stuff" to the shredding company; the "stuff [was] being basically piled pretty high on carts."); CX1052 at 1 (Karp September 1998 email: "Shred Day: Status Report . . . It took about 5 hours to completely fill the shredding truck (capacity is 20,000 lbs)")).

Rambus's Response to Finding No. 1740:

See CCFF 1739.

1741. Mr. Karp testified that he "did a little bit of spot checking" with Rambus employees and "sat and watched over their shoulder" to insure compliance with the document retention policy. (CX2102 at 360-61 (Karp, Micron Dep.))

Rambus's Response to Finding No. 1741:

Rambus has no specific response.

1742. In September 1998, Mr. Karp had a one-on-one meeting with Rambus CEO Geoffrey Tate during which Karp inquired whether Tate and other board members had cleaned out their files. (CX1744A at 141 ("Doc. Retent, Geoff files?, Board members?"); CX2114 at 146-47 (Karp, Dep.) ("Q. You were checking up on Mr. Tate? A. Yes")).

Rambus's Response to Finding No. 1742:

This proposed finding is not supported by the evidence. The cited testimony does not suggest that Rambus board members "cleaned out" their files. In fact, Rambus's chairman, Bill Davidow, testified that he has retained essentially all of the electronic communication he has ever received related to Rambus. (CX 2109 at 190, Davidow Depo.).

1743. Mr. Karp deleted all his Rambus-related files from his computer when he left Rambus in summer 2000. (CX2059 at 62 (Karp, Dep.); CX2102 at 378 (Karp, Dep.)).

Rambus's Response to Finding No. 1743:

This proposed finding is misleading and omits relevant information. Mr. Karp made a hard copy of his relevant computer files before he deleted them. (CX 2114 at 174 (Karp Depo). "What I did was I went through my files and anything that was at all relevant to anything I made

copies of. And I left that behind and then deleted the files from the computer." (CX 2102 at 378 (Karp Depo. 8/7/01)).

1744. From 1998 through 2000, Rambus's outside counsel destroyed massive amounts of material as part of Rambus's document retention policy. (CCFF 1745-48, 1752).

Rambus's Response to Finding No. 1744:

This proposed finding is vague as to the term "massive" and not supported by the evidence. Rambus incorporates by reference its responses to CCFF 1745-48, 1752.

1745. Rambus instructed Lester Vincent, an attorney with its outside patent law firm Blakely, Sokoloff, Taylor & Zafman, to destroy Rambus-related files. (CX3129 at 530 (Vincent, Dep.) ("[Karp] discussed the Rambus document retention policy that he wanted me to implement."); CX3126 at 410 (Vincent, Dep.); CX2114 at 182-83 (Karp, Dep.)).

Rambus's Response to Finding No. 1745:

This proposed finding is irrelevant because Complaint Counsel have conceded that they were not prejudiced by Mr. Vincent's failure to retain all of his Rambus-related documents. (Opening Statement, Tr. 15) ("we have an unusual degree of visibility into the precise nature of Rambus' conduct, as well as the underlying motivations for what Rambus did."). It is also misleading because it omits related information. Joel Karp asked Lester Vincent to comply with Rambus's document retention policy, which specifically called for the *retention* of certain types of documents. The only documents Mr. Vincent did not retain were portions of internal patent prosecution files related to issued Rambus patents. (CX 3129 at 530 (Vincent Depo.)). From those same files, Mr. Vincent retained "communications to and from the patent office," "any conception of [sic] reduction to practice documents," documents related to "maintenance fees," and "copies of prior art." (*Id*. at 530). Mr. Vincent also retained his Rambus general files. (CX3126 at 419). Mr. Vincent did not discard any documents related to either: (1) legal

advice [he] provided to Rambus about the disclosures of patents and patent applications to JEDEC; or (2) the disclosure policy of JEDEC. (CX 3126 at 416 (Vincent Depo.)).

1746. At Rambus's request, Mr. Vincent destroyed a variety of documents from the left hand side of his files, including various "prosecution documents" such as "patent prosecution files for issued patents . . . claiming priority to the 1990 Farmwald, Horowitz application." (CX3126 at 408 (Vincent, Dep.); CX3129 at 530-33, 536, 539-40 (Vincent, Dep.)).

Rambus's Response to Finding No. 1746:

This proposed finding is irrelevant because Complaint Counsel have made no showing that any of the documents discarded by Mr. Vincent were required to be retained or that Mr. Vincent's compliance with Rambus's document retention policy was improper. (*See* RRFF 1745).

1747. Mr. Vincent also destroyed various "drafts, handwritten notes, letters or faxes, and maybe drawings," including correspondence from Rambus to Blakely, Sokoloff and vice versa, Vincent's own handwritten notes and those of other lawyers from his firm, drafts of patent applications and amendments, draft handwritten drawings or informal drawings, electronic versions of such documents, and audio tapes of meetings with inventors. (CX3129 at 531-533 (Vincent, Dep.); CX3126 at 425-26 (Vincent, Dep.) ("drafts or handwritten notes or correspondence in the file . . . would be destroyed.")).

Rambus's Response to Finding No. 1747:

See RRFF 1745-46.

1748. Some of the copies Mr. Vincent destroyed were the "only documents in existence." (CX3129 at 539-40 (Vincent, Dep.)).

Rambus's Response to Finding No. 1748:

This finding is irrelevant because Complaint Counsel do not contend that the documents in question were relevant to this matter. *See* RRFF 1745-46.

1749. Mr. Vincent carried out the document destruction at various points in time, beginning several months after the initial instructions he received from Rambus in 1997 and early 1998. (CX3126 at 418, 422 (Vincent, Dep.)).

Rambus's Response to Finding No. 1749:

This finding is irrelevant because Complaint Counsel have conceded that they were not prejudiced by Mr. Vincent's failure to retain some of his Rambus-related documents. (Opening, Tr. at 15) ("we have an unusual degree of visibility into the precise nature of Rambus' conduct, as well as the underlying motivations for what Rambus did."). This proposed finding is also vague and ambiguous. Mr. Vincent testified that after receiving instructions from Rambus in 1997 or 1998, he implemented Rambus's document retention policy. (CX 3126, Vincent Dep. Tr., 422). Mr. Vincent retained all Rambus related documents once Rambus filed suit against Hitachi. (*Id.*). After the Hitachi lawsuit ended, some copies of documents Mr. Vincent had previously provided to Rambus's counsel in connection with the Hitachi were discarded. (*Id.* at 424). *See also* RRFF 1745-48**.**

1750. Mr. Vincent briefly suspended the document destruction after Rambus filed a lawsuit against Hitachi in 2000. (CX3129 at 534-535 (Vincent, Dep.)).

Rambus's Response to Finding No. 1750:

See RRFF 1749.

1751. Rambus President David Mooring and Mr. Karp did not recall any changes to the Rambus document retention policy once the Hitachi litigation commenced. (CX2112 at 290-92 (Mooring, Dep.); CX2114 at 163 (Karp, Dep.)).

Rambus's Response to Finding No. 1751:

This proposed finding is not supported by the evidence. Mr. Mooring did not recall anything "in writing that went out," but did recall receiving a "a couple of notices over the last few years saying anywhere from save everything on certain subjects to a request to save everything." (CX2112 at 290-93 (Mooring, Dep.)). According to Joel Karp, "once we filed a

lawsuit I believe people were told to freeze everything at that point." (CX 2114 at 164 (Karp FTC Depo.). By "freeze," Mr. Karp understood that "once the litigation started, there was going to be discovery, and we wanted to make sure we could capture anything that was there at that time." (*Id.*).

1752. After the hiatus in document destruction during the pendency of the Hitachi litigation, Vincent's law firm recommenced destroying documents. (CX3129 at 535 (Vincent, Dep.)). This wave of document destruction continued at least until Rambus filed the Infineon suit in August 2000. (CX3126 at 424 (Vincent, Dep.)); CX1329 at 542 (Vincent, Dep.)).

Rambus's Response to Finding No. 1752:

This proposed finding omits relevant information. The only documents the Blakely firm discarded after the Hitachi lawsuit ended were *copies* of documents that already had been provided to counsel in connection with the Hitachi case. (CX 3126 at 420 (Vincent Depo.).

1753. CX0711 is a 199-page collection of emails authored by Richard Crisp that were preserved on Rambus's main server when Crisp transferred the messages from one laptop computer to another via the server. (Crisp, Tr. 3587-91). Crisp later deleted many of his emails, but "forgot about the directory." (Crisp, Tr. 3589-3591). Still, not all of Crisp's e-mails survived. (Crisp, Tr. 3572-73 ("unfortunately, not all of those files could go over the network because of funny characters in the names")).

Rambus's Response to Finding No. 1753:

This proposed finding is contradicted by the evidence. There is no support for the claim that Mr. Crisp "later deleted many of his emails." As the finding suggests, CX 0711 contains a large collection of e-mails that Mr. Crisp *chose* to save from loss during a computer system change. (Crisp, Tr. 3572-76; 3588-96). In order to transfer these emails from his Macintosh to his P.C., Mr. Crisp uploaded (i.e., copied) them to Rambus's server from the Macintosh and then downloaded (i.e., copied) them to the P.C. Therefore, whether he "forgot" that he had left a duplicate copy on the server is wholly irrelevant. The documents were intentionally preserved,

were produced in discovery, and were admitted into evidence. (Crisp, Tr. 3572-76, 3588-92).

1754. Rambus's principal JEDEC representative, Richard Crisp, later joked about DDR SDRAM-related documents "fall[ing] victim to the document retention policy." (CX1079 at 1 (Crisp October 1999 email: "I'm looking for a copy (paper or electronic) of one of the original DDR datasheets from the 1996/1997 timeframe. Hopefully someone here has one that hasn't fallen victim to the document retention policy :-)"); Crisp, Tr. 3431).

Rambus's Response to Finding No. 1754:

This proposed finding is irrelevant, vague and ambiguous.

1755. Rambus knew or should have known from its participation in JEDEC that litigation over the enforcement of its patents was reasonably foreseeable. (February 26, 2003 Order on Complaint Counsel's Motions for Default Judgment and for Oral Argument at 9; CX3051 at 1-26 (in December 1995, Rambus's attorneys received a fax of the FTC's proposed consent agreement in Dell, a case regarding anticompetitive unilateral conduct occurring within the context of a standards setting organization); Rambus Answer at 34, ¶ 81 (Rambus attorneys discussed the Commission's proposed consent order in Dell and "in January 1996 one or more attorneys for Rambus advised Rambus that it should no longer participate in any standards bodies")).

Rambus's Response to Finding No. 1755:

This proposed finding is contradicted by the evidence. Rambus had no reason to believe that its participation in JEDEC would result in litigation because Rambus did not believe (and still does not believe) that it had violated any JEDEC rules. Joel Karp's testimony on this point is illustrative. It "never" occurred to Mr. Karp that "there might be [an] issue if Rambus went after SDRAM or DDR SDRAM products" because he "never saw Rambus do anything that would have -- that was even close to getting into where there would be a problem. I knew exactly what Rambus was doing. . . . I just don't -- I just couldn't connect Rambus in any way with the issues that surfaced in the TI case or in the Wang case." (CX 2102 at 314-316 (Karp Depo. 8/7/01)). In addition, Complaint Counsel have stipulated that Rambus had no patents that were essential to the manufacture or use of any device manufactured to a JEDEC specification

prior to January 1996. (The Parties' First Set of Stipulations, Stipulation 10). Moreover, Rambus has not asserted any patent against a JEDEC-compliant device that issued prior to June 22, 1999 (*id*., ex. A, Patent Tree), and Rambus did not know while it was a JEDEC member that it would in fact get patent claims that covered the four features in question. RPF 417-31. The record evidence makes plain that Rambus did not anticipate litigation over its patents until 1999. RRFF 1729. Until that time, Rambus expected that the companies with whom it was negotiating would agree, as many did agree, to negotiate license agreements with Rambus on terms that Rambus viewed as fair and reasonable. It was only after Hitachi refused to take a license and then later, after Micron even refused to negotiate, that it became apparent that litigation would be necessary to enforce Rambus's patents.

1756. Rambus, at the time it implemented its document retention policy, clearly contemplated that it might be bringing patent infringement suits if its efforts to persuade semiconductor manufacturers to license its JEDEC-related patents were not successful. (February 26, 2003 Order Granting Complaint Counsel's Motion for Collateral Estoppel at 5; CX0613 at 2 (Mr. Karp attended a Rambus Board meeting in March 1998 to "update[] the Directors on the Company's strategic licensing and litigation strategy"); CX2109 at 163-164 (Davidow, Dep.); CX1804 at 23 (Rambus's privilege log withholds a March 1998 memorandum entitled "Rambus Strategic Patent Litigation" and describes two additional documents from the same time period as "Confidential attorney-client communications regarding legal strategy and reflecting work in anticipation of litigation."); CX2102 at 419 (Karp, Dep.); CX1032 at 1 (in May 1998, Rambus executive Allen Roberts commented on the "fun times if/when we enforce our IP on DDR."); CX1778 at 16 (Rambus 1998 Annual Report: "Litigation may be necessary in the future to enforce the Company's patents and other intellectual property rights")).

Rambus's Response to Finding No. 1756:

This proposed finding is not supported by the evidence. The weight of the evidence shows that Rambus did not anticipate any *specific* litigation at the time it implemented its document retention policy. (CX 2114, Karp Dep. Tr., 161-62). As a company dependent upon licensing its intellectual property, Rambus recognized that litigation involving those licenses

and/or its patent rights was a possibility. The patents that Rambus has asserted against JEDEC-compliant products did not issue until June 1999. (Parties' First Set of Stipulations, ex. A, Patent Tree). It was not until the time when Hitachi first refused to take a license from Rambus for SDRAM and DDR SDRAM in the fall of 1999 that Rambus had any specific anticipation of litigation, *i.e.*, against Hitachi, involving its SDRAM and DDR SDRAM patents. (CX2114 at 162-63 (Karp Depo.)). Complaint Counsel's allegations regarding Rambus's document destruction pertain only to materials they contend it should have retained for litigation involving its SDRAM and DDR SDRAM patents. As explained, no anticipation of any such litigation arose until 1999.

1757. Rambus's document destruction was done in anticipation of litigation. (February 26, 2003 Order Granting Complaint Counsel's Motion for Collateral Estoppel at 5; CCFF 1756).

Rambus's Response to Finding No. 1757:

This proposed finding is not supported by the evidence. *See* RRFF 1755-56.

1758. When Rambus instituted its document retention policy in 1998, it did so, in part, for the purpose of getting rid of documents that might be harmful in litigation. (February 26, 2003 Order Granting Complaint Counsel's Motion for Collateral Estoppel at 5; CCFF 1718, 1732-33).

Rambus's Response to Finding No. 1758:

This proposed finding is not supported by the evidence. See RRFF 1718, 1732-33, 1736-38, 1742-43, 1745, 1753, 1755-56.

1759. Paragraphs 1759-1799 are unused.

IX. High Royalty Rates, High Manufacturing Costs and Technical Problems Led to the Decline of the Rambus RDRAM Architecture.

A. DRAM Manufacturers Designed and Prepared to Manufacture Several Memory Architectures, Including RDRAM.

1800. Throughout the 1996-1999 timeframe, most DRAM manufacturers supported three future generation architectures: Direct RDRAM, SyncLink, and DDR SDRAM. (CX3110 at 1 ("RDRAM is just one product in our diverse DRAM family"); CX2716 at 1 ("At Micron, we will promote all three future memory technologies – DDR, SLDRAM, and DRDRAM"); CCFF 1575, 1802-11, 2509).

Rambus's Response to Finding No. 1800:

This finding is not supported by the evidence presented at trial. Rambus previously responded to this same finding in detail at RRFF 1575; that discussion will not be repeated here. *See also* RPF 1548-1602.

1801. The DRAM industry was developing different memory architectures for different market segments. Companies planned to use RDRAM as main memory in mid-range and high end personal computers; DDR as main memory in servers and for graphic applications; and SyncLink as the possible next generation main memory in PC's. (CX2718 at 45; Lee, Tr. 6727-28; CX2297 at 3, 81; Tabrizi, Tr. 9149-9151, 9155-56).

Rambus's Response to Finding No. 1801:

This finding relies solely on documents and testimony from Micron and Hynix and must necessarily be limited to them. The finding is also ambiguous as to which time period it describes. *See also* RRFF 1575 and RPF 1548-1602.

1802. After Intel announced its support for Rambus in late 1996, Hyundai devoted many resources to developing RDRAM and had a "minimum of 50 engineers working on Rambus project[s]." (Tabrizi, Tr. 9136-37 ("Rambus was a fully multilevel project within [Hyundai]. We had at least two or three project and engineering team[s] working on various Rambus project[s]")).

Rambus's Response to Finding No. 1802:

Complaint Counsel cite only to Mr. Tabrizi's trial testimony in support of this finding.

Mr. Tabrizi is not a reliable or credible basis for any finding about Hyundai's purported efforts to produce RDRAM. Not only does he lack foundation for the testimony, since he was based in the U.S. in the marketing department, and the purported activity was ongoing in South Korea in the engineering area, but Mr. Tabrizi's contemporaneous documents show him trying at every turn to *prevent* RDRAM from achieving marketplace success:

- RX 778 at 1 – Tabrizi's 9/96 e-mail to other DRAM manufacturers: "I urge you to please educate others and get their agreement to say 'NO TO RAMBUS AND NO TO INTEL DOMINATION;'"
- RX 808 at 2 – Tabrizi urges other manufacturers at a 12/96 SyncLink Consortium meeting to join in a "united strategy" to resist Intel's choice of Rambus;
- RX 802 at 3 – Tabrizi 12/96 e-mail to other manufacturers asking them to "stick together" in order to avoid "the path of control and domination by Intel;"
- RX 849 at 44 – Tabrizi warns other manufacturer executives at 1/97 Tokyo meeting that if Rambus is the next generation memory device, "DRAM manufacturers would loose control of specification and the gross margins will decline;"
- RX 1280, 1293A, 1295 – Hyundai documents showing that in the fall of 1998, at Tabrizi's recommendation, Hyundai provided inflated RDRAM production and pricing forecasts to Intel;
- RX 2192 at 1, 2 – Infineon trip report from the fall of 1998 quoting Tabrizi as saying that he had indeed given Intel inflated price and production estimates, and

that he "encourage[d] every DRAM manufacturer to do the same," in order to keep the RDRAM supply low;

- RX 1487 at 4 – Hyundai e-mails in July 1999, copied to Tabrizi, show a plan to "work with [Samsung] to limit the supply" of RDRAM in order to avoid "an oversupply;" and
- RX 1661 at 2 – Tabrizi's 6/00 e-mail to Hynix President Sang Park: "[i]f Intel does not invest in us, I really want to ask you to let me go back to my old mode of RDRAM killing."

It would not be appropriate to rely upon the testimony of the self-professed "RDRAM killer" as the sole support – or as any support – for a finding that Hyundai had "devoted many resources" to developing RDRAM. The finding should be rephrased to say that "after Intel announced its support for Rambus in late 1996, senior Hyundai personnel encouraged other DRAM manufacturers to work together in an effort to prevent the successful introduction of the RDRAM device."

1803. Hyundai decided to develop the 128Mb RDRAM product with the most advanced Hyundai technology. (CX2314A at 3 ("Direct RDRAM . . . Development without delay (0.18um Technology)"); Tabrizi, Tr. 9180-83 (".18 micron technology at the time of '98 was our most advanced technology")).

Rambus's Response to Finding No. 1803:

See RRFF 1802.

1804. Hyundai hoped to become a leading producer of RDRAM and assigned its best engineers to the next generation Rambus project. (RX1487 at 6; Tabrizi, Tr. 9114-15 (Hyundai "wanted to be one of the leaders in Rambus" so it assigned its "best engineers to develop the next-generation Rambus project.")).

Rambus's Response to Finding No. 1804:

As noted in RRFF 1802, Mr. Tabrizi lacks the foundation and the credibility to testify about Hyundai's efforts to develop an RDRAM device. Moreover, the only document cited in support of this finding – RX 1487 – contains language that is inconsistent, to say the least, with the proposed finding:

> "With Samsung building significant amounts of [RDRAM], we need to work with them to limit the supply in the market, otherwise we both will be competing for market share which will result in an oversupply. We have to meet with Samsung. . . ."

(RX 1487 at 4).

1805. After Hyundai and Lucky Goldstar merged in 1998, Hyundai planned to develop LG's more advanced RDRAM product. (Tabrizi, Tr. 9112-13; RX1487 at 6). Hyundai moved the best engineers from both companies to one location to facilitate work on its RDRAM device. (RX1487 at 6 ("Tabrizi July 1999 email: put "both companies best engineers to work on 256/288M RDRAM design by using next generation process"); Tabrizi, Tr. 9114-15 ("We wanted to put our best engineers together in one place")).

Rambus's Response to Finding No. 1805:

Neither the testimony nor the cited document supports the proposition that Hyundai ever put its "best engineers" to work on the RDRAM; both speak instead in terms of a *proposal*. Neither is consistent with Tabrizi's subsequent reference to his "old mode of RDRAM killing." (RX 1661 at 2).

1806. Hyundai prepared to deliver RDRAM to customers based on customer needs. (CX2303 at 7; Tabrizi, Tr. 9164-66 ("We were trying to align our road map with Dell['s] requirement in terms of Rambus")).

Rambus's Response to Finding No. 1806:

The evidence supports a finding that in 1998, Hyundai made various RDRAM production commitments to customers *that it then did not meet*. (RX 1302 at 6; Gross, Tr. 2327-29). According to Compaq's Ms. Gross, the DRAM manufacturers would not "increase their output at the rate at which we needed to support our systems." (Gross, Tr. 2345-46). In this same time period, an internal Hyundai e-mail that was copied to Tabrizi said that "we can *overstate* our Direct Rambus production so Intel can feel we are more aggressive on our ramp up." (RX 1295 at 1) (emphasis added).

1807. Compaq planned to transition to RDRAM because of Intel's roadmap. (Gross, Tr. 2318). Compaq also planned to introduce RDRAM throughout its product line. (Gross 2326-27).

Rambus's Response to Finding No. 1807:

Rambus has no specific response.

1808. After Micron signed a license for Direct RDRAM in 1997, Micron devoted many resources to developing RDRAM. (Appleton, Tr. 6354-6357) ("We started to do all those things you would do when you're developing a product"). Micron formed a large design team to work on RDRAM and offered the team cash incentives to meet certain milestones. (Appleton, Tr. 6355-56). Micron also purchased new testing equipment for RDRAM. (Appleton, Tr. 6357).

Rambus's Response to Finding No. 1808:

This finding depends entirely on the testimony of Micron CEO Steve Appleton, whose financial interests in the outcome of this matter are apparent, and who lacks foundation to testify about engineering matters such as efforts to acquire test equipment.

More credible evidence on Micron's position towards RDRAM is found in an April 1999 e-mail discussion among Micron Vice President Bob Donnelly, Micron DRAM

Marketing Manager Jeff Mailloux, and Micron JEDEC representatives Kevin Ryan and Terry Lee. Mr. Ryan started the exchange with an e-mail attaching an article describing Samsung's plans to produce as much as 40 million Rambus devices in 1999. (RX 1444 at 3). Mr. Ryan complained that Samsung had "broken ranks with the other suppliers" and had "sold their soul to the devil." (RX 1444 at 1). One of the recipients of the e-mail, Mike Seibert, responded that "[t]hese guys are big trouble for us all. *If this thing gets into an oversupply mode with RDRAM things could get really ugly*." (RX 1444 at 1) (emphasis added). Mr. Seibert then asked Micron Vice-President Bob Donnelly if *Samsung* understood "what the Rambus/Intel biz model will do to our autonomy?" (*Id.*). Vice-President Donnelly responded that he had "certainly made the point with the officers that Intel . . . ultimately could control the DRAM industry." (*Id.*).

By the following year, Micron's senior management was bragging that Micron was "largely" responsible for RDRAM's failure to become the dominant mainstream memory device. (RX 1700 at 1). In an e-mail sent to all Micron sales and marketing personnel in September 2000, Micron Vice President of Sales Mike Sadler listed the company's "accomplishments" in a "spectacular quarter." (*Id.*). Among Micron's accomplishments:

> "Finally, *thanks largely to Micron's efforts*, established PC 133 and DDR as mainstream memory solutions for the PC industry in favor of another proposed solution, RDRAM."

(*Id.*) (emphasis added).

These documents directly contradict the proposed finding and show that instead of Micron "devot[ing] many resources to *developing* RDRAM," it was devoting many resources to *blocking* RDRAM. (See also RX 1453 at 1 – Intel e-mail from May 1999 revealing that

"technically, [Micron is] well behind" on RDRAM development and has "ignored our attempts to work with them on enabling"; RX 1515 at 2 – Intel e-mail from October 1999 stating that "we have gotten nothing but deception" from Micron and that "Micron is working very hard to do everything against RDRAM").

By September 2001, Micron Vice-President Sadler {

}

(RX 1883 at 1) (*in camera*).

In light of these and other contemporaneous Micron documents (*see, e.g.*, RX 1155 at 1, where Mr. Mailloux refers to Rambus as "the dark side"), Mr. Appleton's attempts to describe his company's purported efforts to develop RDRAM are neither credible nor persuasive. The proposed finding is clearly contrary to the weight of the evidence.

1809. In 1998 and 1999, Micron included RDRAM on its DRAM product road map. (CX2718 at 26; Lee, Tr. 6722-23; CX2742 at 8-11). In September 1999, Micron's packaging for RDRAM was nearly complete. (CX2747 at 66 ("RDRAM Product Status . . . Packaging . . .16-chip RIMM layout is nearly complete for FBGA package")).

Rambus's Response to Finding No. 1809:

A more accurate finding regarding Micron's approach to the DRAM "roadmap" would state that in October 1998, Micron proposed to other DRAM manufacturers that they agree to a "common roadmap" that the manufacturers would then provide to chipset companies and PC OEMs. (RX 2191 at 1; RX 2192 at 3). Such a "roadmap" would be "'signed' by all or most of the DRAM companies" and would show a joint commitment by the manufacturers to support DDR or SLDRAM instead of RDRAM. (*Id.*). The "main target" of such a joint roadmap would be to remove the "current uncertainty about the supply situation" among the chipset companies and PC OEMs. (RX 2191 at 1). A proposed joint roadmap was later circulated to numerous DRAM manufacturers by Micron. (RX 1423 at 1-2).

This and other contemporaneous internal Micron documents belie the notion that it was promoting RDRAM to customers or working to ramp up its production. The evidence instead shows that Micron was "working very hard to do everything against RDRAM" (RX 1515 at 2), and that its senior managers took credit in internal e-mails for RDRAM's failure to obtain marketplace success. *See* RRFF 1808 and evidence cited therein.

1810. In the 1999 timeframe, Micron moved to a higher density RDRAM part based on customer feedback and a "general migration of customers to higher density systems." (Lee, Tr. 6744-46; CX2735 at 29 ("Decided not to develop the 64Mb/72Mb • Density did not meet customer requirements")). The higher density parts also had "manufacturing cost advantages." (Lee, Tr. 6745-47; CX2735 at 30 ("Lower relative cost" per bit)).

Rambus's Response to Finding No. 1810:

The proposed finding is irrelevant and is contrary to the weight of the evidence. *See* RRFF 1808-09, 1811-13.

1811. In April 1999, Micron completed its higher density 144Mb Rambus design and

"taped out" the part, meaning Micron "sen[t] it off for fabrication." (CX2735 at 24; CX2735 at 29; Lee 6744-45). Micron expected to release its 144Mb samples in June 1999. (CX2735 at 31).

Rambus's Response to Finding No. 1811:

The proposed finding is both irrelevant and inaccurate. According to an Intel analysis of Micron's RDRAM performance as of May 1999, "[t]echnically, they are well behind." (RX 1453 at 1). As a result, Micron was unlikely to "ship anything at all in '99. Our contract is a minimum of 12Mu in '99, we expect almost nothing." (*Id.*).

1812. In June 1999, Micron issued a press release announcing its first shipment of RDRAM samples to Intel. (RX1464 at 1).

Rambus's Response to Finding No. 1812:

The proposed finding is irrelevant. Moreover, the trial record shows that regardless of its public statements, Micron was in 1999 "working very hard to do everything against RDRAM." (RX 1515 at 2). (*See also* RRFF 1808-1810 and evidence cited therein).

1813. In 1999, Micron promoted RDRAM through product presentations and advertisements. (Appleton, Tr. 6357; CX3110 at 1 (1999 Advertisement: "With its revolutionary new architecture, RDRAM can help your design take flight. And Micron can show you how . . . We produce RDRAM and back it up with a team of experts")).

Rambus's Response to Finding No. 1813:

The record shows that Micron did virtually nothing in 1999 to promote RDRAM and that its senior managers claimed credit by the following year for having *prevented* RDRAM's marketplace success. Micron was also working behind the scenes to encourage other DRAM suppliers to block or slow the RDRAM ramp. For example, senior Micron executives expressed the view in the spring of 1999 that those manufacturers that had decided to produce RDRAM in volume had "broken ranks with the other suppliers" and had "sold their soul to the devil."

(RX 1444 at 1). Micron also urged other manufacturers to agree to a "common roadmap" to use with customers to show them that the manufacturers were committed to DDR, not to RDRAM. (RX 2191 at 1; RX 2192 at 3; RX 1423 at 1-2).

Intel concluded in May of 1999 that Micron's business plan was intended to "create as much turmoil to prevent rdram as possible." (RX 1453 at 1). The Intel analysis was quite specific:

> "Marketing - they are aggressively rallying the industry on alternate technologies. They are clearly driving the Sdram-133 alternatives, they are strongly driving ddr and the only player left driving sync-link. Their advertising implies that the rest of the industry is blindly following the Intel roadmap (sheep, communism etc). Should make you mad...
> Relationship - we've tried to broker a deal with rambus (fixing contract in area of ip pooling, royalties and marketing) and per earlier mails, with their advertising and aggressive drive to alternatives, they pissed rambus off enough that any hope of an agreement is pretty dead. They have also ignored our attempts to work with them on enabling, design reviews, roadmap alignment etc."

(*Id*.).

Intel saw no change in Micron's position by October 1999. As an Intel manager explained to Intel's Peter MacWilliams,

> "So far all our discussions with Appleton have had zero benefit for us . . . . [w]e have gone out of our way to help them resolve Rambus contract

issue and in return we have gotten nothing but deception. Micron is working very hard to do everything against RDRAM."

(RX 1515 at 2).[3]

In sum, a finding that Micron "promoted" RDRAM in 1999 or at any other time would be contradicted by the weight of the evidence.

B. The DRAM Industry Was Dissatisfied with Rambus RDRAM Royalty Rates.

1814. Even though DRAM manufacturers were gearing up to produce RDRAM, the DRAM industry remained concerned about Rambus's royalty rates. (CCFF 1802-11, 1816-22).

Rambus's Response to Finding No. 1814:

See RRFF 1802-11, 1816-22.

1815. In the mid-1990's, Rambus acknowledged that high royalty rates could "scare" customers away. (CX0711 at 35 (Crisp email: "our proposition should be attractive there if we do not scare them away with extremely high license/royalty terms"); CX0711 at 13 (Crisp March 1994 email noting Terry Walther's statement that Micron did not like "license type business"); CX0711 at 61 (March 1995 Crisp email: "Farhad [Tabrizi of Hynix] says their #1 issue with the Rambus business proposal is the royalty rate.")).

Rambus's Response to Finding No. 1815:

Rambus did not in the mid-1990's, and does not today, charge "high" royalty rates. *See* RFP 1376-1404.

1816. In December 1996, Rambus offered to license RDRAM to Micron for a 2% royalty rate. (Appleton, Tr. 6337-38; RX0828 at 1). Micron considered Rambus's proposed RDRAM royalty rate "high" because Rambus's technology "was just a very small piece of what was required in total to produce" a DRAM. (Appleton, Tr. 6338).

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[3] Micron's efforts "against RDRAM" included running an ad directed to industry participants depicting them as *sheep* for following Intel's decision to adopt RDRAM. (RX 2305 at 1; Appleton, Tr. 6465).

Rambus's Response to Finding No. 1816:

Rambus does not dispute that Micron, as a manufacturer, would like to reduce its costs wherever possible. Rambus's royalty rates were and are reasonable, however, and well within industry standards. *See* RFP 1376-1404.

1817. Micron considered Rambus's royalty rates high because it had never paid a royalty to a company specifically relating to patents covering a memory interface technology. (Appleton, Tr. 6339; Lee, Tr. 7047-48 ("the kind of royalty rate that was being requested there, the 2 percent, was larger than anything we'd ever heard of for an interface technology and certainly the largest thing we ever heard of for some sort of fee we'd have to pay to produce main memory.")).

Rambus's Response to Finding No. 1817:

Contemporaneous documents do not support this finding. For example, the official IBM Standards Practice Manual that was in effect in 1996 stated that:

> "[t]he normal royalty rate for a license to IBM patents ranges from 1% to 5% of the selling price for the apparatus that practices the patents. This is a very reasonable rate in our industry and generally meets the requirement of standards organizations that licenses be made available on reasonable and non-discriminatory terms and conditions."

(RX 653 at IBM/2 128124). Rambus's RDRAM rates were at the low end of the "very reasonable" range described by IBM. (*Id.*).

Many if not most of the patents that relate to the DRAM manufacturing business are held by the manufacturers and are subject to cross-licensing arrangements, which likely explains Mr. Appleton's testimony that Micron had not "paid" equivalent rates before. (Appleton, Tr. 6300-01; 6499-6500; 6507-08). Appleton also testified that when he became Micron's CEO

in 1994, Micron was paying 10% of total revenues in license fees, and that it has now reduced that to zero through a series of "broad patent cross-licenses." (Appleton, Tr. 6300-01).

1818. In December 1996, IBM expressed concern to Rambus about its royalty rate on RDRAM. (CX0913 at 1 (Mooring December 1996 email: "Steve, Jeff, and I met with more than a dozen IBM apps . . . They have all TI's IP concerns, but worse . . . . they are seriously considering Rambus. But the IP thing is a real dilemma.")).

Rambus's Response to Finding No. 1818:

The document does not refer to royalty rates but rather to the sharing of intellectual property among the RDRAM licensees. (CX 913 at 1).

1819. Siemens considered Rambus's proposed royalty rates of 1-2% unacceptable. (RX0855 at 1 (meeting minutes from January 1997 SyncLink meeting: "Siemens was eloquent. No future RB [Rambus] road map. . . . 0.1% royalty ok, 1-2% ridiculous. RB not acceptable"); Tabrizi, Tr. 9050-51; Lee, Tr. 7045-46 (Siemens's representative "was describing at that meeting that for the Rambus interface technology had the royalty been on the order of .1 percent [Siemens] wouldn't have had a problem with it and he thought the 1 to 2 percent royalty rate was ridiculous")).

Rambus's Response to Finding No. 1819:

The cited remarks by Siemens executive Dr. von Zitzewitz were made at a secret January 1997 meeting of DRAM manufacturer executives in Tokyo. At that meeting, Dr. von Zitzewitz expressed his strong disapproval of those manufacturers who had accepted Intel's choice of the Rambus technology, and he discussed particular royalty rates that would or would not be acceptable for a "main memory" device. (RX 855 at 1; CX 2250 at 2).

It is not surprising that manufacturers would prefer to pay less for raw materials, labor *or* intellectual property. As the FTC's own docket attests, it is also not surprising that manufacturing executives like Dr. von Zitzewitz will sometimes ignore the antitrust laws in an effort to lower those costs. What *is* surprising is that Counsel for the Federal Trade

Commission believe it appropriate to cite, as favorable evidence, private discussions among such executives about specific royalty rates that are, or are not, "acceptable to them." (*Id.*).

The proposed finding should be rejected. At a minimum, it should be rephrased to state that "Siemens believed that Rambus's RDRAM royalty rates were too high and sought to enlist the assistance of other DRAM manufacturers in an effort to prevent a "future RB [Rambus] roadmap . . . ." (*Id.*).

1820. Richard Heye, Vice President of Advanced Micro Devices, { } (Heye, Tr. 3918, *in camera*).

Rambus's Response to Finding No. 1820:

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} **(Heye, Tr. 3919, *in camera*).**

1821. Compaq's server group stated that they would "not use Rambus because of the royalty for the chip set." (CX1030 at 2).

Rambus's Response to Finding No. 1821:

The cited statement is third hand hearsay: a Mr. Choi of LG Semicon is reported to have stated to Rambus personnel that he had heard the information in question from an unnamed person at Compaq. (CX 1030 at 2). No Compaq document introduced at trial makes any such statement, and Complaint Counsel did not ask the lone witness they called from Compaq, Mr. Gross, if the statement was accurate. Under the circumstances, the statement is not a reliable basis for the proposed finding of fact.

1822. Throughout 1997 and 1998, Samsung expressed concern about Rambus's royalty

rates. (CX0983 at 1 (Tate December 1997 email); CX2109 at 160 (Davidow, Dep.) ("we were always going back and forth with Samsung, we were always going back and forth with Intel about issues like this . . . this was the type of issue that Samsung always kept raising about royalty rates")).

Rambus's Response to Finding No. 1822:

The cited evidence does not support the proposition that Samsung expressed a concern "throughout 1997 and 1998," as the finding asserts. In any event, Rambus does not dispute that manufacturers prefer to lower their costs wherever possible. Rambus's RDRAM rates were within industry norms. *See* RFP 1376-1404.

1823. When Samsung asked Rambus to lower its royalty rates in January 1998, Rambus CEO Geoffrey Tate replied, "we'd never lower the 1% long term royalty, period." (CX0992 at 2). When Samsung repeated its request one year later, Rambus stated that "going below 1% would be very hard." (CX1059 at 2 (Tate December 1998 email: Samsung's "mentality is now that they are ramping volume they should get royalty breaks below 1% (suggested 0.5%) [and] that 2% is too steep for initial production (want 1%) . . . we told them . . . that going below 1% would be very hard . . . but i said on the 2% we had flexibility")).

Rambus's Response to Finding No. 1823:

Rambus has no specific response, except to note that manufacturers often attempt to negotiate lower costs, for obvious reasons.

1824. In November 1998, Rambus CEO Geoffrey Tate shared with Rambus executives a strategy to increase Rambus's long-term RDRAM royalty rates. (CX1057 at 1 (Tate November 1998 email: only 3 dram companies are at 1% long term - samsung we can move up at 512Mbit . . . nec/toshiba we could negotiate up as part of an infringing dram license negotiation. so maybe we should be thinking of '1.5%' as the long term royalty rate minimum for the major dram partners. [I]f we get samsung/nec/toshiba up to 1.5% over time; LG semicon/hyundai/hitachi are already at 1.5% 1.t; so then we'd have all the biggies at the same royalty rate (and higher than 1%!)")).

Rambus's Response to Finding No. 1824:

The proposed finding is irrelevant to any issue to be decided in this matter, and in any event the cited e-mail does not refer to a "strategy."

C. Intel Was Concerned about Rambus RDRAM Royalty Rates.

1825. Intel, as a manufacturer of chipsets, has an inherent interest in ensuring that interface technology that it is supporting – such as RDRAM – be as widely adopted by makers of complimentary products as possible. Intel wanted to keep the cost of RDRAM low so that DRAM vendors would be motivated to build RDRAM. (MacWillaims, Tr. 4849-50 (if the DRAM vendors "couldn't sell the new technology at a cost pretty close to the old technology once it got in volume, we couldn't see how the market would transition.")).

Rambus's Response to Finding No. 1825:

Rambus has no specific response.

1826. Because the DRAM industry was concerned about Rambus's high DRAM-related royalty rates, Intel conditioned its support of RDRAM on low royalty rates. (RX1532 at 2 ("Intel made decision NOT to negotiate a contract for the memory vendors, but did add conditions into the contract to help the industry (limit royalties)").

Rambus's Response to Finding No. 1826:

The cited passage does not refer to "high" rates, nor does it support any conclusion about cause-and-effect. (*Id.*) The finding therefore has no evidentiary support.

1827. Intel's contract with Rambus capped the royalty rate Rambus could charge for RDRAM technology at 2%. (CX0938 at 2 (Tate July 1997 email: "RDRAM royalty cap of 2% (per [] our contract with Intel)"); CX2109 at 133 (Davidow, Dep.)).

Rambus's Response to Finding No. 1827:

The proposed finding is incomplete and misstates the import of the cited exhibit, which states that "[w]e also explained to Siemens that with our RDRAM royalty cap of 2% (per the our contract with Intel) plus the patent pooling, *the RDRAM will be the least royalty burdened DRAM*." (CX 938 at 2) (emphasis added).

1828. Intel pressured Rambus to keep its royalty rates low throughout the 1996-1998 time frame. (CX0912 at 2 (Tate November 1996 email: "intel's goal here is to keep rambus from driving up dram royalties"); CX0936 at 1 (Davidow July 1997 email noting that Intel "limited the royalties" DRAM makers "have to pay" to Rambus); CX0952 at 2 (Tate September 1997 email reporting on Intel's "NEW REQUEST" that Rambus institute "long term reduction

of royalty based on volume going to less than ½% for rdrams"); Farmwald, Tr. 8404).

Rambus's Response to Finding No. 1828:

Rambus has no specific response.

1829. Despite Intel's efforts to keep Rambus's royalty rates low, DRAM vendors believed Rambus was continuing to insist on higher than expected royalty rates. (MacWilliams, Tr. 4840 (Intel "heard back from several DRAM vendors who were not very happy with Rambus"); MacWilliams, Tr. 4841 (Intel "heard back from DRAM vendors many times that Rambus was taking maximum advantage of their position. They were charging higher royalties for lower volumes."); CX0936 at 1 (Tate July 1997 email noting that "memory manufacturers feel beaten up" by Rambus); RX1532 at 2 ("Intel made the decision NOT to negotiate a contract for the memory vendors . . . In retrospect, this was a mistake . . . RamBus took advantage of the memory vendors")).

Rambus's Response to Finding No. 1829:

The proposed finding is misleading and not supported by the evidence. None of the cited testimony or evidence suggests that the DRAM manufacturers had an "expectation" about the RDRAM royalty rates. The MacWilliams testimony suggests that DRAM vendors were simply unhappy that before the device hit volume production, they were being charged royalty rates they considered high at the time. (MacWilliams, Tr. 4840).

1830. In September 1997, Rambus CEO Geoffrey Tate and Rambus Vice President David Mooring met with Intel executives Gerry Parker and Pat Gelsinger. (CX0952 at 1). Intel requested that Rambus, among other things, lower its RDRAM royalties even further to help overcome DRAM maker resistance to producing RDRAM devices. (*Id.* at 2 ("they want us to have license deals that reward time to market, etc (old request) AND have long term reduction of royalty based on volume going to less than ½% for rdrams (at this point i choked/gasped)")). Intel explained that if Rambus did not lower its RDRAM royalties, this could cause DRAM makers "to find alternate solutions to avoid paying rambus a royalty" and could cause Intel "to rearchitect things to be completely different if necessary." (*Id.* at 2).

Rambus's Response to Finding No. 1830:

Rambus has no specific response.

1831. Mr. Tate and Mr. Mooring responded to Intel by saying that the industry could

successfully pursue an alternative to RDRAM only if it could set an industry standard with multiple compatible sources and avoid or prove invalid Rambus's patent. (CX0952 at 2-3). They further stated that all industry proposals they had seen would infringe Rambus patent or patent applications. (*Id.* at 3)

Rambus's Response to Finding No. 1831:

The proposed finding is incomplete and not supported by the cited evidence. The initial response by Messrs. Tate and Mooring suggested that the industry would have to do more than simply "set an industry standard with multiple compatible sources and avoid or prove invalid Rambus's patent." The cited exhibit states: "for a dram company to pursue an alternative and be successful they have to a) actually have a superior solution – so far the dram companies have proven themselves incapable of doing this b) set an industry standard with multiple sources all 100% compatible – again, poor track record c) avoid EVERY rambus patent or prove it invalid in court – we said this would be extremely hard to do, that all proposals we've seen violate several fundamental patents we have or that are in process" (CX 0952 at 3).

1832. In October 1997, Rambus CEO Geoffrey Tate had a meeting with Pat Gelsinger, the senior Intel executive responsible for the Rambus relationship. The purpose of the meeting was to follow up on Mr. Gelsinger's earlier request that Rambus "lower [] rdram royalties to <0.5%," and his suggestion that if Rambus failed to do so DRAM makers would "insist on developing alternatives" to RDRAM. (CX0961 at 1).

Rambus's Response to Finding No. 1832:

Rambus has no specific response.

1833. The October 1997 Rambus-Intel meeting focused in part on the extent to which DDR had "GAINED ground" with PC manufacturers and thus was a continuing "threat" to RDRAM. (CX0961 at 2-3). Intel believed that at least one DRAM maker was promoting DDR because of Rambus's royalty rates. (*Id.* at 5 (Rambus CEO Geoffrey Tate's report of the October 1997 Rambus-Intel meeting: "they see ddr being aggressively pushed by samsung BECAUSE of rambus royalties.")).

Rambus's Response to Finding No. 1833:

Rmbus has no specific response.

1834. During the spring of 1998, Intel was still complaining to Rambus about size of Rambus's RDRAM royalty rates. (Farmwald, Tr. 8404-5).

Rambus's Response to Finding No. 1834:

The proposed finding is misleading and not supported by the evidence. The cited testimony (Farmwald, Tr. 8404-05) was a discussion about exhibit CX1016 (at 4), which reported on a discussion between Intel and Rambus about Intel's long-term plans for including Rambus in its next-generation DRAM, *e.g.* in 2002 and 2005, (CX1016 at 4), and not about Rambus's royalty rates for RDRAM in 1998. The cited testimony does not state that Intel was complaining that Rambus's RDRAM royalty rates were too high for DRAM manufacturers, but rather that Intel wanted the profits instead of Rambus: "It was one of the things they were complaining about. Essentially Intel likes to have all the profits in a PC. They don't like to see anybody else have profits." (Farmwald, Tr. 8405).

1835. Intel expected Rambus to do its part to make RDRAM a success by lowering its RDRAM royalties. (CX1007 at 1-2) (Tate March 1998 email: "What Intel wants Rambus to do: Share in risk – offer royalty reduction for DRAM suppliers who are willing to risk starting RDRAM as directed by Intel/Rambus").

Rambus's Response to Finding No. 1835:

The proposed finding is misleading and incomplete. The cited exhibit does not identify "expectations" from Intel, but rather is an email from Intel's Chung Lam "stating the issues Intel is trying to solve, *what Intel proposes to do* to address these issues, and what contribution Intel *would like to see* from Rambus." (CX1007 at 1 (emphasis added)). The relevant proposal cited in the proposed finding was one of *seven* Intel proposed actions (four for Intel, three for

Rambus) attempting to find a way to better ramp the manufacture of RDRAM.

1836. Intel believed that one long term problem with RDRAM was Rambus's royalty-based business model. (CX1016 at 3-4) ("big issue is this one. the dram industry doesn't like the rambus business model. . . . [Intel] perceives that rambus business model has been what makes the rdram ramp so hard to manage – royalties – control/rambus using intel as a club").

Rambus's Response to Finding No. 1836:

The proposed finding is misleading and not supported by the evidence. While Rambus agrees that many DRAM manufacturers dislike paying royalties, especially to a non-manufacturer, the cited exhibit, CX 1016 (at 3-4), identifies Rambus's royalty-based business model only as a "big issue" (not a "long term problem," as the finding states) and does not state that Intel believed that there was a problem with the business model other than the fact that many of the DRAM manufacturers disliked it. (*Id.*)

1837. Rambus had the impression that Intel considered Rambus greedy. (CX1041 at 1-2) (Karp July 1998 email: "Senior executives at Intel don't like us. They think we're greedy and they're worried we could screw up their whole program. . . . GS Choi is very paranoid about Rambus. He's worried we'll bump the royalties way up (5%) once Direct [RDRAM] becomes the standard.").

Rambus's Response to Finding No. 1837:

The proposed response misstates the evidence, in part by suggesting through the misleading use of an ellipsis that Mr. Choi was an Intel employee. He was not. (CX 944 at 1). Moreover, the ellipsis replaces six paragraphs between the 'greed' language and the 'GS Choi' reference, which makes it look like the two references are part of a single subject matter. They were not. (CX 1041 at 1-2).

D. As DRAM Manufacturers Worked to Develop RDRAM, They Encountered Significant Cost Problems.

1838. Rambus co-founder Mark Horowitz acknowledged that one obstacle to marketing

RDRAM was the belief that "[i]t will never be cheap enough to be competitive." (CX1323 at 15 (presentation by Rambus co-founder Mark Horowitz)).

Rambus's Response to Finding No. 1838:

The proposed finding is irrelevant and misstates the evidence. Mr. Horowitz was describing some very early reactions (pre-1995) to Rambus's marketing efforts. His presentation makes it clear that the cited concern was soon *replaced* by a concern that the Rambus technology was so attractive that "Nintendo will use all the supply [and there] won't be any for me." (CX 1323 at 15).

1839. In 1998, DRAM manufacturers were encountering significant cost issues associated with RDRAM production. (CX2521 at 1-2 (September 1998 letter from Samsung executive Yoon-woo Lee to Intel describing difficulties with its RDRAM program: "I'm concerned about high cost structure of RDRAM over PC-100 even without considering the royalty to Rambus."); CCFF 1840-47, 1853)).

Rambus's Response to Finding No. 1839:

Mr. Lee's letter is an effort to convince Intel to support his request to Rambus for lower royalty rates. (CX 2521 at 1-2). The letter does not refer to "significant cost issues" and is evidence of nothing more than a manufacturer's negotiation tactics when seeking to lower its costs.

1840. In the 1998 timeframe, DRAM manufactures estimated that RDRAM would be more costly to produce than other DRAMs. (Gross, Tr. 2364-65 ("the cost to manufacture RDRAM were higher than the costs to manufacture the alternative technologies"); CX2108 at 228 (Oh, Dep.) (the cost of producing Direct RDRAM was "much higher" than other types of DRAM); CX2718 at 44; Lee, Tr. 6733 (Micron "projected a 30 percent cost increase for direct RDRAM relative to an SDRAM."); CX2728 at 2 ("RDRAM cost is about 50% higher than SDRAM in 1999, about 30% in 2000); CX2303 at 16; Tabrizi, Tr. 9172-9174 (Based on die, packaging, and testing costs alone, Hyundai estimated that at the initial stage Rambus would cost 18% more to produce than SDRAM.); Tabrizi, Tr. 9172-9174 (In the high volume stage, Hyundai estimated that RDRAM would cost about 13% more to produce than SDRAM)).

Rambus's Response to Finding No. 1840:

The proposed finding is irrelevant and relies upon unreliable evidence supplied by financially interested parties. Because this is the first of a series of proposed findings relating to manufacturing cost issues, Rambus's objections will be explained in some detail here and summarized in response to subsequent findings.

Complaint Counsel have never explained why Your Honor should enter findings relating to the high, or low, or average cost to manufacture RDRAM. When asked during trial about this issue, Mr. Royall could only say that it was "perhaps" a "subissue" and was "not central to the case." (Tr., 6248-49). Thus, it would be appropriate for Your Honor simply to decline to address Complaint Counsel's proposed findings in this area (CCFF 1838-1861).

There are also substantial due process issues arising from the entry of findings adverse to Rambus on issues related to manufacturing costs and resulting "high" RDRAM prices. Prior to January 2003, Rambus had obtained through discovery substantial evidence of concerted action by DRAM manufacturers to keep RDRAM prices high in the 1999-2001 time period in an effort to prevent the successful marketplace entry of the RDRAM device. Among the tactics employed by the manufacturers was the coordinated dissemination to customers of false and misleading information about the costs and difficulties involved in the manufacture of RDRAM. (*See* RPF 1591-1602).

In January 2003, however, in response to a concern expressed by the Department of Justice that Rambus's discovery efforts might interfere with an ongoing Grand Jury investigation into collusion by the DRAM manufacturers, Judge Timony entered an order barring Rambus from taking certain discovery relating to communications between DRAM

manufacturers. The effect of this order was to limit Rambus's ability to pursue discovery that it might now use to rebut Complaint Counsel's findings in this area, including the ultimate proposed conclusion that it was "high manufacturing costs and technical problems [that] led to the decline" of RDRAM. (CCFF, heading IX). It would be procedurally and substantively unfair to base such findings on a record that was limited by Judge Timony's January 2003 ruling.

In addition, the specific finding at issue here, CCFF 1840, is not supported by the evidence and misrepresents the cited testimony in a manner designed to mislead Your Honor. The first citation is to the testimony of Ms. Jackie Gross, formerly of Compaq, about RDRAM manufacturing costs. Complaint Counsel cite to her testimony in the following way:

> ("Gross, Tr. 2364-65 ('the cost to manufacture RDRAM were higher than the costs to manufacture the alternative technologies')))."

It would naturally appear to the reader that Ms. Gross had testified, from her personal knowledge, that RDRAM manufacturing costs were higher than those of the alternative technologies. Ms. Gross did not so testify, however. Here is the full quote, with the portion that Complaint Counsel omitted in italics.

> "*It was our impression that* the cost to manufacture RDRAM were higher than the costs to manufacture the alternative technologies."

(Gross, Tr. 2365) (emphasis added).

Complaint Counsel's decision to omit the italicized portion of Ms. Gross's testimony, without even any indication to Your Honor that there had been any omission, is unfortunate. The omitted language is quite meaningful, for on cross-examination, Ms. Gross explained that

the "impression" she had testified about had come *from "the DRAM suppliers*." (Gross, Tr. 2367) (emphasis added).

Ms. Gross's testimony is thus not a reliable source for any finding about actual manufacturing costs, both because she lacked the necessary foundation and because, as noted above and as discussed below, there is substantial evidence in the record that DRAM suppliers had provided misleading and inflated RDRAM cost, price and production estimates to customers such as Compaq in an effort to slow or block RDRAM's market introduction. Ms. Gross's testimony is only as reliable as the story she was told.

The story she was told was false. As Mr. Tabrizi (whose trial testimony is also cited in support of this finding) acknowledged at trial, one way to cause RDRAM to fail to achieve market acceptance was to convince the OEMs that even if RDRAM volumes went up, prices would not fall. (Tabrizi, Tr. 9083). If the OEMs were convinced of this, they would not adopt RDRAM. (*Id.*).

The evidence shows that Mr. Tabrizi took steps to ensure that RDRAM production stayed low, so that the price difference between RDRAM and SDRAM stayed high. In the fall of 1998, Hyundai and Mr. Tabrizi gave RDRAM price projections to their customers that were on the order of 50% to 60% higher than those reflected in internal pricing documents. (Tabrizi, Tr. 9085-90; RX 1280; RX 1293A). Mr. Tabrizi encouraged Hyundai's sales force to distribute these higher prices to key accounts that were deciding whether to use RDRAM, DDR SDRAM, or PC100. (*Id.*)

Mr. Tabrizi also admitted at trial that in October 1998, Hyundai gave RDRAM production forecasts to Intel that were deliberately inflated. (Tabrizi, Tr. 9092). (*See also*

RX 1295 at 1) (internal Hyundai e-mail, copied to Tabrizi, that states that from the perspective of the Hyundai America marketing group, "we can overstate our Direct Rambus production so Intel can feel we are more aggressive on the ramp up.") It is likely that when combined with Hyundai's inflated price forecasts, the inflated production numbers that Hyundai provided were intended to convince Intel that RDRAM prices would not come down *even if* production increased.

Mr. Tabrizi also urged his fellow DRAM manufacturers to lie to Intel about production and pricing. A report prepared by an Infineon engineer about an October 1998 meeting attended by Mr. Tabrizi, along with Micron's Terry Lee and other engineers from Micron and Infineon, states that "[a]ccording to Farhad Tabrizi, Hyundai has given Rambus ASP projections for end of next year of 2-3 times of todays SDRAM prices; they also gave to Intel a production projection of three times their actual plans => *they encourage every DRAM manufacturer to do the same in order to let Intel not generate a Rambus oversupply*." (RX 2192 at 2) (emphasis added).

In addition, there is evidence in the record that senior Micron executives were also very concerned about the possibility of an "oversupply" of RDRAM, primarily because of Samsung's 1999 RDRAM production plans, and that they had communicated their concerns to Samsung. (RX 1444 at 1). In the same vein, Hyundai's internal documents show a concern in July 1999 that "[w]ith Samsung building significant amounts of product, we need to work with them to limit the supply in the market. . . ." (RX 1487 at 4).

The evidence shows that the manufacturers' efforts to limit RDRAM supply severely impacted the OEM's plans to launch products incorporating RDRAM devices. As an example,

Compaq's Ms. Gross testified that the DRAM manufacturers were not prepared to "increase their output at the rate at which we needed to support our systems." (Gross, Tr. 2346). Dell faced the same problem. In a February 2000 e-mail asking Micron to supply it with RDRAM, Dell stated that it was "committed to Rambus" but that its ability to incorporate Rambus devices in its PC's was "clearly limited by supply." (RX 1560 at 1). Looking ahead to the second half of 2000, Dell projected that with lower pricing, fully 40% of its market demand would be satisfied with RDRAM technology. (RX 1560 at 1).

By May 2000, however, the situation had not improved, and Dell was considering moving into "a low key Rambus mode." (RX 1636 at 1). Dell's "message" was "pretty straightforward:"

> "Dell has booked our products over the last year around the assumption that RDRAM prices would decline and close on SDRAM. This would help us create demand . . . the memory vendors have shown no desire to drop prices, therefore we are reevaluating out strategies . . . so the message to them is drop prices or we will continue to decrease our RDRAM forecasts and we will architect next generation systems around DDR . . . we will give the memory vendors till the end of May to reply to our request . . . if they still have no desire to drop prices, we should push ahead rearchitecting chipsets around DDR."

(RX 1636 at 1). Prices did not come down, however, and Dell shifted its roadmap to DDR.

In sum, while the parties appear to agree that RDRAM's failure to obtain substantial market penetration between 1999 and 2001 was tied to insufficient supply and high prices, they

strongly *disagree* about whether supply shortages and high prices were caused by purportedly high royalties and manufacturing costs and by assorted technical problems, as Complaint Counsel assert, or by a concentrated effort to keep production low and prices high, while disseminating false information about manufacturing costs to justify supply shortages and high prices.

There is evidence on both sides of this equation. Much of the evidence that Complaint Counsel rely upon, however, come from Hynix, Micron and Infineon, each of whom is implicated in the evidence of concerted action that has been put in the record, and each of whom is engaged in vigorous patent litigation with Rambus. The evidence as a whole, when viewed in this light, should lead Your Honor to reject Complaint Counsel's proposed findings (of which this is the first) regarding manufacturing costs and technical problems and their purported role in RDRAM's demise. As an alternative, in light of the evidence that Rambus has submitted, and in light of Judge Timony's ruling blocking Rambus's discovery efforts into the manufacturers' collusive activities, and in light of the concededly "subsidiary" nature of the issues of manufacturing costs and technical problems, the Court should decline to adopt *any* findings regarding these issues.

1841. Several factors contributed to the high cost of producing RDRAM. (CX2716 at 1 (Lee January 1998 email: "There are several issues that effect the cost curve for DRDRAMs, which include the packaging, handlers, burn-in equipment, die size, licensing, and test. Some of these areas will require the purchase of new manufacturing equipment, and some areas have an inherently higher manufacturing cost."); CX2083 at 132-133).

Rambus's Response to Finding No. 1841:

For the reasons set out in detail in response to finding no. 1840, which detail will not be repeated here, this finding is neither relevant nor based on credible evidence. It should be

rejected because:

(1) it is not relevant to any material issue in dispute;

(2) Rambus's ability to take discovery into the manufacturers' concerted efforts to misrepresent to customers the actual manufacturing costs and consequent prices of RDRAM was limited by Judge Timony's January 2003 order; and

(3) the documents and testimony that the finding relies upon are not credible in light of the evidence that *is* in the record of the manufacturers' efforts to block RDRAM's launch by restricting the supply of RDRAM – thus increasing its costs – and by misrepresenting their future production and cost estimates.

Moreover, the issues raised by this particular finding do nothing to explain why DDR SDRAM prevailed in the marketplace in lieu of RDRAM, for all of these issues were present in connection with the product introduction of the DDR device, as Micron CEO Steve Appleton confirmed in an analyst call in September 2002. (RX 2067 at 7 – referring to "the hard transition to DDR . . . because it is a much more complicated device to build and test and to get to yield like you want. . . .")

1842. Most importantly, RDRAM cost more to produce than SDRAM because Rambus's royalty fees drove up the cost. (CX2303 at 16 ("Other Cost Adder - Direct Rambus Royalty); Tabrizi, Tr. 9174 ("Direct Rambus had other costs. We had to pay royalt[ies], so that was [an] additional cost.")).

Rambus's Response to Finding No. 1842:

The cited evidence does not say that the royalty was "most important," and it does not say that RDRAM cost more than SDRAM as a result of any royalties. As a consequence, the finding is without support. It is irrelevant, in any event, and inappropriate for the reasons

described in RRFF 1840-41.

1843. RDRAM cost more to produce than SDRAM because RDRAM involved a larger die size. (Lee, Tr. 6733-5; Tabrizi, Tr. 9167-68; CX2303 at 15 ("13.5% die Penalty over SDRAM")).

Rambus's Response to Finding No. 1843:

The finding is vague and misleading in comparing production costs of RDRAM and SDRAM at very different stages of their product life cycles. By 1999 and 2000, SDRAMs had been produced in commercial volumes for several years and had been through several "shrinks" to reduce die size and other costs. "Shrinks" reduce costs by allowing manufacturers to achieve economies of scale by producing a higher volume of DRAMs per silicon wafer. *See* CCFF 104. As Micron's Brett Williams explained it:

> "Q. And it's been your experience that there are economies of scale which are realized in the manufacture of integrated circuits, correct?
>
> A. Correct.
>
> Q. The higher the volume, generally the cheaper the cost of manufacture?
>
> A. Correct."

(Williams, Tr. 872) (*see also* MacWilliams, Tr. 4837-38) ("the DRAM vendors, for operating reasons, typically will shrink their highest-volume parts first, and therefore those parts have an advantage because they get the process technologies, the best cost structures first, its in their economic interest to do so.")

Comparing the die size of SDRAMs at a time when they have been in high volume production for several years with RDRAMs that are only being sampled is to compare apples and orangutans; it is irrelevant and misleading. The comparison described in the finding also

has no time frame, which likely means that it does not reflect the substantial (and successful) efforts of Rambus to work with suppliers (other than Micron, which declined assistance) to lower the die size of the RDRAM part. (Hampel, Tr. 8691-92; 8696-97; 8709-10; 8723-24).

Finally, the proposed finding is based almost entirely on testimony from Hynix's Mr. Tabrizi and Micron's Mr. Lee. For the reasons stated at RRFF 1840-41, their testimony on issues relating to RDRAM manufacturing costs is entirely unreliable.

1844. RDRAM cost more to produce than SDRAM because companies had to change their packaging and assembly systems to accommodate Rambus's different type of package. (Lee, Tr. 6733, 6735; Tabrizi, Tr. 9174-75; Peisl, Tr. 4416-17; CX2303 at 16; Gross, Tr. 2363-64 ("the RDRAM device was what was known as a ball grid array, BGA package, and that was a new package relative to high volume production in the DRAM industry.")).

Rambus's Response to Finding No. 1844:

The proposed finding is irrelevant and is again based upon the testimony of unreliable, financially interested witnesses from the three companies with whom Rambus is currently in litigation: Micron, Hynix and Infineon. While this finding does cite to (and quote) testimony by Compaq's Ms. Gross about packaging, she only testified that the package was "new," not that it was more expensive. (Gross, Tr. 2363-64).

For the reasons set out in detail in RRFF 1840-41, which will not be repeated here, the proposed finding should be rejected.

1845. RDRAM cost more to produce than SDRAM because companies had to invest in expensive new high performance testing equipment. (Lee, Tr. 6733, 6736; Peisl, Tr. 4416-17; Tabrizi, Tr. 9174-75 (Hyundai "had to invest [in] a new tester because Rambus require[d] a high performance tester, and each . . . tester is in multimillion-dollar range"); Gross, Tr. 2362-63 ("The issue with testing was that because [the] RDRAM product was very fast technology, it would have required new and expensive testing equipment")). Manufacturers had to wait nine months to one year to obtain the new testing equipment. (Gross, Tr. 2363 ("describing "long lead time" to purchase testing equipment)).

Rambus's Response to Finding No. 1845:

The proposed finding is irrelevant, ambiguous as to time frame and inappropriate for the reasons described in RRFF 1840-41. The proposed finding also does nothing to explain why DDR SDRAM prevailed in lieu of RDRAM, since high speed DDR devices also required new and expensive testers. (RX 2067 at 7). Finally, as Mr. Hampel explained, test cost analyses that focus on capital expenditures depend in large part on the volume of devices tested. Assuming equivalent *volume* production of the RDRAM and SDRAM devices, test costs would be at least equivalent, and because of the high speeds at which the Rambus device could be tested, could even be less for the RDRAM devices. (Hampel, Tr. 8703-04).

1846. RDRAM cost more to produce than SDRAM because the RIMMs, memory modules that go with the Rambus memory, were more expensive. (Heye, Tr. 3700-01 ("rim has heat syncs, that's more expensive . . . [also] the layout of the RIMMs, how you physically hook up to Rambus on those RIMMs was extremely expensive")).

Rambus's Response to Finding No. 1846:

The proposed finding is irrelevant, ambiguous as to time and not based on the personal knowledge of the sole witness offered to support it, Mr. Heye. He testified only about what he would "hear" in early 1998 from unidentified individuals at unidentified companies referred to only as "memory module makers." (Heye, Tr. 3700). Moreover, in overcoming a hearsay objection from Rambus's counsel, Complaint Counsel promised several times that he was "not offering [the testimony] for the truth," but only for Mr. Heye's "state of mind." (Heye, Tr. 3697-98). The testimony cannot, therefore, be used to support the proposed finding. *See* Order On Post Trial Briefs, July 10, 2003.

1847. In early 1998, the "cost of Rambus was starting to concern memory vendors." (Heye, Tr. 3696-97 ("some of the initial cost projections of Rambus versus DDR were not

coming in line to what had initially been expected . . . it was much more expensive than people had thought")). Many memory vendors told Mr. Heye that RDRAM had a higher cost structure per part basis than DDR. (Heye, Tr. 3697).

Rambus's Response to Finding No. 1847:

The proposed finding is irrelevant and again violates Your Honor's July 10, 2003 Order. Mr. Royall stated that he was "not offering [Mr. Heye's testimony] for the truth," but only for Mr. Heye's "state of mind." (Heye, Tr. 3697-98). As a result, the Heye testimony cannot support the proposed finding.

1848. DRAM suppliers were reluctant to produce RDRAM because there were "issues with the availability of test equipment and some packaging" and supply materials. (RX1287 at 5 ("Suppliers reluctant on move to RDRAM . . . issues with test, packaging"); Gross, Tr. 2362).

Rambus's Response to Finding No. 1848:

The proposed finding is irrelevant; it also misstates the cited document and the cited testimony, which refer to several reasons, not just the reason referenced in the finding, and which make clear in any event that these reasons were given to Ms. Gross by the DRAM [s]uppliers:

> "Q: And you were asked about some of the reasons why suppliers were reluctant to transition to RDRAM, and all of these bases were things that the DRAM suppliers were telling you. Is that right?
>
> A. Yes.
>
> Q. Did you do any kind of audit to find out whether or not what they were telling you was, in fact, the case?
>
> No."

(Gross, Tr. 2367).

1849. Dell understood that the RDRAM cost premium inhibited the development and production of RDRAM. (CX2180 at 1, 4 (Dell Presentation regarding RDRAM Outlook: "Cost premiums continue to be the main ramp inhibitor . . . Rambus premium over SDRAM are inhibiting ramp . . . No evidence of any significant efforts to reduce Rambus premiums, Dell Customers don't believe cost will ever drop")).

Rambus's Response to Finding No. 1849:

The parties agree that the "premium"– the difference between the price charged by the DRAM manufacturers for RDRAM and the price they charged for SDRAM – inhibited the successful marketplace introduction of RDRAM.

1850. Compaq's customers were price conscious and considered computers with RDRAM too expensive, even though RDRAM had performance advantages. (Gross, Tr. 2293-94 ("it didn't seem that the customers were willing to pay extra for the benefits of RDRAM")).

Rambus's Response to Finding No. 1850:

The proposed finding is irrelevant since it does not explain *why* Compaq was having to charge more for its computers containing RDRAM. As Ms. Gross testified, and as Compaq's own documents show, OEMs were facing a shortage of RDRAM created because the "suppliers have not invested to support current Rambus demand for 1999." (RX 1287 at 4). (See also Gross, Tr. 2346) (the DRAM manufacturers were not prepared to "increase their output at the rate at which we needed to support our systems").

1851. Intel was very concerned about the cost of RDRAM. (CX0974 at 1 (Tate December 1997 email discussing Rambus-Intel meeting: "COST – biggest issue"; "rdram price premiums of 20-30%!!"; "die size premium"; "royalty reduction"); CX2109 at 218-19 (Davidow, Dep.) (Intel representatives attended Rambus Board meetings to review what Rambus was doing to reduce costs)).

Rambus's Response to Finding No. 1851:

The proposed finding is irrelevant and ambiguous as to time frame.

1852. Intel believed that cost-related issues associated with RDRAM's die size could

prevent the industry from accepting RDRAM. (CX0961 at 2) (Tate May 1998 email: "die size is the new BIG concern at pat [Gelsinger's] level – he's concern that our die size premium could price us out of much of the market").

Rambus's Response to Finding No. 1852:

The proposed finding is irrelevant, since it is vague as to time and since the only evidence cited predates the die size control efforts that Rambus successfully instituted in 1999 and 2000. (Hampel, Tr. 8691-92; 8696-97; 8709-10; 8723-24).

1853. In 1998, Intel was doubtful that the cost of manufacturing RDRAM would ever be comparable to the cost of making SDRAM. (CX2541 at 1; CX2887 at 1 ("Rambus's original commitment of achieving #5% parity with SDRAM on cost has been grossly missed. Without dramatic efforts by Rambus, this goal will not be met for several years, if ever.")).

Rambus's Response to Finding No. 1853:

The proposed finding is irrelevant and misleading. The two exhibits it cites are simply two versions of the same document; neither is dated in 1998. Moreover, while it is true that the cost difference between SDRAM and RDRAM widened in 1998, Intel recognized that the reason was that the price of SDRAM had dropped like a rock:

> "1H98 . . . SDRAM costs dropped significantly, introducing a 15-30% cost delta vs. the original thought of 5-10% delta between SDRAM and RDRAM." (RX 1532 at 2).

1854. Rambus was aware of the cost issues associated with producing RDRAM. (CX1034 at 2 ("lots of discussion about cost/price of direct rambus"); CX0622 at 1-2 (July 1999 Rambus Board Meeting Minutes: "reviewed test issues and cost, packaging costs and an evaluation of RDRAM die area overhead")).

Rambus's Response to Finding No. 1854:

The proposed finding is irrelevant, although Rambus agrees that the manufacturers' stated estimates of their purported manufacturing costs and pricing of RDRAM represented a

concern that Rambus worked to resolve. (Hampel, Tr. 8688-8708; CX 1355 at 49, 52-53).

1855. When Sun Microsystem expressed concern to Rambus about cost issues associated with RDRAM, Rambus responded, "once the technology gets to volume, the costs will come down." (Bechtelsheim, Tr. 5823). Sun co-founder Andreas Bechtelsheim believed that Rambus did not "have any understanding of issues such as testing cost" and other problems that "later became significant burdens for their technology." (*Id.*)

Rambus's Response to Finding No. 1855:

The proposed finding is irrelevant and grossly misrepresents Mr. Bechtelsheim's testimony. Mr. Bechtelsheim left Sun in 1995. (Bechtelsheim, Tr. 5740). The conversations with Rambus that he describes occurred in the early 1990's, *before* Intel selected Rambus as its next generation memory technology, *before* Direct RDRAM was developed, and *before* the events described in the other findings in this section. (Bechtelsheim, Tr. 5816-5823). Mr. Bechtelsheim's testimony is thus entirely irrelevant to the proposed findings in this section.

1856. In April 1999, the cost issues associated with producing RDRAM remained a problem. (Lee, Tr. 6747-6750; CX2735 at 33 ("Rambus and RIMM Issues Remain, RDRAM die size adder - Will the customer pay for it?, Extra high-speed testing vs. SDRAM, CSP packaging learning curve; Royalty cost"); CX2334 at 27 ("Hyundai Rambus DRAM Strategy, Cons . . . Cost (royalty/test/yield)); Tabrizi, Tr. 9212-13 (one of the disadvantages of the Rambus product was high costs "due to royalty, test, and yield")).

Rambus's Response to Finding No. 1856:

The proposed finding is irrelevant and inappropriate for consideration for all the reasons set out in detail at RRFF 1840-41.

1857. In September 1999, Micron projected that in 2000, RDRAM would cost 40-50% more to produce than SDRAM. (CX2747 at 68; Lee, Tr. 6763-64). Although Micron estimated that the relative cost of manufacturing RDRAM compared to SDRAM would decrease over time, Micron projected that the added cost of producing RDRAM would remain at 30% in second half of 2000. (CX2747 at 68; Lee, Tr. 6763–65).

Rambus's Response to Finding No. 1857:

The proposed finding is irrelevant and inappropriate for consideration for all the reasons set out in detail at RRFF 1840-41.

1858. Micron also projected that RDRAM would always be more costly to produce than SDRAM because of RDRAM's increased die size. (Lee, Tr. 6765-67; CX2747 at 69 ("Die size adder appears to be constant at -25-30% for standard RDRAM")).

Rambus's Response to Finding No. 1858:

The proposed finding is irrelevant and inappropriate for consideration for all the reasons set out in detail at RRFF 1840-41.

1859. Some people in the DRAM industry were concerned that Rambus could fail for technical reasons or because of cost issues. (Lee, Tr. 6931).

Rambus's Response to Finding No. 1859:

The proposed finding is based solely on unreliable hearsay and is vague as to time.

1860. One and a half years later, at the Intel Developer Forum in spring 2001, companies were still discussing ways to reduce the cost of RDRAM. (Hampel, Tr. 8712-19; RX1762 at 80 (Toshiba presentation on its RDRAM "Cost Reduction Plan")).

Rambus's Response to Finding No. 1860:

The proposed finding is both irrelevant and inconsequential. Complaint Counsel elsewhere propose findings that assert that DRAM manufacturers are "constantly" trying to reduce costs on every DRAM they build. *See* CCFF 95-105.

1861. As late as 2001, despite efforts to reduce the costs associated with producing RDRAM, Elpida expected the cost differential between RDRAM and SDRAM to continue into 2003. (RX1762 at 39).

Rambus's Response to Finding No. 1861:

The proposed finding is irrelevant because of the time frame involved. By 2003, the

appropriate question would not be RDRAM costs versus SDRAM costs; it would be RDRAM costs versus DDR SDRAM costs. On that issue, the cited document shows *lower* projected RDRAM costs than DDR costs in 2002 and 2003. (RX 1762 at 42). The same Elpida presentation called RDRAM the "most competitive leading process" available. (RX 1762 at 43).

E. The DRAM Industry Tried to Resolve the Problems with RDRAM Despite Only Mixed Support from Rambus.

1862. Despite several "cons" with RDRAM, including cost issues associated with testing and royalty payments, DRAM manufacturers were committed to fixing problems with RDRAM. (CX2334 at 27 (Hyundai made solving remaining problems with RDRAM a "High priority"); CX2108 at 227 (Oh, Dep.) (Hyundai assigned resources to solve design and technical related problems with RDRAM); Lee, Tr. 6747-51; CX2735 at 37-40 (Micron attempted to use better packaging); CX1368 at 1-2; Hampel, Tr. 8708-09 (Micron was working with Rambus to reduce the cost of RDRAM)).

Rambus's Response to Finding No. 1862:

Rambus will not describe here all of the contemporaneous documents that prove that the companies (Micron and Hynix) whose witnesses are cited in support of this finding were *not* "committed to fixing problems with RDRAM," as the finding asserts, and were instead trying to "kill" RDRAM, in Mr. Tabrizi's words (RX 1661 at 2), so that they could claim credit for and celebrate RDRAM's demise, as Micron's Vice President Sadler did in September 2000 (RX 1700 at 1). Simply put, the proposed finding is contrary to the overwhelming weight of the evidence on this point. *See* RRFF 1802, 1808, 1840-41.

This finding also cites testimony by Rambus's Craig Hampel for the proposition that Micron was working with Rambus to reduce the cost of RDRAM. The description of Mr. Hampel's testimony is grossly inaccurate. Mr. Hampel testified that Rambus was "pleading

with Micron to let us try to help them" and was "asking them to give us information. . . ."

(Hampel, Tr. 8710-11; 8687-88).

1863. In mid-1997, Intel sought to influence Rambus to establish better relations with DRAM makers. (CX0944 at 1 (Tate August 1997 email noting that he had met with Samsung and that "the main objective of this meeting was to start to address intel's 'dram vendor happiness' issue"); CX0954 at 1-2, *in camera* {
}).

Rambus's Response to Finding No. 1863:

The proposed finding is irrelevant and inappropriate for consideration for all the reasons set out in detail at RRFF 1840-41.

1864. Intel and Rambus executives discussed ways to fix Rambus's relationship with the DRAM manufacturers. (MacWillaims, Tr. 4871-72). Rambus "seemed to be sensitive to the fact that they needed to fix" problems with DRAM manufacturers. (MacWilliams, Tr. 4873). However, Intel "didn't see much action in many cases." (*Id.*) What actions Intel did see "didn't do much to fix the issues." (*Id.*)

Rambus's Response to Finding No. 1864:

The proposed finding is irrelevant and misstates Mr. MacWilliams' testimony. *Immediately* after the quoted portion, he said "well, let me step back a second," and he then described actions that Rambus *did* take. (MacWilliams, Tr. 4873-74). He also explained that he had based his prior answer on what the *DRAM suppliers* were telling him:

> "Well, at the end, *the DRAM vendors* still were telling us that there was a problem."

(*Id*.) (emphasis added).

1865. In 1998, Intel continued its work to make RDRAM a market success by investing in DRAM companies that developed and supplied RDRAM. (CX1006 at 1 (Rambus executive David Mooring reported that Intel "would invest about $1 billion in . . . several of the top DRAM companies with the funding tied to RDRAM execution."); CX2522 at 2-3 (October 1998 Intel press release: "We will invest $500 million in Micron to support the development

and supply of next generation memory products, specifically Direct RDRAM . . . Key Messages: The investment in Micron is part of Intel's strategy . . . to help drive PC industry growth by accelerating the adoption of Direct RDRAM"); Appleton, Tr. 6375-6378)).

Rambus's Response to Finding No. 1865:

Rambus has no specific response.

1866. Intel did not succeed in mending the relationship between Rambus and the DRAM manufacturers. (MacWilliams, Tr. 4874 (in "the end, the DRAM vendors were still telling us that there was a problem. [Rambus] somehow [wasn't] able to take the step to get the DRAM vendors to perceive them as a key part of the value added to the industry.")).

Rambus's Response to Finding No. 1866:

As RRFF 1840 and 1841 make clear, some of the DRAM vendors were not interested in "mending . . . relationships" with Rambus. The evidence establishes that at the same time that *Hynix's* Mr. Tabrizi was engaged in "RDRAM killing" (RX 1661 at 2), *Micron* was "ignor[ing] [Intel's] attempts to work with them on enabling" RDRAM (RX 1453 at 1), ignoring Rambus's efforts to help them design and produce RDRAM (Hampel, Tr. 8710-11), and "working very hard to do everything against RDRAM." (RX 1515 at 2).

F. Rambus and Intel Averted a Major Blow-up in Spring 1998.

1867. Despite Intel's efforts to make RDRAM a market success, by 1998 the Rambus-Intel relationship was on a rocky road. (CCFF 1865, 1868-70, 1873-75).

Rambus's Response to Finding No. 1867:

The cited findings do not support the proposed conclusion.

1868. In March 1998, Intel sought to obtain "rights to Rambus IP for use in non-competing areas," and also in "competing areas after Intel introduces the broad range of products." (CX1007 at 2). Intel wanted "to eliminate any chance of IP-related litigation from Rambus." (*Id.*)

Rambus's Response to Finding No. 1868:

Rambus has no specific response.

1869. On April 14, 1998, Rambus CEO Geoffrey Tate and Chairman William Davidow met with Pat Gelsinger of Intel to discuss Intel's concerns about Rambus. (Farmwald, Tr. 8402; CX1016 at 1; CX2109 at 174-75 (Davidow, Dep.); CX2083 at 127-28, 132 (Davidow, Dep.) (Intel's concern was "whether they could get RDRAMs in a volume and at a price that would enable them to sell their products competitively. And so, I think they were driving home that point to us.")). The basic message of the meeting was that in the intermediate term Intel would continue to support RDRAM, but Intel might support a competing architecture for the next generation. (CX1016 at 1-4 ("Intel says they are basically going to compete with us on next generation.")).

Rambus's Response to Finding No. 1869:

Rambus has no specific response.

1870. The April 14, 1998 Rambus-Intel meeting caused Rambus executives to consider asserting Rambus's patents against DRAM manufacturers. As Rambus CEO Geoffrey Tate wondered, "when will intel tell the dram companies that they are investigating next generation interface without rambus?" (CX1016 at 6; CX2109 at 176-78 (Davidow, Dep.)). Mr. Tate was concerned that a statement from Intel would cause DRAM manufacturers to switch support away from RDRAM for the next generation, which in turn could force Rambus to assert its intellectual property rights against DRAM manufacturers earlier than it wanted to. (*Id.* at 6 ("will the dram companies then not want to work with us (on next generation)? this could force us to play our IP card with the dram companies earlier.")).

Rambus's Response to Finding No. 1870:

The proposed finding is incomplete, misleading and not supported by the evidence. The cited exhibit and deposition testimony do not suggest that the discussion with Intel caused Rambus to consider asserting patents against DRAM manufacturers. They instead suggest that if Intel made the decision to abandon Rambus's RDRAM for the *post*-Direct RDRAM technology (sometime around 2002-2005), and publicly announced that decision (presumably sometime sooner than 2002), this announcement "*could*" force Rambus to protect its shareholders' interests by explaining (CX 1016 at 6) that Rambus had a "very substantial

intellectual property portfolio, including some very strong patents" (Farmwald, Tr. 8405-6) that the *next*-generation (post-Direct RDRAM) technology would not avoid.

1871. Rambus's strategy of "play[ing] the IP card" entailed threatening to sue companies that worked on non-Rambus DRAM devices for the next generation. (Farmwald, Tr. 8405-06 (Q. "do you have an understanding of what Mr. Tate meant here when he refers to the possibility of Rambus having to play its IP card with DRAM companies earlier? . . . [A.] this refers to our telling the DRAM companies that if you work on a new generation with Intel, we will sue you"); CX2109 at 176-77 (Davidow, Dep.) ("Q. What do you understand Mr. Tate to be referring to here when he says, 'this could force us to play our IP card with the DRAM companies earlier'? . . [A.] I would assume that this statement means is that we would inform the DRAM manufacturers that we had intellectual property that read on these technologies.")).

Rambus's Response to Finding No. 1871:

The proposed finding is irrelevant, incomplete and misleading in suggesting that this statement refers to suing companies over SDRAM or DDR SDRAM. It is clear from the exhibit underlying both portions of cited testimony, CX 1016, that "to play the IP card with DRAM companies earlier" did not mean asserting Rambus's intellectual property against SDRAM or DDR SDRAM, as the proposed finding seems to suggests, but against whatever next generation of DRAM Intel might adopt *after* Direct RDRAM. The phrase arises in CX 1016 in Mr. Tate's report about a discussion that occurred on the car ride back from the meeting with Intel, during which the two companies were talking about Intel's "LONG TERM" objectives. (CX 1016 at 3-6). During that earlier discussion Tate reports Intel as having said it was "not clear what's next for memory interface/what rambus role is/2002 or 2005/ don't know. but it's clear that direct rambus won't last forever and something will be next. never guaranteed we'd use rambus forever. decided to launch technical effort by end of Q2 to explore what next generation interface is/needs to be. . . . question is do I tell the design team to work around your IP; or give them the option of using your IP (if it results in a better solution)? [bill and I both heard this as:

we're going to compete with/kill you; but if we don't beat you we might still use you]". (*Id.*)

Later, reporting on the car-ride discussion, Mr. Tate wrote: "seems likely that intel is going to tell their technical team a) what's the best solution without using rambus IP? b) what's the best solution using rambus IP? c) is (a) good enough versus (b)? if so, use it and freeze out rambus. seems they'll do this [tell this to their technical team] whether we give them competing useage rights or not. when will intel tell the dram companies that they are investigating next generation interface without rambus? If so, will the dram companies then not want to work with us (on next generation)? this could force us to play our IP card with the dram companies earlier." (*Id.*)

It is clear that Mr. Tate's concern was about the memory generation *beyond* Direct RDRAM, not whether SDRAM or DDR SDRAM infringed Rambus patents.

1872. After the April 14, 1998 Rambus-Intel meeting, Tate called for a "** TENTATIVE BOARD MEETING**" and immediately began strategizing about how to address Intel's announcement that it would compete with Rambus. (CX1016 at 1 (Tate April 14, 1998 email: "we'll be doing brainstorming/strategy prep meetings at rambus over the next 2 weeks"); CX2109 at 178-79 (Davidow, Dep.)).

Rambus's Response to Finding No. 1872:

Rambus has no specific response.

1873. Rambus executives were "angry" about some of the discussions at the April 14, 1998 Rambus-Intel meeting. (Farmwald, Tr. 8406-7 ("I remember being pretty angry about this")).

Rambus's Response to Finding No. 1873:

The finding is supported only by Mr. Farmwald's testimony, so the reference to "Rambus executives" is inaccurate.

1874. On April 15, 1998, Rambus co-founder Michael Farmwald responded to Mr.

Tate's concerns about Intel's commitment to RDRAM by suggesting that Rambus "shouldn't work with [Intel] and in fact should enforce [Rambus's] patents against the next – a new standard." (Farmwald, Tr. 8406-7; CX1021 at 1 (Farmwald April 1998 email: "[i]f it comes to all-out war" with Intel, Rambus might be "in a position to go after them for royalties," or could produce documents that would make Intel "look extremely bad both to the press, a court, and to the FTC.")).

Rambus's Response to Finding No. 1874:

The proposed finding is irrelevant, incomplete and misleading. On April 15, 1998, Farmwald did not suggest that Rambus "shouldn't work with" Intel. Rather he wrote: "I'm not even sure we want to agree to work together on the next-generation memory interface." (CX 1021 at 1). Nor did he state that Rambus should enforce patents against SDRAM or DDR SDRAM, as the finding suggests. (*Id.*).

1875. On April 16, 1998, Rambus Chairman William Davidow responded to Mr. Farmwald's email by urging a more measured approach. (Farmwald, Tr. 8407; CX2109 at 179-183 (Davidow, Dep.); CX1022 at 1 (Davidow April 1998 email: "I am concerned that Mike [Farmwald] may be right although I would prefer a more measured approach.")). Mr. Davidow suggested that Rambus "try to negotiate something" with Intel. (CX1022 at 2). Mr. Davidow believed that negotiations would gain time, during which Rambus could postpone asserting its intellectual property rights against DRAM manufacturers. (*Id.* ("The advantage of trying to negotiate something with them is that it will take months. In the process we gain time. We will not have to play the intellectual property card with Micron and SDRAMs during this time.")). He noted that if negotiations with Intel did not work, Rambus could still assert its intellectual property rights. (*Id.* ("If things blow up with Intel, then we can begin to pursue the intellectual property issue with these guys. That will get Intel really mad but they will already be really mad."); CX2109 at 183 (Davidow, Dep.)).

Rambus's Response to Finding No. 1875:

Rambus has no specific response.

1876. Richard Crisp believed that if Rambus's failed to meet Intel's performance standard, then Rambus would lose its "one and only chance for world dominance." (CX0656 at 1).

Rambus's Response to Finding No. 1876:

The proposed finding is irrelevant, but it is also undisputed that Rambus *did* meet Intel's performance standards, and *did* design the most cost-effective DRAM, as Intel's Peter MacWilliams testified at trial:

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(MacWilliams, Tr. 5075 (*in camera*)).

G. Technical Problems and Product Delays Caused RDRAM to "Lose Momentum and Collapse."

1877. Technical difficulties and the delay of Intel's supporting chipset eventually caused RDRAM to "lose momentum and collapse." (Tabrizi, Tr. 9221 (Hyundai executive Farhad Tabrizi: "the failure of Rambus was exclusively the Rambus difficulty in design and Intel failure to deliver Camino in time. . . . All the technical difficulties they had and the not readiness of the market and Intel chipset caused Rambus to lose momentum and collapse."); CCFF 1878-94)).

Rambus's Response to Finding No. 1877:

Mr. Tabrizi has neither the foundation nor the credibility to testify about Intel's alleged problems with the Camino chipset, for the reasons set out in detail in RRFF 1802 and 1840-41.

1878. The Camino Chipset, also called the Intel 820 Chipset, "was the first chipset that Intel was developing to interface between their processor and direct Rambus." (MacWillaims, Tr. 4853; Tabrizi, Tr. 9166, 9185). The Camino Chipset was intended to interface exclusively with RDRAM. (Tabrizi, Tr. 9185-86).

Rambus's Response to Finding No. 1878:

Rambus has no specific response.

1879. From 1998 though 2000, "Intel continuously had problem[s] with the Camino Chipset." (Tabrizi, Tr. 9185 (The Camino Chipset "never really materialized in terms of the technology.")).

Rambus's Response to Finding No. 1879:

Mr. Tabrizi has neither the foundation nor the credibility to testify about Intel's alleged problems with the Camino chipset, for the reasons set out in detail in RRFF 1802 and 1840-41.

1880. In the second half of 1998, Intel encountered electrical issues with RDRAM. (RX1532 at 2 (Intel timeline: "2H'98 . . . Electrical side created several issues which were found late in the process"); MacWilliams, Tr. 4852-53 ("we expected these things to have been sorted out way back in the time where we had test chips or even before we had out direct RDRAM").

Rambus's Response to Finding No. 1880:

The proposed finding is irrelevant and inappropriate for all the reasons set out in detail at RRFF 1840-41.

1881. Technical problems with RDRAM forced Intel to delay the Camino Chipset launch several times. (MacWilliams, Tr. 4852-53; Tabrizi, Tr. 9185 (Intel "canceled their schedule of launch many times. At one time they introduced and then they had to pull back and recall all the boards.")).

Rambus's Response to Finding No. 1881:

Mr. Tabrizi has neither the foundation nor the credibility to testify about Intel's alleged problems with the Camino chipset, for the reasons set out in detail in RRFF 1802 and 1840-41.

1882. In February 1999, Intel had to postpone its June 1999 target launch date until October 1999. (MacWilliams, Tr. 4852-53; CX2338 at 57 ("Feb. '99 . . . Intel 820 chipset launch delayed").

Rambus's Response to Finding No. 1882:

This proposed finding is not probative, because it does nothing to explain why DDR SDRAM, rather than RDRAM, became the predominant main memory. It is undisputed that the design and ramp up phases of DDR SDRAM's launch were plagued with delays and difficulties. (Reczek, Tr. 4349-51 (transition to DDR was a "major change," and Infineon had to implement three "major redesigns" before it could achieve "acceptable" performance); Shirley, Tr. 4208-09 {

} **(*in camera*).**

1883. In March 1999, technical problems caused Intel to internally reevaluate its exclusive support of RDRAM and begin investigating alternative DRAMs. (CX2527 at 2 (March 1999 email: "Summary: Most aspects of the Rambus transition have been more difficult than we anticipated. To that end, we believe that a strategy that puts our chipset and value processor line dependent, solely, on Rambus is no longer viable. Furthermore, the SDRAM 133 technology appears to be a relatively low risk approach for the DRAM manufacturers, and at least one chipset company (VIA) is already sampling a part that utilizes this higher speed technology.")).

Rambus's Response to Finding No. 1883:

The proposed finding is irrelevant, misleading and grossly misstates the only evidence it cites. There is *nothing* in the cited exhibit to suggest that the reevaluation was caused by "technical problems," as the finding states.

1884. In April 1999, Intel's microprocessor rival, Advanced Micro Devices, suspended development work on its RDRAM product due to "continuing bad news about RDRAM." (CX2158 at 2 ("(i820 delayed launch, low RDRAM yields)"); Heye, Tr. 3799; 3704-05 (in late summer of fall of 1998 AMD shifted its focus to DDR because Mr. Heye believed "Rambus was going to fail as a commodity part, and that ultimately even Intel would have to go DDR")).

Rambus's Response to Finding No. 1884:

The proposed finding is irrelevant and inappropriate for consideration for all the reasons set out in detail at RRFF 1840-41. Moreover, the author of the only cited exhibit, Steven Polzin, testified that the information in the exhibit about RDRAM costs and yields came "from what [he] was hearing from the memory manufacturers." (Polzin, Tr. 4013).

1885. In May 1999, Intel's customers were skeptical that the cost and availability issues with RDRAM could be resolved. (CX2529 at 1 (Intel May 1999 email: "OEMs skeptical that RDRAM issues will be resolved, some are waiting to see progress"); MacWilliams, Tr. 4884)).

Rambus's Response to Finding No. 1885:

The proposed finding is irrelevant and inappropriate for consideration for all the reasons set out in detail at RRFF 1840-41.

1886. In May 1999, Intel considered adding DDR to Intel's server memory roadmap because it was concerned that RDRAM would not "achieve the cost points in time to be competitive for the server products." (MacWilliams, Tr. 4883-84; CX2529 at 1 (Intel May 1999 email: "Is server memory strategy POR competitive, Do we need to add DDR on Intel server memory roadmap")).

Rambus's Response to Finding No. 1886:

The proposed finding is irrelevant and inappropriate for consideration for all the reasons set out in detail at RRFF 1840-41.

1887. Just before the Camino chipset launch in October 1999, Intel encountered another technical problem that caused an additional one month delay. (MacWillaims, Tr. 4852-53; CX2338 at 57; CX2338 at 79 ("Sep. '99: 820 chipset delayed again")).

Rambus's Response to Finding No. 1887:

The proposed finding is irrelevant and inappropriate for consideration for all the reasons set out in detail at RRFF 1840-41. Moreover, the cited documents and testimony do not state that any RDRAM-related problems caused the alleged delay.

1888. { } (CX2501 at 1, *in camera* ({ })).

Rambus's Response to Finding No. 1888:

The proposed finding is irrelevant and inappropriate for consideration for all the reasons set out in detail at RRFF 1840-41.

1889. { } (CX2501 at 1, *in camera* ({ })).

Rambus's Response to Finding No. 1889:

The proposed finding is irrelevant and inappropriate for consideration for all the reasons set out in detail at RRFF 1840-41.

1890. { } (CX0617 at 2, *in camera*).

Rambus's Response to Finding No. 1890:

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1891. In 1999, DRAM manufacturers were hesitant to ramp up production of RDRAM because Intel was continuously modifying the Rambus system, which increased the costs of production. (Tabrizi, Tr. 9188-9190; RX1425 at 2 ("some DRAM suppliers . . . said privately that they are reluctant to commit additional funds to the [RDRAM] ramp because of design changes that are still being made to the chip.")). Every time Intel changed the specifications for the Rambus system, DRAM manufacturers had to change the complete mask set at a cost of approximately one million dollars. (Tabrizi, Tr. 9190).

Rambus's Response to Finding No. 1891:

The proposed finding is irrelevant and inappropriate for consideration for all the reasons set out in detail at RRFF 1840-41.

1892. In 1999, customer demand for RDRAM was dwindling due to product delays. (Tabrizi, Tr. 9188 ("the demand for RDRAM was continuously being reduced due to delay and delay"); Appleton, Tr. 6371-72 ("There were quite a few delays in the development of [RDRAM]"); CX2338 at 79 ("820 chipset delayed again"); RX1425 at 1 (Chou April 1999 email, quoting NEC Senior Vice President Shigeki Matsue: "Now that Intel has delayed the mass-market introduction of Direct Rambus, customer demand this year will be much lower than we expected.")).

Rambus's Response to Finding No. 1892:

The proposed finding is irrelevant and inappropriate for consideration for all the reasons set out in detail at RRFF 1840-41.

1893. In May 2000, Intel recalled the Camino motherboards due to a defect. (CX2338 at 79).

Rambus's Response to Finding No. 1893:

The proposed finding is irrelevant and inappropriate for consideration for all the reasons

set out in detail at RRFF 1840-41.

1894. In June 2000, Intel had major problems with Timna, another Intel chipset that interfaced with RDRAM, that delayed the Timna product launch. (CX2338 at 79; Tabrizi 9205-06).

Rambus's Response to Finding No. 1894:

The proposed finding is irrelevant and inappropriate for consideration for all the reasons set out in detail at RRFF 1840-41. In addition, Mr. Tabrizi has neither the necessary foundation nor the credibility to testify about Intel's purported problems with Timna. *See* RRFF 1802, 1840-41.

H. After Intel Stopped Exclusively Supporting Rambus, RDRAM's Projected Market Share Plummeted.

1895. In June 1999, Intel publically ceased its exclusive support of RDRAM and announced that the Pentium III chipset would support SDRAM. (Tabrizi, Tr. 9201-03; CX2338 at 57 ("Intel says PC133 SDR w/P-III is possible"); CX1077 at 1 (E. Kinsella, Intel to Back Alternative to Rambus Chips, street.com: "Ending months of speculation, Intel . . . embraced a low-cost alternative to Rambus-based . . . memory chips")). This was the first time Intel indicated that SDRAM could compete with RDRAM as the interface with Pentium III. (Tabrizi, Tr. 9201-03; CX2338 at 57).

Rambus's Response to Finding No. 1895:

The proposed finding is irrelevant and inappropriate for consideration for all the reasons set out in detail at RRFF 1840-41.

1896. In August 1999, Intel confirmed that it would provide support for SDRAM in the Pentium III chipset. (Tabrizi, Tr. 9201-03; CX2338 at 57 ("Intel confirms PC133 will be offered as alternative to D-RDRAM in P-III")).

Rambus's Response to Finding No. 1896:

The proposed finding is irrelevant and inappropriate for consideration for all the reasons set out in detail at RRFF 1840-41. Rambus also notes that the only cited exhibit is simply a

chart that Hyundai took from a newspaper article. It has no probative value. (Tabrizi, Tr. 9218).

1897. After Intel announced its support of SDRAM, Rambus's percentage of market penetration dropped because customers could choose between SDRAM and Rambus. (CX2338 at 57 (Hyundai document charting "Rambus's rocky road"); Tabrizi, Tr. 9203 ("at that time Intel confirmed that they're going to use PC133 . . . in P-III as an alternative to Rambus. As a result, the percentage of Rambus dropped again."); Tabrizi, Tr. 9208 ("at the beginning when Intel introduced they're going to use Rambus, the expectation was Rambus will be almost 80 percent of the market. With all the problems that Intel had and when Intel optioned the alternative, the Rambus penetration came down to maybe around 10 percent or lower than that.")).

Rambus's Response to Finding No. 1897:

The proposed finding is irrelevant and inappropriate for consideration for all the reasons set out in detail at RRFF 1840-41. Moreover, the cited exhibit is not a "Hyundai document," as the finding states. It is a chart from a newspaper article, with no probative value. (Tabrizi, Tr. 9218).

1898. During 1999 and 2000, Intel revised downward its estimates for the total available market ("TAM") for RDRAM multiple times. (CX2338 at 79 (chart depicting Intel's declining Rambus forecast); Tabrizi, Tr. 9193-97 (Hyundai executive Farhad Tabrizi: "from 1Q99 to 4Q2000, every time Intel came to us, they had to reduce their forecast")).

Rambus's Response to Finding No. 1898:

The proposed finding is irrelevant and inappropriate for consideration for all the reasons set out in detail at RRFF 1840-41.

1899. Intel reduced its forecast for RDRAM due to the "many challenges with Rambus." (CX2338 at 79; Tabrizi, Tr. 9185, 9198 (Hyundai executive Farhad Tabrizi: "at the earliest stages when Rambus signed an Intel development agreement the potential was very high. And then as time goes on and as Intel saw many challenges with Rambus, many technical difficulties with the chipset, then they decided to reduce the potential.")).

Rambus's Response to Finding No. 1899:

The proposed finding is irrelevant and inappropriate for consideration for all the reasons

set out in detail at RRFF 1840-41.

1900. In the first quarter of 1999, Intel met with Hyundai and projected that the total available market for RDRAM in the year 2000 would be 600 million pieces. (CX2338 at 79; Tabrizi, Tr. 9194-95).

Rambus's Response to Finding No. 1900:

The proposed finding is irrelevant and inappropriate for consideration for all the reasons set out in detail at RRFF 1840-41.

1901. Intel met with Hyundai again in September 1999 and dropped its year 2000 RDRAM projection to 500 million pieces. (CX2338 at 79; Tabrizi, Tr. 9194-96).

Rambus's Response to Finding No. 1901:

The proposed finding is irrelevant and inappropriate for consideration for all the reasons set out in detail at RRFF 1840-41.

1902. Intel and Hyundai had another meeting in the fourth quarter of 1999 and Intel dropped its year 2000 RDRAM projection to 300 million pieces. (CX2338 at 79; Tabrizi, Tr. 9194-96).

Rambus's Response to Finding No. 1902:

The proposed finding is irrelevant and inappropriate for consideration for all the reasons set out in detail at RRFF 1840-41.

1903. During a Hyundai-Rambus meeting in first quarter 2000, Intel's total available market estimate for RDRAM dropped to 250 million pieces. (CX2338 at 79; Tabrizi, Tr. 9194-96).

Rambus's Response to Finding No. 1903:

The proposed finding is irrelevant and inappropriate for consideration for all the reasons set out in detail at RRFF 1840-41.

1904. Intel also reduced its estimates for the total available market for RDRAM the second and third quarters of 2000. (CX2338 at 79).

Rambus's Response to Finding No. 1904:

The proposed finding is irrelevant and inappropriate for consideration for all the reasons set out in detail at RRFF 1840-41.

1905. Over the course of 1999 and early 2000, Intel's projections for total RDRAM available market plummeted from 600 million pieces to 250 million pieces. (Tabrizi, Tr. 9194-96; CX2338 at 79, (600 million forecast in first quarter 1999); CX2338 at 79 (500 million forecast in fall 1999); CX2338 at 79, (300 million forecast in fourth quarter 1999); CX2338 at 79 (250 million forecast in first quarter 2000)).

Rambus's Response to Finding No. 1905:

The proposed finding is irrelevant and inappropriate for consideration for all the reasons set out in detail at RRFF 1840-41. Rambus also notes that CCFF 1896-1905 are inherently unreliable because each relies solely and entirely upon *Hynix* documents and the testimony of *Hynix* executive Tabrizi, even though the findings purport to address *Intel's* motivations, strategy and concerns.

1906. Micron never introduced RDRAM into the market for commercial sale because customer demand for RDRAM did not materialize. (Appleton, Tr. 6371-6374). In the early stages of development, Micron's customers, particularly Dell computer, forecast a large consumption of RDRAM. (Appleton, Tr 6372-74). As Micron encountered challenges in the technology and delays, its customers "started to change their forecasts for consumption of RDRAM, and ultimately, it was at such a low level that it just wasn't worth it to try to take that to commercialization." (Appleton, Tr. 6372).

Rambus's Response to Finding No. 1906:

The proposed finding is irrelevant and inappropriate for consideration for all the reasons set out in detail at RRFF 1840-41. It should also be noted that Micron claimed credit for the lack of customer demand for RDRAM. (RX 1700 at 1; RX 1883 at 1).

1907. Micron did not take RDRAM into volume production because "it didn't get adopted by the market in a large percentage." (Appleton, Tr. 6319)

Rambus's Response to Finding No. 1907:

The proposed finding is irrelevant and inappropriate for consideration for all the reasons set out in detail at RRFF 1840-41. Micron claimed credit for the market's failure to adopt RDRAM. (RX 1700 at 1; RX 1883 at 1).

1908. Samsung, the world's largest DRAM producer, entered commercialization and full production of RDRAM. (Appleton, Tr. 6373).

Rambus's Response to Finding No. 1908:

Rambus has no specific response.

1909. Intel was not involved in the development of the initial SDRAM specifications. (CX2560 at 1 (MacWilliams July 2000 email: "PC133 specs were driven without us"); MacWilliams, Tr. 4911-13 ("other people in the industry [] proposed the spec changes from PC100 to make PC133 . . . and we weren't part of the loop initially.")).

Rambus's Response to Finding No. 1909:

The cited exhibits have nothing to do with the "initial SDRAM specifications" that are the subject of the proposed finding. The finding therefore has no support.

1910. As projections for RDRAM declined in the 1999-2000 time frame, the anticipated market share shifted to SDRAM and DDR SDRAM. (Tabrizi, Tr. 9214-15).

Rambus's Response to Finding No. 1910:

The proposed finding is irrelevant and inappropriate for consideration for all the reasons set out in detail at RRFF 1840-41.

I. Intel's Decision to Cease its Exclusive Support of RDRAMs and to Plan to Develop a Controller to Support SDRAMs and DDR SDRAMs Caused Rambus to Play the "IP Card."

1911. Between late 1996, when Intel decided to support RDRAM as its exclusive design for next generation main memory for personal computers, and October 1999, Rambus and Intel had a number of "blowup[s]." (Farmwald, Tr. 8419 ("This sort of blowup seemed to happen every one to two years with Intel. We had a number of these episodes."); Farmwald, Tr. 8423

(blowups "happened a lot")).

Rambus's Response to Finding No. 1911:

As explained below, the proposed finding and those that follow are misleading and incomplete. While Rambus does not dispute the cited testimony, the inference Complaint Counsel hopes to draw from these findings is unfounded. (*See* RRFF 1919).

1912. By September 1999, Intel engineers were very frustrated with Rambus. (CX2535 at 1 (September 1999 MacWilliams email: "we want to do a change to make cost better or enhance performance, if RDRAM is already established Rambus will likely use this as an excuse to generate more $$ for themselves."); CX2537 at 1 (September 1999 Ahmad email: "Samsung has done more work in debugging and ramping this technology then Rambus"); CX2536 at 1 (September 1999 Ahmad email: "other concern is that Rambus will use this as an opportunity to potentially gouge more $$")).

Rambus's Response to Finding No. 1912:

The proposed finding is misleading and incomplete. First, none of the cited documents speak to the issue of the frustration of Intel's engineers. CX2535 is an email discussion between Intel employees about proposed changes to Rambus's royalty structure for RDRAM and has nothing to do with "Intel's engineers" and is not evidence of frustration with Rambus. Likewise, CX2537 references Samsung's desire to have a lower royalty due to its debugging efforts on RDRAM and CX2536 reference Intel's desire to make the call on forward compatibility by itself (which would make RDRAM no longer "open"). Neither expresses the views of either company's engineers, but rather involves executive level discussions and contract negotiations.

1913. { } (CX2503 at 2, *in camera* ({ }); MacWilliams, Tr. 5073-74, *in camera* ({ })).

Rambus's Response to Finding No. 1913:

The proposed finding is incomplete. The cited evidence demonstrates that the coordinated actions and misrepresentations of the DRAM manufacturers had started to have their intended effects. (*See* RRFF 1802, 1808, 1813, 1840).

1914. By mid-October 1999, Intel's road map included SDRAM and DDR SDRAM solutions. (CX2540 at 1 (October 1999 MacWillaims email: "making RDRAM work does not solve the business issues Rambus is causing in the industry. Result is that we will not convert our roadmap 100% to RDRAM. In DT we continue to have SDRAM. In server we will try DDR. If the situation continues we will keep alternatives alive indefinitely.")).

Rambus's Response to Finding No. 1914:

The proposed finding is misleading and incomplete. The cited document states that Intel planned to use DDR only for servers. In February 2001, nearly a year and half later, Intel was still telling the world that its memory strategy was to shift from SDRAM to RDRAM in the far larger and more lucrative desktop space. (RX 1762 at 4). According to Intel's presentation at the Intel Developer Forum, Spring 2001, RDRAM was "[t]he best solution," the "[b]est technology for the Intel Pentium 4 Processor Platform," and "RDRAM Remains the Primary Desktop Memory Solution." (RX 1762 at 5). In its summary, Intel stated, "RDRAM Provides the Best Pentium 4 Processor Platform Now and in the Future." (RX 1762 at 24). According to Pete MacWilliams of Intel, this statement accurately summarized Intel's position as of February 2001. (MacWilliams, Tr. 4935).

1915. In late October 1999, Intel told Rambus that it wanted to have a comprehensive review of their business relationship. (CX2887 at 1 (October 26, 1999 letter from Gelsinger to Tate: "Events over the past several months, including changes within the global memory industry and changes in customer demand for memory products, lead us to believe that it is important for Intel and Rambus to conduct a very serious and comprehensive review of our current relationship")).

Rambus's Response to Finding No. 1915:

Rambus has no specific response.

1916. On October 26, 1999, Pat Gelsinger of Intel sent a letter to Messrs. Tate and Davidow highlighting many of Intel's concerns with Rambus. (CX2887 at 1-3; CX2109 at 201-202, 204 (Davidow, Dep.) ("Intel had lots of complaints about how things were going")). Intel believed that industry acceptance of RDRAM technology was "poor, at best" and blamed Rambus for failing to support Intel's efforts to promote RDRAM. (CX2887 at 1-2) ("Our customers are rapidly losing confidence in us and in the technology, largely due to the lack of total, prioritized support from Rambus."). Intel was also frustrated because Rambus had "grossly missed" its commitments in terms of projected cost reductions. (CX2887 at 1) (Rambus's original commitment of achieving #5% parity with SDRAM on cost has been grossly missed.).

Rambus's Response to Finding No. 1916:

The proposed finding is incomplete. Despite Intel's concerns, Intel still believed that RDRAM was the best platform for its processors, planned to switch to RDRAM for its desktop computers, and continued to believe and plan in this manner until at least February 2001. (*See* RRFF 1914).

1917. Intel announced in its October 26, 1999 letter to Rambus that its chipset roadmap now included alternatives to RDRAM. (CX2541 at 2; CX2887 at 2-3 ("Intel has been forced to re-architect its chipset roadmap to accommodate additional SDRAM products as a direct result of Rambus's failure to adequately deal with the issues outline above. . . . we have no choice but to continue re-assessing our chipset road map")).

Rambus's Response to Finding No. 1917:

The proposed finding is misleading and incomplete. Intel still believed that RDRAM was the best platform for its processors, planned to switch to RDRAM for its desktop computers, and continued to believe and plan in this manner until at least February 2001. (*See* RRFF 1914).

1918. { } (CX1080 at 1). {

} (CX1080 at 2).

Rambus's Response to Finding No. 1918:

The proposed finding is misleading and incomplete. The cited document states that Intel changed its roadmap "{ }." (CX 1080 at 2). Intel still believed that RDRAM was the best platform for its processors, planned to switch to RDRAM for its desktop computers, and continued to believe and plan in this manner until at least February 2001. (*See* RRFF 1914).

1919. In October 1999, after reviewing the situation with Intel, Rambus decided to be "proactive" with DRAM manufacturers regarding its SDRAM and DDR-SDRAM related intellectual property. (CX1379 at 4 ("Since 1996 we assumed Intel would drive a rapid transition from SDRAM to Rambus, Before we chose 'not to rock the boat' if all would be Rambus in 2-3 years, [Now] Intel has shifted to 'let the market decide,' is enabling DDR, and may be working on DRAM 2003, We must be proactive on our IP with DRAM companies")

Rambus's Response to Finding No. 1919:

The proposed finding is misleading and incomplete. First, the cited document states that Rambus planned to become "proactive on our IP," not as the proposed finding would have it, "'proactive' with DRAM manufacturers regarding SDRAM and DDR-SDRAM related intellectual property." The distinction is important: As used by Rambus, the phrase refers to stepped up prosecution of relevant patent claims (which occurred in late 1999) and to initial steps to prepare to send out formal notices of infringement on those patents that were infringed by SDRAM and DDR-SDRAM devices, which began at the same time. Second, the phrase "after reviewing the situation with Intel" is misleading as it implies a cause-and-effect relationship that is not supported by the cited evidence or other evidence that this proposed finding ignores. The evidence shows that "the situation with Intel" was not – as this proposed

finding implies – in some sort of crisis in October 1999. Indeed, even over a year later, Intel was still promoting RDRAM as the best platform for its processors and it still planned to switch to RDRAM for its desktop computers. Intel continued to believe and plan in this manner until at least February 2001. (*See* RRFF 1914). Rambus's first patents that were necessarily infringed by SDRAM and DDR-SDRAM devices issued in late 1999. (*See* Stipulation at Attachment A). The evidence shows that Rambus simply began seeking to license these patents soon after they issued. Prior to that time, there were no Rambus patents that were necessarily infringed by any JEDEC standard Nor did Rambus believe to the contrary. In 1997, Rambus was concerned that DDR products might infringe its patents. Geoff Tate had written in a 1997 email that the DDR products "*might* infringe" Rambus's issued and in process patents, "but with so little hard data and no silicon there are no patents that we can definitely say are infringed." (CX 919 at 1). Mr. Tate's instructions therefore had been to ""get hard data . . . and reassess periodically but wait on action until we see silicon." (*Id.*) The convergence of "hard data" and Rambus patents that covered SDRAM and DDR-SDRAM did not occur until late 1999, just prior to Rambus seeking to enforce its newly acquired rights.

Finally, the selective quotation from the only cited evidence, CX 1379, to suggest the cause-and-effect relationship where none exists. The full page of CX 1379 at 4 reads as follows with the removed text in italics.

Rambus IP for High Bandwidth DRAM

- *We have fundamental patents on high bandwidth DRAM*
- Since 1996 we assumed Intel would drive a rapid transition from SDRAM to Rambus

- *We think Rambus is the best solution long term*
- Before we chose "not to rock the boat" if all would be Rambus in 2-3 years
- Intel has shifted to "let the market decide," is enabling DDR, and may be working on DRAM 2003
- We must be proactive on our IP with DRAM companies

The cited exhibit mentions nothing about being proactive with DRAM companies about "SDRAM" or "DDR-SDRAM." In fact, the particular bullet point is not specifically linked to any DRAM technology: it comes under the heading "High Bandwidth DRAM."

1920. In October 1999, Rambus's executives and Board of Directors discussed which company to approach first about enforcing Rambus's SDRAM and DDR SDRAM related patents. (Farmwald, Tr. 8416-17; Farmwald, Tr. 8239-40; CX0623 at 4 (October 1999 Board Meeting minutes: "Mr. Karp reviewed various strategic IP issues including target selection and a negotiation timeline."); CX2109 at 199-200 (Davidow, Dep.) ("Q. What do you understand these minutes to be referring to when they use the term 'target selection'? . . . [A.] those referred to who we were going to sit down and press extremely hard on in negotiation and what sequence we were going to talk with them and who we would litigate with and in what order if we were forced to litigate.")).

Rambus's Response to Finding No. 1920:

The proposed finding is misleading and incomplete. (*See* RRFF 1919).

1921. In November 1999, Rambus was strengthening its patent portfolio and assembling a patent prosecution team. (CX1085 at 1 ("congrats to Neil Steinberg for successful prosecution of another addition to our Strategic Patent Portfolio"); CX1083 at 1 (introducing "Lexington" program); CX1353 at 7 ("Portfolio 1: SDRAM/DDR/Controllers all infringe, Lexington initiated")).

Rambus's Response to Finding No. 1921:

The proposed finding is misleading and unsupported. The cited documents at most suggest that Rambus believed its patent portfolio was strengthened by the issuance of two new patents in November 1999. Nothing in the cited documents speaks to the issue of "assembling a

patent prosecution team"; Neil Steinberg was already a Rambus employee. To be accurate the proposed finding should read: "In November 1999, two patents issued to Rambus relating to SDRAM/DDR/Controllers. In the same month, Rambus initiated sought to enforce those patents."

1922. In November 1999, Richard Crisp, Rambus's primary JEDEC representative joked about enforcing Rambus's DDR-related patents for "Double DRAM Royalties." (CX1084 at 1 (Crisp November 1999 email: "ddr meaning, here is what it currently means: Desperate to Destroy Rambus, it will prove to mean: Didn't Destroy Rambus, and in a year or two: Double DRAM Royalties (for Rambus)")).

Rambus's Response to Finding No. 1922:

The proposed finding is misleading. In November 1999, Rambus had not attended JEDEC for almost four years (CCFF 867), and it had no JEDEC representative.

1923. In December 1999, Intel and Rambus conducted another operations review. (CX2546 at 1). Intel was "very disappointed" with Rambus's presentation, which Intel believed contained "significant misrepresentations and self-serving commentary." (*Id.*) Intel was most upset by Rambus's failure to mention the "two most fundamental reasons why the ramp of RDRAM technology" proceeded slower than expected: technical problems and cost issues. (CX2546 at 2)).

Rambus's Response to Finding No. 1923:

The proposed finding is incomplete and mischaracterizes the evidence in a way that overstated Intel's disappointment. The cited document does not state that "Intel was most upset" but that "[p]erhaps most disappointing from [Intel's] perspective is … ." (CX2546 at 2). Further, the cited document demonstrates that the coordinated actions and misrepresentations of the DRAM manufacturers had started to have their intended effects. (*See* RRFF 1802, 1808, 1813, 1840). Nonetheless, Intel was still presenting RDRAM as the best solution for desktop computers as of February 2001. (*See* RRFF 1914).

1924. { } (CX1418 at 112, *in camera*; CX1379 at 4; CX1355 at 127 ("Rambus has substantial IP and has an obligation to shareholders to get a return on the investment")).

Rambus's Response to Finding No. 1924:

The proposed finding is incomplete and misleading. Rambus's first patents that covered technologies in SDRAM and DDR issued in late 1999. (*See* Stipulation at Attachment A). The evidence shows that Rambus simply began enforcing its patents soon after they issued. Prior to that time, Rambus had no patents that were necessarily infringed by SDRAM or DDR products. (*See* RRFF 1919).

1925. Paragraphs 1925 - 1949 are unused.

X. Rambus Has Acted to Enforce U.S. and Foreign Patents with Respect to Technologies Incorporated in the JEDEC SDRAM and DDR SDRAM Standards.

A. Beginning in 1999, Rambus Asserted that its U.S. and Foreign Patents Covered Use of Programmable CAS Latency and Burst Length, On-Chip DLL and Dual Edge Clocking in JEDEC-Compliant SDRAMs and DDR SDRAMs.

1950. In late 1999, Rambus began informing DRAM manufacturing companies that their SDRAM and DDR SDRAM products might infringe Rambus patents. (Rambus Answer at 38-39, ¶ 92 ("Rambus admits that, in or about November 1999, it began contacting certain memory manufacturers to notify them that, based on analyses of the datasheets of products made by those companies, Rambus believed those products infringed certain of Rambus patents"); CCFF 1953-58)).

Response to Finding No. 1950:

The proposed finding is misleading and not supported by the evidence. As written, it suggests that before 1999, Rambus never informed DRAM manufacturing companies that their SDRAM or DDR SDRAM products might infringe Rambus intellectual property. However, Rambus has not asserted any patents against DRAM manufacturers that issued before June 1999. (Parties First Set of Stipulations, Attachment A). Rambus had previously informed various DRAM manufacturers and others that SDRAM and DDR SDRAM might infringe future Rambus patents. (RPF 549-55). In late 1999, Rambus began informing DRAM manufacturers that Rambus had issued patents that Rambus believed were infringed by certain SDRAM and DDR SDRAM products.

1951. Rambus believes its patents cover SDRAM and DDR SDRAM. (CX1353 at 7 ("Intellectual Property . . . Strategic Patent Portfolio 1: SDRAM/DDR/Controllers all infringe"); CX1382 at 33 ("Non-Compatible License Terms, All agreements cover SDRAM, DDR and logic ICs which control these memories"); CX1364 at 1-2, *in camera* ({

}).

Response to Finding No. 1951:

The proposed finding is vague, misleading, and unclear as to the time period it refers to. The evidence supports only a finding that *by October 1999* Rambus believed that *certain* of its patents covered SDRAM and DDR SDRAM products; all of the presentations cited by Complaint Counsel are in or after November 1999.

1952. As of November 2000, Rambus President Mooring testified that Rambus believed every SDRAM device it examined violated Rambus patents. (CX2055 at 265 (Mooring, Dep.)). In a later deposition in February 2001, Mr. Mooring testified that he was unaware of any firms making SDRAMs or DDR SDRAMs as to which Rambus would not claim patent protection. (CX2066 at 13-14 (Mooring, Dep.)).

Response to Finding No. 1952:

Rambus has no specific response.

1953. In late 1999, Rambus told Hitachi that it believed Hitachi's SDRAM and DDR SDRAM products infringed Rambus's patents. Rambus gave a presentation to Hitachi detailing which Hitachi products it believed infringed various Rambus patents. (CX2102 at 445-47 (Karp, Dep.)).

Response to Finding No. 1953:

The proposed finding is overly broad. As noted in Response to Proposed Finding No. 1951, Rambus only believed that Hitachi's SDRAM and DDR SDRAM products infringed "certain" of its patents.

1954. In April 2000, Rambus told Mitsubishi that it believed Mitsubishi's SDRAM and DDR SDRAM products infringed Rambus's patents. (CX1109 at 1 (April 3, 2000 letter: "Rambus owns patents that are directed to various aspects of, and features implemented in Single Data Rate and Double Data Rate SDRAMs, and Cache DRAMs ('CDRAMs'). . . . We wish to meet with Mitsubishi to discuss these patents and allowed applications in connection with Mitsubishi's SDRAMs and CDRAMs."); Crisp, Tr. 3435-3436).

Response to Finding No. 1954:

The proposed finding is overly broad. As noted in Response to Proposed Finding No. 1951, Rambus told Mitsubishi that it believed that Mitsubishi's SDRAM and DDR SDRAM products infringed "certain" of its patents.

1955. In April 2000, Rambus told NVidia that it believed NVidia products that interfaced with SDRAM and DDR infringed Rambus patents. (CX1371 at 3, 8) (chart: "Rambus IP - NVidia Product Line Overview"). { } (CX1359 at 1, *in camera* ({ })).

Response to Finding No. 1955:

The proposed finding is overly broad. As noted in Response to Proposed Finding No. 1951, Rambus told nVidia that it believed that nVidia's SDRAM and DDR SDRAM products infringed "certain" of its patents.

1956. In June 2000, Rambus informed Hyundai that it believed Hyundai's SDRAM and DDR SDRAM products infringed Rambus's patents. (CX1129 at 1 (June 23, 2000 facsimile: "We have reviewed Hyundai's memory product line and we believe that many of your products infringe one or more claims of the above-identified patents."); Crisp, Tr. 3435-3436). Rambus also attached a chart detailing which Hyundai DDR and SDRAM products it believed infringed various Rambus patents. (CX1129 at 1-4 ("To facilitate your consideration of this matter, we have attached a chart summarizing our preliminary position by Rambus patents and Infineon product.")).

Response to Finding No. 1956:

The proposed finding is overly broad. As noted in Response to Proposed Finding No. 1951, Rambus told Hyundai only that it believed that Hyundai's SDRAM and DDR SDRAM products infringed "certain" of its patents.

1957. In June 2000, Rambus informed Infineon that it believed Infineon's SDRAM and DDR SDRAM products infringed Rambus's patents. (CX1127 at 1 (June 23, 2000 facsimile: "We have reviewed Infineon's memory product line and we believe that many of your products

infringe one or more claims of the above-identified patents.")). Rambus also attached a chart detailing which Infineon SDRAM and DDR products it believed infringed various Rambus patents. (CX1127 at 1-2 ("To facilitate your consideration of this matter, we have attached a chart summarizing our preliminary position by Rambus patent and Infineon product.")).

Response to Finding No. 1957:

The proposed finding is overly broad. As noted in Response to Proposed Finding No. 1951, Rambus told Infineon only that it believed that Infineon's SDRAM and DDR SDRAM products infringed "certain" of its patents.

1958. In or about June 2000, Rambus informed Samsung and other memory manufacturers that it believed their SDRAM and DDR SDRAM products infringed Rambus's patents. (Rambus Answer at 38, ¶ 92; CX2559 at 3).

Response to Finding No. 1958:

The proposed finding is overly broad. As noted in Response to Proposed Finding No. 1951, Rambus told Samsung and "certain" other memory manufacturers only that it believed that Samsung's SDRAM and DDR SDRAM products infringed "certain" of its patents.

1959. Rambus has asserted patents against JEDEC-member companies using programmable CAS latency, programmable burst length, on-chip DLL and dual edge clock technologies in JEDEC-compliant SDRAMs, SGRAMs, DDR SDRAMs and DDR SGRAMs, as well as memory controllers that interface with them. (CCFF 1960-67).

Response to Finding No. 1959:

The proposed finding is misleading and is not supported by the facts. Complaint Counsel has not established which if any SGRAMs, DDR SDRAMs, DDR SGRAMs, or memory controllers that interface with them, are in fact "JEDEC-compliant." Indeed, Mr. Becker of Infineon testified that, although it was his responsibility to confirm JEDEC compliance for Infineon's parts, he could not testify to it. (Becker, Tr. 1174-8; *see also* RPF 116).

1960. Rambus has asserted that its innovations include "Programmable latency register on a SDRAM," "Programmable burst techniques implemented on a SDRAM," "DLL implemented on a SDRAM," and "Double data rate." (CX1371 at 5; CX1383 at 4; *see also* CX1363 at 1).

Response to Finding No. 1960:

Rambus has no specific response.

1961. Rambus has asserted that "programmable latency on a DRAM" and "Programmable burst on a DRAM," as used in SDRAMs, are Rambus innovations covered by its patents. (CX1363 at 3).

Response to Finding No. 1961:

The proposed finding is misleading and not supported by the evidence. Complaint Counsel cite to shorthand in a presentation slide that cannot reasonably be interpreted as an assertion of patent coverage. Rambus has asserted that certain of its patent claims cover certain SDRAMs because those SDRAMs contain each and every limitation of those claims.

1962. Rambus has asserted that "programmable latency on a DRAM," "Programmable burst on a DRAM," "DLL implemented on a DRAM" and "Double data rate," as used in DDR SDRAMs, are Rambus innovations covered by its patents. (CX1363 at 3).

Response to Finding No. 1962:

The proposed finding is misleading and not supported by the evidence. Complaint Counsel cite to shorthand in a presentation slide that cannot reasonably be interpreted as an assertion of patent coverage. Rambus has asserted that certain of its patent claims cover certain DDR SDRAMs because those DDR SDRAMs contain each and every limitation of those claims.

1963. Rambus has asserted that its issued patents cover programmable CAS latency, as described and depicted in JEDEC SDRAM and DDR SDRAM data sheets and individual company data sheets. (CX1371 at 46, 53 (demonstrating that the phrase "value which is representative of a time delay after which the memory device responds to a read request" in

claim 44 of Rambus's '365 patent corresponds to the CAS latency portion of the mode register diagram in the JEDEC 64M DDR SDRAM Data Sheet); CX1383 at 47, 51 (same); *id*. at 20, 23 (demonstrating that same language from claim 23 of Rambus's '195 patent corresponds to the CAS latency portion of the mode register in Micron's 16M SDRAM Datasheet); *id*. at 41, 44 (similar language from Rambus's '918 patent compared to the CAS latency portion of Micron's 16M SDRAM Datasheet)).

Response to Finding No. 1963:

The proposed finding is not supported by the evidence and is misleading to the extent it implies that Rambus has asserted that it has patents that cover SDRAM and DDR SDRAM memory devices based on JEDEC data sheets. The cited documents were used in licensing discussions with manufacturers of graphics chips, not memory devices. (CX 1371 at 8; CX 1383 at 6).

1964. Rambus also disclosed to NVidia the specific language of a claim in a pending patent application – claim 190 of its application no. 09/357,989. Rambus demonstrated how the elements of that claim correspond to specific elements of the JEDEC 64M DDR SDRAM Data Sheet, including the functional block diagram and the mode register diagram of that JEDEC data sheet. (CX1371 at 33-36, 35 (demonstrating that the term "value" in the element "a value which is representative of a number of clock cycles of a first external clock signal to transpite before data is output by the memory device" in claim 190 corresponds to the CAS latency portion of the mode register diagram in the JEDEC 16M DDR SDRAM Data Sheet.)

Response to Finding No. 1964:

The proposed finding is incomplete and misleading. Application no. 09/357,989 issued as United States Patent No. 6,067,592 on May 23, 2000, about a month after the presentation to NVidia in question. (CX1530 at 1; CX1371 at 1). Thus, when Rambus disclosed the language of a claim to NVidia, it was well after the time that that Rambus would have received notification from the PTO that the claim had been allowed and would shortly issue. (*See* CCFF 1076, 1077 (noting that Rambus received a Notice of Allowance from the PTO for the '646 application on October 6, 1995, over six months before the resulting patent, the '327 patent,

issued on April 30, 1996)).

1965. Rambus has asserted that its issued patents cover programmable burst length, as described and depicted in JEDEC SDRAM and DDR SDRAM data sheets and individual company data sheets. (CX1371 at 64, 68 (demonstrating that the phrase "a first amount of data to be output onto a data bus in response to a read request" in claim 1 of its '214 patent corresponds to the burst length portion of the mode register diagram in the JEDEC 64M DDR SDRAM Data Sheet); CX1383 at 60, 64 (same); *id*. at 31, 36 (demonstrating that similar language from Rambus's '918 patent corresponds to the burst length portion of the mode register in Micron's 16M SDRAM Datasheet)).

Response to Finding No. 1965:

The proposed finding is not supported by the evidence and is misleading to the extent it implies that Rambus has asserted that it has patents that cover SDRAM and DDR SDRAM memory devices based on JEDEC data sheets. The cited documents were used in licensing discussions with manufacturers of graphics chips, not memory devices. (CX 1371 at 8; CX 1383 at 6).

1966. Rambus has asserted that its issued patents cover on-chip DLL as depicted in JEDEC SDRAM and DDR SDRAM data sheets. (CX1371 at 84-85 (demonstrating that the term "delay locked loop" in claim 11 of its '214 patent corresponded to the indication "DLL" in the functional block diagram of the JEDEC 64M DDR SDRAM Data Sheet)).

Response to Finding No. 1966:

The proposed finding is not supported by the evidence and is misleading to the extent it implies that Rambus has asserted that it has patents that cover SDRAM and DDR SDRAM memory devices based on JEDEC data sheets. The cited documents were used in licensing discussions with manufacturers of graphics chips, not memory devices. (CX 1371 at 8; CX 1383 at 6).

1967. Multiple witnesses have testified that Rambus has asserted that its patents cover use of programmable CAS latency, programmable burst length, on-chip DLL and dual edge clock in JEDEC-compliant SDRAMs and DDR SDRAMs. (Lee, Tr. 6776-77; Rhoden, Tr. 529-

531). {

} (CX1384 at 1-5, *in camera*; Macri, Tr. 4753-55, *in camera*). {

} (Macri, Tr. 4756, *in camera*).

Response to Finding No. 1967:

This proposed finding is misleading. {

} (Macri, Tr. 4756, *in camera*).

1968. Rambus has also asserted that its issued foreign patents cover use of programmable CAS latency, programmable burst length, on-chip DLL and dual edge clock in JEDEC-compliant SDRAMs and DDR SDRAMs. (Bechtelsheim, Tr. 5884-85; CCFF 1969-74).

Response to Finding No. 1968:

This proposed finding is incomplete and misleading. The evidence cited shows only that Rambus has asserted that *certain* of its issued foreign patents cover use of programmable CAS latency, programmable burst length, on-chip DLL and dual edge clock in *certain* SDRAMs and DDR SDRAMs.

1969. In a presentation involving Rambus's foreign patents, Rambus matched elements of claim 1 of its European Patent No. EP 0525068 B1 to portions of Infineon's 256M DDR SDRAM Datasheet that illustrated the DDR SDRAM's mode register, the storing of CAS latency information in the mode register and the timing of data output following the CAS latency. (CX1268 at 1-8).

Response to Finding No. 1969:

Rambus has no specific response.

1970. In a presentation involving Rambus's foreign patents, Rambus matched elements of claim 5 of its European Patent No. EP 0525068 B1 to portions of Infineon's 256M DDR SDRAM Datasheet that illustrated the DDR SDRAM's delay lock loop. (CX1268 at 13-14).

Response to Finding No. 1970:

Rambus has no specific response.

1971. The block diagram from the Infineon 256 DDR SDRAM Datasheet used by Rambus to match elements of claims 1 and 5 of European Patent No. EP 0525068 B1 is nearly identical to a functional block diagram contained in the DDR SDRAM specification JESD 79. (CX1268 at 4, 14; JX0057 at 8).

Response to Finding No. 1971:

The proposed finding is irrelevant. In addition, the proposed finding is vague in its use of the term "nearly identical." Complaint Counsel has made no showing of the significance, or lack thereof, of the two block diagrams cited.

1972. In a presentation involving Rambus's foreign patents, Rambus matched elements of claim 1 of its European Patent No. EP 0525068 B1 to portions of Micron's 64M DDR SDRAM Datasheet that illustrated the DDR SDRAM's mode register, the storing of CAS latency information in the mode register and the timing of data output following the CAS latency. (CX1269 at 1-8, 22-28, 37-44, 57-63).

Response to Finding No. 1972:

Rambus has no specific response.

1973. In a presentation involving Rambus's foreign patents, Rambus matched elements of claim 5 of its European Patent No. EP 0525068 B1 to portions of Micron's 64M DDR SDRAM Datasheet that illustrated the DDR SDRAM's delay lock loop. (CX1269 at 13-14, 48-49).

Response to Finding No. 1973:

Rambus has no specific response.

1974. The block diagram from the Micron 64M DDR SDRAM Datasheet used by Rambus to match elements of claims 1 and 5 of European Patent No. EP 0525068 B1 is nearly identical to a functional block diagram contained in the DDR SDRAM specification JESD 79. (CX1269 at 4, 14; JX57 at 9).

Response to Finding No. 1974:

The proposed finding is irrelevant. In addition, the proposed finding is vague in its use of the term "nearly identical." Complaint Counsel has made no showing of the significance, or lack thereof, of the two block diagrams cited.

B. Rambus Has Pursued a Strategy of Licensing DDR SDRAMs Only at Royalty Rates Higher than Those Charged for RDRAMs, in Order to Discourage Use of DDR SDRAMs.

1975. Part of Rambus's licensing strategy for SDRAM and DDR SDRAM was to approach Asian DRAM manufacturers first. (CX1273 at 5, *in camera* ({

}); CX1273A at 6 ("Timeline" listing presentations to "Major Asian DRAM companies" before presentations to U.S. and European DRAM companies); CX1273A at 12 (work schedule discussing "Asian exec presentations")).

Response to Finding No. 1975:

This proposed finding is irrelevant.

1976. Rambus also initially targeted companies that were not supportive of RDRAM. (CX1366 at 5 (February 2000 Rambus Presentation: "Rambus IP . . . Initial focus is on those companies not helping to grow RDRAM market")).

Response to Finding No. 1976:

The proposed finding is misleading, not supported by the evidence, and incomplete. The exhibit cited by Complaint Counsel discusses the "initial focus" of Rambus's licensing efforts. Complaint Counsel's rephrasing of this to "initially targeted" suggests litigation. The preceding bullet point, however, states, "Rambus willing to license technology for non-RDRAM use at reasonable rates." (CX 1366 at 5). It is clear from the next bullet point in the same section of the cited document that litigation would commence "only in cases of unwillingness to negotiate" without reference to which companies were or were not helping to grow the RDRAM market.

(CX 1366 at 5). The document further cites Rambus's willingness to license as its long term strategy; under "Rambus: 2000 and Beyond," the document states, "Rambus will license IP for non-compatible uses." (CX 1366 at 6).

1977. Through its licensing strategy, Rambus sought to reduce the competitive threat that SDRAM and DDR SDRAM posed to RDRAM. (CX1097 at 2 (Tate January 2000 email: one way to convince DRAM companies to pay royalties on RDRAM is to "reduce attractiveness of alternatives"); CX1115 at 3, *in camera* ({ }); CX2109 at 229 (Davidow, Dep.); CX1385 at 112 (suggesting that one of the ways for Rambus "to win" was to decrease the RDRAM price premium through "[r]oyalties on alternative DRAMs (eg SDRAM and DDR)"); CX1411 at 3 ("Fight like heck for RDRAM, Have DDR/Lex hammer in order to win on RDRAM, Can make RDRAM more attractive than DDR, 'If we're paying Rambus anyway . . . .'"); CX1273A at 9 ("Objectives for DDR . . . Royalty rates for DDR products are higher than [RDRAM] products . . . by at least 100%, Level the playing field – at least from a perception point of view, Reverse current momentum on Direct vs. DDR design wins"); CX1273A at 23 ("2000: Regain Momentum . . . Publicly disclose DDR licensing policy, Partners choose to ship RDRAMs over DDR, 2003 - Rambus technology will be used"); CX1864 at 6 ("Our policy is that a competitive memory interface that utilizes our patented inventions to achieve its performance cannot have a lower royalty rate than the RDRAM compatible interface")).

Response to Finding No. 1977:

This proposed finding is unsupported, misleading, and incomplete. The proposed finding repeatedly miscites or only partially quotes the evidence. For instance, the proposed finding claims that CX1385 at 112 is "suggesting that one of the ways for Rambus 'to win' was to decrease the RDRAM price premium through '[r]oyalties on alternative DRAMs (eg SDRAM and DDR).'" (emphasis added). The supposed connection between decreasing the RDRAM price premium and royalties on alternatives DRAMs, however, is nowhere in the document. The cited page is a summary of a 113 page presentation and states:

> "Three ways to win:
>
> * Performance requirement increases

* Price premium decreases

* Royalties on alternatives DRAM (eg SDRAM and DDR)"

(CX1385 at 112). Each of these "ways to win" corresponds to a section of the 113 page presentation. The second section, entitled, "Three Ways to Win; 2 RDRAM price premium declines so consumers select it even when performance is not mission critical," (CX 1385 at 35), devotes 59 pages to the issue of decreasing the RDRAM price premium *without a single mention* of royalties on alternative DRAM. (CX 1385 at 35-94). Rather, the document speaks of reducing the price premium by "[i]ncreas[ing] RDRAM volume production" and "[r]educ[ing] RDRAM cost." (CX 1385 at 37). The third section, entitled, " Three Way to Win: 3 Rambus receives royalties on competitive alternatives," (CX 1385 at 95), devotes 12 pages to the issue of Rambus's intellectual property *without a single mention* of the RDRAM price premium. (CX 1385 at 95-107). Rather, it states, "Rambus is willing to license its intellectual property for non-compatible platforms, and "[l]icenses are offered on fair, consistent and reasonable terms." (CX 1385 at 99). The document make no connection at all between offering licenses for SDRAM and DDR on "fair, consistent and reasonable terms" to reducing the RDRAM price premium.

Similarly, the April 2000 email from Geoff Tate, CX 1115 at 3, which Complaint Counsel quote as saying, {

}, (*in camera*), does not support the proposed finding. It reflects a *suggestion* from Mr. Davidow. But Rambus's planning documents in that year state that Rambus is "willing to license technology for non-RDRAM use at reasonable rates." (CX 1366 at 5).

Further, the evidence shows that Rambus had solid economic and business reasons to set its royalties for DDR higher than for RDRAM that had nothing to do with reducing any competitive threat. With its RDRAM licenses, Rambus received benefits that it did not with its DDR licenses; it was able to "participate in future design improvements," obtain information about the partner's customers, and be "part of the process going forward." (Farmwald, Tr. 8179-80). Rambus's RDRAM licenses form a partnership; Rambus works with the licensee, and receives valuable feedback and information. (Farmwald, Tr. 8241). With its DDR licenses, by contrast, there is no partnership, and Rambus receives no additional benefits. (Farmwald, Tr. 8241). There are therefore solid economic reasons for charging a higher rate for DDR licenses. (*See* RPF 1400-04).

1978. Rambus charged a higher royalty rate for DDR than SDRAM because Rambus believed that DDR was more of a threat to RDRAM. (CX2098 at 453-54 (Mooring, Dep.), *in camera* ({ }); CX1864 at 6 ("Why lower royalty on SDRAM? . . . we have never viewed SDRAM as competition . . . DDR on the other hand was created specifically to compete with Direct RDRAM"); CX2070 at 78-81 (Harmon, Dep.); CX2102 at 306 (Karp, Dep.) (when Joel Karp came to Rambus in late 1997 and started working on non-compatible licensing, he initially focused more on DDR than SDRAM, because it was his "sense . . . that DDR was looked on as more of a problem for Rambus than anything else at that point.")).

Response to Finding No. 1978:

This proposed finding is not supported by the evidence. There are solid economic and business reasons for Rambus to charge a higher royalty for DDR that are unrelated to any "threat" to RDRAM. (*See* RRFF 1977). Further, according to Rambus's President, Dave Mooring, Rambus charged higher royalties on DDR SDRAM than on SDRAM because DDR SDRAM "used more of [the Rambus] inventions." (CX 2054 at 205-06 (Mooring Depo.)).

1979. Rambus made it clear to companies that the royalty rates for SDRAM and DDR

SDRAM would be higher than the royalty rates for RDRAM. (CX1864 at 1 (Rambus press release after Hitachi settlement noting the higher royalty rates for SDRAM and DDR than for RDRAM); CX1680 at 18, *in camera* ({

}); CX1384 at 5, *in camera* ({

}); CX1420 at 8, *in camera* ({

}); Heye, Tr. 3898-99, *in camera* ({

})).

Response to Finding No. 1979:

The proposed finding is not supported by the evidence. Rambus does not charge higher royalty rates for SDRAM than for RDRAM, nor do the cited documents or testimony suggest this. Further, there are solid economic and business reasons for Rambus to charge a higher royalty for DDR. (*See* RRFF 1977).

1980. All companies that signed SDRAM/DDR-related license agreements with Rambus agreed to pay royalties on DDR that exceeded Rambus's RDRAM royalty rates. (CX1385 at 102 ("All agreements provide DDR memory and logic royalty rates which are greater than the Rambus compatible royalty rates"); CX1382 at 33; CX2080 at 181 (Karp, Dep.); McAfee, Tr. 7623, *in camera*; CX2067 at 147 (Davidow, Dep.) (qualitatively the rate for DDR is higher than the rate for RDRAM); CX1403 at 27 ("DDR memory and logic royalty rates are greater than Rambus-compatible royalty rates")).

Response to Finding No. 1980:

Rambus has no specific response.

1981. Rambus used a carrot and a stick approach when discussing terms with potential licensees. (CCFF 1982-86).

Response to Finding No. 1981:

The proposed finding is vague and misleading without more detail and context, and is not an appropriate proposed finding. (*See* RRFF 1982-86).

1982. Several years before Rambus began enforcing its patents, in spring 1998, Joel

Karp and Rambus marketing executive Subodh Toprani discussed using a "stick and carrot" approach when talking with companies about Rambus's intellectual property. (CX1744A at 48, 52; CX2114 at 127-128 (Karp, Dep.) ("there was this idea of a stick and a carrot . . . you would have some kind of reward system. . . ."); CX2114 at 129-130 (Karp. Dep.) ("The twig concept so bundles of division equals a stick.")).

Response to Finding No. 1982:

This proposed finding is vague, ambiguous and not supported by the evidence. Mr. Karp, the only person who testified regarding the cited evidence, explained that he "was not sure what this referred to." (CX 2114 at 128-129 (Karp, Dep.)). As best Mr. Karp could recall, Mr. Toprani was referring to a "reward system" for "systems companies" like HP and Sun. (*Id*.).

1983. Rambus informed a number of companies that, if they did not sign a license agreement by a particular date selected by Rambus, Rambus would unilaterally raise their royalty rates. (CCFF 1984-89).

Response to Finding No. 1983:

The proposed finding is irrelevant. In an ordinary license negotiation, neither party negotiates "unilaterally." Further, Rambus's negotiation strategies are irrelevant; it offered the same royalty rates to every potential licensee. (Farmwald, Tr. 8242; CX 2059, Karp Depo. at 251).

1984. Rambus offered Mitsubishi favorable terms if it signed a SDRAM/DDR license agreement early, but also told Mitsubishi that in a few weeks the preferential licensing terms may not be available and Rambus would be "free to pursue other courses of action if [it] needed to." (CX2060 at 73-82 (Tate, Dep.)).

Response to Finding No. 1984:

The proposed finding leaves out relevant information and is irrelevant. (*See* RRFF 1983). Mr. Tate's full explanation of Rambus's options should Mitsubishi not choose to accept

the terms Rambus was offering continued: "this particular proposal was not one that we felt that we were committed to anymore. We were free to reextend it or free to change or free to take other actions." (CX 2060 at 82 (Tate, Depo.)).

1985. { } (CX1141 at 1, *in camera*). Tate also informed NEC that if it did not immediately reach an agreement, Rambus { } and "send an official notice of patent infringement to NEC." (CX1141*, in camera*; CX1141A at 1).

Response to Finding No. 1985:

This proposed finding is incomplete, misleading, and irrelevant. (*See* RRFF 1983). The thrust of Mr. Tate's email to NEC was an explanation that Rambus was negotiating with numerous companies and Rambus was not in a position to tie the NEC license signing to another company's signing date. (CX 1141). Mr. Tate also expressed surprise that NEC was making another request after the parties had apparently reached agreement on all terms the week before. (CX 1141). As Mr. Tate explained, Rambus was "inviting NEC to be a leader and sign early with us on SDR/DDR and in return get the best terms." (CX 1141).

1986. Rambus CEO Geoffrey Tate offered Samsung the "most favored royalty rate," which he argued would give Samsung a "substantial competitive advantage" over companies that chose to litigate rather than agree to Rambus's terms. (CX1146 at 1). At the same time, Mr. Tate threatened to charge Samsung higher rates if it did not immediately sign the license agreement. (*Id.* ("If Samsung doesn't sign now, Samsung's eventual license terms will be on much less favorable terms and Samsung will be at a competitive disadvantage to NEC/Elpida and Toshiba.")).

Response to Finding No. 1986:

The proposed finding is not supported by the evidence. The exhibit cited by Complaint Counsel (CX 1146) does not show Rambus offering Samsung the "most favored royalty rate," or show that Rambus "argued" that doing so "'would give Samsung a substantial competitive

advantage' over companies that chose to litigate rather than agree to Rambus's terms." (CX 1146). The exhibit clearly shows that Rambus met Samsung's request for most favored royalty rate. The exhibit also clearly shows that Rambus wrote that "If Samsung signs now, Samsung will have a substantial competitive advantage." (CX 1146). Nowhere did Rambus "argue that having the "most favored royalty rate" would give Samsung a "substantial competitive advantage." (CX 1146). The proposed finding is also irrelevant. (*See* RRFF 1983).

1987. {
} (CX1384 at 1, 2, 4, *in camera* ({
})).

Response to Finding No. 1987:

This proposed finding is incomplete and misleading. {

} (CX 1384 at 2, *in camera*). The proposed finding is also irrelevant. (*See* RRFF 1983).

1988. {
} (CX1396 at 1, 3, 5, *in camera* ({
}); CX1394 at 3, 5, *in camera* ({ })).

Response to Finding No. 1988:

This proposed finding is incomplete and misleading. {

} (CX 1396 at 3, *in camera*). The proposed finding is also irrelevant. (*See* RRFF 1983).

1989. {

} (CX1384 at 2, *in camera* ({
}); Macri, Tr. 4753-55, *in camera* ({
}).

Response to Finding No. 1989:

This proposed finding is incomplete and misleading. {

} (CX 1384 at 2, *in camera*). Moreover, Mr. Macri did not testify that Rambus was unwilling to negotiate. Mr. Macri testified that it "seemed to him" that the presentation indicated there would be no negotiation. There is no evidence that ATI requested nor that Rambus refused to license ATI at lower rates. The proposed finding is also irrelevant. (*See* RRFF 1983).

1990. Part of Rambus's patent licensing strategy was to demand higher royalty rates from any DRAM manufacturer that refused to license Rambus patents and instead chose to litigate. (CX1385 at 99 ("Rambus Licensing Approach . . . Those companies that decide to litigate will pay higher royalty rates"); CX1382 at 31 (same); CX1379 at 13 (Rambus Policy on Licensing, Settle: Now - Best terms, Later - Higher, but still good; Fight: Then settle - Even higher terms")).

Response to Finding No. 1990:

The proposed finding is misleading and incomplete. To date, with only one exception, Rambus has offered all DRAM manufacturers the same royalty rates on SDRAM and DDR SDRAM. (Farmwald, Tr. 8242.) {
} (RX 2307, *in camera*). In fact, Rambus offered Hitachi a license on substantially the same terms as it offered others. (CX 2059 at 252 (Karp Depo.).) {

} (Teece, Tr, 10539-43, *in camera*). Even Complaint Counsel's economic expert admitted on cross-examination that {

} (McAfee, Tr. 7829-31, *in camera*).

1991. {

} (CX1687 at 2, *in camera*).

Response to Finding No. 1991:

This proposed finding is incomplete and misleading. {

} (CX 1687 at 2, *in camera*).

1992. Part of Rambus's patent licensing strategy was to consider refusing to license any DRAM manufacturer that chose to litigate. (CX1385 at 99 ("Rambus Licensing Approach . . . Rambus may not license those companies that litigate and lose"); CX1382 at 31 ; CX1097 at 1 (Tate January 2000 email: if Hitachi insists "on a fight to the finish we have said we want an injunction: NO LICENSE."); CX2109 at 211-212 (Davidow, Dep.); CX1379 at 13 (Rambus Policy on Licensing . . . Fight: Then settle - Even higher terms, Until decision - No guarantee of a license")).; Rambus Answer at 39, ¶ 94 ("Rambus admits that certain Rambus employees have said that Rambus might treat firms that chose to litigate rather than enter licensing agreements with Rambus less favorably than others.")).

Response to Finding No. 1992:

This proposed finding is incomplete and misleading. Regardless of what Rambus had considered, there is no evidence that Rambus has refused to license anyone. Specifically,

Complaint Counsel has not cited evidence that Rambus refused to license any DRAM manufacturer that chose to litigate. And there is evidence to the contrary – { } (RX 2307, *in camera*).

1993. Rambus intended to threaten to refuse to license its patents to DRAM manufacturers that were unsuccessful in litigation. (CX1864 at 3 (Rambus internal Q&A: "if we are forced to litigate in court, we reserve the right to refuse to license.")).

Response to Finding No. 1993:

The proposed finding is incomplete and therefore misleading. The full internal Q&A answer, a portion of which was cited by Complaint Counsel, was: "Rambus prefers to negotiate and settle amicably. But if we are forced to litigate in court, we reserve the right to refuse to license." (CX 1864 at 3).

1994. Rambus believes it does not have an obligation to license its patents. (CX1097 at 1 (When asked if Rambus had to license Hitachi, Rambus CEO Geoffrey Tate replied "we have NO obligation to do so"); CX3124 at 235 (Vincent, Dep.) ("Rambus would not be under an obligation to license somebody if they didn't want to"); CX2109 at 212 (Davidow, Dep.) ("I don't think we had to license anybody."); Bechtelsheim, Tr. 6387 ("it became public in the press . . . that they may not license companies on these patents moving forward."); CX1864 at 6 (June 2000 Rambus press release Q&A: "We have no obligation to license our patent at all.")).

Response to Finding No. 1994:

This proposed finding is misleading. A patent holder has the statutory right to refuse to license the patent. *See In re Independent Service Organizations Antitrust Litigation*, 203 F.3d 1322, 1327 (Fed. Cir. 2000). Nonetheless, as Rambus makes its revenue through licensing, it has every economic incentive to license its patents to all who will take them. (Teece, Tr. 10341, 10344-45).

C. After Rambus Sued Hitachi, Several Companies Signed License Agreements Calling For Payment of Royalties to Rambus for SDRAMs and DDR SDRAMs.

1995. On January 18, 2000, Rambus initiated litigation against Hitachi in federal district court in Delaware, alleging that Hitachi's SDRAMs and DDR SDRAMs infringed Rambus patents. (CX1855 at 1-14 (Complaint for Patent Infringement asserting that Hitachi's JEDEC-compliant SDRAMs and DDR SDRAMs infringed Rambus patents); Crisp, Tr. 3435 ("Rambus did sue Hitachi at one point for patent infringement"); Rambus Answer at 39, ¶ 95).

Response to Finding No. 1995:

While Respondent has no specific response to the proposed finding, it notes that the complaint cited by Complaint Counsel (CX 1855 at 1-14) asserts patent infringement by SDRAM and DDR SDRAM products, it was not conditioned on the parts being JEDEC-compliant as suggested in Complaint Counsel's parenthetical.

1996. Days after Rambus filed a patent infringement lawsuit against Hitachi, Rambus was still concealing from Samsung that Rambus believed SDRAM and DDR SDRAM infringed Rambus patents. On January 23, 2000, Rambus misled Samsung executives about the nature of Rambus's lawsuit against Hitachi, implying that Rambus sued Hitachi over a contract breach relating to RDRAM. (CX1099A at 1 (Tate January 23, 2000 email: "our strategy in this meeting was to avoid discussing sdram/ddr/infringing ip . . . yw's first question was 'why did you sue hitachi . . . we said 1. hitachi has contracts with rambus for r-chips going back to 93 but have never shipped anything")).

Response to Finding No. 1996:

The proposed finding is misleading and unsupported. The proposed finding relies on a selected portion of the cited exhibit, but it is clear from the entire document that Rambus was not concealing from Samsung its belief about infringement, nor was it misleading Samsung about the nature of its lawsuit. The email states: "our strategy in this meeting was to avoid discussing sdram/ddr/infringing ip *as much as possible and focus instead on promoting rambus and moving forward* together with hastings/taos/etc." (CX 1099A at 1) (emphasis added). The email goes on to state: "yw's first question was 'why did you sue hitachi and how long have you been negotiating with them?.' he asked again at the end of the meeting with a followup

question. we said 1. hitachi has contracts with rambus for r-chips going back to 93 but have never shipped anything 2. they are not a rambus supporter or promoter but they are aggressively promoting ddr 3. *we started meeting with them in october but they wouldn't negotiate so in lights of 1-3 we felt we had no choice.*" (CX1099A at 1) (emphasis added).

1997. On March 23, 2000, Rambus filed a section 337 complaint against Hitachi before the United States International Trade Commission alleging that Hitachi unlawfully imported products infringing Rambus patents. (CX1859 at 5, 20).

Response to Finding No. 1997:

Rambus has no specific response.

1998. Rambus's objective in filing these lawsuits against Hitachi was to stop the import, sale, manufacture and use of Hitachi's DDR and SDRAM products. (CX1366 at 5 ("Hitachi Lawsuit; Filed by Rambus 1/18/00 in Delaware . . . Objective of suit: injunctions against import, sale, manufacture, & use of Hitachi products")).

Response to Finding No. 1998:

Rambus has no specific response.

1999. In June 2000, Hitachi settled with Rambus and agreed to pay a { } royalty on SDRAMs and a { } royalty on DDR SDRAMs. (CX1864 at 1; Rambus Answer at 39, ¶ 95; CX1681 at 15, *in camera*).

Response to Finding No. 1999:

Rambus has no specific response.

2000. { } (CX1681 at 15, *in camera* ({ }); CX1680 at 4, *in camera* ({ }); CX1683 at 13, *in camera* ({ }); CX1685 at 19, *in camera* ({ }); CX1686 at 17, *in camera* ({ }); CX1687 at 16, *in camera* ({ }); CX1689 at 20, *in camera* ({ }); CX2059 at 236-37 (Karp, Dep.), *in camera*).

Response to Finding No. 2000:

This proposed finding is incomplete and misleading. Rambus has offered all DRAM manufacturers the same royalty rates on SDRAM and DDR SDRAM. (Farmwald, Tr. 8242.) In fact, Rambus offered Hitachi a license on substantially the same terms as it offered others. (CX 2059 at 252 (Karp Depo.)). {

} (Teece, Tr. 10539-43, *in camera*).

Even Complaint Counsel's economic expert admitted on cross-examination that it would be consistent with economic theory to charge a higher royalty rate to licensees that require the patent holder to incur costs before taking a license, and that a licensing strategy of charging more to companies that choose to litigate would maximize Rambus's profits by reducing its future costs. (McAfee, Tr. 7829-31).

2001. Rambus CEO Geoffrey Tate testified that Rambus {

} (CX2060 at 297-298 (Tate, Dep., *in camera* treatment requested) ({

})).

Response to Finding No. 2001:

This proposed finding is incomplete and misleading. (*See* RRFF 2000).

2002. Intel believed the Rambus-Hitachi litigation "poison[ed] the industry" by further straining relations between Rambus and DRAM suppliers. (CX2559 at 3 (MacWilliams-Burns June 2000 email exchange: Subject: "Rambus and Hitachi Settle legal dispute . . . [things] turned much more ugly this week in Abid's meeting with DRAM suppliers. Rambus has sent letters to more of them, including Samsung. . . . Bottom line is that Rambus appears to have taken yet another step in poisoning the industry. The extent of this was not expected."); MacWillaims, Tr. 4903 (Rambus was "going to the extent of taking legal action against some of the same vendors, it was very concerning to us that these vendors might not even want to do business with Rambus in the future")).

Response to Finding No. 2002:

Rambus has no specific response.

2003. In 2000, a number of companies signed license agreements with Rambus covering SDRAMs and DDR SDRAMs. (Crisp, Tr. 3436-37; Rambus Answer at 39, ¶ 93).

Response to Finding No. 2003:

Rambus has no specific response.

2004. In June 2000, Toshiba signed a license agreement with Rambus that included a { } royalty on SDRAMs and a { } royalty on DDR SDRAMs. (CX1680 at 4, *in camera*; CX2558 at 1 (June 2000 Ahmad email: "Toshiba, last week signed a license for DDR and SDR (PC100/PC133) to cover themselves against any DDR/SDR IP they may have")).

Response to Finding No. 2004:

Rambus has no specific response.

2005. {

} (CX1683 at 13, 24, *in camera*).

Response to Finding No. 2005:

Rambus has no specific response.

2006. {

} (CX1685 at 19, 34, *in camera*).

Response to Finding No. 2006:

Rambus has no specific response.

2007. By September 2000, Rambus had secured licenses with several major semiconductor companies, representing over 20% of worldwide SDRAM production. (CX1385 at 101 ("4 SDRAM/DDR Patent Licensees; NEC, OKI, Toshiba, Hitachi; 3 of the 7 largest semiconductor companies . . . >20% of the Worldwide SDRAM Production")).

Response to Finding No. 2007:

Respondent has no specific response.

2008. {

} (CX1687 at 16, 28, *in camera*).

Response to Finding No. 2008:

Rambus has no specific response.

2009. {

} (CX1686 at 17, 32, *in camera*).

Response to Finding No. 2009:

Rambus has no specific response.

2010. By November 2000, Rambus had license agreements covering SDRAM and DDR SDRAM with more than 40% of the DRAM market. (CX1391A at 8 (">40% SDRAM/DDR market licensed our IP"); CX1154 at 1 ("great job on samsung/lexington!! . . . great job by Neil & the IP team for their excellent work in getting the SPP1 [strategic patent portfolio] patents and negotiating long and hard for months . . . with samsung on board we now have about 40% of the dram market . . . licensed for sdr/dDR. considering it was about 1 year ago that neil/joel first went to see hitachi this is FANTASTIC progress. add to that the ~10%ish share for rdram and we are close to getting royalties from HALF of the entire dram market! we're not done with the lexington campaign but we sure are winning!")).

Response to Finding No. 2010:

Rambus has no specific response.

2011. {

} (CX 1689 at 20, 37, *in camera*).

Response to Finding No. 2011:

Rambus has no specific response.

2012. By July 2001, Rambus had signed SDRAM/DDR SDRAM license agreements

with DRAM manufacturers (Toshiba, Hitachi, NEC, Elpida, Oki, Samsung, Mitsubishi, Matsushita (controllers)) accounting for over one half of the DRAM market. The remaining hold-outs (Infineon, Hyundai, Micron) accounted for the remainder of the DRAM market. (CX1403 at 28, 49).

Response to Finding No. 2012:

This proposed finding is not supported by the evidence. The only cited document is a draft PowerPoint presentation with an incomplete pie chart.

2013. { } (CX1364 at 1-2, *in camera* ({ }); CX1681 at 10, *in camera* ({ }); CX1687 at 12, *in camera* ({ }); CX1683 at 10, *in camera* ({ }); CX1689 at 14, *in camera* ({ }); CX1685 at 12, *in camera* ({ }); CX1680 at 24, *in camera* ({ }); CX1686 at 11, *in camera* ({ })).

Response to Finding No. 2013:

Rambus has no specific response.

D. Several Companies Refused Rambus's Licensing Demands and Face Patent Litigation with Rambus In the United States and in Various Foreign Countries.

2014. Several companies did not sign license agreements with Rambus for SDRAMs and DDR SDRAMs. (Crisp, Tr. 3437).

Response to Finding No. 2014:

This proposed finding is vague and ambiguous regarding which companies and the time frame at issue.

2015. On August 7, 2000, Rambus filed a patent infringement lawsuit against Infineon Technologies in a German District Court. (CX1866 at 1, 28; Crisp, Tr. 3437).

Response to Finding No. 2015:

Rambus has no specific response.

2016. On August 8, 2000, Rambus filed a patent infringement lawsuit against Infineon Technologies in federal district court in Virginia. (CX1867 at 1; Crisp, Tr. 3437; Rambus Answer at 40, ¶ 97). Infineon asserted various counterclaims, including fraud and antitrust violations. (Rambus Answer at 40, ¶ 97).

Response to Finding No. 2016:

Rambus has no specific response.

2017. On August 10, 2000, Rambus informed Infineon that it would proceed with patent infringement litigation unless Infineon signed Rambus's proposed license agreement. (CX1137 at 1 ("if we are not able to reach agreement on Monday, or make acceptable progress towards finalizing our agreement, we will proceed with litigation.")).

Response to Finding No. 2017:

The proposed finding is not supported by the evidence. As Complaint Counsel accurately quote from the cited exhibit, the August 10, 2000 letter from Rambus to Infineon clearly states that Rambus will proceed with litigation only if Rambus and Infineon "are not able to reach agreement on Monday [August 14th], or make acceptable progress towards finalizing an agreement…." This is not consistent with a finding that states Rambus would proceed with litigation if Infineon does not sign Rambus's proposed agreement.

2018. {

} (CX3111 at 1, *in camera* ({

}); CX3112 at 1-2, *in camera*).

Response to Finding No. 2018:

This proposed finding is incomplete and misleading. {

} (RX 2307 at 1, *in camera*).

2019. In August 2000, Hynix sued Rambus in federal district court in California seeking a declaratory judgment that its manufacture and sale of JEDEC-complaint SDRAM did not

infringe Rambus's patents. (CX1878 at 2-3; Rambus Answer at 40-41, ¶ 98)). Hynix also accused Rambus of antitrust violations, unfair competition, and breach of contract. (CX1878 at 2-3). Rambus asserted counterclaims accusing Hynix of patent infringement. (CX1891 at 1-5; Rambus Answer at 40-41, ¶ 98). The court stayed the lawsuit pending a final ruling in the Infineon litigation. (Rambus Answer at 41, ¶ 98).

Response to Finding No. 2019:

The proposed finding is incomplete and not supported by the evidence. Hynix sued Rambus on August 29, 2000 – the day after Micron sued Rambus (*see* RRFF 2020). Hynix's declaratory judgment claim does not identify Hynix's parts as "JEDEC compliant," and it sought a judgment only that its products do not infringe *several* Rambus patents. (Rambus Answer at 41, ¶ 98.) Finally, while the Hynix litigation was stayed at the time Rambus answered the Complaint in this Action, it was stayed pending a decision from the Federal Circuit and not pending a "final ruling." (Rambus Answer at 41, ¶ 98). That stay was lifted by the Hynix Court before the Federal Circuit ruled and is no longer in effect.

2020. In August 2000, Micron sued Rambus in federal district court in Delaware seeking a declaratory judgment that its manufacture and sale of JEDEC-complaint SDRAM did not infringe Rambus's patents. (CX1880 at 16-21; Rambus Answer at 41, ¶ 99; CX1140 at 1) (Appleton August 2000 email: "Based on Rambus' past and recent behavior the only way to have a sensible resolution is through litigation. Although this is unfortunate, it appears to be compelled by Rambus' action in dealing with others in the industry. We feel strongly that neither judge or jury will approve of Rambus' behavior."). Micron also accused Rambus of monopolization, attempted monopolization, and deceptive trade practices. (CX1880 at 12-15). Rambus asserted counterclaims accusing Micron of patent infringement. (CX1880 at 29-38; Rambus Answer at 41, ¶ 99). The court stayed the lawsuit pending a final ruling in the Infineon litigation. (Rambus Answer at 41, ¶ 99).

Response to Finding No. 2020:

The proposed finding is incomplete and not supported by the evidence. Micron sued Rambus on August 28, 2000 – the day before Hynix sued Rambus (*see* RRFF 2019). Micron's declaratory judgment claim does not identify Micron's parts as "JEDEC compliant," and it

sought a judgment only that its products do not infringe *several* Rambus patents. (Rambus Answer at 41, ¶ 99.) Finally, the Micron litigation was not "stayed pending a final ruling in the Infineon litigation." At that time, the Micron Court postponed trial until after a ruling by the Federal Circuit, but ordered the parties to complete all necessary discovery in the interim. (Rambus Answer at 41, ¶ 99).

2021. Rambus litigation has cost Micron tens of millions of dollars and distracted valuable staff resources. (Appleton, Tr. 6398-99).

Response to Finding No. 2021:

The proposed finding is misleading. Micron chose to file suit and incur these costs instead of negotiating with Rambus. (CX 1140). Rambus would have preferred to negotiate, and to have saved its corresponding Micron litigation costs as well. (CX 1140 Geoff Tate writing to Steve Appleton: "I am disappointed Micron chose litigation over negotiation . . . we prefer licensing over litigation so we are always ready to get together to discuss these issues and negotiate. It appears you are not. If in the future you [Micron] are willing to consider resolution through negotiation I will be happy to meet with you at your convenience.").

2022. Each of the Rambus patents involved in the Infineon, Micron, and Hynix lawsuits claims priority to Rambus's '898 application. (Rambus Answer at 41, ¶ 100). Moreover, every patent that Rambus has asserted in patent litigation can trace its lineage to one of two patent applications in the '898 family: either the 08/222,646 ("'646") or the 07/847,961 ("'961"). (First Stipulations, No. 22; Exhibit A to First Stipulations, No. 22; Nusbaum Tr. 1506-1508; see also DX0014). The '646 and '961 applications, as well as the '490 application which was a continuation of the '961 application, and the '327 patent which issued from the '646 application, were pending while Rambus was a member of JEDEC (CCFF 1008, 1028, 1049, 1076-77, 1092-95) and contained claims that related to ongoing work at JEDEC (CCFF 1028, 1049, 1125-63, 1164-82, 1199-1215, 1216-37).

Response to Finding No. 2022:

The proposed finding is incorrect and misleading. Rambus has provided specific

responses to the proposed findings cited in support of this particular finding and does not repeat them here. (*See* RRFF Nos. 1008, 1028, 1049, 1076-77, 1092-95, 1125-63, 1164-82, 1199-1215, 1216-37). The proposed finding is also misleading because the fact that a patent application traces its lineage back to another patent application does not in any way suggest that the subject matter of its claims is related to the subject matter of the claims of the prior patent application, except that both must be supported by the same written description. (See RPF 78, 83-85.)

2023. Rambus believes it possesses additional patents and patent applications, some claiming priority back to the '898 application, that it could in the future seek to enforce against memory manufacturers producing JEDEC compliant SDRAM. (Rambus Answer at 41-42, ¶ 101 ("Rambus admits the allegations in paragraph 101 of the Complaint").

Response to Finding No. 2023:

Rambus has no specific response.

2024. Rambus has numerous foreign patents that are directly based on its original U.S. patent application no. 07/510,898 (the '898 application). (CX1452 (India); CX1453 (Taiwan)). Many of these foreign patents claim priority based on the '898 application and the benefit of its April 18, 1990 U.S. filing date. (CX1485 (Israel); CX1489 (Israel); CX1496 (Israel); CX1499 (Israel); CX1515 (Korea); CX1527 (Germany); CX1529 (Europe); CX1533 (Europe); CX1536 (Europe)).

Response to Finding No. 2024:

The proposed finding is vague and misleading. Each of the cited foreign patents claims priority to and is based on the '898 application.

2025. {

} (CX2072 at 45-46 (Tate, Dep.), *in camera*).

Response to Finding No. 2025:

Rambus has no specific response.

2026. Rambus is involved in patent infringement lawsuits in various foreign countries that involve foreign patents that cover some of the same inventions at issue in the U.S. litigation. (Rambus Answer at 42, ¶ 102).

Response to Finding No. 2026:

Rambus has no specific response.

2027. In August and September 2000, Rambus filed several patent infringement lawsuits against Micron in European countries. Rambus alleged that Micron's SDRAM and DDR SDRAM products infringed Rambus's foreign patents. (CX1869 at 1, 40 (patent infringement lawsuit against Micron Semiconductor in a German District Court); CX1871 at 1 (patent infringement lawsuit against Micron in a British Patent Court); Appleton, Tr. 6396-6397 (Rambus asserted foreign patents against Micron in France, Germany, Italy, and the United Kingdom)).

Response to Finding No. 2027:

Rambus has no specific response.

2028. Rambus's foreign patent infringement lawsuits "pose risks" for Micron. (Appleton, Tr. 6397-98 (Micron has invested hundreds of millions of dollars in its Italian wafer manufacturing plant, which employs 1,500 to 2,000 people)). If Micron had to shut down its European operations due to litigation with Rambus, it would lose a major source of its product. (Appleton, Tr. at 6397-98 ("we wouldn't be able to service our customers with the products that they're currently buying from there")). If successful, Rambus's foreign patent infringement lawsuits would have a global impact on Micron's business. (Appleton, Tr. 6397-98 (the product that Micron makes in Europe "gets sold around the world")).

Response to Finding No. 2028:

The proposed finding is incomplete and misleading. Despite testifying that Micron faced substantial "risks" from litigation with Rambus, Mr. Appleton has assigned no Micron engineers to design products that would avoid the features covered by Rambus's patents and does not know whether any Micron engineers are working on such a project. (Appleton, Tr.

6411-12). Furthermore, it was Mr. Appleton who chose to break off negotations regarding a license with Rambus in order to litigate. (RRFF 2021; Appleton, Tr. 6412). Indeed, when Mr. Appleton learned that Samsung had entered into a license with Rambus he commented: "We expected Samsung to settle with (Rambus) because they are weak. It's that simple. . . . They don't want to stand up and assume a strategy that gets them into court in the United States. They want to avoid litigation. That has been their strategy all along." (RX1716; Appleton, Tr. 6425).

2029. Rambus President Bill Davidow testified that even if Infineon prevailed in its litigation with Rambus, "there [was] a whole set of subsequent patents that they would be litigating." (CX2067 at 110 (Davidow, Dep.)).

Response to Finding No. 2029:

The proposed finding is irrelevant. There is no evidence that Mr. Davidow was referring to patents relating to the particular features or the particular patent family that are at issue in this case. The proposed finding also contains incorrect information. Mr. Davidow is Rambus's Chairman, not its President.

2030. In a May 2001 press release, Rambus stated that it has additional U.S. and foreign patents covering SDRAMs and DDR SDRAMs that it has not yet asserted in any litigation. (CX1888 at 1 (Rambus May 2001 press release: "Rambus holds newly issued U.S. and European patents covering Rambus inventions used by SDRAMs and DDR SDRAMs that have not yet been asserted in any litigation and are not impacted by the [Infineon trial] Court's decision.")).

Response to Finding No. 2030:

The proposed finding is irrelevant. There is no evidence that the press release was referring to patents relating to the particular features or the particular patent family that are at issue in this case.

2031. In July 2001, Rambus noted that the "Virginian decision involved only 4 patents" and that Rambus has "many others which are used by SDRAM/DDR." (CX1403 at 30).

Response to Finding No. 2031:

The proposed finding is irrelevant. There is no evidence that the draft slide cited by Complaint Counsel was referring to patents relating to the particular features or the particular patent family that are at issue in this case.

2032. In July 2001, Rambus admitted that even if it lost in the U.S. litigation, it could still successfully enforce its foreign patents. (CX1890 at 35 (Rambus Senior Vice President of Finance and CFO Bob Eulau: "I'll take a question then which is "What is the likelihood of SDRAM licensees not paying due to the Virginia outcome? We don't think this is very likely. . . .We've said that the litigation requires success in a major jurisdiction, but not in every jurisdiction.")).

Response to Finding No. 2032:

The proposed finding is incomplete and misleading. The full answer from Rambus's CFO, given during a quarterly conference call concerning Rambus's financial results, was: "We don't think this is very likely. As I said before, we've had discussions with all of the major licensees. We've said that the litigation requires success in a major jurisdiction, but not in every jurisdiction. The current licensees certainly have concerns but they're also getting protection in their current use of our intellectual property. And we're always willing to have discussions with our licensees. And if there are any win/win proposals we're certainly willing to listen to those." (CX 1890 at 35).

E. Rambus's Enforcement of Patents with Respect to Technologies Incorporated in the JEDEC SDRAM and DDR SDRAM Standards Has Caused, and Will Cause, Substantial Economic Harm and Threatens the Integrity of Open Standard Setting.

2033. Rambus has raised the price for use of programmable CAS latency, programmable burst length, on-chip DLL, and dual edge clocking technologies in DDR SDRAM from free (i.e. 0%) to a royalty of { }. (CCFF 734, 742, 745, 2000).

Response to Finding No. 2033:

The proposed finding is misleading and unsupported. The use of Rambus's programmable CAS latency, programmable burst length, on-chip DLL, and dual edge clocking technologies was only "free" in the sense that any infringing use of patented technology is "free" – any unpermitted use of another's property without paying for that use is always "free." The evidence shows, however, that Rambus's DDR royalty rates are lower than the cost savings enjoyed by DRAM manufacturers by the use of Rambus's technologies. (*See* RPF 1125-40).

2034. Rambus has the power to raise the royalty for use of programmable CAS latency, programmable burst length, on-chip DLL, and dual edge clocking technologies higher, and has stated its intention to do so. (CCFF 2035, 2041-43).

Response to Finding No. 2034:

The proposed finding is unsupported. (*See* RRFF 2035, 2041-43). Further, the evidence shows that any power Rambus may have over the royalties for its technologies is due to the superiority of those technologies. (*See* RPF Section XII.B).

2035. In 2000 and 2001, Rambus planned to continue increasing its royalty rates on SDRAM, DDR SDRAM, and RDRAM. (CX1380A at 3 (August 2000 KR01 Kickoff Meeting: "We are ratcheting up royalty rates over time to the value of the IP"); CX1391A at 32-33 (November 2000 Big Picture Update: "over time we can drive royalties [on RDRAM] from 1-2% average to 3-5% (DDR shows the value of our technology; price our own standards to value)")).

Response to Finding No. 2035:

The proposed finding is misleading and unsupported. The cited documents show that Rambus hoped to increase its overall average royalty rates for its entire portfolio of technologies, which included RDRAM, SDRAM, DDR, and its network technology SERDES. (CX 1391 at 20-22). Rambus hoped to do this by developing "fundamental Technology/IP for

memory interfaces through 2020" for RDRAM, developing "technical solution/standard that adds value to DDR customers," and developing "superior signaling technology for network links with fundamental IP" for SERDES. (*Id.*). Rambus sought to get "in the innovation loop" in these areas so as to provide value to its customers, thereby allowing for higher royalty rates.

2036. { } (CX1273 at 11, *in camera* ({ })).

Response to Finding No. 2036:

The proposed finding is misleading and irrelevant. The proposed finding merely cites a planning document; it is not supported by any evidence that those plans were realized.

2037. Rambus plans to charge companies that decide to litigate higher royalty rates,or it will decide not to offer any license to those who lose. (CX1385 at 99 ("Rambus Licensing approach . . . Those companies that decide to litigate will pay higher royalty rates. Rambus may not license those companies that litigate and lose.").

Response to Finding No. 2037:

The proposed finding is incomplete. Complaint Counsel's economic expert admitted on cross-examination that it would be rational and consistent with economic theory to charge a higher royalty rate to parties that impose costs on Rambus before taking a license, such as through litigation, and that a licensing strategy of charging more to companies that choose to litigate would maximize Rambus's profits by reducing its future costs. (McAfee, Tr. 7829-30; *see also* Teece, Tr. 10541-45 (*in camera*) ({ })).

2038. Rambus's requested royalty rate would cost Micron hundreds of millions of dollars. (Appleton, Tr. 6390-92).

Response to Finding No. 2038:

The proposed finding is incomplete. Micron has not taken a license from Rambus for the technologies used in SDRAM and DDR, and it therefore enjoying the benefits of Rambus's technologies without paying for those benefits. Further, when requested to meet with Rambus to discuss Rambus's desire to license Micron "on the best possible deal terms" (RX 2303 at 1), Mr. Appleton chose not to even meet with Rambus but to file suit against Rambus instead. (Appleton, Tr. 6421-24).

2039. Rambus claims that approximately 90% of the entire DRAM market is covered by Rambus patents. (CX1386 at 4 ("Today - We are on the cusp of achieving our original BHAG [big hairy audacious goal] - SDRAM+DDR+RDRAM>>90% of the DRAM market - SDRAM/DDR: -20% paying us royalties now; all by 01E"); CX2112 at 309-310 (Mooring, Dep.) (FTC Deposition January 2003: "If I were to guess on a revenue basis in the most recent quarter . . . I would think that DDR is about 50 percent, SDRAM 40 percent, RDRAM less than 10 percent with EDO taking up the piece that RDRAM doesn't make in the 10 percent. It's a guess."); CX2067 at 171 (Davidow, Dep.) ("Q. So am I right, then, that it's Rambus's position [] that any SDRAM or RDRAM being used in main memory PCs today [January 31, 2001] are covered by their patents? . . . [A] I would say that it is highly likely that is true.")).

Response to Finding No. 2039:

Rambus has no specific response.

2040. In the year 2000, Rambus's 5-year goal was to collect royalties on over 90% of the DRAM market. (CX1380A at 3 ("5 year objectives . . . All/90%+ DRAMs/controllers pay us royalties")).

Response to Finding No. 2040:

Rambus has no specific response.

2041. Graphs from Rambus's "November 2000 Big Picture Update" show, during the 2000-2005 period, (1) Rambus's "Market Share" increasing to 100%; (2) its "Average Royalty Rate" increasing from 1% to 5%; and (3) its annual royalty income increasing from $90 million to $3 billion. (CX1391A at 32).

Response to Finding No. 2041:

The proposed finding is misleading. The cited graphs are part of a presentation that discusses and combines all of Rambus's various technologies. The cited documents show that Rambus hoped to increase its overall average royalty rates for its entire portfolio of technologies, which included RDRAM, SDRAM, DDR, and its network technology SERDES. (CX 1391 at 20-22). Rambus hoped to do this by developing "fundamental Technology/IP for memory interfaces through 2020" for RDRAM, developing "technical solution/standard that adds value to DDR customers," and developing "superior signaling technology for network links with fundamental IP" for SERDES. (*Id.*). Rambus sought to get "in the innovation loop" in these areas so as to provide value to its customers, thereby allowing for higher royalty rates. Further, the cited graphs are under the title, "DRAM MIBU Revenues: What IF," indicating that the graphs represent projections only these conditions are met.

2042. One of Rambus's "2001 Really Big Picture Goals" was to "[c]ollect royalties on all DRAM and controllers forever." (CX1386 at 1, 8; CX1388 at 8 ("BHAG [Big Hairy Audacious Goal] – Our standards dominate the DRAM interface market and our IP is fundamental to all DRAM interfaces forever")).

Response to Finding No. 2042:

The proposed finding is misleading and incomplete. Rambus's plans as indicated in the very documents cited by the proposed finding were to "[d]evelop fundamental IP for all DRAM and enable solutions and standards for the RDRAM roadmap." (CX 1388 at 3). Rambus hoped to "[d]etermine how and where memory will be used through 2010," "[i]dentify problem areas," and "[d]evise strategies to win control of key market segments." (CX 1388 at 4). Rambus's goals were to "[e]numerate viable memory topologies for key 2004+ market segments and file

IP," and "[i]dentify and start development of critical technologies for 2004+ market segments." (CX 1388 at 5). Only if Rambus were to accomplish all of this new technology development, could it then collect royalties for its key technologies.

2043. Rambus expects to collect { } in fees and royalties from DRAM manufacturers. (CX0527 at 1, *in camera* ({ }); CX0528 at 1, *in camera*; CX0529 at 1, *in camera*; CX0530 at 1, *in camera*; CX1343 at 22, *in camera*; CX1401 at 10, *in camera* ({ })).

Response to Finding No. 2043:

Rambus has no specific response.

2044. Rambus's royalties could cause a decrease in the volume of DDR SDRAM that DDR manufacturers produce. (CX2558 at 1 (Ahmad-Krisa June 2000 email: "in talking with memory suppliers, they are re-evaluating their plans for DDR support. Comments that DRAM suppliers have made are that they do not want to produce DDR DRAMs if they have to pay this high royalty"); McAfee, Tr. 7744-45, 7749-50; CX2561 at 2 (Ahmad August 2000 email: "Feedback from suppliers was that if they do end up signing for a royalty structure for DDR then their [sic] inclination would be to limit the DDR volume")).

Response to Finding No. 2044:

The proposed finding is unsupported. The documents cited in support of the proposed finding consist of comments given to Intel by DRAM manufacturers during the 2000 time period regarding their projected volumes of RDRAM and DDR. (CX 2561 at 1 ("RDRAM volume and pricing update . . . DDR volume")). In light of the large quantity of record evidence showing that the manufacturers attempted to mislead Intel and other customers on issues relating to production projections, *see* RPF 1564-94, the cited documents are not probative. Moreover, now that RDRAM has been avoided by the DRAM manufacturers, DDR volumes cannot be affected by production of RDRAM. Further, though one of the documents cites

speculation about a possible impact on the ramp up of DDR if AMD and Via were reluctant to produce controllers (CX 2558 at 1), there is no evidence that that ramp up was actually hindered at all by Rambus's royalties.

The cited testimony of Complaint Counsel's economic expert does not support the proposed finding. He admitted that "the demand for DRAMs themselves is derived from the demand for the final products in which DRAM is used" (McAfee, Tr. 7198), i.e., DRAM volume is driven by the volume of computers and other products using DRAM. There is no evidence that Rambus's royalties will have any effect on the demand for computers and other products using DRAM. In fact, Complaint Counsel's economic expert admitted that he had done no study of the demand elasticity of consumers of PCs or of OEM consumers of DRAM. (McAfee, Tr. 7566). He therefore can have no idea whether Rambus's royalties would affect overall production of DRAM.

2045. In the long run, the increased royalty cost imposed, or threatened to be imposed, by Rambus on manufacturers of DRAMs and memory controllers are likely to be passed on to customers in the form of higher DRAM prices. (CX2107 at 140 (Oh, Dep.) ("Q: . . . Are you saying that the price to the customer is a function of the cost? A: Certainly, yes."); *see also* CX0839 at 2 (Farhad Tabrizi told Richard Crisp that Hyundai "pass[es] on license fees and royalties to their customers"); McAfee, Tr. 7175-76).

Response to Finding No. 2045:

The proposed finding is not supported. The evidence shows that DRAM prices are driven by supply and demand factors and are not necessarily related to manufacturing costs. (Gross, Tr. 2338). Further, Complaint Counsel's economic expert admitted that he had done no study of the elasticity of demand of PC consumers or of customers of DRAM (McAfee, Tr. 7566), which would be necessary to determine whether increased royalty costs could be passed

on.

2046. Rambus's conduct has also caused DRAM manufacturers and others to incur substantial litigation-related costs. (Appleton, Tr. 6398-99 (the litigation has resulted in direct litigation costs of tens of millions of dollars; "more importantly, the litigation costs associated with having all of our technical people and our administrative people and individuals like myself, all of us to focus and prepare for these trials and these cases is obviously a great deal of time and a great burden.")).

Response to Finding No. 2046:

The proposed finding is misleading. "Rambus's conduct" has not caused any one to incur litigation costs; these costs are incurred because certain companies have insisted on infringing Rambus's patents.

2047. Rambus's conduct has caused DRAM manufacturers and others to spend time and effort trying to design around Rambus's patented technologies. (Rhoden, Tr. 532-33 (Mr. Rhoden presented a proposal to JEDEC to change from programmable to fixed CAS latency); Lee, Tr. 6776-6806 (describing efforts to convince JEDEC to adopt alternatives to the technologies claimed by Rambus)).

Response to Finding No. 2047:

The proposed finding is misleading. "Rambus's conduct" has not caused anyone to spend time and effort trying to design around Rambus's patented technologies. The weight of the evidence shows that Rambus's technologies would have been incorporated into SDRAM and DDR products even if Rambus had made the additional disclosures that Complaint Counsel contend should have been made. (*See* RPF Section IX).

2048. Rambus's lawsuits seeking an injunction threaten to shut down DRAM plants. (Appleton, Tr. 6397 ("There's no question [the foreign lawsuits instituted by Rambus] pose risks. . . . [In Italy] Rambus even tried to get a preliminary injunction to shut us down there. Fortunately, it wasn't successful, but it would have a – just a dramatic effect on the company.")).

Response to Finding No. 2048:

The proposed finding is incomplete. Rambus can only obtain an injunction if it is proven that there its patents are valid, enforceable, and infringed.

2049. Rambus's conduct threatens to have a significant adverse impact on JEDEC and other standard-setting organizations. (CCFF 2050-54).

Response to Finding No. 2049:

The proposed finding is unsupported and speculative. (*See* RRFF 2050-54).

2050. JEDEC officials believe that Rambus's conduct and resulting lawsuits could cause a fundamental change in JEDEC and a shift away from open standard setting. (Rhoden, Tr. 536 (Mr. Rhoden, Chairman of the JEDEC Board of Directors and the JC-42 Committee, testified that Rambus' lawsuits could lead to "a fundamental change in JEDEC and a fundamental shift away from open industry standardization.")).

Response to Finding No. 2050:

The proposed finding is unsupported. While Mr. Rhoden testified that Rambus's lawsuits threaten industry standardization, his own contemporaneous documents say otherwise. In a July 2000 email, Mr. Rhoden wrote, "Rambus is certainly not the first to declare IP in this or any other industry and none has had any net negative impact on standardization. The end users still demand standardization (what they are really asking for is low price). JEDEC has continued to work through several actions amazingly similar to this one." (CX 2767 at 4).

2051. Failure to disclose relevant patents and patent applications could cause companies to refuse to participate open standard setting organizations such as JEDEC. (Rhoden, Tr. 537-38 (industry members would "operate in some other environment rather than disclosing [proposals] in an open environment like JEDEC."); *see also* G. Kelley, Tr. 2474-75 (Mr. Kelley intended to inform Texas Instruments that "IBM would not participate in a standards organization where patent information was being hidden while the process of approval went on"); *id*. at 2476-77 ("If companies like IBM are going to leave the process of standardization out of fear of patented material that is not disclosed during the process of standardization, then the standardization process will be so weakened that it will have very little meaning.").

Response to Finding No. 2051:

The proposed finding is unsupported and misleading. As Desi Rhoden wrote in 2000, "Rambus is certainly not the first to declare IP in this or any other industry and none has had any net negative impact on standardization. The end users still demand standardization (what they are really asking for is low price). JEDEC has continued to work through several actions amazingly similar to this one." (CX 2767 at 4). There is absolutely no evidence of any decrease in participation in standard setting organizations.

2052. Rambus's conduct could also discourage industry participants from relying on standards developed by JEDEC or other standard setting bodies. (Bechtelsheim, Tr. 5888-89 ("if that trust into the nature of an open standards process is violated, it makes it very difficult for me to rely on the standards groups developing standards, and this would be extremely disruptive to the industry at large."); (CX2851 at 15 ("Whatever the outcome of [Rambus's] legal cases, the greatest loser will be the wider semiconductor industry. There is bound to be a loss of confidence in the ability of companies to work collectively under the auspices of bodies such as JEDEC to produce industry standards, and this can only retard future semiconductor development. Knowingly or not, Rambus has done a great job of undermining the credibility of one of the main sources of competition in the IP market - the standards bodies.").

Response to Finding No. 2052:

The proposed finding is unsupported. It rests solely on speculation. There is absolutely no evidence of any decrease in reliance of standards set by standard setting organizations.

2053. During the time that Rambus was a member of JEDEC, JEDEC members recognized that failure of members to disclose patents and patent applications relating to JEDEC work could "destroy the work of JEDEC." (CX2384 (G. Kelley letter regarding the Quad CAS incident: "I am and have been concerned that this issue can destroy the work of JEDEC. If we have companies leading us into their patent collection plates, then we will no longer have companies willing to join the work of creating standards"); CX0083 at 15-16 ("The result [of any attempt by a member of standards group to patent an emerging standard, even for defensive purposes] is more likely to be loss of mutual trust essential to the success of the standardization effort, as well as a 'clean room' restart of the standards effort aimed at avoiding the patent.")).

Response to Finding No. 2053:

The proposed finding is misleading and incomplete. There is no evidence that any failure of any JEDEC member to disclose patents or patent applications (which was not required by JEDEC's rules in any event) has "destroyed" the work of JEDEC. To the contrary, as Desi Rhoden wrote in 2000, any perceived failures have not effected JEDEC: "Rambus is certainly not the first to declare IP in this or any other industry and none has had any net negative impact on standardization. The end users still demand standardization (what they are really asking for is low price). JEDEC has continued to work through several actions amazingly similar to this one." (CX 2767 at 4).

2054. Rambus's narrow interpretation of the JEDEC disclosure policy, as accepted in part by the two- member majority of the Federal Circuit panel, threatens the ability of JEDEC to function effectively as a standards setting organization. (CX3089 at 3-4 (JEDEC brief amicus curiae: Rambus's proposed interpretation of the JEDEC disclosure policy, as adopted by the 2-member majority of the Federal Circuit, "impairs JEDEC's ability to effectively function as a standards setting organization."); CX3090 at 4 (industry members' brief amicus curiae: the standard setting process "is deeply impacted by the [Federal Circuit] decision."); *see also* J. Kelly, Tr. at 2066-67 (if companies can drop their membership without having the duty to disclose, that "destabolizes the whole system.")).

Response to Finding No. 2054:

The proposed finding is unsupported. It rests on assertions in two briefs. Assertions in briefs are not evidence.

2055. Paragraphs 2055 - 2099 are unused.

UNITED STATES OF AMERICA
BEFORE THE FEDERAL TRADE COMMISSION

In the Matter of	)	
	)	Docket No. 9302
RAMBUS INCORPORATED,	)	
a corporation.	)	
	)	

CERTIFICATE OF SERVICE

I, Jacqueline M. Haberer, hereby certify that on October 1, 2003, I caused a true and correct copy of *Rambus Inc.'s Responses to Complaint Counsel's Proposed Findings of Fact, Volume II (Public)* to be served on the following persons by hand delivery:

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