Fourth Quarterly Progress Report

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Speech Processors for Auditory Prostheses

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submitted by

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1.0 Introduction

Work performed with the support of this contract is directed at the design, development, and evaluation of speech processors for use with auditory prostheses implanted in deaf humans. Major research efforts are proceeding in four areas: (1) developing and maintaining a laboratory based, software controlled, real time, speech processing facility where processor/stimulator algorithms for monaural and binaural eight-channel implants can be implemented/tested and a wide range of psychophysical measurements can be made, (2) using the laboratory facility to refine the sound processing algorithms used in the current commercial and laboratory processors, (3) using the laboratory facility to explore new sound processing algorithms for implanted subjects, and (4) designing and fabricating programmable, wearable speech processors/stimulators and using these systems to: (a) field test processor algorithms developed and tested in the laboratory, (b) evaluate the effects of learning using longitudinal evaluations of speech reception, and (c) compare asymptotic performance of different speech processors across subjects.

This report concentrates on the design and fabrication of new programmable and wearable speech processors/stimulators (area (4) above) being carried out together with engineers at the Draper Laboratory.

2.0 Wearable Speech Processors/Stimulators

The long-term goal of this segment of our work is to design and fabricate wearable and programmable sound processing systems that are capable of producing high-rate, simultaneous or interleaved stimulation that can be synchronized across bilateral, cochlear implants. These capabilities should enable us to implement a wide range of sound processing schemes. Our current speech processor was developed together with the Microprocessor Laboratory of the Geneva Engineering School (GES), the University of Geneva (UofG) and the Research Triangle Institute (RTI). Support for that work came from this NIH Contract, a parallel Contract at RTI and the Wilsdorf Foundation of Geneva. This wearable unit gives us the ability to implement a wide range of sound processors designed for moderate rate (<3,000 pulses/sec/channel), interleaved, monolateral stimulation.

In order to move from our current system to one capable of high-rate, interleaved or simultaneous stimulation, several modifications are required. First the bandwidth of the current sources must be increased to transmit the narrower pulse widths and guard drivers must be added to combat the waveform distortions that stray capacitances cause at these higher-rates. At the same time, the power dissipation of these circuits as well as their size must be reduced so that six or eight of these current sources can be packaged as part of a single sound processing unit that is comfortable to wear and runs for more than 10 hours on a single battery charge. The following describes the design and testing work that is

leading to a new wearable system that will include six current sources and be capable of high-rate, simultaneous and interleaved stimulation.

2.1 Current Source Design

The current source assembly will include eight D/A converters (all on a single chip) that are driven by serial input from the signal processing electronics. Each D/A output will drive a voltage-to-current converter (V/I) that will produce corresponding output stimulation currents to be applied to implanted cochlear electrodes. This assembly will also include battery voltage conditioning circuits that will produce operating voltages for all of the analog electronics (circuits that operate upon the microphone output and provide a digital encoded sample for the digital signal processor (DSP) chip used in the portable processor, as well as the V/I output circuits). This assembly of V/I converters, D/A converters, and power conditioning circuits will be packaged as a compact multi-chip module (MCM) that can be integrated with the analog input circuits of the portable processor. The V/I converters will be capable of producing pulsatile stimuli with full-scale rise/fall times less than 1 us, maximum output currents of +/- 3 ma with a minimum compliance of +/- 10 volts.

The starting point for this design effort was an analysis of the present laboratory electronics used for the conversion of voltage signals into stimulating currents. This was followed by investigations of alternative circuits leading to selection of a new topology that was optimized based upon the performance requirements. Performance was predicted using computed simulations (SPICE) as well as analytical methods, and then verified with a bread-board assembly. The original circuit was modified significantly in the course of the design process, so that power efficiency, frequency response, transient response, output impedance, and temperature stability were made satisfactory. Another important aspect of this design was the inclusion of guard drivers to minimize the effect of the shunting reactance produced by parasitic capacitances between leads of the shielded cable that connect the current sources to the subject's electrodes[1]. This revised V/I converter was fabricated using standard printed circuit board (PCB) techniques and integrated into our laboratory stimulation system for testing.

Based on initial testing, additional design effort improved the stimulator circuit by including an output (common base or cascode) circuit modification that improved the frequency response - and consequently the output waveform fidelity - by reducing capacitive coupling between stages, and also increased the effective output impedance of the circuit (which should be as high as possible to act as a proper current source) at higher frequencies. A low frequency, negative feedback path was included in the final circuit design to reduce output DC voltages as a result of small imbalances in output leakage currents.

Figure 1 presents the latest design for the Draper Laboratory, V/I circuit (as the diagram indicates, two current sources are included in the design layout). The circuit is divided into three sections by dashed vertical lines. The left section, including the

transistors Q1 and Q2, uses a low-voltage, high-gain, operational amplifier transconductance stage that operates at low quiescent power and drives a level-conversion stage followed by a 1:8 push/pull current mirror stage. The bias configuration of the level shifting stage was adjusted to minimize the added power overhead of the class AB configuration while meeting the minimum rise/fall-time requirements. Two feedback paths were tuned to optimize the V/I transient response over the desired output load range expected. One path connects the operational amplifier output to its inverting input and the other connects the reference side of the current mirror output to the same inverting input.

The middle or current mirror portion of Figure 1 is configured as a pair of balanced hybrid circuits using carefully matched, bare transistor die from common npn and pnp wafers. The reference transistors (Q1 and Q2) are at the center of a circular configuration with the output (drive) transistors surrounding it for each of the respective polarities. These were placed on a substrate to optimize isothermal operation.With the high gain available from the combination of input circuits, an input voltage of V driving the input resistor Rin will establish a current through Q1 and Q2 of V/Rin amperes. This current is established in a very stable manner because of the input operational amplifier and level shifting stage gains, as well as the bias conditions on Q1 and Q2. Since Q1 and Q2 are included within the matched transistor arrays (pnp and npn respectively), and all of the bases of the pnp group and the npn group are connected, the base to emitter voltage that is established across Q1(Q2) is also established across all the other base to emitter connections of the pnp(npn) array. As a consequence of the transistor matching, the current that is caused to flow in Q1 or Q2 is also "mirrored" in each of the other eight transistors in each of the two packages. With all eight of the transistors' collectors also connected in common, the current at this point is exactly 8 times that established in Q1 or Q2. Transistors Q3 and Q4 form the cascode pair that boosts the output impedance but allows the full "mirrored" current to flow to the output node. Thus, the final output current is 8*Vin/Rin, and is available from the middle connection of the cascode transistors. This point is capacitively coupled to the electrode connection as shown.

The right hand portion of the circuit shown in Figure 1 is a unity gain amplifier implemented with an operational amplifier connected as a voltage follower. The output of the unity gain circuit drives the cable's shield connection through a small R-C series load to prevent oscillation and protect the amplifier output. In addition, this output is also fed back, through a lowpass filter, to the input operational amplifier. This feedback provides a nulling of any DC drift voltage at the output of the current source.

This version of the V/I converter provides a number of advantages over the Howland circuit we have used in the past: better temperature stability, improved Power supply Rejection Ratio, and a reduction in quiescent power dissipation by a factor of more than ten.

2.2 Design of the Subsystem

In parallel with the design and testing of the V/I circuit, mechanical/electrical design of a miniaturized subsystem has also been proceeding. This subsystem consists of three entities: (1) the basic V/I circuit replicated six times (for stimulating a six electrode Ineraid implant), (2) the D/A converter circuit that translates serial digital data from the digital signal processing IC used in the portable speech into six analog signals that serve as inputs to the V/I converters, and (3) power conditioning circuits to generate all of the voltages needed by the analog input and output circuits.

Based on studies of alternative packaging formats for size and mechanical stability, the choice was made to use a set of multi-chip modules (MCM) to be integrated on a common substrate. This format uses unpackaged IC die and miniaturized passive elements. A preliminary design of the stimulator circuit has been completed that includes two V/I converters per unit. An MCM design of the eight channel D/A unit has also been completed and is based upon the Analog Devices AD7568 Octal 12 Bit DAC. The D/A unit includes circuits that enable the sound processor's DSP chip to prevent current stimulation until the entire portable processor system is operational and all internal tests are completed successfully. At the present time a power conditioning MCM layout has also been completed that is based upon a single DC to AC conversion oscillator circuit that is transformer coupled to provide isolated outputs that are rectified and smoothed to provide the required voltages.

Figure 2 presents the MCM subsystem layout. The figure shows each of the MCM units arrayed on the final substrate. The upper left hand unit is the voltage conditioning circuit which includes a small toroidal transformer and a voltage converter IC (the MAX 763) used to generate the oscillatory waveform which drives the transformer outputs. The three units arrayed along the top next to the voltage conditioning circuit are the MCM stimulating units (two V/I circuits each). Finally, the circuit spread out along the bottom margins of the substrate is the D/A unit. The entire substrate assembly is roughly 4.5 x 8.5 cm and will occupy one side of one of the two boards that comprise the present portable speech processor.

These subassemblies should be available in late 1997.

3.0 Future Work

Next Quarter we plan to continue work on the design and layout of these MCM subassemblies and their integration with our wearable sound processor units.

Effort will also continue to be directed at normal loudness growth (NLG) mapping functions. We have added a second software program that uses NLG mapping functions with the CIS processor implemented in the Geneva Wearable Processor (GWP) of two Ineraid subjects and plan to extend this to a total of at least five. We are also conducting additional laboratory studies using NLG mapping functions to determine how loudness

grows for tone frequencies positioned at the boundary of two processor channels and for broader band inputs like speech and speech-shaped noise. We hope that these investigations will lead us to refined NLG mapping functions that will improve the listening experience of a large number of subjects.

We are also analyzing the speech reception results we have accumulated with the 18 subjects using the GWP/MIT systems. Virtually all subjects have reached six months with that system. We will also begin longitudinal studies where parameters like stimulus rate, phase duration, and preemphasis will be altered in the eleven subjects not participating in the study of NLG mapping.

In the laboratory, we have revived our high-rate stimulation studies that were halted as we directed effort toward beginning the longitudinal testing program with the GWP/MIT system. We are analyzing the results from tests with our first, bilaterally implanted subject and plan to schedule another experiment later this quarter.

Figure Captions

Figure 1. Schematic of two Draper Laboratory voltage-to-current source (V/I) converters. The figure is divided into three segments by the vertical dashed lines. See text for explanation.

Figure 2. Layout of the subassembly that includes the power condition unit, three V/I units and the D/A unit. Each of the individual units uses multi-chip module (MCM) technology to increase the circuit density. The overall size of the subassembly is approximately 4.5 x 8.5 cm.

Bibliography

1. D.K. Eddington, V. Manzella, W.M. Rabinowitz, M. Svirsky, J. Tierney, and M.A. Zissman, Speech Processors for Auditory Prostheses, Fifth Quarterly Progress Report, (Cambridge: MIT Research Laboratory of Electronics, 1993).

Figure 1

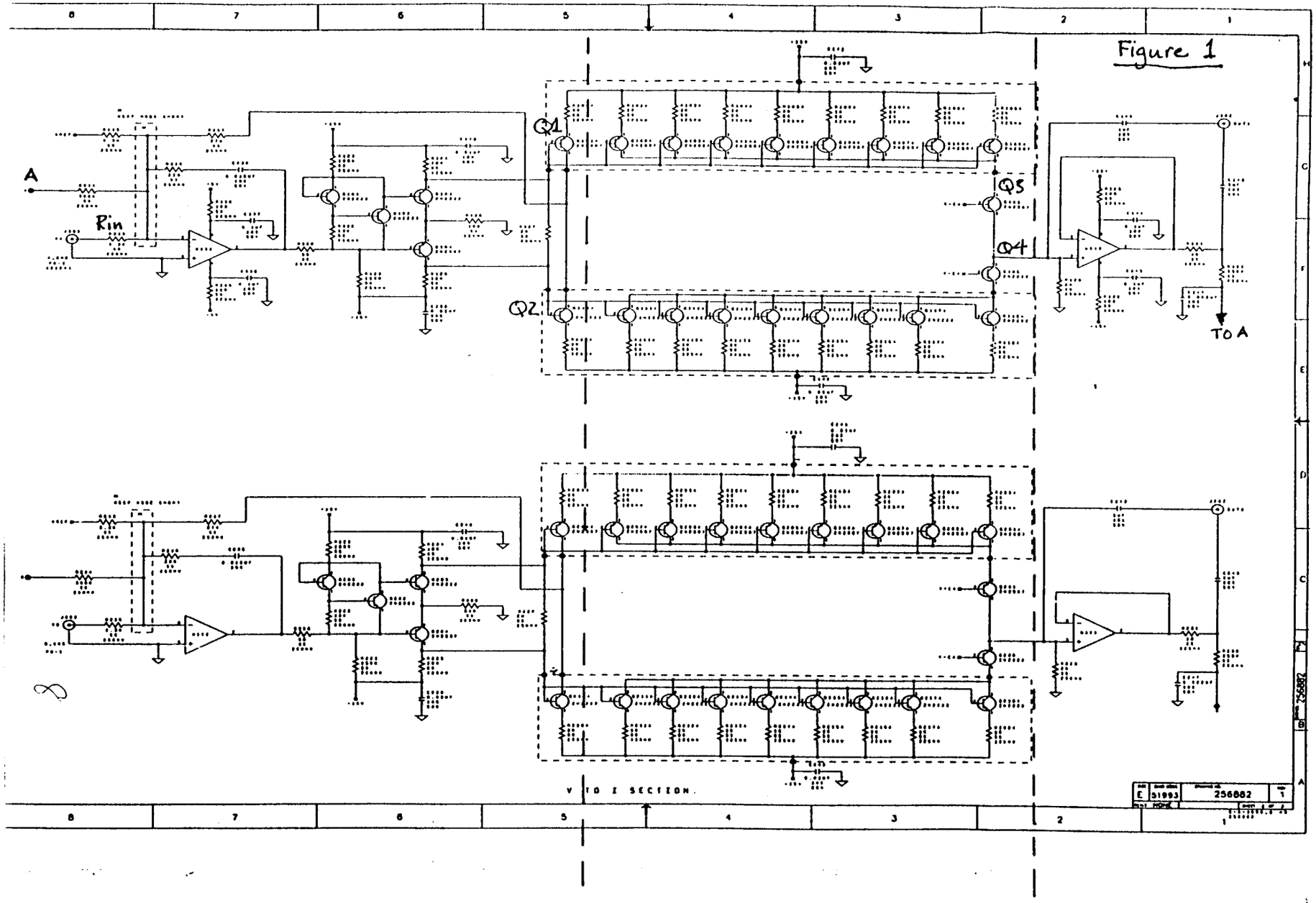

Figure 6