Executive Summary
Workshop on Silicon Nanoelectronics and Beyond
October 28-30, 2003
Intel's Jones Farm Conference Center
Hillsboro, Oregon

A. Introduction

The semiconductor industry has established an aggressive goal to continue Moore's Law scaling for the next fifteen years, obtaining features sizes below 10 nanometers in the limit. The array of technology challenges faced by the industry if it is to achieve these objectives are formidable and certainly involve the creation and manufacture of objects whose dimensions are within the feature size regime of nanotechnology. In this workshop, specialists were convened from government, industry, and academia to examine the role that research sponsored by the US National Nanotechnology Initiative (NNI) might play in addressing some of the challenges faced by the industry. The intent was to initiate a dialog between these three communities with the goal of creating a partnership that can more effectively address the problems industry must overcome in order to follow the technology schedule advocated by the 2003 International Technology Roadmap for Semiconductors (ITRS) (http://public.itrs.net/).

The list of workshop attendees and the agenda can be found on the SRC web site at http://thehub.src.org/SRCForums/dispatch.cgi/f.siliconnano. (Password required)

The workshop was characterized by a spirited discussion among members of the eight panels and the audience. In the following, we attempt to capture the essence of some of the discussions but in the interest of brevity, we do not provide a detailed account of each panelist's presentation. PDF versions of all but one of the presentations can also be found at http://thehub.src.org/SRCForums/dispatch.cgi/f.siliconnano. The overall assessment of the discussions at the workshops is that while the time horizons of the NNI Program stretch beyond the end of ITRS, there are many points of confluence between the technologies required by industry and the work of NNI researchers. Workshop attendees identified some of the salient technical challenges facing the semiconductor industry as it strives to meet the ITRS 2003 cadence and as it develops new technologies to augment and perhaps ultimately replace CMOS. A significant investment in fundamental research is needed to address these challenges.

Salient Technical Challenges: (Not prioritized)

- Materials, processes and device technologies to extend CMOS to the end of ITRS scaling
- Existence theorem for proposed materials that meet a behavioral specification
- Predictive knowledge base and experimental fabrication infrastructure for the design of materials satisfying behavioral specifications
- Basic understanding and demonstration of system configuration with reversible computing to reduce the power dissipation.

- Alternate to von Neumann Computing, such bio-inspired computing or quantum computing etc.
- Identify new computational state variables that are scalable and that leverage CMOS infrastructure
- Materials research for phonon engineering and ballistic heat removal
- Models for beyond-CMOS devices usable for simulation at the circuit and higher levels
- Test for nanotechnology-based systems and a new understanding of the construction of reliable system architectures from un reliable components
    - Fine-grained, real-time reconfigurability and sophisticated on-line monitoring and self-testing
    - Software that is largely self-assembling and evolving
- Synthesis of circuits and systems with new technologies taking advantage of little understood capabilities
- Directed self-assembly (additive process) to create desired structures in required materials
- Integration of "engineered" materials and associated structures on a CMOS platform
- Characterization of materials and structures at atomic scale, both in-situ and ex-situ, to ensure cost-effective, reliable fabrication of devices/products
- Broadly-based hierarchical modeling and simulation of nanotechnology processing and nanodevice performance to guide experimental trials
- Resolution of the contact issue between nanodevices and conventional charge transport interconnect systems

There is a clear need for a coordinated and cohesive national program of significant scope to meet these and many other challenges identified in the sequel. The following material follows the format of the workshop and highlights some of the discussions offered in each panel session.

B. Session Summaries

I. Materials by Design

Problem Statement

The information processing industry is entering a period where conventional material and manufacturing technologies appear to offer diminishing returns, threatening the future of conventional scaling. Within five to seven years, the ITRS calls for the heterogeneous integration of many new materials or transistor components, including: channel, high K, gate stack, metal electrode, low K, interconnect, contact and interface, packaging, resist materials, and new nanopatterning technologies into mainstream semiconductor manufacturing. Yet, it is becoming increasingly difficult for known bulk material systems and processes to address the projected dimensional, performance, energy management, and manufacturing requirements. In fact, the bulk material properties that drove macroscopic device designs are giving way to emerging surface and interface-

dominated effects in nanoscale electronic materials and device systems. Over the next decade, new market opportunities also will drive the heterogeneous integration of novel materials, sensors and systems on a silicon platform. Functional density, or the overall productivity of designed functions, may replace transistor density as the key technology driver. However, new materials or fabrication processes typically undergo a decade or more of research and development before qualifying for insertion in mainstream semiconductor manufacturing and establishing a critical support infrastructure. The lack of new materials that satisfy projected performance and insertion timing requirements and the lack of robust and affordable nanoscale fabrication options create tremendous technological risk for the industry. The convergence of these risk factors between 2007 and 2010 represents what some are beginning to call a technological perfect storm.

Within the next seven years, the information processing industry needs an interdependent predictive modeling, design, characterization, and experimental materials assembly infrastructure sufficient to anticipate and satisfy future structural, functional, and integration requirements. Such a predictive design and directed self-assembly capability for nanoengineered materials could:

- Sustain the scaling of CMOS manufacturing technology to its ultimate limit;
- Provide alternative, scalable, and sustainable benign-high performance materials and manufacturing technologies for CMOS alternatives;
- Create options for integrating heterogeneous nanoengineered functional materials with CMOS technology, enabling a commercialization path for nanotechnology innovations.

Vision

Materials by Design represents a high impact initiative, which would focus our strengths in materials, characterization, and modeling on developing a foundational knowledge base and predictive modeling infrastructure for designing nano- and molecular scale electronic materials. It leverages the chemical industry's 2003 R&D Vision and Roadmap for Nanomaterials by Design: From Fundamentals to Function, summarized elsewhere at:http://www.chemicalvision2020.org/nanomaterialsroadmap.html. This vision asserts that by 2020, "the U.S. chemical industry will offer (its industry) a 'library' of diverse, high quality nanomaterial building blocks with well-characterized compositions, stable architectures, and predicted properties. Safe, reproducible, cost effective, and clearly defined manufacturing and assembly methods will be available to incorporate nanomaterials into [nanoelectronic] systems and devices designed to perform specified functions while retaining nanoscale attributes." The proposed initiative would help create of new classes of functional nanoengineered electronic materials and fabrication options that enable:

- Design and robust fabrication of affordable, sustainable, high performance electronically useful graded composites, such as advanced gate stacks, integrated source-channel-drain systems, and materials that transcend the front – back end dichotomy of current microelectronic technologies;
- Robust integration and directed self assembly of heterogeneous materials onto a silicon platform, such as for communication, sensing, tracking, bio-medical other

information processing applications, with zero defects and reduced material and process variability;

- Discovery of novel 3D nanomaterial systems, with deterministic architectures for remote low power applications and enhanced information processing functionality per unit cost.

Hard Problems

(See also Appendix I for similarities to the Chemical Industry's Priority Research Requirements for Nanomaterials by Design.)

Near Term: A critical near term problem is to search for new material families and nanomanufacturing processes to make the components for Si CMOS devices. Examples include meta-stable materials, gradients and composites for e.g. FET gate stacks and channels. Over the next few years, new robust zero defectivity, gate dielectric materials will be needed which minimize gate leakage current, while preserving channel mobility. A similar challenge exists for mechanically robust metal/low K dielectric (K<2) materials systems that could enable future inter-level interconnect technologies. Future interconnect materials must be highly conductive, with low contact resistance, and exhibit low stress and electromigration. A significant question that a 'Materials by Design' capability might answer is, "Is it possible to design into known families of gate electrode materials the property of a continuously variable work function? "

Another important domain is processing materials, such as novel resists. For example, high frequency line edge roughness, long-range dimensional variability, and diffusion effects in today's chemically amplified resists are pointing to a high volume manufacturing red brick wall for sub-40 nm resist and patterning technology.

Intermediate Term:

a. Low variability fabrication of useful nanomaterials: With dimensional scaling, nanoscale materials variations increasingly will challenge process control technologies. Is it possible to fabricate billions of identical nanoscale electronic devices or functions on a chip?
b. Contact Engineering: In the sub 20 nm regime, treating nanoscale contacts as welded bulk material interfaces no longer will suffice. The challenge of engineering rigid interfaces with desired electronic properties between dissimilar conducting or semiconducting materials warrants molecular scale material design consideration.
c. Characterization and metrology of nanomaterials and graded composites: Known characterization and metrology capabilities are approaching their limits. No known solutions exist for addressing the real time, non-destructive characterization requirements of deep nanoscale materials and nanostructures, such as composition, dimensionality, defectivity, and functionality at the nano, molecular, and atomic scales.

Long Term: Perhaps the Grand Challenge of Materials by Design is to predict and realize the existence of an optimal material that satisfies a given set of specifications or to infer new functionality from a given material composition and structure.

Potential Solutions

The following are representative examples of high risk and potentially high impact near, intermediate, and long term research opportunities:

Near Term: Evolutionary material and process enhancements that enable fabrication of CMOS nanostructures. One example is directed self assembly of resist materials for addressing the resolution, placement, throughput, dimensional variability, and line edge roughness challenges facing conventional lithographic technology. Another example is engineered copolymers and composites. This includes patterned polymers, such as block copolymers or dendrimers, and may warrant consideration as dielectrics or hosts for conducting materials. They also may serve as candidates for integration into other electronically useful composite or interface structures.

Intermediate Term: Novel materials and processes that enable affordable fabrication and extensibility of CMOS nanostructures, especially alleviating the exponentially increasing challenges facing conventional lithography. Examples include, but are not limited to:

- Resistless patterning: Directed additive deposition or anisotropic growth of electronically active materials may enable affordable extensibility of MOSFET technology into the deep nano-domain.
- Single atom electronic materials: This area explores and develops a foundational knowledge base in material and fabrication options, such as nanoscale channel engineering, deterministic doping, atomic scale assembly, etc., that overcome current ITRS identified barriers and enable novel information processing technologies.
- Contact engineering: Foundational and combinatorial conducting materials studies should be directed towards creating design principles for optimal low resistivity contacts,
- Heterogeneous material integration within CMOS platforms: Design active non-silicon materials that exhibit desired field, strain, or interfacial electrical properties.

Long Term: A strategic goal is to create a critical predictive knowledge base and experimental fabrication infrastructure to guide the design and an efficient search for materials with desired functionality. Also, directed self-assembly (DSA) may provide a viable alternative for affordably fabricating sub-40 nm nanoelectronic materials and structures. If successful, DSA-by-design would enable nanoscale manufacturing methods that exhibit orders of magnitude improvements in cost, performance, and process variability, relative to the end-of-ITRS CMOS technologies. Bio-inspired methods may offer new solutions for manufacturing and materials design. These methods seek to achieve a desired functional performance specification by leveraging information

rich, environmentally benign, bio-like DNA/RNA construction methods to synthesize 'programmed' materials.

II. Functional Nanostructures

Problem Statement

In order to continue to increase of functionality per unit area or volume of a material structure, approaches other than scaling of binary switches may be needed. Is it possible to design and fabricate engineered nanostructures with complex input-output behaviors that go beyond the Boolean logic gate? In principle, functional nanostructures could perform certain functions such as sensing, storage, communication, processing, etc. by using the magnetic, electronic, and photonic properties of the nano structures. The fabrication of functional nanostructures should lend itself to cost-effective techniques that for example would require minimal lithographic information, e.g. by using self-assembly.

Vision

Functional nanostructures could utilize interactions between different physical state variables, e.g. electrical, magnetic, optical, spin, etc. to realize novel and integrated functionality, and thereby accelerate effective scaling. For example, the architectural separation of memory and logic in modern day digital circuits is an artifact of technology that drives computer structures and therefore performance. Perhaps a new functional device that could be used either as a memory or as a logic element could enable architectural innovations so that artificial physical separation of memory and logic would not be required. Such an approach might be achievable by utilizing spin, magnetic and electric properties of matter in a nanostructure design. This approach could be extended to a universal logic-memory-sensor cell. As another example, the interface between inorganic and biological systems could require a device that responds to ion transport in the cell to produce an electric response and conversely.

Most explorations to date have focused on using functional nanostructures as *component replacement* for existing devices or entire functional blocks. For example, in molecular electronics, *Moletronics Programs*, funded by DARPA, a 64 bit molecular cross bar memory has been demonstrated (molecules are used as resistive memory element). As another example, there are proposals to use molecules or carbon nanotubes (CNT) to make channels in FET-like devices.

The question remains open, however, with respect to the best direction to pursue for functional nanostructures, e.g., carbon nanotubes, molecules, etc.)? Most of the applications of CNT's to date have been used in attempts to improve existing devices, e.g., as a replacement for the MOSFET channel. It appears that these applications of new functional materials could provide marginal performance increases relative to standard MOSFET materials but innovative utilization of CNT's could offer significant expansions in device functionality.

Hard Problems

The hard problem in this area is the conceptualization of a nanostructure with multiple modes of sensing (input) and response (output). This extends to the concept of using and manipulating alternative state variables to represent information.. There is also a need for tools that utilize the existing knowledge base for nanostructures and deep material knowledge to synthesize functional nanostructures whose input-output characteristics meet specifications.

Potential Solutions

There are many nanostructures with interesting and perhaps useful functional properties, including carbon nanotubes and nanowires, quantum dots, molecules etc. One of the most important enabling technologies for functional nanostructures will be the *Directed Self Assembly for heterogeneous integration with Si platforms.* This will include e.g. engineered heterogeneous dielectric layers and composite nanodot-in-insulator materials for advanced non-volatile memory, dendrimers for photonics/semiconductor hybrids, exploration of self-healing, adaptive and bio-semiconductor hybrid structures, and structures capable of recruiting of components, templating, error-correcting, and defect-tolerant systems.

III. Thermal Physics at the Nanoscale

Problem Statement

A critical challenge facing the semiconductor industry is to maintain the trend in power and performance efficiency. The technology scaling and dense packing of nanoelectronic components for information processing results in increased levels of dynamic and static power dissipation and therefore, heat. The heat issue is getting more complex as we add new materials such as SOI, High K gate dielectrics and increase layers of interconnects and 3-D integration. Therefore, charge-based electronics is likely to create very high power dissipation and heat generation. Indeed, the estimated levels of generated heat may exceed 1000 W/cm^2, which is approximately the capability limit of known heat removal systems. The excessive heat generation may create a “thick red brick wall” in the ITRS for the CMOS scaling and the future CMOS platform. The power dissipation/heat generation on chip may become “a bottleneck or even a night mare” of the ITRS.

Vision

In principle, there are three approaches to addressing the heat problem:

1. **Minimize Power Dissipation:** The technology revolution and evolution path from “Vacuum Tubes to Transistors (Bipolar) to NMOS to CMOS” has been primarily driven by the issue of power dissipation. The CMOS scaling and systems design has always emphasized optimization of energy. The low power characteristics of CMOS systems have given us the ability to achieve giga-scale integration with billion MIPS computing power. This approach includes

minimizing energy consumption on the level of individual device, such as binary switch (e.g. FET) and systems level improvement/using new computational paradigms. However, it is unlikely that any alternative binary switches such as e.g. single electron, molecular, carbon nanotube devices can operate at much lower energy in practical circuits, than CMOS devices. Moreover, even at the fundamental limit of k_BTln2 per bit operation for electron transport devices, heat generation theoretically could reach MW/cm^2 for dense arrays of switches few nm in size operating at attainable switching speeds. *Therefore, it is necessary to design extremely low power systems or shift to new paradigm of computing; such as, adiabatic/reversible computing, or bio-inspired computing.*

2. **Optimize heat distribution:** The overheating problem can be relieved to some extent by minimizing hot spots on the chip. One approach to minimize hot spots is to include this as a constraint in the design of the circuit layout. Another possibility would be to adapt the circuit in response to heat loads.
3. **Maximize the rate of heat removal**: Current state of the art indicates that highest values of the heat transfer coefficient for devices operated at temperature less than 400 K can be achieved by using liquid forced convection and phase change/boiling methods. Experimentally, 790 W/cm^2 was demonstrated by forced water convection cooling of a uniformly heated Si substrate with embedded microchannels and 700 W/cm^2 has been demonstrates by thermoelectric cooling. In practical solid-state information processing systems the upper limit of heat removal would be lower due to concentration of heat sources in local areas of the system and hetrostructure interfaces.

Hard Problems

The power dissipation, heat generation and heat removal is an intertwined system, circuit, device, materials and packaging problem. The key problem arises from the very nature of information processing and can be described as *the barrier* and charge transport *dilemma.* Energy barriers are key components used to *information flow* in electronic information processing systems. Barriers are needed for charge transport to enable distinguishability of binary states. These barriers are made of hetrointerafces. The hetrointerfaces impede the transport of phonons. As a result the heat removal rate from the heterogonous materials system is considerably smaller than from a homogeneous solids.

Potential Solutions

Systems/Circuits Architecture/Design Research: The traditional approach to low power system design is centered around low voltage scaling. However, due to off-state leakage the threshold voltage (V_{th}) and power supply voltage (V_{DD}) does not scale linearly with technology nodes. Mixed V_{th} and power-managed system on a chip (SOC) architectures can help to reduce the power dissipation. In the short term, it is imperative that tools be developed to enable the designer to layout the physical design so that hotspots are avoided. Moreover, new adaptable circuit configurations are needed that minimize power consumption. The other major source of the power dissipation is interconnects. The ITRS projects that with technology scaling, about 70-80% of the total

power may be dissipated in interconnects. The traditional solutions have been to reduce the operating voltage, interconnect resistance and parasitic capacitance. However, these solutions are reaching their fundamental limit. In the longer term, radical alternatives to computing/system configuration are required to face these challenges. For example, the notion of dissipationless or reversible computing has been postulated by a number of researchers for several decades; yet no manifestations of these machines exist. To what extent, can this theory inform the design a low-energy consumption circuits? A second longer-term avenue that should be pursued is that of bio-inspired computation. It is well known that the brain is a very efficient at solving some tasks while utilizing relatively little energy. The brain processing power is about 10^{16} MIPS with 10-30 Wattts. Today's best computer processing power is about 10^{9} MIPS with 150 Watts. Could we learn a new information processing methodology from brain? How neurons communicate with each other (interconnected)? Are there organizational or operational principles that could guide the design of more general information processing systems?

Device/Technology Research: Nanoelectronic devices are likely to operate at time and length scales on the same order of magnitude as the thermal equilibration times and phonon mean free paths. In this regime, the conditions for thermal equilibrium are marginally satisfied and classical transport theory does not apply. In the short-term, it is necessary to invoke detailed phonon transport and coupling models to understand the macro-scale thermal transport phenomena. In the long term, we may need to develop alternate to charge-base electronics. A new information processing could exploit a completely new means of "state variable" for information primitives, such as spin or phase of a wave function. A significant basic concept level research needs to be done to demonstrate the performance power trends of the emerging novel information processing technologies,

Materials Research: There are two aspects of materials research for scaling. The first is to optimize the performance power trend such as, High K gate dielectric to reduce leakage and therefore, standby power dissipation, or Low K inter-level dielectric to reduce parasitic capacitance and therefore, dynamic power dissipation. The second aspect is, materials research required to remove heat from integrated circuits. As shorter-term solutions, microfluidic and superlattice technologies show promise. New creative implementations of these technologies may enhance the maximum heat removal rate from practical solid-state circuits to several hundreds W/cm^2. One example of such new implementations is the use of distributed fuel cells employing microfluidic channels with methanol/water mixture as energy deliverer and heat remover. Another example is on-chip integrated thin film superlattice thermoelectric coolers for hot spot management. In longer-term perspective a broad strategy must be implemented to address more generally the problem of *heat removal from terascale complex matter*. Finally new ideas are needed that enable heat removal at rates that are orders of magnitude greater than techniques known today. For example, the feasibility of ballistic methods for heat removal such as stimulated phonons/heat lasers, solitons, photon emission and photon engineering concepts should be explored.

IV. Tools and Methodologies for Nanoelectronic Design

Problem Statement

Nanoelectronic design issues are all about complexity, whether it be the number of components (billions), the molecular nature of these components, or the scale of applications that will be run on nanoelectronic systems. They include the management of power dissipation, parameter variability, parallelism, definition of effective and efficient test methods for complex functional structures, design for reliability, and design across heterogeneous technologies. As an example, high-level design tools have relatively poor estimates of parameters affected by layout data. In today's ASIC design, we see examples in which designers need ten iterations of place, route, extract, and timing estimation before closure of the design is achieved. At the full chip level, this requires a run time of about one week per iteration, clearly impacting design cycle time significantly.

The role of design can no longer be limited to circuit and system levels but instead must occur across almost all levels of the technology from materials and processes through devices and packaging. As we consider the end of CMOS scaling and the advent of new technologies that will be used to supplement or supplant CMOS in mainstream applications, the challenge is to develop efficient methodologies that migrate from mainstream design tools in use to new tools and methodologies for as yet undefined devices and systems. Part of this challenge involves retaining the advances in design that tools have allowed in traditional CMOS while at the same time leveraging radically new (and not yet fully formed) properties of new technologies. As an example, device simulation has proven its value in device research and technology development, but it now faces the challenge of treating devices at an atomistic level. A broad understanding of the science of conduction at the molecular scale is developing and theory and computation are playing an important role in nanoelectronics research. But until we develop high-quality, public-domain models of these devices, they will not be able to move out of the device lab into the IC design shop.

In the following section, we will focus primarily on design issues at the circuit, system, and device levels; recognizing as we do this that design questions encompass a much broader domain of application.

Vision

Successful research in circuit and system design tools and methodologies will result in capabilities that reduce design cycle time by more effectively mapping behavioral level design descriptions on to a hierarchy of software/hardware design platforms built upon physics level models while comprehending heterogeneous devices operating in different physical domains. These new tools will provide for effective management of complexity to shorten design cycle times and will be organized in such a way that new device and circuit models are easily integrated. In order to achieve this, the science of the design of complex artifacts needs to be strengthened.

Devices are shrinking to dimensions where the atomistic structure of the matter that makes up the device must be included in device simulation. At the molecular scale, the distinction between materials and device simulation vanishes. Device engineers need to add to their toolkit a new class of simulation tools that treat small electronic devices at the molecular scale. These new tools will complement current macroscopic tools to address key issues for ultimate MOFETS, and they will also provide a consistent basis for interpreting experiments and exploring and designing small electronic devices of almost any kind.

Hard Problems

Most of the novel devices beyond CMOS being proposed today have not been equipped with models of use to the circuit designer that encapsulate the essential functional behavior of the device without resorting to explicit physical models. It is certain that little can be done in the development of CAD tools until such models are formulated. In the CMOS area, work is underway to develop compact models for scaled CMOS for several of the anticipated future structures. The problem here is that some of the desirable properties of CMOS (such as off-current) are degrading with scaling and device parameters are more stochastic in nature due to manufacturing variations in the nano-dimension regime. Approaches are needed to handle both the power and variability problems for nanoelectronic devices.

At the system level, the need for flexibility and hardware re-use will require the inclusion of significant amounts of embedded software. Tools for the co-design of software and circuits have historically been limited by the different world-views of software and hardware developers. In devices and circuits, variables interact in a continuous manner whereas, software is often procedural in nature and the representation of concurrency is at best fragile. In software, what flows though is control while in hardware, data flows through. It appears that the platform approach to design that has been successful in facilitating design reuse and design efficiency, could be extended to comprehend embedded software design via the use of synchronous or ‘actor’ software models that more nearly emulate the hardware descriptions of components. In effect, this calls for the creation of an intermediate level platform bridging between applications platforms and programming language platforms.

When some of the new research devices become available for use with CMOS, e.g. on the same chip, design tools including models will be needed to support this hybrid environment. It is likely that the variability of literally billions of new devices combined with the variability of extreme CMOS devices will be significant. This may drive a departure from the perfection now assumed for integrated circuit manufacturing. There is a school of thought that the only viable resolution is to essentially ‘program’ the chip for the desired functionality after it has been fabricated. Mechanisms would be needed to utilize test results to organize the configuration of the functional circuit and perhaps to provide for real-time adaptation of the circuit during applications. (This is a departure from traditional integrated circuit approaches where the reliability of circuits containing,

although not using dysfunctional elements, is viewed as suspect.) Moreover, it is not known if the times required to 'test in the design' are practical for billion device systems.

In the device modeling area, the scientific understanding of conduction at the molecular scale is still developing, and there are several hard problems that need to be addressed within the context of rapidly advancing experimental work. One class of problems has to do with the multi-scale, multidisciplinary nature of the problem, and the other involves dealing with computational demands. An example of the first kind is the treatment of the molecule (or device) –metal interface. Chemists use basis functions that over the years have been developed to give accurate description of the electronic structure of materials. Surface physicists use different basis functions to describe the electronic structure of surfaces. To treat contacts, we need to develop ways to make use of the best work in these two different fields. Most treatments to date assume coherent transport, but learning how to represent vibronic excitation in molecules (or phonons on solids), is important and greatly increases the computational burden, a problem of the second kind. And finally, there is more to the problem than just electronic conduction. One would like to see device simulators capable of handling optoelectronic, spintronic, thermoelectric, etc. effects as well, and all within a consistent theoretical and computational framework.

The general issue of multi-scale simulation is a hard problem that needs to be addressed. Ab initio simulations are necessary for some problems (e.g. understanding the details of surfaces and interfaces), but device models will necessarily be semi-empirical. Even simpler models will be needed to assess the circuit and system implications of novel device. Learning how to traverse this multi-scale hierarch seamlessly is a challenge that should be addressed.

Perhaps the greatest challenge will be managing power dissipation. Nano chips (whether CMOS or otherwise) will not be able to run in the traditional mode in which all devices can be operated continuously at maximum speed. At any point in time, most of the chip will necessarily be shut down. New design flows and tools will be required to monitor power and implement aggressive management techniques that reduce dissipation during non-critical operations.

Potential Solutions

Research in circuit and system design must occur concurrently with that of the synthesis of new devices. This is not a traditional view because designers usually need the existence of stable and well-modeled artifacts before tools can be developed to support the design process, or for that matter, before functional systems can be designed. This challenge is not intractable for there exists a wealth of ideas on approaches to design tools and methodologies for future integrated circuits and systems. An essential ingredient for successful exploitation of emerging research devices to for broad new applications is close collaboration between industry and academic researchers.

Management of complexity will depend on the successful creation of new design platforms that insulate the high level designer from low level details. These may include

application specific parallel architectures that support a tractable programming model (e.g. actors); reconfigurable architectures that allow hardware re-use across applications, simplify testing and improve yield; and modeling platforms that understand parameter spread and allow for intelligent performance/yield trade-offs.

Research is needed on the science of devices at the nanoscale – theoretical formulations, numerical approaches, and team efforts that involve theory, computation, and experiments. Mechanisms need to be developed to embody this research in computational nanoelectronics into high-quality software that can be shared within the community is a harder problem too address. Resolution is essential if rapid reduction to practice by industry is to be achieved.

V. Nanodevices To and Beyond the End of Silicon CMOS Scaling

Problem Statement

The quickening pace of MOSFET scaling is accelerating introduction of new technologies to extend silicon CMOS down to the 22-nm technology node. To sustain the semiconductor industry's historical scaling of information processing technology by 4x every 2 – 3 years, this acceleration simultaneously requires the industry to intensify research on two highly challenging thrusts. One is scaling CMOS into an increasingly difficult manufacturing domain well below the 45-nm node, and the other is an exciting opportunity to invent fundamentally new approaches to information and signal processing to sustain functional scaling beyond the domain of CMOS.

A variety of promising non-classical CMOS and CMOS-compatible technologies are proposed to extend the performance (speed, integration density, etc.) of integrated circuits another factor of 10x within the next 10 – 15 years, reaching the end of the new 2003 International Technology Roadmap for Semiconductors (ITRS). Beyond that time one or more new information processing technologies will be needed to extend CMOS to completely new domains of application. The critical issues are to 1) explore, select and further refine those "non-classical" materials and structural enhancements necessary to scale CMOS to its fundamental limit, and 2) invent, explore and demonstrate new CMOS-compatible information processing technologies that will extend functional/performance scaling another 100x or more.

Vision

A variety of non-classical materials, process and structural changes currently are being explored for extending nanoscale CMOS down to and, perhaps, beyond the 22 nm technology node (physical channel length < 10 nm). These changes will likely include a new gate stack including high-k gate dielectric and metal gate electrode, an ultra-thin body SOI structure eventually leading to a double gate structure, and a quasi-ballistic channel using a completely new channel material and/or structure (e.g., carbon nanotube, silicon/germanium nanowire or III-V nanowire on a silicon/germanium substrate).

Extension of microelectronics beyond the domain of CMOS- dominated applications will require a new information processing nanodevice technology that is compatible with CMOS (integrable and/or functional) and which provides an additional scalability of 100x or more over an extended period of time (20 or more years). Such a new information processing technology will likely supplement rather than replace CMOS. In the near term, this new technology should preserve as much as possible, the elements of CMOS, such as the charge-based state variable, design and architectural methodologies and tools. The question remains open, however, what is the best direction to pursue for such functional nanostructures, e.g., carbon nanotubes (CNT's), silicon or germanium nanowires, III-V nanowires on silicon/germanium substrate, molecules, etc.? Most of the applications of CNT's to date have been used in attempts to improve existing devices, e.g., as a replacement for the MOSFET channel. It appears that these applications of new functional materials will provide only marginal performance increases relative to standard MOSFET materials.

In the longer term, however, a new information processing technology could exploit a completely new means or "state variable" for representing the information primitives, e.g., the phase state of a wavefunction representing a quantum qubit. Such a nanodevice technology can play an important role in extending CMOS by adding new functions, which would be otherwise too difficult or too costly to implement in CMOS. Preferably, the research focus should be on conception and fabrication of nanostructures in silicon, to maintain compatibility with silicon CMOS.

Hard Problems

The hard problems in nanodevices to and beyond the end the scaling of silicon CMOS include the following.

- *Extend CMOS to end of ITRS scaling:* Introduction of 2 or more innovations to the CMOS materials, process and/or structure [e.g., replacement of the conventional gate stack (polysilicon electrode/silicon oxynitride dielectric) with a new high-K gate dielectric plus a new metal gate electrode]. Realization of atomic-scale materials and process technologies integrated with new MOSFET structures (e.g., multiple-gate FETs) with required control of processes and structural parameters [e.g., fabrication of ultra-thin silicon layers (< 10 nm) on insulator for UTB-SOI MOSFET's and line-edge roughness of physical gates]
- *New Information Processing Technologies:* Invent a new technology paradigm for information processing that is in the near term compatible with CMOS and, in the longer term, provides function/performance scaling of >100x over a period > 20 years

Potential Solutions

- *Extend CMOS to the end of ITRS scaling*: Potential solutions for extending CMOS to the end of the IRTS include:
    - Ultra-thin body SOI [silicon body thickness < 10 nm]
    - Double and multiple gate MOSFET structures

- Quasi-ballistic channel using nano-structures [e.g., CNTs, silicon or germanium nanowires, or III-V nanowires integrated on silicon/germanium substrate, etc.]

- *New Information Processing Technologies:* Potential solutions for Memory and Logic include:
  - *Memory*: A strong theme is to merge one or more memory options (e.g., nano-floating gate memory) into a CMOS technology platform in a seamless manner. Memory mechanisms include charge isolated by surrounding dielectrics; charge held in place by Coulomb blockade potential; resistance change caused by chemical phenomena; and resistance change caused by material phase change.
  - *Logic*: Invention and reduction to practice of one or more nanoscale device logic technologies that at once provide a minimum of 100x functional and performance scaling and are also functionally compatible with silicon CMOS. Functional nanostructures could utilize interactions between different physical phenomena, e.g. electrical, magnetic, optical, spin, etc. to realize novel and integrated functionality, and thereby accelerate effective scaling. For example, the separating of memory and logic in modern day digital circuits is an artifact of technology that drives computer structures and therefore performance. Perhaps a new functional device that could be used either as a memory or as a logic element could be designed so that artificial physical separation of memory and logic would not be required. Such an approach might be achievable by utilizing spin, magnetic and electric properties of matter in a nanostructure design. This approach could be extended to a universal logic-memory-sensor cell. An attractive example includes use of nuclear spin or a combination of electron and nuclear spins to realize an energy efficient logic architecture based application of the "exchange potential" to manipulate these particle spin states

VI. Integration of Nanodevices on the Silicon Platform

Problem Statement

Integration of nanodevices on the CMOS silicon platform provides an opportunity for major advances in performance, as well as expansion of applications, of IC technology. However, new structures incorporating nanodevices will still be required to meet CMOS compatibility metrics including energy efficiency, scalability, sensitivity to parameter variations, room temperature operation, reliability, stability, and others. One can think of semiconductor technology as composed of a structured set of technology layers that together enable the design and manufacture of an IC product, e.g., materials, processes, devices, circuits, CAD tools, power delivery and cooling, assembly, system, software, etc. The *Horowitz Technology Filter* postulates that the sphere of successful impact of a new technology is +/- one technology layer. Indeed, a change in one or perhaps two layers is relatively easy, requiring an R&D effort spanning about 2-5 years, while a change across many technology layers can require as much as 6-20 years of R&D. Thus,

when we think of introducing a new technology such as nanodevices into CMOS, we need to carefully gage the degree of impact that this introduction will have on CMOS technology layers.

Vision

It is anticipated that new CMOS based circuits incorporating nanodevices will allow major advances in circuit and system-level exploitation and support their use in large numbers, while preserving the existing CMOS infrastructure. These devices will be compatible with silicon CMOS process temperatures, materials used in the CMOS process, CMOS process sequences, wafer sizes, and will support a seamless connection to CMOS devices. The nanodevice technology will also be compatible with, and fully exploit, the rapidly evolving CMOS process technology that will include Atomic Layer Deposition, Extreme Ultraviolet Lithography, supercritical CO2 cleans, and perhaps limited forms of directed self-assembly by the end of the present decade. The CMOS based technology that incorporates nanodevices will meet the attributes of useful digital devices including: the output of one device can drive the input of a second device, signal level can be continuously restored, circuits are relatively immune to noise, circuits are able to be connected at multiple levels, and they are capable of mass production with good yield. The areas where nanodevices integrated with CMOS are expected to have the largest immediate impact are in low cost, non-volatile, dense memory, sensors, and other system-on-a-chip applications.

Hard Problems

Few of the proposed new electron transport devices (RTD's, SET's, RTT's, crossbars, molecular devices, etc.) emerging from research appear to satisfy all of the criteria listed above for integration on the silicon CMOS platform, at least in their current configurations. All have a relatively large overhead in contacts and interconnects, and many are extremely susceptible to the thermal issues that arise with aggressive scaling. Difficult problems exist in CMOS process and operating temperature range compatibility for nanotubes and molecular devices. Major issues arise in placement of novel nanoelements in needed locations on CMOS structures. Electrical parameters of nanodevice enhanced CMOS are just now beginning to be understood. Developing device modeling and simulation capabilities, and compact models usable in design systems, will require major research investments. Reproducibility of nanodevices sufficient for acceptable manufacturing yield in large-scale circuits has not been demonstrated. Many of the issues described above, along with many others that will surface as the integration of nanotechnology with CMOS develops, must be solved to achieve the goal of continuing to meet the advances needed for devices for commercial and defense applications. The challenge of the present is to sort out and aggressively research the fundamental features that limit the application of these devices in presently envisioned applications, and to continue to look forward to new and novel possible future applications.

Potential Solutions

The incorporation of nanodevices into CMOS circuits may take many forms. Two particularly promising possibilities are 1) to incorporate new materials in place of the MOSFET channel to provide enhanced performance in ultra-scaled CMOS devices, and 2) to develop novel interconnect schemes using nanotubes or nanowhiskers as the interconnect medium. These two possibilities still present major challenges in process and manufacturing technologies, but recent results give good evidence that there are no intractable problems to address. Key needs to make these possibilities become realities are 1) adequate research and development funding to provide a modeling and simulation capability for nanotechnology processing and nanodevice performance, and 2) adequate research and development funding to resolve the many issues in contacts and interconnect construction at the nanolevel. In particular, in the area of modeling and simulation, a capability is needed that allows hierarchical views of processes and device performance. This capability needs to allow high-level simulations to be performed to guide experimental directions towards the most promising alternatives, and detailed calculations to be made to understand the results of experiments and calibrate models. This capability also needs to lead easily into development of compact models of device performance that can be used in device design systems. The modeling and simulation capability developed needs to be broadly based so that it is applicable to a wide range of applications even beyond the incorporation of nanodevices with CMOS technology, not just the relatively simple cases noted in the above applications. The second need noted above is particularly critical for the incorporation of nanodevices as a CMOS component. In the more radical case where nanodevices are used in totally new circuit configurations, it is likely that the interconnect problem will be solved by using the natural interfaces between nanodevices for the interconnects. However, if nanodevices are used only as a component of CMOS devices, then there is a need to provide more conventional contacts between the nanodevices and the CMOS circuit elements. Resolving the contact issue, along with resolving the issues associated with using nanostructures such as nanotubes or metallic nanowhiskers as interconnects, will require extensive experimental and theoretical investigations. The modeling and simulation capability previously mentioned would be an invaluable tool in these investigations, and should be coupled with experimental work directed specifically to the contact and interconnect problem.

VII. Nanoelectronic Fabrication

Problem Statement

Conventional IC fabrication is highly dependent on subtractive and lithographic processes. Some of the limitations associated with these mainstream processing strategies as feature size scaling approaches the end of the International Technology Roadmap for Semiconductors are:

- Ability to control physical parameters and electrical properties at the scaling limits
- Complexity and adverse impact on cycle time
- Costs associated with processes (capital and yield related)

- Testing
- Reliability

Vision

Resolution of these fabrication challenges may require new technologies including:

- Directed self assembly of materials with required structure, properties and physical parameters
- Atomic level control
- Inspiration from biological systems to guide bottom-up fabrication, e.g., DNA
- Integration of radical approaches into CMOS platform
- Introduction of new processes, e.g. ALD, into mainstream manufacturing
- Rapid introduction of new materials in to production environments

Hard Problems

Continued scaling will provide significant challenges to lithography to deliver cost effective pattern transfer with small features and also will require many new materials to continue scaling. Furthermore, as more radical device technologies are developed, they will need to be integrated onto CMOS technologies, and they must be compatible and not degrade the CMOS & interconnect technologies.

Lithography:
The goal of lithography is to replicate a defined feature accurately on a surface with required alignment to predefined features. While considerable resources are being focused on developing future lithography tools, mask making and current resist architectures may limit lithography scaling. First, the conventional mechanism of diffusion of photo-acid will limit the ability to accurately transfer features from a mask to the wafer. Thus, either a new resist exposure mechanism must be developed or a new mechanism for pattern transfer will be required. Furthermore, if optical lithography moves to EUV, the mask cost will only be affordable for high volume products and ASIC products will be restricted to older technologies. Thus, a new mask technology or lithography may be required for ASICs to use the most advanced technologies in the future.

Materials & Devices:
With successive process generations more new materials will be required to replace existing materials that will limit integrated circuit performance and eventually to interface new device technologies to CMOS nano-circuits. When new materials are integrated into a technology, many new process operations and chemicals are required to make the material functional with the integrated process. New materials are currently required for high K gate dielectrics and gate metals, but interconnects and low K ILD materials will need to be developed and integrated. The biggest challenge is the amount of effort and time required to integrate a new material into a CMOS technology. From the time a material emerges from University Research it will take a minimum of 7+ years before it can be included in a new technology, because of integration issues and the large

number of supporting materials and processes that will be required to support it's integration into the process. The challenge is evaluate the wide range of materials & process options earlier for the potential integration issues that may limit usefulness of a material.

Potential Solutions

Lithography

In lithography, research opportunities exist in:

1. Resist mechanisms to extend existing resist architectures to 10nm lines & spaces
2. New resist mechanisms to extend to sub 10nm lines & spaces
3. Explore the viability of imprint technology in a multi-layer pattern transfer evaluation
4. New metrology to rapidly characterize feature resolution and defect identification
5. MEMS programmable mask to enable rapid prototyping or ASIC products

New Materials & Devices

To assess the potential compatibility of new materials and devices with CMOS, it would be important for university researchers to have access to facilities where they can:

1. Fabricate the new materials into older CMOS technologies
2. Fabricate new devices on CMOS wafers to evaluate materials compatibilities
3. Test structures to evaluate the impact of new materials on CMOS devices & interconnects.
4. Standard CMOS test structures with areas assigned for integration of new devices & materials.

Potential Material Research Areas to Support CMOS Scaling

1. Advanced gate dielectrics & gate electrodes
2. Ultra Low K ILDs with high mechanical strength
3. Low loss, dense interconnect materials
4. Directed self-assembly and other engineered materials techniques to facilitate integration of non-CMOS technologies on a CMOS platform

VIII. Novel Nanoarchitectures

Problem Statement

Many of the emerging nanoelectronics devices offer different performance characteristics from silicon CMOS; e.g., some have limited drive capability or little gain, some do not use electron transport for communication between devices, some carry information in states different from charge, some have unusual input/output characteristics, etc. The challenge is to design computing structures that benefit from the properties of these new devices that offer comparable or greater performance than that offered by conventional structures based on known devices. A second challenge is to examine the conventional architectures to determine if alternative approaches might offer relief from some of the problems associated with the degradation of CMOS devices under extreme scaling.

Vision

The tenure of the Intel x86 instruction set architecture for microprocessors is remarkable. All machines in the Intel microprocessor family since the 8086 have been upwardly machine-code-compatible; a program written for the 8086 in 1978 can still be run on the latest Pentium, under any of several operating systems which emulate real mode instructions. Given the tenacity of the x86 architecture, and the huge installed base of application code based on this architecture, it will be challenging to migrate current applications to alternative architectures that are enabled by nanoelectronics advances.
Future research in computing and microarchitectures must focus, not on extensions and refinements of current architectures, but on radically new architectures which exploit the new capabilities and performance of new devices.

If history is a guide, during the inevitable transition from scaled CMOS to nanotechnology, new devices must be compatible with CMOS integration; they must offer gain, power consumption at high device densities must be controlled, they must operate at room temperature, and they must overcome the performance limits of conventional interconnect technologies. At the system level, it will be necessary to support the execution of legacy application code for a very long time. One area where novel devices could have an immediate impact is in the memory area since, for example, about eighty-five percent of a microprocessor chip is consumed by cache memory, and memory content is increasing. While traditional microprocessors have been designed to be "universal," future computing architectures are likely to diverge into several distinct application-driven architectures associated with specialized applications and computing support functions. Some examples include mobile and media-streaming systems, ultra-high clock speed systems, systems that offer a high degree of dependability, and systems that are dynamically reconfigurable for varying applications.

Hard Problems

It is almost certain that the fabrication of nanoscale devices and systems composed of literally billions of components cannot achieve the level of perfection (*i.e.,* no bad components) demanded of today's CMOS technologies. If this surmise is correct, then a major challenge will be to utilize chips with defective or out-of-specification devices to meet product behavioral requirements. It will be necessary to develop the capability to identify portions of a fabricated chip which function properly, and map the desired architecture onto the available resources. Furthermore, it cannot be assumed that long term reliability of new devices will be as good as that of CMOS, so large systems will incorporate extensive online testing and reconfiguration, as devices fail due to single event upsets or wearout. The software, test systems, and reconfiguration architectures necessary to implement such systems pose a major research challenge. Ideally, such architectures and software would be self-organizing, and would evolve in response to their changing environment; failure to develop such capabilities in a timely fashion may pose a major impediment to the deployment of nanotechnology-based systems.

Design and test tools for these new generations of devices have not been addressed and, if current CAD tools are not extensible to design with emerging research devices, a substantial investment in design infrastructure will be required. The challenge is multi-faceted. CAD algorithms today are at the breaking point due to the huge complexity of current designs, and this will only become worse over time. Models for emerging devices will have to be developed concurrently with the devices, and rapidly incorporated into design tools for evaluation of new system architectures and circuits. The problem of testing billion component chips operating at high speeds is well outside the capability of current test technology, even under the simplifying assumptions of single stuck faults in use today; nanodevices are sure to exhibit new failure modes which must be accommodated in test and characterization tools.

Finally, there exists the problem of characterizing the kinds of applications that demand these new architectures. For example, looking ahead for microprocessors that evolve from current architectures, it is likely that much of the complexity will be utilized by the human interface, e.g., speech recognition, computer vision, etc. The challenge will be to creatively exploit the new capabilities and features of nanotechnology, rather than attempt to emulate the behaviors and system architectures of CMOS. It is unlikely that the new device families will be competitive with CMOS for high speed Boolean logic processing, so we must seek out new computational paradigms and system architectures that enable products which cannot be built using CMOS alone. Will the new nanodevices emerging from research laboratories offer compelling advantages relative to CMOS for some of the human interface technologies? If so, they might find application as co-processors for CMOS-based systems.

Potential Solutions

Maybe we are thinking about nanoarchitectures incorrectly. Could it be that we could obtain insight from biological systems that organize themselves hierarchically to meet challenges via goal-oriented actions. In particular, might it be possible to develop a science of organization from computational neuroscience that would allow the ‘design’ of a system to be driven by principles of organization rather than by the placement of each transistor by the designer. In a sense, the idea is to define the goal of the system by a set of behavioral specifications that the system self-configures itself to achieve based on selected organizing principles. This idea is inspired by biological systems and is clearly at an early stage in research.

Even if we are far from design by organization, it might be possible to draw inspiration from the use of time in computation by biological systems. In biology, information is in the timing of signals and in the weights assigned to device interconnections. Could such a strategy be implemented with concurrent increases in performance and decreases in energy consumption relative to conventional digital logic?

There may be an intermediate ground between design-by-organization and digital logic where programmable circuits that are self-testing and self-mapping are developed and where new compute models are defined to exploit spatial parallelism. The realization of

such systems will require an intimate mapping between the architecture of the system and the properties of the devices that are fabricated.

Since it appears that most of the novel electron transport devices that have been proposed must suffer the same ultimate fate of CMOS, i.e., the heat dissipated by their operation will exceed the capacity of any known heat transport system, perhaps we should invest in the development of solid-state quantum computing technologies that do not rely on electron transport. This is a challenging technology to implement and forces a radical re-thinking of architecture, but quantum information processing technologies may offer radical throughput improvements relative to other known technologies in the long term.

C. Workshop Action Items

The workshop on Silicon Nanoelectronics and Beyond (SNB) represents the beginning of an intense and structured dialog between National Nanotechnology Initiative (NNI) academic researchers and program sponsors with the semiconductor industry as it moves aggressively into the far nanometer regime. We believe that the SNB workshop demonstrated that NNI research can address many of the challenges faced by the industry as it seeks to continue to provide exponential gains in performance per unit cost via scaling.

At the workshop, a joint SRC/NNI Consultative Board was formed with the mission of:

- Joint planning and support of collaborative activities in key areas
- Identify and promote joint R&D for exploratory areas of niche markets
- Periodical joint meetings and joint reports
- Exchange information

The members of the Consultative Board are: Mike Roco (NNI, NSF), Clifford Lau (NNI, DOD), Paolo Gargini (SRC, Intel), Ralph Cavin (SRC)

In addition, five Consultative Working Groups were formed. Their mission is to:

- Identify several (2-3) important areas of focus
- Consult and communicate with all participants
- Encourage funding of seed activities
- Support developing longer-term plans

The Consultative Working Groups and their members are:

1. *Signal processing/computational technology beyond charge flow/transfer(Post CMOS)*

Members:

SRC: J. Hutchby (SRC), R. Doering (TI), G. Bourianoff (Intel/SRC), K. Wang (FENA/UCLA), S. Parkin (IBM), Lalita Manchanda (Agereee/SRC)

NNI: J. Murday (DOD), R. Khosla (NSF), S. Basu (NSF), D. Seiler (NIST), R. Burham (Cornell)

2. Unconventional materials, processes and structures for charge transport devices
Members:
SRC: D. Herr (SRC), P. Wong (IBM), A. Bowling (TI), F. Robertson (Intel/SRC), David Kyser (AMD)
NNI: T. Michalske (DOE), TBD (NNI), M. Tirrell (UCSB), D. Antoniadis (MIT), R. Siegel (RPI), Mihal Gross (ONR)

3. Multi-scale/multi-phenomena modeling and simulation
Members:
SRC: W. Joyner (IBM/SRC), H. Hosack (SRC), M. Giles (Intel)
NNI: V. Varadan (NSF), M. Lundstrom (Purdue), TBD Computational Materials (NSF), C. Musgrave (Stanford)

4. New architectures and design concepts: integration of material, device, and system R&D
Members:
SRC: J. Harlow (SRC), J. Parkhurst (Intel), R. Rutenbar (C2S2), D. Hammerstrom (Oregon Health and Science Univ.)
NNI: Cliff Lau (DOD), Valeru Beu (WSU), M. Meyyappan (NASA)

5. Environmental Safety and Health
Members: T. Wooldridge (SRC), M. Roco (NNI, NSF), M. Garner (Intel), B. Kahn (EPA)

The plan is to finalize the membership of these Consultative Working Groups by January 12, 2004 and for each group to have met at least once before the early March, SIA Technology Strategy Committee meeting in Washington DC in 2004. The goal is for each group to provide a preliminary report to the Technology Strategy Committee at the March 2004 meeting.

Appendix I: Priority Research Requirements for Nanomaterials by Design

		Timeframe - Years			
*	**Fundamental Understanding & Synthesis**	**5**	**10**	**15**	**20**
T	Understanding of nanoscale structure-property-processing relationships	■	■	■	■
T	Experimentally validated models and theories of nanoscale physics and chemistry	■	■	■	
T	New paradigms for creating nanoscale building blocks	■	■	■	
T	Design strategies for controlled assembly - nanocomposites, spatially resolved nanostructures	■	■	■	
T	High-throughput screening methods to determine structure-property relationships	■	■		
T	Performance evaluation at the laboratory scale	■	■	■	■
H	Compendium of methods to synthesize and assemble nanomateirals	■	■	■	■
	Manufacturing & Processing	**5**	**10**	**15**	**20**
T	Unit operations and robust scale-up and scale-down methods	■			
T	Manufacturing techniques for hierarchical assembly	■	■	■	■
T	Dispersion and surface modification processes that retain functionality	■			
H	Process monitoring and controls for consistency	■	■	■	■
H	Integrate engineered materials into devices while retaining nanoscale properties	■	■	■	■
M	Impurity removal from raw material precursors	■			
	Characterization Tools	**5**	**10**	**15**	**20**
T	Real-time characterization methods and tools	■	■	■	■
H	Infrastructure for tool development and use	■			
	Modeling & Simulation	**5**	**10**	**15**	**20**
T	Fundamental models to accurately predict nanostructure formation	■	■	■	■
H	Bridging models between scales-from atoms to self assembly to devices	■	■	■	■
H	Infrastructure to support model advancement	■	■		
	Environment, Safety & Health	**5**	**10**	**15**	**20**
T	Assessment of human health and environmental impact hazards	■	■	■	■
T	Determination of exposure potentials for nano-sized materials	■			
T	Handling guidelines for operations involving nanomaterials	■			
	Standards & Informatics	**5**	**10**	**15**	**20**
T	Standard procedures for nanomaterial synthesis	■	■	■	■
T	Reference materials for property measurement	■	■	■	■
T	Standard methods for physical and chemical property evaluation	■	■	■	■
T	Computational standards to improve information processing and transfer	■	■		
T	Standards for material evaluation in applications	■	■		
T	Standardized internationally recognized nomenclature	■			
H	Infrastructure to foster standardization	■			
	Knowledge & Technology Transfer	**5**	**10**	**15**	**20**
T	Technology transfer policies to foster commercialization	■	■		
H	Infrastructure to encourage knowledge sharing	■	■		
	Education & Training	**5**	**10**	**15**	**20**
T	Educated and trained workforce	■	■		
T	Greater public and industry awareness	■	■		

Infrastructure & Enabling Resources

R&D areas above include these research requirements

* Priority Ranking: Importance to developing Nanomaterials by Design capability:

T = Top; H = High; M = Medium