Quantum Information Science and Technology Grand Challenge

LDRD
LABORATORY DIRECTED RESEARCH & DEVELOPMENT

Sandia National Laboratories
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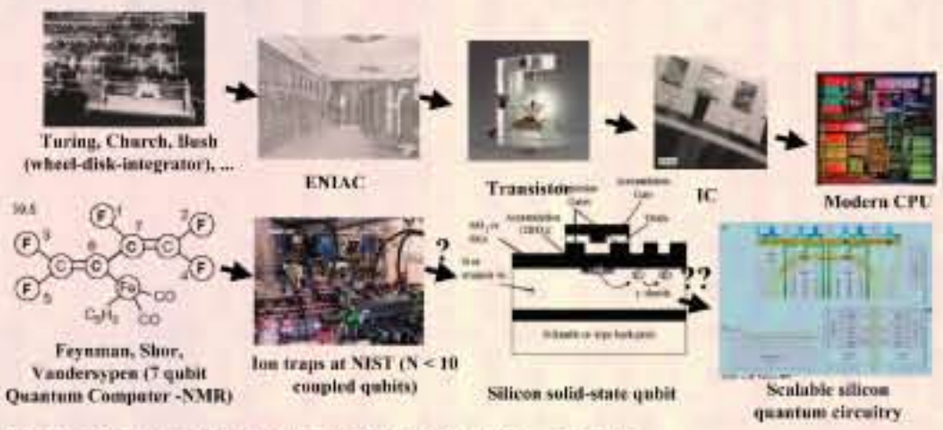
Significance

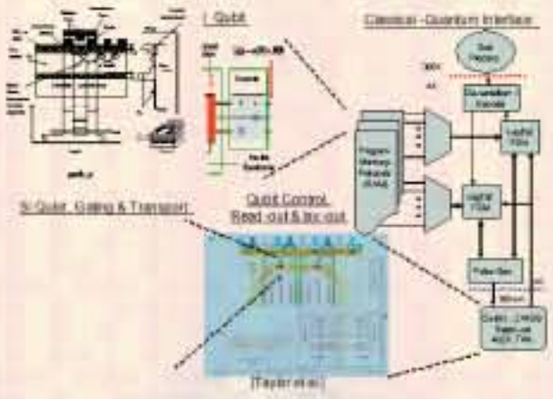
History, Motivation & Vision



- History of computation has evolved dramatically in ~75 years
- Quantum computing (QC) offers disruptive computing potential
- Many two-state quantum systems being examined for QC
- Perceived advantages of proposed silicon quantum circuitry: *infrastructure, integration, power, spin decoherence*
  - Modern CPU enabled by solid-state (i.e., vacuum tube not practical)

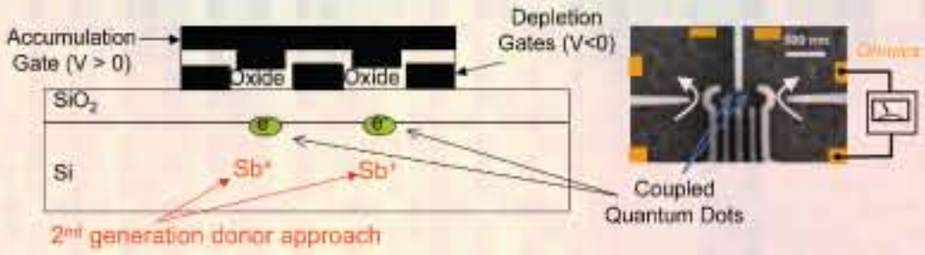
Problem

- *Challenge I:* demonstrate silicon quantum bits (qubit)
  - The problem: Si qubit existence proof
  - GaAs has demonstrated spin qubit
- *Challenge II:* design qubit for quantum circuit
  - Many ideas for single qubits are unsuitable for multi-qubit quantum circuits
- *Big lab problem:* requires basic physics, Si foundry, novel electronics & high performance computing



Approach I:

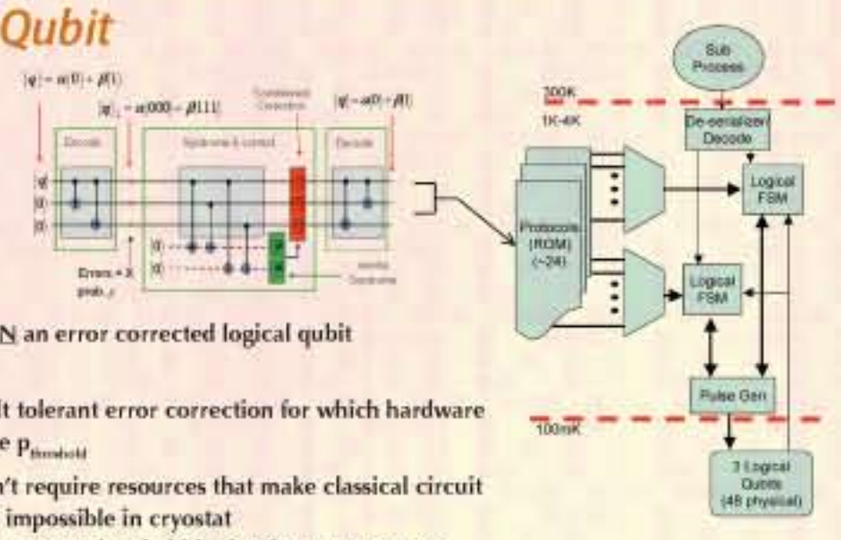
Si Qubit



- GaAs lateral double quantum dots (DQD) have demonstrated qubit gating
- Pauli-blockade recently demonstrated in SiGe/sSi and UTB-SOI cases
- Our approach: pursue surface Si MOS-DQD
  - Compatible with ^{28}Si epitaxy => long T_2
  - Charge stability demonstrated with MOS system [e.g., Zimmerman et al.]
  - Gates very close to 2DEG => smaller dots than modulation doped case
  - Possible drop-in with SNL CMOS process flow (e.g., fast, low noise sense)
  - Pathways to adopt SiGe/sSi or donors through 2nd-generation structures

Approach II:

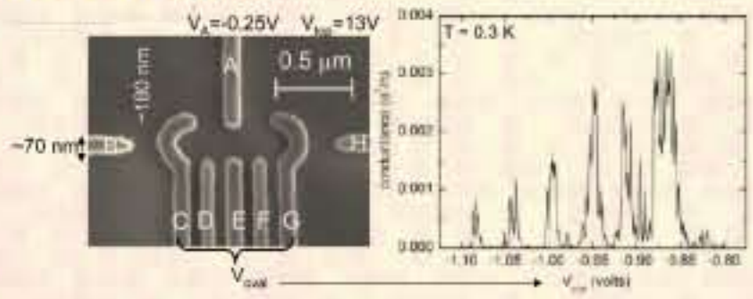
Logical Qubit



- Goal: DESIGN an error corrected logical qubit
- Challenge:
  - Design fault tolerant error correction for which hardware can achieve $p_{threshold}$
  - AND doesn't require resources that make classical circuit realization impossible in cryostat
    - Costs: power, bandwidth, density, transport; etc.

Result I:

Si Coulomb Blockade

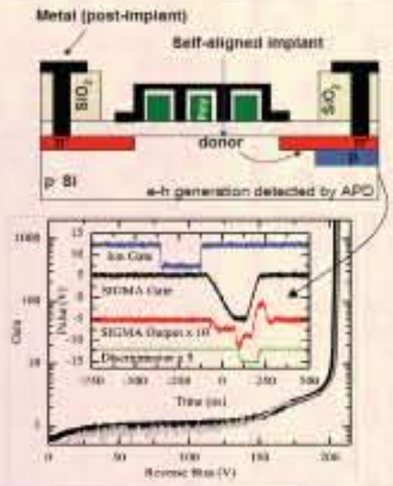


- Initial silicon nanostructures fabricated and measured
- Single electron transistor (SET) action demonstrated
  - Si foundry combination with micro-fab processes (e.g., e-beam lithography) established
  - Early demonstration of SET provide potential electrometry test platform and has helped identify needed materials & processing improvements

Result II:

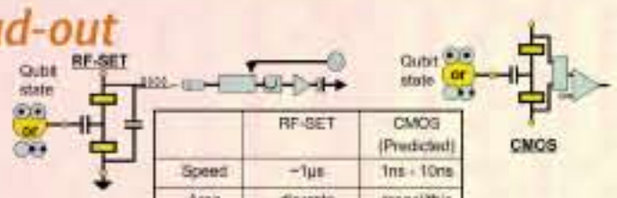
Single Ion Implant Demonstrated

- First ever application of Geiger mode avalanche detection for single ion implantation demonstrated
- Promises superior sensitivity to previous approaches
  - Higher precision placement of single donor (< 15 nm straggle)



Result III:

Circuit Assisted Read-out



	RF-SET	CMOS (Predicted)
Speed	~1μs	1ns - 10ns
Area	discrete	monolithic
Power	mW *SET and tank < mW	nW
Logical	no	yes

- Current qubit read-out uses radio frequency SET (RF-SET)
- SNL "digital read-out" design critically faster & lower power per read
- Models for SNL CMOS7 foundry FETs for 4 K operation established

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