WORLD CUSTOMS ORGANIZATION
ORGANISATION MONDIALE DES DOUANES
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HARMONIZED SYSTEM
COMMITTEE
-
27th Session
-

NC0419E1
(+ Annexes I and II)
O. Eng.

Brussels, 4 May 2001.

STUDY TO DISTINGUISH THE PROCESSORS AND COPROCESSORS OF HEADING 84.71 FROM THOSE OF HEADING 85.42

(Item IX.8 on Agenda)

Reference documents :

NC0340E2, Annex G/20, paragraph 5 (HSC/26 – Report) NC0407E1(HSC/27)

I. BACKGROUND

1. After the preparation of Doc. NC0407E1, the Secretariat received, on 12 April 2001, comments from the International Chamber of Commerce (ICC), regarding the distinction between processors and coprocessors of heading 84.71 vs. heading 85.42. The text is reproduced in Annex I to this document.

II. SECRETARIAT COMMENTS

2. After the receipt of the submission, the Secretariat contacted the ICC with a view to receiving more information concerning some of the issues referred to in the above-mentioned submission. The additional information received is reproduced in Annex II to this document.

3. The Secretariat has not yet been able to study the information provided by ICC thoroughly. Nonetheless, with a view to facilitating discussions (whether or not preliminary) during the present session of the Committee, the Secretariat has given some initial comments below.

4. The Secretariat would like to note first that the ICC submission not only addresses the question of how to distinguish between (co)processors of heading 84.71 (or 84.73) and those of heading 85.42, but that it also addresses the issue of a possible transfer of the (co)processors from heading 84.71 to heading 85.42. The Secretariat understands, however, that the submission at issue does not provide the actual proposal to that effect, and suggests waiting for formal proposals to that effect, which could be sent to the Review Sub-Committee in due time.

File No. 2850

5. Second, the initial question was raised when, in the context of the possible deletion of references to certain obsolete equipment in the Explanatory Note to heading 84.71 (see Item VIII.7 on Agenda), the Committee, at its 26th Session, discussed the possible insertion of a reference to "coprocessors, accelerator, print processor, display processor, graphic cards, math coprocessor" in item (3) of the second paragraph on page 1406. However, one delegate questioned the appropriateness of these references, since they could lead to confusion with the integrated circuits of heading 85.42.

6. The ICC submission addresses the issue of identification by indicating that the processor package (i.e., cartridge package or socket package) is the main factor in making the distinction. It also indicates a possible distinction between the (co)processors of heading 84.71 and those of heading 84.73 (the Committee classified the "Pentium® II" (being described as a microprocessor) in subheading 8473.30), by referring to the fact that the (co)processors of heading 84.71 are externally connected by cable to the central processing unit (CPU).

7. This approach could be reproduced in schematic format as follows :

Heading	**84.71**	**84.73**	**85.42**
Type of package :	externally connected by cable to the CPU	cartridge package	socket package

8. It seems, however, that this type of distinction might oversimplify the actual situation, since none of the legal texts involved (Notes 5 to Chapters 84 and 85, and headings 84.71, 84.73 and 85.42) use this criterion. Moreover, classification in any of these headings is based on functionality and physical appearance. For example, two or more integrated circuits on a layer (e.g., multichip package – see Annex II) are classified outside heading 85.42, whereas they may be presented in a socket package.

9. Having said that, the Secretariat considers that it might be premature to decide on the distinctions on the basis of the information now available. It therefore, suggests further discussions at the next session, based on an in-depth study of the material received through ICC, and of any other information submitted by administrations or other interested parties. As a consequence, the Committee may wish not to insert, for the time being, a reference to "coprocessors, accelerator, print processor, display processor, graphic cards, math coprocessor" in item (3) of the second paragraph on page 1406 (see Item VIII.7 on Agenda).

III. CONCLUSION

10. The Committee is invited to take into account the information provided by ICC in Annexes I and II to this document, and the observations of the Secretariat in paragraphs 2 to 9 above, when considering this Agenda item.

* * *

Note presented by ICC

I. Current

1. The processor package is the main factor that one can distinguish between headings 84.71, 84.73 and 85.42.

2. All processors with the cartridge package are classified in heading 84.73. Processors such as Pentium II and a majority of the Xeon processors. In addition to the CPU being contained on the printed circuit board, there are active and passive components on the same package. The cartridge package has a contact (slot) that inserts into a corresponding slot on the motherboard.

3. There are, however, other coprocessors, which would fall under Note 5 (B) to Chapter 84/84.71 (not 84.73) if they are externally connected by cable to the CPU unit.

4. All processors with the socket package are classified in heading 85.42. Processors such as the latest Pentium III and Pentium 4. The socket package has pins that insert into the corresponding socket on a motherboard.

II. Trade input

5. The trade believes that all processors should be classified in heading 85.42 regardless of their package type.

6. The packaging technology is changing each year and this is true for both, package material and package form factors. The trade believes the processor core should have a priority over the package.

7. One element that does not change over the time is the microprocessor core itself. Here the trade is talking about the functionality and silicon substrate.

8. Currently the trade feels that they are providing unreliable statistics when they classify socket type microprocessor in heading 85.42 and cartridge type in heading 84.71. The function of these processors is identical, both of them will reside on the computer motherboard and provide the same functions.

III. Additional comments

9. Trade associations in the United States, Europe and Japan are currently working on the rewrite of Note 5 (B) to Chapter 85. They are considering whether to rewrite the note to allow processors currently classified in heading 84.71 to be covered by heading 85.42. A significant challenge is how to distinguish them from other populated PCBs.

10. Another challenge they see is the "stacked die" packages, which may include two types of devices, such as flash memory and SRAM.

11. The individuals responding also included a Word file (see Annex II to this document) with some screen shots from a Web page. Hybrid IC's have evolved into multi-chip packages. Laminated printed circuit boards are mentioned in the MCM and MCP definitions. Perhaps this is some language to use to distinguish between the two.

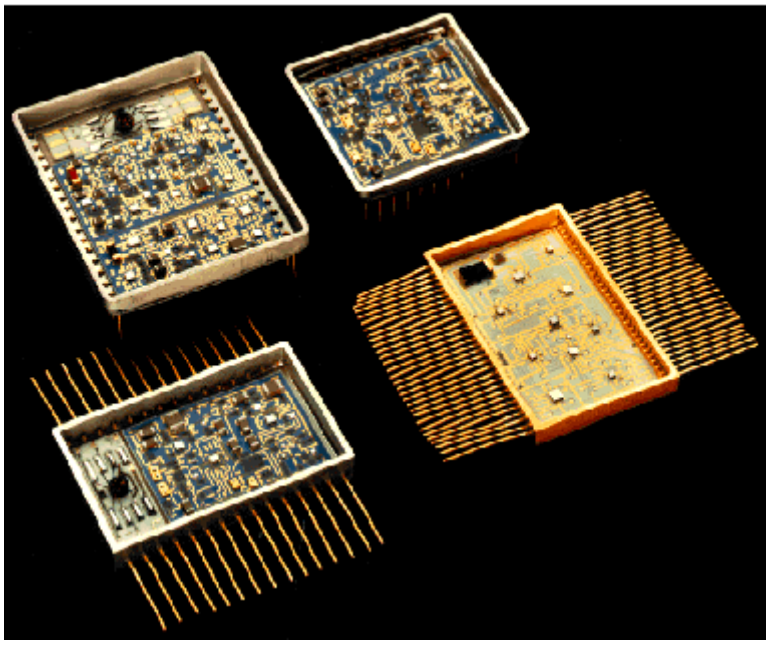
* * *

Additional information received through ICC

I. Package

(i) Hybrid microcircuit

An electronic circuit composed of different types of integrated circuits and discrete components, mounted on a ceramic base. Used in military and communications applications, it is especially suited for building custom analog circuits including A/D and D/A converters, amplifiers and modulators. The hybrid microcircuit evolved into the multichip module (MCM) and, later, the multichip package (MCP).



Hybrid Microcircuits
The picture shows a variety of hybrid circuits. The tiny, square white spots are the actual chips. *(Image courtesy of Circuit Technology, Inc.)*

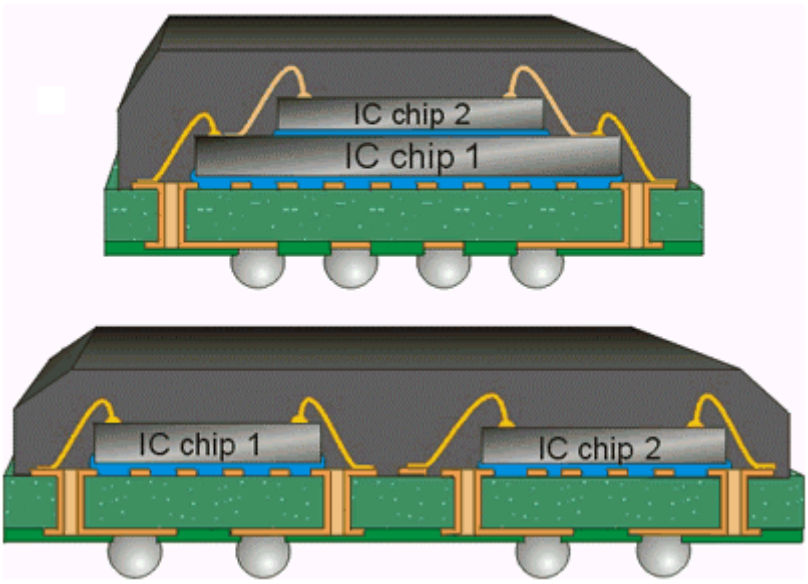
(ii) MCM

(**M**ulti**C**hip **M**odule or **M**icro**C**hip **M**odule) A chip package that contains two or more raw chips closely connected with high-density lines. This method saves space and speeds processing due to short leads between chips. A ceramic base has been widely used with chips wire bonded together (MCM-C) or with thin film interconnects deposited on the ceramic substrate (MCM-D). MCMs have been mounted onto silicon substrates (MCM-S) and resin-based, laminated printed circuit boards (MCM-L), the latter, less-costly version evolving into the multichip package (MCP).

MCMs were originally called "microcircuits" or "hybrid microcircuits," since this technique was suited for mixing analog and digital components together.

(iii) MCP

(**M**ulti**C**hip **P**ackage) A chip package that contains two or more chips. It is essentially a multichip module (MCM) that uses a laminated, printed-circuit-board-like substrate (MCM-L) rather than ceramic (MCM-C). MCPs are also tested after packaging, whereas the bare die of ceramic-based MCMs were tested before packaging so as not to waste the more costly ceramic substrate if the chips were no good.



Multichip Packages
These are examples of multichip packages with stacked chips (top) and side-by-side chips (bottom). The chips are wire bonded to the resin-based substrate which is attached to the printed circuit board using a ball grid array (BGA). *(Illustration courtesy of Joseph Fjelstad.)*

II. IBM PCI Cryptographic Coprocessor (from : IBM 4758 PCI Cryptographic Coprocessor.htm)

The IBM PCI Cryptographic Coprocessor adds a high-security environment to your OS/2, Windows NT, Windows 2000, AIX, OS/400, z/OS, and OS/390 server systems for DES, RSA, and DSA cryptographic functions and sensitive custom applications. The PCI board incorporates specialized electronics to off-load your servers from time-consuming cryptographic functions while providing a tamper-responding, secure computing environment for the storage of keys and performing sensitive processing. Certification under FIPS PUB 140-1 at levels 3 and 4 assures a high-integrity processing environment.

PCI Cryptographic Coprocessor now available for all IBM servers...

The leadership product for high-security cryptography and secure computing is now available for all IBM server platforms and many personal computers. The tamper-responding design has been certified under the USA FIPS 140-1 standard at levels 3 and 4, and has received

German ZKA approval for critical financial transaction system processing. IBM supplies two cryptographic-system implementations, and toolkits for custom application development. The PKCS #11, version 2.01 implementation creates a high-security solution for application programs developed for this industry-standard API. The IBM Common Cryptographic Architecture implementation provides many functions of special interest in the finance industry and a base on which custom processing and cryptographic functions can be added. For more information, visit our product summary page.

The PCI Cryptographic Coprocessor encapsulates a 486-class processing subsystem within a tamper-sensing and tamper-responding environment where you can run security-sensitive processes. A multi-tasking control program gives you access to high performance electronics for DES and public key algorithms. A cryptographic quality random number generation facility and large, secure, persistent data storage complete the physical system. Except for a very small bootstrap loader, all software is loaded into the Coprocessor from your server environment. Only digitally signed software that is validated by the Coprocessor is acceptable. The sophisticated code loading controls enable you to employ signed software from IBM, other vendors, or code that you create using toolkits available from IBM. For additional information, see the product summary page.

More information...

The product summary pages will introduce you to the Coprocessor and its software options. More detailed information in the product publications such as the General Information Manual can be downloaded in PDF format from the library. Product ordering pages explain how to obtain the Coprocessor and its software downloads. Refer to the support pages to find education, ask questions, check for software updates, or locate other support services.

The PCI Cryptographic Coprocesor is one of the IBM Security products that provide solutions to many of your security needs.
We want to hear from you! If you have comments or questions about the product or this website, please fill out our form (or send an e-mail to crypto@us.ibm.com).

III. Other information

The packaging technology is described in the abstract portion of the following URL : http://developer.intel.com/technology/itj/q32000/pdf/flipchip.pdf.

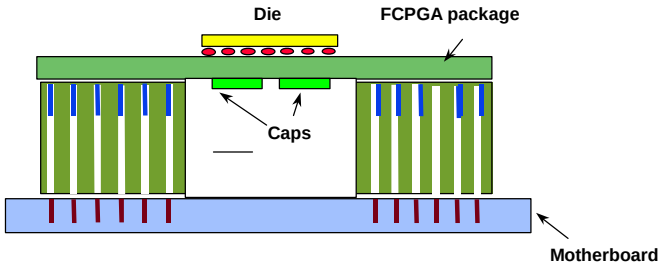
Some webpages for coprocessors.

Here's a German citation for a similar 8473 product : http://www.gris.uni-tuebingen.de/gris/jb95/node20.html and another online definition : http://www.pcwebopedia.com/TERM/c/coprocessor.html.

"As the importance of multimedia and then 3D graphics has increased, the role of the graphics card has become ever more important and it has evolved into a highly efficient processing engine which can really be viewed as a highly specialized co-processor. By the late 1990s the rate of development in the graphics chip arena had reached levels unsurpassed in any other area of PC technology, with the major manufacturers such as 3dfx, ATI, Matrox, nVidia and S3 working to a barely believable six-month product life cycle ! One

of the consequences of this has been the consolidation of major chip vendors and graphics card manufacturers." (http://www.pctechguide.com/05graphics.htm).

Flip Chip PGA Package



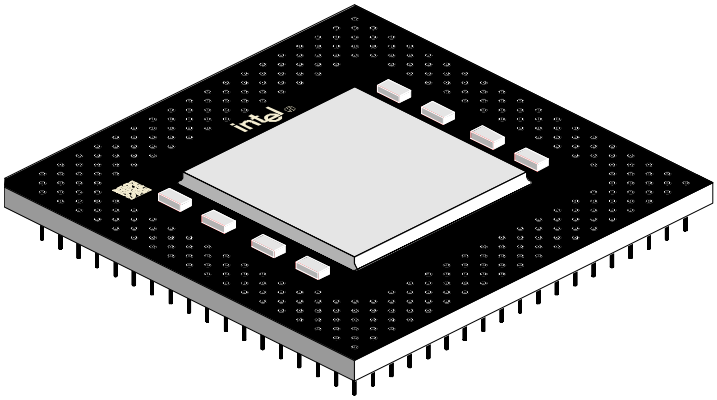
intel 1

(Flip Chip Pin Grid Array (FCPGA) package)

Types of Packages (Interconnection Method)

- Wirebond
  - Tiny gold wire (0.0013” diameter) connects die pad to package bond pad
- Flip chip
  - Die is flipped, and die pads connect directly to package bond pads
  - C4 is flip chip
  - Wave of the future

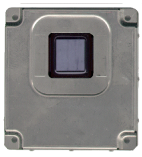
The PPGA Package



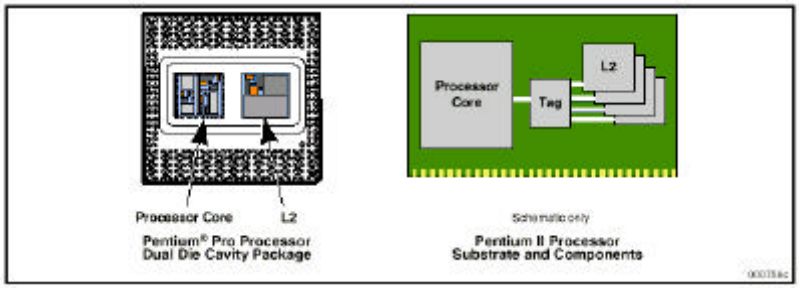
Contemporary Semiconductor Assembly

Cartridges

Slot 1, Slot 2 and Mobile



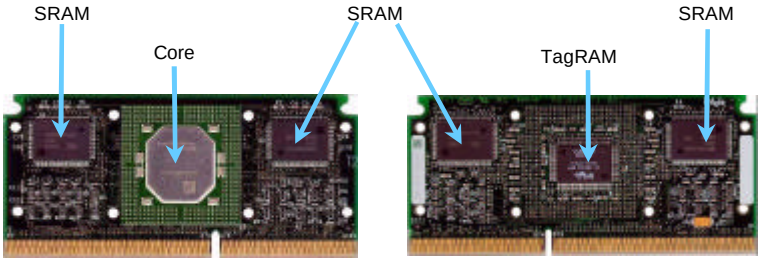
Dual Independent Bus



The Processor Core has a direct, high speed bus connecting it to the Level 2 cache memory, as first developed for the Pentium Pro processor.

Substrates

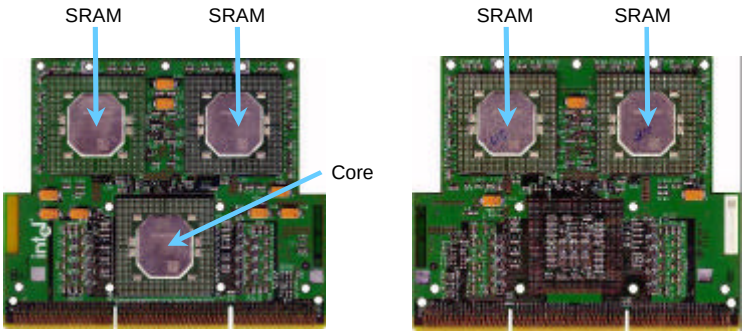
Slot 1 (PC1.S1.A)



Primary Side **Secondary Side**

Substrates

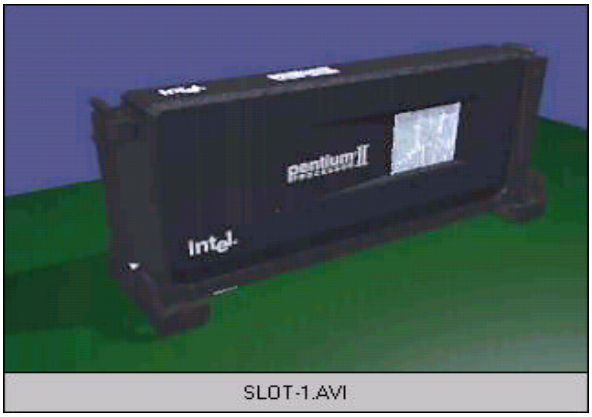
Slot 2



Primary Side

Secondary Side

Slot 1 Cartridge



Slot 2 Cartridge