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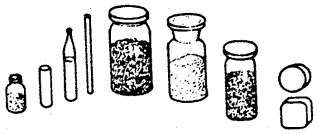

Standard Reference Materials:

CALIBRATION OF NBS SECONDARY STANDARD MAGNETIC TAPE (COMPUTER AMPLITUDE REFERENCE) USING THE REFERENCE TAPE AMPLITUDE MEASUREMENT "PROCESS A"

U.S. Department of Commerce

National Bureau of Standards

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Standard Reference Materials:

Calibration of NBS Secondary Standard Magnetic Tape (Computer Amplitude Reference) Using the Reference Tape Amplitude Measurement "Process A"

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ABSTRACT

This publication describes the design and operation of the NBS signal amplitude measuring system (Process A) that is used for calibrating unrecorded Secondary Standard Magnetic Tapes (Computer Amplitude Reference). The signal level calibration is made with respect to a reference signal level derived from the NBS Master Standard Magnetic Tape (Computer Amplitude Reference) that is kept in repository at NBS. The techniques for measuring and recording the data that accompany each Secondary Standard Magnetic Tape in the form of strip chart recordings and saturation curves are described.

Key words: Magnetic tape, computer amplitude reference, unrecorded reference, Secondary Standard, Master Standard, signal level calibration, average peak signal level, saturation curves, standard reference materials.

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I. INTRODUCTION

The characteristics of present day magnetic computer tapes are the result of long term research and development by the magnetic tape industry. Technological developments in related fields and transducer-tape interplay have stimulated continuing improvement of the tape media and their performance. This has often led to differences in tape characteristics and marginal operation when tapes are interchanged between systems. The only tapes previously available for quality assurance purposes have been industry supplied standards.

At the request of industrial users of computer tape, Government procurement agencies, producers of magnetic computer tapes, and producers of tape handling equipment the National Bureau of Standards has developed a tape measurement system and is supplying unrecorded Secondary Standard Magnetic Tapes (Computer Amplitude Reference) through the NBS Office of Standard Reference Materials.

This new material, which is designated as the NBS Standard Reference Material No. 3200, consists of a 600-foot length of secondary reference tape accompanied by applicable test and calibration data, and a description of the equipment and procedures employed for measurement of the tape. The secondary tapes themselves are 1/2 inch wide unrecorded magnetic computer tapes wound on 8-1/2 inch diameter precision reels.

Each tape is calibrated in terms of a 100% signal level that is derived from the NBS Master Standard Magnetic Tape (Computer Amplitude Reference) which is kept in repository at NBS. This signal level calibration is done at recording densities of 200, 556, 800 and 3200 flux reversals per inch and calibration information in the form of signal output charts recorded near each edge track and center track accompanies each secondary tape. A set of saturation curves relating the reproduce head output voltage (on the first read-after-write pass) to the write current at each bit density of both the NBS

master and each secondary tape is also included. The write current ranges from zero to at least 150% of the saturation current level.

Presently, the main criteria for the selection of unrecorded amplitude reference tapes for calibration as secondaries are signal amplitude uniformity and proximity of read-after-write output voltage to that of the master. The instantaneous track-to-track variation in the average signal amplitude is limited to a maximum of 3% among the outputs from the NBS test tracks 2, 5 and 8. The location of these tracks is defined in USASI Document X3.22-1967. The maximum variation in the longitudinal average signal output voltage along each test track is limited to 4% over the 600 foot length of tape. The absolute value of the average signal amplitude from each test track is within 10% of the NBS Master Standard Magnetic Tape (Computer Amplitude Reference). These criteria are applied for peak current recording on degaussed (fully ac erased) tape when measured on the NBS system in the manner described in this publication.

2. Theory of Operation of the NBS Measurement System

A. System Components

Figure 1 shows the organization of the system used for measuring and calibrating the unrecorded NBS Secondary Standard Magnetic Tapes (Computer Amplitude Reference). The system consists of a write channel (NRZI mode), a signal amplitude read channel and a signal peak averaging channel. Various readout devices and precision voltage supplies are also included in the system.

The following descriptive material lists the components that appear in each of the three major channels. One of the figures that is given with each channel contains the block diagram of the channel functions and the other figures consist of the circuit realizations of the block functions. Note that within most of the individual blocks a figure number is

inscribed which identifies the circuit diagram that corresponds to that block.

1. Write Channel Components (Figures 2, 2a, and 2b):
   a. A variable frequency square wave generator G-1 whose frequency ranges from at least 22.5 kHz to 360 kHz, a pulse counter and a bistable multivibrator circuit BC-1.
   b. A slotted read-write head (IBM Assembly No. 5417960 Part No. 2510730), a write head current driver circuit WD-1 and a write current amplitude control circuit CC-1.
2. Signal Amplitude Read Channel Components: (Figures 3, 3a to 3e)
   a. A slotted read-write head (IBM Assembly No. 5417960 - Part No. 2510730), a line driver LD-1, a termination network TE-1 and a preamplifier PR-1.
   b. A delay network DLY-1, inverters I-1 and I-2, a post-amplifier PO-1 and peak detector PD-1.
   c. A strobe pulse generator SG-1.
   d. A sample-and-hold circuit SH-1.
   e. An electrometer E-1 and a summing amplifier SA-1.
3. Signal Peak Averaging Channel Components: (Figures 4, 4a to 4d)
   a. A sample time pulse generator G-2 with power line frequency control.
   b. An inverter I-3, a linear integrator LI-1, and electrometer E-2.
   c. A sample-and-hold circuit SH-2, an FET-electrometer E- , an inverter I-4 and a summing amplifier SA-2.
4. The tape transport is a modified IBM 729-VI and the readout devices consist of a 6-track pen recorder, an x-y recorder and an oscilloscope. Precision voltage sources are used for calibration purposes.

B. Description of the Channel Operation.

1. Write Channel Operation: (Figures 2, 2a and 2b)

a. The signal amplitude measurements are performed at all bit densities on candidate tapes that have been initially degaussed and then recorded with all "ones" in the NRZI mode.

b. The recording current signal frequency is controlled by pulse generator G-1 whose output pulses are used to drive a binary flip-flop BC-1 that has been designed into the IBM 729-VI transport.

c. BC-1 produces a symmetrical output voltage square wave at one half of the input frequency which is used to gate the write head driver circuit WD-1. WD-1 is constructed with matched components so that it produces equal values of write head current in both directions.

d. The write current controlling circuit CC-1 is used to vary the absolute current value in WD-1 over a range of from 0 to 45 mA. The write current value is determined from the voltage drop across the 10Ω resistance in the write head center tap (Figure 2b).

2. Signal Amplitude Read Channel Operation: (Figures 3, 3a to 3e. The timing for the signals described in steps a through d is shown in Figure 5.)

a. The signal which has been reproduced by a read-after-write operation from a candidate tape is passed through a unity gain, line driving amplifier LD-1 which is physically located at the read head. The line is terminated by network TE-1 at the input of PR-1.

b. This signal is then passed through preamplifier PR-1 that has an adjustable gain of approximately 150 to 300. PR-1 is adjusted to produce a 4.0 volt peak-to-peak output signal when the NBS Master Standard Magnetic Tape (Computer Amplitude Reference) is used for the electronics calibration procedure.

c. This 4.0 volt peak-to-peak signal is then processed during its transmission to SH-1 and PO-1 as follows:

(1) The signal is delayed for a time T_D = 0.75 μs and inverted in I-2. It is then compared to its inverted but non-delayed signal counterpart from I-1 as they enter the peak detection PD-1 system. This comparison process locates the signal peak and at this instant a strobe pulse is generated in SG-1 and injected into SH-1.

(2) The 4.0 volt peak-to-peak signal is simultaneously delayed by an amount equal to that in (1) and is passed through the post-amplifier-clipper circuit PO-1. PO-1 has an adjustable gain capability and its output is half wave rectified and adjusted to consist of negative polarity pulses having 3.0 volt peak amplitudes. This is the nominal signal level that has been chosen for the system.

d. SH-1 will use the above strobe pulse in conjunction with the 3.0 volt negative signal to develop and hold a dc level equal to the peak value of each successive incoming negative signal peak from PO-1. The output of SH-1 is sensed with a very high input impedance, unity gain circuit E-1 in order to prevent information loss due to unwanted discharge of the "hold" capacitor C_1.

e. The E-1 output voltage is then fed into a summing amplifier SA-1 which has a dc offset capability that is controlled with a calibrated potentiometer. SA-1 can be adjusted by the offset circuit so that its output will contain a specific percentage of the total signal range. For example, a range consisting of from 90 to 110% of the total signal amplitude is charted on a recorder by offsetting

the lower 90% of the nominal signal value and then selecting a recorder range setting that is capable of encompassing only the next 20% of the total signal level over its chart limits. It was found useful to convert the output signal amplitude to a value that yields a direct relationship between the major recording chart divisions and the percentage value of the signal under test.

Note: This same offset capability of SA-1 can be used to compare relative signal peak values and to measure the distribution of incoming signal peaks on a high sensitivity range of an oscilloscope. This measurement, however, does not require prior peak detection and sample-and-holding of the signal, *i.e.*, the signal is passed directly from PR-1 to SA-1. When the oscilloscope sweep rate is set to display only one half or less (positive or negative) of one signal cycle per trace then a broad arched band of light appears on the screen. The broadness of the band is a function of the scope sensitivity and of the distribution of the signal peak amplitudes read from the tape. The intensity of the light band varies across its height with the brightest level appearing at the amplitude related to the most prevalent signal peak value. Signal drop-outs have no effect on this measurement and it is possible to differentiate between signal peak amplitudes that differed by less than 5 mV out of 3 volts.

3. Signal Peak Averaging Channel Operations: (Figures 4, 4a to 4d)

The output of SH-1 is transmitted to the average peak voltage measuring system which continuously processes this signal and returns its average peak value to one of the recorder tracks. The operation of the averaging system is as

follows:

a. It has been determined theoretically that if an equi-spaced pulse train is sampled-and-held and is then injected into a linear integrator circuit whose RC product is equal to a sampling time T, then the final output voltage of the linear integrator at each time T is equal to the average peak value of the train over that sampling interval.

b. The sample-and-hold signal output from SH-1 is transmitted *via* E-1 and I-3 to the input of the linear integrator LI-1 whose RC product has been set equal to RC = T = 0.270 seconds. The average peak value of a sample consisting of approximately 50,000 pulses under the recording conditions of 3200 frpi and 112.5 ips tape speed is thus derived by the linear integrator each 0.270 seconds.

c. These average peak values are strobed out each T seconds and stored in the sample-and-hold circuit SH-2 while LI-1 is reset preparatory to the next sampling interval.

d. The output of SH-2 is then transmitted to a recorder track *via* I-4, SA-2 and an extremely high input impedance FET E-3 circuit which has its own gain and level setting capability.

e. A pulse generator that uses the 60 Hz power frequency as its basic clock source controls the sampling time intervals of the averaging system (Figure 4a).

3. Calibration and Set-up of the Reference Tape Signal Amplitude Measurement System

The procedures will be discussed in three sections:

A. e_o *versus* I_w saturation curves.

B. Signal amplitude read channel calibration and setup procedure.

C. Signal peak averaging channel calibration and setup procedure.

It is to be noted in all three sections that the output voltage from the tape is always obtained during a first read-after-write pass of a previously degaussed tape.

A. e_o *versus* I_W saturation curves.

1. An x-y recorder is used for producing curves showing the reference tape read head signal e_o *versus* the write head current I_W (Figure 6). They are produced from the tape by plotting a continuously varying write current level *versus* the read head output voltages that these levels produce during a first read-after-write operation. Individual plots are made at each bit density. These curves are used to determine the saturation write current level at each recording bit density in order to set up the system for the amplitude measurements.

2. In order to produce the e_o *versus* I_W curves on the x-y recorder, the full read signal amplitude (zero SA-1 offset voltage applied) is made available at the output of summing amplifier stage SA-1. The gain of this stage is set so that it converts the nominal 3.0 volt, 100% signal level of the system to 5.0 volts prior to its insertion into the y axis of the recorder. The y axis gain is then adjusted so that the y axis ordinate values are given in terms of the actual peak-to-peak read head output in millivolts as measured by an oscilloscope at the output of the line driver LD-1.

3. The drive to the x (current) axis is derived from the voltage drop across a 10 Ω resistance in the center leg of the write head. These voltage drops are converted by an x axis gain adjustment into abscissa values which represent the write head current in milliamperes. The range of applied write current is 0-45.0 mA and the resulting head output voltage range has been found to range between approximately 12.0 mV at 3200 frpi to 25.0 mV at 556 frpi.

4. If the saturation write current level is considered to be the first level at which the absolute maximum value of output read head voltage is encountered, then it has been found at 3200 frpi that the average saturation write current level is

15.0 mA and that at 556 frpi the saturation current level is approximately 35.0 mA. These average current values were derived from the industry tapes that were sampled in this first program phase. The saturation write current levels are used for producing the three track strip charts that will now be described.

B. Signal amplitude read channel calibration and set-up procedure (Figure 3).

The first four steps are accomplished while using a "working" reference tape in order to make the initial ccarse adjustments. This avoids any unnecessary wear of the Secondary Standard Magnetic Tapes:

1. Set the frequency generator G-1 to the required bit rate.
2. Set the write head current to the saturation level which has been obtained by the method described in Section 3,A.
3. Adjust the gain of the preamplifier PR-1 to obtain an initial output signal level of 4.0 volts peak-to-peak.
4. Adjust the gain of the post-amplifier-clipper circuit PO-1 for a 3.0 volt negative peak signal output.
5. Replace the "working" reference with the Secondary Standard Magnetic Tape and readjust the write current saturation level as in (2). The remainder of the calibration procedure is accomplished using a sensitive chart recorder. (For example, one with at least a 200 mV/cm resolution.)
6. An accurate calibration voltage source is used to inject 3.0 volts into electrometer E-1. This dc signal then passes into the summing amplifier SA-1. The gain of SA-1 is set to produce 5.0 volts at its output when the nominal 3.0 volts input is applied under zero offset conditions. At NBS the useful strip chart width is 5 cm and typically a total tape signal range of 20% (*i.e.* 90 to 110%) is recorded using the 200 mV/cm scale. Under these conditions an input of from 0.0 to 1.0 volt to the recorder will be linearly distributed across the chart with 0.0 volts (90%) at the lower edge, 0.50 volts (100%) at the center and 1.0 volt (110%) at the upper edge. In order to relate the 5.0 volt input signal to these values the

dc input to SA-1 is adjusted so as to offset this signal downward by 90% (4.5 volts). This shifts the 4.5 volt level of the signal to 0.0 volts and causes the higher voltages to shift to their respective values, *i.e.* 5.0 volts shifts to 0.50 volts (100% level) and 5.5 volts shifts to 1.0 volt (110% level).

7. The 3.0 volt calibration signal is now removed and the Secondary Standard Magnetic Tape is run. The preamplifiers PR-1 and/or the postamplifier PO-1 are now fine adjusted during a first read-after-write pass so that the average peak voltage output from two outer tracks and the center track[1] of the tape will fall at the 100% chart level if the tape is a 100% level tape. If the tape is not a 100% level tape but has been precalibrated with the NBS Master Standard Magnetic Tape (Computer Amplitude Reference), then the adjustments are made to that precalibrated percentage level.

This completes the calibration of the peak amplitude measurement portion of the system.

C. Signal peak averaging channel calibration and setup procedure.

1. A 3.0 volt dc calibration signal from E-1 is fed into the signal input terminal of the linear integrator LI-1. This is interpreted by LI-1 as being the output of a sample-and-hold circuit whose input consists of a train of equal amplitude pulses each having the peak value of 3.0 volts. Since the average peak value of the dc signal is also equal to 3.0 volts, LI-1 is adjusted (with the variable R; C is fixed in this system) so that its instantaneous voltage level at each strobe time T (= .270 s) is also equal to exactly 3.0 volts. This is done by using a 2 channel oscilloscope and adjusting the sawtooth output of LI-1 (which is the result of the linear integration of the dc input signal) so that it just equals the input level at each time T. When the adjustment is correctly made then RC = T and the sawtooth voltage peak value will continue to equal the input dc level at each time T as the input voltage is varied over a

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1 See Section 4,D.

range of from approximately 0.5 V to 4.5 V.

2. When the calibration of the linear integrator is completed, a 1.0 volt dc signal is injected into LI-1 and the output voltage of the FET-electrometer E-3 is measured. A coarse adjustment of the voltage level control in E-3 is made to bring its output voltage to approximately 1.0 volt. The dc calibration voltage from E-1 is now increased to 4.0 volts and the output of E-3 is measured. The "gain" control of E-3 is adjusted to bring its output to within 10 mV of the input voltage. All of the preceding steps in (2) are repeated until E-3 displays unity gain over a range of approximately 1.0 V to 4.0 V. After this has been completed, the E-3 voltage level control may be finely adjusted so as to set both ends of the voltage range to their exact absolute value.

3. The output from E-3 is passed through inverter I-4 and SA-2. SA-2 has an adjustment that offsets the average peak signal so that its 100% level coincides with the 100% chart position in the same manner as described for the peak signal in 3,B,6.

The calibration of the system is now complete.

4. Note to Reference Tape Users

A. Important: The NBS Secondary Standard Magnetic Tapes should be used sparingly so as to minimize physical changes to the tape and to assure continued performances as near to the supplied calibrations as possible.

B. A family of e_o *versus* I_w saturation curves (with bit density as the parameter, see Figure 6) will accompany each NBS Secondary Standard Magnetic Tape (Computer Amplitude Reference) from which it is derived. In addition, the family of e_o *versus* I_w saturation curves that was obtained from the NBS Master Standard Magnetic Tape (Computer Amplitude Reference) will also be included in the package. The user will therefore be able to relate the percentage variations in output at different write current levels between the NBS Master Standard

and the NBS Secondary Standard Reference Tapes.

C. Strip charts derived from 3 head tracks at each bit density will also accompany the NBS Secondary Standard Magnetic Tape from which they were derived. Data from each read head will be recorded on 2 adjacent pen tracks with the signal peak amplitude appearing on the lower track and the average peak amplitude of the signal appearing on the upper pen track. Figure 7 shows tracks B and C as they appear on a typical strip chart recording.

The saturation write current level that was used when making these chart recordings is indicated on each e_o *versus* I_w curve by a dark mark at the peak value. The set of curves shown in Figure 6 are in fact the saturation curves derived from track Number 5 of the same reference tape used for Figure 7.

D. 1. Chart track A corresponds to head track Number 2.

2. Chart track B corresponds to head track Number 5.

3. Chart track C corresponds to head track Number 8.

The track numbers are in accordance with USA Standard Recorded Magnetic Tape for Information Interchange (800 CPI, NRZI) - USASI X3.22-1967.

E. The curves shown in Figures 6 and 7 are derived under the following test conditions:

1. The tape is bulk ac erased before writing.

2. The dc erase head on the tape transport is not energized during the measurement process.

3. A slotted read-write head (IBM Assembly No. 5417960 Part No. 2510730) is used as the transducer.

4. The curves are made during a first read-after-write pass.

These are recommended NBS measurement procedures and have led to consistent and repeatable results.

F. Purchasers of the first groups of Secondary Standard Magnetic Tapes (Computer Amplitude Reference) will find that the average signal peak amplitude tracks on the accompanying strip chart recordings will consist of sequentially sampled data. This is due to the fact that only one averaging system existed at the time that these tapes were calibrated. This

single averager was commutated from track-to-track and produced an output in the form of pulses of approximately 2.5 seconds duration.

G. PR-1, LD-1, BC-1 and WD-1 are commercially available units that are part of the test transport read/write electronics system.

H. Systems are being developed that are capable of resolving the higher frequency signal components that will exist on the future types of magnetic tapes.

5. Additional Circuit Descriptions

1. Write Circuits: (Figures 2a and 2b; also Section 2,B,1)

   a. The pulse frequencies supplied by generator G-1 when making the signal amplitude tests are as follows: 200 frpi 22.5 kHz; 556 frpi 62.55 kHz; 800 frpi 90.0 kHz and 3200 frpi 360 kHz. These repetition rates are then halved by the trigger mode operation of BC-1.

   b. The output from BC-1 (Figure 2a) is clipped in the collector circuit of T_5 by the D_7 to D_{10} diode network. This results in a square wave signal having an amplitude of $\pm$ 1.4 volts that is injected into the T_6 - T_7 differential current mode switching circuit (Figure 2b). The circuit containing T_8 and T_9 forms a continuously variable current source for the switch. The current is controlled by the T_{10} - T_{11} - T_{12} Darlington type circuit CC-1 over an adjustable range of 0 - 45.0 mA. This source current is controlled and switched between T_6 and T_7 by the $\pm$ 1.4 volt signal input to the base of T_6 and passes through the write head in a direction depending upon the instantaneous "on" and "off" states of T_6 and T_7. The circuit components in both halves of the head driver circuit WD-1 are matched in order to produce equal values of write current in both directions.

2. Signal Amplitude Read Channel Circuits: (Figures 3a-3e; also Section 2,B,2)

a. The output signal from the read head (Figure 3a) passes through the line driving circuit consisting of T_{13} and T_{14}. The head cable is terminated by network TE-1 in an impedance of approximately 86Ω The signal output from PR-1 drives I-1 and DLY-1 (Figure 3b). Delay line DLY-1 is a lumped L-C line with a delay of 0.25μs per section.

b. The direct signal and its delayed signal counterpart from I-1 and I-2, respectively, are injected into the peak detector PD-1 which contains a commercially available integrated circuit high speed differential comparator IC-1. The comparator functions in the peak detection process by switching its states within 2.0 mV after the occurrence of each of the near to the peak crossover points that occur between the direct and delayed signals during each operating cycle. This switching action produces an output pulse from T_{19} that triggers strobe generator SG-1. SG-1 (Figure 3c) which is a monostable multivibrator then produces an output pulse with an adjustable width range of 0.25 - 1.2 μs. Typically a pulse width of 0.4μs is used in the NBS measurement system. The position of the strobe pulse from SG-1 is adjusted to coincide with the peak of the output signal from PO-1 by varying the gain of I-1 (Figure 3b). The strobe pulse output from T_{25} and the delayed signal component from PO-1 are then injected into the sample-and-hold circuit SH-1.

c. SH-1 (Figure 3d). SH-1 uses the bilateral switching properties of the FET transistor T_{28} to achieve sample-and-hold operation. The strobe pulse into the base of T_{26} is regenerated by the T_{26} - T_{27}

current switch and its output is applied to the input gate (G) of T_{28}. When the negative "off" gate voltage rises towards the zero volt level T_{28} turns "on" and begins the sampling process. During this time capacitor C_1 charges or discharges *via* T_{28} depending upon the relative magnitude of the input signal on the source (S) terminal and the voltage on C_1 which is tied to the drain (D) terminal. When the gate voltage returns towards -12.0 volts T_{28} is turned off and C_1 "holds" its final voltage level until the next sampling interval. The very high impedance of the FET in its "off" state prevents discharge of the capacitor voltage through that device and E-1 prevents discharge in the other direction.

d. The dc offset voltage supply for SA-1 (Figure 3e) uses a Zener diode DZ-1 as a stable voltage source. R_1 and R_2 are adjusted to set the upper and lower offset voltage levels across the precision 10 turn potentiometer R_3. Exact offset voltage values and chart recorder percentages can then be related to the potentiometer vernier dial settings.

The operation of the remainder of the read system is described in Section 2,B,2,e.

3. Signal Peak Averaging Circuit: (Figures 4a-4d; also Section 2,B,3)

a. Gating Pulse Generator Section (Figure 4a). This generator uses the 60 Hz power line voltage directly and converts the input sine waves to fast rising pulses with TD-1, T_{30} and T_{31}. The tunnel diode TD-1 in Figure 4a is loaded by the base-to-emitter junction of transistor T_{30}. The positive peak of the input 60 Hz voltage excursion from the transformer secondary causes the base-emitter load line to shift so as to switch TD-1 into its low voltage

stable state at fractional microsecond speeds. T_{30} is now held in its off state. When the input signal changes to its negative polarity peak, the tunnel diode will then switch to its high voltage state and T_{30} turns on. The voltage variations across the collector resistance of T_{30} causes T_{31} to vary its collector current accordingly. The output voltage from T_{31} is clamped and shaped by the diode network in its collector circuit. Emitter follower T_{32} drives the divide by 16 binary counter IC-2 to IC-5 with square waves whose positive excursions occur each 16.7 ms. The output of the counter consists of square waves whose positive excursions occur every 267.2 ms. It is simple to increase the number of pulses averaged per sample by adding integrated circuits to the counter thereby dividing further down. The output from T_{33} triggers three similar one-shot (OS) circuits (only OS-1 is shown in detail in Figure 4b). The output pulses from the three one-shots are then fed *via* T_{36}, T_{37}, and T_{38} into their respective identical linear integrators LI-1 and sample-hold SH-2 circuits. Only the circuits driven by T_{36} are shown in this report.

b. Gated Linear Integrator Circuit LI-1 (Figure 4c). LI-1 produces an output that is the integral of the difference in input voltage between the positive and negative terminals of OA-7. In this circuit configuration, the integrator output voltage appears across capacitor C_2 which has one side grounded. This allows C_2 to be discharged by transistor T_{39} at the desired sample time intervals. The signal integration process continues for T = 0.27 seconds which is the time that the input

gating pulse to the base of T_{39} is at its upper voltage level. At the instant that the input pulse drops to its lower level (-4.0 volts) it gates T_{39} into its "on" state which discharges C_2 back towards zero volts and the integration process is repeated. The output from C_2 is fed to the signal input (Point G) of SH-2 (Figure 4d) *via* the high input impedance circuit E-2. The sample-and-hold voltage across the capacitor C_3 is prevented from leaking during the hold period by the very high impedance T_{44}-OA-9 circuit. The operation of the remainder of the circuit consisting of I_4 and SA-2 is the same as described in Section 2,B,2,e.

6. Component List

The mention of specific equipments or components is not to be construed as an endorsement of these items by NBS to the exclusion of other equivalent devices. There is considerable latitude particularly in the choice of semiconductor devices such as transistors and diodes. The following is a tabulation of the semiconductor devices that were used in the NBS measurement system in each channel. Only the components of pulse generator G-2 (Figure 4a) are common to all channels.

Transistor Types	T (Number in Figs.)	Remarks
2N3646	10,18,20,29	NPN-Switching
2N3638	19,22-27,31-42	PNP-Switching
*Unmarked	1-9,13-17	See Footnote
2N4222A	28,43,44	N-Channel FET
2N1700	11,12,21	NPN-Switching
2N976	30	PNP-High-speed Switching

Diode Types	D (Number in Figs.)	Remarks
1N916	12-14,19,20,27-30, 32-35,37-40	Si Switch
1N276	17,18,21-26,31,36,41	Ge Switch
*Unmarked	1-11,15,16	See Footnote
1N1766A	DZ-1	Zener Diode
WX822B	TD-1	Tunnel Diode(5mA)

*The devices designated as "unmarked" are located in the commercially available PR-1, WD-1, BC-1 and LD-1 circuits. It was found that the NPN and PNP transistors are replaceable with 2N3646's and 2N3638's respectively in the PR-1, BC-1 and LD-1 circuits. In the WD-1 circuit T_6 and T_7 can be replaced by 2N3831's and T_8 and T_9 can be replaced with 2N3646's.

Integrated Circuit Types	Number in Figures	Remarks
Type 710	IC-1	High Speed Differential Comparator (For example μA710C Fairchild Semiconductor)
MC358	IC-2 to IC-5	J-K Flip-Flop (Motorola Semiconductor Products, Inc.)

Operational Amplifier	Number in Figures	Remarks
PP45U	OA-1 to OA-11	Philbrick Researches, Inc.

7. Acknowledgments

The assistance of Mr. A. W. Ericson (Information Processing Technology Division) with the construction, testing and operation of the measurement system is gratefully acknowledged. The assistance of Mrs. R. E. Davis (Information Processing Technology Division) and Mrs. R. S. Maddock (Analytical Chemistry Division) with the preparation of the report is also gratefully acknowledged.

8. Appendix A

The design of the signal peak averaging system is based upon the following mathematical considerations:

The average signal peak amplitude, $\bar{e}_{peak}$, is defined as the sum of the pulse peak amplitudes, e_i, divided by the number, n, of such pulses which are in the interval, T, being averaged, *i.e.*,

$$\bar{e}_{peak} = \frac{1}{n} \sum_{i=1}^{n} e_i \qquad (1)$$

The passage of the signal pulse train through a peak sample-and-hold circuit (SH-1) converts each incoming pulse into a corresponding voltage step, E, whose amplitude is equal to the signal peak e and whose duration is Δt. The increase in output voltage from the linear integrator LI-1 over each Δt due to its integration of each incoming voltage step, for example say the ith pulse, is

$$e_{oi} = \frac{1}{RC} \int_{(i-1)\,\Delta t}^{i\Delta t} E_i \, dt \qquad (2)$$

Since E_i is a constant amplitude over Δt, therefore the voltage output from LI-1 increases during the ith interval by

$$e_{oi} = \frac{E_i \, \Delta t}{RC} \qquad (3)$$

Since the amplitude of each E_i is by definition equal to each e_i (where, i = 1, 2, $\cdots$n) we can after inverting Equation 3 substitute it into Equation 1 to get

$$\bar{e}_{peak} = \frac{RC}{T} \sum_{i=1}^{n} e_{oi} \qquad (4)$$

where $T = n\Delta t$ the total sampling interval.

Equation 4 shows that when the RC product of the elements of the linear integrator is adjusted to be exactly equal to the sampling time, that is, when $\frac{RC}{T} = 1$, then the final integrator output at the end of each sampling time, T, is exactly equal to the average peak amplitude of the n pulses which occur within the sampling interval. Generally, Equation 4 shows that the average peak value of a train of equi-spaced pulses that have been peak sampled- and-held and then linearly integrated over a sampling time, T, is proportional to the output of the linear integrator system by the factor $\frac{RC}{T}$.

In summary, the measurement of the average signal peak amplitude as defined by Equation 1 is accomplished through the solution of Equation 4 which is based on linear integration and sample-and-hold operations.

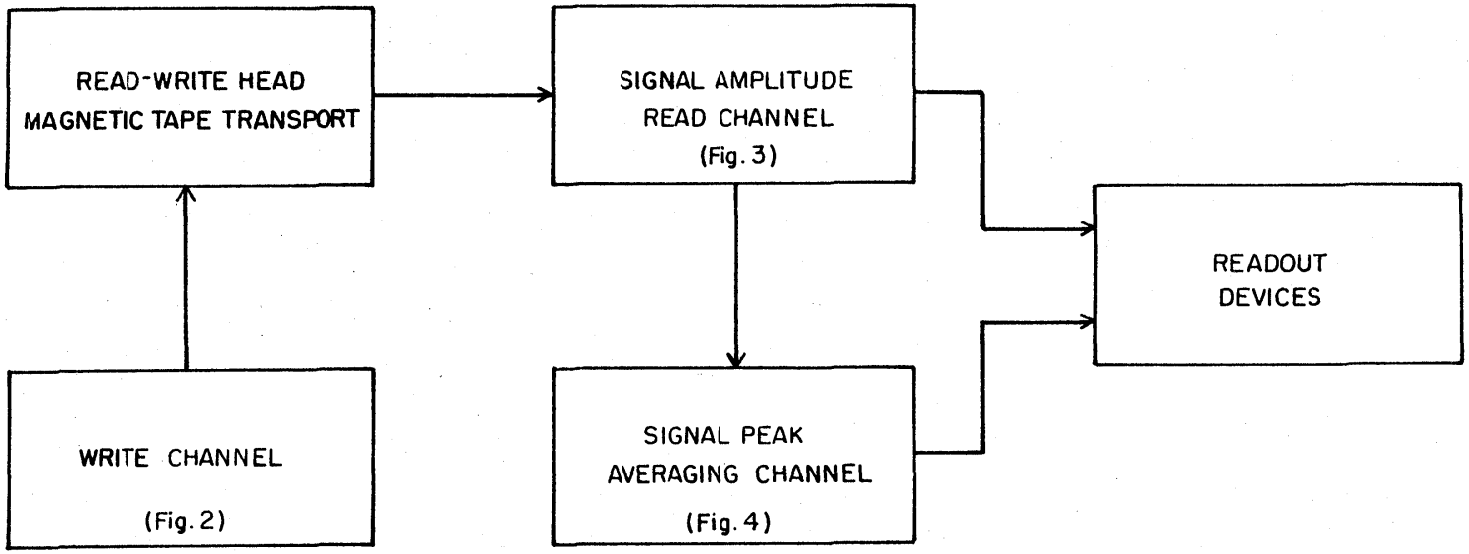

Figure 1. NBS Measurement System.

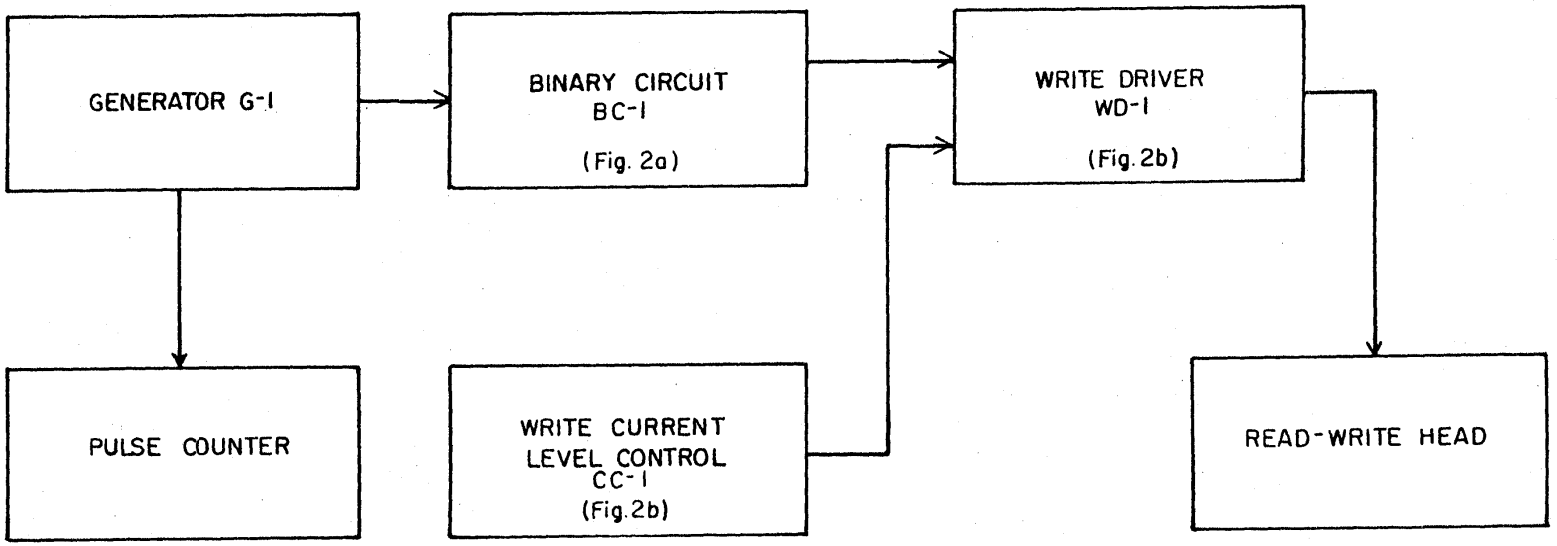

Figure 2. Write Channel Block Diagram

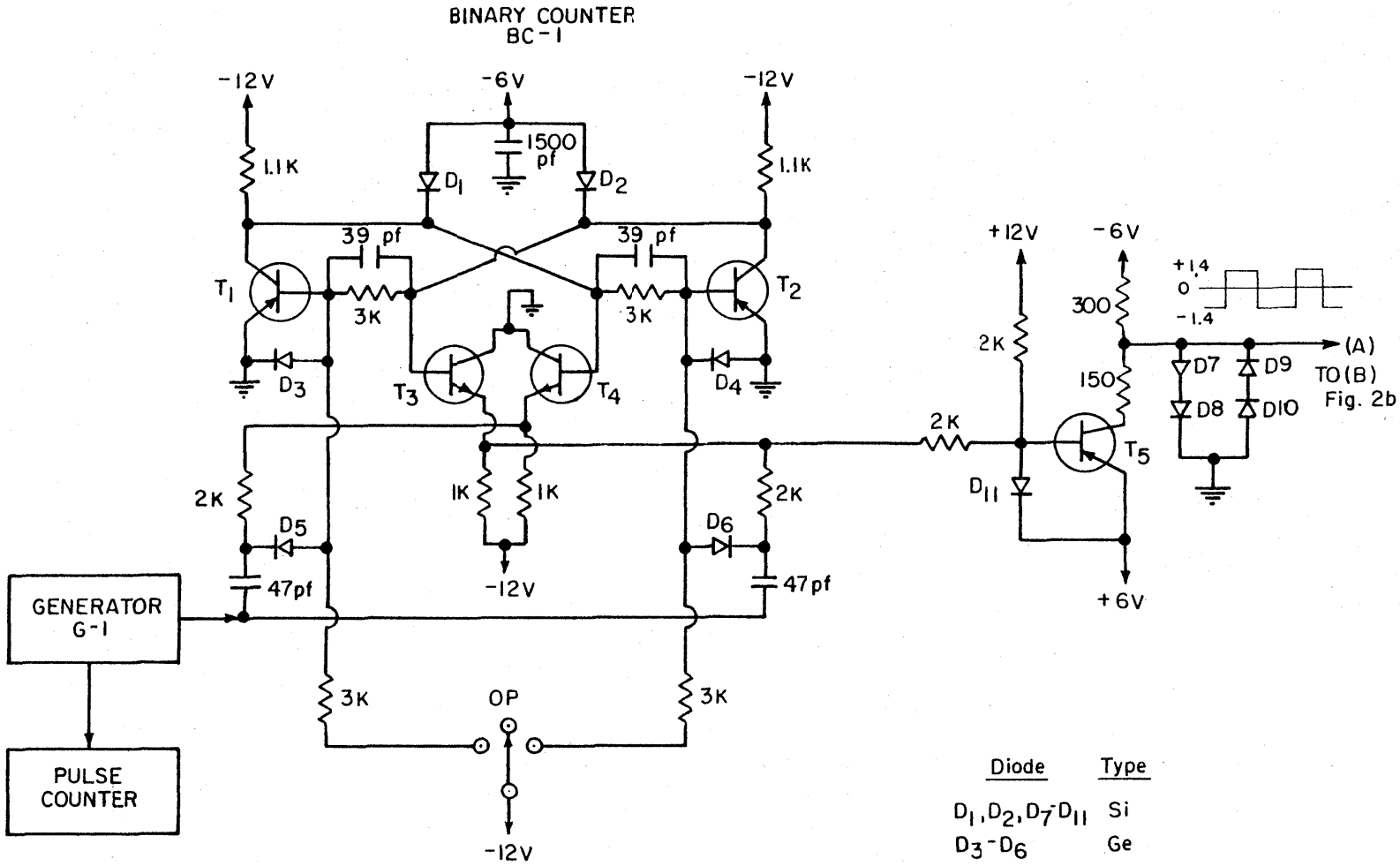

Figure 2a. Write Channel Circuits. (BC-1)

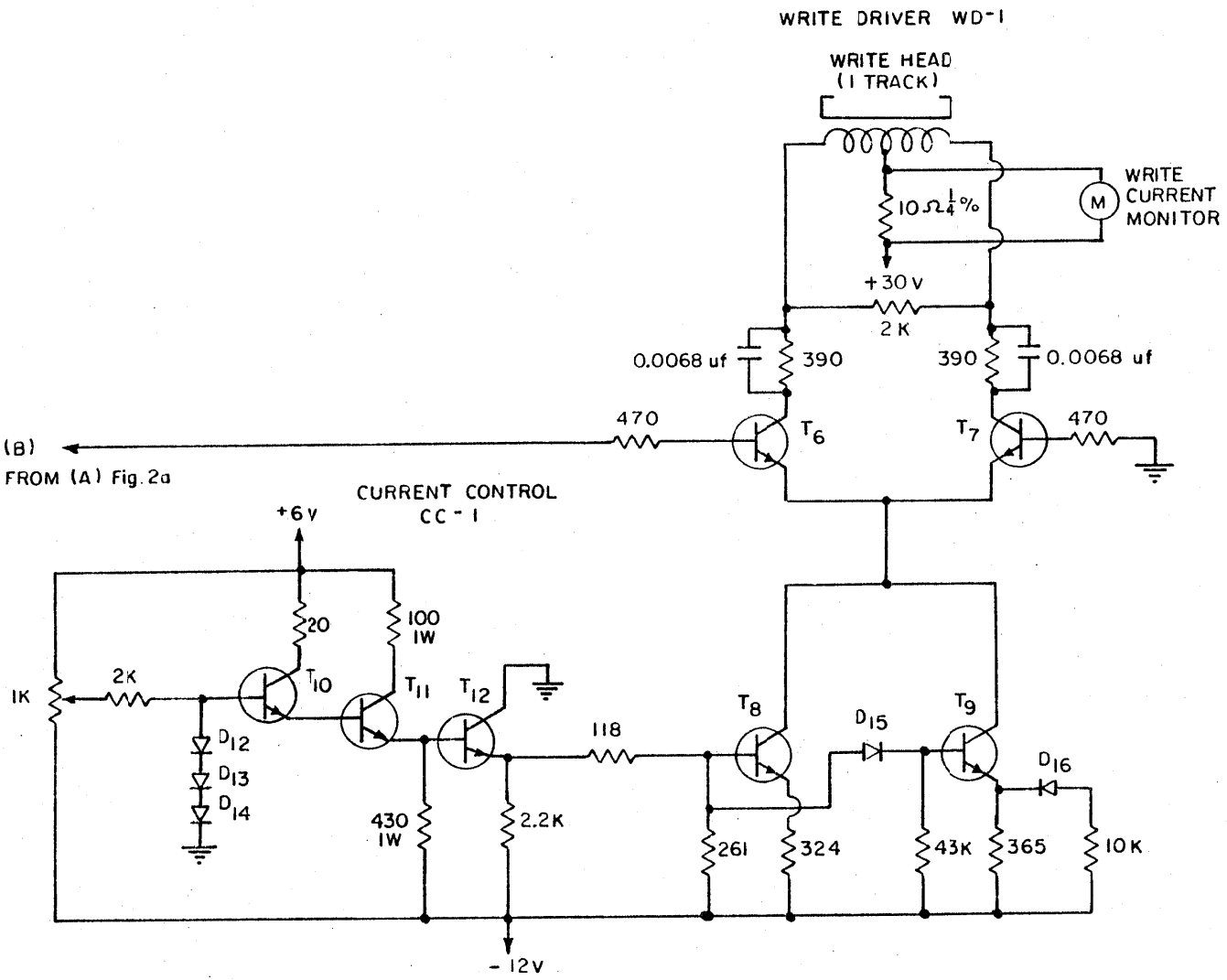

Figure 2b. Write Channel Circuits. (CC-1, WD-1).

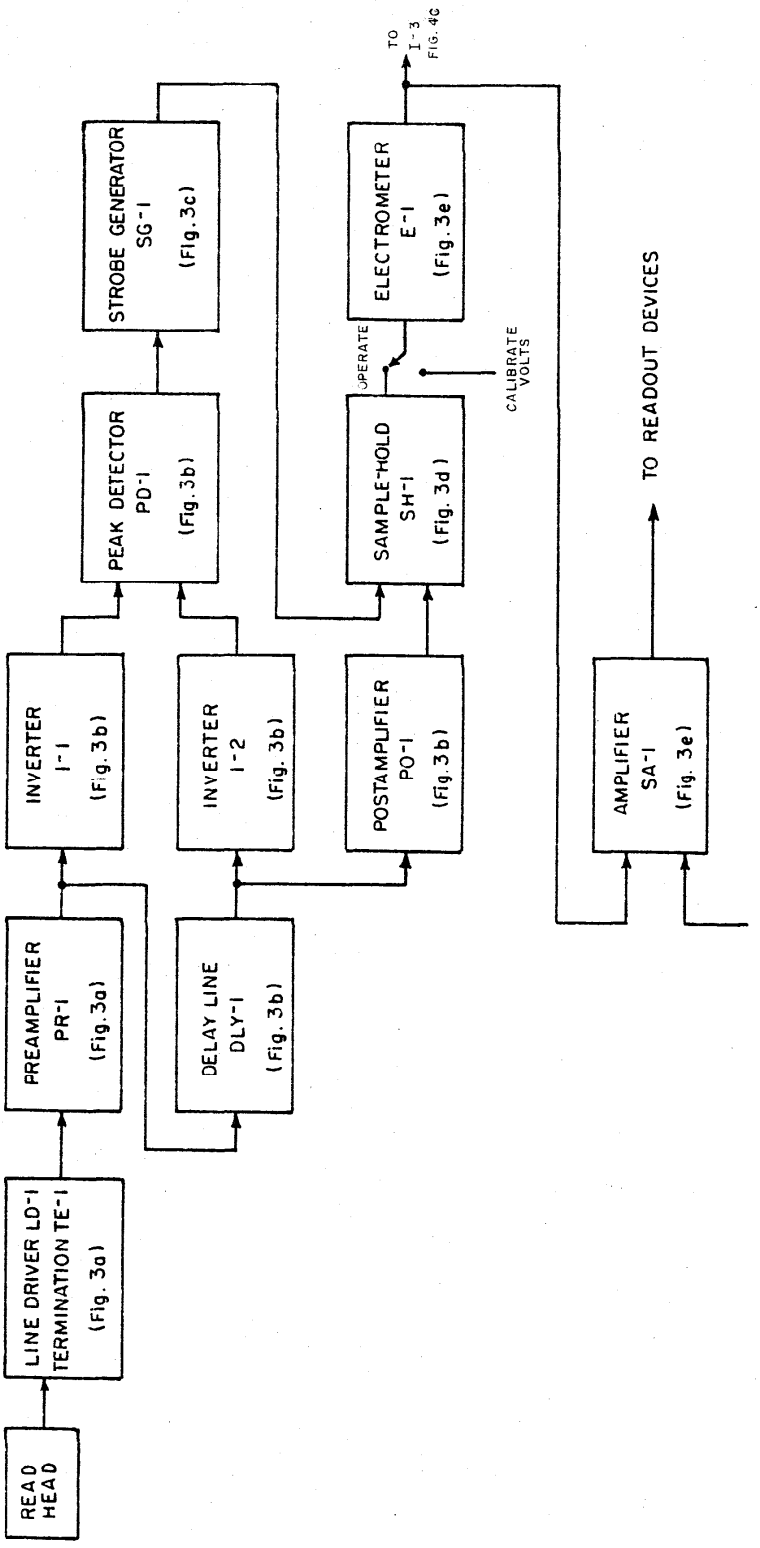

Figure 3. Signal Amplitude Read Channel.

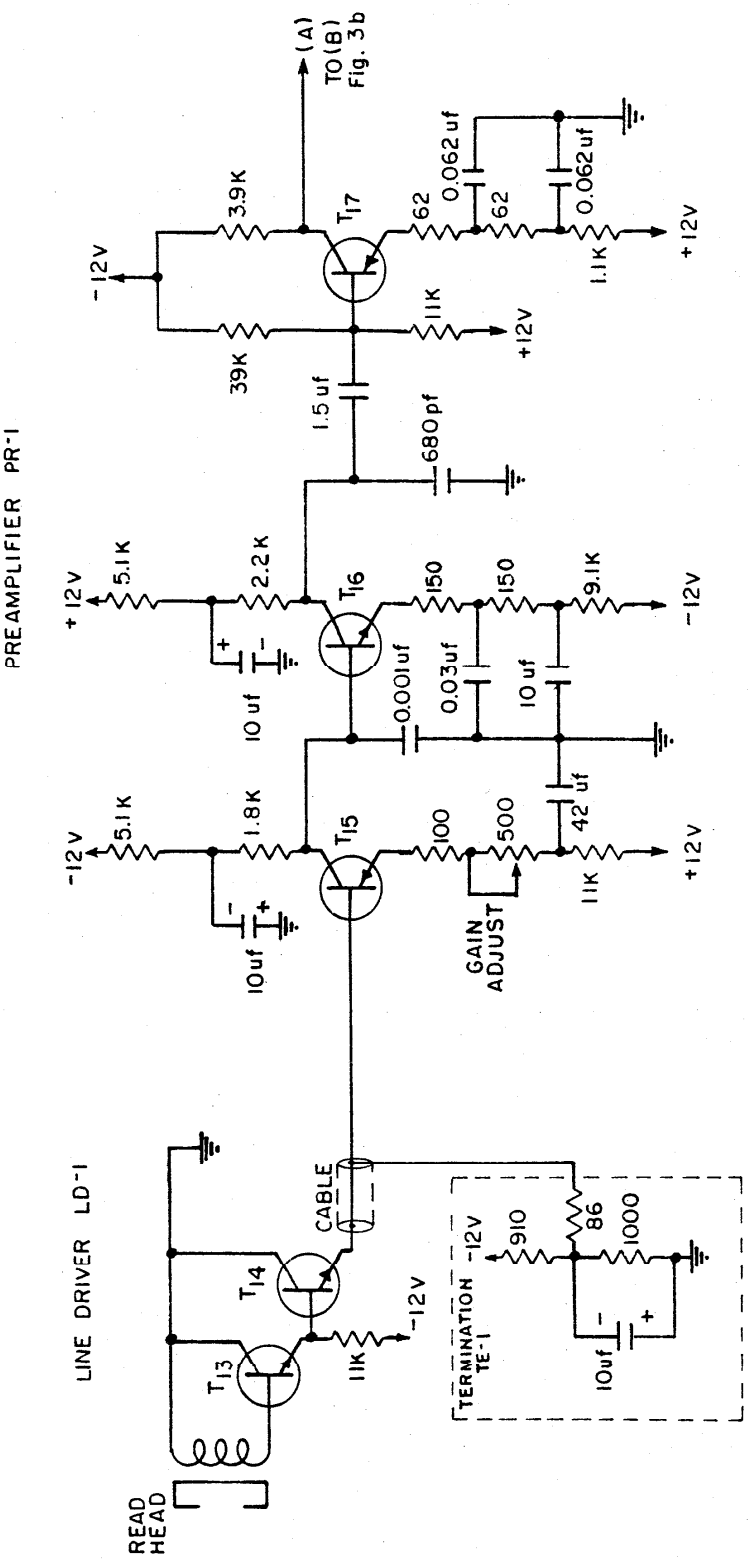

Figure 3a. Signal Amplitude Read Channel Circuits. (LD-1, TE-1, PR-1).

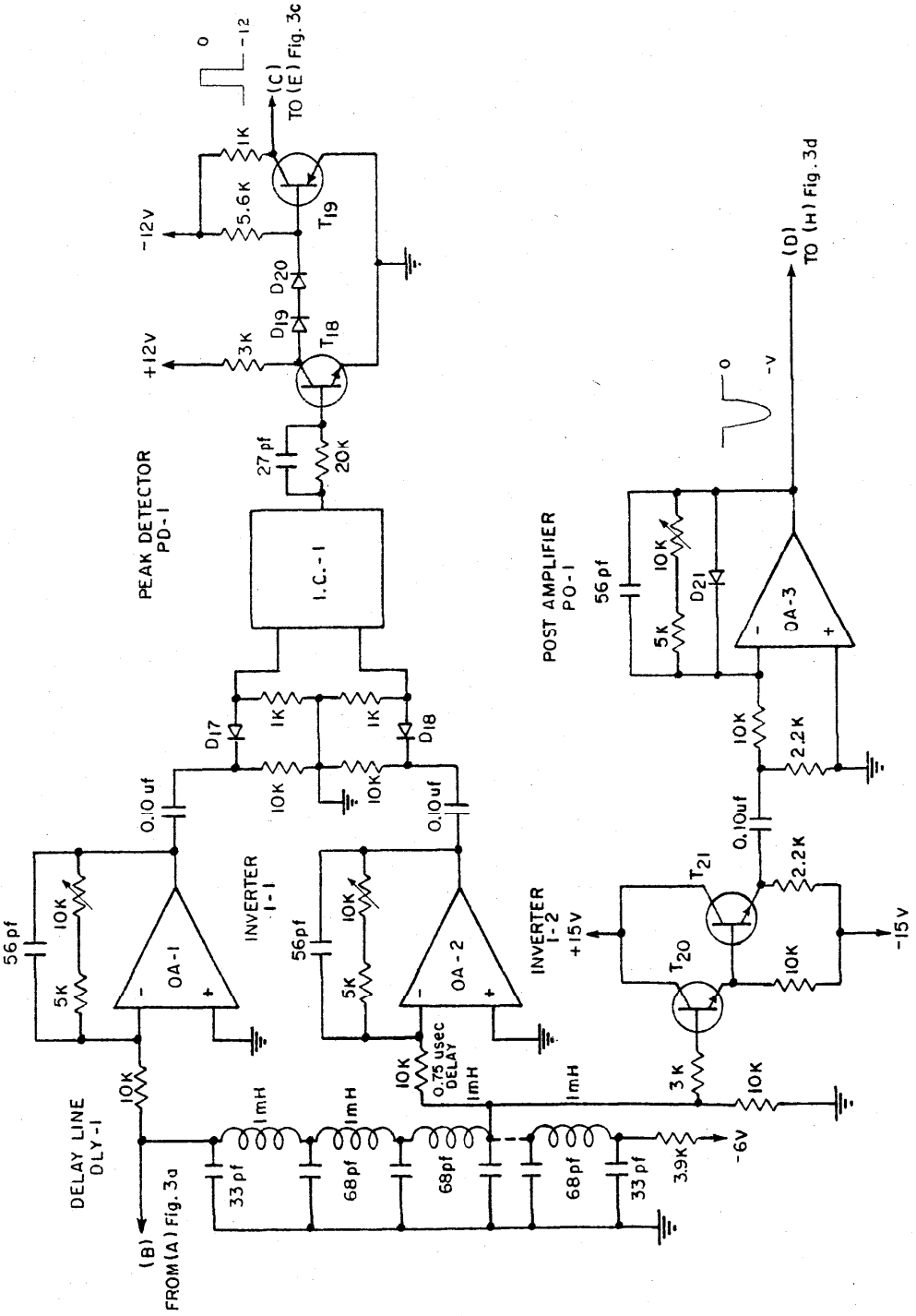

Figure 3b. Signal Amplitude Read Channel Circuits. (DLY-1, I-1, I-2, IC-1, PO-1, PD-1).

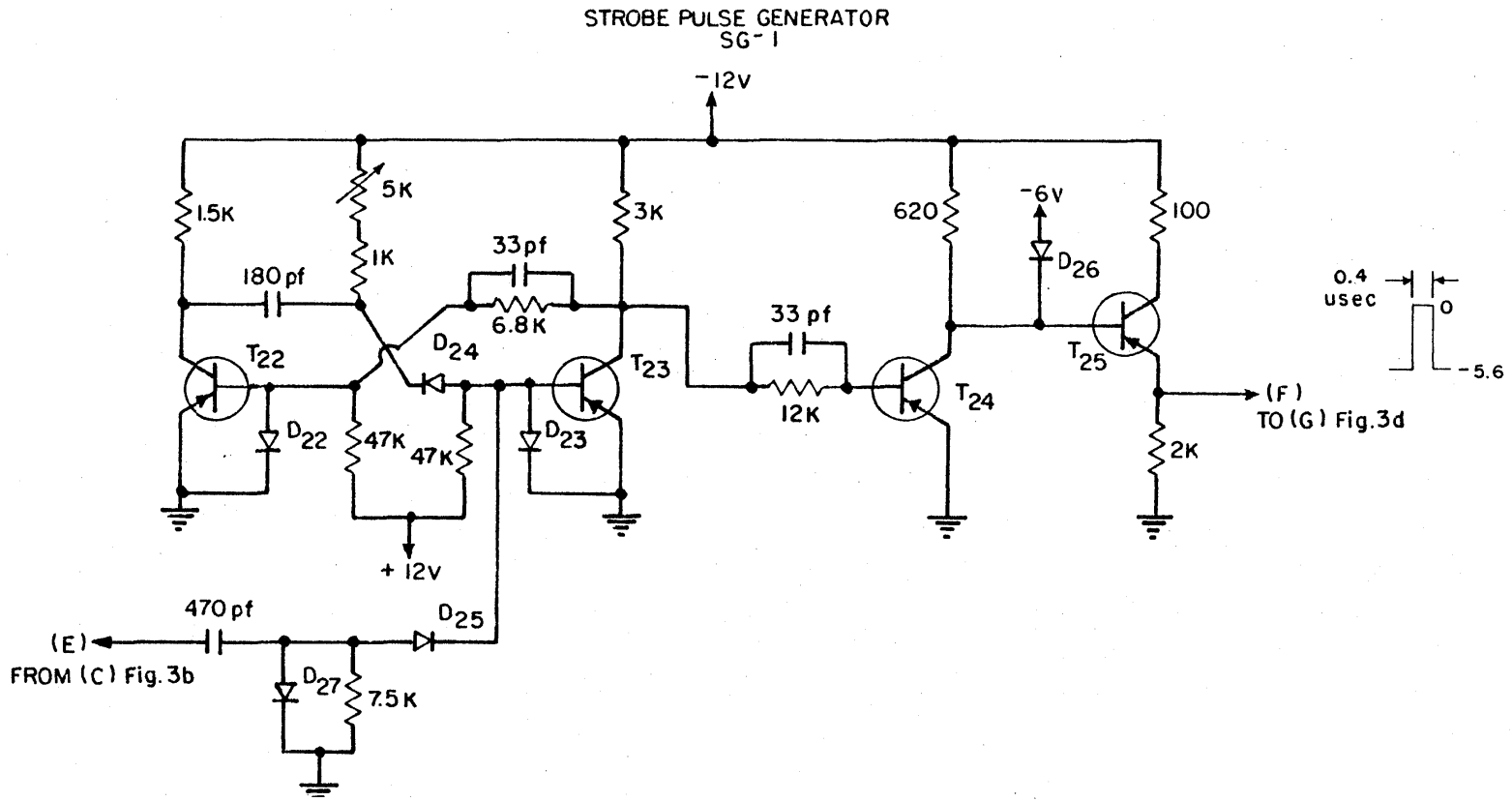

Figure 3c. Signal Amplitude Read Channel Circuits. (SG-1).

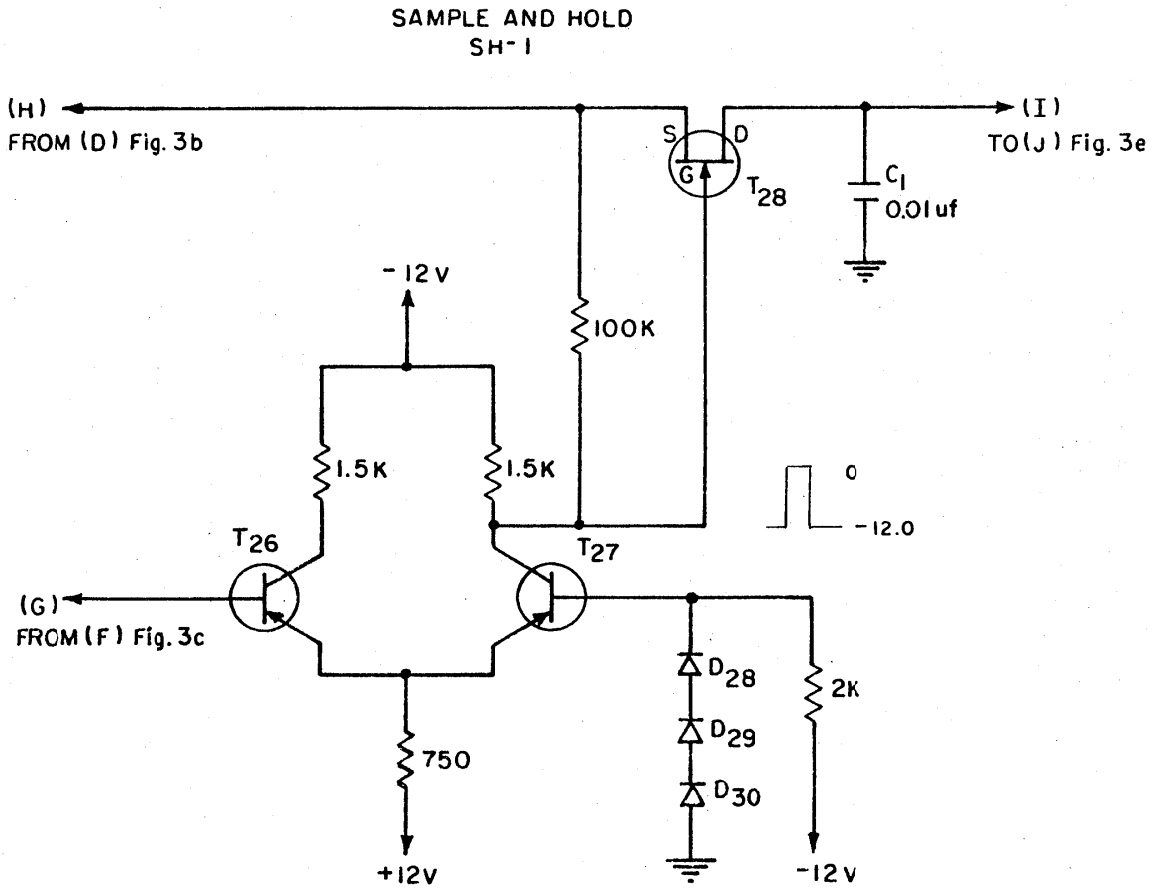

Figure 3d. Signal Amplitude Read Channel Circuits. (SH-1).

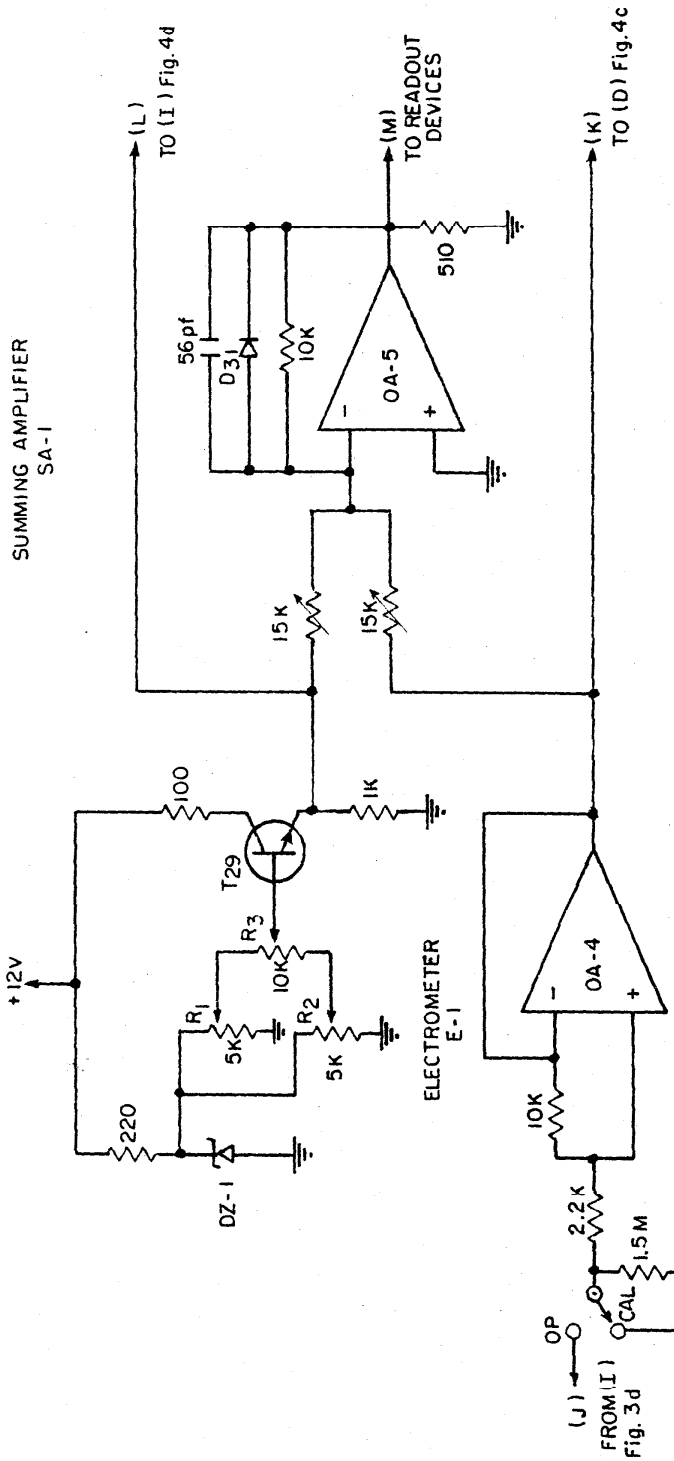

Figure 3e. Signal Amplitude Read Channel Circuits. (E-1, SA-1).

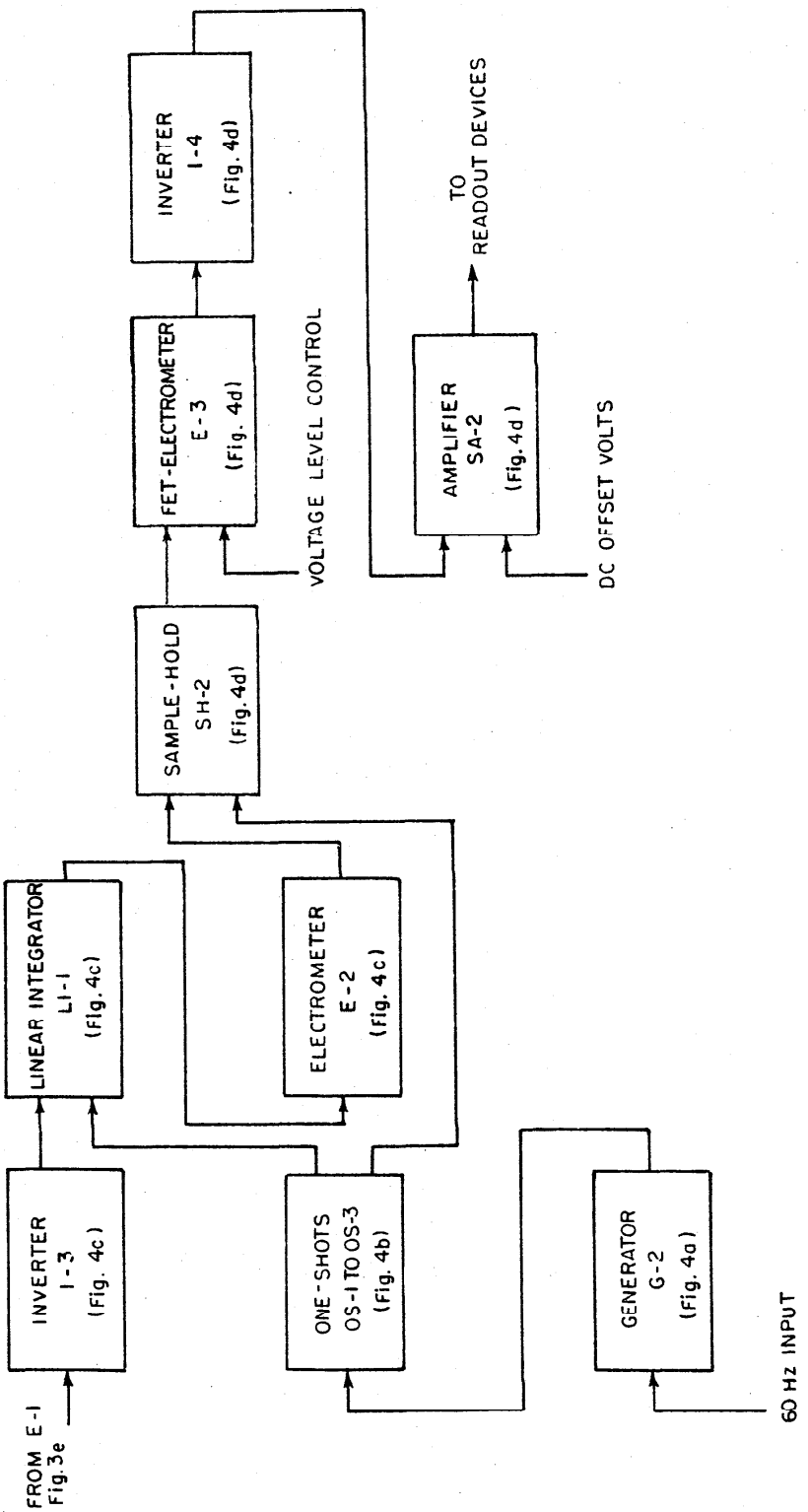

Figure 4. Signal Peak Averaging Channel.

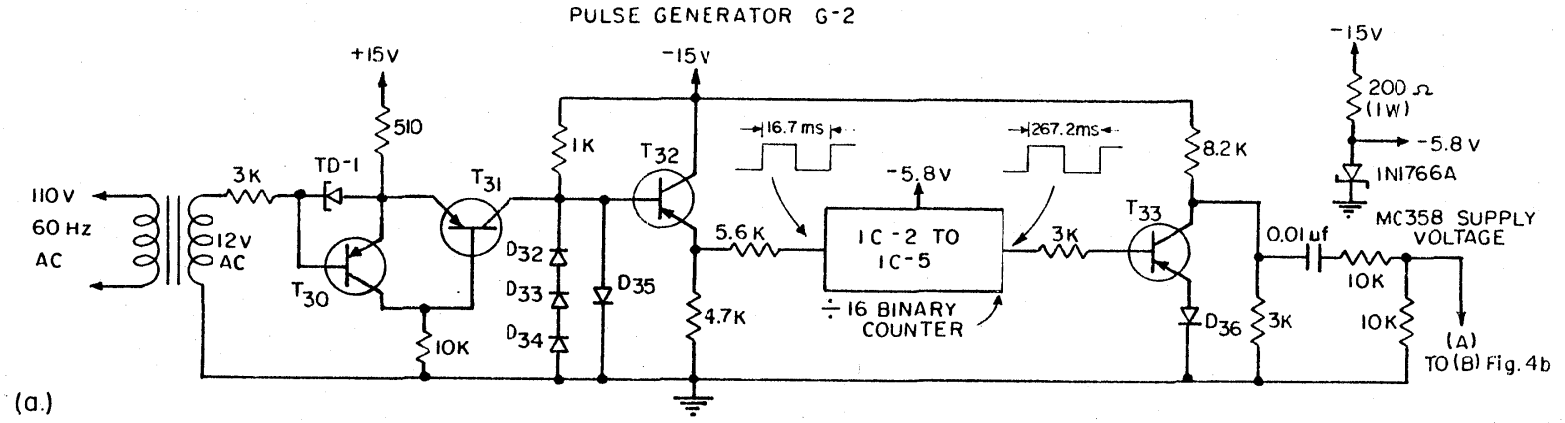

Figure 4a. Signal Peak Averaging Channel. Pulse Generator G-2.

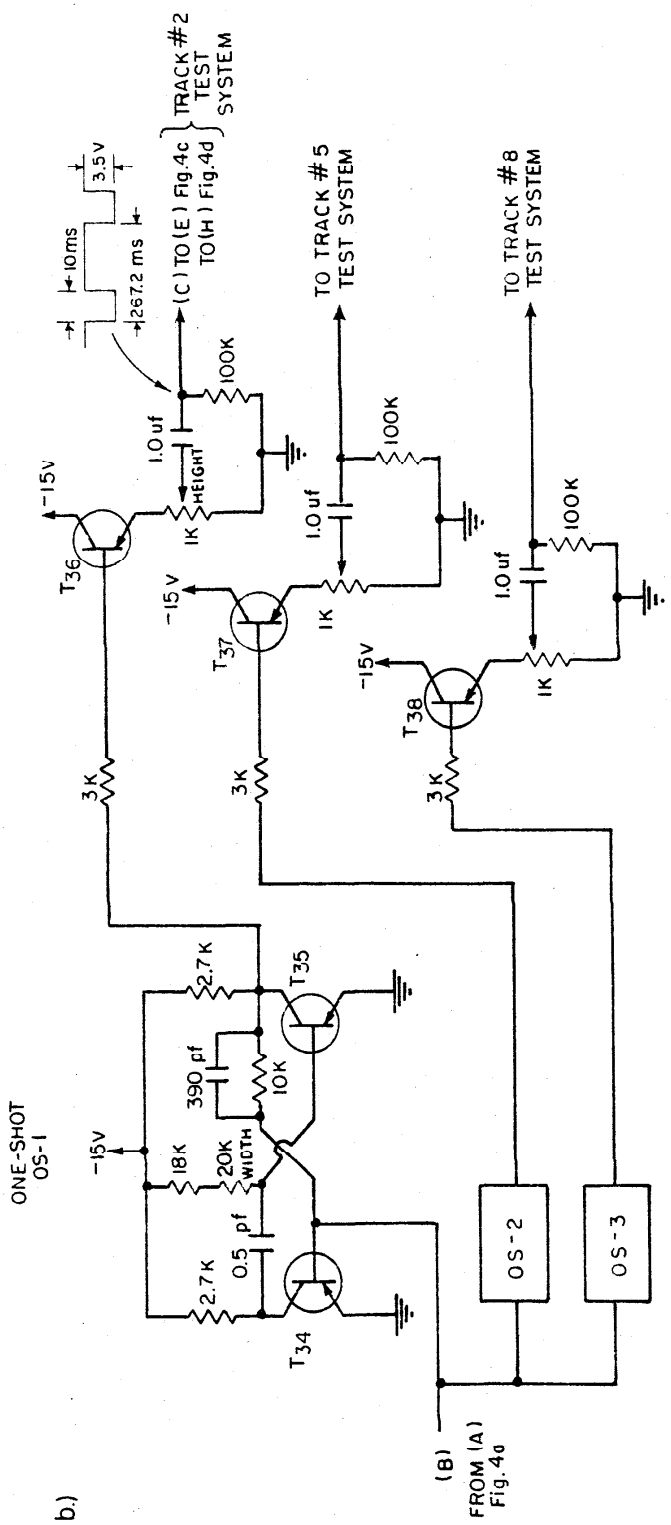

Figure 4b. Signal Peak Averaging Channel Circuits. (OS-1 to OS-3).

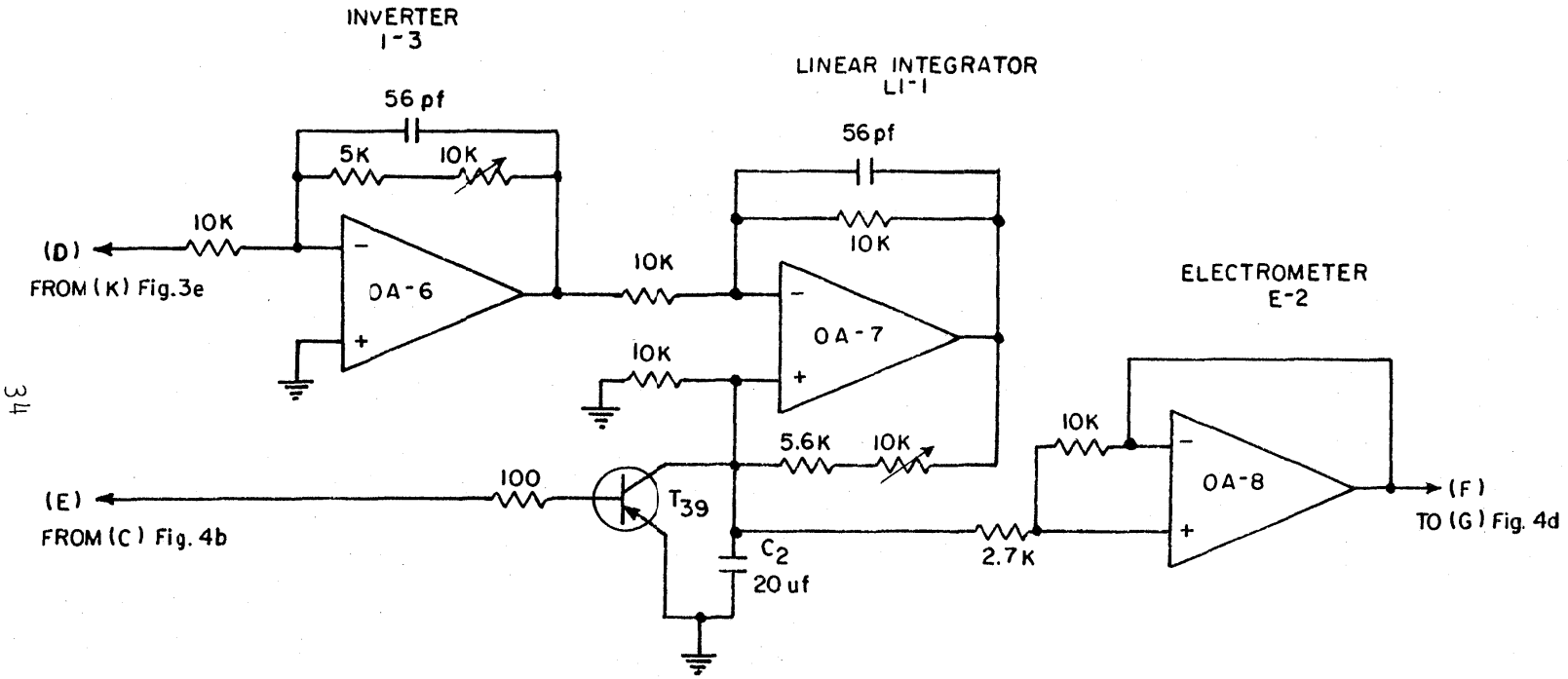

Figure 4c. Signal Peak Averaging Circuits. (I-3, LI-1, E-2).

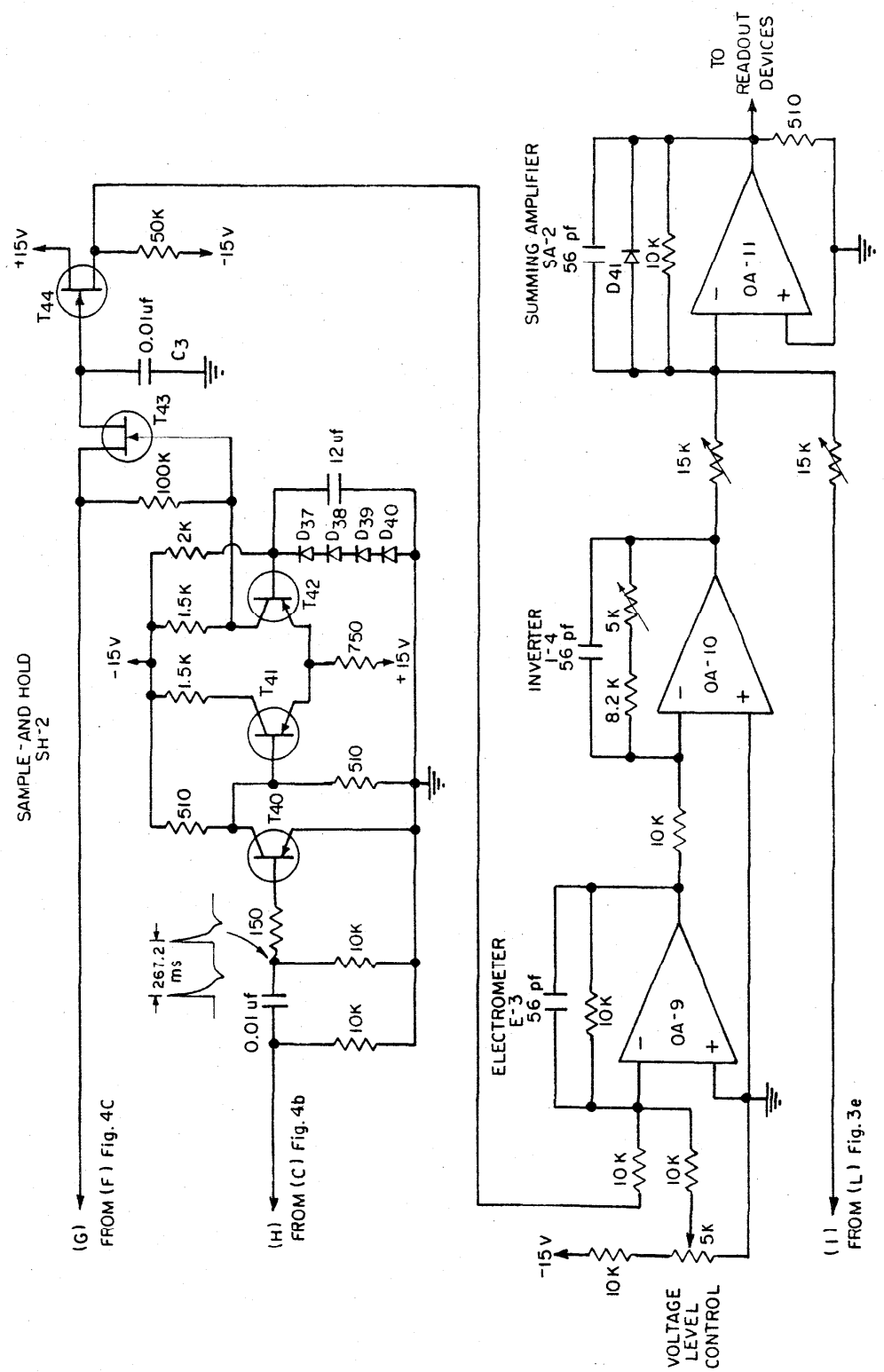

Figure 4d. Signal Peak Averaging Circuit (SH-2, E-3, I-4, SA-2).

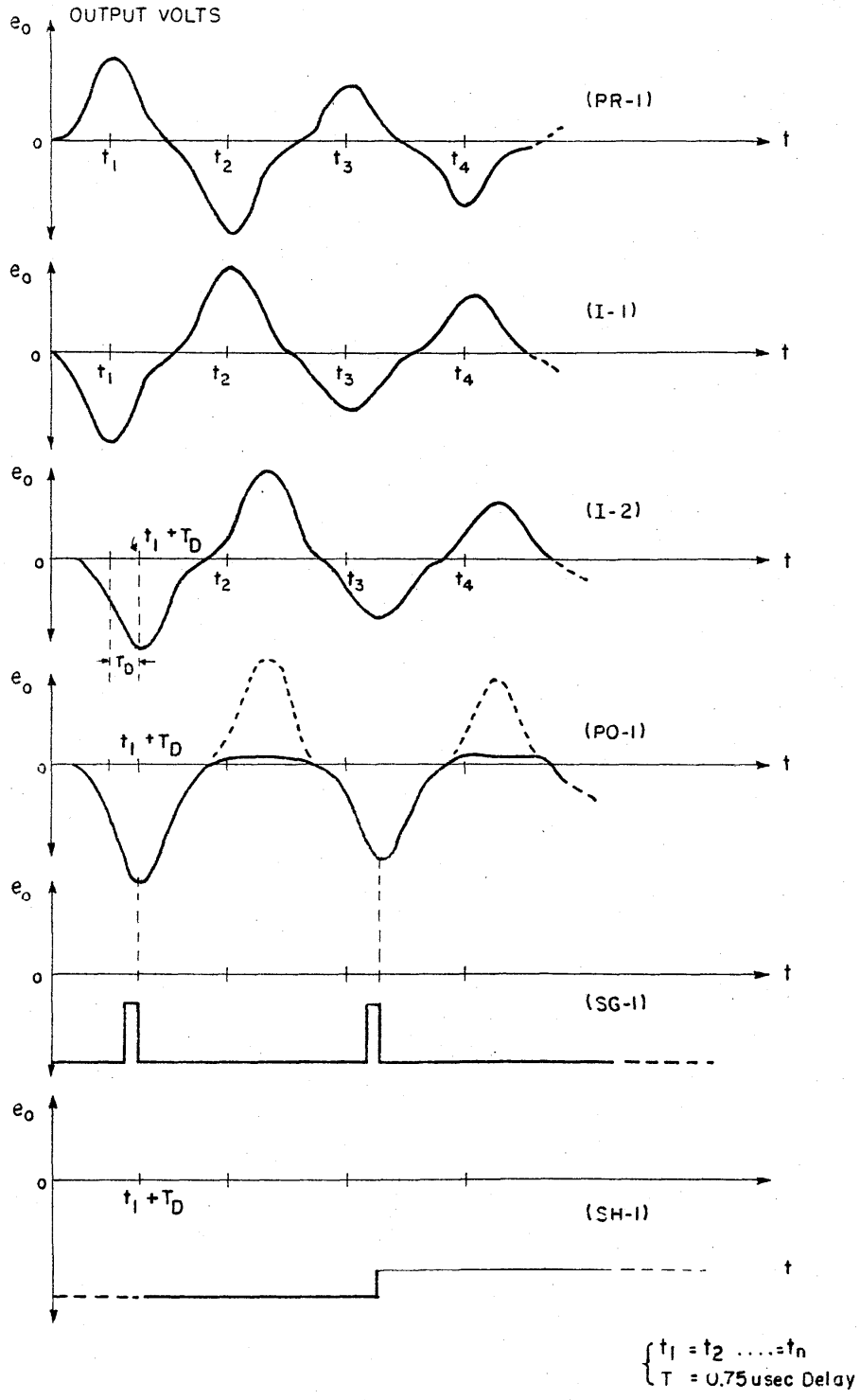

Figure 5. Signal Amplitude Read Channel Timing Diagram.

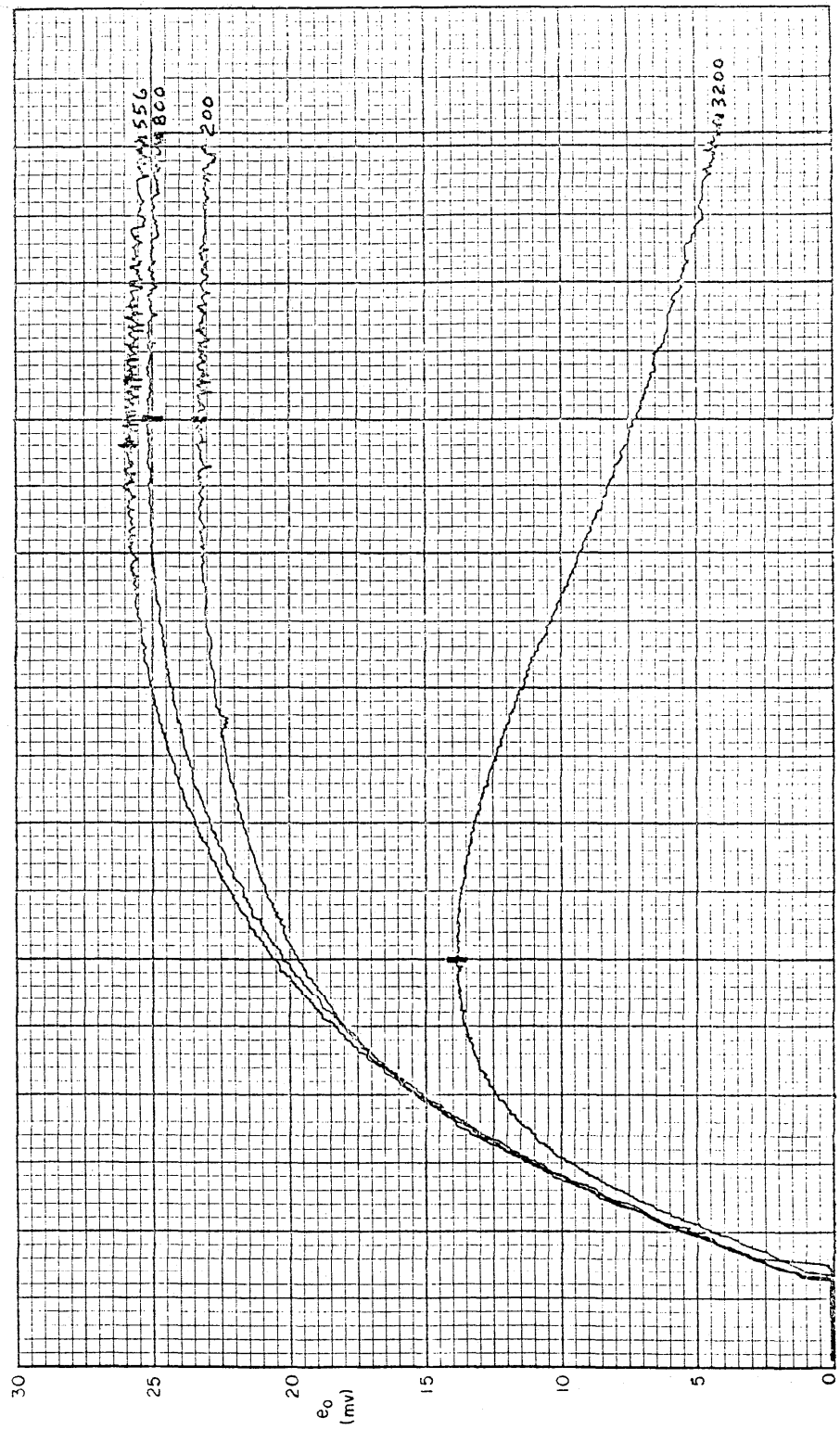

Figure 6. Family of e_o versus I_w Saturation Curves for an NBS Secondary Standard Magnetic Tape

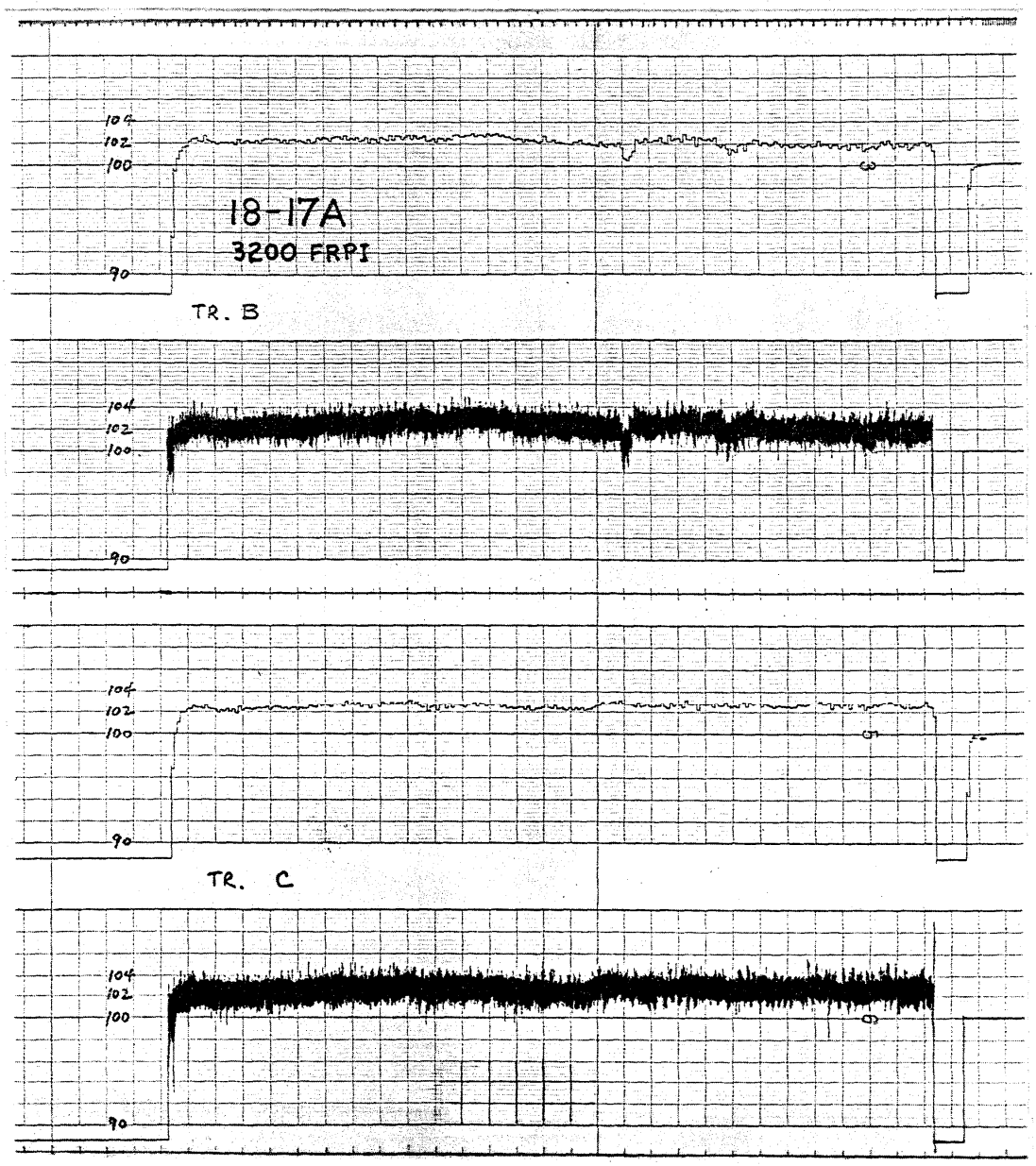

Figure 7. Full Length Recording of the Signal Amplitude and the Average Signal Peak Value on the Same Tape Used in Figure 6.