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Electron Beam Induced Damage in PECVD Si₃N₄ and SiO₂ Films on InP

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ELECTRON BEAM INDUCED DAMAGE IN PECVD

Si₃N₄ AND SiO₂ FILMS ON InP

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ABSTRACT

Phosphorus rich plasma enhanced chemical vapor deposition (PECVD) of silicon nitride and silicon dioxide films on n-type indium phosphide (InP) substrates were exposed to electron-beam irradiation in the 5 to 40 keV range for the purpose of characterizing the damage induced in the dielectric. The electron-beam exposure was on the range of 10^{-7} to 10^{-3} C/cm². The damage to the devices was characterized by capacitance-voltage (C-V) measurements of the metal insulator semiconductor (MIS) capacitors. These results were compared to results obtained for radiation damage of thermal silicon dioxide on silicon (Si) MOS capacitors with similar exposures.

The radiation induced damage in the PECVD silicon nitride films on InP was successfully annealed out in an hydrogen/nitrogen (H₂/N₂) ambient at 400 C for 15 min. The PECVD silicon dioxide films on InP had the least radiation damage, while the thermal silicon dioxide films on Si had the most radiation damage.

INTRODUCTION

Electron beam lithography of fine line geometries for microelectronics has become more common as feature sizes continue to shrink. For high frequency devices such as InP metal insulator semiconductor field effect transistors (MISFETs) and gallium arsenide (GaAs) metal semiconductor field effect transistors (MESFETs), gate definition by electron beam exposure of photoresist has become a standard practice. Direct-write electron-beam lithography has found only a few applications in the production of Si MOSFET technology very large scale integrated circuits. Electron-beam exposure of the sensitive gate insulator and channel region of the semiconductor causes positive charge trapping in the bulk oxide resulting in large threshold voltage (V_{th}) shifts and in turn device degradation (1). As feature sizes decreased, required electron-beam energies have increased to above 30 keV because of backscattering effects (2). However higher beam energies are expected to magnify problems associated with electron-beam induced damage.

The purpose of this study is to measure the change in the C-V characteristics for MIS structures on InP substrates as a function of exposure to high energy electron beams. Two promising gate dielectric materials for InP MISFET technology are silicon nitride and silicon dioxide.

Phosphorus rich silicon nitride and silicon dioxide films were plasma deposited on InP substrates and MIS capacitors were formed. High frequency C-V measurements were made for various electron-beam exposures. Typical exposures and beam energies

for electron-beam lithography are 4.0×10^{-5} C/cm² and 30 keV respectively (2). While the range of exposures and energies used in this study were from 10^{-7} to 10^{-3} C/cm² and 5 to 40 keV respectively. Shifts in the C-V measurements were used to characterize the extent and type of damage to the insulator. Low temperature H₂/N₂ anneals were performed on PECVD silicon nitride capacitors after irradiation because low temperature anneals of electron-beam damaged MOS devices have shown recovery of C-V data (1). Electron-beam induced damage of thermal silicon dioxide on Si MOS capacitors were also studied for comparison.

SAMPLE PREPARATION

All of the MIS capacitors were fabricated on n-type InP 2 inch diameter polished wafers of (100) orientation with carrier concentrations from 4.0 to 4.1×10^{15} cm⁻³. All the MOS capacitors were fabricated using boron doped P-type Si 3 inch diameter polished wafers also of (100) orientation and impurity concentrations on the order of 3.0×10^{15} cm⁻³.

The first step in the processing of these devices was to perform a substrate degrease and initial cleaning. The InP substrate cleaning procedure began with a degreasing process consisting of a 5 min soak in boiling trichloroethylene, followed by 5 min soaks in acetone then methonal, each with ultrasonic agitation. The last step was a 5 min deionized water (DI H₂O) rinse. After degreasing, the rest of the substrate cleaning consisted of the following steps (3):

- (i) (1:1:4)12:1 (HCl:HF:H₂O):H₂O₂ for 30 sec.
- (ii) 10 wt % H₃PO₄ in H₂O for 3 min.
- (iii) DI H₂O rinse for 5 min.
- (iv) 10 wt % HIO₃ in H₂O for 3 min.
- (v) DI H₂O rinse for 5 min.
- (vi) (1:1:4)12:1 (HCl:HF:H₂O):H₂O₂ for 15 sec.
- (vii) 10 wt % H₃PO₄ in H₂O for 15 sec
- (viii) DI H₂O rinse for 5 min.
- (ix) Blow dry with N₂

The first two steps strip the native oxide. Then the fourth step etches about 1000 Å of InP to remove any polish damage. Steps six and seven strip any native oxide that might have formed during the HIO₃ solution.

The Si substrate cleaning procedure began with the same degrease as above followed by these steps:

- (i) Hot soak in H₂O/H₂O₂/NH₄OH solution for 15 min.
 - (a) 50 ml of NH₄OH and 250 ml of DI H₂O at 70±5C.
 - (b) add 50 ml of H₂O₂.
 - (c) let bubble for 2 min before soaking wafers.
- (ii) DI H₂O rinse for 5 min.
- (iii) (1:1) (HF:H₂O) for 2 min.
- (iv) DI H₂O rinse for 5 min.
- (v) Hot soak in H₂O/H₂O₂/HCl solution for 15 min.
 - (a) 50 ml of HCl and 200 ml of DI H₂O at 70±5 C.
 - (b) add 50 ml of H₂O₂.
 - (c) let bubble for 2 min before soaking wafers.
- (vi) DI H₂O rinse for 5 min and blow dry in N₂.

Step one oxidizes any remaining organic contaminants on the substrate surface and also removes heavy metals by forming complex amine groups with them. Then step three etches the native oxide. Finally step four removes any light alkali ions and prevents displacement plating from the solution (6). This clean removes residual organic, ionic, and atomic contamination from the Si surface.

The InP initial cleaning was followed by the formation of

ohmic contacts. The ohmic contacts were formed on the backside by electron-beam evaporation. For the InP substrates a 900 Å layer of a gold-germanium (Au-Ge) eutectic (12 wt % Ge in Au) was deposited first. Then 250 Å of nickel (Ni) was deposited second followed by an overlayer of Au 2000 Å thick. This trilayer of metal was then alloyed for 10 min in N₂ at 400 C.

In the case of the Si substrates, the initial clean was followed by the insulator growth. A dry thermal oxidation was performed in an open ended furnace tube. The O₂ flow rate was 500 sccm at a furnace temperature of 900 C for 9.0 hours. The oxidation was succeeded by a 15 min N₂ anneal at the same temperature with 500 sccm of N₂ flowing. These conditions resulted in a silicon dioxide thickness of 900 Å with a refractive index of 1.44. Then a single 3000 Å layer of Al was electron beam evaporated onto the backside for an ohmic contact.

The silicon nitride and silicon dioxide films were deposited on InP substrates in a Technics Planar Etch II-A plasma deposition system modified for operation at 13.56 MHz with automatic matching. The InP substrates were placed on the heated and grounded lower electrode. The reactant gases were introduced through a manifold and flowed radially inward to an exhaust port in the center of the lower electrode. The flow rates of these gases were maintained with digital mass flow controllers and the deposition pressure was regulated by an electrically controlled throttle valve in the exhaust line.

Prior to performing a deposition, the empty chamber was first etched with a CF₄ plasma of 150 W at 250 mTorr for 5 min. This cleaned the chamber of contaminants from previous

depositions. The next step was a N_2 plasma burn with an N_2 flow rate of 30 sccm for 5 min at 150 W. This step prevented any fluorine contamination of the film from the previous CF_4 etch. The last step before loading the samples was to outgas the chamber by baking it at 300 C for 5 min using the heater in the lower electrode with 20 sccm of N_2 flowing.

After cooling the chamber, the InP substrates and the red amorphous phosphorus source was loaded into the chamber. The phosphorus was contained in a ceramic boat with an aluminum top that had small holes for the phosphorus to escape. The samples were placed between the phosphorus source and the exhaust port. Before starting the deposition, the phosphorus was allowed to bake at 300 C for 1 hour using the substrate heater with 30 sccm of N_2 flowing to outgas the chamber again. This was followed by a N_2 plasma at 30 W with 20 sccm of N_2 for 5 min. The same temperature of 300 C was maintained using the substrate heater. This step deposits a layer of phosphorus onto the InP substrates. The final step prior to the film deposition was a N_2O plasma at 30 W with 30 sccm of N_2O at 300 C for 5 min. This step oxidized the phosphorus and also reduced the thickness of the already deposited phosphorus layer.

Both dielectric films were deposited with a phosphorus rich region 80-100 Å thick at the insulator-semiconductor interface. This region improves the interface properties and reduces the interface state density (4). The silicon nitride films were deposited at a substrate temperature of 300 C and a chamber pressure of 500 mTorr. The flow rates of the reactant gases were 40 sccm of N_2 , 40 sccm of ammonia (NH_3) and 15 sccm

of silane (SiH_4). An RF power of 30 W was maintained for 5 min. The silicon dioxide films however were deposited at a substrate temperature of 275 C at a pressure of 800 mTorr. Flow rates of 55 sccm of nitrous oxide (N_2O) and 17.4 sccm of SiH_4 were used. The RF power was also 30 W for 5 min. In the case of both films, the flow rates of the reactant gases and the chamber pressure was allowed to stabilize for 5 min before the plasma was ignited. These deposition conditions yielded a silicon nitride film thickness of 900 A with a refractive index of 1.99. The silicon dioxide film thickness was 1000 A with a refractive index was 1.49.

One wafer of PECVD Si_3N_4 was furnace annealed in an H_2/N_2 ambient at 400 C for 15 min. The gas ratio in the furnace was (2:1) ($\text{N}_2:\text{H}_2$) with an H_2 flow rate of 1000 sccm. This now gave a total of 4 different samples: unannealed PECVD phosphorus rich silicon nitride on InP, H_2/N_2 annealed PECVD phosphorus rich silicon nitride on InP, unannealed PECVD phosphorus rich silicon dioxide on InP, and dry thermal silicon dioxide on Si.

The final processing step for all 4 samples was to deposit a gate metal to form capacitors. In all cases, Al dots 0.2 cm in diameter and 1000 A thick were electron-beam deposited onto the insulator using a dot shadow mask. This gate metal thickness was chosen as thin as possible so as to not appreciably reduce the incident electron-beam energy while thick enough to support the use of two probes for electrical measurements.

EXPERIMENTAL PROCEDURE

The first step was to place the sample on the stage of a scanning electron microscope and lower two stainless steel probes onto the edge of an Al gate dot. These probes were left in place on the dot during irradiations. The frontside of the Al dot was grounded by these two probes and the backside ohmic contact was also grounded to the substrate stage by two other probes in order to prevent charging of the device during irradiation. The chamber door was then closed and it remained closed for all of the irradiations and C-V measurements for that particular capacitor.

A set of 5 to 10 high frequency (1 MHz) C-V measurements were taken prior to irradiation using the four probe measurement system. The exposures were made by raster scanning of the electron beam over an area larger than the Al dot for a desired dose (C/cm^2) and beam energy (keV). The irradiation was followed by another set of 5 to 10 C-V measurements. This sequence was continued for total exposures of 10^{-7} , 10^{-6} , 10^{-5} , 10^{-4} and 10^{-3} C/cm^2 with a constant beam energy. This procedure was repeated for beam energies of 5, 10, 20, 30 and 40 keV, using a new Al dot for each energy.

Both PECVD phosphorus rich silicon nitride samples were H_2/N_2 annealed after the irradiations were performed. The anneal was done at 400 C for 15 min with 2000 sccm of N_2 and 1000 sccm of H_2 flowing. A final set of C-V measurements was taken following the H_2/N_2 anneal.

RESULTS AND DISCUSSION

The electron beam irradiation of the unannealed silicon nitride MIS capacitors seemed to cause damage to the silicon nitride-InP interface. This is evident in Figure 1 which shows the C-V curves before and after irradiations at 20 keV. In this figure and in the C-V curves to follow, each C-V curve represents a typical curve obtained from the set of C-V measurements, having the V_{th} and space charge voltage ($A*Q_b/C_{ox}$) values near the average values for the set of measurements. Curve #1 is the initial C-V measurement, while curve #2 and #3 were taken after total exposures of 1.0×10^{-5} and 1.0×10^{-3} C/cm² respectively. The initial C-V curve shows a stretching out effect both at the accumulation and inversion regions. This stretching effect seems to increase dramatically with increasing exposure especially in the inversion region. This phenomenon can be explained by a large increase in the interface state density at the conduction and valence bands (7).

An examination of the following calculated values was obtained from the C-V measurement: V_{th} , flatband voltage (V_{fb}), threshold capacitance (C_{th}), flatband capacitance (C_{fb}), dielectric capacitance (C_{ox}) and surface potential ($A*Q_b/C_{ox}$). It was discovered that the $A*Q_b/C_{ox}$ term remained constant during each set of 5 to 10 C-V measurements, while changing for each electron-beam exposure. Therefore this space charge voltage term of the threshold voltage was used to characterize the extent of radiation damage.

In curve #4 it is evident that a 5 min H₂/N₂ anneal at 400 C

greatly reduced the stretching of the C-V curve. This implies that there was a reduction in the interface state density. There was also a dramatic decrease in the space charge voltage term from 2.01 V after the last irradiation to .28 V after the H₂/N₂ anneal. This was a shift of 1.73 V and is 1.17 V less than the original value of 1.45 V.

Similar results were found for electron-beam energies ranging from 5 to 40 keV. This trend can be seen in Figure 2 which shows the space charge voltage as a function of exposure for five different beam energies. For all of the energies, the C-V data showed a larger shift for higher exposures, with the 30 keV curve having a much larger effect to the irradiation than the others. This can be accounted for if the maximum energy loss of a high energy electron occurs at a depth comparable to the combined thickness of the Al gate metal and silicon nitride film (8).

The effects of electron-beam irradiation on the C-V characteristics of the silicon nitride films which were H₂/N₂ annealed initially are shown in Figure 3. Curve #1 is the C-V measurement taken immediately after the anneal. There was a slight improvement in the stretching compared to the initial curve (#1) in Figure 1 of the as deposited film, as well as a decrease in the space charge voltage term. However, there still was evidence of interface states. There was a very large stretching out effect with increasing exposure as seen in curves #2 and #3, irradiated at 5 keV with exposures of 1.0×10^{-4} C/cm² and 1.0×10^{-3} C/cm² respectively. This sample also showed an increase in $A \cdot Q_b / C_{ox}$ with increasing exposure. As before, curve #4 showed a large reduction in stretching after an H₂/N₂ anneal, that even surpassed curve #1 after the

initial H₂/N₂ anneal. This means that the H₂/N₂ anneal reduced the interface state density induced by the irradiation. In addition the space charge voltage which was initially .79 V was reduced from 1.31 V after the last irradiation to .44 V after the final anneal. The electron-beam exposure caused a positive shift of .52 V while the H₂/N₂ anneal caused a negative shift of .87 V, which is .35 V less than the initial value.

The irradiation performed on the phosphorus rich PECVD silicon dioxide capacitors is shown in Figure 4 for a beam energy of 20 keV. In this figure, curve #1 represents the initial C-V measurement of the as deposited silicon dioxide film. Curves #2 and #3 represent irradiations of 1.0×10^{-6} C/cm² and 1.0×10^{-3} C/cm² respectively. A strange effect occurred at the smaller exposures in curve #2. There was an almost parallel positive shift in the C-V curve. This would imply that there was negative trapped charge in the bulk of the oxide without any increase in the interface state density. However as the exposure increased in curve #3, there was a large shift in the negative direction accompanied by some stretching out of the curve in the inversion region. This implies that there was an increase in donor-like interface states near the conduction band as well as positive charge trapping or negative charge detrapping from the smaller exposures. This trend was also seen for beam energies of 5 keV and 40 keV (Figure 5), which shows $A \cdot Q_b / C_{ox}$ as a function of exposure.

Finally, irradiations were performed on thermal silicon dioxide MOS capacitors for comparison. These results are shown

in Figure 6 which shows C-V curves for a range of doses at 20 keV. The initial C-V measurement is curve #1 and the C-V measurements after irradiations at exposures of 1.0×10^{-6} C/cm² and 1.0×10^{-3} C/cm² are represented by curves #2 and #3 respectively. There was an increasing negative parallel shift in the C-V curves with increasing exposure. This could have been due to a build up of positive trapped charge in the oxide bulk from the irradiation. There did not seem to be any stretching, therefore the interface state density in this sample was insignificant. Similarly, the space charge voltage was not effected by irradiation at any energy as shown in Figure 7. However, there was a very large shift in V_{th} due to irradiation as shown in Figure 8, which is valid due to the absence of interface states. This shift is on the order of 8.0 V.

CONCLUSION

Electron-beam irradiation effects were investigated on phosphorus rich PECVD silicon nitride and phosphorus rich PECVD silicon dioxide on InP as well as thermal silicon dioxide on Si capacitors. From these experiments several conclusions were drawn. First of all, the electron-beam irradiation had an effect on the phosphorus rich silicon nitride capacitors, however the damage was successfully annealed and in fact, improved the device characteristics. The least radiation damage was found in the phosphorus rich silicon dioxide on InP capacitors as shown in Figures 4 and 5. While the most radiation damage was caused in the thermal silicon dioxide MOS capacitors fabricated on Si.

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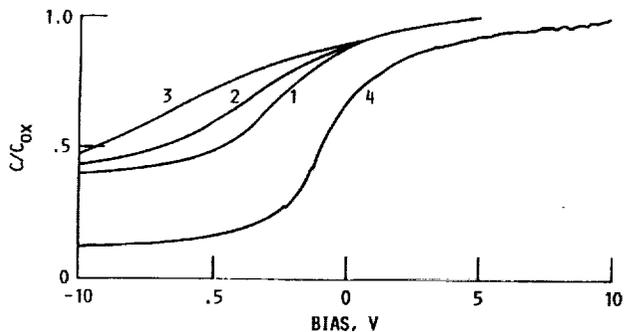


FIGURE 1. - C-V CHARACTERISTICS OF THE UNANNEALED PECVD PHOSPHORUS RICH INTERFACE SILICON NITRIDE ON InP SAMPLE. CURVE NO. 1 IS THE AS DEPOSITED INITIAL MEASUREMENT, WHILE CURVES NO. 2 AND NO. 3 WERE TAKEN AFTER DOSES OF $1.0 \times 10^{-5} \text{ C/cm}^2$ AND $1.0 \times 10^{-3} \text{ C/cm}^2$ RESPECTIVELY. CURVE NO. 4 WAS TAKEN FOLLOWING A H_2/N_2 ANNEAL AT 400 C FOR 15 MIN.

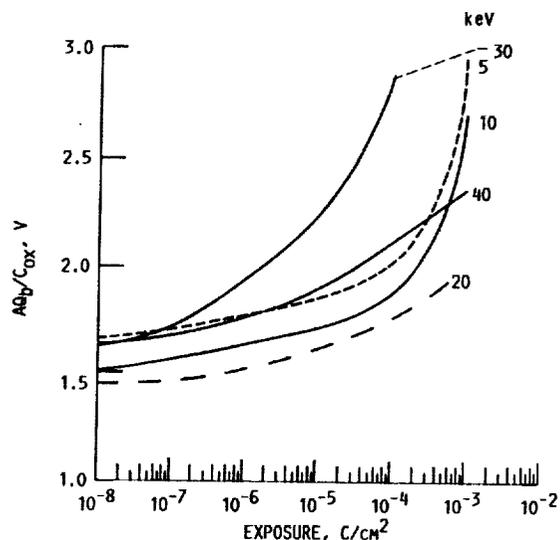


FIGURE 2. - SPACE CHARGE VOLTAGE VERSUS EXPOSURE FOR A RANGE OF ELECTRON BEAM ENERGIES OF THE PECVD PHOSPHORUS RICH INTERFACE SILICON NITRIDE ON InP SAMPLE.

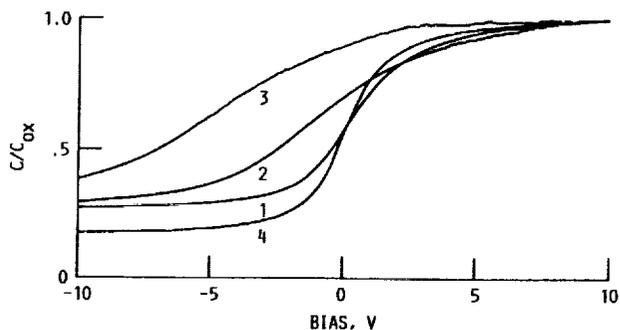


FIGURE 3. - C-V CHARACTERISTICS OF THE H_2/N_2 ANNEALED PECVD PHOSPHORUS RICH INTERFACE SILICON NITRIDE ON InP SAMPLE. CURVE NO. 1 WAS TAKEN AFTER THE INITIAL H_2/N_2 ANNEAL AT 400 C FOR 15 MIN, WHILE CURVES NO. 2 AND NO. 3 WERE TAKEN AFTER DOSES OF $1.0 \times 10^{-4} \text{ C/cm}^2$ AND $1.0 \times 10^{-3} \text{ C/cm}^2$ RESPECTIVELY. CURVE NO. 4 WAS TAKEN FOLLOWING THE SECOND H_2/N_2 ANNEAL AT 400 C FOR 15 MIN AFTER THE IRRADIATIONS.

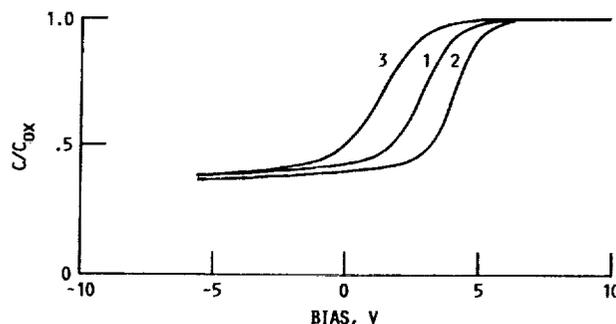


FIGURE 4. - C-V CHARACTERISTICS OF THE UNANNEALED PECVD PHOSPHORUS RICH INTERFACE SILICON DIOXIDE ON InP SAMPLE. CURVE NO. 1 IS THE AS DEPOSITED INITIAL MEASUREMENT, WHILE CURVES NO. 2 AND NO. 3 WERE TAKEN AFTER DOSES OF $1.0 \times 10^{-6} \text{ C/cm}^2$ AND $1.0 \times 10^{-3} \text{ C/cm}^2$ RESPECTIVELY.

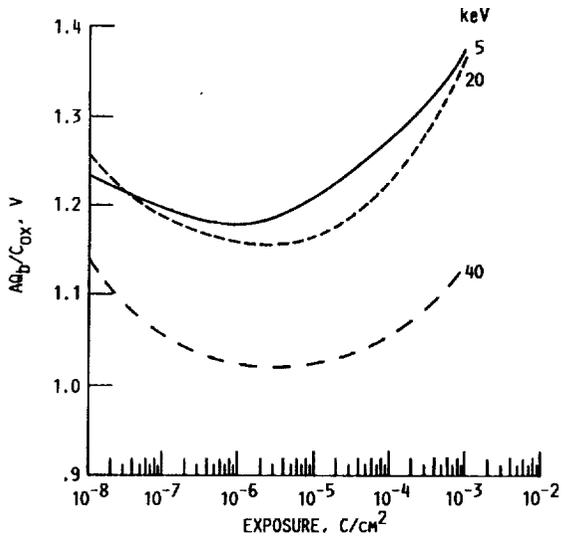


FIGURE 5. - SPACE CHARGE VOLTAGE VERSUS EXPOSURE FOR A RANGE OF ELECTRON BEAM ENERGIES OF THE PECVD PHOSPHORUS RICH INTERFACE SILICON DIOXIDE ON InP SAMPLE.

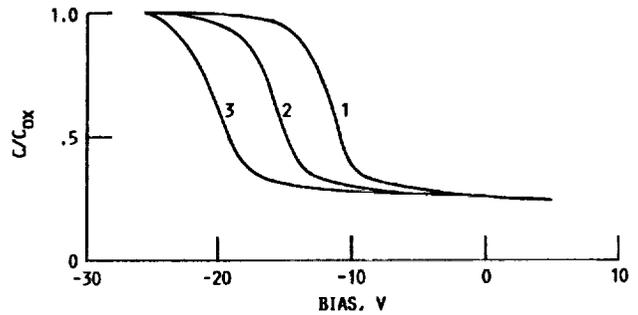


FIGURE 6. - C-V CHARACTERISTICS OF THE THERMALLY GROWN SILICON DIOXIDE ON SI SAMPLE. CURVE NO. 1 IS THE AS GROWN INITIAL MEASUREMENT, WHILE CURVES NO. 2 AND NO. 3 WERE TAKEN AFTER DOSES OF $1.0 \times 10^{-6} C/cm^2$ AND $1.0 \times 10^{-3} C/cm^2$ RESPECTIVELY.

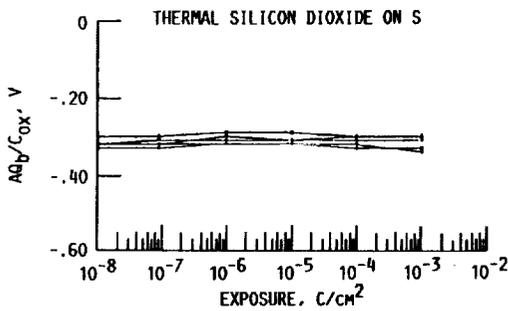


FIGURE 7. - SPACE CHARGE VOLTAGE VERSUS EXPOSURE FOR A RANGE OF ELECTRON BEAM ENERGIES OF THE THERMALLY GROWN SILICON DIOXIDE ON SI SAMPLE.

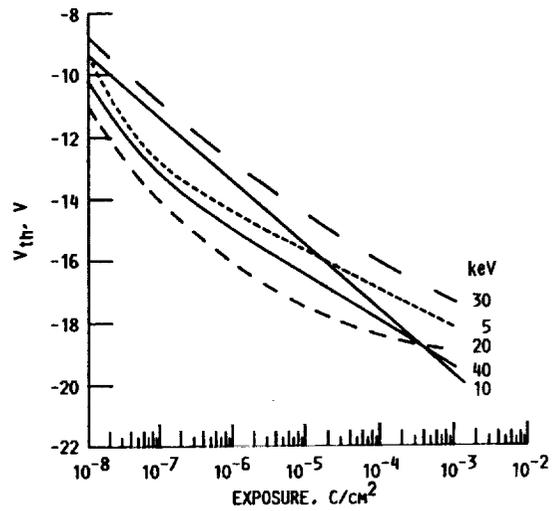


FIGURE 8. - THRESHOLD VOLTAGE VERSUS EXPOSURE FOR A RANGE OF ELECTRON BEAM ENERGIES OF THE THERMALLY GROWN SILICON DIOXIDE ON SI SAMPLE.

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