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Well-Passivated a-Si:H Back Contacts for Double-Heterojunction Silicon Solar Cells

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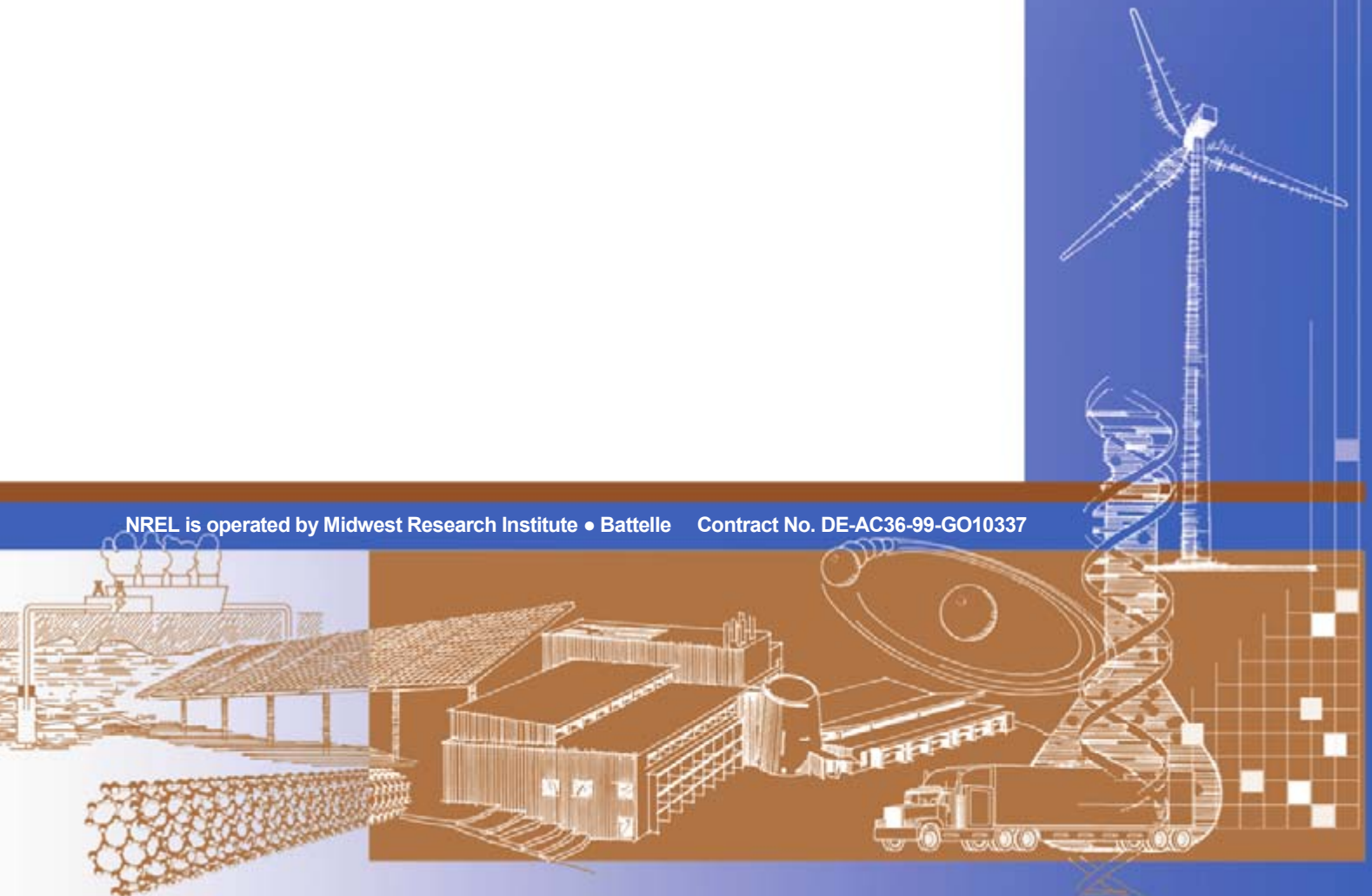

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WELL PASSIVATED a-Si:H BACK CONTACTS FOR DOUBLE-HETEROJUNCTION SILICON SOLAR CELLS*

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ABSTRACT

We have developed hydrogenated amorphous silicon (a-Si:H) back contacts to both p- and n-type silicon wafers, and employed them in double-heterojunction solar cells. These contacts are deposited entirely at low temperature (<250°C) and replace the standard diffused or alloyed back-surface-field contacts used in single-heterojunction (front-emitter only) cells. High-quality back contacts require excellent surface passivation, indicated by a low surface recombination velocity of minority-carriers (S) or a high open-circuit voltage (V_{oc}). The back contact must also provide good conduction for majority carriers to the external circuit, as indicated by a high light I-V fill factor. We use hot-wire chemical vapor deposition (HWCVD) to grow a-Si:H layers for both the front emitters and back contacts. Our improved a-Si:H back contacts contribute to our recent achievement of a confirmed 18.2% efficiency in double-heterojunction silicon solar cells on p-type textured silicon wafers [1].

INTRODUCTION

When applied to the full area of a crystalline silicon (c-Si) wafer, thin hydrogenated amorphous silicon (a-Si:H) layers have an excellent passivation capability and enable good carrier transport. These layers can serve as both the front emitter and back-surface-field (BSF) contact, as demonstrated in high-efficiency silicon heterojunction (SHJ) solar cells such as Sanyo's 21.5% double-heterojunction "HIT" solar cells [2]. The unique combination of passivation and current conduction of a-Si:H on c-Si offers many possibilities for high-efficiency device structures processed at temperatures below 250°C. Optimization of the i/n a-Si:H front emitter allowed us to achieve 17.1%-efficient single-heterojunction solar cells on p-type silicon wafers with a screen-printed Al-BSF [1]. However, an Al-BSF introduces a back-surface-recombination velocity on the order of 10^3 cm/s which limits further improvements in device performance. The Al-BSF leads to a high back-surface dark saturation current component that limits the open-circuit voltage. Further, an Al-BSF has to be processed at temperatures above 800°C, and this may cause severe bowing of the thin (~200 μm) wafers now being introduced. Such bowing contributes to problems in wafer-handling and module assembly in manufacturing.

Here, we report on the development of deposited a-Si:H back contacts for both p- and n-type silicon wafers. For both doping types, we obtain higher V_{oc} than with standard Al-alloyed or phosphorus-diffused (P-diffused) BSF contacts. Any dark-current path through inadequately passivated interface states reduces both the V_{oc} and the collection of photogenerated charge carriers. Therefore, high V_{oc} is the key to high-performance solar cells: V_{oc} and S indicate the effectiveness of an a-Si:H/c-Si heterointerface. We first demonstrated excellent surface passivation using HWCVD a-Si:H thin layers at the back-surface to achieve a very low S of 15 cm/s. This advance enabled us to obtain a high V_{oc} of 676 mV on textured p-type silicon wafers in a double-heterojunction structure with a front n/i a-Si:H emitter and back i/p a-Si:H contact. On textured n-type wafers, we obtained an even better V_{oc} of 686 mV, employing an a-Si:H (p/i) front emitter and a-Si:H (i/n) back contact. In comparison, an Al-BSF on a p-type silicon wafer and a P-diffused BSF on an n-type silicon wafer yielded far lower V_{oc}'s of 652 mV and 630 mV, respectively. These results indicate that a-Si:H back contacts passivate the back surface much better than the standard Al-alloyed or P-diffused BSF contacts. With a pure a-Si:H full-area back contact to a p-type wafer, we obtain a good fill factor of 78%, indicating excellent hole conduction across the back c-Si(p)/a-Si:H(i/p) interface.

EXPERIMENTAL

We use commercially available (100) float-zone (FZ) c-Si wafers for our SHJ device development and optimization because they have the highest bulk carrier lifetimes. The absence of significant boron-oxygen pair metastability in the FZ p-type B-doped wafers is also significant. We use HWCVD, rather than plasma-enhanced CVD, to grow the a-Si:H layers for both the front emitters and back contacts, because there is no possibility of plasma damage deleterious to the high-quality c-Si wafers we use. For all devices, including single- and double-sided planar SHJ and those on wafers textured in-house or by collaborators, we employed identical cleaning procedures, discussed in detail below.

For SHJ devices, the junctions are formed at the a-Si:H/c-Si interfaces, so it is critical to have a clean interface just prior to a-Si:H deposition. The goal is to avoid introducing defects and impurities at the interface that would cause junction recombination and hurt surface passivation. We employ a cleaning procedure that begins with a degreasing step using commonly available laboratory chemicals, with ultrasonic agitation for particle removal. Thorough rinsing and stripping of organic residues is essential, so we use modified RCA cleaning steps for final organic and metallic contaminant removal. We have found that the chemically grown oxide works well as a capping layer for the sensitive c-Si interfaces. The stable cap is stripped using a 2.5% hydrofluoric acid flush immediately before loading in our HWCVD vacuum deposition system maintained at 10^{-8} torr.

Double-sided texturing of c-Si substrates to reduce reflection losses using standard alkaline texturing solutions and practices yields pyramidal features on the order of 5 μm. The sharp tips of the pyramid peaks and deep valleys at the pyramid bases present challenges during deposition of thin a-Si:H layers. Our HWCVD layers provide excellent conformal coverage of a textured substrate with very little evidence of shunting at the tips. Cleanliness and surface passivation are all the more important on the increased surface area of the textured surface. Because of the excellent surface passivation of a-Si:H, one can use bifacially textured c-Si and reflective backing for improved light trapping in thin silicon wafers.

Our HWCVD deposition systems are capable of i-, n-, and p-layer deposition in separate chambers, but only with an air break between i- and n-layer depositions. Our optimized a-Si:H layer deposition conditions are summarized in Table 1.

Table 1. Summary of optimized a-Si:H deposition conditions for SHJ solar cell devices.

LAYER	THICKNESS (nm)	T (°C)	DEPOSITION RATE (Å/s)	GAS
i	~ 5	<150	3 - 12	SiH_4
n	~ 5	~200	~ 3	PH_3 SiH_4 H_2
p	5 - 6	~200	3	B_2H_6 SiH_4 H_2

Thermally evaporated indium tin oxide (ITO), deposited at below 200°C, with a thickness of 60-80 nm, is used for the transparent top contact to a-Si:H emitter and as the single-layer antireflection coating. Our full-area back contact and the shadow-mask-defined front contacts are deposited using electron-beam evaporation of Al or Ti/Pd/Ag metal stacks at room temperature. We have used a number of isolation techniques to form the 1-cm^2 solar cell area including photolithography, a dicing saw, and physically masked argon ion milling.

An important diagnostic used in our solar cell device development process is the measurement of effective minority-carrier lifetime using a Sinton lifetime tester. Lifetime is a sensitive measure that probes both the bulk lifetime and surface passivation of a c-Si wafer. We measure the interface quality of our devices prior to ITO contact deposition so we can avoid wasting effort and materials applying ITO to bad devices. With high bulk-lifetime FZ-Si wafers, we can estimate surface recombination velocities and the implied device V_{oc}. For rapid feedback on device quality, we also measure the V_{oc} of 0.05-cm^2 ITO dots at the edges of the full device region, as defined by shadow-masked ITO deposition. High-resolution transmission electron microscopy (HRTEM) was helpful for optimizing the SHJ interface; we used it to determine whether the initial HWCVD-deposited layers were a-Si:H, microcrystalline silicon (μc-Si:H), or epitaxial c-Si. HRTEM micrographs were made in the ITO dot region and correlated to I-V measurements on fully isolated 1-cm^2 solar cell devices measured on an AM1.5 calibrated XT-10 solar simulator.

RESULTS AND DISCUSSIONS

Surface preparation

As we have improved our SHJ solar devices, we have developed increasingly stringent cleaning procedures, usually involving an increasing number of cleaning steps. This has certainly contributed to our rapid improvement in V_{oc}. The cleaning procedures all consist of a sequence of organic solvent-degreasing and particle-removal steps, followed by more rigorous cleaning. We next describe the various generations of these cleaning procedures, as summarized in Table 2. Generation One (GEN-1) was a boiling 18-MΩ·cm high-purity deionized (DI) water rinse, followed by a long DI water rinse and a 0.5% hydrofluoric acid (HF) dip until the surface became hydrophobic due to oxide removal. GEN-1 cleaning provided a stable, hydrogen-terminated surface that allowed us to reach a maximum V_{oc} of 630 mV. Our subsequent improvements to the cleaning procedure added more chemical modification of the surface, such as oxidation followed by HF stripping and more aggressive acid cleaning solutions. With GEN-2, V_{oc} increased to 680 mV as we added an

Table 2. Summary of 4 generations of cleaning processes and the maximum V_{oc} (mV) for planar n-type FZ devices.

GEN	V_{oc}	CLEANING SUMMARY
1	630	Solvent Degrease High-Purity DI Water Rinse at Boiling Long DI Water Rinse at RT, Dilute HF Etch
2	680	Solvent Degrease Aggressive Acid Cleaning Short High-Purity DI Rinse RT, Dilute HF Etch Chemical Oxidation, Long DI Rinse
3	690	Solvent Degrease Repeated Aggressive Acid Cleaning, DI Rinse Dilute HF, Chemical Oxidation, Long DI Rinse
4	710	Solvent/Acid Degrease High-Purity DI Water Rinse, Dilute HF Repeated Aggressive Acid Cleaning, DI Rinse Dilute HF, High-Purity Chemical Oxidation, DI

aggressive acid cleaning combined with chemical oxidation of the surface to trap surface impurities and subsequent removal by flushing in dilute HF. With GEN-3 cleaning, V_{oc} increased to 690 mV when we repeated the aggressive acid cleaning of GEN-2 in alternation with a long DI water rinse. In GEN-4, which led to V_{oc} of 710 mV, the greatest improvement was due to control of contamination from the organic degreasing step that had occasionally resulted in haze at the wafer surface. We also increased the purity of chemicals we used for the final chemical oxidation step.

a-Si:H for better passivation instead of c- or μc-Si:H

We optimized thin HWCVD a-Si:H surface passivation layers to achieve a low S of 15 cm/s. It is critical to avoid formation of epitaxial c-Si or μc-Si:H. This is achieved by limiting the initial undoped a-Si:H layer deposition temperature to 150°C or less. As seen in Fig. 1, the effective minority-carrier lifetime rises and the surface recombination velocity falls as the deposition temperature is reduced from 230° to 100°C. We have shown earlier [3] that for deposition temperatures above 150°C for (100) wafers or 200°C for (111) wafers, epitaxy can occur and this reduces V_{oc}. On a textured p-type wafer having an Al-BSF back contact, we attain a respectable V_{oc} value of 652 mV.

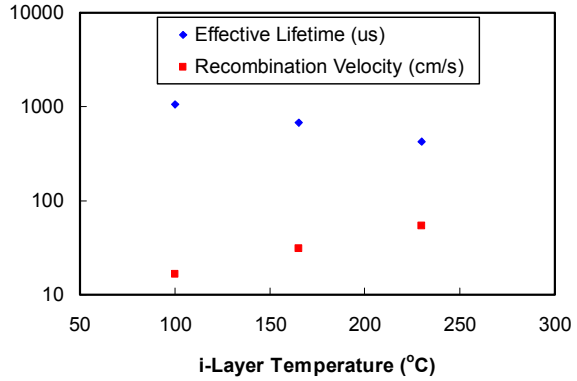

Fig. 1. The i-layer temperature effect on passivation.

a-Si:H back contacts instead of μc-Si:H

We obtained a high V_{oc} of 676 mV on textured p-type FZ c-Si wafers in the double-heterojunction structure (front n/i SHJ emitter and back i/p SHJ contact). On textured n-type wafers, we employed an a-Si:H (p/i) front emitter and an a-Si:H (i/n) back contact to reach 686 mV. These results indicate that both back- and front-surface passivation are excellent (see Table 3). For comparison, replacing the SHJ back contact on a p-type c-Si wafer with an Al-BSF yields a V_{oc} of only 652 mV; replacing the SHJ back contact with a P-diffused BSF on an n-type c-Si wafer yields a V_{oc} of only 630 mV, as shown in Table 3. Although traditional alloyed/diffused BSF contacts have excellent contact-resistance characteristics, a-Si:H back contacts are superior for their combined passivation and current-transport capabilities.

Table 3. Effects of different back contacts on V_{oc} (mV). The a-Si:H back contacts have i/p doping on p-type wafers and i/n doping on n-type wafers.

FRONT / c-Si \ BACK	Al-BSF	a-Si	P-Diffused
a-Si(n/i) / Textured p-FZ	650	680	-
a-Si(p/i) / Textured n-FZ	-	690	-
a-Si(p/i) / Planar n-FZ	-	710	630

Fill factor is another important measure of back-contact performance. When using dielectric back-surface passivation with insulating materials, one must employ local contact windows [4] to obtain low resistance and effective majority-carrier collection. Conversely, with simpler full-area back contacts of a-Si:H, it is possible to obtain excellent hole conduction across the back c-Si(p)/a-Si:H(i/p) interface; we obtain a good fill factor of 78%. On n-type wafers, Sanyo's excellent HIT cell results showed that they have solved the electron transport across the c-Si(n)/a-Si:H(i/n) back contact; we also found the heterojunction contact to n-type wafers straightforward to make. Other groups have required a μc-Si:H p-layer for good back contact to c-Si(p) [5]. In contrast, we make an a-Si:H (i/p) back contact to c-Si(p), as shown clearly in HRTEM (Fig. 2). Typical I-V curves of our double-

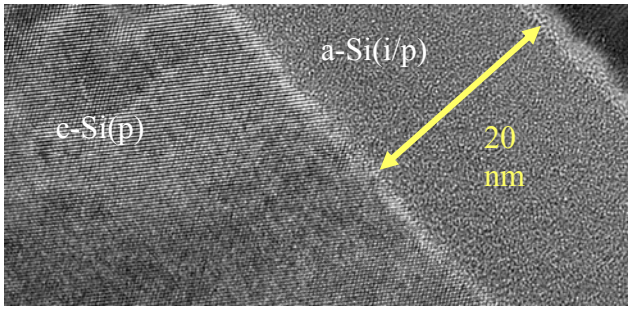

Fig. 2. High-resolution TEM of abrupt c-Si(p)/a-Si:H(i/p).

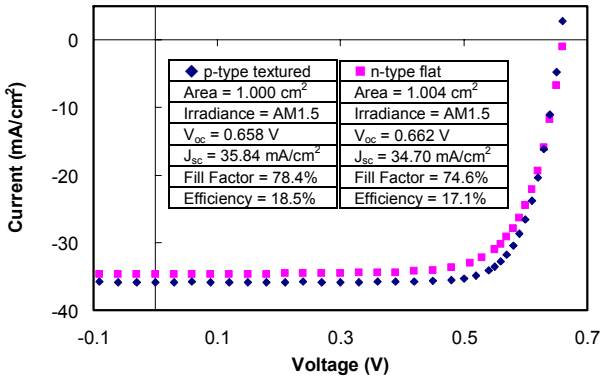

Fig. 3. Good fill factors for double-heterojunction c-Si solar cells based on both p-type (◆) and n-type (■) wafers.

heterojunction solar cells for both p- and n-types are shown in Fig. 3, indicating that good fill factors are achievable with entirely a-Si:H back-contact layers.

Back-surface reflection

In addition to good passivation, the back contact must provide good back-surface optical reflection. External quantum efficiency (EQE) measurements in Fig. 4 demonstrate that a back contact of a-Si:H(i/n)/ITO with a Ti/Pd/Ag stack of metal is better than a-Si:H(i/n)/ITO with Al. The long-wavelength photons get reflected back into the wafer more effectively, improving the near-infrared spectral response. Figure 4 also shows that simply replacing the a-Si:H(i/n)/ITO with a P-diffused n^+ BSF made the red spectral response worse, likely because the back surface is inadequately passivated. Similarly, inferior back-surface passivation by an Al-BSF compared to a-Si:H(i/p) on a p-type wafer is evident from the EQE measurements in Fig. 5. A transparent ITO layer between the a-Si:H(i/p) and Al metal does not appear to be essential. Figure 6 compares the internal QE (IQE) of two different back contacts, thereby removing the effect of the reflected light from the identically textured front surfaces. Enhanced long-wavelength response with the a-Si:H(i/p)/Al back contact is evident.

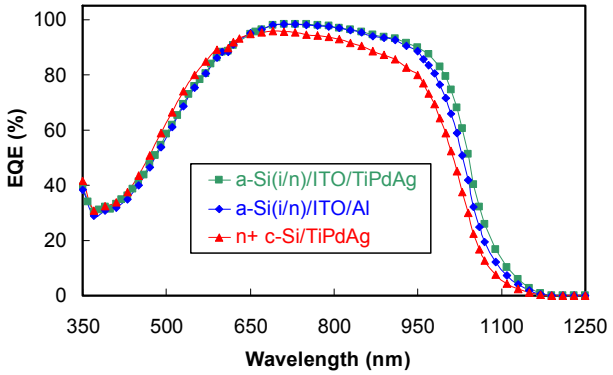

Fig. 4. EQE comparisons. The red response of n-type FZ solar cell is enhanced by better back-surface passivation of a-Si:H(i/n) and by higher back-surface reflection of Ti/Pd/Ag than Al.

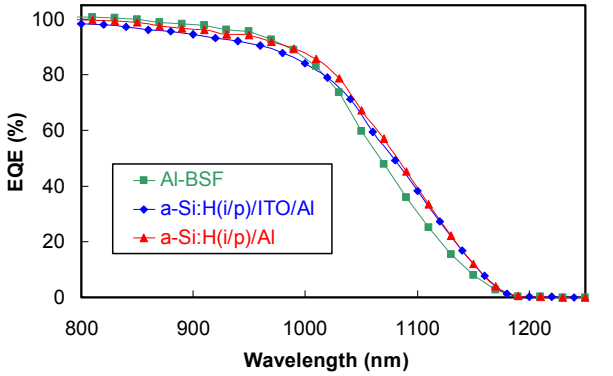

Fig. 5. Enhanced red response by a-Si:H(i/p) compared to Al-BSF for p-type silicon wafers.

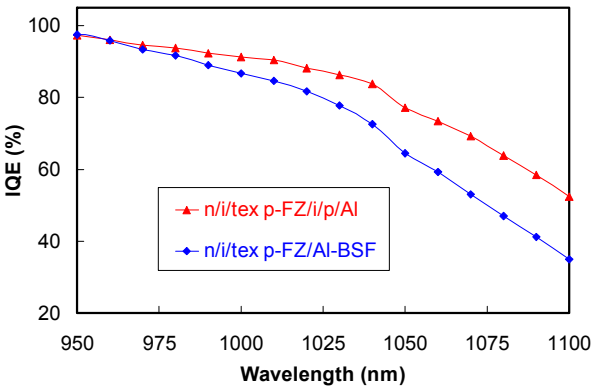

Fig. 6 Significant enhancement in IQE by front ITO/texture coupled with an effective a-Si:H(i/p)/Al back reflector, as compared to a simple Al-BSF.

CONCLUSIONS

We successfully replaced the conventional high-temperature Al-BSF or P-diffused BSF in double-heterojunction solar cells. These cells employ HWCVD a-Si:H front emitters and HWCVD a-Si:H back contacts on both p- and n-type silicon wafers. A full metal layer directly on an a-Si:H(i/p) back contact significantly enhances back-surface reflection. The a-Si:H(i/p)/Al back contact has enabled us to achieve fill factors exceeding 78% and conversion efficiencies of 18.2% on textured p-type FZ silicon wafers.

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