NASA Technical Memorandum

NASA TM-86581

INTERFACE CIRCUITRY FOR SUPERCONDUCTING BOLOMETER

By P. J. Nelson

Space Science Laboratory
Science and Engineering Directorate

January 1987

National Aeronautics and Space Administration

George C. Marshall Space Flight Center

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

TECHNICAL MEMORANDUM

INTERFACE CIRCUITRY FOR SUPERCONDUCTING BOLOMETER

INTRODUCTION

The circuitry to be described evolved from a requirement to demonstrate feasibility of a new concept for reading out images from an array of bolometers. This concept, proposed by Palmer N. Peters and being co-investigated by Robert C. Sisk, is the basis for a Marshall Space Flight Center Director's Discretionary Fund, entitled "Superconducting Sensors for IR Astronomy Applications." One embodiment of the circuitry required has been finalized by this author as a project for the Marshall Space Flight Center's Professional Intern Program.

The interface circuitry described in this report is used to link a computer with the superconducting bolometer array. Rows of resistive lines and columns of superconducting lines are utilized for this array. When a current is passed through a resistive line, it produces heating, thus causing a transition to normal conduction on the corresponding superconductors.

When a radiation pattern is imaged on the array, a temperature pattern unique to that radiation pattern is obtained. The length of time that the heating must be applied before the superconductor switches to a normal conductor is inversely proportional to the intensity of the infrared image projected on that element. The interface circuitry is designed to accommodate a 16x16 array. The main purpose of this circuitry is to show the feasibility of the array. Further applications will be on a much larger array than the initial 16x16 array.

CONFIGURATION

The circuitry, whose primary components were suggested by Robert W. Austin and Palmer N. Peters, was designed primarily in four stages. The first two stages of the interface circuitry consist of amplifiers. The first stage amplifies the input signal by a factor of 140 and the second stage amplifies by 10, thereby providing a total amplification of 1400. Two OP27 OP-AMPS provide this gain (Figure 1).

The next stage consists of a LM311 comparator that compares the voltage it sees with a predetermined reference voltage whose level can be adjusted (Figure 2). The output of the comparator goes high (+5V) when the input signal, after being amplified 1400

times, is higher than the reference voltage. The comparator's output is negative logic ANDed with a gating signal provided from the computer. This enables control of the last stage in the circuit, an MM74HC590 eight-bit binary counter. When the output of the comparator goes high, the counter stops counting. The count from the counter is then stored in the computer (Figure 3). Since the count corresponds to the image from the array, the computer can then compile the counts of all 16 counters to reproduce one line of the image on the computer.

There were several specifications to be considered when designing the interface circuitry. One of the primary factors to be considered was the signal level necessary to trigger the interface circuitry. With the appropriate adjustment of the potentiometer, the circuitry will trigger on a signal level as low as 30 μV. Since this is amplified 1400 times, the comparator sees 42 mV. Several capacitors were added to reduce the level of noise in the circuit. Diodes were added to prevent possible damage to the chips should the power supplies be incorrectly connected. The supply voltages for this circuit are as follows:

+5 V
+12 V
-12 V

The final phase of the circuit involved etching a circuit board. A custom layout of the circuit was made, after which a circuit board was etched from the pattern of the layout (Figure 4). Holes were drilled in the circuit board and the components were soldered in place (Figure 5).

CONCLUSIONS

The main purpose of this interface circuitry is to demonstrate the feasibility of the superconducting bolometer array. The circuitry described here ties the computer to the array. Initial attempts at imaging will be performed on laboratory objects, and the characteristics of the pixels will be investigated experimentally. The present circuitry will have to be modified for astronomical or very weak signal sources to include phase-sensitive detection after chopping the signal. Both regulation at the transition temperature and fast Fourier analyses of the signal will be required for future very weak signal applications. The relative simplicity of the readout technique should permit easy scaling from the present 16x16 array to much larger arrays.

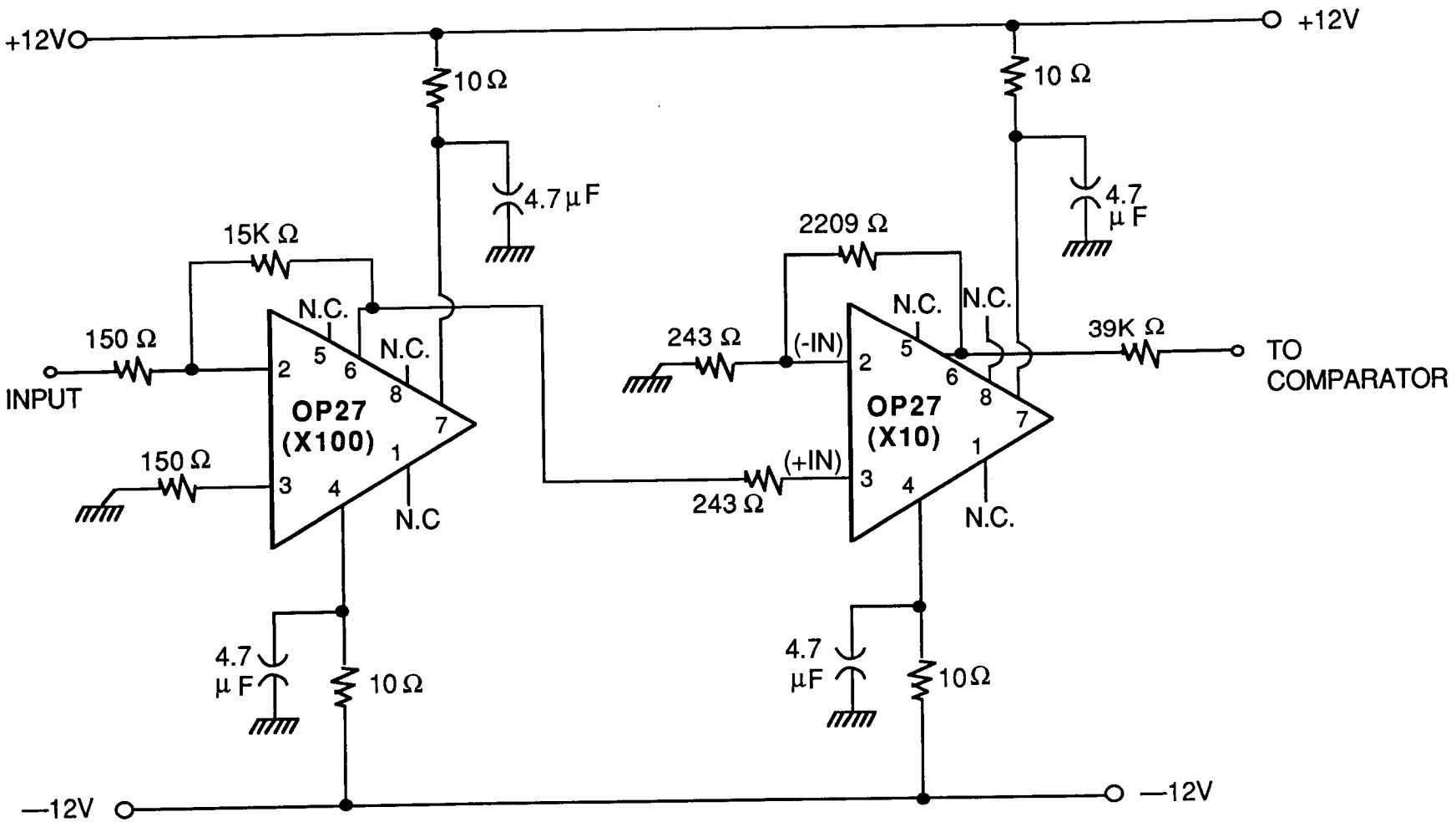

Figure 1. Operational amplifiers.

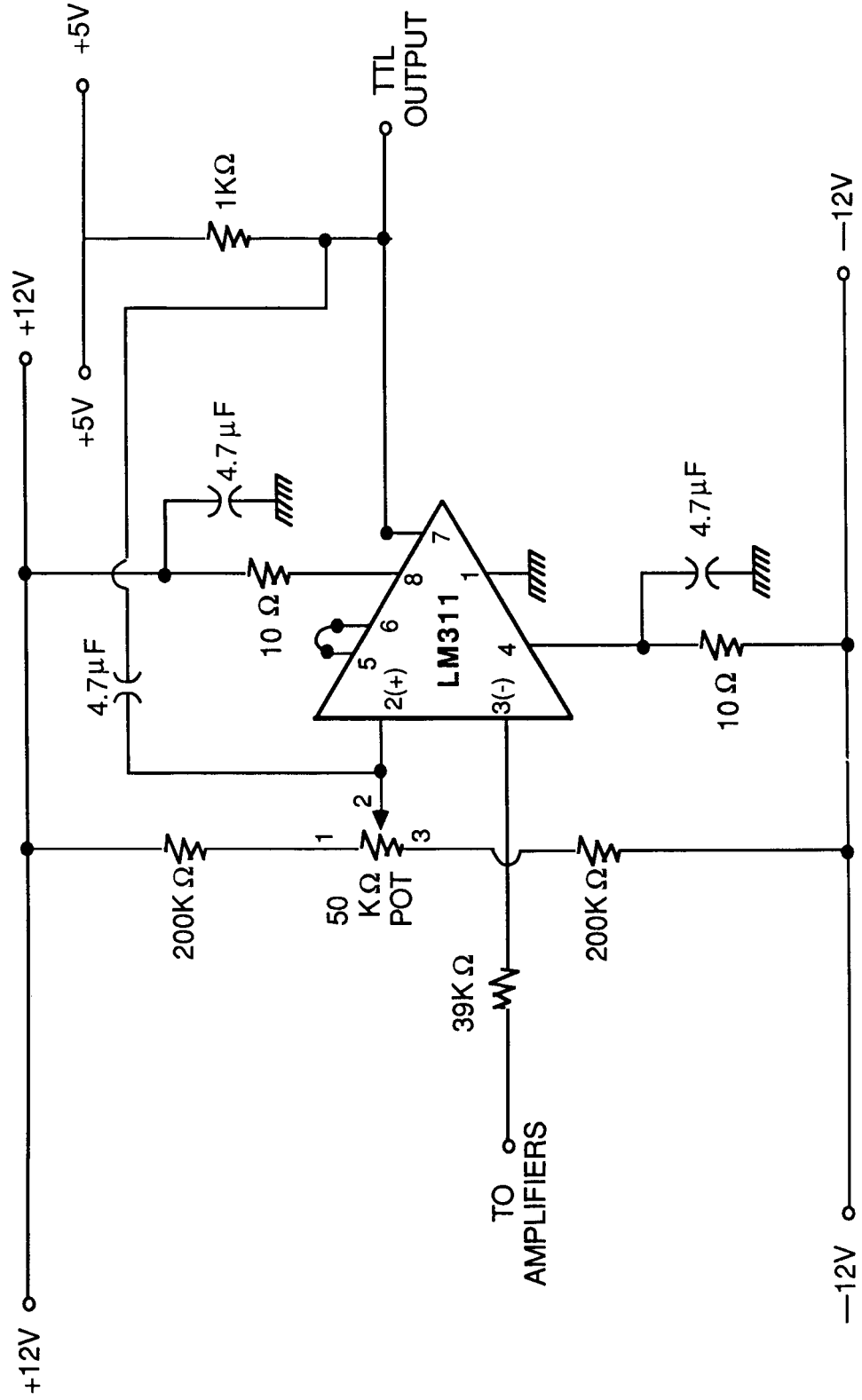

Figure 2. Comparator.

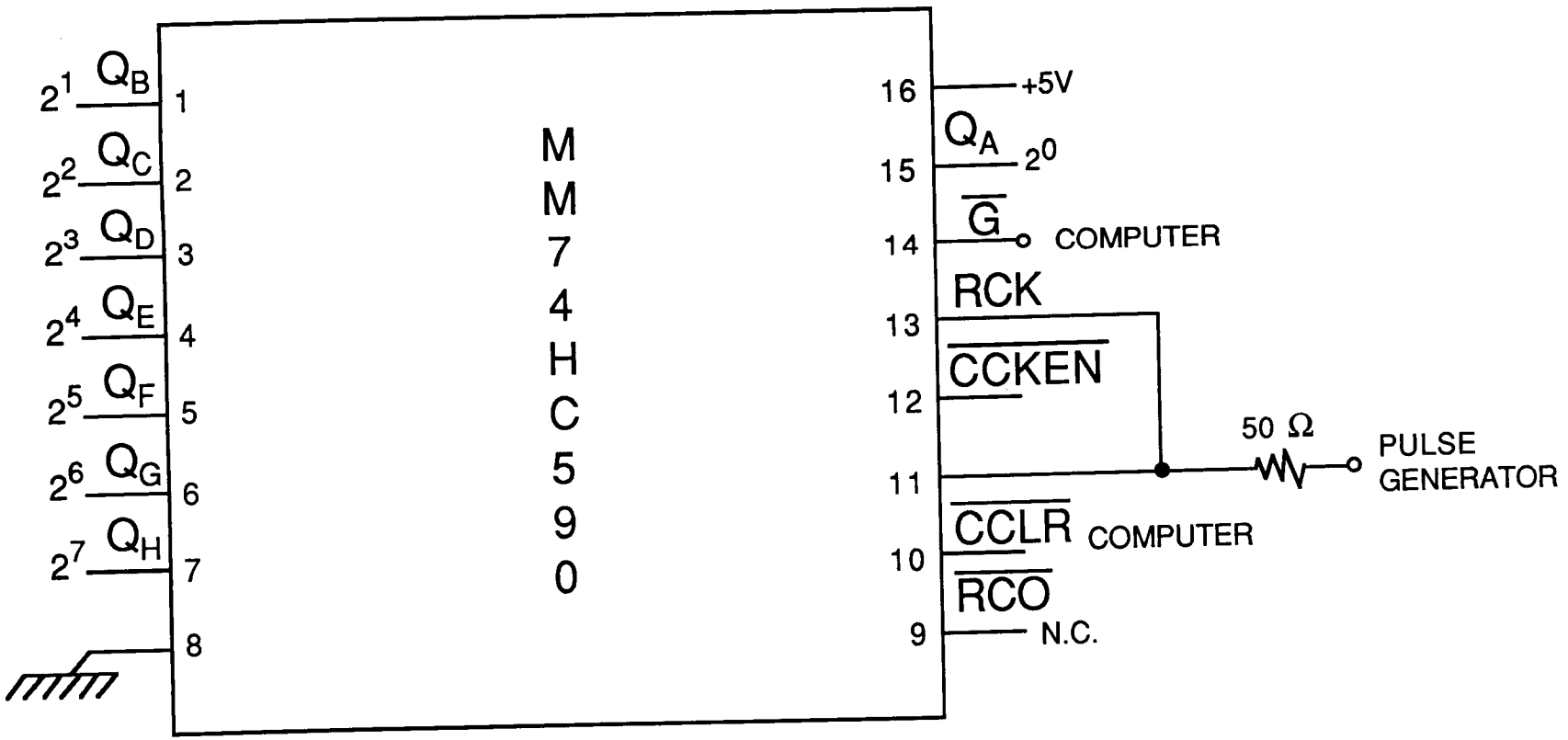

Figure 3. Counter.

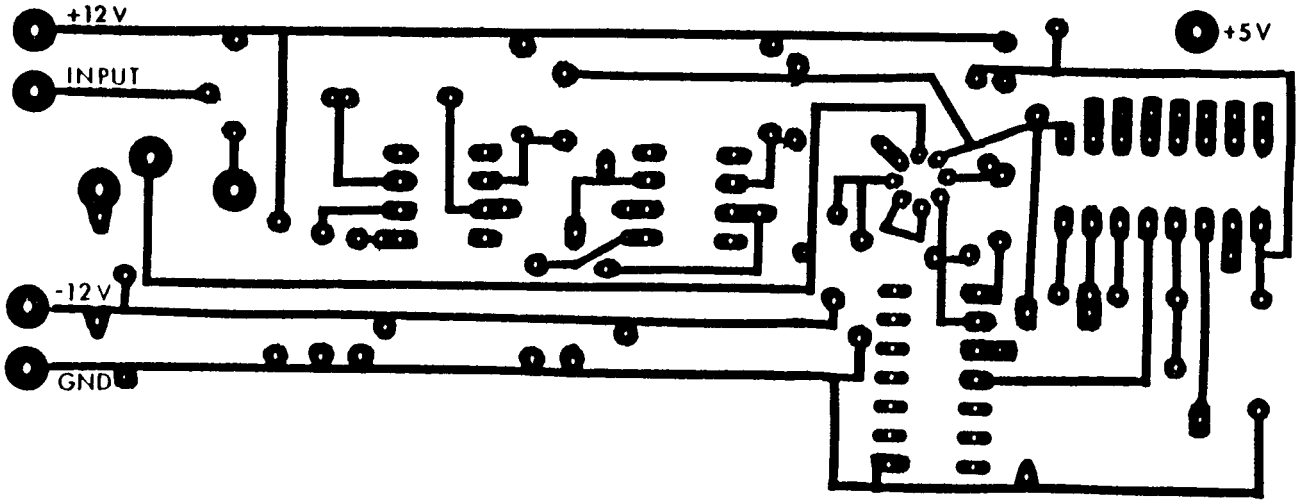

Figure 4. Circuit layout.

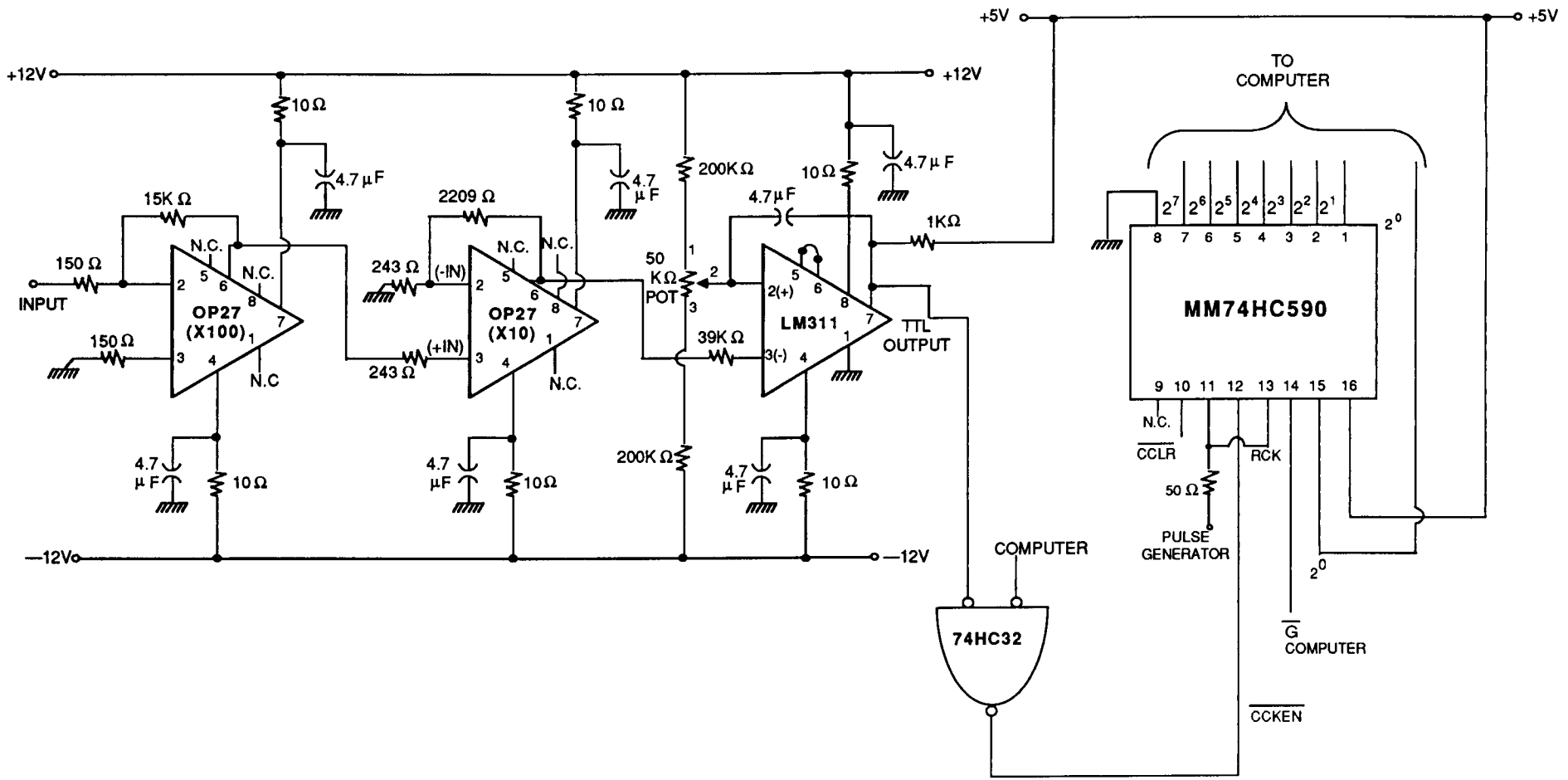

Figure 5. Complete circuit diagram.

APPROVAL

INTERFACE CIRCUITRY FOR SUPERCONDUCTING BOLOMETER

By P. J. Nelson

The information in this report has been reviewed for technical content. Review of any information concerning Department of Defense or nuclear energy activities or programs has been made by the MSFC Security Classification Officer. This report, in its entirety, has been determined to be unclassified.

E. A. Tandberg-Hanssen

E. A. TANDBERG-HANSSEN
Deputy Director, Space Science Laboratory

☆U.S. GOVERNMENT PRINTING OFFICE 1987—730-067/40065

TECHNICAL REPORT STANDARD TITLE PAGE

1. REPORT NO.	2. GOVERNMENT ACCESSION NO.	3. RECIPIENT'S CATALOG NO.
NASA TM-86581		

4. TITLE AND SUBTITLE	5. REPORT DATE
Interface Circuitry for Superconducting Bolometer	January 1987
	6. PERFORMING ORGANIZATION CODE ES62

7. AUTHOR(S)	8. PERFORMING ORGANIZATION REPORT #
P. J. Nelson*	

9. PERFORMING ORGANIZATION NAME AND ADDRESS	10. WORK UNIT NO.
George C. Marshall Space Flight Center Marshall Space Flight Center, Alabama 35812	11. CONTRACT OR GRANT NO.
	13. TYPE OF REPORT & PERIOD COVERED
12. SPONSORING AGENCY NAME AND ADDRESS National Aeronautics and Space Administration Washington, D.C. 20546	Technical Memorandum
	14. SPONSORING AGENCY CODE

15. SUPPLEMENTARY NOTES

Prepared by Space Science Laboratory, Science and Engineering Directorate.
*PIP on rotation in Space Science Laboratory from Information & Electronic Systems Laboratory.

16. ABSTRACT

The interface circuitry described in this report links the computer with the superconducting bolometer array. This helps demonstrate the feasibility of the array. Using the circuitry and the array, imaging will be made possible. Initial imaging will be done on laboratory objects, and the pixel characteristics will be investigated experimentally.

17. KEY WORDS	18. DISTRIBUTION STATEMENT
Superconducting, Interface, Bolometer, Array	Unclassified--Unlimited

19. SECURITY CLASSIF. (of this report)	20. SECURITY CLASSIF. (of this page)	21. NO. OF PAGES	22. PRICE
Unclassified	Unclassified	12	NTIS

MSFC - Form 3292 (May 1969)

For sale by National Technical Information Service, Springfield, Virginia 22151