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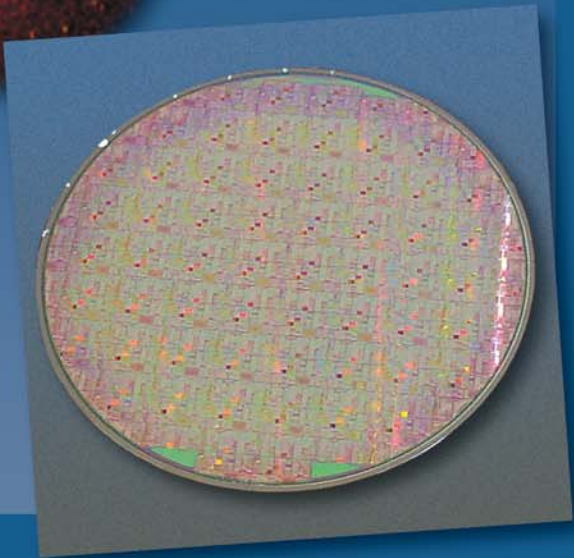
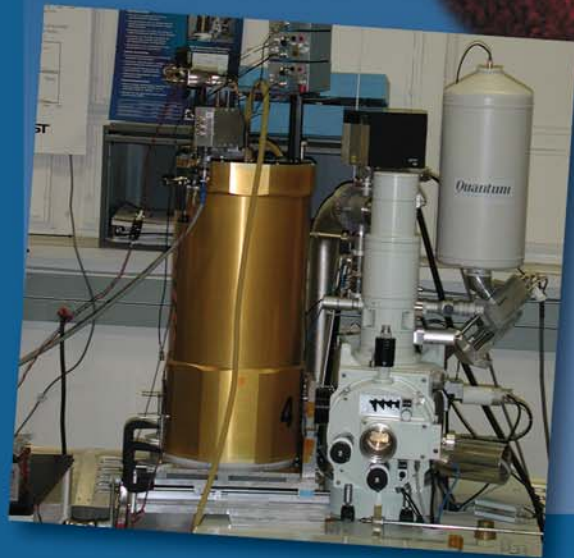
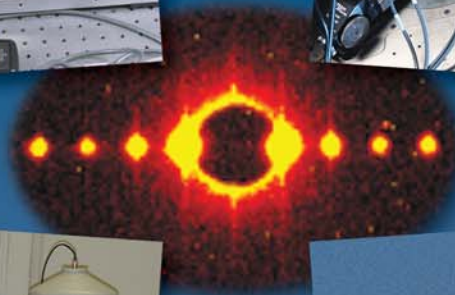
NISTIR 7171

January 2005

ELECTRONICS AND ELECTRICAL ENGINEERING LABORATORY

OFFICE OF MICROELECTRONICS PROGRAMS

PROGRAMS, ACTIVITIES, AND ACCOMPLISHMENTS



THE ELECTRONICS AND ELECTRICAL ENGINEERING LABORATORY

One of NIST's seven Measurement and Standards Laboratories, EEEL conducts research, provides measurement services, and helps set standards in support of: the fundamental electronic technologies of semiconductors, magnetics, and superconductors; information and communications technologies, such as fiber optics, photonics, microwaves, electronic displays, and electronics manufacturing supply chain collaboration; forensics and security measurement instrumentation; fundamental and practical physical standards and measurement services for electrical quantities; maintaining the quality and integrity of electrical power systems; and the development of nanoscale and microelectromechanical devices. EEEL provides support to law enforcement, corrections, and criminal justice agencies, including homeland security.

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- Semiconductor Electronics Division
- Optoelectronics Division
- Quantum Electrical Metrology Division
- Electromagnetics Division
- Office of Microelectronics Programs
- Office of Law Enforcement Standards

This document describes the technical programs of the Office of Microelectronics Programs. Similar documents describing the other Divisions and Offices are available. Contact NIST/EEEL, 100 Bureau Drive, MS 8100, Gaithersburg, MD 20899-8100, Telephone: (301) 975-2220, On the Web: www.eeel.nist.gov

Cover caption: From top picture, left to right #1 and #2; bottom left to right #3 and #4; and center is #5

- #1 – Deep Ultraviolet Twyman Green Interferometer*
- #2 – Dr. Curt Richter testing molecular electronics structures*
- #3 – Microcalorimeter high resolution energy dispersive X-ray spectrometer mounted on analytical scanning electron microscope*
- #4 – Patterned silicon wafer*
- #5 – Small angle X-ray scattering diffraction pattern from silicon nano-scale test structure.*

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U.S. DEPARTMENT OF COMMERCE

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Technology Administration

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References: References made to the *International Technology Roadmap for Semiconductors* (ITRS) apply to the most recent edition, dated 2003:

Semiconductor Industry Association. *The International Technology Roadmap for Semiconductors, 2003 edition*. International SEMATECH: Austin, TX, 2003.

This document is available on-line at URL: <http://public.itrs.net> or in printed copy by contacting International SEMATECH, 2706 Montopolis Drive, Austin, TX 78741, ITRS department 860-008, phone: (512) 356-3500.

The reader will notice that there are acronyms and abbreviations throughout this document that are not spelled out due to space limitations. We have listed the acronyms and abbreviations in an appendix at the end of this document.

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WELCOME AND INTRODUCTION

WELCOME

The microelectronics industry supplies vital components to the electronics industry and to the U.S. economy, enabling rapid improvements in productivity and in new high technology growth industries such as electronic commerce and biotechnology. The National Institute of Standards and Technology, NIST, in fulfilling its mission of strengthening the U.S. economy, works with industry to develop and apply technology, measurements and standards; and applies substantial efforts on behalf of the semiconductor industry and its infrastructure. This report describes the many projects being conducted at NIST that constitute that effort.

HISTORICAL PERSPECTIVE

NIST's predecessor, the National Bureau of Standards (NBS), began work in the mid-1950s to meet the measurement needs of the infant semiconductor industry. While this was initially focused on transistor applications in other government agencies, in the early 1960s the Bureau sought industry guidance from the American Society for Testing and Materials (ASTM) and the (U.S.) Electronic Industries Association (EIA). ASTM's top priority was the accurate measurement of silicon resistivity. NBS scientists developed a practical nondestructive method ten times more precise than previous destructive methods. The method is the basis for five industrial standards and for resistivity standard reference materials widely used to calibrate the industry's measurement instruments. The second project, recommended by a panel of EIA experts, addressed the "second breakdown" failure mechanism of transistors. The results of this project have been widely applied, including solving a problem in main engine control responsible for delaying the launch of a space shuttle.

From these beginnings, by 1980 the semiconductor metrology program had grown to employ a staff of sixty with a \$6 million budget, mostly from a variety of other government agencies. Congressional funding in that year gave NBS the internal means to maintain its semiconductor metrology work. Meeting industrial needs remained the most important guide for managing the program.

INDUSTRIAL METROLOGY NEEDS

By the late 1980s, NBS (now NIST) recognized that the semiconductor industry was applying a much wider range of science and engineering technology than the existing NIST program was designed to cover. The necessary expertise existed at NIST, but in other parts of the organization. In 1991, NIST established the Office of Microelectronics Programs (OMP) to coordinate and fund metrological research and development across the agency, and to provide the industry with easy single point access to NIST's widespread projects. Roadmaps developed by the (U.S.) Semiconductor Industry Association (SIA) have independently identified the broad technological coverage and growing industrial needs for NIST's semiconductor metrology developments. As the available funding and the scope of the activities grew, the collective name became the National Semiconductor Metrology Program (NSMP), operated by the OMP.

The NSMP has stimulated a greater interest in semiconductor metrology, motivating most of NIST's laboratories to launch additional projects of their own and to cost-share OMP-funded projects. The projects described in this book represent this broader portfolio of microelectronics projects. Most, but not all, of the projects described are partially funded by the NSMP, which provided a \$12.4 million budget in fiscal year 2003, and a \$11.9 million budget in fiscal year 2004.

FOSTERING NIST'S RELATIONSHIPS WITH THE INDUSTRY

NIST's relationships with the SIA, International SEMATECH (ISMT), and the Semiconductor Research Corporation (SRC) are also coordinated through the OMP. Staff from OMP represent NIST on the SIA committees that develop the International Technology Roadmap for Semiconductors (ITRS) as well as on numerous SRC Technical Advisory Boards. OMP staff are also active in the semiconductor standards development work of the American Society for Testing and Materials (ASTM), the National Electronics Manufacturers Initiative (NEMI), the Electronic Industries Association (EIA), the International Organization for Standardization (ISO), and Semiconductor Equipment and Materials International (SEMI).

LEARN MORE ABOUT SEMICONDUCTOR METROLOGY AT NIST

This publication provides summaries of NIST's metrology projects for the silicon semiconductor industry and their suppliers of materials and manufacturing equipment. Each project responds to one or more metrology requirements identified by the industry in sources such as the ITRS. NIST is committed to listening to the needs of industry, working with industry representatives to establish priorities, and responding where resources permit with effective measurement technology and services. For further information, please contact NIST as follows:

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LITHOGRAPHY METROLOGY PROGRAM

Advances in lithography have largely driven the spectacular productivity improvements of the integrated circuit industry, a steady quadrupling of active components per chip every three years over the past several decades. This continual scaling down of transistor dimensions has allowed more and more components on a chip, lowered the power consumption per transistor, and increased the speed of the circuitry. The shrinking of device dimensions has been accomplished by shortening the wavelength of the radiation used by the lithography exposure tools. The industry at this point has moved into the deep ultraviolet (DUV) spectrum. Currently, exposure tools operating at 193 nm are in leading edge manufacturing facilities, and exposure tools operating at 157 nm are in development. The first 193 nm immersion lithography tools will be shipped later this year. Looking beyond the deep ultraviolet, extreme ultraviolet radiation (EUV) at 13 nm is being investigated, and demonstration tools are being designed and assembled. The overall goal of this task is to support these developments in DUV and EUV. The areas of emphasis are characterization of lens materials, and immersion fluids, laser calorimetry, radiation detector sensitivity and damage, EUV lens metrology, and metrology for the development of advanced photoresist materials for both DUV and EUV.



METROLOGY SUPPORTING DEEP ULTRAVIOLET LITHOGRAPHY

GOALS

Develop solutions to key metrology issues confronting the semiconductor lithography industry. These include development of measurement methods and standards for characterizing deep ultraviolet (DUV) laser sources, detectors, and materials. One focus is on delivering high-accuracy measurements of DUV detector parameters and materials properties of immediate need by the industry. There is ongoing activity in the following areas: standards development, calibration services, characterization of optical materials, sources, and detectors, in addition to advising customers on in-house measurements.

CUSTOMER NEEDS

Increasing information technology requirements have yielded a strong demand for faster logic circuits and higher-density memory chips. This demand has led to the introduction of DUV laser-based lithographic tools for semiconductor manufacturing. These tools, which employ KrF (248 nm) and ArF (193 nm) excimer lasers, have led to an increased demand for accurate measurements at DUV laser wavelengths.

A new lithography technology, immersion lithography, depends on incorporating a high-index fluid between the optical system and the wafer. Design and development of 193nm lithography and 157nm lithography requires accurate measurements of the index properties of the potential 193nm and 157nm fluids.

To support these efforts, the National Institute of Standards and Technology (NIST), with International SEMATECH support, has initiated a DUV metrology program focusing on the characterization of DUV optical materials, sources, and detectors.

The potential solutions for lithographic systems are discussed in the 2003 International Technology Roadmap for Semiconductors on page 15 of the Lithography section, "Optical lithography is expected to be the dominant approach through the 65 nm node, with NGL (Next Generation Lithography) possibly appearing at the 45 nm node, although more likely later." The need for metrology in lithography is discussed on page 9

of the Metrology section, "As a minimum, the complex refractive index (refractive index n and extinction coefficient κ) of all layers needs to be known at the lithography wavelength. Literature data for such properties are usually not available or obsolete and not reliable" In addition, the need for metrology is discussed on page 32 of the Metrology section on Integrated Metrology and Advanced Process Control, "Metrology plays a key role in productivity gains made through advanced process control (APC), particularly as the trend toward integrated metrology—from offline to inline to in situ techniques—enables a richer, more powerful spectrum of process control strategies."

TECHNICAL STRATEGY

1. Beginning with the first edition of the National Technology Roadmap for Semiconductors (NTRS) in 1992, the semiconductor industry has made an organized, concentrated effort to reduce the feature sizes of integrated circuits. As a result, there has been a continual shift towards shorter exposure wavelengths in the optical lithography process. Because of their inherent characteristics, deep ultraviolet (DUV) lasers, specifically KrF (248 nm) and ArF (193 nm), and more recently F_2 (157 nm) excimer lasers, are the preferred sources for high-resolution lithography at this time. To meet the laser metrology needs of the optical lithography community, we have developed primary standards and associated measurement systems at 193 and 248 nm, and 157 nm. Figure 1 shows the 157 nm facility.



Figure 1. Measurement system for excimer laser power and energy calibrations at 157 nm.

Technical Contacts:

J. H. Burnett
M. Dowell

"It's an excellent service NIST has performed for the entire industry. The kind of thing NIST is there for – to identify issues before the train wreck takes place."

Mordechai Rothschild,
Massachusetts Institute
of Technology's
Lincoln Laboratory

DELIVERABLES: Proved high-quality calibration services for excimer laser power and energy to the Semiconductor Industry at 248 nm, 193 nm, and 157 nm. Ongoing.

2. To meet the semiconductor industry's demands for more rapid, accurate measurements of excimer laser power and energy, we are building a system to determine the nonlinear response of an excimer laser detector, Fig. 2. This system uses a correlation method to measure the nonlinear response of pulsed-energy detectors at 248 nm. The response of the detector under test is compared to the corresponding response of a linear monitor detector as a function of incident laser pulse energy. This method addresses the difficulties related to large pulse-to-pulse instability of most excimer lasers.

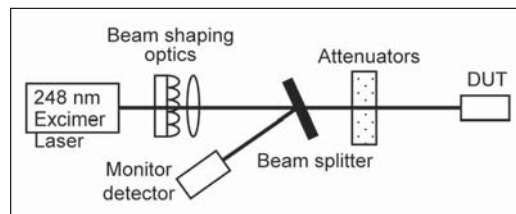


Figure 2. Schematic diagram of 248 nm nonlinear response system.

DELIVERABLES: Add capability to perform nonlinearity measurements at 248 nm. 4Q 2004

3. Improvements to transfer standards used with excimer lasers are needed to better provide for customer traceability to NIST standards. Transfer standard long-term stability, signal/noise, spatial uniformity, linearity, and temperature dependence all contribute to the accuracy of the sensor. Improvements in these critical characteristics will improve the accuracy of laser power and energy measurements for end users.

DELIVERABLES: Develop improved transfer standard detectors of UV power and energy for better dissemination measurements and traceability to NIST standards. 4Q 2004

4. High-accuracy measurements of the index properties of UV materials are required for the design of DUV lithography systems. NIST has been providing absolute index measurements at 193 nm and 157 nm with an accuracy of about 5ppm to the industry using its DUV minimum-deviation-angle refractometer. To improve on this absolute accuracy, NIST has begun a substantial upgrade of the minimum-deviation system and separately begun developing a new system based on a VUV FT spectrometer and a synchrotron radiation as a

continuum source. Both of these systems will enable measurements to an accuracy of 1ppm, and will be used to characterize lens materials and immersion fluids for 193 nm and 157 nm lithography systems.

DELIVERABLES: Index measurement capability with 1 ppm uncertainty. 4Q 2004

5. In order to characterize the index properties of 248 nm, 193 nm, and 157 nm immersion fluids, we developed a high-throughput fluid refractometer, based on a Hilger-Chance design. It incorporates a fluid cell made of 157 nm-transmitting fused silica and uses 248 nm, 193 nm, and 157 nm excimer laser lines. The system measures absolute index with an accuracy of up to 1×10^{-4} and measures index changes with ppm accuracy. This allows accurate measurement of the sensitivity of index to temperature, pressure, and impurities.

DELIVERABLE: Survey of potential 193nm and 157nm immersion fluids indices and dn/dT . 4Q 2004

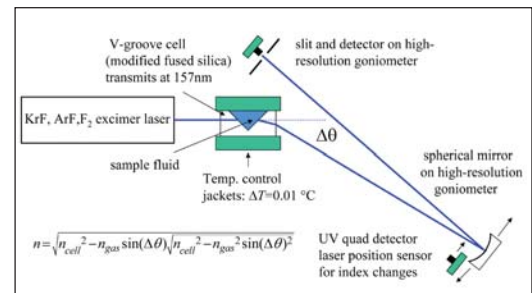


Figure 3. Schematic of VUV Hilger-Chance Refractometer. Measures absolute index n at 248 nm, 193 nm, and 157 nm with uncertainty 1×10^{-4} , and index changes with uncertainty 1×10^{-6} .

6. A beamline at the NIST Synchrotron Ultraviolet Radiation Facility (SURF III) uses the monochromatized radiation from SURF along with a high-accuracy cryogenic radiometer to provide absolute detector-based radiometric calibrations in the spectral range from 125 nm to 320 nm with a standard uncertainty of better than 1%. The spectral range covers all of the current important wavelengths for semiconductor industry such as 248 nm, 193 nm, and 157 nm. We have used this beamline to calibrate a variety of detectors for both power response and irradiance response. In addition, this beamline is capable of measuring both the transmission and reflection from an optical sample such as calcium fluoride with high accuracy.

DELIVERABLES: Achieve an improved accuracy of 0.1% for wavelength longer than 200 nm by transferring the detector scale from a tunable laser-based cryogenic radiometer facility at NIST. 1Q 2005

7. In addition to the cryogenic radiometer-based radiometric beamline, we have constructed a new synchrotron radiation-based beamline for irradiance calibration. This beamline let the synchrotron radiation irradiates the device under test with minimal optical components such that the calculability of the synchrotron radiation can be preserved. By carefully measuring the fundamental parameters of synchrotron radiation such as electron energy, orbital radius, and electron beam current, the irradiance at the user plane can be determined for a wide spectral range from EUV to IR. The accuracy from the calculation was compared to the response of several filtered radiometers and the agreement was better than 0.5%. This establishes SURF as a national standard light source. We are also comparing our irradiance scale in the UV with many other nations in the world via deuterium lamps.

DELIVERABLES: Calibrate the irradiance response of DUV filtered radiometers with an uncertainty of 0.5% level and compare the irradiance scale at SURF with international standard laboratories. 1Q 2005

8. A new facility for characterizing the degradation of diodes to excimer radiation at 157 nm and 193 nm has been completed. This facility allows the measurement of the spectral responsivity of the devices in the spectral range from 130 nm to 600 nm along with the measurement of the reflectivity of the diodes as the devices are irradiated by the excimer laser. This not only allows the identification of potentially stable diodes but also sheds light on the mechanisms responsible for the degradation which can help in the development of more radiation resistant diodes. For example, we have identified some important processes involved in the degradation of diodes such as the formation of trap states at the silicon-silicon dioxide interface.

DELIVERABLES: Characterize the stability of a variety of semiconductor diodes using a range of laser wavelengths from 157 nm to as long as 248 nm for more insight in the radiation damage processes. 4Q 2004

ACCOMPLISHMENTS

■ We have completed construction and testing of a fundamentally new type of laser calorimeter standard for 157 nm excimer laser energy measurements. This new calorimeter is electrically cali-

brated and uses a thin-walled SiC absorbing cavity, which is designed to completely absorb and spread the incoming laser energy through multiple reflections. We have also completed construction of the measurement system needed to use these new standard calorimeters to calibrate excimer laser sensors at 157 nm for customers. To date, we have calibrated two detector systems for companies supplying excimer laser energy sensors to the semiconductor industry.

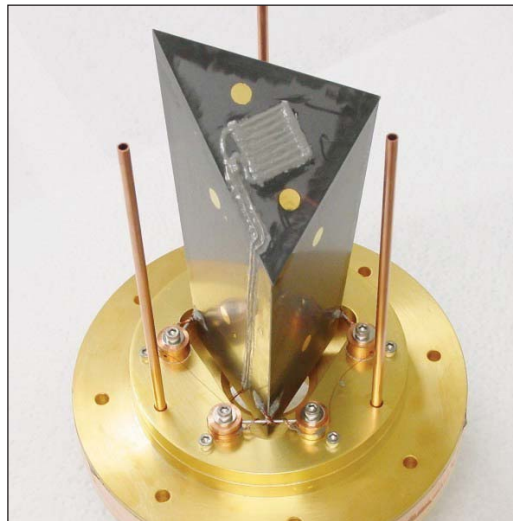


Figure 4. Fundamentally new type of laser calorimeter standard (QDUV) based on multiple reflections inside a thin-walled SiC cavity. The cavity, pictured with the opening pointed down, shows the electrical heater on the top side, and the thermopile consisting of 24 thermocouples distributed on the three bottom corners.

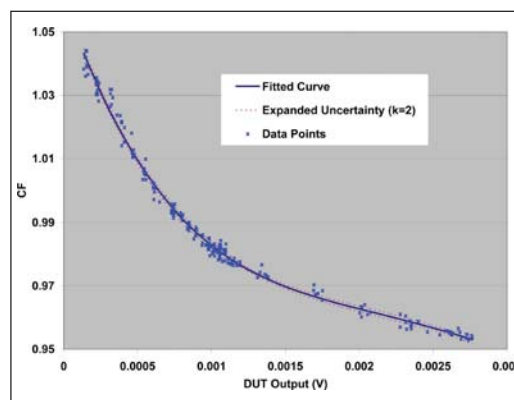


Figure 5. Nonlinearity measurement results at 193 nm of a commercial pyroelectric detector. CF is the correction factor for the detector's nonlinear response.

■ We have developed a system to characterize the nonlinear response of a 193 nm excimer laser detector based on the correlation method. The method and system solves measurement difficulties associated with the temporal and spatial fluctuations of excimer laser pulse energy. The system has a dynamic range of 30 μ J to 50 mJ of pulse energy. The typical measurement uncertainty is 0.8%. Several DUV detectors were tested. Using this system, one can easily determine the origin of a detector's nonlinear response, such as those due to the incident pulse energy, range discontinuities associated with detector gain, and detector background noise, see Fig. 6. We have discovered detectors having nonlinearity as high as 8%.

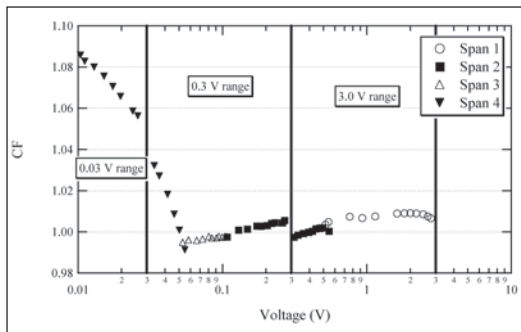


Figure 6. Nonlinearity measurement result of a 193 nm pulsed laser energy detector. CF is the correction for the detector's nonlinear response. The response is measured in four spans, covering 2.5 meter settings. The large degree of nonlinearity at the low end of the meter range is due to background effects.

■ We have determined the damage thresholds and lifetimes of several materials using 157 and 193 nm excimer lasers and a beam profile technique similar to ISO 11254-2, Fig. 7. We made these measurements to select an appropriate absorbing

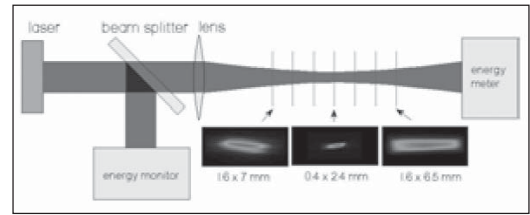


Figure 7. Damage threshold measurements. Beam profiles were recorded and characterized at 22 planes along the propagation axis using a CCD camera and quantum converter. Three energy density distributions at inner- and outer-most positions, together with their dimensions, are shown. The dimensions are based on the calculation of the second moments according to ISO 11146.

material for use in our primary standard laser calorimeter for 157 nm excimer laser power measurements. The materials we tested were nickel-plated sapphire, chemically-vapor-deposited silicon carbide (CVD SiC), nickel-plated copper, and polished copper. Applied pulse energy densities (or dose) ranged from 80 to 840 mJ/cm². We determined the applied dose from a series of laser beam profile measurements. Silicon carbide had the highest damage threshold: 730 mJ/cm² per pulse. For this reason, and for its high thermal and electrical conductivities, we have chosen silicon carbide as the absorber material for the 157 nm calorimeter.

Using our unique VUV Hilger-Chance refractometer with an excimer laser source, we have made the first measurements of the refractive index (n) and thermo-optic coefficient (dn/dT) of candidate 157nm immersion fluids. Results for some of these fluids are shown in Fig. 8. 157nm immersion fluids with improved properties may be required, and we are collaborating with several companies on the development of these fluids. We are also surveying potential high-index 193 nm fluids, as alternatives to water.

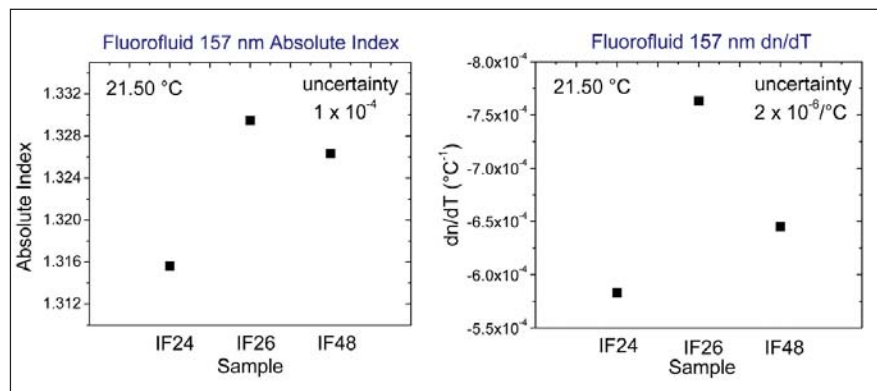


Figure 8. Refractive properties of potential fluorofluids for 157 nm immersion lithography.

- The stability of semiconductor diodes under irradiation from an excimer laser operating at 157 nm has been evaluated. We have determined that for silicon photodiodes, for example, an important mechanism for the degradation is the formation of trap states at the interface of the silicon-silicon dioxide induced by the damaging radiation. These trap states act as recombination centers and reduce the yield of electric current generated by incident radiation. A model was developed to simulate the change in response for photodiode irradiated by 157 nm radiation.

We have built a facility at SURF III that allows simultaneous exposure of photodiodes to excimer radiation (see Fig. 9) and synchrotron radiation. Measurements of the spectral responsivity can be made in the spectral range from 130 nm to 320 nm with a standard uncertainty of less than 1%. The intense, pulsed laser radiation was used to expose the photodiodes for varying amounts of accumulated irradiation whereas the low intensity, continuously-tunable cw radiation from the

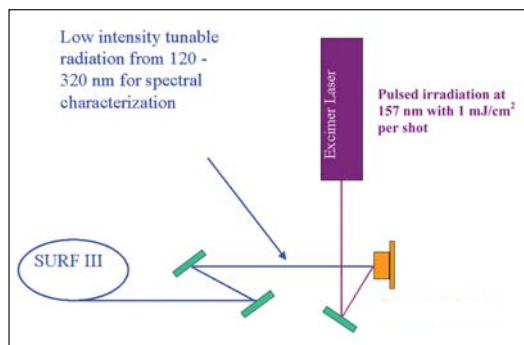


Figure 9. Photodetector damage experiment for 157 nm radiation.

synchrotron source was used to characterize the photodiodes. The changes in the spectral responsivity of different kinds of diodes such as UV silicon, GaP, GaAsP, PtSi, diamond, and GaN were measured for a large range of total accumulated dose from an F₂ excimer laser operating at 157 nm. Differing amounts of changes were seen in different diodes depending on the total excimer irradiation dose and they showed different spectral changes in the responsivity as well. This yields important information about the mechanism responsible for the degradation of photodiodes.

- We have also characterized pyroelectric detectors which are commonly used for high-power laser application. In the vacuum UV to near UV range, pyroelectric detectors are commercially available because of important applications in

areas like semiconductor photolithography. Instead of calibrating these detectors using high-power radiation, we performed measurements with low-power UV radiation at beamline 4 of the SURF III. To accommodate the pulse detection nature of the pyroelectric detectors, we installed a 10 Hertz tuning fork chopper at beamline 4 and lock-in amplifiers were used for detector signal processing. Several commercial pyroelectric detectors were tested at our facility. We found that in most cases, the manufacturer-supplied amplifiers were too noisy for our light intensity on the order of one microwatt. Subsequently, a low-noise amplifier was constructed and installed near the detection head. In addition, for several high reflectance pyroelectric detectors, we also measured the reflectance of the pyroelectric element to check the internal quantum efficiency of the detector.

- We have constructed and characterized a probe that is suitable for accurate measurements of irradiance in the vacuum ultraviolet spectral range. Many industrial applications such as UV curing, photolithography, or semiconductor chip fabrication require accurate measurement of the irradiance and will benefit from having such a stable, accurate UV probe. The probe was characterized at various wavelengths ranging

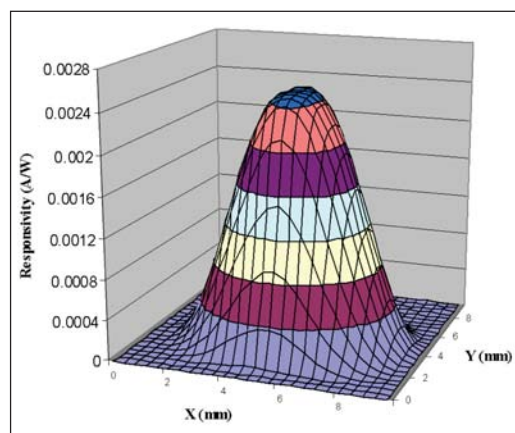


Figure 10. Measurement of the areal responsivity of a UV probe at 157 nm.

from 157 nm to 325 nm, encompassing many of the important industrial application wavelengths. The principle of measurement of the irradiance is based on scanning the probe in a light field and measuring the spectral responsivity on a grid with regular spacing. Measurement of the spectral responsivity in the center of the probe along with the integrated total responsivity yields the spectral irradiance (see Fig. 10). This method can

alternatively be used to calculate aperture areas as well by measuring the ratio of the total responsivity and the responsivity in the center.

COLLABORATIONS

MIT Lincoln Laboratory, Mordechai Rothschild; DUV detector damage, immersion optical fluid measurements.

RECENT PUBLICATIONS

“A Primary Standard for 157 nm Excimer Laser Measurements,” C. L. Cromer, M. L. Dowell, R. D. Jones, D. A. Keenan, S. Yang, 2003 Int’l Conf. on Characterization and Metrology for ULSI Tech. (March 2003) *in press*.

“A 193 nm Detector Nonlinearity Measurement System at NIST,” S. Yang, D. A. Keenan, H. Laabs, M. L. Dowell, Proc. SPIE Metrology, Inspection, and Process Control for Microlithography XVII, (February 2003) *in press*.

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METROLOGY SUPPORTING EXTREME ULTRAVIOLET LITHOGRAPHY

GOALS

Provide leading-edge metrology for the development and characterization of optical components and detectors used in Extreme Ultraviolet Lithography (EUVL). (EUVL utilizes radiation at 13.4 nm.)

CUSTOMER NEEDS

An intense international effort is presently underway to develop EUVL for the patterning of wafers beginning in about 2009. A milestone in the U.S. effort was the building of an alpha-tool called the ETS (Engineering Test Stand) that is housed at the Sandia National Laboratory. While the ETS has demonstrated the feasibility of EUVL for 70 nm design rules and beyond, much work needs to be done to improve the throughput, mask fabrication, and lifetime of the optics.

High resolution imaging with EUV radiation was not possible until the development of multilayer EUV mirrors in the mid 80s. This development has spawned the relatively new field of EUV optics and its associated set of new metrological challenges. Among these are: 1) precise EUV reflectivity maps; 2) EUV dosimetry; 3) EUV damage characterization; and 4) nanometer level optical figure measurement.

TECHNICAL STRATEGY

1. PRECISE EUV REFLECTIVITY MAPS

The present NIST/DARPA EUV Reflectometry Facility is located on a multipurpose beamline on the NIST Synchrotron Ultraviolet Radiation Facility (SURF III) storage ring. The beamline can provide a monochromatic beam of EUV or soft X-ray radiation in the 3 nm to 40 nm (400 eV to 30 eV) spectral range. Although primarily designed to serve the EUVL community by providing accurate measurements of multilayer mirror reflectivities, this beamline with its associated sample chamber has been used for many other types of measurements since the beamline's commissioning in early 1993. Among the other measurements performed recently are grating efficiencies, photocathode conversion efficiencies, phosphor conversion efficiencies, film dosimetry, and determination of EUV optical constants through angle dependent reflectance measure-

ments. A diagram of the NIST/DARPA EUV Reflectometry Facility is shown in Fig. 1.

Currently the NIST/DARPA facility is the only one in the U.S. large enough to measure optics larger than 200 mm in diameter. A recent international intercomparison among NIST and several other labs demonstrated reflectivity accuracy of 0.3 % and wavelength accuracy of 0.01 nm. Plans are underway to reduce wave-length uncertainty by an order of magnitude.

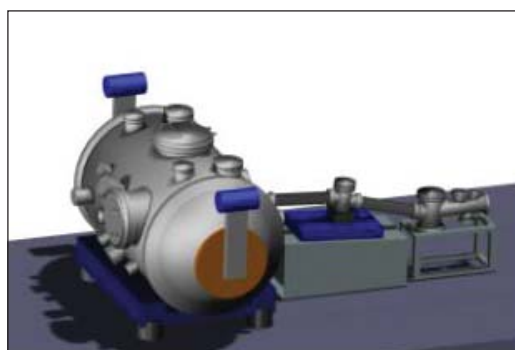


Figure 1. Diagram of NIST/DARPA EUV Reflectometry Facility, including the sample chamber and monochromator.

DELIVERABLES: Full reflectivity map of EUV mirrors up to 40 cm in diameter and 45 kg mass on an as needed basis for the EUVL community. Reflectivity and transmittance measurements of metrology components for International SEMATECH.

2. EUV DOSIMETRY

NIST is the primary national source for the radiometric calibration of detectors from the infrared to the soft X-ray regions of the spectrum. Until recently all NIST-characterized EUV photodetectors were calibrated on the SURF storage ring, which is essentially a cw source. Recently we have designed and built a pulsed EUV source similar to the source being used in the ETS to calibrate EUV detectors for characterizing sources as well as wafer-plane dosimeters to be used in EUVL.

Two major concerns arise when using solid state photodiodes for detection of short pulse length radiation. First, while the average power may be quite modest, the peak power can be quite high. For example, a 10 Hz laser with an average power of 10 mW has a peak power of 100 kW for a 10 ns

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pulse. Photodiode saturation may seriously affect the linearity of EUVL dosimeters, even at fairly low average power levels. We have measured the limit of the linear operating range for an EUV sensitive Si photodiode using 532 nm radiation as a proxy for 13.4 nm; the absorption characteristics in Si are nearly identical. We have found that the photodiode responsivity is an inherently non-linear function of pulse energy, but the responsivity can be fit by a calibration function having two constant parameters. Use of the non-linear calibration function allows the photodiode to be used with reasonable uncertainty even when the responsivity has decreased due to saturation effects by as much as a factor of two. Defining the limit of linear operation as the pulse energy at which there is a loss of responsivity of 2 %, the total charge collected from a Si photodiode is a linear function of pulse energy at peak powers of 1 W (for an unbiased device) to 5 W (for a reverse bias of 10 V). The peak voltage developed is a linear function of pulse energy from 60 mW (unbiased) to 250 mW (10 V reverse bias). Currently, we are extending these results to determine the effect of the longer pulse lengths typical of EUVL plasma discharge sources, to understand the dependence on pulse energy density, and to explore a range of higher reverse bias conditions. A second concern is the equivalence of the responsivity under pulsed conditions and under the cw conditions of calibration facilities. We have compared the measured responsivity of a Si photodiode under pulsed conditions to the results of a low-power cw calibration. The low-power limit of the non-linear pulsed responsivity function is identical to the low-power cw responsivity with a relative standard uncertainty of 1 %. Thus, the results of a cw calibration may be transferred to a pulsed application if the pulse energy dependence is properly accounted for. Finally, we are investigating the saturation behavior using CW EUV radiation. The combination of these three conditions should lead to a good understanding of pulsed-EUV behavior.

We have developed a model of the physical processes that are responsible for the observed non-linear response function of the photodiodes. The loss of total collected charge is modeled as a result of recombination processes in the device during the electronic readout process. In this model, the decrease in the peak voltage developed arises from an increase in the junction capacitance due to the presence of the photogenerated electron-hole pairs, which act as a polarizable

dielectric medium. The model correctly predicts the behavior of both calibration parameters as a function of reverse bias. To date, we have obtained results in the reverse bias range from 0 V to 10 V, and we will shortly be extending our observations to 150 V.

We have recently reduced the uncertainty of our cw radiometric scale in the neighborhood of 13 nm wavelength from the previous relative standard uncertainty of 4 % to 1 %. We accomplished this by operating an absolute cryogenic radiometer (ACR) on a high-throughput beamline at the SURF III synchrotron radiation facility and calibrating working standard photodiodes by direct comparison to the radiometer. The improved cw scale is transferred to the EUVL calibration facility described above to provide a U.S. national radiometric scale for detector-based pulse energy measurements at 13.4 nm wavelength with a relative standard uncertainty of a few percent.

Our group recently conducted the first ever responsivity measurements of an assembled Flying Circus metrology tool for EUVL. The Flying Circus (FC2) was developed by FOM (Foundation for Fundamental Research on Matter in the Netherlands). It is a filtered radiometer composed of Mo/Si Multilayer mirror, a thin film filter, and an EUV sensitive photodetector. The measurements were done by utilizing in-vacuum transfer optics to relay EUV radiation from within the NIST/DARPA EUV reflectometer sample chamber into an external endstation as shown in Fig. 2. Beyond the sample chamber the endstation housed a removable calibrated transfer standard followed by the FC2. Measurements were conducted by placing the working standard in to the incident beam and transferring its calibration to the double slit beam monitor of the reflectometer by scanning the wavelength of the monochromator and recording the ration of the two detectors. The working standard was then removed from the beam path and light was brought in the FC2 where it was directed onto its detector. The calibration of the beam

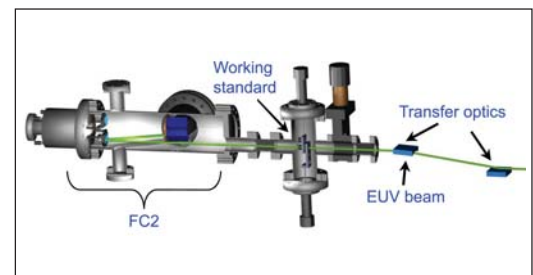


Figure 2. Schematic of Flying Circus 2 mounted on Beamline 7.

monitor was then transferred to the output of the FC2. This cycle was repeated for various configurations and filter combinations to fully measure the instrument's performance. These measurements showed excellent agreement in both peak and integrated comparisons of predicted values based on individual component calibrations. All the measurements and calculations of the FC2's responsivity agreed to within the uncertainties of the measurements and were typically on the order of 2.5 %.

DELIVERABLES: (1) Assemble E-Mon calibration. 2Q 2004 (2) FC2 calibration on LPP-source. 3Q 2004 (3) Development of Al_2O_3 based diagnostic for plasma environment. 4Q 2004

3. EUV DAMAGE CHARACTERIZATION

The energetic (91 eV) EUV photons impinging on the mirrors in the vacuum environment of the stepper induce various reactions that can damage the multilayer coatings. Some of the reactions can be attributed to EUV-excited water vapor and EUV-dissociated hydrocarbons. (Both a small amount of residual water and hydrocarbon vapors are present in the stepper environment.) In fact, lifetime tests show that the expected lifetime under present conditions is far short of the year duration needed for economic operation.

We have recently commissioned a beamline that is dedicated to the exposure of multilayer optics under controlled environmental conditions. This effort has been supported by Sandia National Laboratory and International SEMATECH. Multilayer samples with silicon and ruthenium capping layers, provided by Lawrence Livermore National Laboratory, have been exposed for periods of 60 hours each. The samples resided in a water rich atmosphere under an average EUV intensity of 5 mW/mm^2 . The results are shown in Fig. 3. The Si capped sample exposed for 60 hours suffered a degradation in reflectivity of more than 20 % due to oxidation at the surface of the mirror. In contrast, the Ru-capped sample suffered a reflectivity degradation of only 2 % under similar illumination and atmospheric conditions. We are currently adding the capability of introducing additional atmospheric components like hydrocarbons to further simulate the conditions present in a projection optics box. This beamline will provide a valuable tool for the EUV optics development community by permitting long-term exposures of various capping layer schemes under controlled atmospheric conditions.

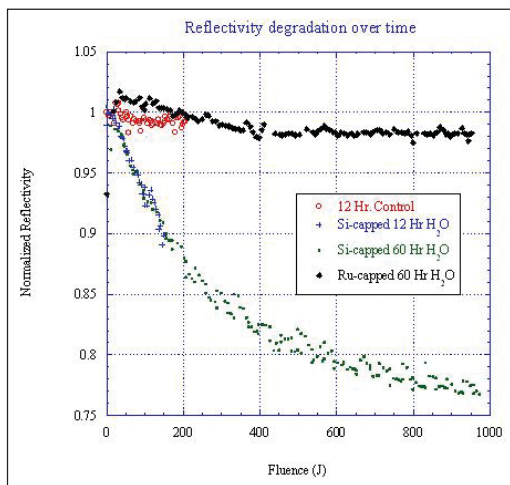


Figure 3. Reflectivity vs. fluence for multilayer samples exposed to EUV radiation.

It is estimated that the required optics lifetime is about 20,000 hours. It will not be possible to test multiple optics types for this length of time, so a method of accelerated testing must be developed. This will require both an understanding of the damage mechanism and experiments in order to verify this understanding. We are beginning scaling experiments, in which we expose multilayers to various intensities under various atmospheric conditions. The data from these studies will be used by NIST and collaborators to determine optimum conditions for accelerated testing.

DELIVERABLES: (1) Carry out experiments on samples provided by EUVL community and International SEMATECH. (2) Work with collaborators to develop accelerated lifetime testing protocol. 4Q 2004

4. SUB-NM OPTICAL FIGURE MEASUREMENT

The commissioning of the “eXtremely accurate CALIBration InterferometerR” (XCALIBIR) at NIST is now complete and the instrument is fully functional (Fig. 4). The XCALIBIR interferometer is a multi-configuration precision phase-measuring interferometer for optical figure measurements of flat, spherical and aspheric optics that can achieve the very low measurement uncertainties that are required for the measurement of EUVL optics.

The interferometer may be operated in either Twyman-Green or Fizeau configurations. A beam expander in the test arm of the interferometer provides a collimated test beam with 300 mm diameter. Transmission spheres are used to realize a spherical Fizeau interferometer for the testing of spherical and aspheric surfaces. The part under

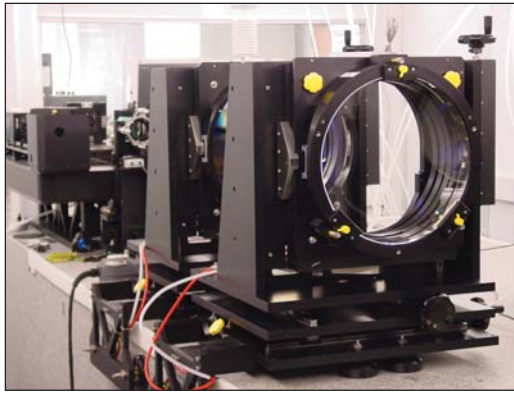


Figure 4. A view of the XCALIBIR interferometer.

test is mounted on a remotely controlled 5+1-axis mount that can be moved on air bearings along a precision slideway in the direction of the optical axis of the interferometer. A system of three laser-interferometers tracks the movement of the test mount in the direction of the optical axis. A single-mode external cavity diode laser (ECDL) is used as the light source in XCALIBIR. The laser frequency can be modulated to vary the effective temporal coherence over a wide range. Optical fibers with different core diameters are used to couple the light into the interferometer. The spatial coherence of the light source can thus be varied by changing the fiber core diameter.

The 300 mm diameter reference flats for the flat Fizeau configuration of the interferometer were calibrated with a 3-flat, 6-position self-calibration test. Figure 5 shows the topography of one of the reference flats. A large number of 3-flat measurements were made to estimate the measurement uncertainty. For each of the flats A, B, and C the *rms* of the difference between the averaged flat solutions and the individual

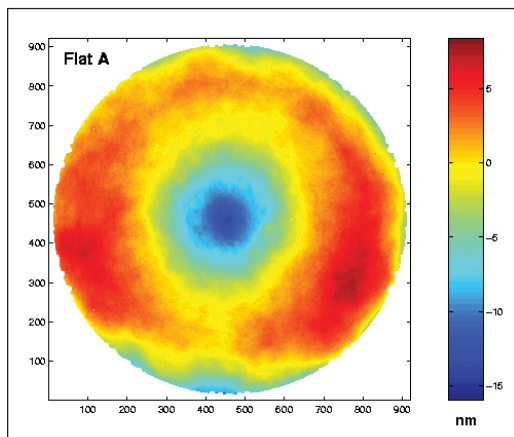


Figure 5. Topography of a 300 mm diameter XCALIBIR reference flat.

measurements was plotted in a histogram (Fig. 6). A (statistical) measurement *rms* uncertainty of approximately 0.2 nm is evident.

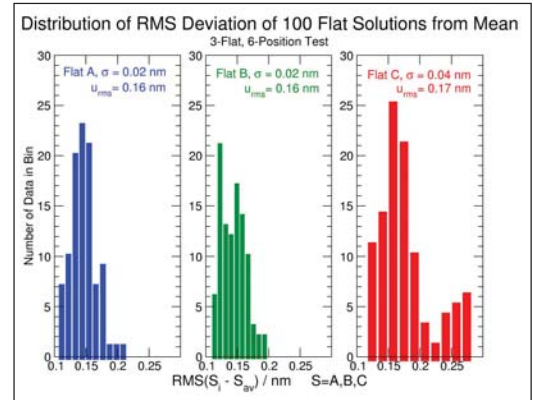


Figure 6. Distribution of *rms* deviations from best estimates surface (mean) for three flats A, B, and C.

When measurements of aspheric optics without null-optics are made, it is frequently the case that only a part, or subaperture, of a surface can be measured at once. For the figure measurement of the entire aspheric surface a number of overlapping subaperture measurements must then be combined, or “stitched” together. We have implemented flexible and robust algorithms for the stitching of subaperture measurements. To demonstrate the power of the stitching algorithm a precision silicon sphere was set up on a rotary table in XCALIBIR and the surface figure error was measured with an F/1.3 transmission sphere. 36 surface error measurements were made at 10° intervals. As shown in Fig. 7, the individual, overlapping, surface error measurements were then stitched together to form a map of the form error of the silicon sphere.

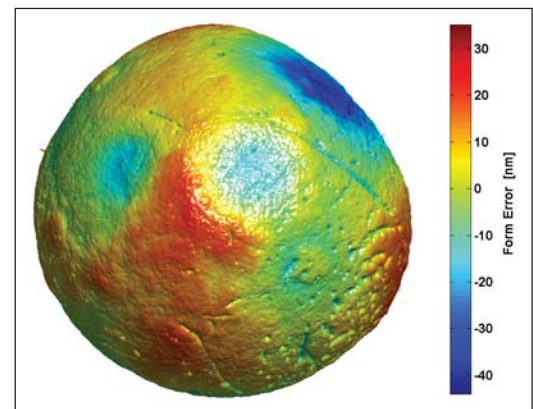


Figure 7. Topography of a precision silicon sphere, stitched from 132 measurements. The figure error is approximately 60 nm PV.

DELIVERABLES: Establish capability for measuring aspheric optics without null optics. 4Q 2003

ACCOMPLISHMENTS

- IR² has undergone a major upgrade that enables us to address the metrology needs for 300 mm diameter wafers. A collimator lens has been installed that can illuminate the entire surface of a 300 mm wafer and thus allows us to make a measurement of the wafer's thickness variation in a single measurement. The imaging system of the interferometer now can measure wafers with larger slopes and the spatial resolution of the detector was doubled. Further improvements will be aimed at reducing the noise level and at improving the measurement uncertainty.
- The thickness variation (TTV) of a low-dopant double side polished silicon wafer has been characterized.
- The flatness of 200 mm and 300 mm diameter wafers in the chucked condition was explored using the XCALIBIR interferometer.

COLLABORATIONS

VNL at Sandia National Laboratory, Leonard Klebanoff, and Mike Malinowsky, Environmental Team.

VNL at Lawrence Livermore National Laboratory, Eberhard Spiller (consultant), Saša Bajt, and Regina Soufli, EUV Multilayer Development and Coating Team.

RECENT PUBLICATIONS

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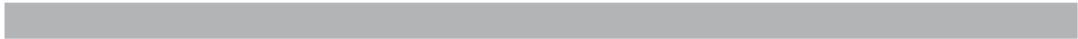
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POLYMER PHOTORESIST FUNDAMENTALS FOR NEXT-GENERATION LITHOGRAPHY

GOALS

In this project, we are developing an integrated program involving fundamental studies of photoresist materials to be correlated with resist performance metrics impacting next generation photolithography. We work closely with industrial collaborators to develop and apply high spatial resolution and chemically specific measurements to understand varying material properties and process kinetics at nanometer scales and to provide high quality data needed in advanced modeling programs. The understanding developed in this program will provide a detailed foundation for the rational design of materials and processing strategies for the fabrication of sub 100 nm structures. The unique measurement methods we apply include X-ray and neutron reflectivity (XR, NR), small angle neutron scattering (SANS), incoherent neutron scattering (INS), near-edge xray absorption fine structure (NEXAFS) spectroscopy, quartz crystal microbalance (QCM), nuclear magnetic resonance (NMR), atomic force microscopy (AFM), Brillouin light scattering (BLS), and combinatorial methods. Our efforts focus on the fundamentals of polymeric materials and processes that control the resolution of the photolithography process including: (1) the physical properties of and polymer chain conformation within sub 100 nm structures; (2) the spatial segregation and distribution of photoresist components; (3) the transport and kinetics of photoresist components, environmental contaminants, and the deprotection reaction interface over nanometer distances; (4) the material sources of line-edge roughness (LER), a measure of the ultimate resolution of the lithographic process; (5) the polymer physics of the developer solution and the dissolution process; and (6) influence of moisture on the thermo-physical properties of interfaces as applicable to immersion lithography. These data are needed to meet the future lithographic requirements of sub 100 nm imaging layers and critical dimensions.

CUSTOMER NEEDS

Photolithography remains the driving and enabling technology in the semiconductor industry to fabricate integrated circuits with ever decreasing feature sizes. Today, current fabrication facilities use chemically-amplified (CA) photoresists, complex and highly tuned formulations of a

polymer film loaded with photoacid generators (PAGs) and other additives. Upon exposure of the photoresist film through a mask, the PAG creates acidic protons. A post-exposure bake is then applied and the acid protons diffuse and catalyze a deprotection reaction on the polymer that alters its solubility in an aqueous base developer solution. These reaction, diffusion, and development processes must be understood and controlled at the nanometer length scale to fabricate effectively integrated circuits. Chemically amplified resists are also deposited onto bottom anti-reflection coatings (BARCs). Interactions and component transport between the BARC and resist layer can lead to loss of profile control or pattern collapse. Detailed studies of these interaction and transport mechanisms are needed to design materials for the successful fabrication of sub 100 nm structures.

There are significant challenges in extending this technology to fabricate the smaller feature sizes (sub 100 nm) needed to continue performance increases in integrated circuits. First, new radiation sources with shorter wavelengths (193 nm, 157 nm, or EUV) require photoresist films nearing 100 nm thick to ensure optical transparency and uniform illumination. In these ultrathin films, confinement can induce deviations in several key materials parameters such as the macromolecular chain conformation, glass transition temperature, viscosity, or transport properties. Furthermore, the required resolution for a sub 100 nm feature will be on the order of 2 nm, approaching the macromolecular dimensions of the photoresist polymers. It is not yet clear how deviations due to confinement will affect the ultimate resolution in these ultra-thin photoresist films. Additionally, the material sources of feature resolution (line-edge and sidewall roughness) and profile control need to be identified and understood to ensure the success of needed patterning technologies.

The requirements for advanced photoresists are discussed in the 2003 International Technology Roadmaps for Semiconductors on page 3, Lithography Section, "Photoresists need to be developed that provide good pattern fidelity, good linewidth control (including roughness), and low defects. As feature sizes get smaller, defects and polymers will have comparable

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"[This work] opens a window of opportunity to construct structure-property relationships between chemical transport mechanisms and ultimate resist resolution. It may also lead to insights into the ultimate, intrinsic resolution limits and critical dimension control of polymer-based imaging materials."

*E. Reichmanis and
O. Nalamasu, Bell Labs,
Lucent Technologies,
Science, 297, 349 (2002).*

dimensions with implications for the filtering of resists.”

TECHNICAL STRATEGY

1. In this project, we use model photoresist materials to validate the new measurement methods. Model 248 nm and 157 nm photoresist materials have been used initially to address several important fundamental questions including the thermal properties of ultrathin films as a function of film thickness and substrate type, the conformation of polymer chains confined in ultrathin films, the surface concentration of PAGs, the diffusion and the reaction kinetics of the deprotection reaction, and the physics of the development process. We also are adapting the application of combinatorial methods as a tool to determine rapidly important lithographic parameters and to identify material factors impacting feature resolution. These results provide a strong basis for understanding the material property changes that may affect the development of lithography for sub 100 nm structures using thin photoresist imaging layers. The interaction between model photoresists and BARC materials also requires detailed experimental investigation to optimize the materials factors impacting lithographic performance.

DELIVERABLES: Utilize XR and QCM techniques to measure the physical properties of sub-100 nm structures and polymer thin films, compared to the bulk material. 2Q 2004

DELIVERABLES: Develop model thin films to measure the transport and kinetics of photoresist components and the deprotection reaction with dispersed PAG components. 3Q 2004

DELIVERABLES: Quantify small molecule transport or uptake with varying solutes and polymer materials including amines (contaminants) and residual casting solvent materials using NEXAFS. 2Q 2004

DELIVERABLES: Utilize reaction-front bilayer geometry to identify and quantify the effects of developer solution parameters (base concentration, pH, ionic strength) on the final resolution of lithographic materials. 2Q 2004

DELIVERABLES: Quantify surface segregation, surface deprotection chemistry, distribution of photoresist components (resist, photoacid, solvent, base additive), using NEXAFS. 4Q 2004

DELIVERABLES: Identify material transport and chemical interactions leading to the formation of residual layers at the BARC-resist interface as a function of processing conditions. 4Q 2004

DELIVERABLES: Develop immersion metrology methods using NR and QCM to quantify small-molecule encapsulation and release by ultrathin photoresist films. 1Q 2004

ACCOMPLISHMENTS

■ The molecular origin of dimensional changes within ultrathin films when exposed to developer solutions was measured using neutron reflectivity. A model 157 nm photoresist material provided needed in the fundamentals of material sources to line-edge roughness. Quartz crystal microbalance measurements complement these measurements with the added ability to measure the kinetics of swelling, however, the profile and chemical specificity are exclusively obtained with NR.

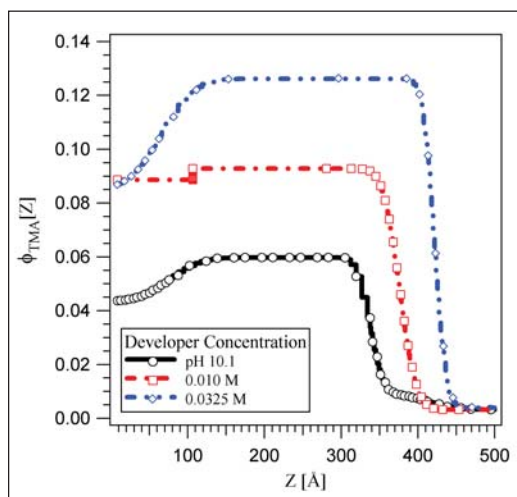


Figure 1. Developer Fundamentals for LER. Direct measure of the base concentration dependence of swelling and deuterated tetramethyl ammonium ion profile throughout the thickness, of a model 157 nm photoresist using liquid immersion neutron reflectivity.

These new measurement methods, applicable to immersion lithography, demonstrate that swelling and aqueous base penetration must be considered to improve dissolution models involving solid-liquid interfaces. The aqueous base profile shown in Fig. 1, illustrates the penetration of the small base molecule throughout the thin film as a function of developer strength. The swelling, due to polyelectrolyte effects, was predicted in FY03. The influence of moisture and interfacial energy are also probed using NR, XR, and quartz crystal microbalance techniques allowing a complete equilibrium and kinetics measurement methods.

■ Incoherent neutron scattering was used to measure the atomic-level dynamics of model photoresist polymer thin films for the first time. The local, atomic-level, dynamics of the photoresist polymer directly affect transport processes essential to modern photoresists, such as the diffusion of photogenerated acids and other small molecules within the polymer matrix. To date, changes in the local dynamics of polymer thin films have been inferred from changes in macroscopic quantities such as the apparent glass transition temperature, T_g , as a function of film thickness and substrate interaction energies.

Direct measurements of the segmental motions of polymer chains confined to ultrathin films provide a molecular picture of observed changes in these macroscopic quantities and insight into differences in photoresist transport processes in ultrathin films. QCM measurements of moisture diffusion rates in ultrathin resist films are dramatically reduced relative to those in thicker films. Further, in Fig. 2, three different measurements show similar reductions of mobility at similar film thickness length scales.

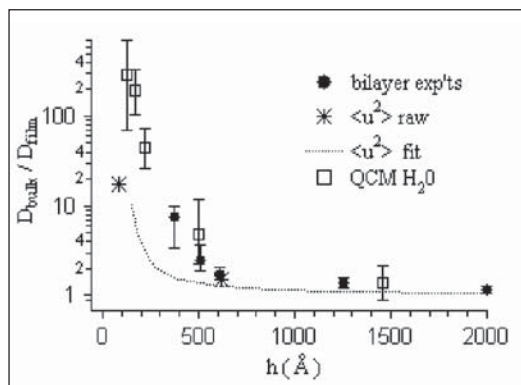


Figure 2. The ratio of the bulk to film diffusion coefficients are displayed as a function of film thickness for the bilayer, neutron scattering, and QCM experiments. All three techniques indicate similar reductions of mobility at similar length scales.

■ After photogeneration, acid molecules catalyze multiple reactions within the photoresist matrix. A central issue in photoresist design is quantifying both the number of reactions each acid can catalyze and the size and shape of the deprotected volume created upon reaction. The size and shape of the volume have been identified in recent computer simulations as a primary source line edge roughness (LER) formation.

Using SANS and specially deuterated polymers, we successfully measured characteristics of the

deprotection volume due to acid diffusion paths in a model photoresist. The general technique is readily extendible to photoresists with the appropriate deuterium labeling, independent of the PAG species. The deprotection volume from dispersed acid molecules features a diffuse interface, a result inconsistent with a well-defined two-phase structure. The data in Fig. 3 are consistent with models for random walk statistics. We determined that the deprotection volume has a radius of approximately 8.5 nm after 120 s of post exposure bake at 90 °C. Infrared spectroscopy was used to determine the level of deprotection at 32 % with a 0.7 % mass fraction of PFOS. The result is consistent with a large diffusion path, and hence a large number of catalyzed reactions per acid molecule.

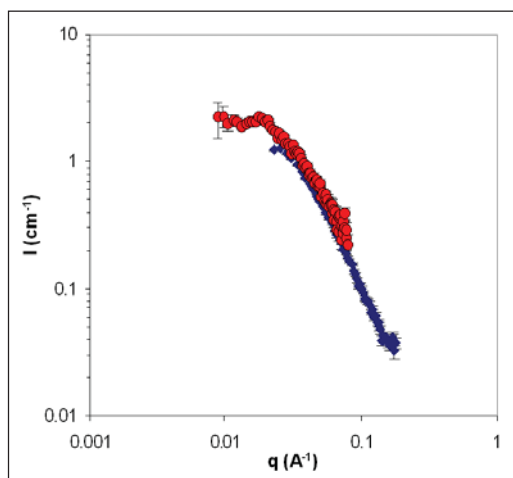


Figure 3. SANS data from the deprotection of dispersed PAGs after exposure and bake. The data are consistent with a random walk deprotection reaction path.

■ The deprotection reaction front profile was measured with nanometer resolution using both xray and neutron reflectometry on a bilayer structure prepared with a specially labeled (deuterated) protected polymer. The upper layer of the structure is loaded with the PAG. Upon exposure and baking, the acid diffuses into the lower layer and catalyzes the deprotection reaction. The protecting group is deuterated and is volatile upon reaction. Thus, contrast to neutrons results from the reaction allowing for observation of the reaction front. By comparing the reaction front to the developed film profile, we obtain important insight into both the spatial extent of the reaction and the development process itself. These data are the first available with this spatial resolution and are critically

needed for the development of process control over nanometer length scales. We find that the reaction front broadens with time while the surface roughness of the developed structure remains relatively sharp. Additionally, we find that a broader reaction front results in changes in the compositional profile upon development in an aqueous base.

- NEXAFS measurements were used to measure the surface concentration of photoresist and BARC components and the surface reaction kinetics in model photoresist polymers as a function of common processing conditions. A significant advantage of the NEXAFS measurement is the capability of separating interfacial and bulk signals within the same sample and experiment in Fig. 4. NEXAFS measurements of interfacial chemistry are possible because of the limited escape depth of produced secondary electrons. By separately observing the electron and fluorescence yield, the chemistry at the surface (2 nm) and bulk (200 nm) may be determined. Different chemistries may be observed by examining the near-edge xray spectra of light elements such as carbon, oxygen, fluorine, and nitrogen. In this way, changes in the surface chemistry relative to the bulk film can be investigated as a function of lithographic processing steps such as exposure and heating. We have found that fluorinated PAG molecules preferentially segregate to the film surface. The relative amount of segregation is dependent upon the specific polymer. In addition, NEXAFS analysis of residual layers arising from BARC-resist component transport and interactions enable detailed analysis of potential mechanisms leading to loss of profile control. UV exposure, post-exposure bake, and a novel atmosphere controlled chamber have been developed to test environmental stability against model air-

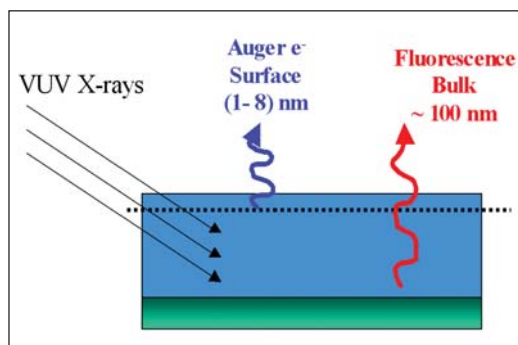


Figure 4. Schematic diagram of the NEXAFS measurement geometry. Spectra are obtained from the film surface and bulk simultaneously.

borne contaminants and influence on *in situ* processing.

- The development step selectively removes UV exposed photoresist material and represents the last step in the fabrication of nanostructures prior to semiconductor etch and deposition. With dimensions shrinking to sub 100 nm, control of line-edge roughness becomes more important and contributions to roughness from the development step requires an improved framework. In the development step, the aqueous base TMAH developer shifts the local chemical equilibrium from an unionized form to the ionized form, for instance in the 248 nm material poly(hydroxystyrene). SANS data, in Fig. 5, demonstrate the origin of the miscibility in aqueous base is due to the ionization of the photoresist leading to polyelectrolyte behavior. The identification of the presence of polyelectrolyte behavior during the development process provides an improved framework to understand the roles of added electrolytes, such as low molecular weight organic (tetramethyl ammonium chloride) and inorganic salts (NaCl, KCl). The addition of salts controls the observed line-edge roughness, by reducing the influence of polyelectrolyte behavior. Current experiments using different developing and rinsing protocols demonstrate that the pH of the rinse step is very important. This suggests the surface layer may contain polyelectrolyte effects even after development as demonstrated by an increase in surface RMS roughness for the development of bilayer samples with 0.26N TMAH followed by water rinse and 0.01 M HCl rinse.

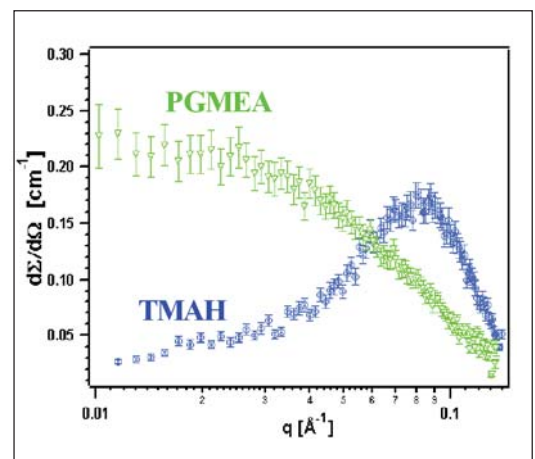


Figure 5. SANS data from a model photoresist polymer in organic solvent (PGMEA) and the developer base solution (TMAH). The scattering peak in TMAH solution is representative of the polyelectrolyte behavior.

COLLABORATIONS

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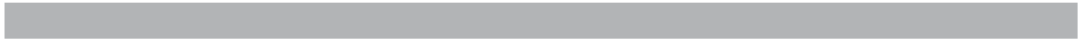
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CRITICAL DIMENSION AND OVERLAY METROLOGY PROGRAM

The principal productivity driver for the semiconductor manufacturing industry has been the ability to shrink linear dimensions. A key element of lithography is the ability to create reproducible undistorted images, both for masks and the images projected by these masks onto semiconductor structures. Lithography as a whole, fabricating the masks, printing and developing the images, and measuring the results, currently constitutes $\approx 35\%$ of wafer processing costs. The overall task of the Critical Dimension and Overlay Program is to assist the industry in providing the necessary metrology support for current and future generations of lithography technology. These goals include advances in modeling, the provision of next generation critical dimension and overlay artifacts, development of advanced critical dimension and overlay techniques, and comparisons of different critical dimension and overlay measurement techniques.

Currently, resolution improvements have outpaced overlay and critical dimension measurement improvements. To maintain cost effectiveness significant advances must be made.

WAFER-LEVEL AND MASK CRITICAL DIMENSION METROLOGY

This project is the single largest project at NIST supporting the semiconductor industry. It involves metrology and artifact development across a broad range of techniques. For this reason the project is presented in a number of sub-sections, each focusing on a single technology. These are:

- Scanning Electron-Based Dimensional Metrology
- Scanning Probe Microscope-Based Dimensional Metrology
- Small Angle X-Ray-Based Dimensional Metrology
- Electrical-Based Dimensional Metrology and Single Crystal Critical Dimension Artifact Development
- Optical-Based Photomask Dimensional Metrology
- Model-Based Linewidth Metrology
- Atom-Based Dimensional Metrology

SCANNING ELECTRON-BASED DIMENSIONAL METROLOGY

GOALS

Provide the microelectronics industry with highly accurate SEM measurement and modeling methods for shape-sensitive measurements and relevant calibration standards with nanometer-level resolution.

Carry out SEM metrology instrumentation development, including improvements in electron gun, detection, sample stage and vacuum system.

Conduct research and development of new metrology techniques using digital imaging and networked measurement tools solutions to key metrology issues confronting the semiconductor lithography industry.

CUSTOMER NEEDS

The scanning electron microscope is used extensively in many types of industry, including the more than \$200 billion semiconductor industry in the manufacture and quality control of semiconductor devices. The industry needs SEM standard artifacts, specifically those related to instrument magnification calibration, performance and the measurement of linewidth. This entails a multidimensional program including: artifact fabrication, understanding the function and signal generation in the SEM, electron beam interaction modeling, developing NIST metrology instruments for the certification of standards, and developing the necessary artifacts and calibration procedures. The manufacturing of present-day integrated circuits requires that certain measurements be made of structures with dimensions of 100 nm or less with a high degree of precision. The accuracy of these measurements is also important, but more so in the development and pilot lines. The measurements of minimum feature size known as critical dimension (CD) are made to ensure proper device operation. The U.S. industry needs high-precision, accurate, shape-sensitive dimension measurement methods and relevant calibration standards. The SEM Metrology Project supports all aspects of this need since scanning electron microscopy is the major microscopic technique used for this sub-micrometer metrology.

TECHNICAL STRATEGY

The Scanning Electron Microscope Metrology Project a multidimensional project. It is being executed through several thrusts fully supported by the semiconductor industry.

1. SEM Magnification Calibration Artifacts: Essential to SEM dimensional metrology is the calibration of the magnification of the instrument. Standard Reference Material (SRM) 2120 is an SEM magnification standard that will function at the low beam voltages used in the semiconductor industry and high beam voltages used in other forms of microscopy (Fig. 1). A prototype with 200 nm lines and spaces was fabricated by the Nanofabrication Facility at Cornell University as a proof of concept and was used in a round robin study that clearly demonstrated the need for this standard. In order to make this artifact available (while the final certification details are being completed) the artifact will be released as Reference Material (RM) 8120.

DELIVERABLES: Development of a new metrology SEM based on a variable pressure instrument. This instrument will be able to work with full size wafers and photomask. Preparation of an assessment of the error budget for the fully functional metrology system. Preparation of customized recipes for various versions of magnification calibration samples. Upon availability of suitable quality samples, quality assessment and delivery of a batch of RM 8120. Upon availability of suitable quality samples, completion calibration and delivery of a batch of SRM 2120 samples.

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“Scanning Electron Microscopy (SEM) – continues to provide at-line and inline imaging ... and CD measurements. Improvements are needed ... at or beyond the 65 nm generation ... Determination of the real 3D shape ... will require continuing advances in existing microscopy ...”

International Technology Roadmap for Semiconductors, 2003

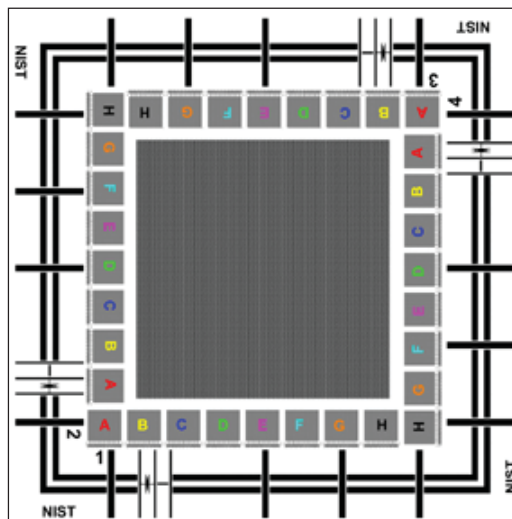


Figure 1. The new design of the SRM 2120 Magnification calibration Standard Reference Material.

2. SEM Performance Measurement Artifacts:

This effort included the development of the Reference Material 8091 and evaluation procedures suitable for correctly measuring image sharpness of scanning electron microscopes, especially of those that are used in the semiconductor industry. The resolution performance characteristics of the SEM are particularly important to precise and accurate measurements needed for semiconductor processing. New methods and suitable samples are being sought to further improve this type of metrology.

3. SEM Linewidth Measurement Artifacts: Artifacts that are characterized and calibrated to the required small levels of uncertainty were and are in the focal point of the IC industry's dimensional metrology needs. Therefore, at NIST, it has been a longer-term goal to develop and deliver appropriate samples. For a long time the possibilities were limited by the lack of various technologies available, especially the lack of accurate modeling methods. NIST, through several years of systematic efforts, developed Monte Carlo simulation-based modeling methods that can deliver excellent results. These new methods can deduce the shape of integrated circuit structures from top-down view images through modeling and library-based measurement techniques with few nm accuracy. NIST in several publications demonstrated the possibilities and described power of this measuring approach. Based on the newest results, now it is becoming possible to start to develop the long-awaited relevant line width standard for the semiconductor industry. Reference Material 8120 line width samples will be a relevant sample on a 200 mm and 300 mm Si wafer with polySi features with sizes from 1 μm to down to 70 nm. Standard Reference Material 2120 is going to be the calibrated, traceable version for line width measurements. This work is being carried out in cooperation with ISMT.

DELIVERABLES: Design and preparation of line width metrology artifact suitable for calibration on NIST and external measuring systems for certification of wafer format line width samples. Accomplishment of preliminary measurements on samples made by ISMT with the new "NISTMAG" metrology mask. 4Q 2005

ACCOMPLISHMENTS

■ **SEM Magnification Calibration Artifacts** – Samples for Reference Material 8090 have been made in the past once successfully, but later several attempts with e-beam lithography yielded

no further useful samples. We now have a new mask designed at International SEMATECH to get samples made by 193 nm UV light lithography. The use of this conventional lithography and a somewhat modified design provides a chance for large amount of good quality samples produced inexpensively. Because of this technology, it is now possible to produce the finest lines with 100 nm width and with 200 nm pitch values. The largest pitch is 1500 μm . There are a large number of 250 nm wide crosses for distortion and other measurements. Also scatterometry patterns with varying pitches will be available. The features on the conductive Si wafer will be formed from polySi material. These samples will give suitable contrast in any SEM to allow the user to set the magnification of the instrument from the smallest to the highest magnifications.

■ **SEM Performance Measurements** – After comprehensive studies and experiments a plasma-etching Si called "grass" was chosen for Reference Material 8091 (Fig. 2). This sample has 5 nm to 25 nm size structures as is illustrated in the figure below. 75 samples have been delivered to the Office of Standard Reference Materials, NIST. A sharpness standard and evaluation procedure have been developed to monitor (or compare) SEM image quality. A NIST kurtosis method, Spectel Company's user-friendly analysis system called SEM Monitor, and University of Tennessee's SMART algorithm can be used with RM 8091. An effort is underway to produce more of these samples. These samples are now available to the public.



Figure 2. The RM 8091 Sharpness Reference Material.

■ **SEM Linewidth Measurement Artifacts** –

The development of accurate modeling methods are in progress have shown excellent results on polySi samples. From a top-down view, using our high-accuracy modeling and fitting methods a cross section of the lines can be determined with few nm uncertainties and discrepancies. The match is so good that this method may be capable of eliminating the costly and destructive cross sectional SEM measurements. The candidate sample for linewidth artifact must be relevant to state-of-the-art IC technologies, should have chips on 200 mm and later 300 mm wafers with all process variation and include a meaningful focus-exposure matrix (FEM). The design and the fabrication of ISMT/NIST mask have been successfully completed. After CD-SEM measurements at ISMT, cross sectional measurements will be made at NIST. All these measurements will yield an excellent database for a decision on how to proceed with this wafer type linewidth reference sample. It is conceivable that by the end of the year 2005 the Reference Material 8120 line width samples will be available. This work is being carried out in close cooperation with ISMT.

■ **Development of High Accuracy Laser Interferometer Sample Stage for SEMs** –

The development of a very fast, very accurate laser stage measurement system facilitates a new method to enhance the image and line scan resolution of SEMs (Fig. 3). This method, allows for fast signal intensity and displacement measurements, and can report hundreds of thousands of measurement points in just a few seconds. It is possible then, to account for the stage position in almost real time with a resolution of 0.2 nm. The extent

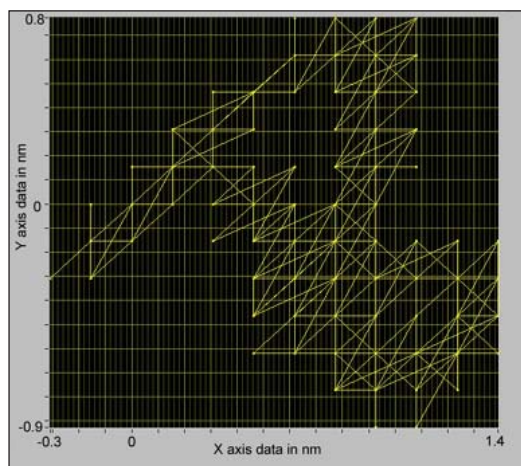


Figure 3. High-accuracy laser stage measurement locations.

and direction of the stage motion reveal important characteristics of the stage vibration and drift, and helps to minimize them. The high accuracy and speed also allow for a convenient and effective technique for diminishing these problems by correlating instantaneous position and imaging intensity. The new measurement technique gives a possibility for significantly improving SEM-based dimensional measurement quality.

■ **Development of Line Edge Roughness Metrology for Integrated Circuit Technology** –

The measurement of line-edge roughness (LER) has become an important topic in the metrology needed for the semiconductor industry. NIST has successfully developed various LER metrics and methods to make reliable and statically sound LER measurements. The findings have impact on the ITRS as they call for longer lengths for LER evaluation and on LER metrology in general because the new methods offer significantly better metrology than what was available previously. The final report of a year-long study was delivered on time to ISMT.

■ **Development of Ultra-High Resolution Nano-tip Electron Gun for CD-SEMs** –

The source diameter and the brightness of the electron beam are two of the major factors limiting the performance of CD-SEMs in the semiconductor production environment. Thus, alternative solutions to improve performance are being sought as the metrology for sub-100 nm lithography is being pushed to its limit. One possible alternative approach is the application of nano-tips as an electron source. Nano-tips, by comparison to conventional cold field offer a substantial increase in brightness (10 x to 100 x) and a large reduction (5 x to 10 x) in source size (Fig. 4). Therefore, in an optimized electron optical column, substitution of a CFE source by a nano-tip could be expected to produce:

- Higher beam currents into a spot of given size,
- Better signal-to-noise ratio and resolution, and

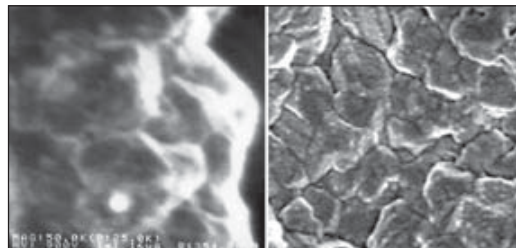


Figure 4. Resolution improvement with a nano-tip.

– Faster scan rate and better charge control.

This work has proved that nano-tips indeed improve the resolution performance of SEMs and can be used for longer periods of time.

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COLLABORATIONS

International SEMATECH, Metrology Council.

International Technology Roadmap for Semiconductors; Microscopy and Metrology Sections.

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SCANNING PROBE MICROSCOPE-BASED DIMENSIONAL METROLOGY

GOALS

Improve the measurement uncertainty of critical-dimension measurements in the semiconductor industry through improvements in SPM-based measurements. *The International Technology Roadmap for Semiconductors (ITRS)* identifies dimensional metrology as a key enabling technology for the development of next-generation integrated circuits. For example, according to the 2003 edition, the goal in 2004 for critical dimension (CD) measurement precision for isolated lines is ± 0.8 nm; this demand tightens to ± 0.4 nm by 2009. The technical focus of this project, development and implementation of scanned probe microscope instrumentation, is driven by the anticipated industry needs for reduced measurement uncertainty, particularly for existing tools such as the SEM.

CUSTOMER NEEDS

The SEM is the current tool of choice for inspection and metrology of sub-micrometer features in the semiconductor industry. SPMs possess unique capabilities, which may significantly enhance the performance of SEMs for in-line critical dimension (CD) measurements, and are also emerging as CD measurement tools in their own right. A creative strategy, which successfully harnesses the strong points of both techniques in order to reduce the measurement uncertainty of sub-micrometer features, will help NIST meet the expectations of the semiconductor industry expressed in the current *ITRS*. As is the case with SEMs, the magnification or scale of an SPM must be calibrated in order to perform accurate measurements. Although many SPMs are commercially available, appropriate calibration standards have lagged. In particular, traceable pitch/height standards with sub-micrometer pitch values are not yet available.

TECHNICAL STRATEGY

SPM development is proceeding along two parallel directions: The first direction addresses dimensional metrology of SPM specifically through two in-house research instruments, a calibrated atomic force microscope for measurement of pitch and step height and a critical dimension atomic force microscope (CD-AFM) for measurement of line width. The C-AFM has metrology traceable

to the wavelength of light for all three axes of motion and has provided calibrated pitch and height measurements for nano-scale applications. Pitch, ranging up to 20 μm has been measured with standard uncertainties (u_c) as low as ~ 0.5 nm at submicrometer scales and relative standard uncertainties of ≈ 0.1 % at the largest scales. Step height, ranging from a few nanometers up to several hundred nanometers, can be measured with u_c on the order of 0.5 % at the largest scales. Calibration procedures are being developed for the newly acquired CD-AFM for linewidth measurements. As part of the project, we have also begun to pursue research in the measurement and standardization of line edge roughness.

DELIVERABLES: Report published demonstrating new stitching method for linewidth measurements using sharpened tips. 4Q 2004

DELIVERABLES: SRM 2089, a combined pitch and height standard for AFM, released. 2Q 2005

DELIVERABLES: Report published on international Supplementary Key Comparison in Nanometrology on step height measurement. 1Q 2004

DELIVERABLES: Report published demonstrating operation of CD-AFM for measurement of 100 nm linewidth. 2Q 2005

DELIVERABLES: Report published demonstrating traceable measurements of line edge roughness using an AFM. 4Q 2004

The second direction addresses increasingly overlapping demands for dimensional control during fabrication and subsequent calibration of nanometer scale features. For this purpose we employ an SPM-based lithography technique, pioneered at NIST, to produce grating structures with linewidths of 20 nm or below. Latent oxide patterns function as masks for anisotropic wet or dry etching. We are also developing an instrument that integrates both SPM and probe station measurement capabilities whereby we are able to compare SPM-based electrical (capacitance and surface potential) and topographical measurements of active device structures simultaneous with traditional current-voltage (IV) characteristics measured with a probe station. This allows us to examine local nanoscale variations at exposed and buried interfaces of critical dimensioned features

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in order to identify processing induced variations which contribute to linewidth uncertainty in dimensional and electrical test structures.

DELIVERABLES: Development of a predictive model for SPM oxidation kinetics for optimized linewidth control of latent oxide features. Model includes influence of electronic and ionic transport on the intrinsic thickness growth and lateral spreading due to space charge.

DELIVERABLES: Investigation of anomalous features on the growth and breakdown of Group 4 metal films (Ti, Zr, Hf) and their nitrides during local oxidation.

ACCOMPLISHMENTS

■ We are participating in a series of International Supplementary Comparisons in nanometrology coordinated by the CIPM (Comité International des Poids et Mesures) CCL (Coordinating Committee for Length). Successful participation in these Comparisons will facilitate international recognition of NIST-traceable measurements of dimensional quantities important to the semiconductor industry. The results from NIST and other national measurement institutes (NMIs) for step height and grating pitch have now been published under the Mutual Recognition Arrangement (MRA) through which the NMIs recognize each other's measurement capability, thus helping to eliminate technical barriers to trade. Comparisons of 2D pitch and linewidth measurements are in the planning stage.

■ Another effort involves the study of single atomic Si steps as fundamental height standards in the sub-nanometer regime. During 2003 we submitted a draft procedure for AFM z-calibration using the single atom steps to the ASTM Subcommittee E42.14 on STM/AFM and were invited to develop a draft standard based on the procedure.

■ We are developing two techniques to measure linewidth using AFM. One involves the acquisition of paired images using a nanotube probe. The nanotube probe enables data acquisition at high resolution on each side of the line. Stitching of the paired images into one could provide an accurate measurement of the linewidth itself. An example of our preliminary measurement result is shown in Fig. 1. We currently are assessing the feasibility and uncertainties of this approach. The other technique is CD-AFM whereby the AFM probe senses the side of a line directly using an advanced sensing method. We

have recently acquired a CD-AFM for this purpose. Preliminary measurements with this instrument are shown in Fig. 2.

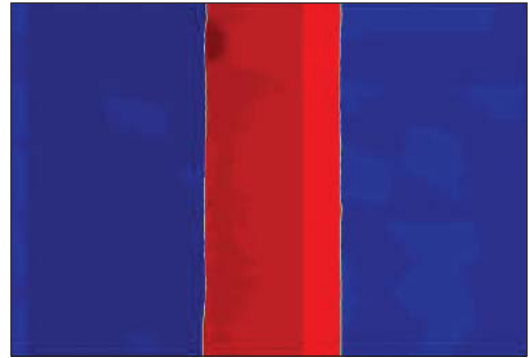


Figure 1. Stitched composite of paired topographic images of a prototype NIST linewidth standard measured by AFM using a nanotube probe. The field of view is about $2.5 \mu\text{m}$ by $2.5 \mu\text{m}$. Measurement taken by J. Fu; specimen developed by M. Cresswell and R. Allen; probe developed by C. Nguyen, ELORET/NASA Ames.

■ We also have begun working on development of AFM-based techniques for traceable measurement of physical standards for line edge roughness (LER), a potential showstopper in the ITRS.

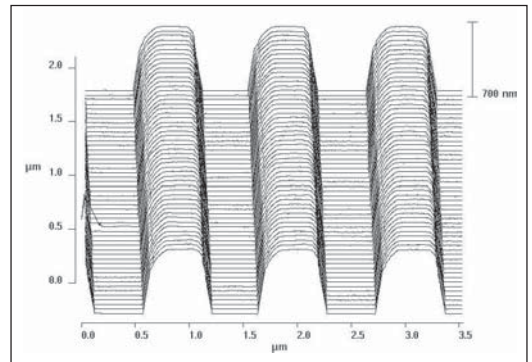


Figure 2. Preliminary AFM data of a line test structure taken with recently acquired CD-AFM. Measurements taken by J. Fu and N.G. Orji, Guest Researcher.

■ Ronald Dixon is currently on detail as NIST's first Guest Scientist at International SEMATECH. He is working with SEMATECH and industrial researchers on calibration and statistical process control techniques to establish SEMATECH's critical dimension AFM as a reference measurement system (RMS). He is also working with NIST EEEL researchers on calibration by AFM of new NIST physical standards for linewidth.

■ In the integrated SPM probe-station thrust, we have completed systematic low-noise (sub-pA) measurements of current flow during SPM oxidation of silicon substrates. Two methods of data acquisition were employed, measurements made directly as a function of voltage, humidity, and exposure time during contact-mode oxidation and those made during a (so-called) force vs. distance curve in which a biased SPM probe tip approaches, contacts, and retracts from a substrate (see Fig. 3). In the latter, electrostatic bending of the SPM cantilever can be easily modeled and the bending capacitance calculated. Electronic and ionic currents have been identified and their consequences for oxide growth and space-charge buildup during lithography have been determined. The role of the water meniscus as a conduit under noncontact oxidation has been clarified.

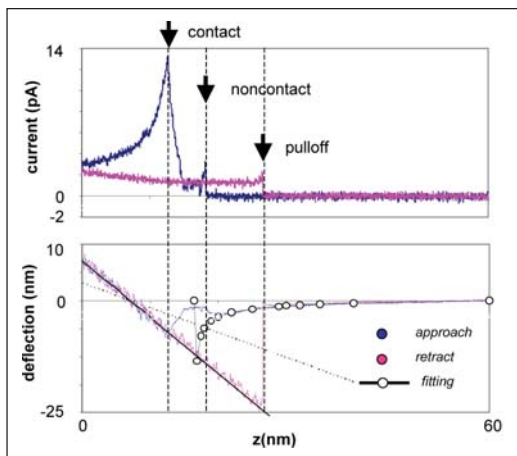


Figure 3. Simultaneous SPM current vs. distance (a) and force vs. distance (b) curves for an 18.5-V biased silicon probe tip approaching, contacting, and retracting from a silicon substrate at 65 %RH. A small 2-pA current flows through the nanometer-scale water meniscus that forms at the junction. A much larger 12-pA current flows when the tip makes hard contact with the substrate.

■ As part of the integrated SPM probe-station thrust, we have also begun studying anomalous oxide growth kinetics in the Group 4 metal films (Ti, Zr, Hf) and their nitrides. In addition to insight into potential defect behavior in alternative dielectrics, SPM kinetic studies of these films reveal new insight into ionic and electronic transport in local oxides that are quite different than in other systems (see Fig. 4).

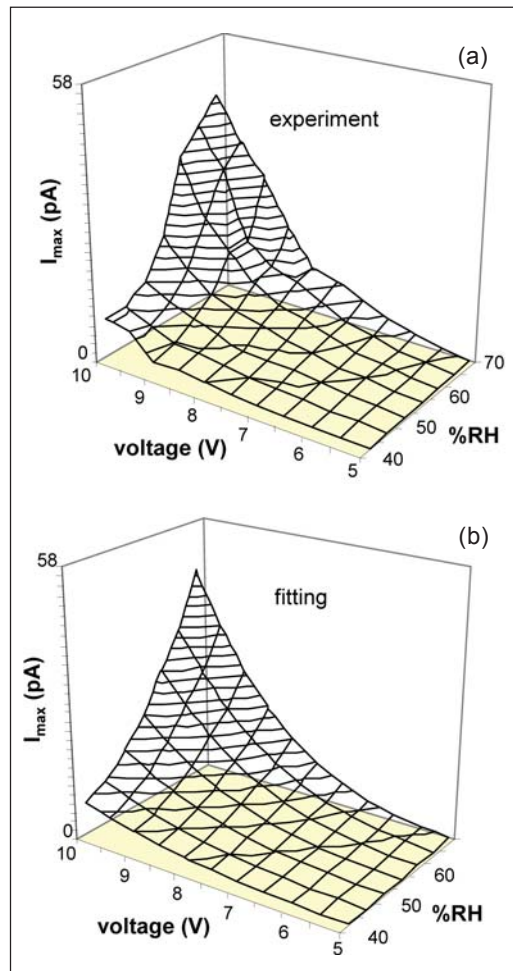


Figure 4. Experiment (a) and fitting (b) of the maximum current achieved during SPM local oxidation as a function of voltage and humidity. The SPM tip used in these experiments was coated with a PtRh metal film and the substrate was hydrogen-passivated n-type Si(100).

COLLABORATIONS

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SMALL ANGLE X-RAY-BASED DIMENSIONAL METROLOGY

GOALS

To develop a SAXS-based methodology to quickly, quantitatively, and non-destructively measure critical dimensions and feature shape with sub-nanometer resolution on production scale test samples. Quantities of interest include critical dimension, sidewall angle, and statistical deviations across large areas. Of particular focus is delivering a technique capable of routine measurement of pattern shape, including critical dimension, sidewall angle, line width fluctuations, and line edge roughness, in dense high aspect ratio patterns possessing sub-50 nm critical dimensions. In addition to addressing the metrological needs of future technology nodes, the sub-Angstrom wavelengths utilized by SAXS based measurements offer the possibility of calibration and testing of current metrological tools based on light scatterometry, SEM, and AFM.

CUSTOMER NEEDS

The drive to reduce feature sizes to the sub-100 nm regime outlined by the ISMT Roadmap continues to challenge metrology techniques for pattern characterization. As pattern sizes decrease, existing techniques such as CD-SEM face significant technical hurdles in imaging quantities such as Line Edge Roughness (LER). Emerging metrologies based on techniques such as atomic force microscopy are still being evaluated, providing a lack of clear definition in suitable metrology for standardized measurements of both organic and inorganic structures. To address these issues, NIST is evaluating the potential application of X-ray scattering as a metrology tool for both process development and the production of standards for industrially practiced metrologies such as CD-SEM.

TECHNICAL STRATEGY

1. Exposure systems capable of sub-50 nm patterning are expected by 2005, requiring control of CD on the level of nanometers and in some cases sub-nanometer precision. These requirements will challenge traditional methods including CD-SEM and light scatterometry. We are developing a transmission scattering based method capable of angstrom level precision in critical dimension

evaluation over large (50 μm x 50 μm) arrays of periodic structures (see Fig. 1). In contrast to light scatterometry, SAXS is performed in transmission (see schematic below) using a sub-Angstrom wavelength. With a wavelength more than an order of magnitude smaller than the pattern size, the patterns are characterized using methods employed in crystallographic diffraction. The high energy of the X-ray allows the beam to pass through a production quality silicon wafer, and is therefore amenable to process line characterization. As with light scatterometry, the measurements are performed in ambient conditions, minimizing time required for sample preparation. The current capabilities of commercially available X-ray sources and detectors suggest that the technique is portable to a laboratory scale device capable of high precision measurements.

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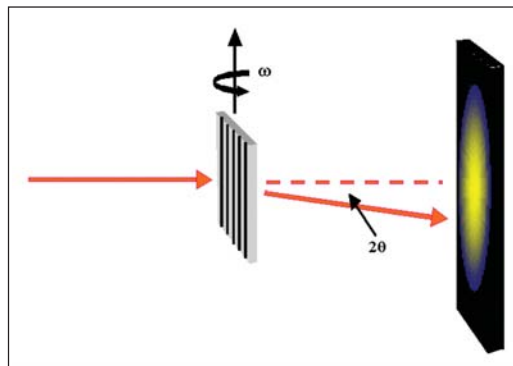


Figure 1. Schematic of the SAXS transmission geometry. Shown is the X-ray beam (solid line) as it passes through the patterned sample and scattered at an angle 2θ . For a precisely aligned sample with known composition, a 3-d lineshape is obtained in one transmission measurement. Unknown samples can also be characterized through measurements at a variety of sample angles.

While measurements and technique development will still continue to rely on synchrotron technology for the coming year, NIST has committed to develop the world's first laboratory scale CD-SAXS device. A primary goal of this year will be the specification, purchase, construction and testing of the laboratory scale prototype.

DELIVERABLES: Develop specifications for a laboratory sized CD-SAXS prototype based on current commercially available X-ray components. 1Q 2004.

DELIVERABLES: Purchase and construct world's first device devoted primarily to development of CD-SAXS on a laboratory scale. 4Q 2004

2. Characterization of pattern quality includes shape factors indicating the slope of the line edge and curvature. Using the above protocol for scattering, measurements taken at a series of angles of incidence allows the reconstruction of the line shape in a manner similar to microscopic tomography. We have performed an initial set of tests using multiple angles on a test grating and determined an ability to measure sidewall angle to within 1°. Ongoing analysis and technique refinement will provide additional shape factors, allowing determination of more complex shape information such as sidewall curvature. In addition to a "high speed," model dependent characterization performed in a single measurement, a second method will be developed based on measurements at multiple sample orientations. This slower method will provide a more precise picture of the entire pattern cross section analogous to cross sectional SEM in a non-destructive and model independent manner. In the current technology node, this more extensive measurement will be critical to the evaluation of light scatterometer models for line shape, while providing a general capability to measure a pattern of arbitrary cross section in future technology nodes. Specific cross sections being studied include simple trapezoids, trapezoids with rounded corners, and double trapezoids possessing a second sidewall angle due to T-topping or footing.

DELIVERABLES: Provide measurements of line shape in terms of simple trapezoidal model for grating patterns. 2Q 2004

3. Current Line Edge Roughness (LER) and CD specification of LER in CD budgets requires high precision metrology for both quality control by vendors as well as quality assessment by customers. Metrologies such as CD-SEM, a top down technique, measure qualitatively different quantities compared to that of light scatterometry and AFM. Our approach is to provide metrology of sidewall roughness, where sidewall roughness is defined by deviations from the average sidewall plane on length scales smaller than the CD. These measurements can then be connected to varying definitions of LER through cross measurement of samples with, for instance, CD-SEM. In the case of photoresists, we are employing AFM to provide the appropriate wavevector range, or frequency spectrum, over which correlations exist. These data are being used to develop the appro-

priate neutron and X-ray optical configurations for sidewall roughness characterization. Our goal is to produce techniques applicable to a wide range of roughness types and size scales.

DELIVERABLES: Provide outline of specific types of LER and their expected effects in the CD-SAXS spectrum. 1Q 2004

DELIVERABLES: Provide first model of LER for CD-SAXS describing the effects of correlated roughness between patterns. 3Q 2004

4. As circuit designs increase in complexity, next generation metrologies require capabilities to characterize patterns that deviate substantially from the often employed line/space pattern. As an example, a capability to precisely characterize dense arrays of high aspect ratio vias non-destructively is an outstanding need even in the current technology node. The use of a beam 2-D collimated beam and a 2-D detector in the CD-SAXS technique provides a natural capability to characterize patterns such as vias, posts, and via pads. While the capability to observe such structures has previously been demonstrated, routine analysis of this class of structures has not been achieved. Using a series of patterns including vias of diameter less than 60 nm, we are developing specific experimental protocols, extending those developed for line/space patterns, to provide a data set capable of describing a precise pattern shape in 2-D arrays of patterns.

DELIVERABLES: Provide measurements and model describing the measurement of 2-D arrays of 60 nm via patterns. 3Q 2004

DELIVERABLES: Provide experimental protocols for high precision measurements of 2-D arrays of arbitrary pattern shapes. 4Q 2004

ACCOMPLISHMENTS

■ We have provided the first measurements of sidewall angle using small angle X-ray scattering (SAXS). Using a series of photoresist gratings produced at the IBM T. J. Watson Research Center (Q. Lin), CD-SAXS was performed using at the Advanced Photon Source (Argonne National Laboratory) to measure photoresist patterns with well defined sidewall angles. The protocol involves measurements of the sample over 20 degrees of incident angles, and reconstructing the fourier representation of the pattern cross section. For a pattern with trapezoidal cross section, ridges of intensity propagate at twice the

sidewall angle (see Fig. 2). The existence of the ridges is a model independent check on the validity of the trapezoidal model, while different shapes, such as a T-topped line, will produce different scattering patterns. The protocol is therefore generalizable to a wide class of pattern shapes.

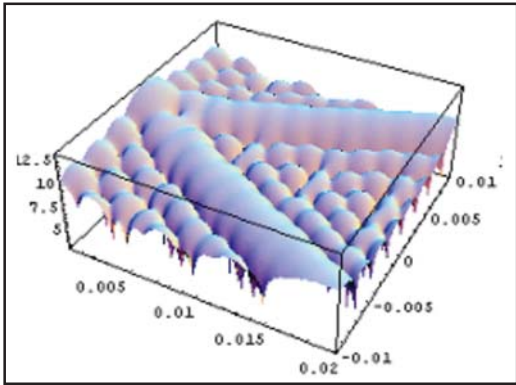


Figure 2. Model of the expected scattering in the plane parallel to the line cross section. Calculation assumes a trapezoidal cross section. The sidewall angle is obtained by the half angle between the prominent ridges.

■ Demonstrated a capability to measure correlated fluctuations in line edge position using CD-SAXS measurements of a series of line/space patterns in a “193nm” photoresist produced at IBM T. J. Watson Research Center (A. Mahorowala) (see Fig. 3). These samples are believed to possess systematic, small shifts in the pattern. These shifts provide insight into measurements of line edge roughness (LER) where the roughness is highly correlated. The resulting data shows distinct streaks of intensity emanating from the diffraction peaks, particularly strong in the lower order peaks. These represent the first evidence of a capability of CD-SAXS to

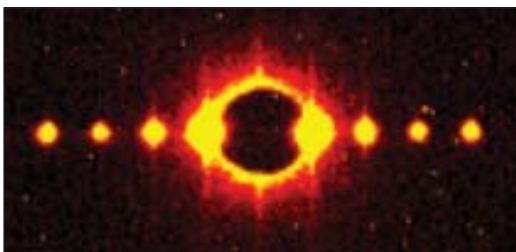


Figure 3. Detector image of a 193nm photoresist of an approximately 1:1 line/space pattern with a total repeat of 240 nm. In addition to the typical diffraction spots characterizing pitch and linewidth, streaks of intensity are observed emanating from the diffraction peaks. The streaks are a result of correlated roughness.

measure different types of defects related to the overall line edge roughness.

■ Demonstrated a capability to measure a dense array of vias where the diameter of the vias are less than 60 nm (see Fig. 4). Vias were etched into a plastic substrate at the IBM Almaden research center (M. Sanchez). The result demonstrates the capability of CD-SAXS to probe dense vias of sub-100 nm size. Ongoing work will attempt to provide a protocol for the evaluation of the full 3-D via shape as demonstrated for line/space patterns.

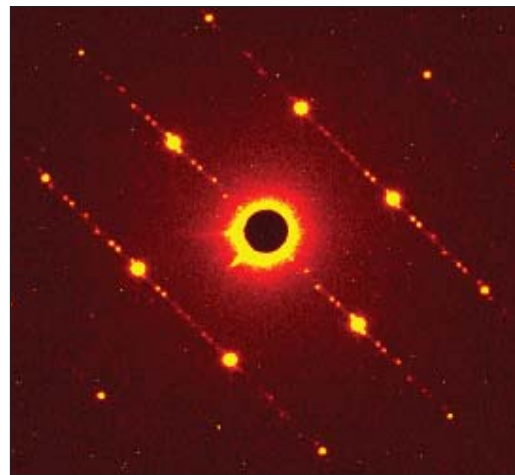


Figure 4. CD-SAXS detector image resulting from a dense array of 60 nm vias. The array of diffraction patterns suggests an approximately hexagonal packing of the vias.

COLLABORATIONS

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IBM Almaden, Martha Sanchez, Characterization of sub-50 nm structures.

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ELECTRICAL-BASED DIMENSIONAL METROLOGY AND SINGLE CRYSTAL CRITICAL DIMENSION ARTIFACT DEVELOPMENT

GOALS

Develop test-structure-based electrical metrology methods and related reference materials with emphasis on linewidth metrology tool calibration and parameter extraction for interconnect modeling and materials characterization; contribute to standards organizations supporting the development of metrology standards for the semiconductor industry; target the specific near-term goal of fabricating a quantity of reference-features with nominal critical dimensions (CDs) in the range 70 nm to 100 nm and having CD uncertainties less than 5 nm by May 2004.

CUSTOMER NEEDS

The Semiconductor Industry Association's (SIA's) International Technology Roadmap for Semiconductors (*ITRS*) states that it is critically important to have suitable reference materials for lithography support available when on-wafer measurements are made as a new technology generation in integrated circuit (IC) manufacturing is introduced, and particularly during development of advanced materials and process tools. Each generation of ICs is characterized by the transistor gate length whose control to specifications during IC fabrication is a primary determinant of manufacturing success. The SIA projects the decrease of gate linewidths used in state-of-the-art IC manufacturing from present levels to below 70 nm in the near future. Scanning electron microscopes (SEMs) and other systems used for traditional linewidth metrology exhibit measurement uncertainties exceeding *ITRS* specifications for these applications. It is widely believed that these uncertainties can be at least partially managed through the use of reference materials with linewidths traceable to nanometer-level uncertainties. Until now, such reference materials have been unavailable because the technology needed for their fabrication and certification has not been available.

It is also widely believed that the usefulness of SEM metrology for monitoring wafers in advanced development and production may become inadequate at some future IC generation. Thus, there exists a need for new methodology to meet future metrology requirements.

TECHNICAL STRATEGY

The technology that the project staff have developed for fabricating linewidth and overlay reference materials is known as the Single-Crystal CD Reference-Material (SCCDRM) implementation. Patterning with lattice-plane selective etches of the kind used in silicon micro-machining provides reference features with quasi-atomically planar sidewalls over local length segments of the reference feature, typically extending to several micrometers. This unique attribute is highly desirable for the intended applications, particularly if the quasi-atomically planar sidewall smoothness can be further extended to reference-feature segment lengths of up to 2 micrometers. Essential elements of the technology implementation include starting silicon wafers having a (110) orientation; alignment of the reference features to specific lattice vectors; and lithographic patterning with lattice-plane selective etches of the kind used in silicon micro-machining.

The traceability path for dimensional certification originates with High-Resolution Transmission Electron Microscopy (HRTEM) imaging. This method provides nanometer-level accuracy, but is totally destructive and thus is not practical for supplying reference features to end users. The project's traceability strategy now features state-of-the-art Atomic-Force Microscopy (AFM) as a transfer metrology. Since use of the available Veeco Dimension X3D AFM tool is also very costly due to the heavy demand of other metrology applications, an elaborate candidate-reference-feature selection protocol has been established. Multiple reference features on a large set of as-patterned chips are identified initially by high-power optical inspection. This checks primarily for reference-feature continuity, cosmetics, and apparent uniformity of the narrowest-drawn features on the test chip that are replicated by the i-line imaging process. Drawn feature linewidths range from 350 nm to 600 nm and the "process bias" typically decreases these to replicated-CDs of between 50 nm and 300 nm. The "best" 10% of the features passing optical inspection, and having estimated replicated CDs in the range 50 nm to 200 nm, are then SEM-imaged at 20KX. Profiles of the CDs of the captured top-down SEM

Technical Contact:

Michael W. Cresswell

I would like to thank you and NIST for your pioneering work on silicon pocket wafer technology. We have now incorporated this technology in one of our products. We also regard very highly your work on the single crystal linewidth standard. We see this as the first and only attempt by anyone in the world to produce a linewidth standard traceable to the fundamental units of measure, in the sub-100 nm range, for use in the semiconductor industry.

This work is of technical and economic importance to the semiconductor industry, because the ability to correctly size ever smaller lateral dimensions on silicon substrates is key to the manufacturing yield of silicon chips.

We look forward to a continuing technical relationship between VLSI Standards and NIST."

Marco Tortonese, Ph.D.,
Engineering Manager,
VLSI Standards, Inc.

images are then extracted from them at 25-nm pitch. The measurements are transferred to a custom-designed database which is then electronically interrogated to identify a sets of chips, and the reference-features on them, that are the most uniform at the narrower CDs – typically less than 150 nm. Candidate reference-features so identified on chip are CD-profiled by AFM. The AFM CD-profiles of several features on each chip are examined and the chips are then partitioned into a *calibration* sub-set and a *product* subset.

Scatterometer gratings and electrical-CD test structures are among the various patterns on the test chip now being used for CD reference-feature fabrication, Fig. 1. However, the subject of all chip- and feature-selection criteria for transfer metrology has recently been some special structures called “HRTEM” targets. There are several hundred of these on each chip. The one on each chip of the calibration sub-set that is identified on the basis of AFM metrology allows the capture of six HRTEM images in a single dual-beam FIB-and-thinning operation, Fig. 2a and Fig. 2b. Since such operations are very costly, this capability is financially advantageous. Moreover, since the features on each target are designed such that they are systematically staggered in CD by increments between 30 nm and 50 nm, HRTEM inspection of a single target enables the generation of an entire 6-point calibration curve which is the basis of calibrating the product chips for the end-user community, Fig. 3.

An important measure of the progress and success of the project is the level of uncertainty attributed to the product CD reference features. The units that were delivered to International SEMATECH (ISMT) previously, per contractual arrangements, typically exhibited in excess of 14 nm uncertainty which was attributed to average

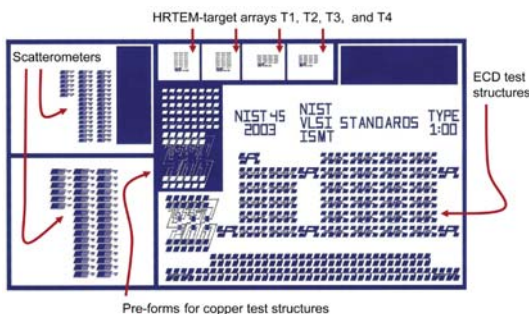


Figure 1. Structure groupings on upper section of NIST45 SCCDRM Chip including HRTEM-target arrays T1, T2, T3, and T4.

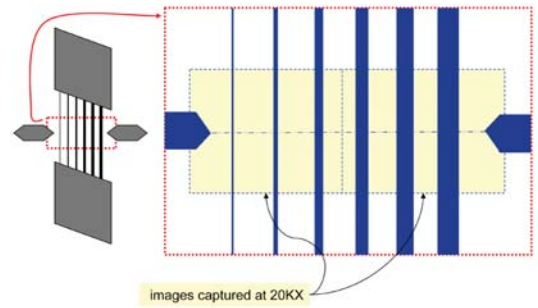


Figure 2a. The new HRTEM-Target Layout provides images from six features having different drawn linewidths from a single FIB cut at precisely known locations along the segment lengths.

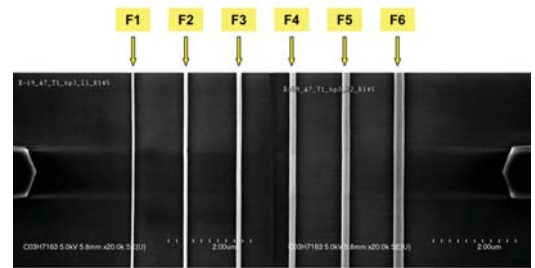


Figure 2b. Composite of two 20KX SEM images of an HRTEM Target with annotated feature numbers. The FIB cut is made between the extremities of the markers on either side of the reference-feature grid.

CD over several micrometers of reference feature. This macro uncertainty level is not necessarily that of interest to the user who needs a value applicable to an order-of-magnitude less segment length. In addition, the cited uncertainty levels were considered to be four to five times higher than what is desired for the road-map out years. Therefore, the main goal of the project during the current year has been reducing the uncertainty to 5 nm or better over reference-feature micro-segment lengths of the order of several tens of nanometers.

To facilitate achieving the stated goal, the current year’s effort has focused on reducing the macroscopic variations of the physical CDs of the reference features by refinements to the starting-material specifications and to the wafer-fabrication process. The data-base implementation previously referenced has tracked progress on this front during the last year. The uniformity of fabricated reference features with a nominal 100-nm dimension has improved from the 6 nm per micron level to less than 2 nm per micron of reference-feature segment-length. On this basis, we anticipate that we will be assigning CD-uncertainties between 3nm and 5 nm to the product

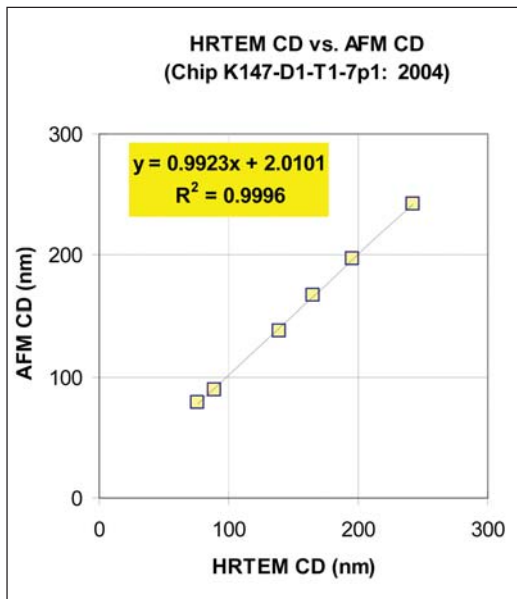


Figure 3. Example of AFM Transfer-Calibration from a single HRTEM target.

chips when they are distributed in the July – August 2004 time-frame. The HRTEM calibration imaging for these chips has been completed. The technical strategy has to be responsive to industry’s requirement for reference materials to have the physical properties of standard 200 mm wafers. Since 200 mm (110) starting material is virtually unobtainable at an acceptable cost, this project’s technical strategy has been to dice each 150 mm (110) wafer after lithography and to mount the separate chips in micro-machined standard 200 mm wafers to accommodate the product reference-feature chips. The result is that finished units are rendered metrology-tool-compatible at an acceptable cost. The chips to be delivered in May 2004 are presently being mounted in 200-mm carrier wafers for distribution. The entire fabrication and certification process is planned to be transferred to a commercial standards vendor.

In the current year, project researchers have set up a chip-level reference-material patterning facility at the ISMT facility in Austin. One leading motivation for this effort was the ready availability of SEM imaging facilities having a capability to inspect the high volume of reference-material chips being generated by processing variations. The latter are directed at reducing single-feature CD variation to below the several-nanometer level. In addition, qualified operating staff were also made generously available. ISMT has been contributing 20 to 40 hours of SEM machine time per week, with operators. In addition, the project

has access to a state-of-the-art dual-beam focused ion beam (FIB) inspection tool and operator staff for necessary cross section measurements on an as-needed basis.

A second motivation for setting up the reference-material patterning facility at the ISMT facility in Austin was essential proximity to the Advanced Technology Development Facility (ATDF), which is being operated by a NIST assignee from the Manufacturing Engineering Laboratory in ISMT’s clean room. Our current year’s CD-variation control effort has depended exclusively on this one-of-a-kind world-class installation and the unique skills of the NIST assignee. As stated previously, the atomic force microscope (AFM) facility is intended also to serve as an alternative transfer-calibration tool.

DELIVERABLES: Design a new test chip for reference-feature patterning with multiple instances of novel targets with different drawn line widths that substantially reduces the cost of HRTEM imaging. Provide new navigational tools to facilitate coordinate referencing along the entire lengths of all reference features. Include a new segmentation photolithography-level that partitions reference features into multiple shorter segments after patterning without adversely affecting essential reference feature properties such as sidewall planarity and provide all necessary on-chip navigational aids to facilitate identification of segments so produced under high-power imaging. 1Q 2004

DELIVERABLES: Develop substrate pre-patterning processing and patterning processes capable of replicating reference features in Silicon-on-Insulator (SOI) with nominal CDs in the range 70 nm to 150 nm and having uncertainties less than 5 nanometers over reference-feature segment-lengths extending to up to 2 micrometers. Patterning processes are to include procedures for removing particles and precipitates having low-single nanometer dimensions that are typically produced by the patterning-process chemistry. In addition, develop decontamination procedures for removing organic side-wall residues that are not detectable by electron-beam imaging but adversely affect AFM transfer metrology. 1Q 2004

DELIVERABLES: Identify reference features on a set of over 1000 chips that are judged to have potential for meeting nominal-CD and uncertainty requirements on the basis of CD-profile extraction 25-nm pitch from high-resolution (4-Mbyte-plus) SEM images captured at 20KX. Design a database in which to insert all extracted CD-data to enable its interrogation in order to rank all captured SEM images according to desired dimensional properties at the chip, target, and/or feature levels. 2Q 2004

DELIVERABLES: Select reference features on a sub-set of 30 chips that are judged to have superior potential for meeting nominal-CD and uncertainty requirements on the basis of AFM measurements made at 25-nm pitch. Select a further sub-set of 3 chips to be submitted for HRTEM imaging to establish an 18-point calibration curve for referencing AFM measurements on the other 27 chips to the lattice-spacing-based absolute measurements. Select 10 of the 27 remaining chips for assembly into carriers wafers for delivery to ISMT client. 3Q 2004

DELIVERABLES: Develop a protocol for extracting consistent HRTEM-CD measurements by multiple observers from the 18 features that were submitted for imaging. Reconcile the HRTEM and AFM measurements of each respective feature on a single calibration curve for the purpose of assigning nominal CDs and their uncertainties to the 10 chips that will be assembled into carrier wafers for delivery to ISMT client. 4Q 2004

DELIVERABLES: Fabricate scatterometry targets using the single-crystal reference-material implementation. Invite industry partners to evaluate performance. 4Q 2004

ACCOMPLISHMENTS

■ *A selection of SIMOX (Separation by Implantation of Oxygen (110) 150 mm wafers was procured, pre-processed by ion implantation and annealing, and delivered to VLSI Standards for i-line lithography. After lithography the wafers with patterned hard-mask films were delivered to NIST for dicing prior to being shipped to ISMT for patterning at the chip level and optical and SEM screening. They were then returned to NIST for segmentation processing.*

■ *Project staff designed a new reference-feature chip-layout that embeds multiple-feature HRTEM targets to manage the cost of HRTEM imaging. The new NIST45 design also features multiple scatterometry targets, a sub-set of which can be electrically tested for ECD sampling, electrical CD test structures, a selection of which have reversed feature/-field-areas to enable future work in fabricating traceable CD-reference features implemented in materials other than single-crystal silicon for a new interconnect metrology-infrastructure. Navigational tools to facilitate coordinate-referencing along the entire lengths of all features was incorporated. The NIST45 design includes a new segmentation photolithography-level that partitions post-patterning reference features into multiple shorter segments after without adversely affecting preferred reference feature properties such as sidewall planarity. The segmentation process also provides on-chip navigational aids to facilitate identification of seg-*

ments under high-power imaging. A facility for patterning individual reference-feature chips was set up and operated at ISMT. Processes, such as those for cleaning, for silicon pattern-transfer and for oxide hard-mask removal at the chip level were established and documented. Chemical variables that were optimized for pattern-transfer include TMAH-etch immersion time, concentration, and temperature. The variables that were optimized for hard-mask stripping include immersion-time and BOE etch concentration and ultra-sonic agitation conditions. Comparisons between straight TMAH and hybrid TMAH/KOH etching processes were also investigated. The accomplishments listed above were applied to the identification of a hybrid TMAH/KOH etching process that reduces average line-edge roughness from last year's 6 nm to typically 3 nm on SOI material. This is a very important result because it is a prerequisite for the reduction in final-product uncertainty to levels consistent with requirements of the 70 nm node. Key contributions to achieving this result were made by the staff of the Failure-Analysis Laboratory and numerous other professional staffers at ISMT in Austin. Another procedure that was recently introduced was locating the patterning-etch reflux-system in a heated ultra-sonic tank. The reference-feature uniformity and cosmetic appearance improved with the introduction of this practice but the cause-effect relation has not been definitively established. Patterning processes that were developed and implemented included procedures for removing particles and precipitates having low-single nanometer dimensions that are typically produced by the patterning-process chemistry. In addition, decontamination procedures for removing organic side-wall residues and suspected residual water that were not detectable by electron-beam imaging but adversely affected AFM transfer metrology were developed and applied to the chips that were selected by the optical-SEM-AFM-HRTEM inspection sequence. Finally, a chip-level photo-lithography-and-etching process for segmenting the features of the scatterometer targets was developed and implemented in the NIST micro-fabrication facility.

■ *Protocols for SEM imaging and evaluation of large quantities of reference features by ISMT operators were established and implemented. The problem addressed was screening and inspecting many thousands of top-down reference-feature images for fabrication-process development purposes and for selecting reference features for AFM and HRTEM imaging, both of which are*

very costly and time-consuming operations. Reference features on a large set of chips that were judged to have potential for meeting nominal-CD and uncertainty requirements on the basis of CD-profile extraction with 25-nm pitch from high-resolution (4-Mbyte-plus) SEM images were captured at 20KX. To facilitate this critical function, a server-based database in which to insert all extracted CD-data to enable its interrogation in order to rank all captured SEM images according to desired dimensional properties at the chip, target, and/or feature levels was designed, built and implemented. In order to conduct the necessary SEM inspection below budget, a hybrid optical/SEM inspection process was implemented. In addition, image-analysis software was purchased and modified to allow off-line, large-sample, CD extraction from high-density SEM images of single features. This result was facilitated through collaboration with Hitachi Instruments, FEI, Inc., Image-Pro Company, Leeds Instrument Company, and SEM image-analysis specialists at NIST/MEL and ISMT. All extracted CD-data was archived in the database to enable its interrogation in order to rank all captured SEM images according to desired dimensional properties at the chip, target, and/or feature levels and relate these to the laboratory procedures that were used to pattern the respective chips. A protocol for extracting consistent HRTEM-CD measurements by multiple observers from 18-features that were submitted for imaging was developed. HRTEM and AFM measurements of each respective feature were incorporated into a single calibration curve for the purpose of assigning nominal CDs and their uncertainties to the 10 chips that were assembled into carrier wafers for delivery to ISMT client.

FY OUTPUTS

COLLABORATIONS

- International SEMATEC: Development of SEM imaging and AFM CD-profile extraction
- NIST ITL: Traceability statistics and procedures NIST MEL: AFM CD-profile extraction VLSI Standards: Substrate implant and anneal specifications: photo-lithography and hard-mask engineering solutions.
- Accurel Systems: Design of HRTEM targets and formulation of appropriate imaging procedures University of Edinburgh, U.K.

STANDARDS COMMITTEE PARTICIPATION

- Electrical Test Structures Task Force, Co-Chair (Richard A. Allen)
- SEMI International Standards Microlithography Committee, member (Richard A. Allen)

RECENT PUBLICATIONS

R. A. Allen, M. W. Cresswell, C. E. Murabito, W. F. Guthrie, L. W. Linholm, C. H. Ellenwood, E.H. Bogardus, "Test Structures for Referencing Electronics Linewidth Measurements to Silicon Lattice Parameters Using HRTEM," Proceedings of the 2002 ICMTS, IEEE 2002 International Conference on Microelectronic Test Structures, Apr 09-11, 2002, Cork, Ireland, pp. 13-18, (08-APR-2002).

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OPTICAL-BASED PHOTOMASK DIMENSIONAL METROLOGY

GOALS

Provide technological leadership to semiconductor and equipment manufacturers and other government agencies by developing and evaluating the methods, tools, and artifacts needed to apply optical techniques to the metrology needs of semiconductor microlithography. One specific goal is to provide the customer with the techniques and standards needed to make traceable dimensional measurements on photomasks and wafers, where appropriate, at the customer's facility. The industry focus areas of this project are primarily the optical based methods used in overlay metrology, photomask critical dimension metrology, and high-accuracy two-dimensional placement metrology.

CUSTOMER NEEDS

Tighter tolerances on CD measurements in photomask and wafer production place increasing demands on photomask linewidth accuracy. NIST has a comprehensive program to both support and advance the optical techniques needed to make these photomask critical dimension measurements.

In addition, improved two-dimensional measurement techniques and standards are needed for measuring and controlling overlay capabilities of steppers and mask-making tools under development. Overlay is listed in Table 96 of the 2001 SIA ITRS as a difficult challenge for both >65 nm and <65 nm processes. As shown in Table 99a, the problems are more acute for CD mask metrology where the industry is currently encountering metrology problems without known manufacturing solutions.

TECHNICAL STRATEGY

There are two main strategic technical components of this project.

1. The ultraviolet transmission microscope, calibration of NIST Photomask Linewidth Standard SRM 2059, and the development of calibration methods to obtain photomask linewidth measurement uncertainties adequate to meet industry needs.

The technical strategy for photomask linewidth standards is similarly divided into two segments:

- (1) instrumentation and model development and
- (2) design and calibration of standard artifacts.

An ultraviolet transmission microscope (Fig. 1) has been constructed to replace the green-light linewidth calibration system. This new instrument uses a unique geometry (a Stewart platform) as the main rigid structure and shows considerable improvement in vibration characteristics over a conventional microscope. Higher image resolution, reduced transmission of UV light through the chrome, and reduced instrument vibration will offer improved linewidth measurement uncertainties.

Technical Contact:

R. Silver
J. Potzick
T. Doiron

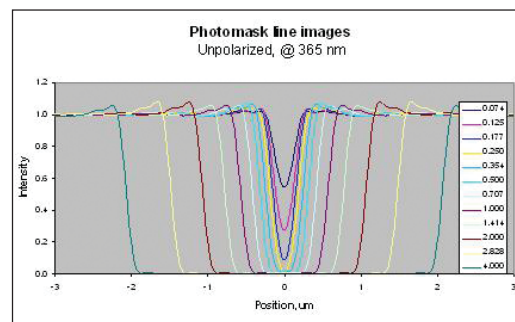


Figure 1. Modeling results for linewidth photomask samples showing CDs down to 0.25 micrometers.

NIST has supplied a substantial number of photomask linewidth standards worldwide over the past decade. Chrome-on-quartz photomasks with linewidth and pitch features in the range of $0.5 \mu\text{m}$ to $30 \mu\text{m}$ have been certified on a green light optical calibration system. Linewidth uncertainties have been reduced to 40 nm. The next generation in this line of standards is SRM 2059 (Fig. 2), printed on a standard size $6 \times 6 \times 0.25$ inch substrate with calibrated linewidths and spacings ranging from nominally $0.25 \mu\text{m}$ to $32 \mu\text{m}$, and pitch patterns from $0.5 \mu\text{m}$ to $250 \mu\text{m}$.

In response to customers' needs for more accurate photomask feature size measurements, an industry group was formed for the improvement of mask metrology through process modeling. The features on even the highest quality masks exhibit roughness and runout at the chrome edges, compromising the definition of edge and linewidth. Modeling the effects of all of the relevant feature properties in both the mask metrology process and in wafer exposure and development processes, using existing and new software tools,

can improve feature size accuracy by establishing the relationship between mask-feature metrology results and the corresponding wafer-feature sizes.

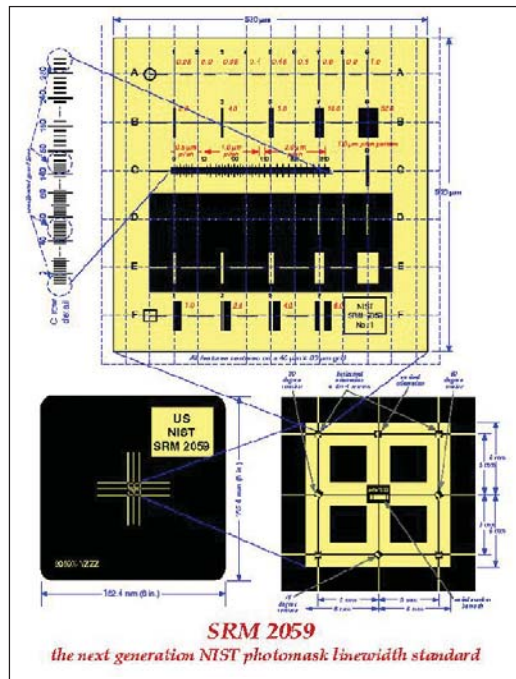


Figure 2. The new linewidth photomask standard.

DELIVERABLES: Compare and test the accuracy of new scattering models for line width evaluation in transmission. 3Q 2004.

2. The third component is the development of two-dimensional grid calibration standards and associated measurement techniques, including statistical analysis and CCD characterization as used by industry. These individual technical strategies for these components are described in more detail next.

We are approaching the problem of two-dimensional measurements from a couple of directions. The first, and most immediate, is to develop an artifact standard which can be used to bring all of the two-dimensional based inspection instruments to the same metric. This work has developed a standard grid which will be available as a NIST Standard Reference Material, # 5001, to standardize 2-D measurements in the semiconductor industry. The effort has three main parts: development of an industry consensus standard grid, measurements by state-of-the-art machines in private industry, and verification of the measurements using NIST capabilities.

Grids for the SRM have been made and final measurements are in process. Each measurement of

the grid will have data in each of at least two orientations. Rotating the grid 90° between measurements samples a number of the geometric errors of the machine. The remaining geometric sources of uncertainty are the scale and some components of the linearity of each machine axis travel.

Verification of the grid measurements is being done at NIST. The overall scale of the grid is checked with the NIST linescale interferometer, an instrument that is known to provide the most accurate 1-D measurements available in the world. Two sources of uncertainty not captured by these measurements include components of the straightness and effects of the plate bending when fixtured. Work is now focused on methods to characterize both of these effects. These studies provide a complete error budget for SRMs.

To strengthen the foundation of NIST's claims for linewidth measurement traceability and to support the BIPM *Mutual Recognition Arrangement*, NIST has become the pilot laboratory for an international intercomparison of submicrometer linewidth measurements. National metrology institutes in nine countries around the world are participating.

DELIVERABLES: Use fully automated focus and positioning control systems to improve system performance. Continue to develop comprehensive analysis capabilities for centerline and edge detection methods. 3Q 2004.

DELIVERABLES: Develop standards and new mapping software for the new Nikon 5I system. Measure with a complete uncertainty 2 dimensional grids with a fully calibrated system. 4Q 2004.

DELIVERABLES: Complete calibrations of SRM 2059 and the related documentation. Deliver the accompanying documentation to the Office of Standard Reference Materials for distribution to customers. 3Q 2003.

ACCOMPLISHMENTS

- **SRM 2800 Microscope Magnification Standard** is a standard-size microscope slide with calibrated pitch features ranging from 1 µm to 1 cm (see Fig. 3). It contains a lithographically produced chrome pitch pattern consisting of a single array of parallel lines with calibrated center-to-center spacings. It contains no linewidth structures. This SRM is intended to be used for the calibration of reticles and scales for optical or other microscopes at the user's desired magnification. The SRM may be used in either transmis-

sion or reflection mode optical microscopes, SEMs, or SPMs. Calibration is traceable to the meter through NIST Line Scale Interferometer. Fifty-six units have been calibrated and delivered to the NIST Office of Standard Reference Materials.

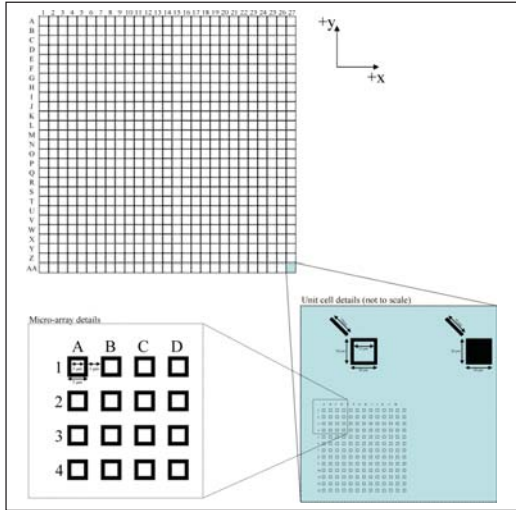


Figure 3. The two dimensional grid photomask standard, now available through the SRM office.

- NIST currently is commencing calibration for SRM 2059 Photomask Linewidth Standard, intended to enable customers to make traceable measurements of the dimensions of features on integrated circuit photomasks.

- The first set of two-dimensional grid artifacts, is known as SRM 5001, and has been received. These 6-inch photomasks have been measured on a state-of-the-art I-pro metrology system by the photomask manufacturer. This effort, to make available traceable, 6-inch feature placement standards involves a close collaboration between NIST and Photonics. The collaboration employs

the industry tool and the traceability of the NIST line scale interferometer with appropriate statistical analysis (see Fig. 4). The uncertainty budget for grid measurements has been developed and peripheral studies on various items are near completion.

- Leadership for the industry group for the improvement of mask metrology through process modeling has been transferred to ISMT.

COLLABORATIONS

ISMT, IBM, IVS Schlumberger, KLA-Tencor, Intel, Motorola, AMD and several other leading manufacturers or tool vendors.

The 14 members of The Neolithography Consortium.

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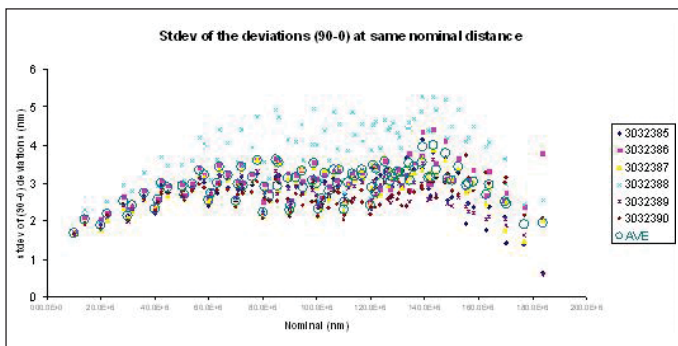
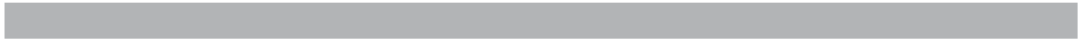


Figure 4 shows tool repeatability and mapping data for the two-dimensional mask calibration procedure.



MODEL-BASED LINEWIDTH METROLOGY

GOALS

The goal of this project is to address the metrology needs of industry, particularly the U.S. semiconductor industry, for linewidth metrology with uncertainties of a few nanometers.

CUSTOMER NEEDS

“Stack materials, surface condition, line shape and even layout in the line vicinity may affect CD-SEM waveform and, therefore, extracted line CD. These effects unless they are accurately modeled and corrected increase measurement variation and, therefore, total uncertainty of CD-SEM measurements.” International Technology Roadmap for Semiconductors, Metrology Section, p. 7 (2003).

“Due to the changing aspect ratios of IC features, besides the traditional lateral feature size, e.g. linewidth measurement, full three-dimensional shape measurements are gaining importance and should be available inline. Development of new metrology methods that use and take the full advantage of advanced digital image processing and analysis techniques, telepresence, and networked measurement tools will be needed to meet the requirements of near future IC technologies.” International Technology Roadmap for Semiconductors, Metrology Section, p. 6 (2003).

“...the exponential rise in value of each nanometer, as nominal gate dimensions shrink, can be estimated... Under these assumptions, the value of CD control for the 180 nm generation of microprocessors exceeds \$10 per nanometer.” C.P. Ausschnitt and M. E. Lagus, IBM Advanced Semiconductor Technology Center, Proc. SPIE Vol. 3332, p. 212 (1998).

A feature's width is one of its fundamental dimensional characteristics. Width measurement is important in a number of industries including the semiconductor electronics industry, which had approximately \$166 billion in worldwide sales in 2003.¹ As a measure of its importance in that industry, consider that the term “critical dimension” or “CD” is used there nearly interchangeably with “linewidth,” and semiconductor device generations are known according to the characteristic width of the features, as in “the 90 nm generation.”

Existing linewidth standards are optical photo-mask standards, the minimum linewidth of which is 0.25 μm with a combined expanded uncertainty of ≈ 10 nm (coverage factor 2). To support present and future semiconductor technologies, industry needs to measure gate widths with total uncertainties, as identified in the International Technology Roadmap for Semiconductors (ITRS), of less than 3 nm and with measurement repeatabilities of better than 0.6 nm. Neither NIST nor any other national laboratory presently offers a wafer linewidth measurement service or SRM with uncertainty at this level.

A line's width must generally be determined from its image. However, the image is not an exact replica of the line. The scanning electron microscope (SEM), scanning probe microscope (SPM), and optical microscope all have image artifacts that are important at the relevant size scales. Physical linewidth determination therefore requires modeling of the probe/sample interaction in order to correct image artifacts and identify edge locations. Barriers to accurate linewidth determination include inadequate confidence in existing models, the complexity and consequent expense of using some models, inadequately quantified methods divergence, and ignorance of best measurement practices.

TECHNICAL STRATEGY

The scope of the model-based linewidth metrology project includes the development and improvement of computational models to simulate the artifacts introduced by measuring instruments, inversion of these models (to the extent possible) to deduce the sample geometry that produced a measured image, validation of models by appropriate experiments, development and testing of measurement processes that provide the necessary inputs for model-based deduction of sample width and shape, estimation of uncertainties for the measurement process, assistance to industry linewidth measurement by communication of best practices, and laying of the necessary research groundwork for a future linewidth and/or line shape Standard Reference Material.

Technical Contact:
John Villarrubia

“[The] theoretical work on the behavior of the probe-sample interaction has had a profound influence on our ability to quantitatively analyze probe microscope images.”

*Joseph Griffith, Bell Labs,
Lucent Technologies*

“The modeling work ... for electrical CD, AFM, and CDSEM is of value to us ... The current crisis in CD offset uncertainty may be partially answered by this work.”

*Anonymous industry
feedback to NIST*

¹ Computed using statistics compiled by the Semiconductor Industry Association.

NIST is uniquely positioned to execute such a project. NIST is a center of expertise in the instrument models to be tested, with optical, SEM Monte Carlo, and SPM tip and sample reconstruction models all having been developed at NIST. Also, because NIST's standards function necessitates concern for accuracy, the NIST measurement tools are among the best characterized anywhere. For example, transmission optical measurements can be made here with the same instrument used to calibrate standard reference materials, and scale calibrations can be assisted by the NIST linescale interferometer.

We have been developing a model-based library method of determining line width and line shape from top-down SEM images. The top-down measurement configuration is the one employed by industry CD-SEMs. Edge locations tell us the line's width (the "CD" desired by industry). However, lines with different sidewall geometries appear to have different widths when measured using algorithms that are standard today on CD-SEMs. That is, sidewall variation masquerades as width variation. Accordingly, our method is a model-based algorithm that explicitly accounts for the physics of the interaction of the electron beam with the sample and the effect of sidewall geometry.

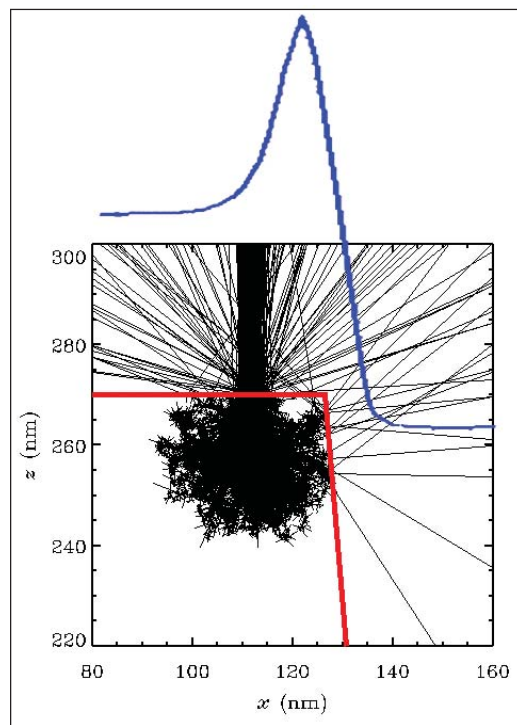


Figure 1. The SEM image may be calculated for a given edge geometry by using a Monte Carlo algorithm that follows a number of representative electron trajectories.

The method works like this: A set of parameters for describing edge geometry is chosen. These parameters might be, for example, sidewall angle and corner radius. For a given set of parameter values, the expected image is calculated using a Monte Carlo algorithm that simulates electron trajectories (Fig. 1). This calculation is repeated for other choices of edge parameters at discrete intervals representative of the range of shapes that one is likely to encounter in a measurement. The resulting actual shape / calculated image pairs form a library, or database. To determine the shape of an unknown sample, its measured image is compared to computed images in the database to find the closest match. The corresponding line shape is assigned to the unknown (Fig. 2). In practice there may be more than two parameters, and the library may be interpolated.

In recent years we have reported encouraging results for this method. Results for polycrystalline Si are shown in Fig. 3a and Fig. 3b. Measurements like these on poly-Si are industrially relevant after etch, and are also important as a prerequisite for the calibration of wafer linewidth standards. Such standards are likely to be fabricated in Si rather than resist because resist geometry is too unstable for a long-term standard. However, a capability to measure resist would also be industrially useful for pre-etch process control measurements. The effects of contamination, charging, and shrinkage when imaging nonconducting resists may result in poorer accuracy for resist samples than for Si

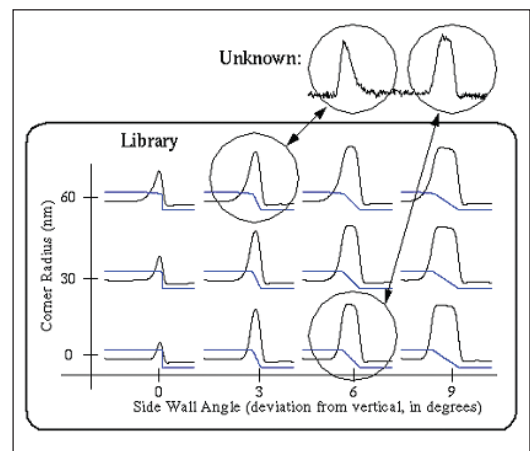


Figure 2. Concept of metrology using a model-based library. The measured left and right edges are compared to a library of images calculated for a range of possible edge shapes. The shape of the unknown structure that gave rise to the measured image is assigned to be the line shape corresponding to the image that most closely matches the measured one.

samples. Results for a UV resist were obtained in 2003 and are shown in Fig. 3c. One manufacturer of CD-SEMs is now marketing a microscope, announced in summer 2003 at SEMICON WEST, with their own implementation of a MBL method. Others are investigating the method.

In 2004 we are improving the capabilities of the underlying modeling tools used to generate libraries. The existing simulation codes are limited to certain classes of sample shapes, essentially lines uniform along their length and with cross sections characterized by a small number of geometrical parameters, e.g., width, sidewall angle, and corner radius. Improvements to the modeling code would permit simulation of other industrially important sample shapes, such as rough-edged lines, contact holes, and line footing.

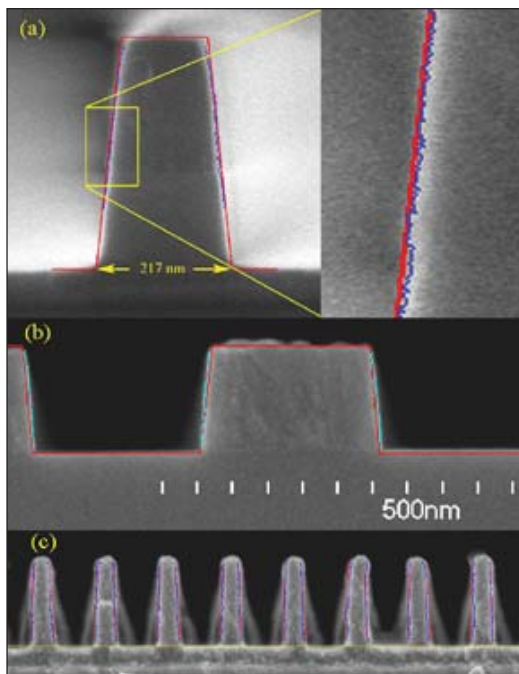


Figure 3. Agreement between MBL and cross-section measurement(s) (a) for isolated polycrystalline (“poly”) Si lines in which top-down measurements were performed with a laboratory SEM, (b) for dense poly lines measured with a commercial CD-SEM, and (c) for dense UV resist lines measured with a commercial CD-SEM. In all cases the red lines are the cross sections predicted by the MBL technique based upon top-down measurements, and the blue lines are edges assigned based upon the cross-sections.

DELIVERABLES: New more general sample shapes will be added to those capable of being simulated by NIST’s MONSEL Monte Carlo SEM modeling code. These shapes will permit extending the MBL method to line edge roughness, contact holes, and other industrially relevant samples. Results will be reported 4Q 2003.

ACCOMPLISHMENTS

- A simulation study of repeatability and bias in the CD-SEM was completed and presented at the 2003 SPIE Microlithography meeting. Among other significant findings, the paper described the relationship between microscopy resolution, precision, and measurement biases for scanning electron microscope measurements of semiconductor feature widths, calling into question assumptions implicit in the International Technology Roadmap for Semiconductors concerning the relationship between measurement resolution and repeatability. This paper received the SPIE Diana Nyssonen Memorial Best paper Award at the 2004 meeting held this February.

- All the known major manufacturers of CD-SEMs were given free access to the simulation codes. One announced a product using their own implementation of the MBL method at SEMICON West 2003. Others are investigating the technology.

- In a collaboration with International SEMATECH, test patterns were fabricated in resist and polysilicon, measured top-down in a CD-SEM, cross-sectioned, and remeasured in a laboratory SEM. MBL analysis on the resist samples was completed. Comparison with the cross section results indicated substantial agreement (see Fig. 3c), though there was some evidence of e-beam induced resist shrinkage similar to that observed by others.

COLLABORATIONS

International SEMATECH, Benjamin Bunday, Michael Bishop.

RECENT PUBLICATIONS

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“A Simulation Study of Repeatability and Bias in the CD-SEM,” J. S. Villarrubia, A. E. Vladár, and M. T. Postek, *Proc. SPIE* **5038**, 2003, pp. 138-149.

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ATOM-BASED DIMENSIONAL METROLOGY

GOALS

Provide technological leadership to semiconductor and equipment manufacturers and other government agencies by developing the methods, tools, and artifacts needed to apply leading edge, high-resolution atom-based dimensional measurement methods to meet the metrology needs of semiconductor microlithography. One specific goal is to provide the customer with the techniques and standards needed to make traceable dimensional measurements on wafers with nanometer accuracy. We are developing three-dimensional structures of controlled geometry whose dimensions can be measured and traced directly to the intrinsic crystal lattice. These samples are intended to be dimensionally stable to allow transfer to other measurement tools which can measure the artifacts with dimensions known on the nanometer scale.

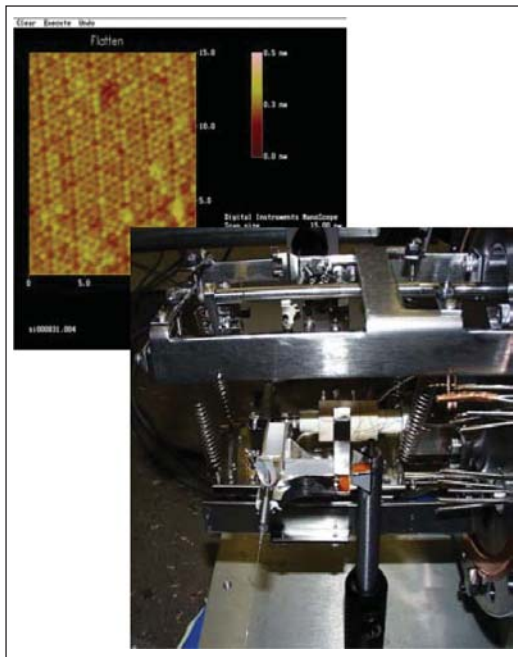


Figure 1. The atomic resolution image above was measured with a 20 picometer resolution interferometer system mounted on the UHV STM.

CUSTOMER NEEDS

NIST responds to U.S. industry needs for developing length intensive measurement capabilities and calibration standards in the nanometer scale regime. The new class of scanned probes have unparalleled resolution and offer the most promise for meeting these future needs of the micro-

electronics industry. One important application of the high-resolution SPM methods is in the development of linewidth standards whose dimensions can be measured and traced through the crystal lattice from which they are made. In addition, these high-resolution tools can be coupled directly to a new NIST-designed picometer resolution interferometer (Fig. 1).

Technical Contact:
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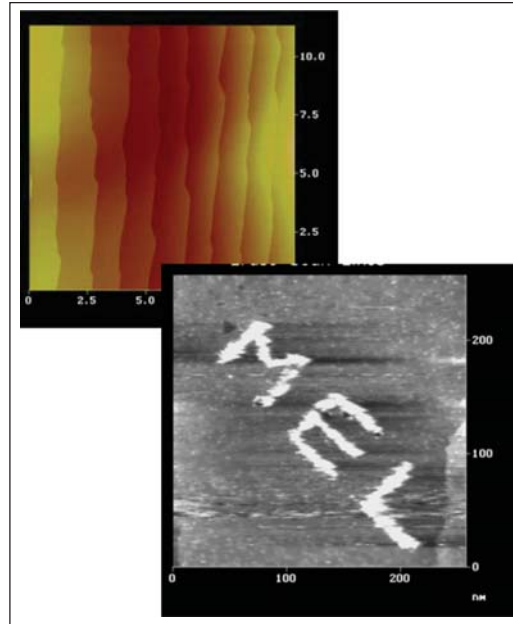


Figure 2. This recent result utilizes the atomically flat surfaces as a substrate for nanomanufacturing. The featured CDs are 10 nm and the entire lateral field of view is 250 nm. The background shows an atomically flat substrate

The work funded in this project is for the development of atom-based linewidth standards to assist in the calibration of linewidth metrology tools and the development of unique interferometry capabilities which can be used in conjunction with accurately measured tips to measure feature critical dimensions. This effort is intended to enable the accurate counting of atom spacings across a feature in a controlled environment and to subsequently transfer that artifact to other measuring instruments as a structure with atomically known dimensions.

An essential element of this project is the fabrication of test artifacts and structures for the development of high resolution imaging methods. It is imperative to enable fabrication methods for sub-10 nm sized features. Several recent developments

in optical microscopy, scatterometry and SEM metrology require test samples with critical dimensions below 10 nm. These test structures are simply not available at this time. In this project we are developing the methods for fabrication of sub-10 nm sized features and etching methods to transfer these patterns into the silicon substrates (Fig. 2).

As critical dimensions continue to shrink, the detailed atomic structure, such as edge roughness or sidewall undercut, of the features to be measured represents a larger portion of the measurement uncertainty. Furthermore, particularly with SEMs, the instrument response and the uncertainty in the edge location within an intensity pattern becomes significant issue due to the increased sensitivity to detailed elements of the edge detection model. The complexity of these models and large computer resources required for each individual computation make the idea of having samples of known geometry and width essential. This project is intended to develop samples of known geometry and atomic surface structure which will yield measurements resulting in a specific number of atoms across the line feature or between features. These samples will be measured in the UHV environment and then stabilized and subsequently transferred to other instruments (Fig. 3).

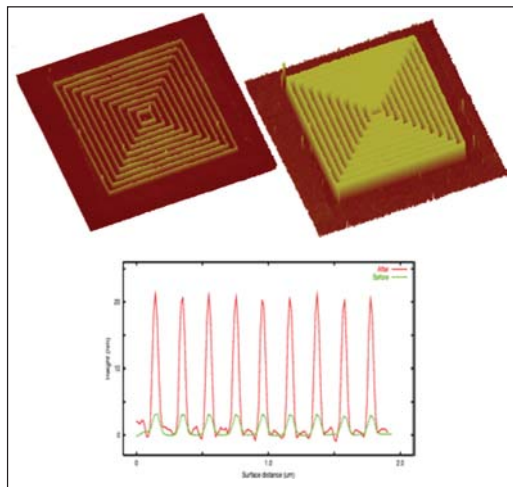


Figure 3. A demonstration of the nanofabrication process with an RIE process used to transfer the patterns into the silicon substrate.

These methods of atom counting and high-resolution interferometry, as outlined in this project description, are non-destructive and are intended to yield samples which can be measured by various instruments such as an SEM and subsequently re-measured atomically. This is a unique

and important element of this work since there are no other known methods that allow this kind of atomic dimensional measurement without being destructive. In addition, this new method opens up the possibilities of basing the measurement metric on the intrinsic crystal lattice.

TECHNICAL STRATEGY

The technical work is focused into four thrust areas.

1. The development of methods to prepare photolithographically patterned three-dimensional structures in semiconductor materials. These structures are being prepared in silicon to allow the atomic surface order which is commensurate with the underlying crystal lattice. This involves either using conventional photolithography methods for sample production or using the STM itself to fabricate very small nanometer scale features as shown in Fig. 2.

DELIVERABLES: Write features in silicon with critical dimensions smaller than 10 nm. Develop the process so it can be implemented in the M-cubed STM metrology system. Develop the process to write patterns and etch features for optical test structures. 3Q 2004.

DELIVERABLES: Work with SEMATECH and EEEL for the development of improved methods for etching nanostructures written in silicon. Use RIE etching techniques. These structures must be prepared in such materials as to allow the measurements of those features in silicon. 3Q 2004.

2. The development of techniques for the preparation of SPM tips with reproducible geometries and the direct characterization of the SPM tip geometry and dimensions on the atomic scale. These well characterized tip probes can then be used to measure the samples with photolithographically defined and canonically ordered surfaces on the sub-nanometer length scale. We are developing the SPM tip etching, field evaporation, and cleaning procedures which reliably yield stable W tips and produce atomic resolution on Si (7x7) surfaces. These tips are also useful in a collaboration with the SEM project for development as nanotips as SEM field emitters. Our tip preparation methods leave us uniquely qualified in this arena.

DELIVERABLES: Investigate nanotubes and alternative W tips as for use in high resolution imaging. 1Q 2004.

3. Focus on the development of artifacts that can be atom counted and then measured in a number

of different metrology tools such as SEM and AFM. The integrity of the line geometry, such as side wall angle, is crucial to having useful artifacts for linewidth specimens. These edge geometry requirements are not as stringent for the magnification standards since feature symmetry is the most crucial element in these measurements. The work on linewidth artifacts, therefore, is focused on reducing the process temperatures required for atomic reconstructions. We have made wet chemical processing fully operational and are currently working on preparing atomically ordered Si surfaces at significantly reduced temperatures. For sample preparation, we are utilizing the existing *in-situ* processing apparatus and techniques from the UHV STM and concentrating on the reproducible production of atomically ordered Si surfaces and Si (111) step and terrace structures (Fig. 4).

DELIVERABLES: Procure a new STM which has improved atomic scale imaging capability for atom-based dimensional metrology. This new STM should have coarse positioning to enable fabrication and metrology on the atomic scale with aligned crystallography patterns. 4Q 2003.

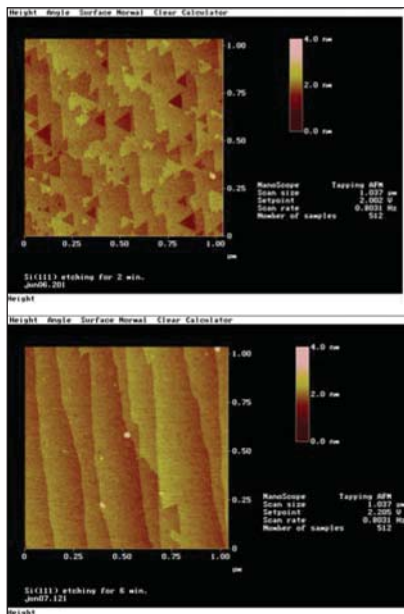


Figure 4. These are atomically flat, chemically prepared surfaces for use in atom-counting and nanomanufacturing.

4. The development of a new interferometer system intended to measure dimensions in the 20 picometer range with high accuracy. The system should also be capable of use on the STM so atomic scale measurements can be made with new

levels of accuracy. In addition we are exploring new applications of FIM calibrated tips in conjunction with the interferometry to measure CDs of leading edge, small semiconductor features.

The long term technical objective is the development of *in situ* stabilized, atomically ordered surfaces that can be transferred to other measurement instruments such as scanning electron microscopes, AFMs, or optical metrology tools. These nanometer-scale standard artifacts with atomically ordered surfaces will then act as linewidth or magnification calibration samples. These samples will have been measured either by direct atom counting or high-resolution interferometry and atomically measured tips.

ACCOMPLISHMENTS

- We have obtained atomically flat surfaces and obtained atomic order on the wet chemical prepared surfaces. The routine imaging of these surfaces on the atomic scale should be enhanced with the new STM development.

- The ability to prepare atomically sharp tips in W (111) has been demonstrated. The details of this methodology and the new models we have developed for analyzing sharpness have been published as an archived journal article.

- We have prepared two publications which give new insight into the etching process for fabricating atomically flat silicon surfaces. The results, seen in figure 4, yield a new, more comprehensive understanding of the physical processes involved in making atomically flat surfaces in silicon as required for much of the work in this project.

- The etching process has developed and demonstrated for patterns written on silicon. Patterns with features as small as 10 nm have been written in hydrogen terminated silicon surfaces with subsequent pattern transfer into the silicon substrates. A journal article is now in preparation.

- We have developed techniques for the preparation of SPM tips with reproducible geometries and the direct characterization of the SPM tip geometry and dimensions on the atomic scale. We are now applying these ideas to FIM tips used in SEM metrology (Fig. 5).

- We have measured directly the surface atom spacings based on an interferometer measurement. We have fitted our UHV STM with a high accuracy sub angstrom resolution interferometer.

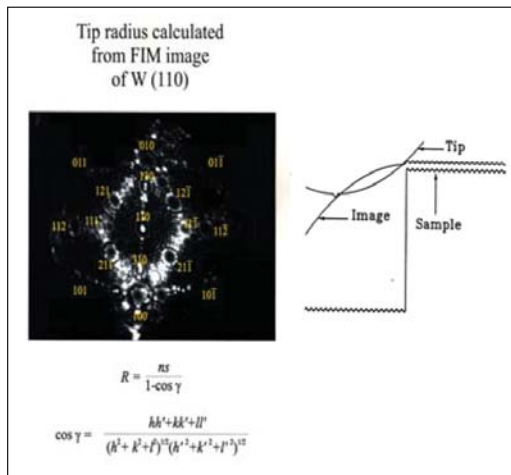


Figure 5. An FIM image showing the atomic order in a W tip is shown. The schematic on the right shows the method of atom counting or high resolution tip-based interferometry.

We have closed the loop and made atomic resolution measurements with full interferometer length basis. The successful completion of this aspect has enabled direct distance determination with simple atomic counting.

ACCOMPLISHMENT: The results for the first demonstration of direct interferometer measurements of surface atom spacings with a complete unbroken uncertainty have been published. These results were presented at the ASPE conference and SPIE to make the new interferometry methods available to the industry.

- Wafers from the NIST designed metrology reticle set have been evaluated for use in atom-based dimensional metrology. The initial evaluation is very promising and all four wafer flows yielded good product wafers. These wafers contain the prototype test structures, including a comprehensive set of critical dimension and line space arrays for general metrology purposes. The double-etched silicon multi-level features are intended to provide long term stable artifacts for calibration with the line arrays being test patterns for atom-based dimensional metrology work.

COLLABORATIONS

ISMT, IBM, University of Maryland, Dept. of Physics, University of Purdue, Dept. of Physics., George Washington University.

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J. Fu, H. Zhou, J. Kramar, S. Gonda and R. M. Silver “Dependence of Morphology on Miscut Angle for Si(111) Etched in NH₄F,” Applied Physics Letters, Vol. 82, No. 18 (2003).

R. M. Silver, S. Gonda, J. Jun, L. Howard, and C. Jensen, “Atomic Resolution Measurements with a New Tunable Diode Laser-Based Interferometer,” Optical Engineering, Vol. 43 No. 1 (Jan. 2004).

P. V. M. Rao, C. P. Jensen, and R. M. Silver “An enhanced model for STM tip geometry measured with FIM,” JVST B (Mar/Apr 2004).

WAFER-LEVEL AND OVERLAY METROLOGY

GOALS

Provide technological leadership to semiconductor and equipment manufacturers and other government agencies by developing and evaluating the methods, tools, and artifacts needed to apply optical techniques to the metrology needs of semiconductor microlithography. One specific goal is to provide the customer with the techniques and standards needed to make traceable dimensional measurements on wafers at the customer's facility. The industry focus areas of this project are primarily the optical based methods used in overlay metrology and optical, wafer level critical dimension metrology.

CUSTOMER NEEDS

Tighter tolerances on CD measurements in wafer production place increasing demands on linewidth accuracy and on overlay tolerances. NIST has a comprehensive program to both support and advance the optical techniques needed to make these overlay and photomask/wafer critical dimension measurements (see Fig. 1).

Improved two-dimensional overlay measurement techniques and standards are needed for mea-

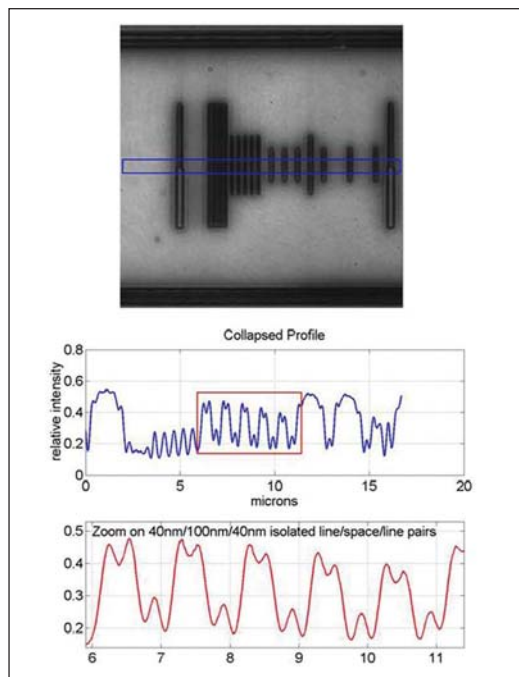


Figure 1. An optical image and profiles of sub-40 nm CD targets used in the development of new advanced high-resolution optical techniques.

suring and controlling overlay capabilities of steppers and separating out the contributions from the photomask. Overlay is listed in Table 96 of the 2001 SIA ITRS as a difficult challenge for both >65 nm and <65 nm processes. Overlay improvements have not kept pace with resolution improvements and will be inadequate for ground rules less than 65 nm. In fact, Table 98b shows that no known solutions for overlay output metrology exist beyond the 65 nm node. As shown in Table 99a, the problems are more acute for CD metrology where the industry is currently encountering metrology problems without known manufacturing solutions.

TECHNICAL STRATEGY

There are two main strategic technical components of this project.

1. The NIST's overlay metrology tool, continuous development of the tool, measurement methods to obtain uncertainties comparable to or better than the best industry overlay tools, and standards to support and calibrate these tools. The technical strategy for overlay metrology is divided into two segments: (a) instrumentation development and overlay metrology methodology, and (b) design and calibration of standard artifacts. Pattern placement and overlay of the various lithographic levels is monitored with a series of targets, each in a different plane. The overlay offset is then obtained by optical measurements with a determination of the relative target centerlines. Any misalignment in the overlay metrology system will translate into an artificial overlay offset, referred to as *tool induced shift* (TIS). Additionally, there are residual errors caused by asymmetries in the target edges or covering layers (resist) known as *wafer induced shift* (WIS) (Fig. 2).

A set of standard artifacts and procedures, under development at NIST, is designed to assist in aligning overlay measurement systems and eliminating TIS. After alignment, the tool must then be calibrated with standard artifacts to yield accurate overlay offsets. The measurement system used in this component is an optical reflection mode instrument, operational in either a bright field or confocal mode, with interferometry on three orthogonal axes also capable of monitoring the stage tilt. Additional hardware capabilities include the options to scan the sample while ac-

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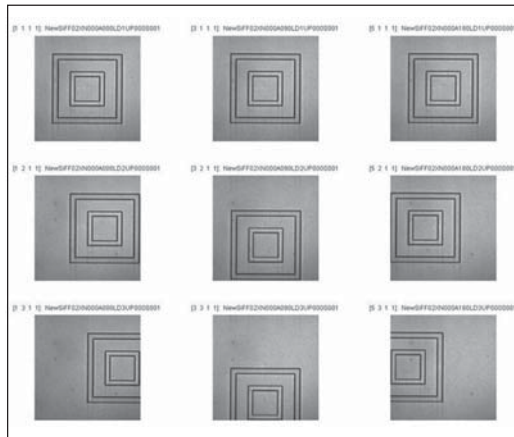


Figure 2. An example of reversal methods applied to determine WIS and the asymmetry of the target itself.

quiring data with an on-axis photometer or high resolution image capture with a full field CCD data acquisition system. This latter mode has enabled a detailed study of CCD array performance and characterization. In this work, several CCD acquisition systems are being evaluated and improved edge detection and CCD array calibration procedures are being developed. These same methods for two-dimensional CCD array analysis are now being applied to optics analysis. Additional investigation of CCD measurement problems are focused on the detailed response of typical CCD camera light sensors.

WIS-free standard overlay artifacts have been fabricated in 200 mm and 300 mm wafers. These overlay artifacts are for the calibration of industrial optical overlay tools. The artifacts have been fabricated in single crystal silicon and provide an array of etched silicon three-dimensional targets with additional targets fabricated using industry standard process levels. These wafers additionally have an extensive set of characterization targets and structures developed in close collaboration with SEMATECH and several leading semiconductor manufacturers, for example, Fig. 3 and Fig. 4.

DELIVERABLES: Finalize the qualification numbers on the overlay microscope, optics, and the x-y metrology stage. Complete the final uncertainties and tabulate the combined uncertainty value. The current, most difficult challenge is the qualification for calibration of complex overlay target process levels such as contact-to-poly. 2Q 2004

DELIVERABLES: Use the new metrology reticles from the ISMT collaboration to make leading edge overlay calibration targets/wafers. Work with industry partners to determine designs and which

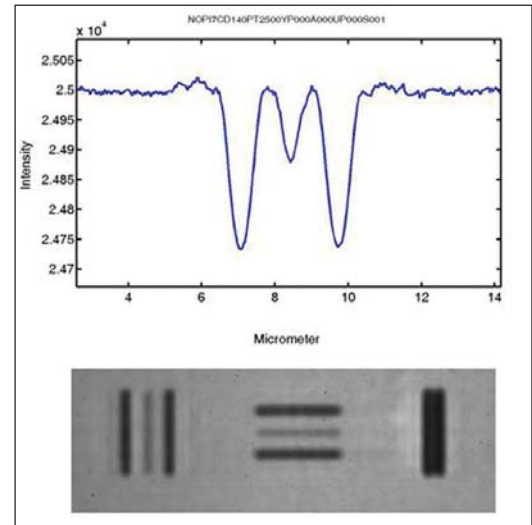


Figure 3. The new in-chip overlay targets.

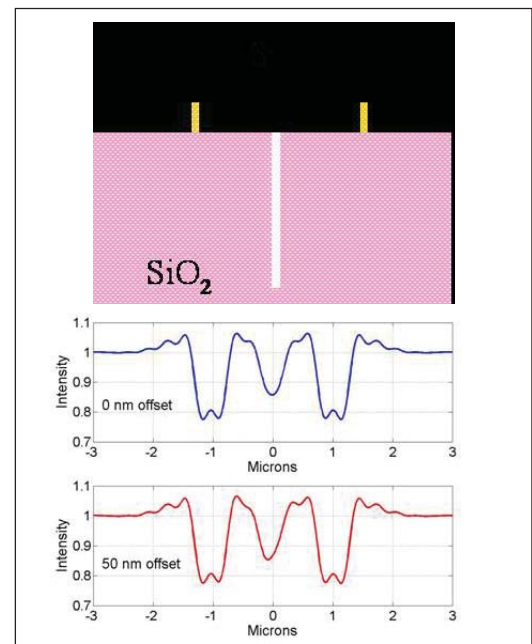


Figure 4. New proposed overlay targets, which occupy less than 2 micron x 2 microns in total space. This is designed to be an in chip target.

levels are most appropriate for the silicon fabrication phase. Calibrate these overlay standards (both alignment and calibration) for SRM certification, 3Q 2004

Modeling the effects of all of the relevant feature properties in both the mask metrology process and in wafer exposure and development processes, using existing and new software tools, can improve feature size accuracy by establishing the relationship between mask-feature metrology results and the corresponding wafer-feature sizes, as in Fig. 5.

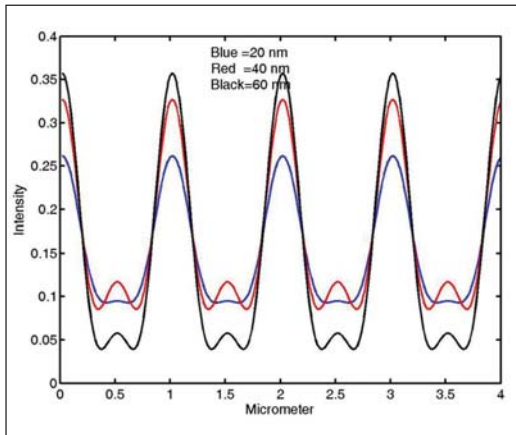


Figure 5. These data are modeling results showing the potential for using high resolution optical methods for wafer level CD metrology.

DELIVERABLES: Compare and test the accuracy of new scattering models for line width evaluation in transmission. 3Q 2003

DELIVERABLES: Work with SEMI and ISEMATECH in the development of a new standards specifications document for overlay metrology. 4Q 2003

2. The second component is the development of two-dimensional grid calibration standards and associated measurement techniques, including statistical analysis and CCD characterization as used by industry. These individual technical strategies for these components are described in more detail next.

We are approaching the problem of two-dimensional measurements from a couple of directions. The first, and most immediate, is to develop a wafer level artifact standard which can be used to bring all of the two-dimensional based inspection instruments to the same metric. This work has developed a standard grid which is printed on wafers for calibration purposes.

DELIVERABLES: Develop new calculation methods for analyzing asymmetric overlay targets. Compare with modeling results of more standard double etched silicon structures. Publish and present these results at ISMT Microlithography. 2Q 2004

DELIVERABLES: Use fully automated focus and positioning control systems to improve system performance. Continue to develop comprehensive analysis capabilities for centerline and edge detection methods. 3Q 2004

DELIVERABLES: Complete the overlay wafer calibrations and measurements. Continue to work with ISEMATECH on the development of new standard wafers and test structures. Deliver the wafers to the SRM office. 2Q 2004

ACCOMPLISHMENTS

- New image recognition and quantitative image analysis software has been developed by lead analyst J. Jun of the Precision Engineering Division. This comprehensive software package is based on the Matlab programming language and tool set and allows the evaluation of numerous effects on algorithm performance. The package has been used to quantify feature roughness and asymmetry effects on overlay pattern evaluation used in the feedback and control of lithography stepper tools. It has also been used in the quantification of algorithm robustness for sample-to-noise effects. This code has been used extensively to evaluate correlation and least-squares.

- Two sets of overlay wafers have now been received from SEMATECH. These will be made available in the very near future as SRM 5001 for overlay.

- The overlay metrology project is working closely with several companies such as Schlumberger and KLA Tencor to make available recent important research results on optical characterization, CCD data acquisition calibration, and focus and edge detection work. Neil Sullivan of Schlumberger showed strong interest in strengthening the collaboration with the overlay metrology project. NIST development of new correlation methods and image analysis/recognition software has enabled the detailed evaluation of noise, feature roughness, and feature inhomogeneity effects on repeatability and robustness of measurement tool performance, issues of paramount importance in semiconductor overlay metrology. We have performed a detailed, in depth study of CCD data acquisition cameras including the development of CCD mapping methods

- The NIST Overlay Metrology project leader has played a significant role in the Overlay Metrology Advisory Group (OMAG) of ISMT. This group is developing a comprehensive set of measurement guidelines, test methods, and tool performance measures to be adopted by the semiconductor manufacturing industry. The group is made up of more than 15 international semiconductor manufacturers. The OMAG has strong interest in adopting several new methods developed in the NIST Overlay Metrology Project. In particular, the recently published methods for evaluating CCD array performance and overall optical system characterization and calibration performance measures have been adopted.

■ The OMAG organized by ISMT has completed the specification document for the evaluation and benchmarking of overlay metrology tools for semiconductor manufacturing. The document will be used for procuring, testing, and matching tools.

■ The first set of two-dimensional grid artifacts is known as SRM 5001, and has been received. These 6-inch photomasks have been measured on a state-of-the-art I-pro metrology system by the photomask manufacturer. This effort, to make available traceable, 6-inch feature placement standards involves a close collaboration between NIST and Photonics. The collaboration employs the industry tool and the traceability of the NIST line scale interferometer with appropriate statistical analysis. The uncertainty budget for grid measurements has been developed and peripheral studies on various items are near completion.

■ NIST researchers have made comparisons between the E. Marx developed optical scattering code with the Spectel company Metrologia metrology modeling package. Different material systems were compared as well as one overlay feature at different focus positions. New results, based on the full integration of the NIST scattering code and Spectel optical microscope model, show very good agreement. This is an important step in the effort to provide industry the quantitative ability to determine sample-dependent effects on overlay tool performance. Results have been presented at SPIE Microlithography, 2004.

■ Near completion for the clean room enclosure on the overlay metrology tool. This will allow us to work closely with the industry and make SRMs directly transferable to a clean room environment.

COLLABORATIONS

ISMT, IBM, IVS Schlumberger, KLA-Tencor, Intel, Motorola, AMD and several other leading manufacturers or tool vendors.

The 14 members of The Neolithography Consortium.

RECENT PUBLICATIONS

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FRONT-END PROCESSING METROLOGY PROGRAM

The dimensions of the active transistor areas are approaching the spacing between dopant atoms, the stochastic regime, complicating both modeling and doping gradient measurements. Thin dielectric and conducting films are approaching monolayer thicknesses.

As device dimensions continue to shrink, junctions and critical film thicknesses approach the realm of several atoms thick, challenging gradient, thickness and wafer flatness and roughness metrology as well as electrical and reliability characteristics. The gate dielectric, traditionally SiO_2 , will soon no longer be viable. The overall task is to provide starting wafer dimensional and defect metrology, suitable metrology and reference materials for their dielectrics and junctions, including electrical characterization, gradient, thickness and roughness metrology and overall reliability metrology.



WAFER AND CHUCK FLATNESS METROLOGY

GOALS

Develop measurement support for 300 mm diameter silicon wafers used in lithography applications. This project provides measurement and infrastructural technology to support the interferometric measurement of thickness variation and surface flatness in the free form or chucked condition.

CUSTOMER NEEDS

Decreasing linewidths, and the resulting reduced depth of focus, combined with larger wafer diameters for current stepper lithography applications place ever increasing restrictions on flatness measurement and the required measurement uncertainty for thin parallel windows. For example, the International Technology Roadmap for Semiconductors (ITRS) suggests a flatness of less than 90 nm will be required per die site for the 90 nm node (expected by 2004). We are focused on meeting customer requirements for calibrated thickness variation maps of free form wafers and flatness measurements of chucked wafers. We are addressing the need for thickness variation maps of 300 mm diameter wafers using the NIST Improved Infrared Interferometer (IR³). There are two reasons for concentrating on wafer thickness variation. First, an independent traceable measurement is required by instrument manufacturers to certify the performance of their instruments. Second, thickness variation measurements of silicon wafers can be combined with models of wafer/chuck interactions to determine the flatness of low surface area wafer vacuum chucks, which is difficult to measure directly. The surface flatness of chucked wafers can be measured using NIST's "eXtremely accurate CALIBration InterferometerR" (XCALIBIR). XCALIBIR has a 300 mm aperture for flat measurements and provides a way of verifying models of wafer/chuck interactions.

TECHNICAL STRATEGY

1. IR² is a prototype infrared interferometer that can be used in several configurations. The collimated wavefront mode is the current focus of the project. In this method, the planar infrared wavefront is normally incident on the wafer. A portion of the beam is reflected from the front wafer surface, while the rest passes through the wafer and reflects from the rear surface. The in-

terference of these two wavefronts produces fringes and, by wavelength phase shifting, allows calculation of the wafer thickness variation (see Fig. 1 below). This measurement configuration is limited to double side polished wafers.

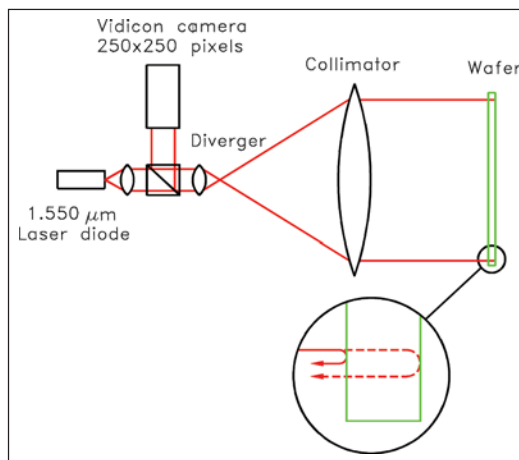


Figure 1. Schematic for collimated wavefront wafer thickness variation measurement.

DELIVERABLES: Calibrate thickness variation of low-dopant double side polished (DSP) wafers. 4Q 2004

2. A component in the evaluation of chucked wafer non-flatness is the characterization of interactions between the vacuum chuck and wafer. We are collaborating with Wavefront Sciences, Inc. (WFSI), Albuquerque, New Mexico and potentially one or more lithographic stepper manufacturers to help understand these interactions. WFSI is carrying out numerical analyses of the chuck/wafer interface for various chuck geometries. XCALIBIR, a general purpose 300 mm aperture phase measuring interferometer developed at NIST, can now be used to measure the flatness of chucked wafers. We will compare our measurements with measurements made on the WFSI optical measurement tool. The data can then be used to evaluate the influence of wafer/chuck interactions on the chucked wafer flatness.

DELIVERABLES: Make flatness measurements with XCALIBIR of 300 mm diameter wafers to help characterize interactions between vacuum chucks and wafers. 3Q 2003

ACCOMPLISHMENTS

■ A drift test was carried out using a 150 mm aperture collimator that captured data from the

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U. Griesmann
R. Polvani

"NIST continues to support the effort to bring quantitative standards and measurement practices to the semiconductor wafer metrology area. Their support in the area of wafer-chuck interaction studies are enabling advances in the state-of-the-art of wafer chucking that are essential to fully realize the potential of short wavelength lithography. WFSI's ability to collaborate with NIST in this area is critical to us."

T. D. Raymond
Wavefront Sciences, Inc.,
Albuquerque, NM

central portion of a 200 mm diameter, 750 μm thick, double side polished wafer. The measured optical path difference (*OPD*) was converted to thickness variation in nm using an assumed, homogeneous silicon index of 3.5. Total thickness variation (*TTV* or *GBIR*), which includes both the constant wafer thickness as well as local and/or linear variations in thickness, was not measured here because the piston, or constant, term was considered a setup error and removed during data analysis. Piston was removed because the *OPD* between the front surface and back surface reflections varies with changes in the angular orientation between the wafer and collimated source.

■ Average of repeatability testing measurements. The average of 192 phase measurements recorded at 15 minute intervals over a two day period is shown in Fig. 2. A peak-to-valley (PV) thickness variation of 1663.0 nm and root-mean-square (RMS) value of 414.4 nm were recorded over the measured aperture. Clearly, this wafer geometry is dominated by wedge, or a linear variation in thickness across the wafer face (the wafer is thinner at the top).

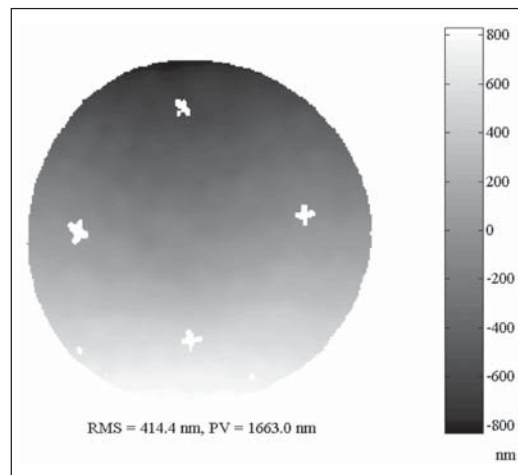


Figure 2. Average of repeatability testing measurements.

The (one sigma) pixel by pixel standard deviation in the 192 measurements is also shown in Fig. 3. This result, which was dominated by stray light in the interferometer, suggests repeatability at the 6 nm level for this set of tests. Temperature sensitivity was also measured; however, no strong correlation between variation in the results and temperature existed due to the high stability of the measurement cavity (*i.e.*, the wafer).

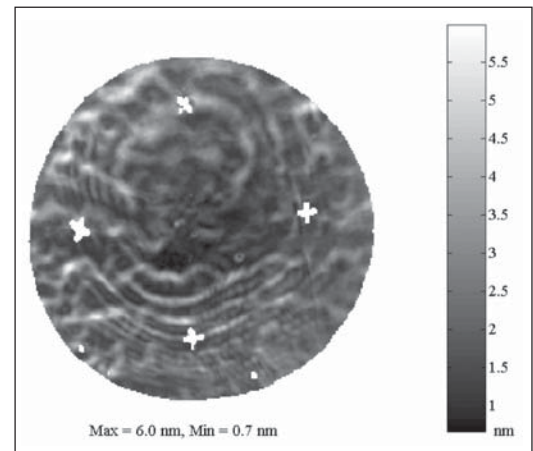


Figure 3. One sigma pixel by pixel standard deviation of repeatability measurements.

■ The result for a thickness variation measurement of a 100 mm diameter, 750 μm thick double side polished wafer follows and shows a PV thickness variation of 204 nm, Fig. 4, where the thickness variation is manifested as “power,” or the Zernike a_2^0 term, in the phase map. This large power suggests a gradual thinning radially from the outside edge to the center of the wafer.

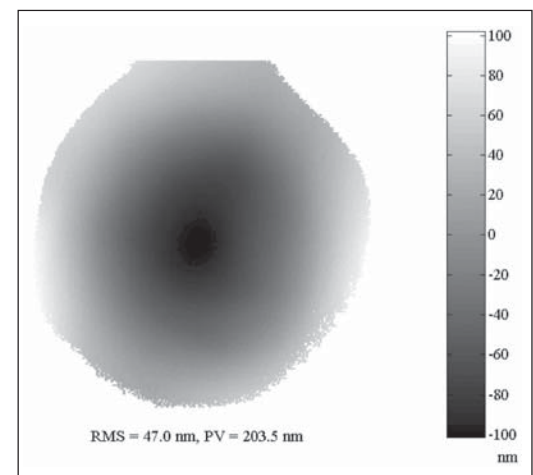


Figure 4. Thickness variation measurement for 100 mm diameter, 750 μm thick double side polished wafer (piston and tilt removed). Map shows that wafer is thinner in center by approximately 204 nm.

Surface reflection measurements of this wafer were performed using a commercial phase measuring interferometer in a Fizeau configuration. A front surface measurement showed a slightly concave shape with an a_2^0 Zernike coefficient of 4.437 waves (at a wavelength of 632.8 nm). A back surface measurement demonstrated a slightly convex shape with an a_2^0 value of 4.372 waves. The sag, *s*, for each surface can be calculated as

$s = 2 \cdot a_2^0 \cdot 632.8(\text{nm})$. The larger sag for the front (concave) surface suggests the wafer is thinner in the center, as shown by the IR² result. The sag for the front surface measurement was 5615 nm and 5533 nm for the back surface. The difference of these two gives an estimate of the gross thickness variation over the approximate measurement aperture of 30 mm (the smaller aperture was required to obtain reasonable fringe density for the bowed wafer and allow successful phase unwrapping). This difference is 82 nm.

- IR² has undergone a major upgrade that enables us to address the metrology needs for 300 mm diameter wafers. A collimator lens has been installed that can illuminate the entire surface of a 300 mm wafer and thus allows us to make a measurement of the wafer's thickness variation in a single measurement. The imaging system of the interferometer now can measure wafers with larger slopes and the spatial resolution of the detector was doubled. Further improvements will be aimed at reducing the noise level and at improving the measurement uncertainty.

- The thickness variation (TTV) of a low-dopant double side polished silicon wafer has been characterized.

- The flatness of 200 mm and 300 mm diameter wafers in the chucked condition was explored using the XCALIBIR interferometer.

COLLABORATIONS

Wavefront Sciences, Inc, T. D. Raymond; flatness measurements of free form and chucked wafers on XCALIBIR.

Virginia Semiconductor, Inc., Stephen Jones; thickness variation measurements of ultra-flat wafers.

Komatsu Silicon America, Paul Langer; 300 mm diameter wafer measurements.

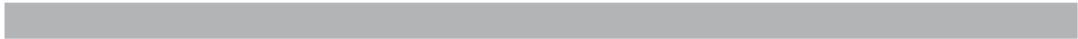
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MODELING, MEASUREMENTS, AND STANDARDS FOR WAFER SURFACE INSPECTION

GOALS

Provide industry with models, measurements, and standards for particles and other defects in order to improve the inspection of wafer surfaces. Develop facilities to accurately measure particle size and to deposit monosize particles on calibration artifacts to reduce the uncertainty in the sizes of particles used by the semiconductor industry to calibrate scanning surface inspection systems (SSIS). Investigate theoretically and experimentally the behavior of light scattering from particles, defects, and roughness on wafer surfaces.

CUSTOMER NEEDS

The Semiconductor Industry Association's (SIA) International Technology Roadmap for Semiconductors identifies the detection and characterization of defects and particles on wafers to be a potentially show-stopping barrier to device miniaturization. The roadmap specifies polystyrene latex (PSL) equivalent diameter particles that must be detectable on bare silicon, nonmetallic films, metallic films, and wafer backsides each year. Currently, no solutions to this inspection problem exist now for particles on bare silicon and on non-metallic films, while solutions do not exist for wafer backsides and metallic films in 2007 and 2009, respectively. While the detection sensitivity for defects must be increased, the ability to characterize defects in terms of size, shape, composition, etc., is critical for yield-learning. Defects must be characterized independent of defect location and topology.

With the need to detect smaller defects, the costs of inspecting wafers are skyrocketing. In order for new advances to be implemented in production environments, improvements in sensitivity must be achieved without suffering a tradeoff in throughput and must be cost-effective. The drive towards *in situ* sensors for production tools requires techniques which can be effectively miniaturized.

In order that wafer manufacturers and device manufacturers have a common basis for comparing specifications of particle contamination, improved standards for particles are needed. A recent comparison of the measurements of calibration wafers by thirteen different SSISs in-

dicated unacceptably large deviation between the SSIS results and the actual particle sizes. This study involved six particle sizes ranging from 88 nm to 290 nm and included the NIST SRM 1963 and two other sizes measured by NIST. For the two smallest particle sizes, 88 nm and 100.7 nm, the scanners systematically underestimated the size by about 8%. By 2005, it is anticipated that accurate calibration particles as small as 30 nm will be needed.

By 2010, at the 45 nm node, particles having diameters 22.5 nm must be detectable on bare silicon and nonmetallic films, 36 nm on metallic films, and 45 nm on the backsides of wafers. No known solutions exist at this time. [2003 ITRS, Yield Enhancement, Table 112b]

TECHNICAL STRATEGY

There are two major strategies to improving the performance of scanning surface inspection systems. One strategy is to develop a fundamental understanding of optical scattering at surfaces so that tool manufacturers can optimize the performance of their instrumentation, in terms of defect detection limits and discrimination capabilities, to characterize the response of instrumentation to different types of defects, and to develop and calibrate particles of well-defined size and material. Recent work by this group has demonstrated that the polarization of light scattered by particulate contaminants, subsurface defects, and microroughness has a unique signature that can be used to identify the source of scatter. In particular, it was found that small amounts of roughness do not depolarize scattered light. This finding has enabled the development of instrumentation which can collect light over most of the scattering hemisphere, while being blind to microroughness. That instrumentation, for which a patent has been awarded, should result in a factor of two improvement in minimum detectable defect size.

A second strategy is to provide leadership in the development of low uncertainty calibration particles for use in calibrating surface scanners. A major focus has been development of the differential mobility analysis (DMA) method for accurately sizing monosize polystyrene spheres. This work together with a SSIS round robin has pro-

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G. W. Mulholland

"I would like to thank you and NIST for the support that you have provided to VLSI Standards in the sizing of polystyrene latex spheres through the work of Dr. George Mulholland. We are very pleased with the measurements that Dr. Mulholland has performed, and with the level of technical support that the NIST staff has provided to us. This work is of technical and economic importance to the semiconductor industry and to VLSI Standards, because the ability to correctly size ever smaller particulate contaminants on silicon substrates is key to the manufacturing yield of silicon chips. We look forward to a continuing technical relationship between VLSI Standards and NIST."

*Marco Tortonese, Ph.D.
VLSI Standards, Inc.*

vided evidence that current SSIS measurements have an unacceptably large uncertainty for particle sizes in the 90 nm to 100 nm size range. The technical focus of our future work will be applying the DMA for accurately sizing calibration particle sizes as small as 30 nm, developing methods for generating other types of monosize particles, and developing laser surface scattering methods for quantitative particle sizing.

Specific project elements are defined below:

1. Polarized Light Scattering Measurements –

The Goniometric Optical Scatter Instrument (GOSI) enables accurate measurements of the intensity and polarization of scattered light with a wide dynamic range, high angular accuracy, and multiple incident wavelengths (visible and UV) (see Fig. 1). We measure the light scattering properties of well-characterized samples exhibiting interfacial roughness, deposited particles, subsurface defects, dielectric layers, or patterns. The emphasis is on providing accurate data, which can be used to guide the development of light scattering instruments, and to test theoretical models.

DELIVERABLE: Light scattering measurement of diameter of a 60 nm sphere standard and an associated uncertainty analysis. 3Q 2004

2. Theoretical Light Scattering Calculations –

The focus of our theoretical work is on (a) developing models that accurately predict the polarization and intensity of scattered light, and (b) determining what information can be efficiently

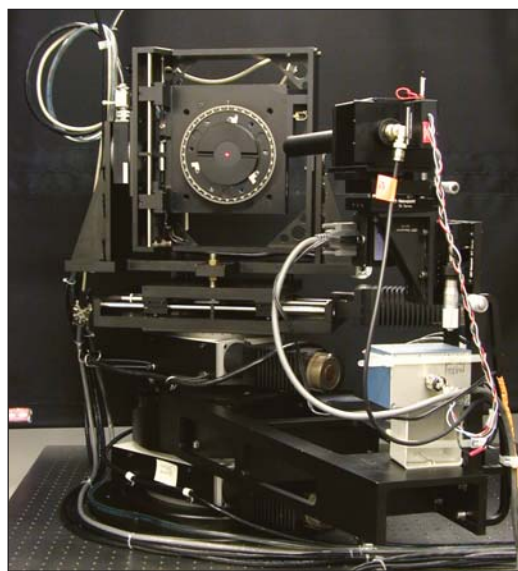


Figure 1. The Goniometric Optical Scatter Instrument is a state-of-the-art laser scattering facility.

and accurately extracted from light scattering measurements. Approximate theories are used in conjunction with more complex techniques to gain an understanding of which parameters affect the light scattering process. Particular cases that are being analyzed include (a) scattering by defects and roughness associated with dielectric layers, (b) scattering by particulate contamination on bare and oxidized wafers, and (c) scattering by periodic structures.

DELIVERABLE: Develop discrete source method code for arbitrary shape particles on surfaces. 1Q 2005

3. Instrument Development –

A second instrument, the Scanning Optical Scatter Instrument (SOSI), complements the capabilities of GOSI as a prototype for a production-line light scattering inspection tool (see Fig. 2). An instrument with twenty-eight fixed detection elements covering the scattering hemisphere, SOSI enables a determination of the differential scattering cross section, for individual particles or defects on a wafer surface. This instrument can be configured so that it is blind to interfacial roughness. Together with an understanding of the light scattering functions for different imperfections, SOSI has a substantially improved capability for rapidly detecting and identifying defects, particles, and microroughness on wafers.

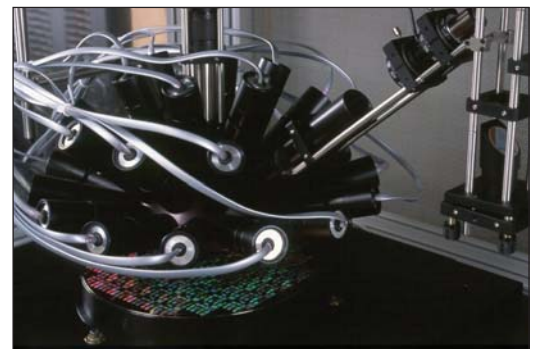


Figure 2. The Scanning Optical Scatter Instrument enables the scattering from individual particles to be analyzed.

DELIVERABLES: Perform size distribution measurements of the 100 nm sphere standard (NIST SRM 1963) using the SOSI system. 3Q 2004

4. Size Distribution Measurements –

Differential mobility analysis (DMA) has been shown to be capable of making accurate size measurements for mean particle size for 100 nm monosize polystyrene spheres. There are promising results for the measurement of the size distribution for

broader size distributions; however, the results are not quantitative. Work is in progress to quantify the uncertainty in the size distribution measurement and to extend the method to smaller particle sizes.

DELIVERABLES: Certify a 100 nm particle size SRM to replace SRM1963 using the NIST particle sizing calibration facility. 4Q 2004

Provide uncertainty estimates for moments of the size distribution for PSL spheres based on DMA measurements. 4Q 2004

5. Aerosol Generation – An aerosol must be formed typically from a liquid spray of a particle suspension before the particles can be sized by the DMA or deposited on a wafer. Work is in progress to use a variety of innovative methods for generating, shaping the size distribution of the aerosol, and depositing the particles. These include the electrospray for generating particle sizes smaller than 60 nm, impactor to remove the large size fraction of the aerosol and to deposit the particles, and an electrostatic chamber for depositing small particle sizes (see Fig. 3). Work is also in progress to generate metallic particles from chemical precursors in a tube furnace.

DELIVERABLES: Deposition of monosize 65 and 100 nm spheres on silicon wafers for use in light scattering measurements and on electron microscope grids for assessing the sphericity of the particles on the surface. 3Q 2004

Publication of manuscript on the slip correction of nano-size particles based on the DMA. 4Q 2004

6. Resource on Particle Science – Over the past five years, the particle related work has included projects with SEMATECH and particle suppliers to the semiconductor industry. A number of needs by particle related companies were expressed at a NIST particle workshop including redoing the uncertainty assessments of existing particle SRMs and offering a particle sizing calibration service. Providing support for particle needs critical to the semiconductor industry will continue to be a priority.

DELIVERABLES: Provide technical and statistical support for the development of a SEMI document entitled: Test Method for Evaluating DMA-Based Particle Deposition Systems and Processes. 3Q 2004

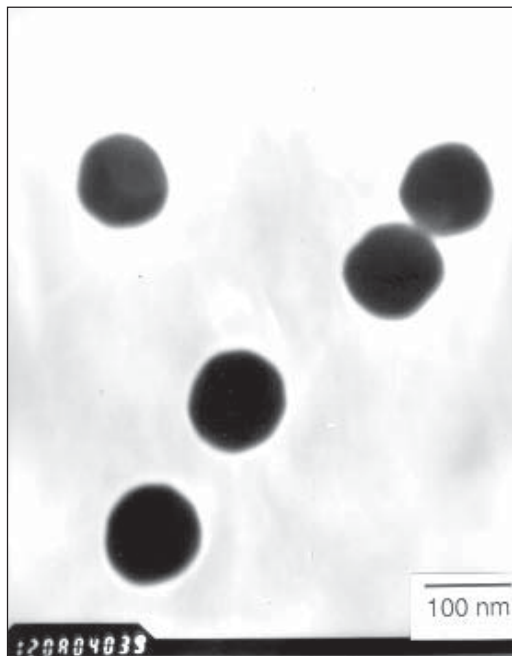


Figure 3. Transmission electron microscope images of 100 nm copper spheres generated by a novel spray pyrolysis method. These particles were developed to test light scattering theories for scattering by particles on surfaces.

ACCOMPLISHMENTS

- Determined that the electrospray technique can produce an aerosol having characteristics optimal for transferring particles in a liquid suspension onto wafers for particle diameters as small as 25 nm. This significant finding enables improved wafer depositions by reducing the number of contaminant residue particles, the number of doublets, and the amount of residue on the particles.
- Developed a NIST Calibration Facility for sizing monodisperse spheres suspended in water in the size range of 50 nm to 400 nm with an expanded uncertainty of 1.5 % of the peak size. This facility has been used for two customers providing calibration particles to the semiconductor community.
- Coordinated the experimental design and uncertainty analysis with the University of Minnesota for the first measurement of slip correction of particles smaller than 300 nm. These measurements are critical to improving the accuracy of particle size by the DMA in the nanometer size range.

■ In collaboration with the University of Maryland, developed a method for generating pure copper spheres with diameters ranging from 100 nm to 200 nm. These spheres, which mimic real-world particles better than polystyrene, were used to validate particle scattering theories in conditions for which models have a higher degree of uncertainty. Measured polarization and intensity of light scattered from the copper spheres and found good agreement with the Bobbert-Vlieger theory for light scattering from a sphere above a surface.

■ Developed a method, based upon scattering ellipsometry, for quantifying scatter from two sources and demonstrated its use by characterizing the roughness of both interfaces of an SiO₂/silicon system. This finding establishes the validity of the light scattering models for roughness in a dielectric film, which in turn limits the detection sensitivity of SSIS instruments. The method was also used to characterize scattering from steel surfaces, demonstrating capability to distinguish between scattering from surface roughness and material inhomogeneity. The method was further used to study the scatter from an anti-conformal polymer film, helping to establish the limits of validity of the scattering theory.

■ Developed the SCATMECH library of C++ routines for light scattering. Published the SCATMECH library, providing a means for distributing scattering models and polarized light calculations to others. From the time of its public availability in March 2000, over 2000 copies of the library have been downloaded from the web. In July 2004, Version 4 was released, which contains an accurate theory for the scattering of light by a spherical particle on a surface and theories for scattering from roughness and small defects in dielectric layers.

■ Extended the theory of scattering of a sphere on a surface to axially-symmetric non-spherical particles. Demonstrated that the scattering by a metal particle on a surface is extremely sensitive to the shape of the particle in the region where the particle contacts the surface. This unusual sensitivity to shape must be considered when light scattering tools classify particles for material and size.

■ Performed a light-scattering-based diameter measurement of the NIST 100 nm PSL sphere standard (SRM 1963) deposited onto a silicon wafer. The measurement results included a thorough assessment of the uncertainties that

arise in such measurements. It was found that the uncertainty was dominated by sample-to-sample variations, which probably result from the presence of doublet particles. Uncertainties in the substrate optical properties, the thickness and optical properties of the substrate oxide, and the shape of the particle dominate the systematic uncertainty. Results for smaller PSL particles suggest that surface-induced deformation of the particles must be considered.

COLLABORATIONS

Department of Chemical Engineering, University of Maryland, Professor Sheryl H. Ehrman, Validation of Scattering Theory Using Novel Monodisperse Particles.

Department of Mechanical Engineering, University of Minnesota, Professor David Pui, Generation and Measurement of Nanosize Particles.

National Metrology Institute of Japan, Dr. Kensei Ehara, Nanoparticle Metrology.

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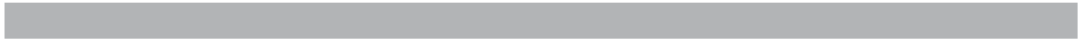
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FRONT-END MATERIALS CHARACTERIZATION

GOALS

To provide industry with new and improved measurements, models, data, and measurement traceability/transfer mechanisms to enable the more useful and more accurate metrology infrastructure needed for select silicon CMOS front-end materials characterization. Major focus is placed on metrology requirements from the 2003 International Technical Roadmap for Semiconductors (ITRS) expressed as difficult challenges: (1) Structural and elemental analysis at the device level, including SIMS, HRTEM, and 1-D and 2-D dopant profiling by scanning probe microscopes, and (2) Metrology for advanced gate stacks and other thin films. Additional work will be undertaken as possible on additional important thin films and bulk material properties for silicon and other emerging semiconductors.

(1) To improve capabilities for compositional depth profiling, this project defines optimum procedures for ultra-high depth resolution by Secondary Ion Mass Spectrometry (SIMS), develops depth-profiling reference materials needed by U.S. industry, and improves the uncertainty of implant dose measurements by SIMS. To provide industry with the metrology infrastructure needed to measure two- and three-dimensional dopant profiles in the ultra-shallow junction regime, this project develops measurement methodologies, theoretical models, and data interpretation software for the Scanning Capacitance Microscope and other scanning probe microscopes.

(2) To address needs in composition and thickness measurements for thin films and interfaces, this project develops new optical and physical characterization methods, as well as, characterizes the accuracy and reliability of existing methods. Materials of interest include high- κ and low- κ materials, polymers, silicon-on-insulator (confined silicon), and strained silicon-germanium. High Resolution Transmission Electron Microscopy (HRTEM) is being characterized for thickness measurements of ultra-thin gate dielectrics.

CUSTOMER NEEDS

The Front-End Materials Characterization project addresses key material characterization problems associated with the integrated circuits industry's front-end process, particularly new gate stack pro-

cesses and materials, and metrology for structural and element characterization at the device level, particularly ultra-shallow junctions. Front-end processing requires the growth, deposition, etching, and doping of high quality, uniform, defect-free films. These films may be insulators, conductors, or semiconductors. The 2003 International Technology Roadmap for Semiconductors (ITRS) near-term (through 2009) difficult challenges for front-end processes include: *metrology issues associated with gate dielectrics film thickness and gate stack electrical and materials characterization, introduction of metal gate electrodes with appropriate workfunctions, and metrology issues associated with 2-D dopant profiling. Metrology needs for Thermal/thin films, Doping Technology, SOI, and strained-silicon are discussed in the 2003 International Technology Roadmap for Semiconductors in the Metrology Section.*

Since source/drain dopant profiles are a critical factor determining the performance of a transistor, dopant profiling has always been needed by the silicon integrated circuit industry. One-dimensional dopant profiles from SIMS or electrical techniques remain an important process control tool. As transistors are scaled to ever-smaller dimensions, the variation of dopant profiles in two- and three-dimensions also begin to influence device operation. Two- and three-dimensional dopant profiles are now needed to validate models of the processes used to produce ultra-shallow junctions and for accurate device simulations.

SIMS is most likely to provide the solution to precision requirements for 1-D dopant concentration measurements. These goals can be achieved by careful control of SIMS depth-profiling conditions and by developing and making available implant reference materials for common dopant elements. Scanning Capacitance Microscopy (SCM) is a contender to provide two-dimensional carrier profiles. Relatively accurate 2-D profiles of the dopant concentration can be obtained when SCM images are combined with SIMS measurements.

The ITRS identifies structural and elemental analysis at devices dimensions (for example 3-D dopant profiling) as one of the difficult challenges beyond 2009. Offline secondary ion mass spectroscopy has been shown to provide the needed precision for current generations including ultra-shallow junctions. Two- and preferably three-dimensional profiling is essential for achieving

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(Ellipsometry)
David Simons (SIMS)
John Small (HRTEM)

future technology generations. Activated dopant profiles and related TCAD modeling and defect profiles are necessary for developing new doping technology. The ITRS requirements are for at-line 2-D dopant profile concentration measurements with spatial resolution of 4.1 nm and precision of 4 % in 2004, increasing to spatial resolution of 2.8 nm and 2 % precision for the 2010 through 2018 timeframe. Complete specifications are given for the short term in Table 119a on page 20, and for the long term in Table 119b on page 21 of the Metrology section.

The evolving decrease over time of the gate dielectric film thickness to an oxide-equivalent value below 2 nm is identified as a critical front-end technology issue in the ITRS. An effective oxide thickness of 1.0 nm, or less is being projected for the 0.1 μm CMOS technology node in 2006, dropping to 0.8 nm or less by 2010. For effective gate dielectric thicknesses below ~ 2.0 nm, SiO_2 is being replaced, initially by oxynitride or oxide/nitride stacks, and then by either metal-oxides or compounds such as metal-silicates. Process control tolerance needs for dielectric thickness are projected to be less than 0.1 nm for 2 nm films. Requirements for process control measurements are a factor of ten smaller still. HRTEM provides a means of establishing traceability of film thickness to the lattice spacing of silicon.

The microelectronics industry has a high demand for reliable thin film measurement methods that yield composition and dimensional information with known accuracy and precision. The metrology section of the ITRS section states the needs for reference materials and standard measurement methodology for new high- κ gate and capacitor dielectrics with interface layers, and thin films such as interconnect barrier and low- κ dielectric layers. Optical measurement of gate and capacitor dielectric averages over too large an area and needs to account for and characterize interfacial layers. The same is true for measurement of barrier layers.

Spectroscopic ellipsometry (SE) is expected to continue as a preferred measurement for process monitoring of future gate dielectric films. IC fabrication metrology needs: (1) improved methods to determine film thickness and compositions; (2) techniques to determine the structure of individual films and the interfaces between them; (3) an improved understanding of the relationship between physical, electrical, and optical determination of film properties; and (4) mechanisms for enabling

traceability to NIST. In order for SE to meet process control requirements of film thickness and the determination of film composition and morphology, the optical properties of these advanced dielectric film systems must be characterized and understood.

The ITRS identifies measurement of complex material stacks and interfacial properties including physical and electrical properties is identified as one of Metrology's 10 difficult challenges through 2009. Development of metrology for high- κ materials needs to continue and metrology for the interfacial layer remains a difficult challenge. The dielectric properties of transistor dielectric films after deposition are different from those subsequent to thermal processing.

TECHNICAL STRATEGY

The 2003 ITRS expressed as difficult challenges: (1) structural and elemental analysis at the device level, including SIMS, HRTEM, and 1-D and 2-D dopant profiling by scanning probe microscopes, and (2) metrology for advanced gate stacks and other thin films. Our focus areas include: (1) development of refined metrology methods and standards for SIMS; (2) scanning probe metrology for ultra-shallow junctions, particularly two-dimensional dopant profiling; (3) identifying structural models and developing preferred optical index dispersion functions or data for improved ellipsometric analysis of future generation gate-dielectric film systems; (4) correlating optical, electrical, and physical measurements of thickness, composition, and interface structure; (5) development of metrology for evaluating candidate metal gate materials; and (6) measurements and analysis for silicon optical constants and advanced silicon materials.

SECONDARY ION MASS SPECTROMETRY (SIMS)

Secondary ion mass spectrometry (SIMS) has demonstrated the capability to meet the ITRS dopant profiling requirements for B, As, and P. However, the detailed analytical protocols required to achieve these goals have not been completely specified. We have organized an international round robin study through ISO committee TC201 to investigate the parameters that must be controlled to make highly repeatable dose measurements of As with magnetic sector SIMS instruments. In addition to improved repeatability for dopants, the ITRS roadmap also requires increased SIMS detection limits for trace metal contamina-

tion analysis of semiconductor devices. We are also working on novel methods to enhance detection limits for common metal contaminants by increasing the ionization efficiency during the SIMS sputtering process.

DELIVERABLE: Conduct international round robin of arsenic dose determination by SIMS. Develop improved methods for high sensitivity analysis of trace surface metals and impurities. 3Q 2004

Shrinking semiconductor device dimensions require increased depth resolution for depth profiling analysis. Typically, the highest depth resolution is achieved by using ultra-low energy primary ion bombardment. However, this capability is not available on most commercial SIMS instruments. In instruments where low energy analysis is available, slow sample erosion rates can result in prohibitively long analysis times. We are exploring an alternate approach that involves using a high energy, focused ion beam to rapidly mill a beveled cross-section in the sample under examination. The “altered layer” produced by the high energy milling beam can be removed by subsequent bombardment in a special gaseous cluster ion beam sputtering instrument. The cross section prepared in this fashion is then analyzed using high resolution imaging Auger and SIMS analysis.

DELIVERABLE: Improve SIMS depth profile resolution using ultra low energy ion beam cleaning of ion milled cross-sections and bevels. 2Q 2004

Some thin-film materials such as metals do not sputter as uniformly as silicon under ion bombardment. The initial surface topography of the metal surface or topography induced by the sputtering process itself often limits the achievable depth resolution. We are exploring a mechanical thinning method that will allow SIMS depth profiling from the back-side silicon through the interface with the top layer. This will allow subtle diffusion effects to be distinguished and will eliminate degradation in depth resolution from surface or sputter-induced topography. This method relies on a commercial polishing system that allows precise adjustment of the parallelism between the sample surface and the platen containing the polishing material. Silicon is removed by mechanical grinding using a series of diamond lapping films of decreasing abrasive size. This approach is being applied to the depth profiling analysis of blanket films (copper metallization on silicon) as well as PMOS patterned wafers in collaboration with International SEMATECH.

DELIVERABLES: Develop sample preparation for backside SIMS depth profiling. 1Q 2004 Test procedures on new thin oxide materials supplied by International SEMATECH. 3Q 2004 Apply approach to analysis of gold films on copper. 4Q 2004

Cluster primary ion beam SIMS offers several advantages for the analysis of semiconductors over using monoatomic primary ions. Cluster bombardment SIMS offers improvements in depth resolution; higher sputter rates, and increased sensitivity for some elemental species. Also, greater sensitivity for organic species may greatly increase our ability to detect organic contamination on silicon surfaces. We are exploring various applications of this technique and attempting to develop new, low cost cluster ion beam sources to promote more widespread use of the technique.

DELIVERABLE: Continue development of cluster SIMS technique for depth profiling of semiconductors. Implement new C_{60}^+ primary ion source capability on NIST SIMS instruments. 2Q 2004

SiGe thin film compositional standards – After the need for SiGe compositional standards was discussed at the 14th Annual Workshop on Secondary Ion Mass Spectroscopy (SIMS) in 2001, NIST contacted fabrication and analytical laboratory facilities to develop a reference material using an interactive approach. The typical time frame for an NIST SRM is many years to develop, characterize, and bring to market. The need for SiGe standards was seen as an immediate need, because the current calibration method of Rutherford Backscattering is only accurate from 5 % to 10 % relative and this is insufficient for reliable device production. NIST is collaborating with several semiconductor facilities and analytical laboratories to develop a suite of SiGe compositional standard films. Using an interactive data collection mechanism with collaborators and publishing the data on the web, a faster approach to standard materials production is being developed. This will allow materials to be used and compared even while reference data are being developed.

DELIVERABLE: Develop a suite of SiGe compositional standards to allow accurate and reproducible SiGe thin film production. 4Q 2004

SCANNING PROBE METROLOGY FOR ULTRA-SHALLOW JUNCTIONS

We are developing tools that are intended to enable scanning capacitance microscopes to function as two-dimensional dopant profiling tools. This work is divided into three tasks: Task 1 is to develop SCM measurement methodologies. Best

measurement practices are being determined via collaborative projects with industrial users and research into the physics of the silicon surface preparation. Task 2 is to develop theoretical models of the SCM. The focus of our modeling effort has been to develop 2-D and 3-D finite-element solutions of Poisson's equation for the SCM geometry. Task 3 is interpretation of SCM data and technology transfer. Our expertise with interpreting SCM images is being transferred to industry through our software program *FASTC2D*. The program features an easy to use interface, rapid profile extraction, and operation in a Windows environment.

The version of *FASTC2D* currently available utilizes a calibration curve, determined from a database of pre-calculated solutions, which can very rapidly determine a 2-D carrier profile from an SCM image. When used in conjunction with SIMS measurements or a reference sample, relatively accurate profiles can be obtained. We are also developing an additional tool for technology transfer: a new generation of test structures consisting of fully processed and partially processed transistors. These will eventually be produced in sufficient numbers so that every *FASTC2D* user can get a set. A round-robin set of measurements based on these structures and using an easy to implement measurement procedure, is planned, with devices to be distributed through the SEMATECH 2-D dopant profiling working group. Figure 1a shows an SCM image of the prototype

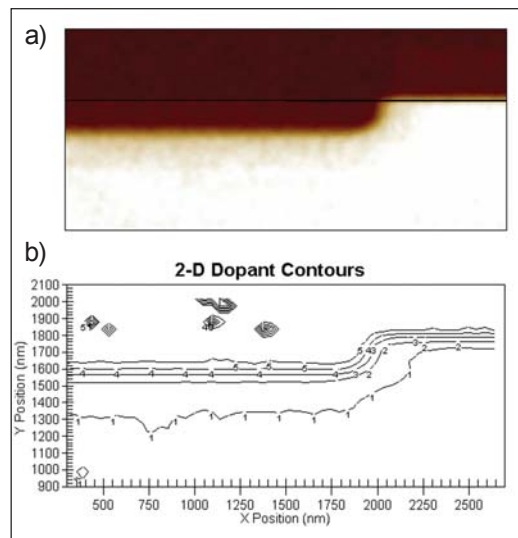


Figure 1. a) Typical SCM image of cross-sectioned, p-type, prototype tutorial test structure. b) Two-dimensional dopant contours extracted from SCM image using *FASTC2D*.

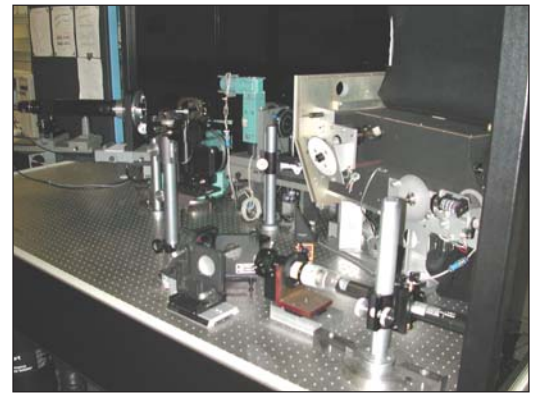


Figure 2. NIST custom-built High Accuracy Ellipsometer.

test structure consisting of a boron implant into p-type silicon; Fig. 1b shows the corresponding 2-D dopant contours extracted from the SCM image using *FASTC2D*.

DELIVERABLE: Demonstrate SCM-measured dopant profiles with improved spatial resolution through use of sample beveling and refined data interpretation.

STRUCTURAL AND OPTICAL MODELS FOR ELLIPSOMETRY

The high- κ dielectric stack (the bottom interface, the high- κ dielectric, the top interface, and the gate metal) is a critical component of future generation integrated circuits and one that is rapidly nearing production. We seek to develop spectroscopic ellipsometry (SE) measurement metrology requirements and models required for high- κ materials and processes and have them in place and on time for their introduction into standard fabrication processes. A custom-built, high-accuracy ellipsometer, Fig. 2, with a spectral range of 1.5 eV to 6.2 eV and a commercial VUV ellipsometer, Fig. 3, which extends the spectral range to 9.5 eV, are



Figure 3. J. A. Woollam VUV Variable Angle Spectroscopic Ellipsometer (VUV-SE).

available for this task. Project staff are working with International SEMATECH, IC companies, and SRC university staff to obtain and optically characterize advanced oxynitrides, oxide/nitride stacks, and more complex compounds, such as, hafnium silicon oxynitride and hafnium-aluminum silicate.

Since many of these materials have bandgaps just below 6 eV, the additional measurement range obtainable with the VUV ellipsometer enables the investigation of important processing related structure in the index of refraction (dielectric constant) of these materials, which shows up in the absorbing region above the bandgap energy. Project work is directed at determining preferred structural models, spectroscopic index of refraction values, or preferred optical dispersion functions for each of these film systems, and where possible the variability of these parameters due to differences in film fabrication processes. Work is also directed at extraction of accurate bandgap values and at interpreting the processing related structure found in the dielectric function. Analysis has been done primarily with software developed at NIST for SE. This software, Fig. 4, allows maximum flexibility for addition of the latest published or custom-developed optical response models as appropriate for each material system investigated, and has allowed the maximum transparency of analytical procedures employed. High- κ thin films obtained for this project have been deposited using Chemical Vapor Deposition, Atomic Layer Deposition, Sputtering Deposition, or Jet-Vapor Deposition. Figures 5 and 6 show the results of our recent studies of the optical properties on a set of ZrO₂ films formed by atomic-layer-deposition. It is significant to observe the dielectric function (Fig. 5) and the optical bandgap (Fig. 6) increase with the film thickness. This may

be due to a transformation of the ZrO₂ films from amorphous to tetragonal phase when the films become thicker than ~80 Angstroms.

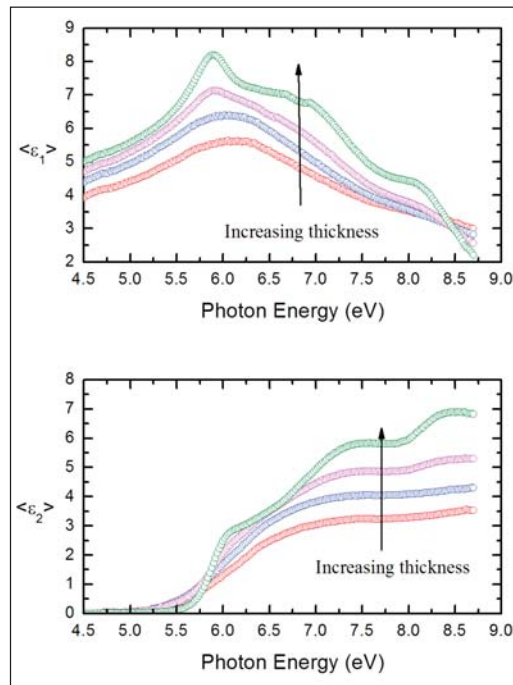


Figure 5. The real part of the complex dielectric function of a series of ZrO₂ films grown on c-Si under the same condition except the film thickness.

DELIVERABLES: By the end of 2004, determine the optical properties of technologically relevant high- κ thin films (ZrO₂, HfAlO, and Hf-based alloys) and their optical bandgaps by using VUV spectroscopic ellipsometry. Demonstrate optical models for high- κ materials.

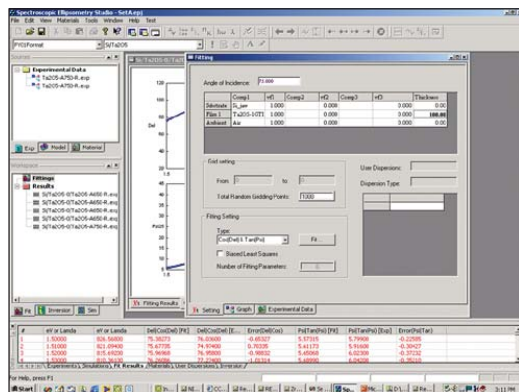


Figure 4. NIST spectroscopic ellipsometry modeling software.

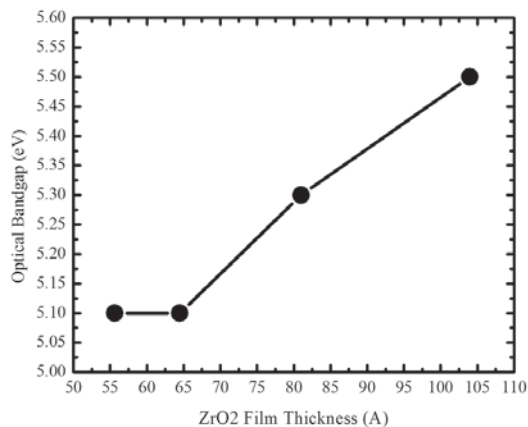


Figure 6. Optical bandgap of ZrO₂ films changes with the film increasing thickness. It is believed that the ZrO₂ changes phase from amorphous to tetragonal when the film thickness increases above ~80 Angstroms.

RELATION BETWEEN THE OPTICAL, ELECTRICAL, AND PHYSICAL MEASUREMENTS OF HIGH- κ MATERIAL PROPERTIES

We seek to develop fundamental understanding of the physical properties of high- κ dielectric films via comparison of structural, optical, and electrical characterization. Through collaborations with International SEMATECH, IC industry companies, SRC university staff, and with key researchers in other parts of NIST, project staff are leading a number of multimethod comparison studies of various ultra-thin gate dielectric films. These multimethod studies utilize techniques such as transmission electron microscopy (TEM), soft X-ray photoemission (SXPS), X-ray absorption spectroscopy (XAS), grazing incidence angle X-ray diffraction (GIXRD), capacitance-voltage (C-V) and current-voltage (I-V) analysis, as well as SE, reflectivity, and FTIR-ATR. Figure 7 shows the use of FTIR-ATR to study the relation between ZrO_2 film thickness and crystalline phase. When used in conjunction with other techniques, FTIR-ATR can be used to determine information on the film composition, impurities, and crystal phase.

DELIVERABLE: By the end of 2004, demonstrate the capability of the FTIR-ATR to acquire absorption data that can be used to characterize the molecular structure, composition, impurities, and possible strain in high- κ dielectric films in the nanometer thickness regime.

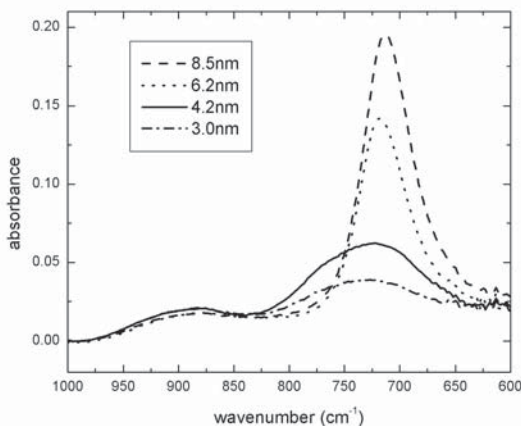


Figure 7. FTIR-ATR Absorption Spectra of a set of ultra-thin ZrO_2 films showing a thickness dependent bulk Zr-O vibration absorption peak at $\sim 710\text{cm}^{-1}$, likely due to an LO phonon. Such absorptions can be related to crystal phase through comparison with other techniques such as X-ray diffraction. The location, strength and broadening of such peaks as a function of processing conditions can lead to a variety of other information about the film bulk, interfaces, or surfaces.

Only through development of a complete understanding of these high- κ metal-oxide, -silicate, -aluminate, etc. materials will their full potential as components in state-of-the-art integrated circuits be realized. Many of the materials of interest have been studied previously, but only in bulk, or powder, form. Thin films of nominally the same composition prepared on silicon by different methods (CVD, ALD, or PVD), or from different precursors can result in quite different physical and electrical properties and may be in metastable states due to kinetics. The crystalline phase of various high- κ dielectrics films can depend on film thickness, stress, grain-size effects as well as impurities that may lead to the stabilization, or predominance, of one or more of these phases. For example, zirconia, a material of significant interest as a possible dielectric film, can be found to exist in three crystallographic phases: cubic, monoclinic, or tetragonal, but its morphology as a thin film is not well correlated to deposition processes or anneals. The degree of crystallinity, interface roughness, chemical homogeneity, and stoichiometry can have a direct effect on the dielectric properties and the leakage current across such dielectric layers. Strain, interface properties and the effects of surface contamination species can also have important effects.

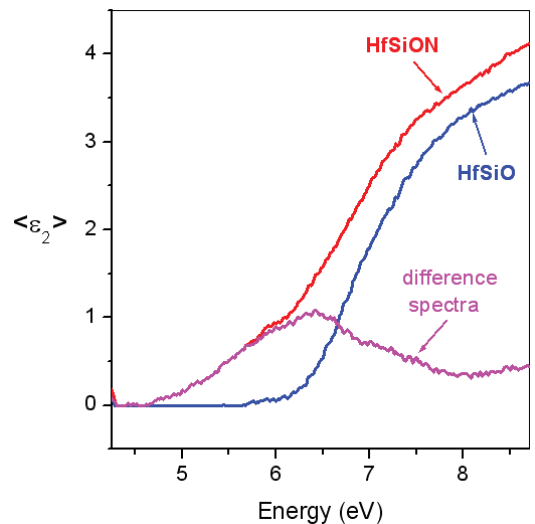


Figure 8. Imaginary part of the dielectric function, ϵ_2 , obtained from spectroscopic ellipsometry for films of HfSiO and HfSiON. This lossy part of the dielectric function gives a measure of the optical band-gap (non-zero values for ϵ_2), and near-band edge states. In this figure, the addition of nitrogen is seen to reduce the band-gap by about 1.6eV. If the HfSiO spectrum is shifted to align its slope with that of HfSiON (not shown), a difference spectrum (shown), which should be due to nitrogen states, can be calculated.

Figures 8, 9, and 10 illustrate the use of SE, XPS, and XAS, respectively, to determine effects of the oxygen and nitrogen on the electrical properties of HfSiO and HfSiON films. SE is used to determine the dielectric function, XPS yields information about the valence band edge, and XAS can be used to determine the O:N ratio. Access to a range of complimentary techniques is essential to develop a complete picture of the properties of the films.

DELIVERABLE: By Q2-2004, determine the crystal structure of high- κ dielectric films by physical techniques and demonstrate the relevance of the crystalline phase to electrical properties and other important material properties.

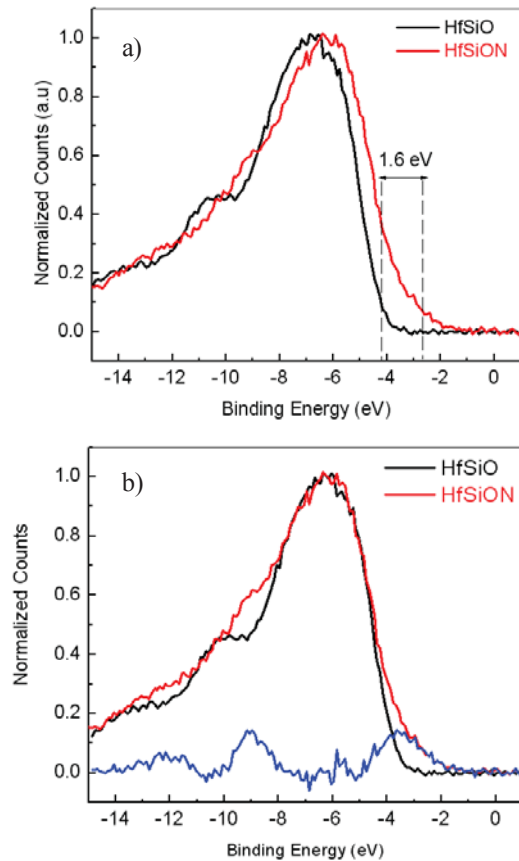


Figure 9. a) Soft X-ray photoelectron spectroscopy spectra of HfSiO and HfSiON thin films. This spectroscopy gives information about the valence band edge, but not about the full band-gap. Here, inclusion of nitrogen into the silicate network decreases the valence band offset (about 1.6 eV, left panel) by introducing states in the gap. A shift in the O2p edge is also observed. b) The aligned spectrum is shown along with the calculated difference spectrum. The difference spectrum shows the states due to nitrogen. Compare the change in band offset structure here, due to the addition of nitrogen, with the change in band-gap edge structure related to nitrogen, as shown in Fig. 7.

DELIVERABLE: By the end of 2004, complete a systematic study of the valence band offsets of hafnium-based high- κ dielectric films. (The valence band offset is a critical parameter in determining leakage and power dissipation for a given dielectric composition).

One of the most common methods of evaluating film thickness is through the use of HRTEM. The ability of HRTEM to measure the thickness of sub-4 nm gate dielectric films is in question pending a quantitative understanding of the errors and uncertainties in the measurement process. The goal of this work is to quantify the accuracy of HRTEM as a technique for measuring the thickness of such films.

DELIVERABLE: Determine uncertainty budget for the thickness measurement of gate dielectrics by HRTEM. 3Q 2004

METROLOGY FOR METAL GATES

Channel autodoping associated with boron out-diffusion from the polysilicon gate and polysilicon depletion will eventually require the phase out of dual-doped polysilicon gate material. Work function, resistivity, and compatibility with CMOS technology are key parameters for new candidate gate electrode materials. Different materials may be needed for the PMOS and NMOS transistor gates to achieve acceptable threshold voltages. Eventual introduction of single-gate, fully-depleted ultra thin body SOI devices with intrinsic channels will change the optimal values of the gate

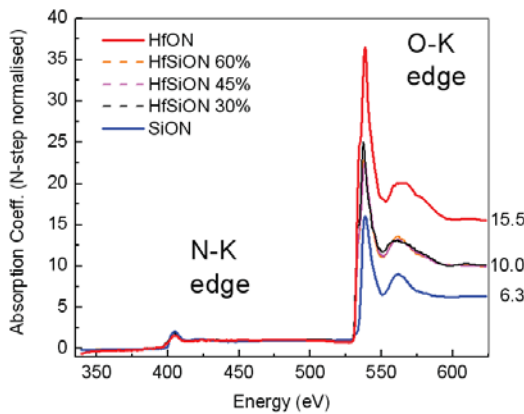


Figure 10. X-ray absorption scattering (XAS) measurements are used to determine the oxygen to nitrogen ratio in a variety of dielectric films that are currently being used, or are being investigated for use in advanced silicon IC's. For analysis, the nitrogen K-edge data is normalized to 1.0. The numbers noted on the right scale reflect the O:N ratio. (The percent composition values shown next to the HfSiON films refer to the HfO₂: SiO₂ ratios in the makeup of these films.

work function, suggesting that tunable workfunction systems are of high importance.

We are addressing the metrology needs for evaluation of candidate gate electrode metals by developing a test chip to provide test structures for the measurement of sheet resistance and work function, and a resolution pattern to enable measurement of workfunction via scanning Kelvin probe microscopy. We also are developing an internal photoemission measurement of barrier height.

DELIVERABLES: By the end of 2005, investigate characterization of dielectrics on semiconductors with SCM, TUNA, and Scanning Kelvin Probe. Develop test structures and measurement capabilities to measure with high accuracy metal gate work function and barrier height.

SILICON OPTICAL CONSTANTS AND ADVANCED SILICON MATERIALS

The project also conducts research into materials needed to extend CMOS beyond its current and conventional implementation. As part of this work, project members are using SE and Raman Scattering to characterize silicon-on-insulator materials, strained silicon, and other materials for confined silicon applications. We also have an effort to characterize silicon compatible light emitters and detectors.

The crystalline quality of bonded Silicon-On-Insulator (SOI) wafers is being examined by spectroscopic ellipsometry and Raman spectroscopy. Both techniques detect slight structural defects in the SOI layer. If a pure crystalline silicon dielectric function is assumed for the SOI layer, the SE data fitting yields an unacceptably large discrepancy between the experimental and modeled data. The best fits for all the samples result in a dielectric function of the SOI layer that consists of a physical mixture of crystalline silicon and about 4 % to 7 % of amorphous silicon. Using such a mixture indicates that there are still some defects in the SOI layer when compared with the high-quality bulk crystalline silicon. This observation is further supported by Raman spectroscopy measurements. The Raman spectra of all SOI samples exhibit a feature at about 495 cm^{-1} that is not observed in the crystalline silicon spectrum (see Fig. 11). Features similar to the 495 cm^{-1} feature have been reported in the literature and attributed to dislocations or faults in the silicon lattice

DELIVERABLE: Determine the structural qualities of Silicon on Insulator by SE and Raman Scattering. Q2, 2004

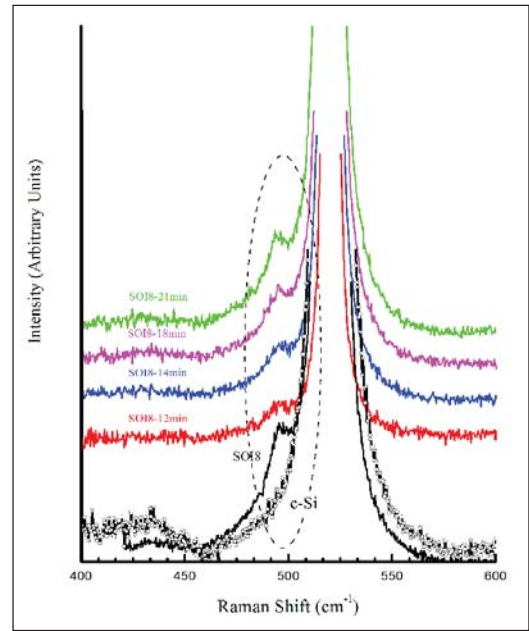


Figure 11. Raman spectra for all SOI8 samples.

ACCOMPLISHMENTS

■ **Enhanced Detection Limits for Trace Elements** – Secondary ion signals in SIMS are strongly dependent on the local chemistry of the sample. Oxygen gas backfilling of the analytical chamber is often used to enhance positive secondary ion yields for many metals of interest in semiconductor metrology. In some cases, the use of halogen containing gases, rather than oxygen, may lead to further sensitivity enhancements. To address this issue, pure metal and ion implant standards have been examined using Freon gas backfilling of the sample chamber. Preliminary data suggests that Cu and Zn are less enhanced under Freon exposure as compared with oxygen. The ion yields for Al, Ti, Fe, and Ni are similar under Freon and oxygen, but the ion yields for V, Cr, Mn, Zr, Nb, Mo, Ag, and under Freon enhancement is several times higher than that of oxygen. The sputtering rate under Freon flooding is about 2.5 times greater than oxygen flooding under similar sputtering conditions.

■ **Bevel Image Depth Profiling** – The NIST magnetic sector SIMS instrument has been modified to create custom ion-milled bevel cross sections in multilayer test structures, Fig. 12, using high energy O_2^+ bombardment. The use of an oxygen primary ion beam was found to minimize sputter rate variations between layers and to reduce sputter-induced topography. Subsequent removal of the implanted oxygen and subsurface mixed zone is accomplished using a novel low

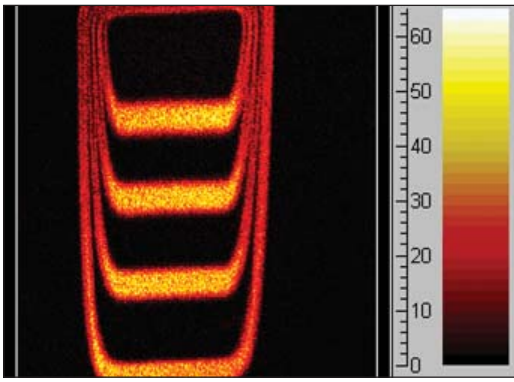


Figure 12. SIMS Image of Ni⁺ secondary ion signals from a bevel cross-section cut into a depth profiling reference material of alternating Cr/Ni layers on silicon. The bevel surface was treated with 100 eV Ar⁺ bombardment to reduce topography and minimize atomic mixing.

energy ion source designed by 4Wave Inc, Reston, VA, under a NIST Phase 1 SBIR grant. This approach provides a means to produce depth profiles that have higher depth resolution than is possible using conventional SIMS analysis using higher energy primary ion beams.

■ **SIMS Backside Depth Profiling of Test Pads on PMOS Patterned Wafers** – SIMS analyses of interlayer diffusion can be limited by mixing effects that occur during sputtering and by the formation of sputter-induced topography. To minimize ion mixing for the element of interest, it is desirable to sputter (analyze) from a direction of low concentration into a region of higher concentration. Often, this can only be accomplished by analyzing the semiconductor device from the backside. We have developed a procedure for backside SIMS analyses of patterned wafers using a mechanical grinding and polishing procedure to remove the silicon substrate before analysis. Since the features of interest (devices, test pads etc.) cannot be observed from the backside, their location must first be marked from the front side before sample preparation. Marking can be accomplished by ion sputtering to tag the features of interest and also aid with thickness determinations and planarity adjustments during mechanical preparation. This approach has been used to study the distribution of hafnium in a thin hafnium oxide film in patterned wafers in collaboration with International SEMATECH, see Fig. 13.

One potential problem with backside SIMS depth profiling is that it is difficult to achieve perfect planarity on the polished surface. Any tilt of the sample will distort the depth profile and degrade

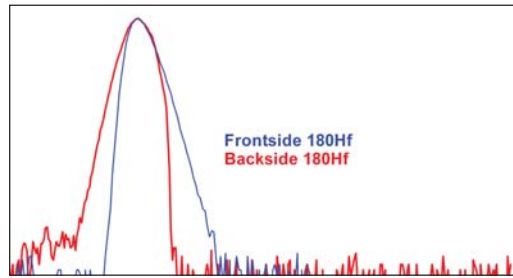


Figure 13. Comparison of a conventional SIMS depth profile (blue) with a backside SIMS depth profile (red) through a 10 nm thick hafnium oxide layer.

the apparent depth resolution, which can distort the depth profile. To identify and correct for the presence of sample tilt, we are utilizing 3-D image depth profiling. In this approach secondary ion imaging is combined with ion sputtering to produce a 3-dimensional distribution for the sample under examination. Any sample tilt is immediately apparent in the 3-D image. Using custom NIST written image processing software, the effect of tilt can be removed from the image stack. Depth profiles from the corrected stack can then be produced. Figure 14 is an example of a 3-D backside profile with an interface that is tilted with respect to the polished surface.

■ **Polyatomic Primary Ion Beam SIMS** – Studies of polyatomic primary ion beam sources for high depth resolution SIMS dopant profiling are continuing. Collaborations with International SEMATECH have focused on depth-profiling of novel ZrO₂ films on both magnetic sector and TOF-

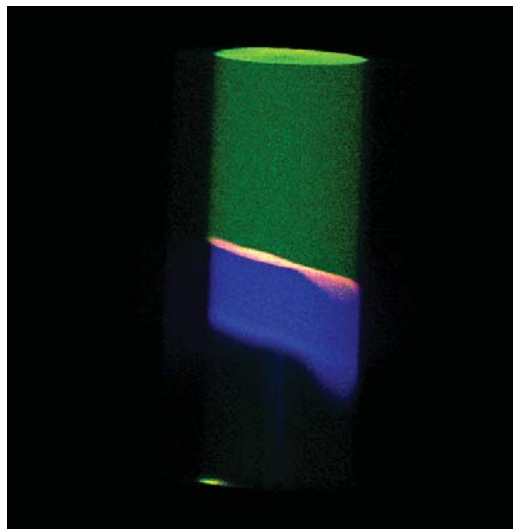


Figure 14. Three-dimensional backside SIMS depth profile of a multilayer stack consisting of TiN/ZrAlO/Si. Green-Si, Red-Al, Blue-Ti. 500 images in stack, each 250-µm in diameter.

SIMS instruments. A new polyatomic ion source is being built for the NIST magnetic sector SIMS instrument that is based on the production of a fullerene ion beam (C_{60}^+) using electron impact ionization. This source should allow for equivalent individual atom impact energies of a few tens of electron volts resulting in almost no penetration of the cluster ion below the surface of the sample. It is hoped that this development will provide significant improvements in available depth resolution.

■ **SiGe Compositional Standards** – SiGe specimens cut from single-crystal boules normal to the growth axis were obtained from Virginia Semiconductor. The nominal compositions were 3.5 at. % Ge in Si, 6.5 at. % Ge in Si, and 14 at. % Ge in Si. The wafers were evaluated with the electron probe microanalyzer (EPMA) for micro- and macroheterogeneity for use as primary standards for characterization of SiGe thin films on Si that are needed by the microelectronics industry as reference standards. The specimens were rigorously tested with wavelength dispersive spectrometers (WDS) using multiple point, multiple sample, and duplicate data acquisitions. On each specimen two 40-point traverses normal to one another were prepared at two randomly selected locations with steps of 2 μm or 5 μm between points. Such traverses are routinely prepared during heterogeneity testing to determine if distinct phases across short distances (5 μm to 100 μm) within specimens are present. In addition random sampling tests on each specimen were run to evaluate the overall specimen heterogeneity. The expanded uncertainties (3σ) in percent mass fraction determined from data for each specimen ranged from 1–2 % in $\text{Si}_{.86}\text{Ge}_{.14}$ to as high as 15 % in $\text{Si}_{1.965}\text{Ge}_{.035}$. The $\text{Si}_{.86}\text{Ge}_{.14}$ was chosen as the primary standard for the SiGe films on Si due to the low heterogeneity of this material for which the maximum expanded uncertainty due to heterogeneity is no greater than 1.5 % relative mass fraction for Ge and considerably less for Si.

■ **HRTEM Studies of Gate Dielectrics** – Because high-resolution transmission electron microscopy (HRTEM) relies on a complex contrast mechanism to produce images of gate dielectric films in cross section, there are many factors affecting the uncertainty of thickness measurements based on these images. A preliminary survey revealed approximately 50 parameters that affect the uncertainty in a gate dielectric dimensional metrology experiment using HRTEM, along with approximately 1,200 two-term interactions and almost 20,000 three-term interactions. Using established

design-of-experiment (DEX) methodologies, a screening experiment based on a 2IV (8-4) fractional factorial design was performed to determine which factors had the greatest impact on the absolute error of the thickness measurements. Absolute error was determined by simulating HRTEM micrographs using a multislice calculation. The model used for the simulation consisted of a variable SiO_2 film approximately 2 nm thick positioned between two pieces of crystalline Si. This approximation to a gate stack was built atom-by-atom using commercial molecular modeling software supplemented with custom Tcl scripts to assemble the gate structures from simpler primitives. By varying the molecular model, sample parameters such as crystallographic orientation, film thickness, density, and along-beam thickness can be varied precisely. Instrument parameters and details of the imaging conditions are inputs to the multislice calculation, a simulation technique that has been vetted by the microscopy community and has been in use for decades. Beam tilt, defocus, and vibration amplitude were the main factors found to have the largest effects, while beam-tilt, defocus and defocus vibration were the most important two-term interactions (see Fig. 15).

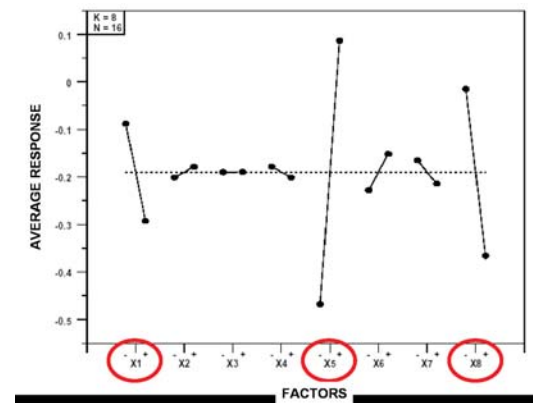


Figure 15. Main Effects Plot showing the importance of each of the input parameters X1 through X8. The information conveyed is qualitative: important variables exhibit a large slope. Based on this data, factors X1 (Beam tilt), X5 (defocus), and X8 (vibration amplitude), (all circled) have a significant effect on the thickness measurement error.

■ **Optically Pumped SCM for Carrier Lifetime Measurements** – Implemented optical pumping and voltage spectroscopy of scanning capacitance microscopy for local measurement of carrier lifetime. Using a pulsed laser and precisely synchronized SCM measurements of the induced capacitance transient, local carrier lifetime can be measured with spatial resolution limited only by

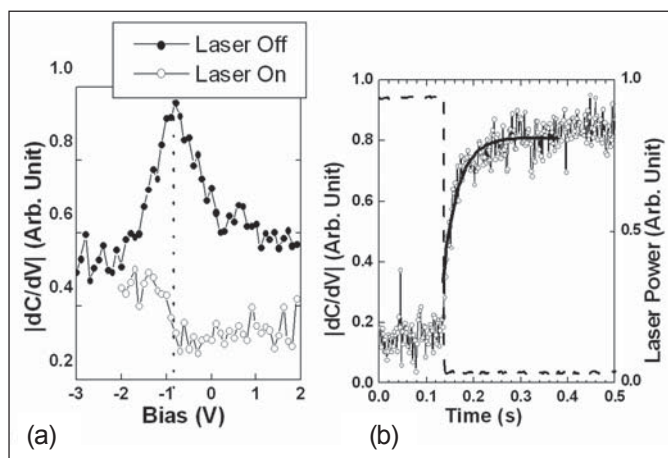


Figure 16. a) dC/dV curves between the SCM tip and silicon with a thin oxide layer, measured with the AFM laser on and with the AFM laser off (after achieving equilibrium). b) Transient capacitance signal as measured as a function of time. The laser power intensity (dashed line) is monitored to synchronize precisely the measured transient with the change in illumination. An estimate of carrier lifetime can be estimated from an exponential fit to the measured transient.

the carrier diffusion length, Fig. 16. Details of the technique were published in Applied Physics Letters and a patent application is in progress.

■ **Developed Local C-V Measurement Techniques** – Local C-V measurements with the SCM are being used for the characterization of high- κ dielectric films on silicon and native oxides on wide bandgap semiconductors. An invited paper was presented at the Interfaces in Electronic Materials Symposium at the Fall 2003 Electrochemical Society Meeting.

■ **First Non-Contact Measurement of Diffusion Length in GaN** – Measured, for the first time, diffusion length of GaN using the Surface PhotoVoltage technique. Presented data at the Materials Research Society 8th Wide-Bandgap III-Nitride Workshop and at the 2004 American Physical Society March Meeting.

■ **Observed Residual Defects in SOI** – Completed SE and Raman measurement and analysis of a set of Semiconductor-On-Insulator (SOI) wafers. From SE and Raman scattering data, we have shown that the SmartCut SOI wafers contains slight structural defects in the SOI layer. These defects manifest a slightly different dielectric function used for the SOI layer in the SE data analysis and the observation of a weak extra feature at 495 cm^{-1} in Raman spectrum that is not observed in the spectra of device quality crystalline silicon

substrates. Two manuscripts for this work were submitted in FY2004, one to Applied Physics Letters, and the other to Materials Research Society Spring 2004 Meeting Proceeding. Also the work was presented at the same MRS meeting.

■ **Phase Transition in ZrO_2 films due to Anneal and Film Thickness** – Completed SE measurements and data analyses on two series of ZrO_2 in collaboration with the University of Minnesota, and Stanford University. Two significant results from this study are: (i) optical bandgap and the dielectric function of ZrO_2 increase with increasing film thickness; (ii) optical bandgap and the dielectric function of ZrO_2 increase when annealed at high-temperatures; and (iii) it is believed that the ZrO_2 phase changes from the amorphous state to the tetragonal polycrystalline state

when the film thickness is greater than 80 Angstroms or the film is annealed at temperature above $\sim 600\text{ }^\circ\text{C}$. A manuscript concerning the physical characterizations has been submitted to Applied Physics Letters. Another manuscript focusing on the optical properties will be submitted later in 2004.

■ **Compositional Effects on the Properties of High- κ Dielectrics** – Completed an extensive set of spectroscopic ellipsometry, soft X-ray photoemission, inverse photoemission, and TEM measurements on a specially designed set of SiO_2 , SiON , HfO_2 , HfSiO_2 , and HfSiON films. This study is intended to investigate the effect of compositional components particularly Hafnium and nitrogen on the dielectric function, band-gap, band offsets and near band-edge density of states, and well the ability to determine nitrogen concentration from ellipsometry measurements.

■ **Comparison of Oxide Thickness by Various Methods** – Completed comparison of oxide thickness determination methods of 2 nm SiO_2 films by Ellipsometry, C-V, and HRTEM/STEM. Determined that the dominant uncertainty in ellipsometer-based thickness (due to choice of optical model and best optical constants for the silicon substrate and the oxide film) was less than the uncertainty in C-V based thickness (due to differences resulting from available Q-M corrections for 2-D quantization of states in the silicon substrate and poly-

layer depletion). However, the largest overall uncertainty in trying to establish a unification of optical, electrical, and physical thickness scales and a relation to absolute SI-unit based thickness determination results from the uncertainty of HRTEM-based thickness (approximately ± 0.2 nm).

■ **Traceability of SiO₂ Film thickness to the SI unit of Length** – Completed participation in the first round of an international, multimethod investigation of the ability to measure the thickness of very thin SiO₂ films traceable to the SI unit of length. Participants included representatives from eight national laboratories. Spectroscopic and single-wavelength ellipsometry measurements, and TEM were contributed by project members. Other laboratories also contributed ellipsometry measurements as well as XPS, Neutron-reflection, Medium Energy Ion Scattering, X-ray reflectivity, SIMS, RBS, and TEM. Results, analyzed by the sponsoring laboratory, England's NPL, were sufficiently encouraging, that a formal "key comparison" is planned.

■ **SE Measurements of Confined Silicon** – Completed SE measurement and analysis for a set of quantum dot devices consisting of amorphous silicon films grown over a SiO₂/c-Si substrate. Bandgaps were extracted and correlated with Si film thickness and growth temperature. Good agreement was found between SE and TEM thickness values. This work was presented at the spring 2003 MRS meeting.

COLLABORATIONS

ATMI – ellipsometry on GaN, AlN (Nguyen)

Arizona State University, Candi Cook – Photorefectance measurements of Ge:Sn:Si samples (Chandler-Horowitz)

Army Research Lab, SEDD, Kenneth Jones – GaN and SiC device, process, and material characterization (Kopanski)

Brooklyn Polytechnic, Dr. F. Pollack – Photorefectance of FeSi₂ (Birdwell)

4 Wave Inc. – Phase 1 SBIR to develop low energy ion beam milling of high-energy ion beam cut bevels.

FM Technologies – High brightness oxygen ion source for 2-D dopant profiling by SIMS

IBM, E. Gusev – Study of high- κ materials (Ehrstein, Nguyen, Sayan)

International SEMATECH, Joe Bennett – Thin oxide depth-profiling by SIMS, backside depth profiling of patterned PMOS wafers

International SEMATECH, P. Y. Hung – SE of high- κ dielectrics (Nguyen), B. Foran, Metrology of Film Thickness (Ehrstein)

Ionoptika – Development of a C₆₀⁺ primary ion source for advanced semiconductor technology

MicroFAB Inc – Advanced inkjet printing technology for deposition of trace metal standards on silicon surfaces

NIST, 836 Process Measurements Division, J. Maslar and Roger van Zee – Molecular electronic thin film (SAM films) (Nguyen)

NIST, 837, T. Jach – Development of Kelvin Probe for Electrode Metal Work Function (Sayan)

NIST, 852, I. Levin and D. Fischer – Study of High- κ Films (Sayan); L. Robins – Photorefectance measurements (Chandler-Horowitz)

NIST, 855, A. Davydov – Characterization of contacts to GaN (Kopanski); Study of high- κ films (Sayan)

NIST, 856, J. Dura – Film Thickness Metrology (Nguyen)

Northrop-Grumman, Joe Giagante – Boron and Aluminum implanted silicon carbide for dopant profiling with SCM and SSRM (Kopanski)

Northrop Grumman Corp., Advanced Technology Laboratories, Anthony Margarella – oxynitride film characterization (Nguyen)

Peabody Scientific – Ion source development for SIMS

Pennsylvania State University, Prof. Robert Collins – SE modeling (Nguyen)

Rutgers University, E. Garfunkel, R. Bartynski – (Nguyen, Sayan)

Stanford University, P. J. McIntyre – (Ehrstein, Sayan)

Texas Instruments Inc., Dr. J. Chambers and Dr. M. Visokay – (Ehrstein, Sayan)

UCLA, Prof. J. Chang – (Nguyen)

University of Delaware, Prof. R. Opila – (Sayan)

University of Minnesota, Prof. Campbell – (Ehrstein, Sayan)

University of Texas, Austin, Prof. Jack Lee, Ellipsometric characterization of high- κ films (Nguyen)

Yale University, Prof. T. P. Ma, Ellipsometric characterization of high- κ films (Nguyen)

RECENT PUBLICATIONS

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N. V. Nguyen, J. E. Maslar, Jin-Yong Kim, Jin-Ping Han, Jin-Won Park, D. Chandler-Horowitz, and E. M. Vogel, "Characterization of Structural Quality of Bonded Silicon-On-Insulator Wafers by Spectroscopic Ellipsometry and Raman Spectroscopy," *MRS Spring 2004 Conference Proceedings* (2004).

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CHEMICAL METROLOGY OF MATERIALS AND PARTICLE CONTAMINATION

GOALS

Develop methods, standard materials and data for the characterization of the elemental composition, crystallographic phase, and chemical structure of microelectronic thin films and particle contaminants at nanometer spatial resolution. We develop and test X-ray, Field Emission Gun Scanning Electron Microscopy (FEGSEM), Transmission Electron Microscopy (TEM), X-ray Photoelectron Spectroscopy (XPS), Auger-Electron Spectroscopy (AES), Scanning Probe Microscopy (SPM) and diffraction methods to characterize the chemical composition and phase of microelectronic components and particle contaminants. Standard materials and data are developed to support these methods and enable improved accuracy and applicability of these methods to microelectronic devices.

CUSTOMER NEEDS

The constant introduction of new materials (SiGe, oxynitride, novel high- κ , low- κ , Cu, etc.) and decreasing dimension size in semiconductor fabrication cause increasing demands for new, selective, quantitative, interface and thin film metrology tools. Typically, many of these same measurement tools are applied to identify particle contaminants in the Fabs. There is a critical need to attain better speed and accuracy of chemical information from thin and chemically complex layered materials. The development of faster methods with known accuracy and the development of standards to demonstrate and maintain the quality of chemical analysis methods is critical to the continuous advancement of semiconductor technology.

The challenges and needs are outlined in the metrology section of the 2003 International Technology Roadmap for Semiconductors on page 29. "The rapid introduction of new materials, reduced feature size, new device structures, and low temperature processing continues to challenge materials characterization and contamination analysis. Correlation of appropriate offline characterization methods with each other and with inline physical and electrical methods should be accelerated. Use of characterization methods to provide more accurate information such as layer thickness or elemental concentra-

tion will continue. Characterization methods will continue to move toward whole wafer measurement capability and clean room compatibility."

TECHNICAL STRATEGY

1. Reference Data for AES and XPS – chemical characterization using AES and XPS depends on reference data for interpretation of measurements and an understanding of the physics of X-ray and electron interactions with semiconductor materials for modeling AES and XPS experiments with complex structures.

Standard Reference Database (SRD) 20 provides identification of unknown spectral lines in user measurements, retrieval of data for selected elements, retrieval of data for selected compounds, and retrieval of data by scientific citation.

SRD 64 provides values of differential elastic-scattering cross sections, total elastic-scattering cross sections, phase shifts, and transport cross sections for elements with atomic numbers from 1 to 96 and for electron energies between 50 eV and 300 keV. These data are needed for modeling the transport of signal electrons in AES and XPS; in addition, they can be used for modeling electron transport in resists utilized in electron-beam lithography.

SRD 71 provides values of electron inelastic mean free paths (IMFPs), generally for electron energies between 50 eV and 2,000 eV. IMFPs are needed for quantitative analyses by AES and XPS, for deducing the surface sensitivity, and for modeling the transport of the signal electrons.

SRD 82 provides values of electron effective attenuation lengths (EALs) and related data for AES and XPS. EALs are needed mainly for measurements of thicknesses of overlayer films. Since XPS is being used to an increasing extent for the characterization of new gate-oxide materials, EALs have been computed from SRD 82 for zirconium dioxide, zirconium silicate, hafnium dioxide, and hafnium silicate for common XPS measurement conditions.

NIST is developing a new database (SRD 100: Simulation of Electron Spectra for Surface Analysis (SESSA)) to be used for AES and XPS analyses of thin-film structures. This database includes data from SRD 64 and SRD 71 and additional data

Technical Contacts:

E. B. Steel
C. J. Powell

"Researchers in the Microanalysis Research Group continue to drive the commercialization of new X-ray detectors for materials microanalysis. The new silicon drift detectors, whose development is being supported and encouraged by the group, will allow unprecedented high-count X-ray detection. The semiconductor industry eagerly awaits the availability of commercial instrumentation, first for laboratory analysis applications, then eventually for online defect identification and classification."

Anne Testoni,
KLA-Tencor

describing X-ray and electron interactions with solids. SESSA will enable comparisons to be made of measured and simulated spectra for user-specified specimen morphologies and analytical conditions.

DELIVERABLES: Develop new database for interpreting AES and XPS data from thin-film structures. 3Q 2004

2. New X-ray Technology – Silicon Drift Detectors: A prototype of a silicon drift detector energy dispersive X-ray spectrometer (SDD-EDS) developed by Photon Imaging, Inc. of Los Angeles under a NIST Phase II SBIR grant is being tested on a scanning electron microscope (SEM) at NIST, Fig. 1. Conventional silicon (lithium) EDS forms the backbone of X-ray microanalysis systems implemented on more than 25,000 SEMs worldwide. Conventional EDS is limited to a maximum count rate of approximately 25,000 per second and is usually cooled with liquid nitrogen. The new SDD-EDS technology is capable of limiting count rates of 1MHz with 150 eV energy resolution and operates at -70 C, which is achieved with Peltier cooling. The SDD-EDS detection area is also physically large. Individual detector chips are 50 mm², and assemblies of multiple chips are possible. The combination of a large solid angle and a high-count rate are expected to lead to increased efficiency for SEM/X-ray microanalysis. The high count rate capability of SDD-EDS will be especially important for elemental mapping, where the number of photons counted per image pixel defines the concentration level that can be detected.

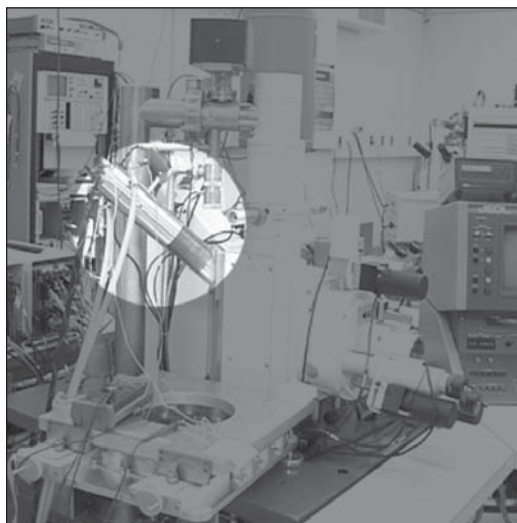


Figure 1. Silicon drift X-ray detector (highlighted oval) on conventional SEM.

DELIVERABLES: Install and test second generation SDD detector system on UHV Auger microscope. Q1 2004

3. New X-ray Technology – Microcalorimeter-EDS: The microanalysis laboratory at NIST Gaithersburg, Maryland is working as a Beta-test site for the NIST-Boulder, Colorado μ cal EDS system (discussed elsewhere). The system has been outfitted with a second-generation Cu-Mo thermometer rather than the first-generation Al-Ag. Immediately after installation of the new detector, the NIST Boulder staff obtained 7 eV resolution on Al. The NIST Gaithersburg staff was then instructed on the operation and maintenance of the cryogenic systems and the adjustment of the cryoelectronics, including the SQUID array, that are critical to obtaining optimum performance.

The initial thrust of the research for the application of this high resolution X-ray detector is in the development of fundamental X-ray data including X-ray weights of lines and peak shape and energy shifts. While the characteristic X-ray energies above about 3 keV are reasonably well known, the energy and especially the relative intensity of lower energy X-ray lines in L and M shell X-rays are not well known and causes significant uncertainty and bias when analyzing complex thin film systems, *e.g.*, W-Si. The characteristic peak energy can shift and peak shape can change as a function of chemical bonding allowing the possibility of chemical compound identification and mapping using the microcalorimeter. A feasibility study of a new database for chemical X-ray data is being initiated.

The development of these standard X-ray data systems requires that we first establish a reproducible response function in intensity and energy for the detector.

DELIVERABLES: Test modifications to the microcalorimeter temperature regulation system to determine if they improve detector stability. 1Q 2004

4. Characterization of particles: We are developing two areas of metrology for particles – quantitative chemical analysis using electron and X-ray spectroscopies and quantifying morphology through image analysis of electron microscope images.

The quantitative elemental characterization and identification of nanometer and micrometer-sized particles is critical to defect control. In the chemical analysis of particles with electron-beam instruments, the size and shape of the particle often

results in large analytical errors associated with X-ray emission and absorption. Over the years, several different researchers have developed correction procedures to minimize the uncertainties associated with particle analysis. Although these correction procedures reduce the effects of particle geometry, elemental concentrations determined from the quantitative analysis of particles by these methods are often accompanied by errors on the order of 10 % to 50 % relative compared to 3 % to 5 % relative errors for the analysis of conventional samples. We are investigating the advantages and disadvantages of low voltage electron beam analysis, schematically shown in Fig. 2.

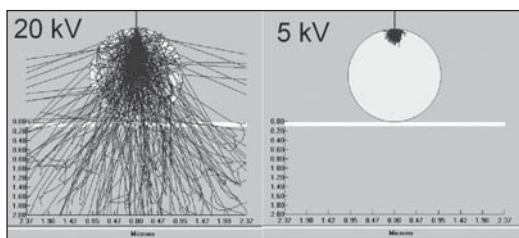


Figure 2. Schematic results of Monte Carlo calculation of electron beam interaction with a two micrometer particle sitting on substrate.

In addition to using chemical composition to classify particles, the shape and surface texture of a particle can help to classify or identify it and may also be indicative of its chemical composition or the process through which it was created. Shape and texture are used routinely by humans viewing objects, while many image analysis approaches currently only use a handful of parameters, such as roundness or root mean square roughness. Since the fractal dimension of a boundary or surface seems visually related to its roughness or tortuosity respectively, we are investigating the applicability of these dimensions for the description of the shape and texture of individual grains of particulate matter. These physical objects by their very nature do not have true fractal shapes, but we hope that they do exhibit fractal-like behavior in a limited size range (the “local fractal dimension” or LFD). After investigation of some image processing methods in the literature, we have chosen and refined two, to characterize the LFD of the projected boundary of a particle and the LFD of an averaged brightness profile representing the surface. These measurements require the particle to be segmented from background, a tedious task to perform manually and a problematic one to do automatically.

We have developed operator-aided segmenting methods that are designed for the image data sets under study.

DELIVERABLES: Develop an accurate quantitative analysis procedure for high-angle X-ray emission spectroscopy to allow simultaneous combined X-ray/EBSD phase mapping and X-ray elemental analysis.

ACCOMPLISHMENTS

- The new NIST Database for Simulation of Electron Spectra for Surface Analysis (SESSA) was utilized for calculations of electron effective attenuation lengths (EALs) for thin films of hafnium dioxide on silicon (the EAL is needed for measurements of film thickness by XPS). These EALs, calculated from Monte Carlo simulations for excitation of Si 2p photoelectrons excited by Al K α X-rays, generally agreed well with values obtained from the NIST Electron EAL Database (SRD 82) that is based on a more approximate analytic approach. Deviations of up to 10 % in EAL values were found for HfO₂ film thicknesses less than 2 nm. This comparison indicates that SESSA will be valuable for measurements of high- κ gate-oxide thicknesses by XPS because approximations in the algorithm of SRD 82 are less valid in this application than for thin films of SiO₂ on Si.

- An extensive analysis has been made of differential elastic-scattering cross sections obtained from two commonly used atomic potentials. This analysis has shown that cross sections derived from the Dirac-Hartree-Slater potential are more accurate than those from the commonly used Thomas-Fermi-Dirac potential. Cross sections from the former potential are now available in the NIST Electron Elastic-Scattering Cross-Section Database (SRD 64) for electron energies from 50 eV to 300 keV. These cross sections can be used for simulations of electron transport in AES and XPS and in electron-beam lithography.

- It has been known for many years that backscattered electrons have to be considered in quantitative AES. For high-spatial-resolution scanning Auger microscopy (SAM), however, the backscattered electrons need to be considered in “point” analyses (e.g., of a defect) because appreciable signal can arise from signals created by backscattered electrons in the surrounding matrix. The radius of the analysis area (for a defined fraction of the total Auger-electron signal) has been estimated both from a simple model calculation and from Monte Carlo simulations.

This radius can be appreciably larger (by more than a factor of 10) than the radius of the primary beam. In critical SAM analyses, the primary-beam energy will need to be adjusted for optimum spatial resolution for the feature of interest while minimizing the matrix Auger signal excited by backscattered electrons.

- The Microcalorimeter energy-dispersive X-ray spectrometer has an inherent resolution that is vastly superior to other energy-dispersive X-ray spectrometers, but its performance is highly sensitive to its operating environment, particularly its temperature and electrical supplies. As indicated in last year's report, "long term (>100 s) measurements have been found to be subject to instability that limits accurate measurements of X-ray peaks." Commercial versions are available which achieve a resolution of 20 eV, but this requires recalibrating the shifting energy scale continuously. A group of scientists at NIST, Gaithersburg have been evaluating ways in which the Microcalorimeter can be stabilized to achieve higher resolution without constant recalibration over the long periods necessary to analyze microscopic inclusions in a sample. By stabilizing the temperature of the detector to 1 part in 1000, they have been able to obtain X-ray spectra over periods of many hours which show a resolution of 12 eV and a drift less than 2 eV (see Fig. 3). This performance is a considerable improvement over conventional detectors for the desired operating periods.

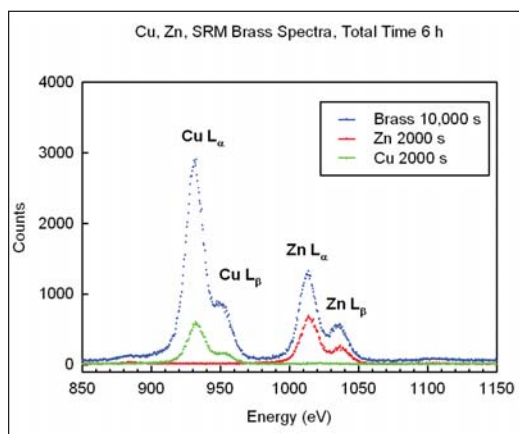


Figure 3. 10,000 s X-ray spectra of brass overlapped on 2000 s spectra for Cu and Zn showing detector stability over a 6 h time period.

- The Silicon Drift X-ray Detector has been used successfully to collect a 256x256 spectrum image with total mapping time of approximately 650 s. This compares to a collection time of

approximately 2 hours using a conventional monolithic Si detector. We are actively working with Photon imaging to develop a faster pulse processing system.

- We have evaluated the X-ray analysis of particles at low accelerating voltages (5 keV). Results indicate that the effects of particle morphology increase as a result of X-ray absorption requiring careful alignment of the particle under the electron beam to minimize the magnitude of the absorption.

COLLABORATIONS

Institute of Physical Chemistry (Warsaw), Jablonski, development of databases for AES and XPS; calculations of backscattering factors (for scanning Auger microscopy), effective attenuation lengths (for measurement of film thicknesses by AES and XPS), and differential elastic-scattering cross sections (for Monte Carlo simulations of electron transport in AES and XPS and in electron-beam lithography).

University of Barcelona, Salvat, calculations of differential elastic-scattering cross sections (for Monte Carlo simulations of electron transport in AES and XPS and in electron-beam lithography).

Institute of General Physics, Technical University of Vienna, Werner, development of the new NIST database for simulation of electron spectra for surface analysis by AES and XPS.

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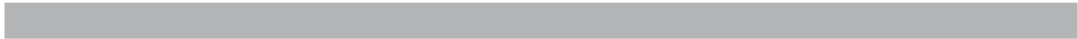
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INTERCONNECT AND PACKAGING METROLOGY PROGRAM

Advances in interconnect and packaging technologies have introduced rapid successions of new materials and processes. Environmental pressures are leading to the reduction and eventual elimination of lead in solder used for attaching chips to packages and packages to circuit boards. The overall task of this program is to provide critical metrology and methodology for mechanical, chemical, metallurgical, electrical, thermal, and reliability evaluations of interconnect and packaging technologies.

The function of packaging is to connect the integrated circuit to the system or subsystem platform, such as circuit board, and to protect the integrated circuit from the environment. The increasing number of input/output (I/O) on circuits with vastly larger scale of integration is forcing ever smaller I/O pitches, the use of flip chip bonding, and the use of intermediary platforms called interposers. The integration of sensors and actuators onto integrated circuits through MEMS technology and the increasing use of low cost integrated circuits in harsh environments is increasing the complexity of the packaging task. Environmental concerns are forcing the need for development of reliable lead-free solder and other low environmental impact packaging materials.

System reliability requirements demand modeling, testing methods, and failure analysis of the integrated circuits before and after packaging. Metrology is a significant component of reliability evaluation.



ATOMIC LAYER DEPOSITION – PROCESS, MODELS, AND METROLOGY

GOALS

Develop validated, predictive process models and *in situ* metrologies for atomic layer deposition processes.

CUSTOMER NEEDS

Atomic layer deposition (ALD) is increasingly being utilized as a method of depositing the thin (nanometer-scale), conformal layers required for many microelectronics applications, including high- κ gate dielectric layers, diffusion barrier layers, copper seed layers, and DRAM dielectric layers. However, significant developmental issues remain for many of these applications.

One potential solution to some ALD developmental issues is technology computer-aided design (TCAD). TCAD has been identified in the 2003 *International Technology Roadmap for Semiconductors (ITRS)* as “one of the few enabling methodologies that can reduce development cycle times and costs.” [2003 *ITRS, Modeling and Simulation, page 1*] Important aspects of TCAD include “simulation tools that predict physical properties of materials and, in some cases, the subsequent electrical properties”; and a “hierarchy of models which allows the simulation of the local influence of the equipment (except lithography) on each point on the wafer, starting from the equipment geometry and settings.” [2003 *ITRS, Modeling and Simulation, page 1*] Further, it is expected that “Simulations that can predict the impact of process conditions of film morphology as well as interface characteristics will become increasingly important.” [2003 *ITRS, Modeling and Simulation, page 15*] However, many difficult challenges to development of validated, predictive ALD process models that allow prediction of equipment influences on film properties have been identified, including “Fundamental physical data (e.g., rate constants, cross sections, surface chemistry); reaction mechanisms, and reduced models for complex chemistry.” [2003 *ITRS, Modeling and Simulation, Table 121, page 2*] In addition to a lack of quality fundamental physical and chemical data, experimental validation has been identified as a “key difficult challenge across all modeling areas.” [2003 *ITRS, Modeling and Simulation, page 1*] Further, with respect to experimental validation, “The

major effort required for better model validation is without doubt sensor development.” [2003 *ITRS, Modeling and Simulation, page 15*] This project is an attempt to assist in solving some ALD developmental issues by developing validated, predictive process models and associated *in situ* metrologies for ALD processes.

TECHNICAL STRATEGY

This project involves two primary directions: development of *in situ* metrologies sensitive to ALD chemistry and development of ALD chemical reaction mechanisms. These two directions are seen as mutually-supporting. It is expected that experimental results that elucidate ALD chemistry will aid in chemical mechanism development and ultimately in process model validation. Further, it is expected that the most important reaction species will be identified as understanding of a particular ALD reaction improves, thus facilitating the design of improved process metrologies.

Ultimately, aspects of both of metrology development and reaction mechanism development will be required to create validated ALD process models. ALD process models would be created by incorporating the chemical reaction mechanisms developed here into commercially available computational fluid dynamics code and then validating the process model under a range of parameters using experimental data collected in the course of this project. Initial reaction mechanism development will focus on Al_2O_3 ALD deposition.

While these two directions will be closely coupled for development of a specific ALD chemical reaction mechanism, this will not preclude exploration of non-mutually-supporting aspects of the metrology development and model development directions. For example, fundamental thermochemical and chemical kinetic properties of numerous organometallic compounds potentially suitable for ALD are under investigation. However, it would not be feasible to simultaneously provide experimentally validated ALD process models for all compounds.

1. The first step in providing validated ALD process models is evaluating the suitability of diagnostics that are sensitive to ALD chemistry. Mass spectrometry and optical spectroscopic tech-

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niques are of particular interest because of their potential for in situ monitoring. Mass spectrometry is relatively straight-forwardly integrated with an ALD reactor and, when in situ diagnostics are applied to ALD reactors, mass spectrometry is frequently employed. However, mass spectrometry is only sensitive to volatile species and, hence, it is sometimes difficult to relate the species detected to mechanisms of interest on the growth surface. Because of the desire to directly probe ALD surface chemistry, Raman spectroscopy and infrared spectroscopy are also being investigated as potential ALD diagnostics. However, it is technically challenging to apply Raman and infrared spectroscopy to detect species present at monolayer quantities. For this reason, the suitability of these techniques is being evaluated using research-grade ALD reactors with optimized optical accessibility. After various diagnostics are evaluated in test ALD reactors, a more industrially-relevant ALD reactor will be designed and built. Suitable diagnostics will be integrated into this reactor to provide data that will aid in chemical mechanism development and overall process model validation.

DELIVERABLES: Fabrication of pulsed ALD precursor delivery system [3Q 2004]. Performance of in situ optical spectroscopic measurements during ALD processes [4Q 2004]. Interface of mass spectrometer with ALD chamber. 4Q 2004

2. The calculation, estimation, and dissemination of fundamental thermochemical and chemical kinetic properties of organometallic compounds with potential application to ALD, as well as chemical vapor deposition (CVD), processes is on-going. The thermochemical properties and reaction kinetics of most useful organometallic compounds and related molecular precursors are poorly characterized. This project obtains these properties through three activities involving theoretical estimations and modeling studies. The first data activity, which is in coordination with the Standard Reference Data Program, compiles and evaluates currently available thermochemical data of organometallic compounds and related precursors. This data is available through a NIST Website: <http://srdata.nist.gov/ckmechx/>. The second activity supplements available data by using *ab initio* and semi-empirical calculations to develop reaction mechanisms from computed molecular structures, thermodynamic properties and spectroscopic properties of Group III and Group V compounds. The third activity utilizes the experimental and computed thermochemical

and chemical kinetic data to develop mechanisms for the decomposition of organometallic precursors.

DELIVERABLES: Extend current bibliography pertaining to aluminum and aluminum oxide ALD and CVD with thermochemical, chemical kinetic, and mechanistic information to related deposition systems involving other metal, metal oxide, and metal nitride containing metals such as Sc, Ti, Zr, Nb, Hf, Ta, Zn, Mg, Pb, and Sn. Tag these references with appropriate keywords and make available through Standard Reference Data website. Compile bond dissociation energies from the literature, both experimental and calculated, for boron, aluminum, indium and gallium hydrides, alkyl hydrides, and chlorohydrides. 1Q 2004

Complete series of *ab initio* and density functional theory (DFT) calculations for reference compounds relevant to aluminum hydrides and alkyl aluminum hydrides. Initiate overview report of thermochemical, chemical kinetic, and mechanistic data available in the literature for these systems. Provide basic, initial detailed chemical kinetic model for thermal decomposition and radical-mediated reactions involving aluminum hydrides and alkyl aluminum hydrides based on Rice-Ramsperger-Kassel-Marcus theory (RRKM) calculations for rate expression employing *ab initio* transition states (and literature data when available). 2Q 2004

Complete initial draft of overview report of mechanistic information in literature pertaining to these systems. Provide refined detailed chemical kinetic model for decomposition of alkyl aluminum hydride precursors. 3Q 2004

Perform *ab initio* calculations necessary to develop rudimentary model for gas phase reactions involving H₂O and alkyl aluminum hydride species. Develop simple model involving surface chemistry of alkyl aluminum hydride and oxygenated (H₂O-mediated) species. 4Q 2004

ACCOMPLISHMENTS

- ALD Reactor Construction — Research-grade, optically-accessible ALD reactors with associated vacuum systems have been assembled and tested: one designed for Raman and one designed for infrared spectroscopic measurements.
- ALD Reactor Modeling — An axisymmetric computational fluid dynamics model has been developed based on the dimensions of the experimental ALD reactor(s). Numerical solutions have been obtained for flow and a heated substrate (no chemistry yet). Modeling of trimethyl-aluminum chemistry for Al₂O₃ ALD has begun.
- Optical Measurements — Optimization of the Raman spectroscopic optical system for in situ measurements is complete. The system was qualified with different (non-ALD) monolayer films in

an attempt to establish the sensitivity of the optical system. Optimization of the infrared spectroscopic optical system is on-going.

■ **Chemical Properties Calculations**—Molecular structure and vibrational frequency data for a number of Group III and Group V hydrides, alkyl hydrides, and chlorohydrides (stable molecules and radicals) have been compiled. *Ab initio* and DFT calculations for many of these molecules have been performed using a range of methods and compared with available experimental data. Transition state calculations involving unimolecular and bimolecular decomposition pathways for aluminum and indium hydrides and alkyl hydrides have also been performed in order to elucidate the mechanisms for decomposition of these species. RRKM calculations have been performed employing transition state structures for many of these reactions in order to provide temperature dependent rate expression for use in detailed chemical kinetic models. A new model has been developed for the gas phase decomposition of these species and is in the process of being refined through simulations in a model reactor. This model is to be extended to include oxygenated species (H_2O) and rudimentary surface chemistry.

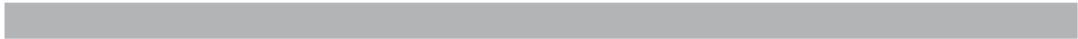
■ **Database Website** — A Website <http://srdata.nist.gov/ckmech/> (external) and <http://h105097.nist.gov/ckmech/> (internal) has been made available through the NIST Standard Reference Data website. This site currently contains bibliographic and thermochemical information of silicon hydrides, halocarbons, and organometallic compounds important to semiconductor processes, including information pertaining to ALD and CVD of aluminum, aluminum oxide, and other related ALD systems (*e.g.*, Ti, Zr, Hf, etc.), as well as a significant amount of information pertaining to hydrocarbon-based reactions. The plan for this site is to have it provide all data necessary to support chemical mechanisms of significance to the industry. The current version of CKMechX has a number of capabilities. Over 4000 enthalpies of formation are available for more than 1000 species with over 5000 bibliographic citations. These data were taken from NIST compilations and evaluations of silicon hydrides, silicon oxyhydrides, hydrocarbons, fluorinated hydrocarbons, and chlorinated hydrocarbons.

■ This ALD project relies heavily on experience obtained in the course of a previous project investigating silicon thermal CVD via silane py-

rolysis. That CVD project also involved development of chemical reaction mechanisms and experimental measurements to support mechanism development and process model validation. Multiple CVD process models were constructed employing the silane pyrolysis mechanisms, including gas phase nucleation of silicon particles, developed during this project and validated using the experimental results obtained in the course of this project. The different models employed reaction mechanisms of varying complexity and reactor geometries of varying dimensionality. Experimental measurements were performed in a vertical flow, rotating disk reactor under various process conditions. Gas temperature profiles were determined using rotational Raman spectroscopy. Gas phase silicon particle spatial distributions were determined with elastic light scattering. The extent of precursor decomposition and the chemical composition of the gas-phase-nucleated particles were investigated with vibrational Raman spectroscopy. A Website has been established in order to disseminate the numerical and experimental results obtained from this investigation (<http://www.cstl.nist.gov/div836/836.02/cvd/toppage.html>).

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SUPERCONFORMAL DEPOSITION COPPER AND ADVANCED INTERCONNECT MATERIALS

GOALS

This project is developing solutions to metrology issues confronting integrated circuit manufacturers in the area of interconnect metallization. Present efforts include determining the essential process requirements for superconformal fabrication of high aspect ratio, low resistivity copper metallizations, examining the generality of the superconformal filling mechanism for metallizations other than copper and exploring processes utilizing novel barriers and/or seed geometries.

CUSTOMER NEEDS

Increasing information technology requirements have yielded a strong demand for faster logic circuits and higher-density memory chips. The low electrical resistivity of copper and the ability of electrodeposition to “superconformally” fill high aspect ratio features has made electrodeposited copper the interconnect material of choice. However, the move to ever smaller dimensions has led to the rise of new challenges, including fabrication of ever thinner copper seeds that are required for the copper superfill process and increased resistivities of the metallizations due to size effects. To overcome these hurdles the National Institute of Standards and Technology (NIST) has a program focusing on novel metallizations such as silver, new fabrication techniques such as seedless processing, and evaluation of the factors affecting electrical resistivity of sub-100 nm wires as well as enhancing existing copper technology through improved understanding of the fundamentals of the superfill process.

Interconnect metallization issues are discussed in the Interconnect section of the 2003 update of the International Technology Roadmap for Semiconductors.

TECHNICAL STRATEGY

The semiconductor industry has steadily worked to reduce interconnect dimensions, while improving their electrical performance. As a result, metallization has changed from sputtered aluminum (copper) alloys to electrodeposited copper. To meet future industrial needs, we have developed the metrology and fully disclosed electrolytes that permit characterization of the ability of generic electrolytes to fill fine features. We have also de-

veloped electrolytes and metrology for deposition of advanced interconnect materials such as silver (the only metal with a higher conductivity than copper) as well as alternative processing schemes such as chemical vapor deposition.

Some of our newest work eliminates problems related to copper deposition on seeded substrates.

DELIVERABLES: Publications developing robust understanding of Cu superfilling directly on Ru barriers in patterned features. 3Q–4Q 2004

Our recent publication on the use of evaporated ruthenium barriers for superconformal feature filling without use of a copper seed is the first to demonstrate this possibility (see Fig. 1). Features as narrow as 50 nm ensure industrial relevance. Work in progress includes studies with both ruthenium and iridium barriers fabricated by atomic layer deposition.

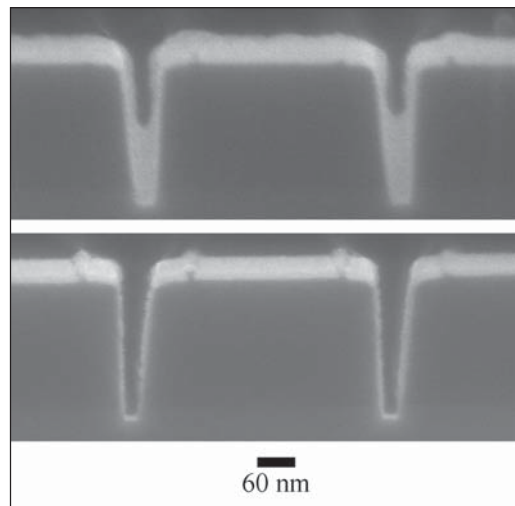


Figure 1. Superconformal electrodeposition of copper without the use of a copper seed layer. The lower image shows ruthenium barriers in trenches that are approximately 50 nm wide. The upper image shows copper bottom-up filling directly on the ruthenium barrier.

DELIVERABLES: Publication on the electrical properties of superfilled sub-100 nm silver metallization. 4Q 2004

Our study of size-dependent resistivity of silver wires with widths between 850 nm and 50 nm and heights between 100 nm and 300 nm (see Fig. 2) demonstrated that the substantial increase of

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resistivity with decreasing wire size necessarily includes a contribution from grain boundary scattering. This work, to appear in the Journal of Applied Physics, also includes derivation of equations that permit the impact of surface scattering on wire resistivity, to be predicted for the entire range of surface scattering conditions between specular and diffuse.

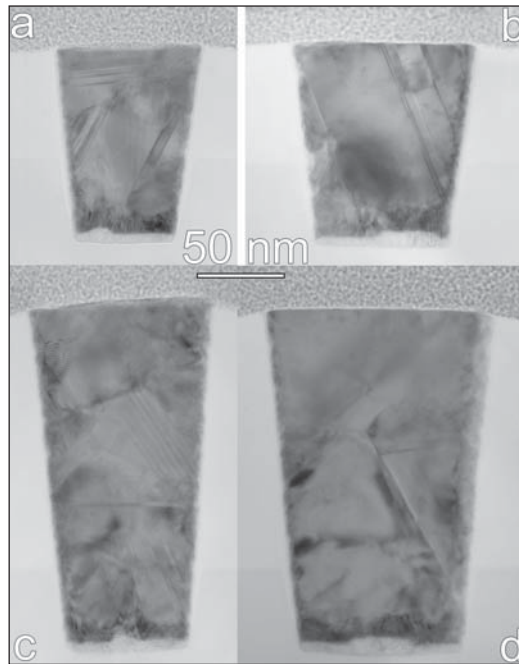


Figure 2. Silver wires viewed in cross-section using a transmission electron microscope. These four wires come from the more than 200 whose electrical resistivities were measured for evaluating size effects in ultrasmall wires. Overburden has been removed from the field above the wires using a hybrid chemical mechanical planarization and oblique argon ion polishing process.

DELIVERABLES: Develop and make available advanced software for modeling superconformal filling of vias and trenches. 3Q-4Q 2004

Previously developed codes that utilize the Curvature Enhanced Accelerator Coverage (CEAC) mechanism to predict superconformal feature filling (see Fig. 3) have been provided to researchers at ST Microelectronics, ATMI, and Intel. However, the code that includes full evaluation of transport in the electrolyte runs on a proprietary computational platform, limiting its usefulness for outside researchers. Code now being developed will operate on a freeware platform, to ensure greater access, and be more efficient and user friendly.

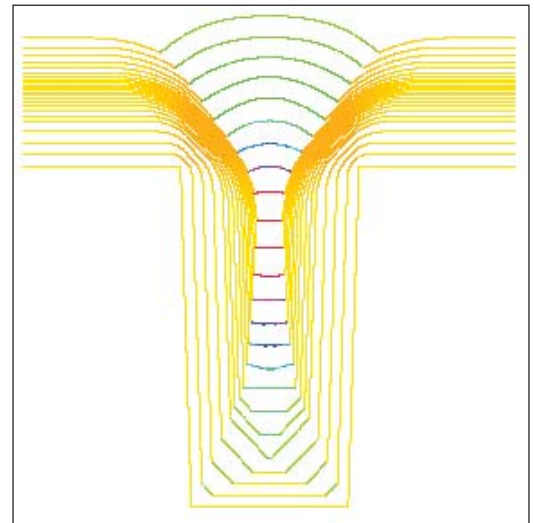


Figure 3. This simulation details the time-dependent filling of a trench (viewed in cross-section). Industrially observed conformal deposition at early times, followed by bottom-to-top superconformal filling and formation of an overfill bump are all predicted. Color coding shows the evolution of the surface coverage of adsorbed catalyst due to changing surface area as quantified by the CEAC mechanism.

A recent publication presents a closed form solution that quantifies superconformal feature filling for a subset of deposition conditions (see Fig. 4). This exact solution permits evaluation of best-case (minimum) sidewall deposition prior to bottom-up feature filling as well as yielding “known” solutions for evaluation of the accuracy of more general feature filling codes.

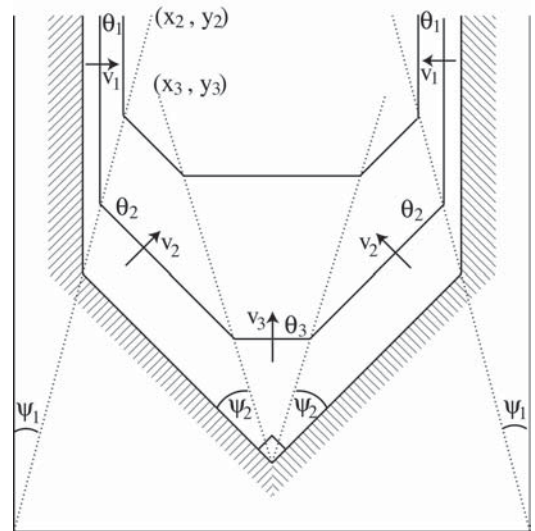


Figure 4. The geometry and parameters that quantify the exact solution of the second stage of superconformal feature filling (the first stage of bottom-up filling).

DELIVERABLES: Write a series of papers detailing the effect of additive composition and catalyst consumption on superfilling behavior of copper and silver. 2Q 2004

One of our newest publications extends our CEAC mechanism to include the impact of catalyst consumption. While such consumption degrades superfilling ability of the electrolyte, as well as leading to undesirable incorporation of impurities in the deposit, it is a very real phenomenon. The experimental techniques used to assess the consumption, as well as the kinetics obtained, provide a clear roadmap for how to examine and control this deleterious effect.

Related measurements have provided a robust assessment of additive aging in industrially relevant electrolytes. A procedure for ensuring process stability was demonstrated; this strategy is now being implemented in the latest generation of commercial plating tools.

DELIVERABLES: Submit high visibility paper to IBM Journal of Research. 2Q 2004

It was IBM that first developed the superconformal copper electrodeposition process. It was therefore a significant opportunity to write a review article on the mechanism behind superconformal feature filling for the IBM Journal of Research. The article, in press, summarizes our most current understanding of the superfill process. Significantly, it also presents a synopsis of the substantial output of the NIST superfill effort to the most relevant industrial audience.

ACCOMPLISHMENTS

- We have fabricated and studied silver metallizations from ~840 nm down to ~50 nm wide to quantify size effects in ultrasmall metallizations
- We have demonstrated the use of ruthenium barriers to obtain superconformal electrodeposition of copper metallizations without the need for a copper seed layer.
- We have quantified the kinetics of catalyst consumption on the electrodeposit surface and the (detrimental) impact of such consumption on the superconformal feature filling process.

COLLABORATIONS

D. Wheeler, R. R. Keller, Y.-W. Cheng, J. E. Bonevich, D. R. Kelley, L. J. Richter, M. L. Walker, W. F. Egelhoff, J. Mallett, G. B. McFadden, S. R. Coriell, NIST.

International SeMaTech, Christian Witt; fabrication of patterned substrates with electrical test structures including sub-100 nm wire widths.

T. Aaltonen and M. Ritala, University of Helsinki; ALD deposition of Ru and Ir seed layers.

Clarkson University, Y. Li and C. Burkhard; chemical mechanical planarization of electrical structures.

RECENT PUBLICATIONS

D. Josell, C. Burkhard, Y. Li, Y.-W. Cheng, R. R. Keller, C. A. Witt, D. Kelley, J.E. Bonevich, B. C. Baker, T. P. Moffat, "Electrical Properties of Superfilled Sub-Micrometer Silver Metallizations", *Journal of Applied Physics*, in press.

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G. B. McFadden, S. R. Coriell, T. P. Moffat, D. Josell, D. Wheeler, W. Schwarzacher, and J. Mallett, "A Mechanism for Brightening: Linear Stability Analysis of the Curvature Enhanced Accelerator Coverage Model", *Journal of the Electrochemical Society* 150(9), C591-C599 (2003).

T. P. Moffat, B. Baker, D. Wheeler and D. Josell, "Accelerator Aging Effects During Copper Electrodeposition", *Electrochemical and Solid-State Letters* 6(4), C59-C62 (2003).



POROUS THIN-FILM METROLOGY FOR LOW-K DIELECTRIC

GOALS

In this project, we are developing measurement methods of morphological characteristics in porous thin films for low- κ dielectric applications. We work closely with industrial collaborators to develop and apply these methods to advanced materials destined for integration in the next generation of integrated circuits. The unique measurement methods we apply include X-ray reflectivity (XR), small angle neutron scattering (SANS), Rutherford backscattering spectroscopy (RBS), and forward recoil elastic spectroscopy (FRES). Our efforts focus on two areas, providing high quality data and measurements of film thickness, coefficient of thermal expansion (CTE), moisture uptake, film connectivity, pore volume, pore size, and matrix density on films under development, and devising new measurement methods to characterize pore size distribution (PSD), pore connectivity, and matrix homogeneity.

CUSTOMER NEEDS

As integrated circuit (IC) feature sizes continue to shrink, new low- κ interlevel dielectric materials are needed to address problems with power consumption, signal propagation delays, and cross talk between interconnects. One avenue to low- κ dielectric materials is the introduction of nanometer scale pores into a solid film to lower its effective dielectric constant as discussed in 2003 ITRS, Interconnect, pages 1 and 2. However, the pore structure of these low- κ dielectric materials strongly affects important material properties other than the dielectric constant such as mechanical strength, moisture uptake, coefficient of thermal expansion, and adhesion to different substrates. The characterization of the pore structure is needed by materials engineers to optimize and to develop future low- κ materials and processes. Currently, there is no clear consensus among IC chip manufacturers for the selection of a class of material or a processing method of nanoporous films. Candidates include silica-based films, organic polymers, inorganic spin-on materials, chemical vapor deposited materials, and several others. With the large number of possible materials and processes, there is a strong need for high quality structural data to understand correlations between processing conditions and the resulting physical properties.

TECHNICAL STRATEGY

■ The small sample volume of 1 μm films and the desire to characterize the film structure on silicon wafers narrows the number of available measurement methods. A unique suite of measurement techniques, Fig. 1, has been developed at NIST using a combination of SANS, XR, RBS, and FRES to determine important structural and physical property information about thin porous films less than 1 μm thick deposited on a 1 mm thick substrate. These measurements are performed directly on films supported on silicon substrates so that processing effects can be investigated.

The elemental composition of the films is determined by RBS for silicon, carbon, and oxygen and FRES for hydrogen. In both techniques, a beam of high-energy ions is directed toward the sample surface. The number of scattered particles is counted as a function of their energy. Fits are performed on the scattered peaks to compute the relative fraction of each element. The atomic composition information is necessary to calculate the relative contrast factors for X-rays and neutrons.

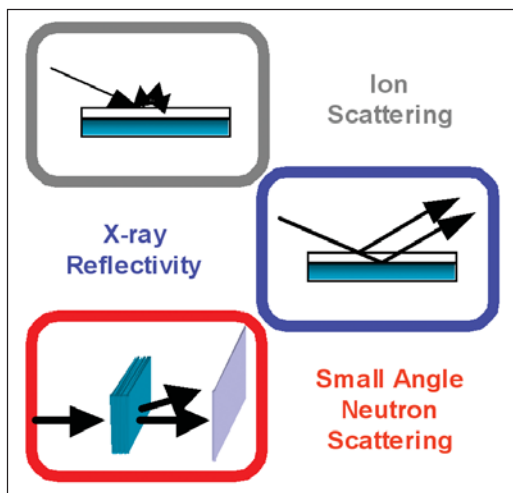


Figure 1. Three thin film measurements that are combined for complete characterization.

The XR experiments are performed at grazing incident angles on a modified to $\theta-2\theta$ X-ray diffractometer at the specular condition. With the modified configuration, reflectivity fringes can be observed from films up to 1.2 μm thick. High-

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Wen-li Wu

“The SANS/SXR measurements have become a key metric in our low- κ dielectric materials characterization and screening process”

Jeffrey Wetzel –
International SEMATECH

“The NIST X-ray reflectivity program is useful, perhaps even critical, to the industry”

Abner Bello –
Applied Materials

resolution XR is a powerful experimental technique to accurately measure the structure of thin films in the direction normal to the film surface. In particular, the film thickness, film quality (roughness and uniformity) and average film density can be determined with a high degree of precision. In addition, changes in the density profile from processing or post-application treatments can be determined. The CTE is determined from measurements of the film thickness at different temperatures.

The SANS measurements are performed at the NIST Center for Neutron Research (NCNR). Up to 10 films are stacked to increase the SANS signal and the samples are placed in vacuum without any obstructions between the sample and the neutron detector. Scattering measurements are initially performed under ambient conditions to determine the structural characteristics of the pore structure. The scattering data are initially analyzed using a simple random two-phase description of the film, the Debye model. This model is appropriate for a class of films having random pores that makes up a majority of the samples measured. Other models are applied where appropriate such as a polydisperse collection of non-overlapping spherical pores. An additional method has been developed in which the Debye model is extended to include more complex distributions of pore sizes that need not be spherical in shape.

DELIVERABLES: Measure and report on up to 20 films for pore volume, pore size, and matrix density associated with ISMT. 3Q 2004

- Further developments in the determination of pore size distributions have focused on the adaptation of conventional probe molecule porosimetry methods to the NIST experimental techniques. For example, XR was done on films that have been measured in vacuum in a conventional way, and then exposed to saturated toluene vapor for several hours, Fig. 2. Capillary action fills the pores of the film. The XR critical edge where adsorption first begins gives an accurate value of the average mass density that is a combination of the walls and the solvent-filled pores. By comparing the results of the sample in air or vacuum with the toluene results, one can calculate the amount of toluene adsorbed, and hence the volume of open pores. Also, XR oscillations at higher angles provide a measurement of the total film thickness before and after exposure to toluene and gives a measure of the solvent resistance and rigidity of the walls.

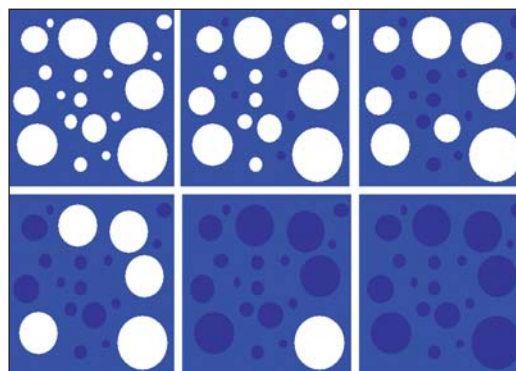


Figure 2. Schematic of the porosimetry measurement, increased solvent vapor pressure fills increased pore sizes.

The toluene infusion results confirm that the open pores of thin films can be filled by toluene supplied by saturated vapor and that XR can accurately measure the amount adsorbed. If the vapor pressure of the toluene or any other condensable solvent can be controlled at a partial pressure, standard porosimetry techniques may be applied to thin films. Data on the amount of solvent adsorption for a series of pressures could be converted to a PSD through the appropriate thermodynamic analysis.

DELIVERABLES: Identify strengths and weaknesses in XR porosimetry using varying methods of generating specific partial pressure environments. 3Q 2003

- The use of deuterated and hydrogenated probe molecules enables the powerful use of contrast match methods with the SANS technique. This technique can be used for characterization of the porous thin films by filling the pores with various mixtures of toluene- h_8 and toluene- d_8 . If the pores are accessible to the solvent and there are homogeneous walls, the wall density can be found. If the wall is heterogeneous, the average wall density could be found with information on the extent of heterogeneity also being possible. If closed pores exist that are inaccessible to solvent, closed pore porosity can be determined.

We have developed a combination of contrast match SANS and XR porosimetry. A match solvent mixture at controlled vapor pressures deposits the contrast match liquid in the pores through capillary action. SANS would provide an additional measure of PSD.

DELIVERABLES: Develop measurement methods for SANS contrast match porosimetry technique. 2Q 2004

■ A practical method of transforming phase size distributions into density correlation functions and PSD's and into SANS or SAXS is being developed. Previous methods of calculating scattering from a PSD assume spherical pores, while important for a certain class of pores, are inappropriate for the majority of pore structures that are randomly interconnected. The Debye methodology assumes a random, interconnected type of pore structure, but is limited to a single distribution type. A new method has been developed to provide information on the size distributions of the pore and matrix phases based on the "chord length distribution" introduced by Tchoubar and Mering.

The transformation of scattered intensity into phase size distributions is possible by this method and has been demonstrated for bimodal distributions. Development of a computational scheme to fit data is underway.

DELIVERABLES: Develop improved data fitting methods for small angle scattering. 4Q 2004

ACCOMPLISHMENTS

■ A project was completed with International SEMATECH (ISMT) in which 20 thin films have been characterized for film thickness, CTE, moisture uptake, film connectivity, pore volume, pore size, and matrix density by XR, SANS, RBS, and FRES. Quarterly reports were delivered on the results and distributed to member companies. Additional measurements were performed on specific samples for further analysis using methods such as additional SANS configurations or X-ray porosimetry.

■ X-ray reflectivity measurements were used to assess depth-dependent phenomena in nanoporous thin films. Measurement of electron density profile can identify gradients in chemical composition or porosity. Measurements on low- κ films exposed to either plasma or electron beam treatments show modified electron density profiles. Modeling of SXR data collected in air indicates that the film is densified near the top (air-film interface). When the film is exposed to saturated toluene vapor, an overall increase in electron density is noted due to the filling of pores with liquid toluene by capillary condensation. However, when the film is exposed to saturated water vapor, the SXR data clearly show that the topmost portion of the film fills with liquid water, whereas the lower portion remains essentially empty, indicating that the top portion is more

hydrophilic. This information is vital to the screening of low- κ materials because solvent uptake during processing can adversely affect device performance.

■ X-ray porosimetry measurements have been implemented utilizing the controlled infusion of toluene into the open pores of a film through mass flow controllers and computer control. All of the connected open pores become filled with liquid toluene through capillary action. The critical edge measured by XR is used to calculate the total mass density and, hence, the total amount of adsorbed solvent and open pore content. This method allows calculation of the total open pore porosity that can be compared to the total combined open and closed pore porosity that is measured by the previous method that uses a combination of XR, SANS, RBS, and FRES. Further, pore size distributions may be extracted using conventional thermodynamic equations from obtained absorption/desorption curves.

■ A contrast match method using saturated solvent vapor was developed to provide an independent SANS measurement of pore volume, pore size, and matrix density as well as pore connectivity, and matrix homogeneity. The films in the SANS cell become saturated by the vapor and the pores become filled. Several solvent ratios are used and the SANS results of the saturated films along with SANS of the films in vacuum are used to calculate the exact match composition. The match composition is used to calculate the mass density of the matrix material and closed pores. This matrix density measurement is independent of the method that uses toluene infusion XR. The contrast match method offers improved accuracy of the final measured parameters. The matrix heterogeneity and the closed pore content can also be determined by the contrast match method. The contrast SANS method was further advanced by performing SANS porosimetry measurements to determine pore size distributions that may be compared with the X-ray porosimetry data.

■ The structural evolution of pore formation in low- κ dielectric thin films (with a deuterated porogen) at various stages in processing was investigated using a combination of specular X-ray reflectivity (SXR) and small angle neutron scattering (SANS). SXR provides information as to the porosity and the density of the wall. SANS data show that the neutron scattering decreases during processing as the deuterated porogen

degrades and pores are formed. The pore size and pore size distribution were estimated by fitting the SANS data to a structural model that describes the scattering intensity from a population of polydisperse spheres that includes hard sphere interactions between the particles and uses a Schultz distribution to describe the polydispersity. The porosity was found to decrease, while the pore size increased, during processing. A practical method of transforming phase size distributions into density correlation functions has been demonstrated. The computations are rapid and can produce density correlation functions, and hence scattered intensities to any necessary degree of accuracy. Phase size distributions other than the exponential ones described by Debye et al. can be transformed into density correlation. The transformation of scattered intensity into model phase size distributions is possible by this method.

COLLABORATIONS

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INTERCONNECT MATERIALS AND RELIABILITY METROLOGY

GOALS

The objectives of this project are: (1) to develop experimental techniques to measure the reliability-related properties of thin interconnect conducting and insulating films, including basic tensile properties, elastic modulus by both static and dynamic means, residual stresses, fatigue, fracture resistance, and electromigration and stress-voiding resistance, in specimens fabricated and sized like materials used in actual commercial devices; and (2) to advance the ability to anticipate and meet thin interconnect reliability challenges by relating thin film reliability to microstructure and by developing understanding of the relationships between various modes of thin film failure, for example, electromigration and mechanical fatigue.

CUSTOMER NEEDS

Thin films are an essential component of all advanced electronic devices. Interconnect structures built up on ULSI microchips consist of 10 thin-film layers now, and will soon reach 12 layers (*International Technology Roadmap for Semiconductors, 2003, Interconnect, Table 81a*). These structures are fabricated using adjacent layers of materials with very different thermal expansion coefficients, exotic materials such as nanoporous low- κ dielectric, and operate at ever higher temperatures. Both experimental measurements and modeling and simulation of material behavior are needed, and these efforts need to be complementary. According to the *Roadmap (2003), Interconnect, p. 34, Cost effective first pass design success requires computer-aided design (CAD) tools that incorporate contextual reliability considerations in the design of new products and technologies. It is essential that advances in failure mechanism understanding and modeling, which result from the use of improved modeling and test methodologies, be used to provide input data for these new CAD tools. With these data and smart reliability CAD tools, the impact on product reliability of design selections can be evaluated. The 2003 NEMI (National Electronics Manufacturing Initiative) Research Priorities document reports a similar need. In a section beginning on page 24, entitled Modeling, Simulation and Design Tools, Emerging Areas for Electronics Packaging, Table 3,*

Projected Development and Research Needs for Simulations in Emerging Areas, includes nanoscale modeling and simulation as an area, experimental tools capable of measuring electrical, thermal, and mechanics phenomena/material properties at smaller scale as a need, and "Issue: how is the property and behavior different from bulk behavior/macro-scale?" as a comment. The message is clear: understanding and modeling of mechanical performance and potential failure modes in these devices require knowledge of the mechanical behavior of the films. This issue of mechanical modeling is likely to increase in significance with the growing integration of interconnect between the chip and the package, with their disparate material sets.

Because the films are formed by physical vapor deposition or spin-on deposition, their microstructures, and hence their mechanical properties, are quite different from those of bulk materials of the same chemical composition. While the general principles of conventional mechanical testing are applicable to thin films, conventional test equipment and techniques are not. Because vapor-deposited films are of the order of 1 μm thick, the failure loads are of the order of gram-forces or less, and the specimens cannot be handled directly. So, techniques specific to films on silicon substrates are needed. Developing test methods must eventually become applicable to test structures that can be included in production or development wafers, so that applicability to 'real' materials can be demonstrated. The intent of our goal of testing specimens similar in size to structures on actual production devices is to maximize the relevance of our results.

Radically different materials and material technologies are being considered for future ULSI devices, as the further development of leading-edge lithography increases in cost and complexity. An example of a radically new material is the carbon nanotube. An example of a new material technology is self-assembly. Effective use of these new materials systems will require significant extension of the reliability metrology and analysis toolset, to understand and address new kinds of reliability issues. The NIST laboratory research programs, which back up the near-term metrology developments described here, are beginning to develop experimental and analytical techniques

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"A microtensile methodology, developed at the National Institute for Standards and Technology, has been adopted and applied in Motorola to evaluate material properties of thin films. This methodology is a significant part of the materials technology development at Motorola."

Betty Yeung, David Read, Yifan Guo, Bill Lytle, and Vijay Sarihan (Motorola AISL, Tempe, AZ), "Microtensile Methodology for Mechanical Characterization of Thin Films," Solid State Technology, June 2002, p. 125.

to address these challenges; NIST management is encouraging these developments through the new strategic focus area in nanotechnology.

TECHNICAL STRATEGY

We are developing a variety of measurement techniques to provide material property data on interconnect materials. In testing and exercising these techniques, we develop data that are valuable in themselves, and we also develop our understanding of the relationship between the observed behavior and the microstructure, as influenced by processing conditions specific to the specimen material at hand.

We study individual thin films and multilayer interconnect structures on silicon substrates, both obtained from industry and fabricated by researchers within NIST and elsewhere. Specimens of CMOS structures have been obtained through the MOSIS service run by UCLA (Fig. 1). Occasionally, wafers or fabricated specimen geometries are received directly from our counterparts in industry. Some of our techniques require the removal of the silicon substrate beneath the test structure itself, to a depth of up to 50 μm . We have developed dry etching systems that use xenon difluoride to carry out these processes.

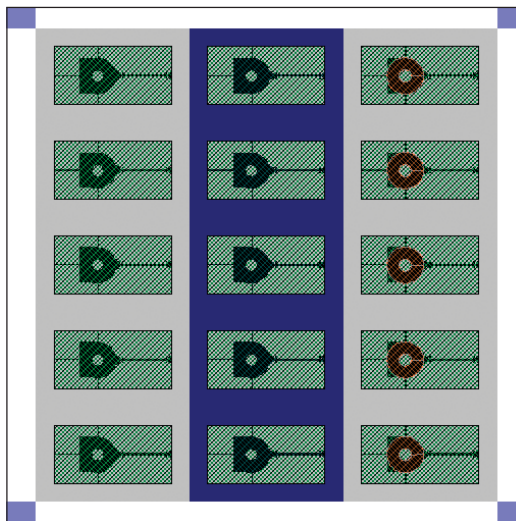


Figure 1. Test chip produced in the 1.2 μm AMI CMOS process available through the MOSIS service.

Measurement capabilities operating within this project include microtensile testing, d.c. and a.c. electromigration measurements, and resonant structure measurements. We have developed the silicon-frame tensile specimen and the piezo-actuated tensile tester, which operate successfully

for specimens 100 μm wide and larger. Because problems were encountered with specimens narrower than 100 μm , a new technique, called the force-probe tensile test technique, has been developed. The apparatus includes a tensile loading system operable within the scanning electron microscope (SEM). This system has now been used on specimens as small as 2 μm wide. It is anticipated that the magnification of the SEM will allow testing even narrower specimens.

We have begun an effort on electrodeposited copper, including specimens from industrial colleagues and produced in-house, to characterize the variability of the mechanical behavior of electrodeposited copper with deposition conditions, film thickness, annealing, and other relevant variables.

Our measurements involving alternating current stressing of chip-level interconnects are used to explore the relationships between electrical and mechanical reliability. High current density a.c. signals are run at low frequencies through Al- and Cu-based electromigration structures in either passivated or unpassivated states. Joule self-heating results in a cyclic strain due to thermal expansion mismatch between the metal lines and their substrates. The associated deformation then leads to severe topographic distortions in the lines, and can eventually cause open circuit failure. We investigate the effects of current density, frequency, crystallographic orientation, and encapsulant material.

We have work in progress, with the NIST Metallurgy Division, to address reliability of advanced interconnect materials with linewidth less than 100 nm. In addition to the challenges associated with electrodeposition into extremely narrow trenches, we expect significant influences of the interconnect sidewalls on electrical resistivity and possibly on electromigration resistance.

We are also developing non-contact optical methods to measure mechanical properties of thin films and interconnects using MEMS test structures that are compatible with the CMOS process. Such non-contact methods may be useful in monitoring the variations of mechanical properties in the production environment. A method has already been developed to measure the residual strain in the passivation and interconnect films using fixed-fixed beams. We are currently developing resonant measurements for cantilever beams to characterize the elastic modulus of each layer (Fig. 2).

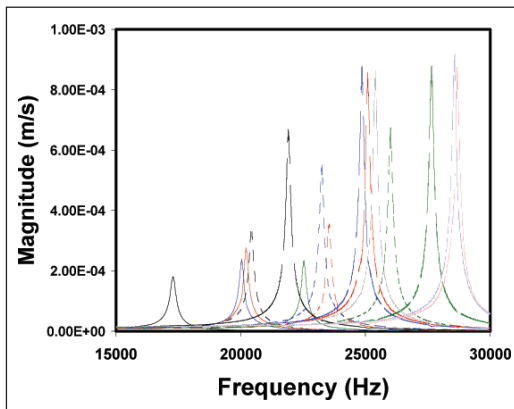


Figure 2. Resonant frequency response of micromachined CMOS cantilever test structures.

The method is based on the fact that the resonant frequency of the cantilevers is related to their elastic modulus, density, and the geometry. They can be fabricated with different combinations of layers and then comparisons of the resonant frequency can be used to extract the modulus of the individual layer. The cantilever test structures can be fabricated simultaneously with the fixed-fixed beams used to measure residual strain and strain gradient. With the residual strains, from the fixed-fixed beam method, and the elastic constant, from the resonant method, the residual stress and its gradient can be calculated.

DELIVERABLES: Our results are being disseminated in conference presentations and peer-reviewed articles in archival journals, as well as in presentations and written reports to the organizations that have supplied specimens.

Design and fabricate a test chip with improved cantilever test structures; develop method to determine elastic modulus from resonant frequency measurements.

Conduct electrical tests on electrodeposited copper lines of width 100 nm or less. 4Q 2003.

ACCOMPLISHMENTS

Progress in recent years on measurements of the mechanical behavior of thin films has put us in the position of starting to be able to make various kinds of critical comparisons among our results: results for the same materials in different laboratories; results for similar materials from different sources; results for the same property by different measurement methods; and experimental results versus numerical simulations. These comparisons are necessary to reach our goals of providing accurate and believable measurement

techniques and an understanding of the results. This year we obtained nanoindentation results on a previously tested aluminum film and on thick copper films from an outside collaborator. From the nanoindentation load-displacement data, we deduce Young's modulus and yield strength of the material in a very small volume deformed by the nanoindenter tip. The results obtained from nanoindentation scatter widely in both Young's modulus and yield strength for electron beam-evaporated aluminum; both values are consistently higher than those obtained from microtensile tests (see Fig. 3). This problem of scatter between nanoindentation and microtensile results is typical in such comparisons. Nanoindentation results for polyimide were also higher than microtensile results, but with less scatter. Work is continuing with other materials and understanding the causes of the scattering. The measurements on the thick copper films, analyzed using plastic-zone-sized deduced from AFM images, gave a good correlation with the micro-tensile results shown below.

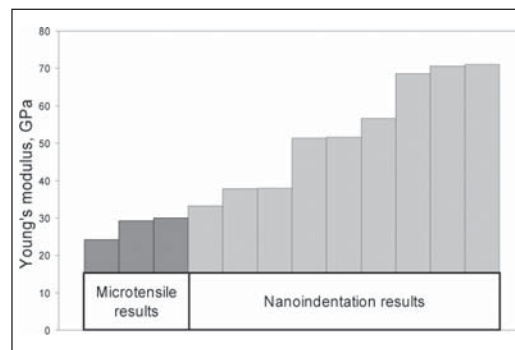


Figure 3. Comparison of Young's modulus obtained from nanoindentation and microtensile tests.

DELIVERABLE: The collaborative study on copper has been presented at a technical conference and submitted for publication in a technical conference proceeding.

A key experimental tool for understanding the sources of mechanical weakness is fractography of broken specimens. A new scanning electron microscope, with a field-emission source and an in-lens detector, is allowing us to obtain very clear images of the fractures surfaces of microtensile specimens. An example is shown in Fig. 4. This aluminum CMOS contact metal had low elongation, and variable tensile strength with some very low values.

Recently, we have been working to demonstrate the applicability of these techniques to materials

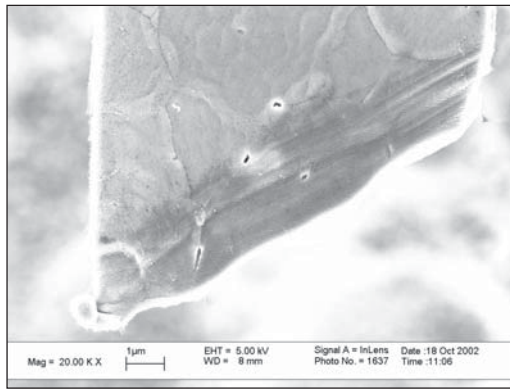


Figure 4. Fracture surface of tensile specimen of CMOS contact metal obtained through the MOSIS service.

recently introduced in the microelectronics industry, specifically copper, in the form of both sputtered thin films and thick electrodeposits. A microtensile specimen of electro deposited copper is shown in Fig. 5. We typically find that the strength values are far above the handbook values for pure annealed bulk copper, and the elongations are much lower than the handbook values. Increasing the film thickness from, for example, 1 to 10 μm , increases the ductility from around 1 % or less to 5 % or more. Annealing also changes the tensile properties markedly. We have extended our microtensile test capability to temperatures up to 150 $^{\circ}\text{C}$. Figure 6 shows recent results for contact Al-Si, from MOSIS, and electrodeposited copper, made at NIST.

The demonstrated applicability of the force-probe technique to a variety of specimen materials and temperatures leads us to think that this technique and its complementary specimen geometry may become a standard method for microtensile testing.

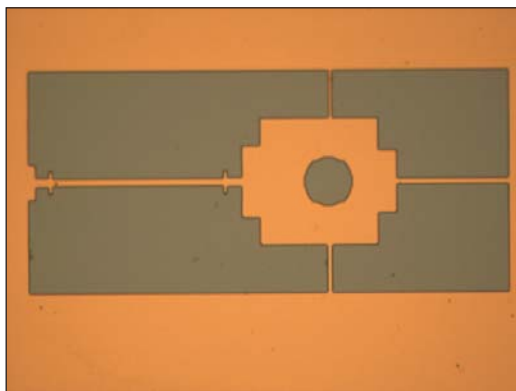


Figure 5. Microtensile specimen of electrodeposited copper produced at NIST. The slender strip on the left is the test section; the tab with the hold is used for loading. The grip section is 10 μm wide by about 200 μm long.

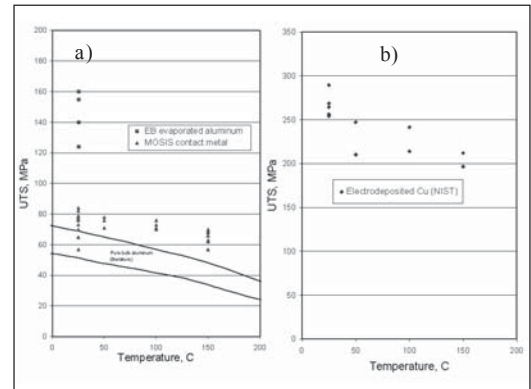


Figure 6. Tensile strength plotted against temperature for microtensile specimens of aluminum contact metal obtained through MOSIS, and electrodeposited copper made at NIST.

Figure 7a shows a high-resolution SEM image of the surface of an electrodeposited (ED) copper specimen made at NIST. The distinctive morphology, an array of joined spheres, may not be representative of normal production material. But it may represent, in an exaggerated form, microstructural features commonly present in ED copper. Its crystallographic symmetry, lattice parameter, and mechanical properties all appeared normal when measured by standard techniques. Figure 7b shows an atomistic mode that simulates the mechanical behavior of this morphology, though at a smaller scale. The atoms shown as solid black are in regions of low face-centered-cubic symmetry, while the atoms shown in color are surrounded by near-perfect fcc structure. This simulation presents a possible explanation for our measured values of the elastic constant of ED copper, which are lower than the bulk value.

Our a.c. tests continue to reveal damage phenomena drastically different from that observed in conventional d.c. electromigration tests. Figure 8 shows the large difference in lifetime seen under the AC and DC test conditions. We have pursued crystallographic mapping experiments within a field emission SEM, due to the generous amount of information that can be obtained with such an approach. What has become apparent is the tremendous variation in behavior from grain to grain. We have observed significant growth of selected grains in a polycrystalline interconnect, which subsequently become more susceptible to surface offset formation with further cycling (Fig. 9). Accompanying such grain growth is a re-orienting of some grains, into a more accommodating orientation for slip activity. In other words, grain re-orienting seems to provide a larger resolved

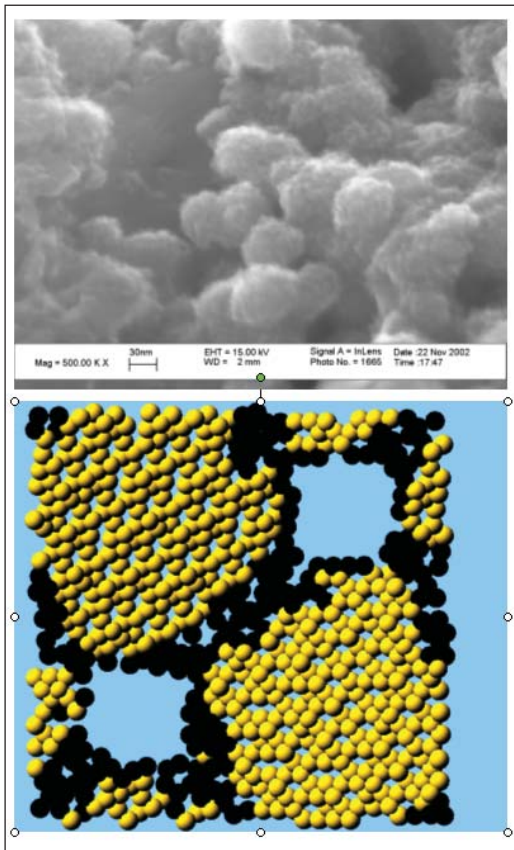


Figure 7. a) High-resolution SEM image of electrodeposited copper specimen made at NIST. The original magnification was 500,000. The copper “balls” are 30–50 nm in diameter. b) Atomistic model simulating the morphology and mechanical behavior of this copper electrodeposit. The atoms shown as copper-colored have near-normal face-centered-cubic crystal environments; the atoms shown as black are also copper atoms, but their local crystallographic symmetry is lower. Through the use of periodic boundary conditions, this 23000-atom model simulates a specimen of indefinite size.

shear stress on a particular grain. Many factors interact to control the processes leading to catastrophic failure by open circuit, at a site where the interconnect cross section has decreased very significantly due to deformation. We are attempting to construct a model describing the roles of these factors, including strength of individual grains (grain size), ease of slip within individual grains (grain orientation), and prevalence of dislocation sources (grain boundary structures, surrounding grain constraints). The end goal is to offer a scheme for predicting where an open circuit should be expected, given the initial grain structure of the interconnect.

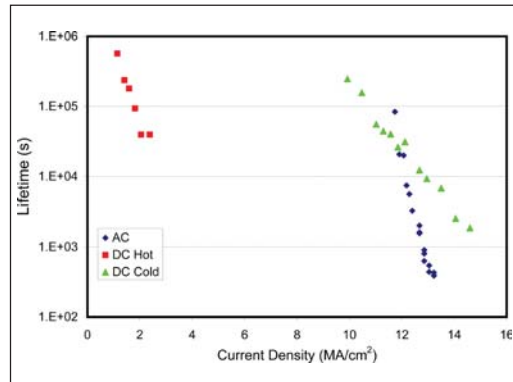


Figure 8. Time to open circuit under various electrical testing conditions. “AC” and “DC Cold” data obtained with specimen nominally at room temperature. “DC Hot” tested at nominal specimen temperature of 227 °C. “DC Hot” data from U. E. Möckl, M. Bauer, O. Kraft, J. E. Sanchez, Jr., and E. Artz, *MRS Symp. Proc. Vol. 338, 373 (1994)*.

Because it is sometimes impossible to get films of individual materials with the interconnect stack in a chip that goes through a normal manufacturing process, we are studying measurement methods that use composite laminate specimens that include several materials, such as metal and dielectric. The elastic modulus of the individual films in the laminate is to be determined by differences between the resonant frequencies of beams with different combinations of metal, dielectric, and polysilicon. A model has been developed for a composite cantilever beam. Preliminary measurements indicate that this technique can provide accurate values of the different layers in the interconnect structure, as well as insight into the behavior of the structure as a whole.

The Matlab optimization procedure to extract the Young’s modulus values of the various interconnect and oxide layers has been automated. This procedure includes the calculation of the thicknesses of the various layers given inputs such as capacitances, sheet resistances, and step height measurements.

Also, a sensitivity analysis has been semi-automated where each of the Matlab inputs gets varied $\pm 10\%$ or ± 3 standard deviations. The resulting Young’s modulus values are then recorded. The important conclusion is that even if the various inputs are off by $\pm 10\%$, reasonable Young’s modulus values can still be obtained. *The optimization technique is not as sensitive to layer thicknesses as originally believed.* The technique is proving to be solid and reliable.

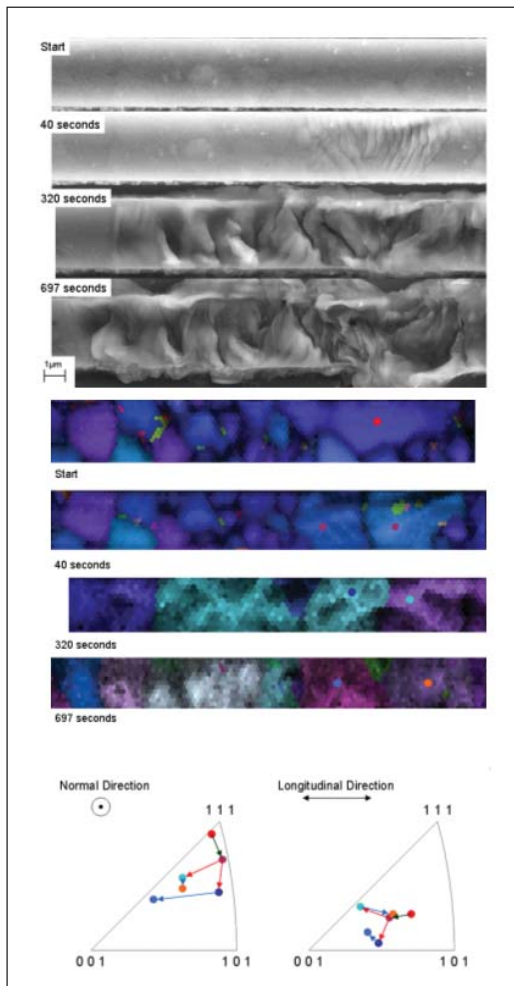


Figure 9. AC testing sequence in Al-1Si, showing development of surface offsets, grain size and shape changes, and grain orientation changes, at 0, 40, 320, and 697 seconds of AC cycling at about 12 MA/cm². Upper images: surface topography by SEM; lower images: same locations, color indicates grain orientation; drawing: changes in crystallographic orientation of grains as indicated.

CMOS cantilevers tend to exhibit extreme curling, which can affect their resonant frequencies. The latest test chip design (see Fig. 10) includes shorter cantilevers and fixed-fixed beams, whose bending/curling out-of-plane will be less severe and hence the resonant frequencies obtained from these structures will be more believable. With this test chip, we will be able to determine if MEMS is “linear.”

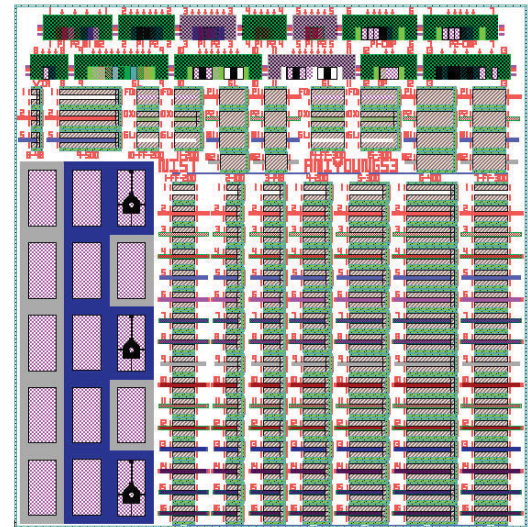


Figure 10. Test chip design fabricated on the AMI 1.5 μm CMOS process.

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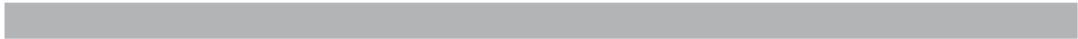
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WIRE BONDING TO COPPER/LOW- κ SEMICONDUCTOR DEVICES

GOALS

The overall objective is to determine optimal conditions for achieving high yield reliable wire bonds to advanced technology semiconductor chips with copper/low- κ interconnect structures.

CUSTOMER NEEDS

The introduction of copper metalization interconnect structures in advanced integrated circuit manufacture has forced changes in wire bonding. The process should be invisible to the current wire bonding machines. However, the copper bond pads oxidize, requiring a protective/bondable coating. When low-modulus low-dielectric materials lie below the pad, a support structure is necessary to prevent damage to the interconnection/dielectric layers. There are many approaches to solving these problems; the NIST program is attempting to optimize and develop new solutions where necessary.

TECHNICAL STRATEGY

1. One approach to protecting the copper is to coat the bond pads with a bondable gold layer. For this approach, the first objective is to determine the diffusion coefficients of copper through gold, because copper can diffuse to the surface and will oxidize, preventing a good bond. Literature values on various gold platings are contradicting and have been performed on non-damascene structures. A more classical approach, but also a more difficult process, using SIMS has been proposed. We have developed a two step (immersion + auto-catalytic gold) deposition process over the copper-low- κ chips. This will be pursued at NIST. Even without the actual diffusion coefficients, a pragmatic approach is being carried out by heating gold coated samples and doing extensive wire bonding and evaluating with ball shear tests. A subset of this work will be to determine the minimum thickness of gold necessary to prevent copper diffusion/oxidation in normal bonding/processing temperatures. At the same time several inorganic coatings for protection are being evaluated. Sandia has applied thin deposited SiO₂ coatings on the copper wafers and they were evaluated. Results so far indicate that all of our coatings are nonuniform, but bonding did occur on the better pads. This

evaluation is continuing, possibly by depositing a thick, uniform coating and then etching thinner.

2. Another objective is to measure the nano-hardness and modulus of the damascene copper in order to optimize bonding, [hardness should be minimized (80 Knoop to 100 Knoop)].

Problems have occurred when sawing the bare copper chips in which the saw particles stick to the bare copper. Several approaches to curing this problem have been pursued and are adopted. Copper damascene process samples have been supplied by IBM and International SEMATECH for this effort.

DELIVERABLES: Problems with the two-step gold deposition will be solved. Some pad lifting during gold deposition will be studied and an understanding obtained. The desired thickness of gold deposition will be determined, and hardness and modulus studies completed. A nickel strike coating also was developed. Diffusion studies of copper into gold will be made.

ACCOMPLISHMENTS

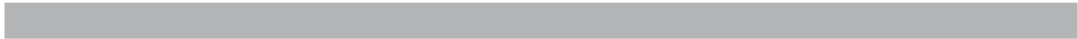
- Knoop hardness measurements have been accomplished with a series of annealing experiments made with copper chips, and pragmatically verified by actual bonding experiments. Values of measured nanohardness have been dependant on the annealing gas (argon is best) and have been as low as 60 GPa (about 120 unannealed) and the modulus as low as 20 GPa.

- One paper published, entitled "Wire Bonding To Advanced Copper-Low- κ Integrated Circuits, the Metal/Dielectric Stacks, and Materials Considerations," by George G. Harman and Christian E. Johnson, Proc. 2001 IMAPS Symposium, Oct 9-11, 2001, Baltimore, MD, pp. 484-491. This paper won an award as an outstanding paper in the Symposium. An updated version of this was published in the IEEE Transactions on Components and Packaging Technologies, V-25, Number 4, Dec. 2002, pp. 677-683.

- The two step non-contact gold deposition process used on some of the original International SEMATECH (ISMT) wafer copper were etched in our processing, whereas other copper deposition methods were satisfactory and bonded well. Currently, wafers from another source with thicker copper are being acquired. Copper diffusion through the gold is being measured.

Technical Contacts:

G. G. Harman
C. Johnson



SOLDERS AND SOLDERABILITY MEASUREMENTS FOR MICROELECTRONICS

GOALS

Solders and solderability are increasingly tenuous links in the assembly of microelectronics as a consequence of ever shrinking chip and package dimensions, the broadening use of flip-chip technology, and the movement toward environmentally friendly lead-free (Pb-free) solders. To support needs in this area, the goal of this project is to provide data and materials measurements of critical importance to solder interconnect technology for microelectronics assembly.

CUSTOMER NEEDS

The U.S. microelectronics industry has clearly articulated measurement needs for solderability and assembly, especially for Pb-free solders. For example, the urgency for materials data for Pb-free solders has been specified in the 2002 NEMI, 2003 IPC, and 2003 ITRS Roadmaps. Pressure from the European Union and the Japanese consumer product market to produce lead-free microelectronics continues to increase. These industrial needs are addressed under this NIST project.

Additional needs have been identified through participation in the National Electronics Manufacturing Initiative (NEMI) working group on Pb-free solder alloys. It was learned that significant industrial problems had arisen due to contamination of Pb-free solders by the Pb contained in the protective solder coatings that are used on copper (Cu) leads. The protective layer deposited on Cu is usually referred to as a "pretinned" coating and is required to maintain solderability of the component during storage prior to assembly. Pb-free coatings of nearly pure tin (Sn) tend to grow "whiskers," however, which can cause shorts across leads. Thus the development of Pb-free alloy platings to replace Pb-containing protective layers is considered important, and tests which ascertain the tendency to form whiskers are much needed. NIST co-chairs the NEMI Sn Whisker Modeling Group and is an active participant in the NEMI Accelerated Sn Whisker Test Group.

TECHNICAL STRATEGY

We are providing the microelectronics industry with measurement tools and data to address solder interconnect problems. For example, a ther-

modynamic database has been developed and publicly distributed for modeling the processing behavior of lead-free solder systems. These databases for phase diagrams and thermodynamics critical to solder development and for mechanical properties of solder will continue to be expanded and distributed via the web. We also provide guidance for adoption of these solders into assembly processes through work with industrial standards organizations. In addition, a much-needed guide to interpretation of thermal analysis data will be produced.

It is well known that the use of pure Sn protective deposits has serious problems. Sn whiskers (filamentary whiskers typically 1 μm diameter and several mm long) can grow from the plating and cause electrical shorts and failure. Historically Pb was added to Sn plate to prevent whisker growth as well as to lower cost. In the current research program, it was decided to focus on Pb-free Sn-rich deposits with alloying additions that might retard whisker formation. The Sn-Cu system was selected for compatibility reasons, since Sn-Cu-Ag is likely to be the Pb-free solder of choice for industrial application. The substitution of a different solute for Pb in the Sn-rich deposit was

Technical Contacts:

Carol Handwerker
Maureen Williams
Christian Johnson
Kil-Won Moon

"I consider your [NIST Metallurgy Division] group a key asset to industry in making these decisions on the soundest possible scientific basis. There is no comparable body of expertise anywhere in the world that matches that found in your group."

*Dr. George T. Galyon (IBM) -
Chairman, NEMI Tin Whisker
Modeling Committee*

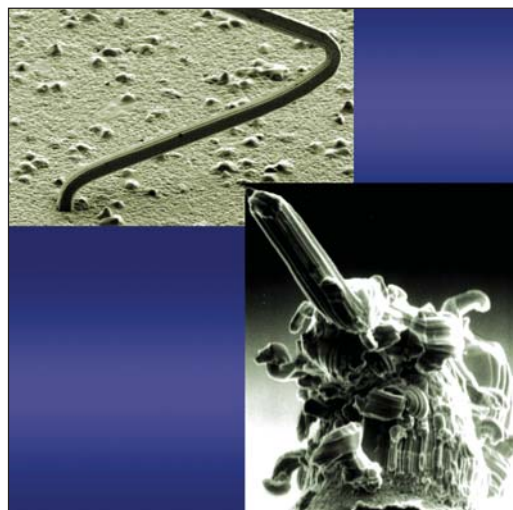


Figure 1. Two characteristic tin whisker geometries. In each case, the filaments are about 1 micrometer in diameter, and can grow over a period of years to several mm in length, causing electrical arcing or shorts. Such whiskers are a critical concern for high reliability applications using pre-tinned lead-free surface finishes.

proposed to also retard whisker growth. A detailed microstructural comparison of deposits with high and low whiskering tendency is being conducted. Sn grain size, shape, preferred orientation and residual stress will be measured and correlated with a goal of determining the dominant mechanism(s) for whisker growth.

DELIVERABLES: Analyzing stresses in Sn, SnCu and SnPb electrodeposited films on cantilever beams. 3Q 2004

DELIVERABLES: SEM inspections for NEMI Tin Whisker Accelerated Test Group to document ambient whisker growth on 14 different plating types and provide a report. 3Q 2004

DELIVERABLES: Expand pages for phase diagram Metallurgy Division Webbook with emphasis on solder alloys. Add pages for constituent binary and ternary systems containing Sb. 4Q 2004

DELIVERABLES: Develop an easy-to-use interface for phase equilibria software for the calculation of liquids temperature, lever rule equilibrium and Scheil solidification. Make this simple phase equilibria software available for interactive use; make more complex programs available for downloads. 4Q 2004

DELIVERABLES: Prepare draft of Best Practice Guide for Differential Thermal Analysis. 4Q 2004

DELIVERABLES: NIST will co-sponsor a Sn Whisker Workshop at NEMI headquarters in Herndon, VA. 4Q 2004

ACCOMPLISHMENTS

- NIST has taken a major role working with industry through a NEMI Task Force to identify and move Pb-free solders into practice. NIST co-chairs the NEMI alloy selection group that selected standard alloy compositions for U.S. microelectronics assembly.
- The NIST-developed thermodynamic database allows the calculation of phase transformations in solder alloys containing Ag, Cu, Bi, In, Sb and Sn and provides essential information for Pb-free alloy development. New data for Ag, Cu, and Sn with Ni expands the applicability of the database to the characterization of interactions between Pb-free solders and Ni-based surface finishes.
- NIST-developed software for the calculation of melting temperatures, and lever rule equilibrium and Scheil solidification, as well as the thermodynamic database, are now disseminated on the NIST website.

NIST is a co-chair in the NEMI Sn Whisker Modeling Group (working closely with members ChipPAC, Cookson, Delphi Delco, FCI Framatome, Hewlett Packard, IBM, Intel, Intersil, IPC, Motorola, Rohm & Haas Electronic Materials, Soldering Tech, Solectron, Sun Microsystems, Texas Instruments, and Tyco Electronics) and is an active participant in the NEMI Accelerated Sn Whisker Test Group.

Previous NIST work has characterized grain size and surface topography of electrodeposited films on a variety of substrates as a function of Cu and Pb additions to the Sn electrolyte, pointing out the role of even trace levels of copper in whisker propensity. Now focusing on the relationship of microstructure and stress, our current attention is on residual stress measurements of electrodeposited Sn, SnCu, and SnPb alloys using the cantilever beam technique. Preliminary work shows that the initial stress in all of the deposits is always compressive. The Sn-Cu deposits are the most compressive and Sn-Pb deposits are the least compressive.

In collaboration with NEMI, NIST will also co-sponsor a two-day workshop on Tin Whisker Formation in Microelectronics for industrial and academic participants at NEMI headquarters in Herndon, Virginia on October 19 and 20, 2004.

COLLABORATIONS

National Electronics Manufacturing Initiative; Lead-free solders and reliability.

RECENT PUBLICATIONS

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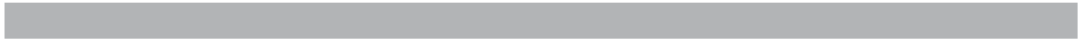
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THERMAL MEASUREMENTS AND PACKAGING RELIABILITY

GOALS

The goals of this project are the following:

a) Provide the microelectronics packaging industry with information, guidance, and tools through technology transfer to characterize the behavior of features and interfaces in packaging that are thermally stressed. Information and guidance are provided directly to individual companies and to consortia through collaborations whereby we are provided with specimens that present a reliability concern to the manufacturer or end-user. The results of the tests are reported to the provider, and are typically reported in the general literature or at technical meetings. This system contributes toward achieving our third and primary goal—providing the industry with the tools to characterize these thermomechanical behaviors. Review and evaluation of the techniques by our industrial collaborators allow us to refine the techniques to make them optimally beneficial to industry, and to demonstrate to the industry at large the capabilities of the techniques on actual packages in development, which is essential for technology transfer.

b) Develop and evaluate methods for measuring temperatures at and within the chip-level for the purposes of determining *in situ* material thermal properties (e.g., thermal properties of interlayer dielectrics), device performance (e.g., SOI devices), and for evaluating the thermal performance of new architectures and technologies (e.g., 3-D integration and innovative cooling methods for high performance logic).

CUSTOMER NEEDS

The trend in electronics is toward components of higher density and smaller size using less expensive materials. Materials used in packaging are many and display a variety of thermal responses that are not always compatible. This makes interfaces particularly vulnerable to thermomechanical fatigue failures. The program seeks to offer support and verification of models conducted or sponsored by the microelectronics industry.

Thermal measurements on small, <10 μm structures are needed due to the high density of current and future interconnect and packaging designs. Heat transfer information at interfaces,

such as those seen at solder/intermetallic interfaces, is needed for modeling of future package designs.

Temperature measurements for microelectronic devices are more important today than they ever have been. It always has been true that extreme temperature places limits on the operating range of nearly all devices, but today, increasing power dissipation and power densities threaten to create temperatures that block continued progress according to “Moore’s Law.” Clearly, new and innovative methods for cooling chips and packages must be found along with new materials and circuit designs, and architectures for decreasing the power dissipation and operating temperature. Equally as clear, we must have accurate and well-understood methods for measuring the temperature of devices to aid in the development of these new techniques and materials.

“Packaging cost is a second area that could be an obstacle to realizing the potential of advances in silicon technology. ...the average packaging share of total product cost will double over the next 15 years and, more significantly, the ultimate result will be greatly reduced gross profit margins, limiting investments in R&D and factory capacity.” 2000 NEMI Roadmap.

The maximum junction temperatures for chip operation are shown in tables 93 a and b of the ITRS Assembly and Packaging section. Issues concerning the poor thermal conductivity of low- κ dielectrics is discussed on page 34 of the Reliability section.

TECHNICAL STRATEGY

1. Our established program in infrared (IR) (thermal) microscopy and our developing techniques in scanning thermal microscopy, utilizing the AFM (atomic force microscope), have much to offer the microelectronics industry. We have been approached by industry with requests for aid as simple as “How high are the temperatures in this MCM (multichip module) during service” to as challenging as “What is the interfacial thermal resistance of an alloy/intermetallic interface.” The first was answered using the IR microscope; the second has yet to be answered.

Technical Contacts:

A. J. Slifka
D. L. Blackburn
A. R. Hefner

“I am writing to let you know that NIST has been of great assistance to Cenymex Corporation, one of our portfolio companies. This portfolio company has developed a novel material. Dr. Andrew Slifka at NIST was able to provide the company with thermal measurements that are critically important to Cenymex as it approaches potential customers. It is great to have NIST in the community as a resource to companies like Cenymex.”

*Tim Connor
Sequel Venture Partners*

“In the area of the Grand Challenges for Assembly and Packaging, it is noted that thermal dissipation and thermomechanical stress must be handled comprehensively.”

“Advanced modeling tools covering the related electrical, thermal, and mechanical aspects are needed to support the development and optimization of those technologies.”

2003 International Technology Roadmap for Semiconductors

We have just completed our third year of applying thermal conductivity measurements using the IR microscope to the problem of packaging reliability, and have engendered great interest from the Advanced Embedded Passive Technology (AEPT) Consortium. As thermal conductivity measurements are one of the most sensitive indicators of metal purity, likewise they are one of the most sensitive indicators of interfacial integrity. A minute increase in interfacial thermal conductivity is the first indication of the microcracks and fissures that ultimately may result in failure.

2. As the size of packages gets smaller, heat removal becomes a more significant problem. The SPM is being used to develop a technique to measure thermal conductivity of thin films for application to metal interconnect lines. The technique also will be able to measure interfacial thermal resistance between coatings and substrates. The theoretical work on this development is being done in collaboration with Dr. Kevin Cole of the University of Nebraska.

DELIVERABLES: Report via the literature, on measurements of a model film, such as gold or different substrates. 3Q 2004

3. Diamond-like carbon has potential applications in heat removal from electronic devices and in wear applications. Thermal properties and thermomechanical fatigue behavior need to be evaluated on novel materials for design and modeling use.

DELIVERABLES: Measure thermal conductivity of industrial films produced under various conditions. 2Q 2004

4. Interfacial thermal resistance measurement of the interface between solders and intermetallics supplies a piece to the puzzle of thermal dissipation from high-density packages. The small size of current and future solder bump processes requires higher spatial resolution thermal measurement methodologies.

DELIVERABLES: Measure interfacial thermal resistance of interfaces in in-house and industrial solder alloys. 4Q 2004

5. The reasons for desiring to know the operating temperature of a semiconductor device can be divided into the following four broad categories:

- Predict reliability or operating life of device
- Measure material/device thermal properties *in-situ*;

- Confirm or determine the operating limits or thermal performance of a device; and
- Validate thermal models for chip and device performance.

A broad range of temperature measurement techniques will be investigated. These will include:

- Electrical techniques that use temperature sensitive device and material parameters (such as junction voltages, threshold voltages, and resistivity) as thermometers, optical techniques such as infrared thermal emission, micro-Raman spectroscopy, and reflectance and micro-probes based upon AFM systems.

DELIVERABLES: Develop metrology to characterize thermal performance of high voltage SiC devices and packages. 4Q 2004

Develop high power IGBT thermal models for 6-pack IGBT, and validate thermal performance. 4Q 2004

Extract IGBT electrical model parameters for 6-pack IGBT. 4Q 2004

Perform electro-thermal simulation of 6-pack IGBT in full three-phase inverter application. 4Q 2004

Publish paper on high-speed power module thermal characterization system. 4Q 2004

Develop high-power IGBT thermal models for Integrated Power Electronics Module (IPEM) MOSFET, and validate thermal performance. Enhance measurement system as needed. 4Q 2004

Complete review paper on methods of measuring the temperature of microelectronic chips. 4Q 2004

ACCOMPLISHMENTS

- Completed analysis of measurements on industrial specimens from AEPT using thermal SPM, laser-heated IR microscopy, and Joule-heated IR microscopy. Reported results at GOMACTech 2004 Conference.

- Thermal measurements have continued on three similar embedded resistor specimens. One specimen each is being measured using laser-heated IR microscopy, Joule-heated IR microscopy, and thermal SPM. The results were analyzed and the techniques compared. All three specimens have been thermally cycled 18 times, and data analysis shows consistency between the techniques. Figure 1 shows relative thermal resistance data as a function of thermal cycling from Joule-heated measurements.

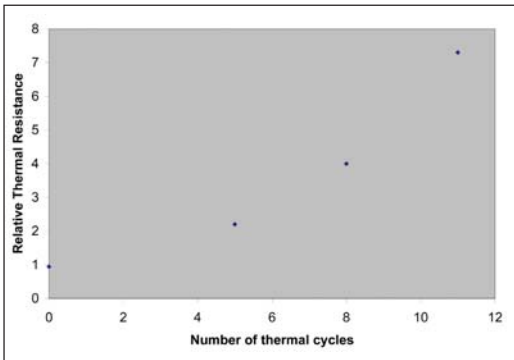


Figure 1. Joule-heated IR microscopy measurements showing relative thermal resistance as a function of thermal cycling.

■ Development of a technique for measuring the thermal conductivity of thin films using the SPM has begun. Most films used in electronics and electronic packaging are so thin that a measurement using even the thermal SPM would be primarily a measurement of the substrate material. With collaboration from Dr. Kevin Cole of the University of Nebraska, work has begun on a theoretical treatment of the data to allow measurement of thin films and the interfacial thermal resistance between the film and substrate. One application for this technique is measurement of thermal properties of interconnect lines. Measurements have begun using a model system, consisting of gold films of various thickness evaporated onto glass substrates. Figure 2 shows thermal measurement data on films of differing thickness.

■ We have been approached by Cenymmer Corporation to make thermal and other measurements

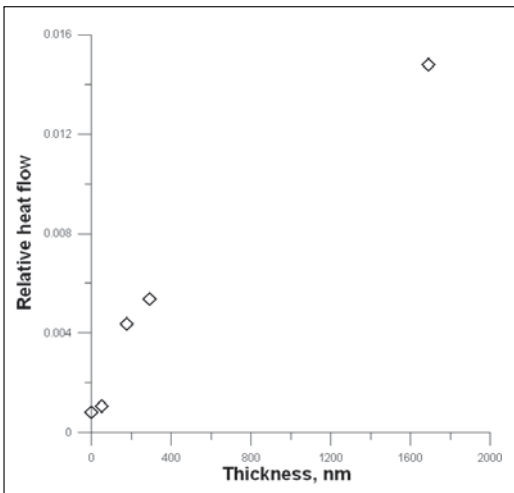


Figure 2. Thermal measurement data on thin gold films on glass substrates.

on a diamond-like carbon coating that they manufacture. Since these coatings are typically around a micron thick, the thermal SPM is a good tool for this measurement. Cenymmer also is interested in interface materials to allow adhesion of diamond-like carbon coatings to various substrates. This work fits well with our thin-film research, providing specimens with different, controlled interfaces to help solve the problem of analyzing thermal data on thin films and even thinner adhesion layers. Figure 3 shows a measurement result from one of their coatings.

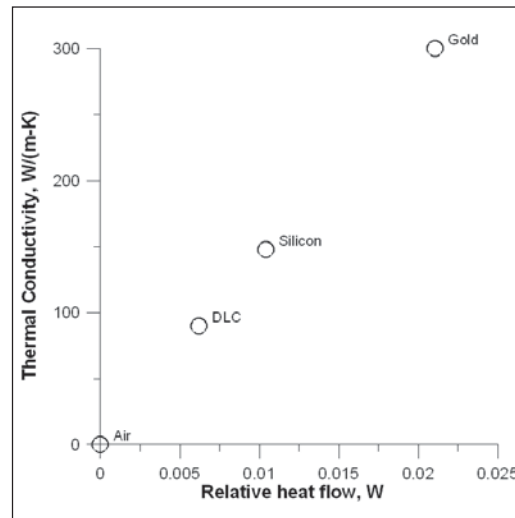


Figure 3. Thermal conductivity measurement of a 1.9 μm thick DLC coating and the comparative measurements of known materials using the same setup.

■ We have developed a method to measure the high-speed heating response of Insulated Gate Bipolar Transistors (IGBTs) packaged in high power modules. The method uses the gate-source voltage, V_{GS} , at a constant, relatively low current and at a high anode-cathode voltage as the temperature sensitive parameter. Under these circumstances, variations in V_{GS} result from equal changes in the threshold voltage. The method is used to validate and extract short-time constant thermal parameters for an electro-thermal simulation model of the IGBT (including the details of the package module). Under the measurement conditions used, there are concerns about the sharing of current between the chips in the package, but by taking these into account, excellent agreement is obtained between the measured and simulated temperatures (see Fig. 4). The module is shown in Fig. 5a.

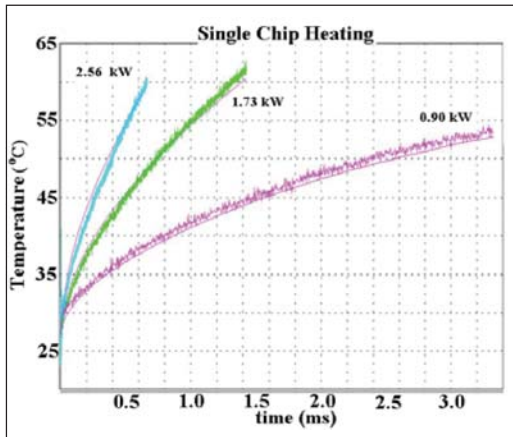


Figure 4. Electrically measured and computer simulated measurement of the temperature of IGBT chip in a power module.

■ An invited presentation, “Semiconductor Device Temperature Measurements,” was presented at the 20th IEEE Semiconductor Thermal Measurement and Management Symposium (SemiTherm) in March 2004. The talk covered the basic physical phenomena of a wide variety of temperature-sensitive devices and material parameters that have been used for measuring chip-level temperatures. The temperature, spatial, and temporal resolutions of each of the three generic measurement types (electrical, optical, and contacting) were emphasized. Power dissipation and excessive temperature have been identified as barriers to the continued shrinking and performance improvements for CMOS and beyond technologies. Perhaps the major issues with temperature measurements for advanced semiconductor chips and novel electronic structures are spatial and temporal resolution. Scanning thermal probes have been shown to have a spatial resolution between 30-50 nm, but they have a relatively slow time response and measurement interpretation is difficult due to the complexity of the physical contact between the probe and the specimen. Optical methods, such as thermoreflectance and Raman spectroscopy, potentially have picosecond time resolution, but they are diffraction limited in their spatial resolution typically to about 1 μm typically. There continues to be much interest in the development of methods for measuring chip temperatures with improved spatial and time resolution.

COLLABORATIONS

AEPT Consortium

DuPont: John Felten

MacDermid: Dennis Fritz

Merix: Bob Greenlee

MicroFab: Virang Shah

SAS Circuits: Richard Snogren, Matt Snogren

Colorado School of Mines: Ivar Reimanis, Saki Krishnamurthy, John Berger

University of Nebraska: Kevin Cole

Cenymex Corporation: Scott Joray

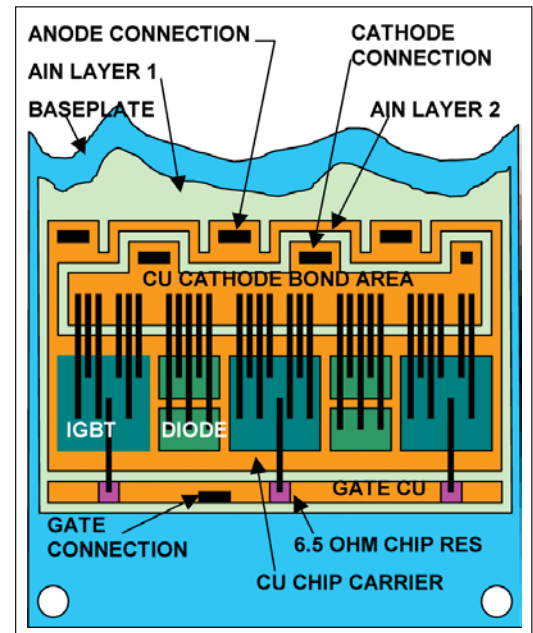


Figure 5a. Drawing of the layout of the IGBT chips within the module.

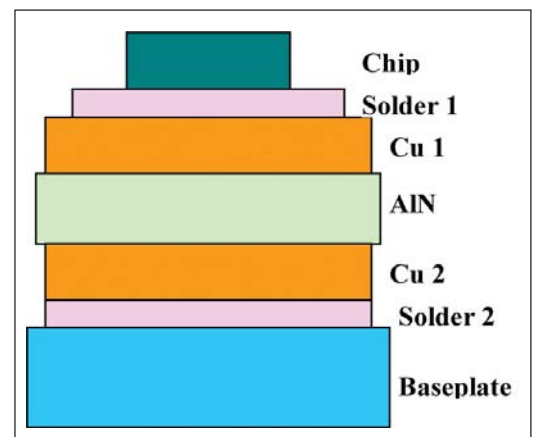


Figure 5b. Drawing of the vertical structure in the power module from one of the chips at the top to the baseplate at the bottom.

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DIELECTRIC METROLOGY SUPPORTING INTEGRATED PASSIVE DEVICE TECHNOLOGY

GOALS

To develop testing procedures which are specific to the needs of the electronic industry in the area of novel materials for Embedded Passive Device Technology. The current focus is on the broad-band permittivity at microwave frequencies, on dielectric withstanding voltage, and on key structural attributes that control the properties of organic resins filled with electronic modifiers. The development of Integrated Passive Device technology depends on the availability of suitable measurement techniques to evaluate materials' properties and the functional characteristics of the corresponding passive devices and power planes.

CUSTOMER NEEDS

Continuous reduction in the electrical charge required to drive logic gates and storage cells has resulted in tremendous progress in miniaturization and density of integrated circuits. However, in modern high speed electronics, the functional performance increasingly depends on passive components where the dielectric permittivity and impedance characteristic are the main factors that control spatial dimensions, time scale, speed, shape and amplitude of electronic signals. Passive devices have not shrunk in size as rapidly as active devices and they tend to occupy an increasingly larger area and mass fraction of the electronic subassemblies. In order to increase component density and reduce the parasitic effects of the associated interconnections, passive components may be integrated within substrates. Since integrated passive components are formed during substrate fabrication, they require new processing steps in addition to those that provide only interconnections. Also needed are new thin-film dielectric materials.

Novel dielectric hybrid materials based on polymers filled with modifiers of the electromagnetic properties have been identified by the industry as essential for advancing miniaturization and functional performance of high-speed electronics. There are significant challenges in developing new thin-film materials that must exhibit enhanced electrical performance characteristics, such as impedance and high dielectric constant (high- κ), in order to operate at higher microwave

frequencies and at increased voltage strengths. Consequently, new metrology methods are needed to address the specific behavior of thin film specimens and for better fundamental understanding of the relation between functional performance and the structural attributes of the materials.

The materials and testing requirements for Embedded Passives Technology are outlined in the National Electronics Manufacturing Initiative (NEMI) 2004 Roadmap. A need for new standard test methods for embedded materials was identified by the Association Connecting Electronic Industries (IPC), Roadmap 2005 Outlook Update, IPC Embedded Passive Device Standard Committee D-39.

TECHNICAL STRATEGY

1. The strategy pursued for the high frequency metrology for high- κ materials is to incorporate a thin passive film material into a device that comprises a capacitive or resistive termination in a transmission line. Samples that represent the recent development and technological trends in embedded passive materials are obtained from our industrial partners. We also use model polymer composite materials to validate the measurement methods. Multifunctional acrylate polymers filled with electronic modifiers such as ferroelectric ceramics, metal particles and carbon tubes of nanometer size are used to address fundamental dielectric properties of the composites. We have developed a broad-band measurement technique for measuring permittivity of embedded passive device materials at frequencies of 100 MHz to 12 GHz.

2. We are exploring non-linear dielectric measurement methodology for testing passive materials at high electric fields and voltages. Due to a thin film configuration, nonlinear effects may be activated at moderate bias levels and contribute to the dielectric break-down. Nonlinear dielectric effects cause rectifying, an increased repolarization loss, or act as frequency multipliers, thus altering the nominal impedance characteristic.

Technical Contacts:
J. Obrzut

"We truly need NIST expertise to take on this metrology work and help guide the participating people in the proper direction."

*Tom Newton
Director of PWB Standards
& Technology,
IPC, Association Connecting
Electronics Industries*

"Your effort to characterize the dielectric performance of the materials at high frequencies helped us to understand these materials and successfully realize our program objectives."

*David R. McGregor,
Leader of the high- κ
Materials Project, DuPont*

DELIVERABLES: AC dielectric withstanding voltage measurement system for embedded passive materials. Measure complex impedance of high- κ films as a function of applied high voltage using waveforms. Determine both the magnitude and phase of impedance from the corresponding voltage and current waves. 2Q 2004

3. Chairing the Test Methods Task Group, D-37d, for the IPC-4902 Embedded Passive Devices Standard Specification. This Subcommittee is responsible for developing test methods which are specific to the needs of the D-37 Embedded Passive Devices Committee and its three subcommittees for materials, performance and design. As these Embedded Passive Devices-specific test methods are developed, they will then be sent to the 7-11 Test Methods Subcommittee for inclusion in the TM-650 manual.

DELIVERABLES: IPC Test method for dielectric permittivity and loss tangent of embedded passive materials from 100 MHz to 12 GHz. 2Q 2004

4. Exploring the relationships between the dielectric properties and structure in polymer resins filled with ferroelectric ceramics. Our effort is focused on the local fast relaxation mechanism that we have discovered in dielectric composites.

DELIVERABLES: Identify key materials' attributes that control dielectric properties in polymers filled with ferroelectric inclusions. 2Q 2004

ACCOMPLISHMENTS

We have implemented a broadband technique as a standard test method that enables dielectric measurements at microwave frequencies of up to 12 GHz. The technique is based on the observation and theoretical analysis of the fundamental mode propagating at high frequencies in thin film dielectrics that terminate a coaxial air-filled transmission line.

In partnership with the Association Connecting Electronic Industries, IPC Task Force, we initiated a standard test method development, and chair the IPC-D37-d test method subcommittee for Embedded Passive Devices. We guided the design of the test protocol and made arrangements with co-sponsoring member companies for round robin evaluation. Example measurement of the dielectric constant obtained for high- κ DuPont materials are shown in Fig. 1.

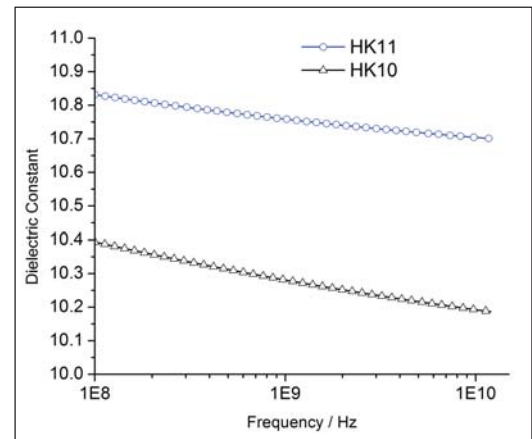


Figure 1. Dielectric constant of high- κ polyimidebased composite films determined according to the Standard Test Method. (HK10 is a 25 μm thick, HK11 is a 14 μm thick composite)

Our capability to measure the dielectric properties at high frequencies, in the sub-nanoscond regime for a wide range of dielectric permittivity values is used to quantify dispersion, alignment, and structure in hybrid materials. Using the broadband study, we demonstrated that the composites of organic polymer resins filled with ferroelectric ceramics exhibit a dominant intrinsic high frequency relaxation behavior. Such dielectric properties were found to be beneficial in eliminating the electromagnetic noise in processors and logic devices.

We have confirmed that the fastest dielectric relaxation process is controlled by the di-polar dynamics of the polymer matrix while the dielectric loss arises from the difference in coupling between the relaxed and unrelaxed dipoles. Our numerical models are capable to quantitatively correlate the dependence of the real and imaginary parts of the complex permittivity on the volume fraction of the ceramic filler.

Suitable experimental set-up and testing procedures have been demonstrated for unambiguous determination of the dielectric withstanding voltage of embedded passive materials.

In contrast to conventional procedures, the specimen voltage and current are determined as complex quantities from the corresponding time-resolved voltage waves. The new testing procedure represents a compatible extension of the existing standard test method, but is better suited for capacitive and resistive thin film materials. The specimen impedance and the loss tangent of the material can be determined by performing com-

plex algebra calculations. It was found that thin-film materials for embedded passives do not exhibit a constant impedance characteristic, as is the case for conventional dielectrics, but their impedance sharply decreases with increasing voltage. Conventional dielectrics, such as FR-4, exhibit a flat impedance characteristic, nearly independent of voltage, up to the material breakdown conditions. The break-down symptoms are associated with high-voltage flashing and sparking that typically require further failure analysis. We concluded that the existing test methods seem to be adequate for typical dielectrics for which substantial laboratory and field data have been accumulated. In contrast, the impedance of embedded passive materials decreases rapidly with increasing voltage.

Figure 2 shows that the impedance of the high- κ films decreases considerably with increasing voltage.

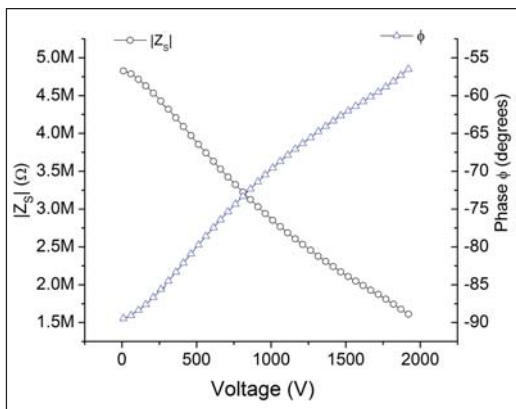


Figure 2. Impedance magnitude (circles) and phase angle (triangles) of high dielectric constant composites ($\kappa=11$).

The drop in impedance is accompanied by a significant change in phase. Under the applied electric field, the material undergoes a reversible transformation from dielectric to resistive. An equivalent impedance comparison indicates that high- κ organic composites can withstand only a small fraction of the conventional dielectric withstanding voltage. Such changing functionality from capacitive to resistive, may lead to thermal run-away due to excess of dissipated current. This mechanism is fundamentally different than the dielectric breakdown that occurs in typical dielectric materials, where the dielectric failure is due primarily to voltage excited avalanche ionization. It should be noted that the presented procedure of recording and analyzing waveforms allows the

evaluation of specific characteristics of materials that cannot be readily evaluated with conventional techniques. This measurement procedure is especially suitable for detecting and analyzing non-linear dielectric effects that can result from polarization reversal and rectifying barriers. Such effects may appear at relatively low voltages in nano-sized interfaces, composites and sub-micron thin dielectric films that are of interest to new technologies.

The voltage withstanding condition may be attributed to a voltage range where the impedance characteristic remains insignificantly affected by the applied voltage. The presented results demonstrate that such a condition can be inferred from Fig. 2 without ambiguity.

COLLABORATIONS

McGregor (DuPont), D. Senk (Shipley), D. Fritz (MacDermid), T. Bergstresser (Gould Electronics), K. Fjeldsted (Electro Scientific Industries), R. Greenlee (Merix Corp.), G. S. Cox (DuPont), J. Felten (DuPont), R. Crosswell (Motorola), C. Vanderpan (UL), R. Whitehouse (Sanmina-SCI)

RECENT PUBLICATIONS

J. Obrzut and A. Anopchenko; "High frequency input impedance characterization of dielectric films for power-ground planes," IEEE Trans. Instrum. Meas., vol. 52, pp. 1120-1124 (Aug. 2003).

J. Obrzut, A. Anopchenko, K. Kano, and H. Wang, "High Frequency Loss Mechanism in Polymers Filled with Dielectric Modifiers", Mat. Res. Symp. Proc., vol. 783, pp. B3.5-8 (2003).

J. Obrzut and A. Anopchenko, "Input Impedance of a Coaxial Line Terminated with a Complex Gap Capacitance – Numerical and Experimental Analysis", IEEE Trans. Instrum. Meas., vol. 54, August 2004 (in press).

J. Obrzut and K. Kano, "Measurement of Complex Impedance at High AC Voltages using Waveforms", IEEE Instrumentation and Measurement Technology Conference, IMTC/2004, Como, Italy 18-20 May, 2004, Conference Proceedings, vol. 3, pp. 1994-7 (2004).



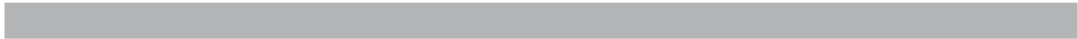
PROCESS METROLOGY PROGRAM

Device scaling has been the primary means by which the semiconductor industry has achieved unprecedented gains in productivity and performance quantified by Moore's Law. Until recently only modest changes in the materials used have been made. The industry was able to rely almost exclusively on the three most abundant elements on Earth — silicon, oxygen, and aluminum.

Recently, however, copper has been introduced for interconnect conductivity, replacing aluminum alloys. A variety of low-dielectric constant materials are being introduced to reduce parasitic capacitance, replacing silicon dioxide. As dimensions continue to shrink, the traditional silicon dioxide gate dielectric thickness has been reduced to the point where tunneling current has become significant and is compromising the performance of the transistors. This is requiring the introduction of higher dielectric constant materials. Initially the addition of nitrogen to the gate material is sufficient, but in the near future more exotic materials such as transition metal oxides, silicates, and aluminates will be required. As dimensions are reduced, gate depletion effects and dopant diffusion through the gate dielectric are limiting transistor performance. With the replacement of the traditional silicon dioxide/polysilicon gate stack processes with materials capable of supporting ever shrinking geometries, the task of the industry becomes more difficult. The overall task represented by the projects below reflects the need for analytical techniques with unparalleled spatial resolution, accuracy, robustness and ease of use.

Accurate metrology of process gases is essential for reproducible manufacture of semiconductor products. Critical physical parameters need to be measured on a wide variety of reactive and non-reactive process gases, allowing the accurate calibration of flow meters and residual gas analyzers. Water contamination at extremely low levels in process gases presents serious manufacturing difficulties. Accurate calibration of water vapor at extremely low vapor pressures is required.

Accurate metrology of process gases is essential for reproducible manufacture of semiconductor products and a wide variety of metrology issues emerge in plasma, chemical vapor, and rapid thermal processing steps used in semiconductor manufacture.



GAS PROPERTY DATA AND FLOW STANDARDS FOR IMPROVED GAS DELIVERY SYSTEMS

GOALS

NIST will measure the thermophysical properties of the gases used in semiconductor processing. The property data will improve the modeling of chemical vapor deposition and the calibration of mass flow controllers (MFCs). As the data are acquired, they will be posted to an online database.

NIST also will develop primary standards for gas flow in the range from 10^{-7} to 10^{-3} mol/s and transfer this flow measurement capability to the US semiconductor industry. (10^{-6} mol/s \approx 1.3 standard cubic centimeters per minute.)

CUSTOMER NEEDS

The 2003 *International Technology Roadmap for Semiconductors* (ITRS) emphasizes that the grand challenge for front-end processes is “material limited device scaling.” The Modeling and Simulations section reinforces this theme: “*Modeling and simulation tools in equipment, process, device, package, patterning, and interconnect are only as good as the input materials parameters. In many cases, these parameters are not known. Databases ... are needed.*” Meeting this challenge will require improvements in MFCs for the deposition and etching of diverse new materials. Thermal MFCs meter a wide variety of toxic, flammable, and corrosive gases over a large range of flow rates. Elements necessary for improved MFCs will be accurate models of gas properties and reliable physical standards for gas flow.

Participants at an industry workshop at NIST identified the gases and properties of highest priority, and they recommended publishing the property values in a public, Web-based database. The gases include process gases, “surrogate” calibration gases, and binary mixtures of process and carrier gases. The identified properties and required uncertainties include the following.

- heat capacity at constant pressure $\pm 0.1\%$
- equation of state (gas density) $\pm 0.1\%$
- viscosity $\pm 0.5\%$
- thermal conductivity $\pm 0.5\%$

The workshop also required the following uncertainties for physical standards for gas flow.

- primary standards for gas flow $\pm 0.025\%$
- transfer standards for gas flow $\pm 0.1\%$

TECHNICAL STRATEGY

We are measuring the speed of sound $u(T, p)$ in process gases and in the surrogate gases that are often used for calibration. The speed-of-sound data have relative standard uncertainties of 0.01 %. Measurement conditions range as high as 400 °C and 1500 kPa (or to 80 % of the vapor pressure for condensable gases). Figure 1 shows an example of such data. The speed-of-sound data are used to determine the ideal gas heat-capacities $C_p^0(T)$ with the targeted uncertainty of 0.1 %. The pressure and temperature-dependences of $u(T, p)$ are correlated with model two-body and three-body intermolecular potentials. These potentials are used to calculate the virial equation of state for the density $\rho(T, p)$ and to get first estimates of the viscosity $\eta(T)$ and the thermal conductivity $\kappa(T)$. For gases where reliable data exist, we verified that results calculated in this way have uncertainties that are less than 0.1 % for density, 10 % for viscosity, and 10 % for thermal conductivity from 200 K to 1000 K.

Technical Contacts:

Robert F. Berg
John J. Hurlly
Michael R. Moldover

“I was pleasantly surprised when I came across your database of thermophysical properties of gases used in the semiconductor industry. It was virtually exactly what I was searching for.”

Bob Rathfelder,
Project Engineer,
Parker Hannifin

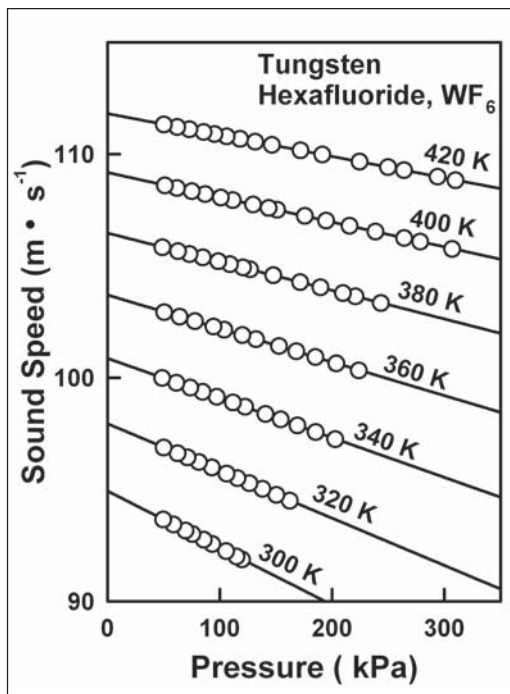


Figure 1. Speed of sound in tungsten hexafluoride as a function of pressure along isotherms.

We also are developing novel acoustic techniques to measure the viscosity and thermal conductivity with uncertainties of less than 0.5 % as specified by the industry workshop. Figure 2 shows a second-generation acoustic viscometer made from Monel. Throughout the project, the results will be made available to industry through publications in professional journals, presentations at professional meetings, and entries in an on-line database at <http://properties.nist.gov/semiprop> (see Fig. 3).

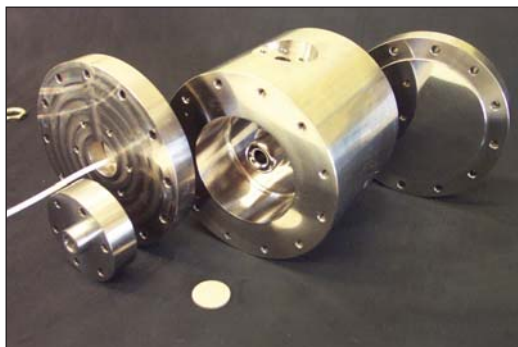


Figure 2. Second-generation acoustic viscometer made from Monel for use with corrosive gases.

Tungsten Hexafluoride				M.W. [1]	N.B.P. [2]	T.P. [2]	
WF ₆				P _c [3]	T _c [3]	V _c [3]	
				4.57 MPa	452.7 K	0.1 m ³ /kmol	
Returns to [Gas Index Fluid Science Group Process Measurements Division NIST Home SEMI NISTMP]							
T	C _p ^o (T)	Vapor Pressure	R(T)	ΔH _{vap}	C(T)	ΔC _v (T)	
K	J/mol·K	MPa	cm ³ ·mol ⁻¹	cm ³ ·mol ⁻¹ ·K ⁻¹	cm ³ ·mol ⁻¹	cm ³ ·mol ⁻¹ ·K ⁻¹	
Estimated Uncertainty	1% [4]	1%	Gas densities are calculated to better than 0.1% over the temperature and pressure ranges of the reference.			10%	10%
Reference	[4]	[6]	[5]	[5]	[5]	[5]	[5]
205	11.84	0.19	-2001.6	5951.2	-4638932	47121716	-
210	12.00	0.34	-1864.5	5441.0	-3653771	36754361	-
215	12.16	0.58	-1741.8	4994.1	-2894907	28924191	5.2
220	12.32	0.95	-1631.6	4600.8	-2291807	22949084	5.4
225	12.48	1.53	-1532.2	4252.9	-1829413	18345717	5.6
230	12.64	2.39	-1442.1	3943.9	-1446994	14767456	5.7
235	12.80	3.62	-1360.3	3668.3	-1109656	11942851	5.9
240	12.96	5.37	-1285.7	3421.6	-852936	9347555	6.0
245	13.12	7.79	-1217.5	3199.8	-770738	7985050	6.2
250	13.28	11.08	-1154.9	2999.9	-634150	6573288	6.3
255	13.44	15.47	-1097.3	2819.0	-505611	5435305	6.5
260	13.60	21.22	-1044.2	2654.0	-409306	4512569	6.6
265	13.76	28.66	-995.0	2505.4	-330711	3760514	6.8

Figure 3. Sample page from on-line database located at <http://properties.nist.gov/semiprop/>.

We have developed a diverse series of primary standards for gas flow. The first was a constant-volume (pressure rate-of-rise) primary standard that we developed to measure flows up to 10⁻³ mol/s with uncertainties of about 0.1 %. It has been replaced by a constant-pressure (variable volume) standard that can operate at pressures from 0.5 to 9 atmospheres. The third primary standard is gravimetric; flow measurements made by a transfer standard are integrated and compared to the weight change of a gas bottle. The second and third standards have a standard uncertainty

of 0.02 %. Figure 4 demonstrates the accuracy of the flow standards.

Transfer standards allow the primary flow standards at NIST to be compared to flow meters at other locations, such as MFC manufacturers. Although a flow meter manufacturer often uses its own primary standard, comparisons with NIST allow the manufacturer to demonstrate proficiency and, if necessary, provide traceability to NIST. For this purpose, we have developed a series of very stable transfer standards based on laminar flow through a thermostatted duct. The first generation used a stainless steel, helical duct of rectangular cross-section. It was used to perform on-site proficiency tests of industrial flow standards at fabrication facilities and MFC manufacturers. The second-generation transfer standard uses quartz capillaries with a circular cross-section, which are available commercially for gas chromatography. It has been used for comparisons with metrological institutes of other countries as well as manufacturers of flow meters. Its standard uncertainty is 0.03 %. The third-generation standard improves convenience by combining the quartz capillary with commercial instrumentation to measure pressure and temperature.

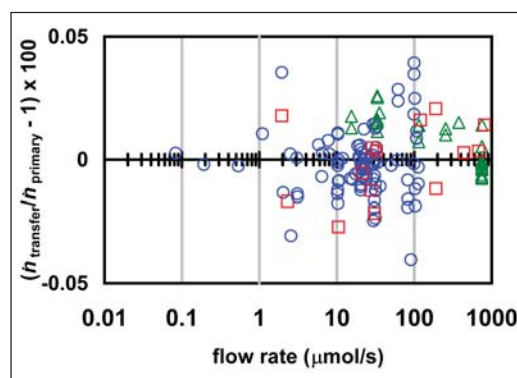


Figure 4. Comparison of three primary flow meters. The transfer standard compared the constant-pressure flow meter (circles) with the gravimetric flow meter (squares) and a constant-volume flow meter (triangles). (1 μmol/s ≈ 1.3 sccm.)

DELIVERABLES: Install new spherical resonator for measuring the speed of sound in the hazardous gases facility. 2Q 2004 Calibrate resonator by 3Q 2004.

A cylindrical resonator was used to study nine process gases, but it must be replaced due to contamination. A spherical resonator has been fabricated and will be installed in the hazardous gas handling facility. The spherical resonator will

be capable of producing higher accuracy measurements than the cylindrical resonator.

DELIVERABLES: Develop improved model of acoustic viscometer by 2Q 2004, develop model of acoustic thermal conductivity resonator by 3Q 2004.

The second-generation Greenspan viscometer incorporates lessons learned from the previous device, thereby allowing an improved acoustic model. The model of the thermal conductivity acoustic resonator will need to be tested and further developed from calibration measurements.

DELIVERABLES: Install second-generation Greenspan viscometer in hazardous gas facility by 1Q FY2004; write and test automation software by 2Q FY2004. Install gas thermal conductivity device in test facility by 2Q FY2004; write and test automation software by 3Q FY2004.

The improved Greenspan viscometer will be installed in the existing hazardous gas handling facility and the software running the apparatus modified. The thermal conductivity acoustic resonator needs to be incorporated into the facility to provide temperature and pressure control, and the computer code developed to run the system.

DELIVERABLES: From the speed-of-sound measurements, determine the ideal-gas heat capacity and equation of state for each species. Calibration gases by 3Q 2004, octafluoro-cyclobutane by 4Q 2004.

DELIVERABLES: Measure the transport properties in the semiconductor process gases identified by the customer. Calibration gases by Q2 2004, HBr by 4Q 2004.

Each new resonator must be calibrated with test gases such as helium and argon. After calibration and the appropriate safety assessments, the measurements of the semiconductor process gases will begin.

DELIVERABLES: Update on-line database by 4Q 2004, publish viscosity measurements in NF_3 and N_2O by 2Q 2004.

The measurements will be disseminated through papers in professional journals, talks given at professional meetings, and the on-line database.

DELIVERABLE: Submit to archival journal a paper on primary gas flow standards by 2Q 2004.

“Two primary standards for low flows of gases” was accepted by the NIST Journal of Research.

DELIVERABLE: Repackage transfer standard based on commercial measurement package by 2Q 2004.

The third-generation transfer standard will use commercial instrumentation to measure the pressures and temperature of gas flowing through a quartz capillary. The commercial instrumentation will improve the flow meters' convenience, and the quartz capillary will be the similar to that of the second-generation standard. Using the same capillary and model will ensure an uncertainty of 0.1 %. An improved design based on preliminary tests will improve the reliability of the capillary package.

DELIVERABLE: Test prototype Coriolis flow meter for gases by 3Q 2004.

Coriolis flow meters are the only devices that measure directly mass flow rate instead of a secondary quantity such as velocity or heat loss. The prototype flow meter is designed to measure the small Coriolis forces induced by flows less than 1000 sccm.

DELIVERABLE: Draft SP-250 for gas flow calibrations by 4Q 2004.

The SP-250 document will be used to establish a routine calibration service at NIST for gas flows in the range from 10^{-7} to 10^{-3} mol/s (0.1 to 1000 sccm).

ACCOMPLISHMENTS

- We designed and assembled a second-generation Greenspan viscometer. Its Monel construction allows the study of corrosive process gases.

- We measured the speed of sound in the process gases Cl_2 , NF_3 , and N_2O . Typically, the standard uncertainty of the speed of sound was less than 0.01 %. From these data the ideal-gas heat-capacity was determined to within 0.1 %, and an equation of state was developed to predict the gas densities to within 0.1 %. Viscosity was measured in these three gases plus CF_4 and C_2F_6 with an uncertainty of approximately 0.5 %.

- We continued to provide immediate access to our results by updating the database of gas properties at <http://properties.nist.gov/semiprop/>.

- We verified the accuracy of the primary flow meters by comparing the lower and upper ends of their ranges with other, overlapping NIST flow meters. Near both the lower end (0.3 sccm) and the upper end (1000 sccm) the agreement of 0.03 % was within the mutual uncertainty of the comparison.

- We used the second-generation transfer standard and a prototype of the third-generation transfer standard to make a comparison of gas flows with a manufacturer of mass flow controllers.
- We improved the temperature control of the constant-pressure primary flow meter to 0.01 K. We used additional temperature and volume measurements to further characterize this primary standard.

RECENT PUBLICATIONS

R. F. Berg, "Quartz capillary flow meter for gases," *Rev. Sci. Instrum.* **75**, 772-779 (2003).

J. J. Hurly, K. A. Gillis, J. B. Mehl, and M. R. Moldover, "The viscosity of seven gases measured with a Greenspan viscometer," *Int. J. Thermophys.*, **24**, 1441-1447 (2003).

LOW CONCENTRATION OF HUMIDITY STANDARDS

GOALS

The primary objective is to establish quantitative standards enabling the accurate measurement of trace quantities of water vapor ($< 10^{13}$ molecules cm^{-3}). This effort supports the development and application of commercial humidity sensors used for gas purity measurements and inline monitoring and process control — functions that are relevant to minimizing wafer misprocessing.

CUSTOMER NEEDS

As discussed in the 2001 International Technology Roadmap for Semiconductors (ITRS) in the chapter entitled Metrology, the evolution of sensor-based metrology for integrated manufacturing requires the development of in-situ sensors enabling in-time measurements. In Table 96 entitled Metrology Difficult Challenges, the need for robust and accurate sensor technology and impurity detection in starting materials is highlighted. Of the known impurities in processing gases, water vapor is one of the most ubiquitous and difficult to eliminate. Thus its measurement and control is often critical to various semiconductor-related processes.

Although a variety of high sensitivity sensors of water vapor are available, most do not directly measure water in the gas phase. Rather they typically respond to moisture-induced changes in bulk or surface properties associated with the adsorption of water vapor. Consequently, a rigorous first-principles determination of sensor response is often precluded, thus compromising accuracy. Moreover, since many such devices exhibit drift and poor reproducibility, frequent recalibration is required. Interpretation of these measurements is also complicated by complex physical interactions of water vapor with technical surfaces in transfer lines, in reaction chambers and in sensor housings.

TECHNICAL STRATEGY

The development of accurate and robust water vapor sensors requires well-characterized reference standards against which such devices can be evaluated. This should include a primary method of measurement for water vapor concentration and a complementary method yielding high-precision and stable sources of water vapor. By providing access and traceability to the unique capabilities at NIST discussed

below, instrument manufacturers and sensor users can assess the overall performance and accuracy of their measurements.

Technical Contacts:
J. T. Hodges
Dean Ripple



Figure 1. NIST Low Frost-Point (humidity) Generator.

“The LFPG is the ‘Gold’ standard for moisture generation and after the round robin experiments it is possible for the industry to talk about moisture measurements that can be compared to the standard.”

Suhas Ketkar,
Air Products and Chemicals

Our strategy is to establish complementary capabilities in high-precision generation and measurement of water vapor. To address these respective needs, we have developed a thermodynamically based humidity source and high-sensitivity optical absorption measurement methods discussed below. The thermodynamic humidity source, known as the Low Frost-Point Generator (LFPG) (see Fig. 1 and Fig. 2), serves as the project cornerstone and is capable of delivering 3 mmol to 3 nmol of water vapor per mole of dry gas. Here the water vapor concentration in a gas stream is precisely controlled by active regulation of the saturator temperature and pressure. As such, the LFPG

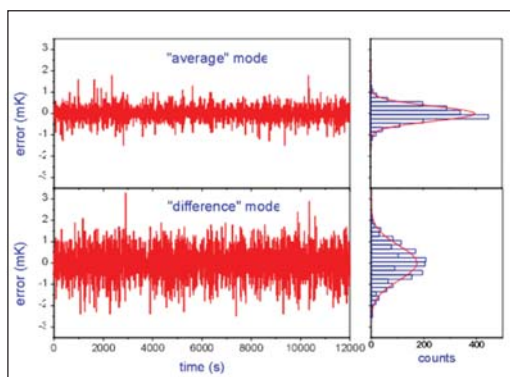


Figure 2. Steady state response of saturator control thermometers in NIST Low Frost-Point Humidity Generator.

is ideally suited for testing the performance of various sensing and humidity generation technologies. To date, it has been used to characterize water vapor measurement and generation systems at the research and development stage as well as commercial devices.

1. A common technology used by the semiconductor industry for delivering controlled quantities of water vapor is based upon the controlled permeation of water vapor (called permeation tube generator (PTG)) through a material, followed by mixing and dilution with a dry gas of known flow rate. We recently constructed a calibration system for water permeation tubes, comparing permeation tubes to the LFPG using a commercial water vapor sensor as a nulling device. This approach constitutes an efficient and low-cost mechanism for the dissemination of NIST trace humidity standards. To meaningfully characterize the long-term stability of this system and its combined uncertainty, measurements of the system performance must be taken over an extended time frame.

DELIVERABLES: Complete system testing and uncertainty analysis of permeation-tube calibration system. 3Q 2004

2. The basis for the LFPG as a humidity standard is knowledge of the temperature-dependent ice vapor pressure. The most commonly used correlation is that developed by Wexler of NBS. This correlation is generally considered valid to a minimum temperature of $-100\text{ }^{\circ}\text{C}$. Recent comparisons in our laboratory have revealed inconsistencies between humidity levels generated by thermodynamic saturators, which use the Wexler correlation, and permeation-tube based generators. To use the LFPG at temperatures below $-100\text{ }^{\circ}\text{C}$ will require understanding the source of these inconsistencies, which are as large as 2 nmol/mol . We will examine the validity of the Wexler ice-vapor pressure correlation as well as other possible effects.

DELIVERABLES: Determine the validity of the Wexler correlation at low temperatures, and determine the cause of the 2 nmol/mol inconsistencies. 3Q 2004

3. The LFPG is currently limited to generating greater than 3 nmol mol^{-1} of water vapor in N_2 based on the minimum achievable temperature of the saturator, and knowledge of the ice vapor pressure discussed above. A new strategy for pmol mol^{-1} -level humidity generation has been

identified. The approach involves the controlled dilution of water vapor/gas mixtures produced by the LFPG, using a flow dilution system similar to that incorporated within the PTG calibration system described above.

DELIVERABLES: Demonstrate extension of the LFPG to pmol mol^{-1} levels of humidity generation. 3Q 2004

4. To complement our established capability in precision generation of trace humidity levels, we are developing absolute techniques based upon the absorption of visible and near-infrared laser radiation. Water vapor has an absorption spectrum comprising thousands of distinct rovibronic absorption transitions in this spectral region. Thus, the concentration of water vapor can be readily determined in terms of measurements of sample absorbance and independently determined absorption line strengths. Recent advances in source and detector technology, and new spectroscopic techniques that extend the sensitivity of laser absorption measurements now enable the precise sensing of water vapor at concentrations below $10^{10}\text{ molecules cm}^{-3}$. To account for line broadening effects, and mitigate interference effects associated with absorption by other species the most precise absorption measurements require that individual transitions be spectrally resolved. This demands a technique having a frequency resolution much smaller than the characteristic widths of the absorption transitions, and requires that the frequency intervals in the measured spectrum be accurately determined. By combining high spectral resolution with high precision absorbance measurements, the water vapor concentration can be found independently of the composition of the carrier gas. Of the optical absorption methods, cavity ring-down spectroscopy (CRDS) is expected to be the most suitable for a primary method. CRDS is a cavity-enhanced optical absorption technique that has high sensitivity, fast response, and probes a compact well-defined volume. It is important to emphasize that under certain conditions, CRDS can exhibit exceptional spectral resolution, enabling detailed measurements of absorption line shape. To this end, we have developed a refined version of CRDS called frequency-stabilized single-mode cavity ring-down spectroscopy (FSSM-CRDS). Here, the ring-down cavity is actively length stabilized, the probe laser is frequency locked to the ring-down cavity, and the frequency axis of the spectra is based upon the longitudinal mode spacing of the ring-down cavity (see Fig. 3).

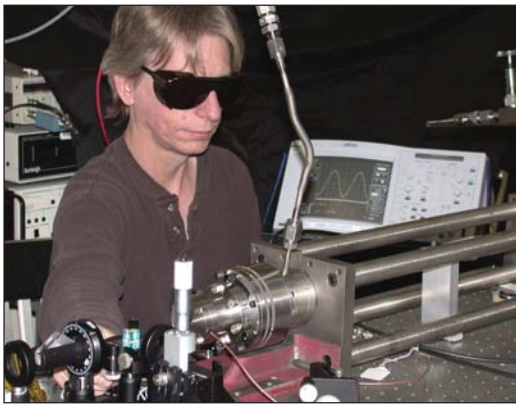


Figure 3. Frequency-stabilized CRDS system.

Using the existing FSSM-CRDS apparatus, appropriate transfer standard generators and hygrometers, we will link H₂O transition line strengths to thermodynamic-based LFPG. Taking advantage of the high spectral resolution afforded by FSSM-CRDS, pressure-broadening of these transition line shapes by various media will also be quantified.

DELIVERABLES: Link H₂O transition line strengths to LFPG for water vapor concentration measurements in the range 10 nmol mol⁻¹ to 100 μmol mol⁻¹ and measure N₂ pressure broadening coefficients. 4Q 2003

ACCOMPLISHMENTS

- In FY 2003 we constructed a permeation tube calibration facility (see Fig. 4). The purpose of this system is to provide measurement traceability for industrial users of permeation tube humidity generators. The calibration system comprises a custom PTG, the LFPG and high-sensitivity quartz crystal microbalance (QCM). The water-containing permeation tubes to be calibrated are placed inside the temperature-stabilized PTG oven. Water vapor diffuses from the tube surface into a



Figure 4. New PTG calibration apparatus.

precisely controlled stream of purified N₂. The diluent gas flow rate is adjusted so that the water vapor concentration produced by the PTG is equivalent to that produced by the LFPG, as measured by the QCM. From these measurements the water permeation rate of the tube under test can be determined in terms of the known LFPG output. As seen in Fig. 5, the calibrations derived from this system are repeatable to approximately 1%, which is significantly superior to traditional gravimetric methods.

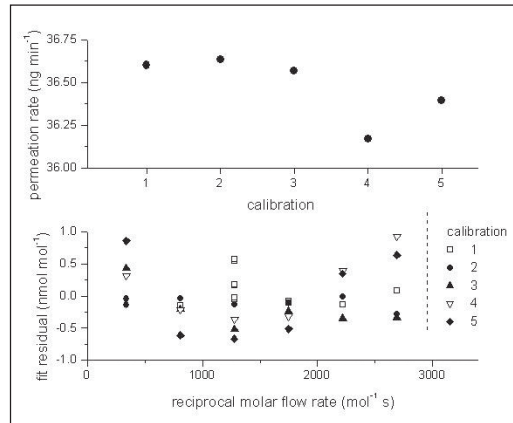


Figure 5. Calibration repeatability (top) and deviations from the fitting function (bottom) of a water-vapor permeation tube in the NIST Permeation Tube Calibration Facility.

- A new strategy for pmol mol⁻¹ (ppt) -level humidity generation was recently identified. The approach, shown in Fig. 6, involves the controlled dilution of water vapor/gas mixtures produced by the LFPG, using a flow dilution system similar to that incorporated within the PTG calibration system described above.

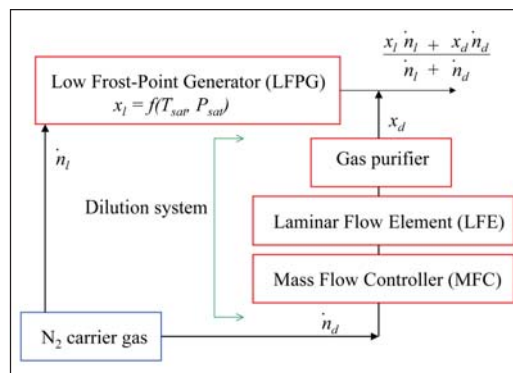


Figure 6. Proposed dilution system for extending the LFPG operating range to pmol mol⁻¹ levels.

■ The LFPG uncertainty analysis is based on the uncertainties in temperature and pressure within the LFPG saturator, ice vapor pressure and the enhancement factor for mixtures of water vapor and air. However, this analysis neglects background effects associated with the transient adsorption and desorption of water vapor from internal surfaces in the flow manifold located downstream of the LFPG. For the lowest range considered, such processes may affect significantly the water vapor concentration in the sample gas delivered by the LFPG to test instrumentation. In collaboration with Air Products Inc., we quantified the magnitude of this water vapor background using atmospheric pressure ionization mass spectrometry (APIMS). Results, shown in Fig. 7, indicate that background contribution to H₂O from system components downstream of the LFPG was less than 0.2 nmol/mol. These measurements also demonstrated that linearity deviations of the LFPG output H₂O mole fraction are less than 0.1 nmol/mol.

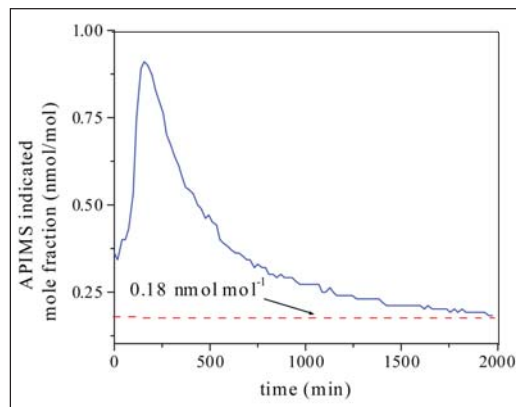


Figure 7. APIMS measurement of LFPG background H₂O concentration showing decay to steady state level.

■ We developed a quantitative method for comparing the outputs of commercial and custom permeation tube moisture generators (PTGs) to that of the LFPG. This technique is capable of resolving fractional differences of approximately 1 %, for PTGs covering the mole fraction range 10 to 100 nmol/mol. An intercomparison of PTG devices from several customers was completed. Uncertainties in flow metering and background water vapor present in the carrier gas were identified as limiting effects. This technique was the basis for the newly developed permeation-tube calibration service discussed above.

■ We measured trace levels of water vapor generated by the LFPG using a prototype diode laser hygrometer (DLH). This hygrometer, which was based upon wavelength modulation spectroscopy, had a linearity better than 1 % over the water vapor mole fraction range 3 nmol/mol to 2 μmol/mol and yielded a sensitivity of better than 0.5 nmol/mol when tested against the LFPG. These experiments and subsequent tests on a beta system were critical to the development of a similar DLH that is now commercially available.

■ We have successfully developed an FSSM-CRDS system to study the optical absorption of trace levels of water vapor with a resolution and accuracy unobtainable with other techniques. The system is based on a near-infrared continuous wave diode laser emitting near 936 nm. The gas sampling system is optimized for high-precision measurements of trace water vapor concentration. The flow system has all-metal seals, low dead volume, and active mass flow rate and pressure regulation. Background levels < 0.5 nmol mol⁻¹ (background equivalent) have been demonstrated. The FSSM-CRDS method was used to probe water vapor absorption transitions in the 935-nm spectral region. In conjunction with humidity standards for determination of water vapor concentration, these spectroscopic measurements yielded relative uncertainties in line strengths less than 1 %. Figure 8 shows measured spectra (symbols) and theoretical spectra (solid lines) for a pair of overlapping water vapor absorption transitions, each case corresponding to a given total gas pressure (with N₂ as the buffer gas). These results illustrate that the spectral resolution and linearity of the FSSM-CRDS method enable precise quan-

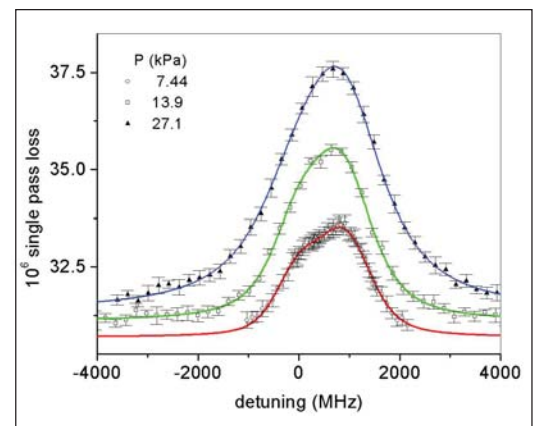


Figure 8. High-resolution FSSM-CRDS spectrum of a pair of pressure-broadened water vapor absorption transitions. Symbols are experimental points, and lines are Voigt fits to the measured profiles.

tification of pressure broadening, collisional narrowing and asymmetries of the absorption line shape, thus minimizing systematic errors in the determination of number density and line strength that typically arise from instrumental line broadening effects. Also, detection limits less than 10 nmol mol^{-1} of H_2O in N_2 have been demonstrated, using the relatively weak absorption lines near 935 nm accessible with the near-ir diode laser used in this system. Finally, a replica of the FSSM-CRDS system is now used to characterize the purity of semiconductor source gases in a molecular beam epitaxy (MBE) facility at NIST-Boulder.

COLLABORATIONS

Air Products and Chemicals Inc., Seksan Dheandhanoo; APIMS measurements of trace moisture and characterization of semiconductor gas purity.

NIST Optoelectronics Division, Kris A. Bertness; CRDS measurements of H_2O in III-V compound process gases.

Dow Chemical, Linh Le and J. D. Tate; CRDS measurements for process gas control RH Systems, Robert Hardy; Characterization of low range chilled-mirror hygrometers and humidity generators for standards laboratories.

Southwest Sciences Inc, Chris Hovde.; Development of wavelength modulation laser hygrometer for trace H_2O sensing.

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TEMPERATURE MEASUREMENTS AND STANDARDS FOR RAPID THERMAL PROCESSING

GOALS

The goal is to develop the technologies required to enable the improved accuracy of temperature measurements in semiconductor wafer processing as prescribed in the International Technology Roadmap for Semiconductor (ITRS).

Our project, initiated in FY97, has approached this goal with four objectives: (1) to improve calibration wafer technology to a 2 °C standard uncertainty in RTP by demonstrating the use of thin-film thermocouples (TFTCs) in conjunction with wire thermocouples (TCs) on test wafers for in-tool radiation thermometer (RT) calibration; (2) to improve procedures for calibration and characterization of lightpipe radiation thermometers (LPRTs); (3) to develop and validate models to account for wafer emissivity and the effects of chamber reflected-irradiation on temperatures determined from model-corrected RTs that are calibrated against blackbodies; and (4) to collaborate with the semiconductor industry in implementing new methods for reliable and traceable temperature measurements.

CUSTOMER NEEDS

The measurement needs of the semiconductor manufacturing industry have been stated in the ITRS. The requirement is for measurement and control of RTP tools to ± 2 °C at 1,000 °C during dopant anneal with calibrations traceable to the International Temperature Scale of 1990 (ITS-90). In the 2003 edition of the ITRS in the section on "Metrology Difficult Challenges" the roadmap states "Better sensors must be developed for ... wafer temperature measurement during RTA."

Current needs include better temperature measurement uncertainty in post exposure bake processing of resists and in rapid thermal processing (RTP) of wafers including silicide formation in the temperature range of 300 °C to 700 °C.

Our customers are the device manufacturers and the suppliers of thermal processing equipment and temperature measurement instrumentation. This community forms our project's Common Interest Group (CIG), 20 companies meeting annually at NIST since 1997. They serve as a bridge between research and practice, provide advice on shaping objectives, and generate

opportunities for technology transfer. We have had our NIST patented thin-film thermocouple wafer evaluated at the ISMT (Sematech)/University of Texas RTP LPRT test facility and at Vortek Ltd. manufacturers of RTP tools. Currently Applied Materials and Atmel, both RTP tool manufacturers, are evaluating the NIST test wafer.

TECHNICAL STRATEGY

Our strategy is to address five core elements of our research that will enable the semiconductor industry to meet the roadmap requirements: (a) fabrication of test wafers with improved thin-film technology for use by our industrial collaborators to demonstrate in-tool calibration of RTs traceable to the ITS-90; (b) development of silicon wafer emittance standards for improved temperature and emittance measurements; (c) experimentation on the NIST RTP test bed and thermal modeling to determine the effects of wafer emissivity and lightpipe proximity on in-tool calibration of LPRTs; (d) evaluating the transient response of temperature sensors in the post exposure bake (PEB) process; and, (e) calibration and characterization of RTs (including LPRTs, cable-less LPRTs or CLRTs, and laser-reflectometer RTs or LRRTs).

For the past few years, the CIG community has expressed the need for improved temperature and emittance uncertainties by using emittance standards. The ideal suite of emittance standards would include a set of three to six silicon wafers with different coatings. These standards would exhibit reproducible emittance behavior with temperature and time at heating. A set of such standards with calibrated emittances versus temperature and wavelength would be invaluable in verifying *in-situ* emittance and temperature measurements. With the advent of the NIST high-temperature emittance facility, the possibility of assembling a practical emittance standard suite is being realized.

DELIVERABLES: Evaluation and measurement of high-temperature emittance for suites of wafers; report of characterization results to be reported at key industry RTP conference. 4Q 2004

LPRTs have become mainstream in the temperature measurement in the RTP community. We have calibrated the LPRTs for RTP applications using a sodium heat-pipe blackbody (Na-HPBB)

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Staff-Years (FY 2004):

3 professionals
0.25 technician

Funding Sources:

OMP STRS (50%)
OU STRS (50%)

"On behalf of SensArray Corporation, I express our deep gratitude to NIST for significantly contributing to advances in semiconductor lithography process optimization and control. NIST has contributed to improved CD control in lithography processes through the establishment of measurement methods and standards for wafer thermal bake cycle dynamics in resist processing. This support is just in time, as the next area of focus for photo resist processing optimization is bake cycle dynamics. Your work will be of value to every advanced semiconductor factory."

Wayne Renken, President
SensArray Corp.

between 700°C and 900°C with an uncertainty of about 0.3°C ($k=1$) traceable to the ITS-90. Recently, cable-less LPRTs (CLRTs) offer a decisive advantage to enable radiometric measurements at lower temperatures than traditional LPRTs. New application of CLRTs can eliminate 2.0 °C or more uncertainty from the calibration scheme.

We are using the NIST RTP Test Bed to perform inter-comparisons between the TFTCs and the new low temperature (300 °C to 700 °C) CLRTs. The aims are (a) to demonstrate calibration procedures for and establish uncertainties of the CLRTs against the TFTCs *in situ*, and (b) to establish uncertainties for model-corrected CLRTs calibrated against blackbodies.

DELIVERABLES: NIST blackbody calibration of the CLRT and *in situ* calibration of CLRT at low temperature (300 °C to 700 °C) using NIST TFTC wafers. 3Q 2004

Cooperative projects with Applied Materials and Atmel industries are permitting investigations of the use of the NIST calibration wafers in industrial RTP tools. These evaluations are critical for transferring the NIST developments to the semiconductor processing industry. The NIST TFTC calibration wafer has demonstrated unique capabilities in temperature measurements and in establishing traceability to the ITS-90.

DELIVERABLES: NIST TFTC calibration wafers for RTP measurements and joint report with Applied Materials and Atmel on LPRT calibrations. 3Q 2004

Members of our CIG have also asked us to develop calibrated thin-film resistors for wafer temperature measurement from 300 °C to 600 °C. These measurements are needed for more accurate control of the silicide anneal RTP. We have undertaken the development of precision platinum thin-film RTDs directly on the Si wafers to improve the uncertainty of *in situ* wafer temperature measurement at these temperatures. This project is part of a CRADA (Cooperative research and development agreement) with the leading U.S. supplier of RTP calibration wafers.

DELIVERABLES: Report on the uncertainty and temperature range of thin-film Pt resistor thermometers directly on Si wafers. 4Q 2004

CIG meetings have been held annually since 1997 for the purposes of assessing and planning project research directions, and for fostering collaborative work with equipment suppliers, chip makers, and instrumentation suppliers. At the

11th International Conference on Advanced Thermal Processing of Semiconductors (RTP'03, Sept. 25-27, 2003, Charleston, SC), the meeting addressed several major needs in temperature measurement. We had requests by our industrial collaborators for test wafer demonstrations, post exposure bake process temperature measurement, and discussions on proposals for establishing emittance standard wafers. At RTP'03 our team organized two regular conference sessions under the theme of traceability of RTP temperature measurements. Papers were presented on TC and RT calibrations methods and thermal modeling. A panel discussed plans for an industry-wide emittance standards initiative. An important contribution by NIST to the initiative is the use of the high temperature properties measurement facilities to generate a reliable, traceable database and to validate optical properties models.

DELIVERABLES: Organize and conduct CIG meeting on traceable temperature measurements at key industry RTP conference. 4Q 2004

ACCOMPLISHMENTS

EMISSIVITY EFFECTS

We investigated the effect of different silicon wafer emissivities and the effect of low emissivity films on RTP wafer temperature measurements using LPRTs. We used a NIST TFTC calibration wafer in the NIST RTP test bed to calibrate the LPRTs *in situ*. The measurements of LPRTs viewing Au and Pt thin-film spots in the center of the wafer were compared to LPRT radiance temperature readings that viewed silicon surface with thermal oxide film. We found differences of up to 36 °C at 900 °C in the LPRT measurements due to the low emissivity films. A wafer temperature measurement model was presented at the annual RTP Conference to provide insight into the effects of wafer emissivity on LPRT measurements in RTP tools.

LIGHTPIPE PROXIMITY

We designed an experimental and analytical study to quantify the lightpipe proximity effect and provide a model for industrial users of LPRTs to correct their LPRT readings. The experiments employed TFTC wafers, our RTP test bed, and LPRT readings to characterize the effects of lightpipe proximity on wafer temperatures. We found that the wafer temperature can be depressed more than 20 °C by positioning the lightpipe tip too close to the wafer. These results were presented in a paper for the 2003 International Conference on Char-

acterization and Metrology for ULSI Technology and at the 2003 10th International Conference on Advanced Thermal Processing of Semiconductors (RTP03).

TRANSIENT RESPONSE OF TEMPERATURE SENSORS DURING THE POST EXPOSURE BAKE PROCESS

Recent studies on dynamic temperature profiling and lithographic performance modeling of the PEB process have demonstrated that the rate of heating and cooling may have an important influence on resist lithographic response. We conducted an experimental and analytical study to compare the transient response of commercial, embedded platinum resistance thermometer (PRT) sensors with surface-deposited TFTC. A dual instrumented wafer for PEB evaluation is shown in Fig 1. Experiments were performed on a commercial, fab-qualified module with hot and chill plates using wafers that have been instrumented with calibrated type-E (NiCr/CuNi) TFTCs and commercial PRTs.

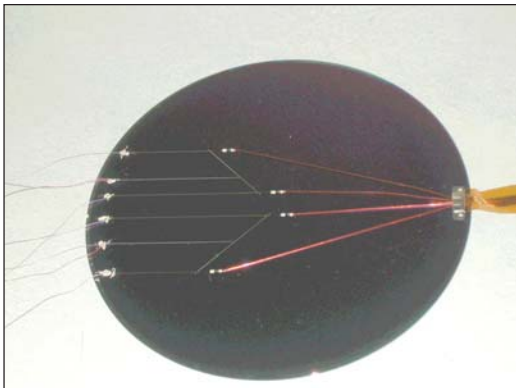


Figure 1. Wafer instrumented with PRTs and type-E thin-film thermocouples.

We measured the temperature of 200 mm Si wafers in a commercial type PEB module using both embedded PRTs and thin-film thermocouples (TFTCs). This instrumented wafer was thermally cycled from a chill plate to the PEB hot plate (up to 150 °C) and back to the chill plate. The sensors were read at 0.1 s intervals for 100 s. Figure 2 illustrates the differences between the PRTs and the TFTCs during the PEB cycle. The transient response of the TFTCs led the PRT sensors indicating a PRT lag (typically) of 2 °C on heating and up to 4 °C on cooling for several seconds. The wafer time constants for response were strongly affected by the air gap distance between

the wafer and hot plate as expected. The response times of the wafers were slower at lower hot plate temperatures (100 °C) as would be expected because of the lower thermal conductivity of air. Thermal models were presented that showed estimates for heating time constants in good agreement with experimental data (4.6 s to 5.1 s). Lithography simulation results were presented that showed the effects of transient and offset temperature profiles on CD variations.

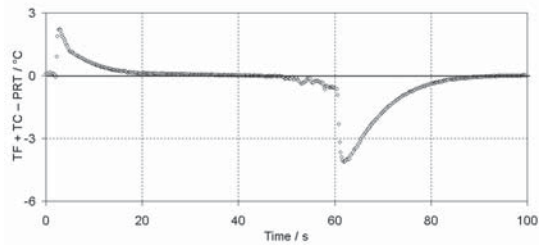


Figure 2. Difference between TFTC junction temperature and PRT during PEB thermal cycle.

EMITTANCE STANDARDS INITIATIVE

During the RTP 2003 Meeting in Charleston, SC, a whole session was dedicated to the introduction of the emittance standards initiative. The session was opened by comments from Steve Knight, the NIST OMP Director, who explained the role of NIST in the initiative. Three talks focused on NIST's role in the initiative and explained the NIST room-temperature reflectance facility, the NIST high-temperature emittance facility, and experimentally validated optical property models for semiconductor materials. The climax of the meeting occurred when a panel of experts in the RTP industry discussed the need for creating emittance standards with measurements traceable to NIST and explained what the standards would entail. A summary of conclusions and action items were listed, and the final outcome was the unanimous desire and support for creating emittance standards, as voiced by the panel. Invitations were issued to five different RTP manufacturers and users, who had expressed a need for emittance standards. To date, four of the five vendors have already submitted sets of silicon wafer standards for measurement. The high-temperature facility is being set up to commence characterization of the standards.

LASER-REFLECTOMETER RADIATION THERMOMETER

A Laser-Reflectometer Radiation Thermometer (LRRT) employs a reflectometer to measure normal

reflectance and Kirchoff's Law to calculate the emissivity. The measurements of the emissivity and the radiance temperature can be combined to determine the true surface temperature. Although alignment was very sensitive and frequent in-situ emissivity calibrations with the LRRT was necessary, the measured emissivity values differed from NIST measurements with the Spectral Tri-function Automated Reference Reflectometer (STARR) facility by less than 2%, while the measured temperatures differed with the NIST thin-film thermocouples by less than 4 °C. With improvements in the LRRT, it is possible to take advantage of the emissivity measurement to make a more accurate temperature measurement of the wafer during processing.

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PLASMA PROCESS METROLOGY

GOALS

To provide advanced measurement techniques, data, and models needed to characterize plasma etching and deposition processes important to the semiconductor industry, enabling continued progress in model-based reactor design, process development, and process control.

CUSTOMER NEEDS

To fabricate future generations of devices, the semiconductor industry requires improvements in plasma etching and deposition processes. Plasma processes and equipment face increasingly stringent requirements due to the need to maintain high device yields at decreasing feature sizes, the introduction of new dielectric materials, and the constant pressure to keep production efficiency high. To meet these challenges, the International Technology Roadmap for Semiconductors (ITRS) identifies a need for better predictive system modeling. To obtain more reliable predictions of the chemical, physical, and electrical properties of processing plasmas, further progress in model development and validation is required. ITRS also identifies a need for improvements in intelligent process monitoring and control, which require the development of robust and reliable sensors that are compatible with manufacturing equipment.

TECHNICAL STRATEGY

Our multifaceted program provides numerous outputs to assist our customers, including advanced measurement methods, high-quality experimental and fundamental data, and reliable, well-tested models of plasma behavior.

First, we develop and evaluate a variety of *measurement techniques* that provide industry and academia with methods to characterize the chemical, physical, and electrical properties of plasmas. The techniques we develop include improved laboratory diagnostic measurements for use in research and development, as well as more robust, non-perturbing measurements for use in process monitoring and control in manufacturing applications.

In addition to measurement techniques, we also provide *data* necessary for gaining an understanding of complex plasma properties and for testing and validating plasma models. The data help semi-

conductor manufacturers and plasma equipment manufacturers to better understand and control existing processes and tools and help them to develop new ones. The experimental data we provide are measured under well-defined conditions in highly-characterized standard plasma reactors. Our reactors include capacitively coupled cells as well as inductively coupled, high-density plasma reactors, one of which is shown in Fig. 1.

Finally, we are engaged in the development and validation of plasma *models*. Such efforts concentrate on modeling of plasma sheaths, the thin regions at the boundary of the plasma. Sheaths play a dominant role in determining discharge electrical properties and the properties of the highly energetic ions that are necessary for plasma etching. More accurate sheath models are needed to better predict and optimize discharge electrical characteristics and ion kinetic energies. Sheath models are also used to develop new types of process monitoring techniques based on radio-frequency electrical measurements.

Our ongoing and planned efforts focus on measurement, data, and modeling challenges in the following specific areas:

1. An electrical measurement technique for use in process monitoring and control applications is under development. This technique relies on non-invasive, non-perturbing measurements of the radio-frequency current and voltage applied to plasma reactors. The rf measurements are compatible with commercial reactors and they contain valuable information about the flux and energy of the ions that bombard wafers during

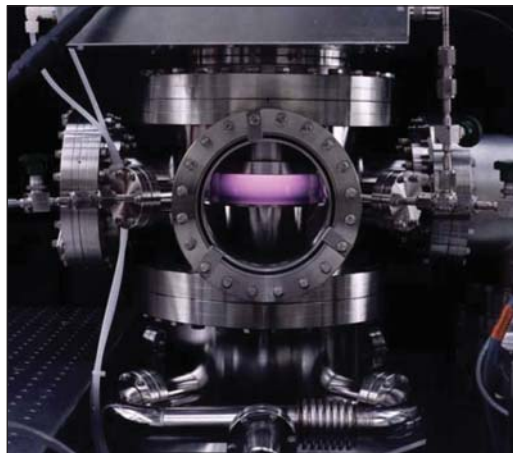


Figure 1. One of the inductive, high-density plasma reactors used in our experimental studies.

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“NIST is one of the leaders in plasma processing related research in the US. They have capability to thoroughly understand plasma behavior using a variety of diagnostics tools.”

Peter Ventzek
Motorola

“The NIST plasma process metrology group has helped us to understand the fundamental physical and chemical processes that are important to electronics materials and semiconductor processing industries.”

Bing Ji,
Air Products and
Chemicals, Inc.

processing. Values for the total ion flux and ion energies are obtained by analyzing the current and voltage signals using electrical models of plasma sheaths. Tests to validate the technique have largely been completed. Plasma potentials, sheath voltages, total ion currents, and ion energy distributions obtained from the rf measurements have been compared against independent measurements and shown to be in good agreement. At present, development is focused on making continued improvements in the speed of the analysis algorithms. Present and future efforts are also directed towards demonstration of the usefulness of the technique in real-time process monitoring and control applications. We have already demonstrated that large drifts in ion flux and ion energy can be detected and monitored during sputter deposition processes. Additional experiments are planned to evaluate the usefulness of the technique in monitoring drift in ion flux and ion energies during plasma etching processes.

DELIVERABLES: Demonstration and evaluation of rf-based ion flux and ion energy monitoring during plasma etch processes. 4Q 2004

2. Many industrial plasma etchers are equipped with optical emission spectrometers, which have proven useful for endpoint detection, fault detection and classification, and automatic process control. At present we are planning and initiating experiments in which optical emission measurements will be combined with the noninvasive electrical measurements described in item 1, above. Optical emission complements the electrical measurements by providing information about drift or other changes in the chemical species within the plasma—information that would be difficult or impossible to obtain solely from electrical measurements. We will evaluate whether data provided by optical emission can be used by the electrical analysis algorithms to obtain increased accuracy in ion current and ion energy monitoring. We also plan to assess the relative merits of optical and electrical detection of various types of process drift, equipment faults, and other changes such as etch endpoint.

DELIVERABLES: Compare sensitivity and utility of optical emission and electrical techniques for monitoring drift in etching reactors. Evaluate improvements gained by combining electrical and optical emission measurements. 4Q 2005

3. We currently are developing a new optical diagnostic technique, sub-millimeter wave spectro-

scopy, to measure the density and temperature of important chemical species in plasmas. Work is progressing on validating the sensitivity limits of important plasma species and feed gas contaminants. In addition, spatially resolved absorption measurements will be made to map out the species and temperature distributions within the plasma and surrounding gas. Sub-millimeter wavelength absorption measurements of radical densities will be correlated with the etching characteristics of coated wafers for a variety of different fluorocarbon/oxygen etching plasmas.

DELIVERABLES: Measure variations of radical densities in fluorocarbon/oxygen etching plasmas as a function of oxygen content for comparison with etching characteristics of blanket coated wafers. 3Q 2004

4. In order to continue the progress in shrinking semiconductor device dimensions, the ITRS Roadmap requires that lithographic techniques switch to shorter wavelength sources. Photoresist materials which are now commonly used do not work at these shorter wavelengths, so that entirely new materials based on very different chemistry are required. How the new photoresist materials will interact with etching plasmas is poorly understood at best. We will be applying a broad range of diagnostic capabilities (optical emission spectroscopy, sub-mm absorption spectroscopy, electrical diagnostics, ion mass spectrometry, ion energy analysis, microwave interferometry, and Langmuir probe techniques) to study plasma-surface interactions with new 157-nm photoresists. Initial work will focus on how etching of photoresist alters the etching plasma. Later work will examine polymer deposition and other means by which the plasma affects the photoresist surface.

DELIVERABLES: Characterize plasma-surface interactions of 157 nm photoresists with fluorocarbon etching plasmas. 4Q 2004

ACCOMPLISHMENTS

■ We have recently demonstrated that our noninvasive, model-based electrical technique is able to monitor drift in ion current and ion energy in an inductively coupled plasma reactor. The drift is caused by the slow deposition of a conductive film on the vacuum surface of the quartz “dielectric window” which is located beneath the inductive source. Such films can be formed during plasma etching or deposition processes, or simply by operating the reactor in an inert gas

(argon) when no wafer is present on the substrate electrode. The conductive layer interferes with the coupling of power from the inductive source into the plasma, resulting in a decrease in ion current and plasma density. As the film grows, the downward drift in ion current and plasma density in turn produces drift in ion kinetic energy distributions. The drift in ion energies can be large or small, increasing or decreasing, depending on rf bias conditions (see Fig. 2). Three different mechanisms have been identified that explain the changes in ion energies. These mechanisms, as well as the monitoring technique itself, are not limited to the particular experimental conditions studied so far; rather, they are applicable to a wide range of plasmas and reactors. Undoubtedly, similar drifts in ion energy have contributed to process drift in many manufacturing and research reactors. Future experiments are planned to monitor drift and other sorts of irreproducibility during plasma etching processes. These studies should provide additional demonstration of the usefulness of the noninvasive monitoring technique. They also should provide an understand-

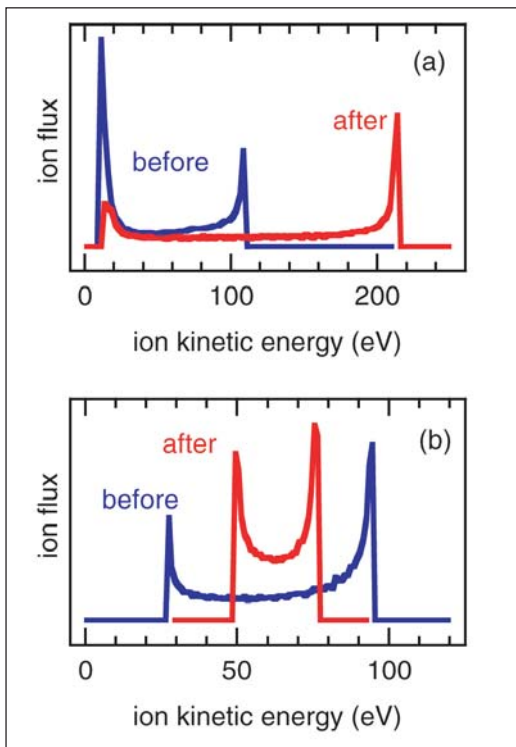


Figure 2. Ar^+ ion energy distributions obtained from noninvasive electrical measurements before (blue) and after (red) deposition of a conductive film on the inductive source window, for 10 mTorr argon plasmas at 100 W inductive source power. (a) constant bias power at 1.0 MHz, and (b) constant bias voltage at 10 MHz.

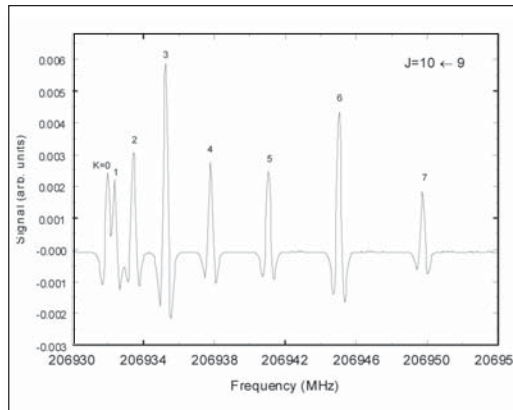


Figure 3. Sub-millimeter wave absorption spectrum of CHF_3 in a high-density, inductively coupled plasma.

ing of drift processes that could help one to minimize or eliminate ion energy drift and the damage to processed wafers that results from it.

- Sub-millimeter wave absorption spectroscopy is being developed as a plasma diagnostic to identify and monitor species in etching plasmas. Sub-mm wave spectroscopy can monitor the crucial chemical species in a plasma and provide the necessary feedback for understanding plasma processing (see Fig. 3). A new sub-millimeter source based on a 48x frequency multiplication chain of planar diodes has been evaluated. The spectral resolution of the sub-mm diagnostic is high enough to easily enable measurements of translational temperatures through the Doppler broadening of absorption line shapes. Gas temperatures are important input parameters to many plasma models since they are necessary to relate the measured gas pressure to the actual particle density in the chamber. All measurements indicated absorption line shapes consistent with room temperature gas. This is in disagreement with other spatially resolved measurements such as laser-induced fluorescence measurements of rotational temperatures which have found significantly higher temperatures in inductively coupled plasmas. This disagreement is probably due to a large volume of cool gas which surrounds the plasma due to the geometry of our plasma vacuum chamber. The vacuum chamber was modified with special window inserts to reduce the outside gas volume. The window inserts did significantly decrease the signal contributed by cold gas outside the plasma, but even with the inserts, line shape measurements still indicated room temperature gas within the cell. Simple modeling of a two temperature gas distribution indicates that even a very small volume of cool gas can mask a high

temperature region when measuring line-integrated line width measurements. In order to measure translational gas temperatures within the plasma using sub-millimeter absorption spectroscopy, multiple radial absorption measurements will need to be mathematically inverted to spatially resolve the Doppler broadened absorption line shapes.

■ We also recently developed the capability to measure spatially resolved 2-D temperature maps in fluorocarbon plasmas using planar laser-induced fluorescence (PLIF) of the CF radical (Fig. 4). Several PLIF images are measured, each probing a different rotational level to give a 2-D map that is related to the CF population in the probed rotational state. With the relative population for several rotational levels known at each location, a rotational temperature map is calculated and assumed to be equivalent to the gas temperature under these conditions. We have measured temperature maps in CF_4 plasmas as a function of pressure and power, with and without silicon wafers present. Simultaneously, CF density images were obtained. Under our conditions, radial variations in temperature from 10 K to 90 K were observed. Axial temperature gradients were also observed to be quite large, especially under our highest pressure conditions (800 mTorr or 107 Pa). The strongest temperature gradients were consistently found near the cooled electrode surfaces. These variations can have strong implications. Species density measurements that probe a specific rotational level can

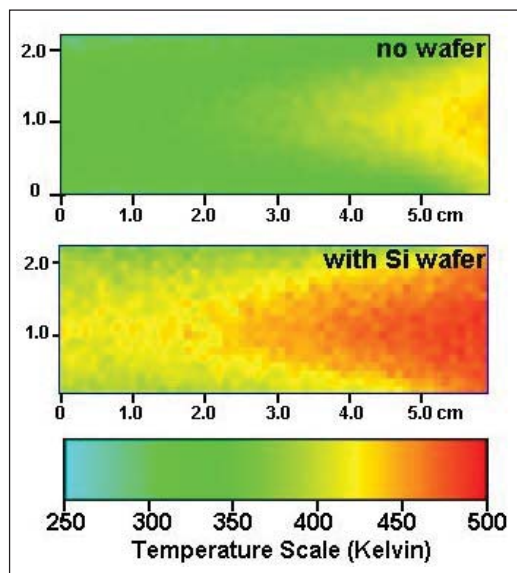


Figure 4. Temperature maps of a capacitively coupled CF_4 plasma at 200 mTorr with and without a Si wafer.

be misleading if the population of the chosen rotational level is not constant within the temperature range investigated. In addition, gas density in hotter regions will be lower, and this must not be interpreted as a chemical effect. Especially near surfaces, where species density fluxes are often interpreted as indicating surface chemistry, one must be aware of the implications of these temperature effects. In addition, understanding temperature is important for modeling, since chemical reaction rates are often a function of temperature.

■ Fundamental data continue to be distributed to plasma modelers throughout industry and academia via the Web-based NIST “Electron Interactions with Plasma Processing Gases” database (<http://eeel.nist.gov/811/refdata/>) (Fig. 5). This Web site has experienced tens of thousands of hits throughout its history.

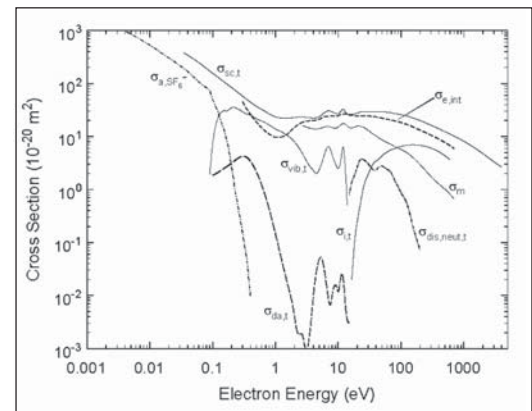


Figure 5. Recommended electron cross section data for SF_6 (shown here) and many other plasma processing gases are available at <http://eeel.nist.gov/811/refdata/>.

RECENT PUBLICATIONS

K. L. Steffens and M. A. Sobolewski, “A technique for temperature mapping in fluorocarbon plasmas using planar laser-induced fluorescence of CF,” *J. Appl. Phys.* **95**, in press (2004).

M. A. Sobolewski, “Monitoring sheath voltages and ion energies in high-density plasmas using noninvasive radio-frequency current and voltage measurements,” *J. Appl. Phys.* **95**, 4593-4604 (2004).

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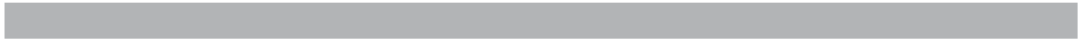
E. C. Benck, Y. Wang, and A. Goyette, "Ion energy distribution and optical measurements in high-density, inductively coupled C₄F₆ discharges," *J. Appl. Phys.* **94**, 1382-1389 (2003).

M. Edamura and E. C. Benck, "Transition from E to H mode discharge in pulse-modulated inductively coupled plasmas," *J. Vac. Sci. Technol. A* **21**, 470-475 (2003).

M. A. Sobolewski, "Monitoring sheath voltages and ion energies in high-density plasmas using noninvasive radio-frequency current and voltage measurements," in *AIP Conf. Proc.* **683**, *Proceedings of the 2003 International Conference on Characterization and Metrology for ULSI Technology*, 195-199 (2003).

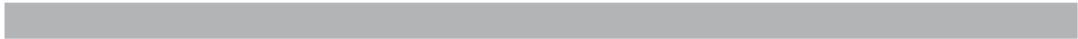
E. C. Benck, G. Y. Golubiatnikov, G. T. Fraser, D. Pluesquelic, R. Lavrich, B. Ji, S. A. Motika, and E. J. Karwacki, "Submillimeter-wavelength plasma diagnostics for semiconductor manufacturing," in *AIP Conf. Proc.* **683**, *Proceedings of the 2003 International Conference on Characterization and Metrology for ULSI Technology*, 190-194 (2003).

M. A. Sobolewski, Y. Wang, and A. Goyette, "Measurements and modeling of ion energy distributions in high-density, radio-frequency biased CF₄ discharges," *J. Appl. Phys.* **91**, 6303-6314 (2002).



ANALYSIS TOOLS AND TECHNIQUES PROGRAM

The continuing shrinking of device dimensions and the rapid inclusion of new materials into device fabrication demands the development of new analytical tools and techniques. These offer substantially greater sensitivity over existing tools and techniques.



THIN-FILM X-RAY METROLOGY FOR MICROELECTRONICS

GOALS

This new multi-year collaborative effort between ISMT and NIST will provide the semiconductor community with the methodology for accurate thin film characterization using X-Ray Reflectometry (XRR).

CUSTOMER NEEDS

In recent years, the semiconductor industry has driven scientific advancement for the processing of nanometer-scale material coatings with unprecedented uniformity in thickness, composition control, and unique electrical and mechanical properties. Nano-technology represents the fastest growth area of industry in the United States today. Simultaneous to this rapid advance in thin film technologies, the X-ray diffraction community and instrument vendors have developed techniques such as High-Resolution X-Ray Diffraction (HRXRD) and X-Ray Reflectometry (XRR) that permit the quantitative profiling of thin film characteristics, such as thickness, density profile, composition, roughness, and strain fields. With the XRR method in particular, parameter modeling has become an increasingly intractable problem, involving de-convolution of instrument response effects and software modeling assumptions, which has prevented the realization of the technique's potential in the characterization of nano-dimensional thin film structures. This program addresses the mounting industry call for accuracy in thin film characterization, such as in thickness and roughness determination.

TECHNICAL STRATEGY

This fundamental XRR study involves two parallel characterization projects being performed on identical, temporally stable, multilayer artifacts supplied by SEMATECH. The NIST project will consist of in-house XRR and HRXRD characterization analyses with traceable measurement equipment and fundamental modeling providing analysis of instrumental and material parameters (see Fig. 1). This work will take approximately three years to provide calibration artifacts and will start June 2004.

Technical Contact:
James P. Cline
Donald Windover

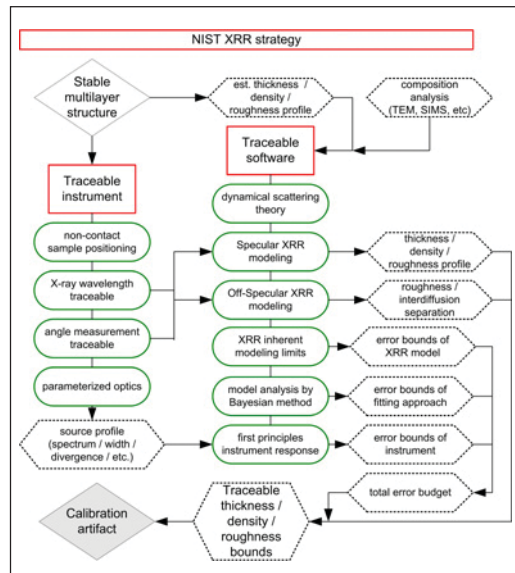


Figure 1. NIST XRR strategy. Measurements and modeling performed on temporally stable test structures will be performed using NIST SI traceable instrumentation constructed for current High Resolution X-Ray Diffraction work.

Over the past seven years, the Ceramics Division of the Materials Science and Engineering Laboratory (MSEL) has constructed the Ceramics Division Parallel Beam Diffractometer (CDPBD) for traceable measurements of XRR and HRXRD artifacts (see Fig. 2). Two axes of the goniometer assembly, ω and 2θ , feature on-axis optical angle encoders capable of $\pm 0.2 \mu\text{rad}$ accuracy (± 0.04 arc seconds). With the use of reference crystals with traceable lattice parameter to a relative uncertainty of $3 \text{ in } 10^{-8}$, the X-ray wavelength can be calibrated with a relative uncertainty of $\sim 1 \text{ in } 10^{-7}$ (this instrument will be used to redefine the literature value for Cu $k\alpha$ radiation accuracy). The interchangeable, kinematic-mounted monochromator used for XRR and HRXRD features twin, independently controllable asymmetric/symmetric Si (220), 2/4-bounce channel-cut crystals in a Bartels configuration. The wavelength spectrum, peak intensity, beam width, angular divergence, and all associated optics parameters will be incorporated in a first-principles characterization of the instrument response function suitable for XRR profile modeling.



Figure 2. Ceramics Division Parallel Beam Diffractometer (CDPBD). Showing rotating anode source (center left), monochromator / optics platform (upper center), diffraction goniometer (lower right), receiving optics/detector (center right), and cable managing goniometer (top center).

The collaboration project with SEMATECH will consist of measurements with conventional XRR instrumentation and include complimentary compositional analysis results as feedback comparison with NIST measurements performed in parallel. NIST will then use results from NIST traceable measurements, SEMATECH measurements, and NIST reflectometry modeling, to develop software for estimating the accuracy and precision ranges possible from conventional instrumentation and conventional modeling software. The XRR results comparison will allow for accuracy in measurement error analysis (see Fig. 3).

This accuracy simulation in measurement error will address both alignment / instrumentation error bounds and XRR modeling limitations, and will be applicable to arbitrary films of user input thickness, roughness, and compositional values. Instrument / software calibration artifacts will be developed by comparing resulting conventional measurement error budgets with traceable measurement error budgets to assess the total error budgets for several unique, temporally stable structures for use by SEMATECH. These artifacts will be available for conventional instrument calibration and stability monitoring.

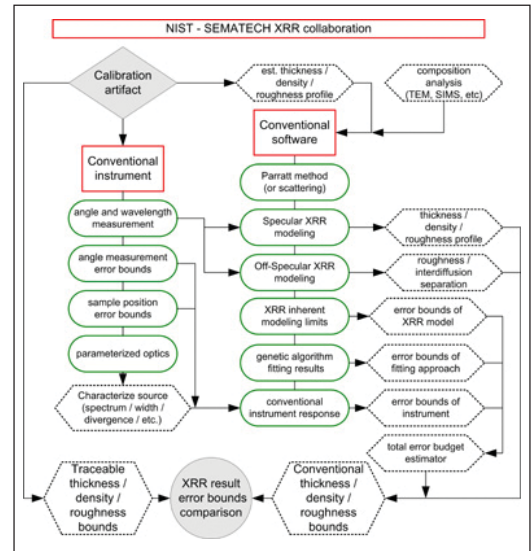


Figure 3. NIST – SEMATECH XRR strategy. Measurements performed on temporally stable test structures at SEMATECH will be analyzed at NIST using conventional software and compared NIST traceable results to provide error bounds comparison.

To address instrumentation effects on accuracy, work must be performed with different conventional XRR system geometries to discover the mechanical alignment parameters that dominate errors in XRR modeling results. We will start with a rigorous analysis on the error bounds imposed by goniometer and sample misalignment in conventional XRR instrumentation. The conventional-instrument X-ray source characteristics will be parameterized to provide further model refinement parameters. These combined error budgets will provide a multidimensional range of instrument response profiles that will be analyzed for parameter-specific limitations and accuracy restrictions on modeling of thickness and roughness.

Conventional modeling software results will be compared to results from NIST XRR theoretical, computational and Bayesian analysis results. Several analytical approaches will then be applied to conventional software to separate result deviations caused by conventional software approaches (for example, the Parratt continuous media model has limitations in analyzing porous films) from the limitations inherent in the XRR modeling methodology (for example, materials with intensive inelastic scatter and/or minimal scatter cross-section contrast between layers). Genetic algorithm fitting minimization will be compared

with a range of complimentary fitting approaches including Bayesian approaches to identify possible error bounds associated with the various fitting criteria and initial layer parameter estimates. Effects on modeling results caused by varying instrument parameters such as the physical dimensions, divergence terms, and wavelength spread of the X-ray source must be carefully analyzed. Some conventional software packages account for some of these instrumental parameters and the conventional results must be compared to NIST fundamental results to verify applicability and proper implementation. The calculated thickness, density, and roughness information provided by modeling Specular XRR (S-XRR) and Off Specular XRR (OS-XRR) as well as total error budgets caused by the instrument response function and modeling effects will be compared against the same parameters measured from NIST traceable instrumentation, to verify the validity of the error budgets and overall project approach.

The final results available to SEMATECH will include XRR error budget estimation software, and calibration artifacts necessary for optimizing the performance of conventional XRR instruments. Accuracy and precision estimation software will determine the limitations of XRR applicability for arbitrary multilayer systems on conventional XRR instrumentation. Calibration artifacts measured on NIST traceable instrumentation will allow routine system monitoring, alignment calibration, and instrument response function profiling to ensure conventional instrument precision and stability. Both deliverables will dramatically improve the precision and accuracy of conventional XRR characterization of multilayer structures having well-established composition and uniformity.

Our deliverables schedule for the calendar year 6/2004-6/2005 time frame follows:

DELIVERABLES: XRR modeling analysis with conventional software. 4Q 2004

DELIVERABLES: First Principles XRR Theory – equations. 2Q 2005

DELIVERABLES: Measurements of ISMT artifacts with traceable XRR instrument. 2Q 2005

DELIVERABLES: Report comparison of measurement results from ISMT and NIST instruments on same artifacts. 2Q 2005

ACCOMPLISHMENTS

The CDPBD has recently been moved to our new equipment space in the Advanced Measurements Laboratory. Measurements last year in our prior lab determined that high accuracy angle control would require the temperature stability of $\pm 0.01^\circ\text{C}$ provided in our new facility. Preliminary measurements and calibration of the system will take place this fall. The first year progress will consist of system calibration, preliminary XRR modeling theory development, and measurement comparisons between same/similar samples on both conventional and NIST traceable XRR systems.

COLLABORATIONS

ISMT, Metrology – P.Y. Hung & Alain Diebold

PTB, Precision Metrology – Peter Thomsen-Schmidt

Bede Scientific Inc. – Keith Bowen & Matthew Wormington

Bruker AXS – Arnt Kern & Alan Coelho

RECENT PUBLICATIONS AND PRESENTATIONS

J. P. Cline and S. T. Mixture, “Alignment & Standards” – workshop at Denver X-Ray Conference, Denver, CO, August, 2003.

D. Windover and J. P. Cline “Goniometer angle calibration for traceability using the method of circle closure” – poster at Denver X-Ray Conference, Denver, CO, August, 2003.

D. Windover and J. P. Cline, “Calibration standards for X-ray metrology systems using a traceable high-resolution diffractometer” – poster at American Vacuum Society, Baltimore, MD, November, 2003.



ELECTRON MICROSCOPE TOMOGRAPHY OF ELECTRONIC MATERIALS

GOALS

Enable the use of three-dimensional imaging for thick samples using commercial scanning transmission electron microscopes (STEM). Typical samples include porous low- κ dielectrics, two-layer interconnect samples, and photonic band gap materials.

CUSTOMER NEEDS

The NTRS/ITRS has recognized the need for three-dimensional imaging of interconnects for several years. In this study, our principle objective is to determine the morphology of pores in low- κ dielectric material. Two aspects of the pore distribution are critical: (a) the largest pores may lead to failure of the dielectric (*e.g.*, short circuits), and (b) the connectivity of the pores is important to understand the transport of chemicals during the fabrication of the inter-connect.

The potential solutions for interconnect are discussed in the 2003 International Technology Roadmap for Semiconductors on pages 13 and 26 of the Interconnect Section. "Two new measurement needs [include] the pore size distribution in porous low-k materials."

TECHNICAL STRATEGY

1. First, we will upgrade an existing commercial transmission electron microscope to be able to obtain high angle STEM images with a full quantitative understanding of the input and output signals. Noise reduction is also a key issue.
2. In parallel, we will develop theoretical and computational expertise for the understanding of STEM signals associated with multiple scattering of electrons.
3. We will obtain a tilt series and perform a tomographic — analysis of a photonic band gap system an artificially periodic polymer structure.
4. We will perform a similar analysis on a low- κ dielectric material.

DELIVERABLES: Tomographic study of photonic band gap material. 3Q 2004

Three-dimensional images of a photolithographically patterned polymer photonic band gap

material will be obtained after the STEM is upgraded.

DELIVERABLES: Tomographic study of a low- κ dielectric material. 4Q 2004

The porous low- κ dielectric will pose more of a challenge, particularly for alignment, because of its random nature. Hence, it will be studied second.

ACCOMPLISHMENTS

- To date, we demonstrated the ability to obtain three-dimensional information using a scanning confocal transmission electron microscope on integrated interconnect samples several micrometers (Frigo, Levine, and Zaluzec, 2002) as well as the ability to obtain three-dimensional information on integrated circuit interconnect samples using a commercial scanning transmission electron microscope (Levine *et al.*, 2003).
- We simulated the tomographic reconstruction using transmission electron microscopy of an 8-micrometer square sample of photonic band-gap material, see Fig. 1 (Levine, 2003). This represents an order of magnitude increase in sample size compared to all TEM-based reconstructions

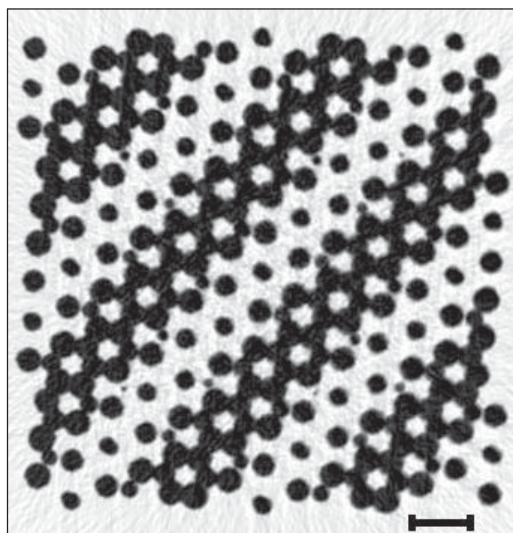


Figure 1. Tomographic reconstruction of a slice through a photonic band gap material from simulated scanning transmission electron microscope data. The scale bar is 1 micrometer, which also corresponds to the typical size of the largest samples used in TEM tomography in the scientific literature.

Technical Contacts:

Z. H. Levine
J. H. Scott

in the scientific literature (to the best of our knowledge).

COLLABORATIONS

International Sematech, Brendan Foran, preparation of low- κ samples, electron microscopy.

Lucent Technologies, Shu Yang; preparation of photonic band gap material.

RECENT PUBLICATIONS

S, Frigo, Z. H. Levine, and N. J. Zaluzec., "Submicron imaging of buried integrated circuit structures using a scanning confocal electron microscope," *Appl. Phys. Lett.* **81**, 2112 (2002).

Z. H. Levine, "Tomography in the Multiple Scattering Regime of the Scanning Transmission Electron Microscope," *Appl. Phys. Lett.* **82**, 3943 (2003).

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HIGH RESOLUTION MICROCALORIMETER X-RAY SPECTROMETER FOR CHEMICAL ANALYSIS

GOALS

We will develop new generations of X-ray spectroscopy tools to meet the materials analysis needs of the semiconductor manufacturing industry. Energy-Dispersive Spectrometers (EDS) based on microcalorimeters have the ability to detect photons with high energy resolution and near-unity quantum efficiency. Using these tools, a wide range of materials analysis problems can be solved. In semiconductor manufacturing, improved X-ray materials analysis is needed to identify nanoscale contaminant particles on wafers and to analyze very thin layers of materials and minor constituents. Microcalorimeter EDS improves the spectral resolution by one to two orders of magnitude compared to the semiconductor Si-EDS, the existing industry standard. Such improved resolution combined with energy dispersive operation makes possible direct spectral separation of most overlapping peaks often encountered with Si-EDS in complex multi-element systems. The improved resolution of the microcalorimeter EDS also increases the peak-to-background ratio. Peak shape and shift can be studied to reveal chemical state information.

Developing arrays of X-ray microcalorimeters will enable the acquisition of high statistics spectra in reduced time, improving the efficiency and statistical quality of existing materials analysis applications. Further, large-format arrays (up to 1,000 pixels) will make it possible to chemically analyze smaller features and trace constituents, and to track rapidly evolving X-ray spectra for in-process and process-stream monitoring.

The microcalorimeter EDS detector invented at NIST consists of a superconducting thermometer (a superconducting transition-edge sensor (TES)) and an X-ray absorber fabricated on a micromachined Si_3N_4 membrane, and cooled to cryogenic temperatures (0.1 K). When X-rays are absorbed in the detector, the resulting heat pulse in the microcalorimeter is measured by the TES thermometer. The change in the temperature of the thermometer is measured by a superconducting quantum interference device (SQUID) amplifier. The temperature pulse height gives a measurement of the energy of the X-ray photon one to two orders of magnitude more sensitive than

Si-EDS. The detector is cooled to 0.1 K by a compact adiabatic demagnetization refrigerator.

CUSTOMER NEEDS

Improved X-ray detector technology has been cited by SEMATECH's Analytical Laboratory Managers Working Group (ALMWG, now ALMC) as one of the most important metrology needs for the semiconductor industry. In the International Technology Roadmap for Semiconductors, improved X-ray detector technology is listed as a key capability that addresses analysis requirements for small particles and defects. The transition-edge sensor (TES) microcalorimeter X-ray detector developed at NIST has been identified as a primary means of realizing these detector advances, which will greatly improve in-line and off-line metrology tools that currently use semiconductor energy-dispersive spectrometers (EDS). At present, these metrology tools fail to provide fast and unambiguous analysis for particles less than approximately 0.1 μm to 0.3 μm in diameter. Improved EDS detectors such as the TES microcalorimeter are necessary to extend the capabilities of existing SEM-based instruments to meet the analytical requirements for future technology generations. With continued development, microcalorimeter EDS should be able to meet both the near-term and the longer-term requirements of the semiconductor industry for improved particle analysis.

Promising new technology such as high energy resolution X-ray detectors must be rapidly commercialized. Prototype microcalorimeter energy dispersive spectrometers (EDS) and superconducting tunnel junction techniques have X-ray energy resolution capable of separating overlapping peaks and providing chemical information. These advances over traditional EDS and some wavelength dispersive spectrometers can enable particle and defect analysis on SEMs located in the clean room. 2001 International Technology Roadmap for Semiconductors

TECHNICAL STRATEGY

1. The usefulness of single-pixel X-ray microcalorimeter EDS in materials analysis has now been well established in a variety of demonstrations. Small arrays of X-ray microcalorimeters are being

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C. D. Reintsema
J. N. Ullom
L. R. Vale

"[T]his type of resolution, very simply, was something that I thought was truly, truly a dramatic advance. And I really would like to encourage the people working on this at NIST and the equipment industry to get this into commercialization as soon as they possibly can."

*Mark Melliar-Smith,
Former President and
Chief Executive Officer
of SEMATECH*

tested, and the development of technologies for large-format arrays is in process. To meet the needs of the semiconductor industry, it is necessary to make both single-pixel and array microcalorimeter systems more widely available. In addition to microcalorimeters, the system requires novel superconducting electronics to instrument the detectors, compact adiabatic demagnetization refrigerators to simplify cooling to milliKelvin operating temperatures, and custom room-temperature electronics and software to process the output signals. Our goal is to develop new generations of detector systems, to transfer them to the Chemical Science and Technology Laboratory (CSTL) in NIST Gaithersburg for collaborative use in studying problems of interest to the industry, and to work with other partners in disseminating the technology (Fig. 1).



Figure 1. Single-pixel NIST X-ray microcalorimeter system on a scanning-electron microscope. The system was developed in the Electronics and Electrical Engineering Laboratory (EEEL) at NIST, Boulder, and transferred to the Chemical Science and Technology Laboratory (CSTL) at NIST Gaithersburg to be used to study problems of interest to the semiconductor industry.

DELIVERABLES: Provide continued support and upgrades for the single-pixel microcalorimeter system transferred to CSTL. Prepare for the eventual transfer of an array microcalorimeter system. Collaborate with CSTL on using the microcalorimeter to study problems of interest to the semiconductor industry. 3Q 2004

2. For many semiconductor materials analysis problems, further improvements in energy resolution (beyond that already demonstrated with these detectors (Fig. 2)) are not as important as an increase in the maximum count rate and collection area. Both the collection area and count rate can be improved by the implementation of multipixel arrays of detectors (see Fig. 3 and Fig. 4).

Small arrays of X-ray microcalorimeters are now being tested. The performance of these arrays should be similar to that of earlier, successful single pixels.

DELIVERABLES: Achieve high-resolution operation of a close-packed X-ray microcalorimeter array to demonstrate the increase in collection area and count rate achievable with arrays. 4Q 2004

3. One of the barriers to widespread dissemination of X-ray microcalorimeter instruments is the complexity and cost of the adiabatic demagnetization refrigerator used to cool to 100 mK. The development of an on-chip solid-state microrefrigerator based on superconducting tunnel junctions to cool from 300 mK to 100 mK would greatly simplify the cryogenic system needed for microcalorimeter EDS. Adiabatic demagnetization refrigerators could be replaced by small, simple, and inexpensive ^3He systems, which cool to 300 mK, coupled to the solid-state tunnel-junction refrigerator cooling to 100 mK.

DELIVERABLES: Demonstrate the cooling of an electrically-separate piece of thin-film electronics using a tunnel-junction refrigerator that could be coupled to a simple ^3He refrigerator. 2Q 2004

4. The operation of microcalorimeter arrays requires multiplexed SQUID readout. A time-domain SQUID multiplexer has previously been demonstrated. The integration of this multiplexer with X-ray microcalorimeters is a crucial step towards the deployment of large sensor arrays. The operation of such an integrated system under X-ray illumination will allow its capabilities to be measured and routes to improvement to be determined.

DELIVERABLES: Demonstrate multiplexed operation of microcalorimeters under X-ray illumination. Characterize multiplexer performance and design next-generation system. 3Q 2004

ACCOMPLISHMENTS

- We continue to support the microcalorimeter system installed previously on a CSTL scanning electron microscope in Gaithersburg. We are collaborating with CSTL researchers on improvements to the stability and ease-of-use of the system. In particular, we developed improved magnetic shielding for the microcalorimeter which greatly increases reproducibility.

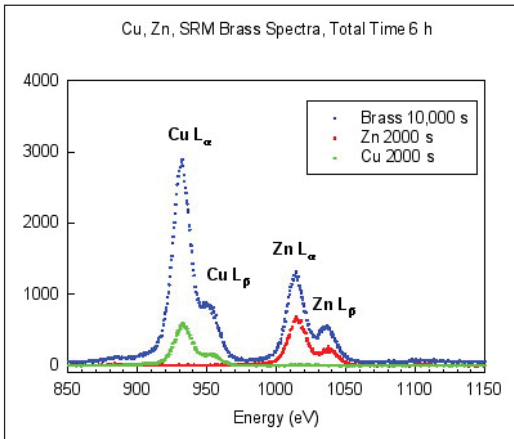


Figure 2. Spectra of Cu, Zn, and NIST SRM brass taken on JEOL JXA-840 Microscope at NIST, Gaithersburg, Maryland by T. Jach, D. Newbury, and J. Small. No recalibration was required over ~6 hrs of counting time.

■ We acquired high-resolution X-ray spectra from multiplexed microcalorimeter pixels in a close-packed array. The measurements required several upgrades to our measurement station: the installation of an internal X-ray source, line-of-sight access to the sensors through our optical and magnetic shielding, infrared blocking filters, a micromachined collimator, and an electromechanical shutter. The measurements successfully demonstrated the capabilities of both the detector arrays and the SQUID multiplexer. In a 4 pixel multiplexed measurement, we demonstrated FWHM energy resolutions of ~6.9 eV at 5.9 keV, only 0.4 eV worse than when unmultiplexed. The experiments validated our models of multiplexer performance which predict that a realistic future system can be scaled to 32 pixels. A faster SQUID multiplexer chip has been designed for our next series of multiplexer tests.

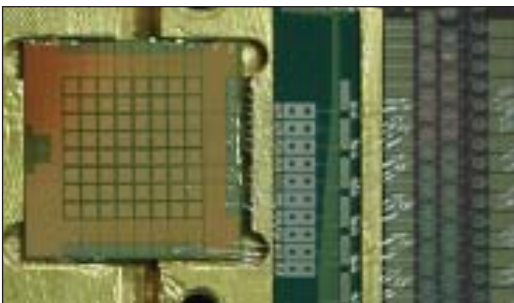


Figure 3. Photograph of an 8x8 array of microcalorimeters. Each microcalorimeter has a 1.5- μm -thick Bi absorber. The middle chip is a filter chip. The chip on the right is a SQUID multiplexer. We have demonstrated high-resolution multiplexed operation of 4 sensors in the middle of the array under illumination by 5.9 keV X-rays.

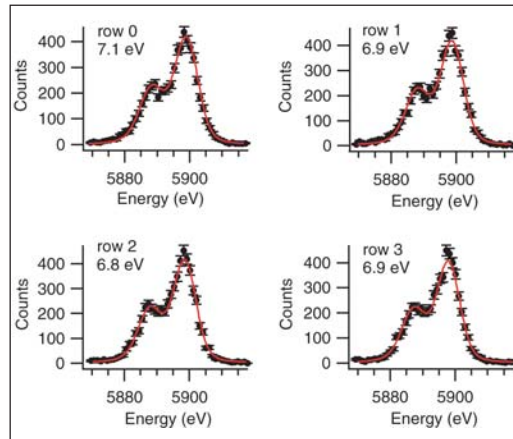


Figure 4. X-ray spectra from 4 pixels in the array shown above. Signals from all 4 pixels were compressed into a single output channel using a SQUID multiplexer. The FWHM resolution of the sensors was ~6.9 eV for 5.9 keV X-rays.

■ We have continued work on an on-chip solid-state refrigerator to cool X-ray microcalorimeters from 300 mK to 100 mK (see Fig. 5). If successful, this refrigerator could greatly simplify the cryogenic system needed for microcalorimeter EDS. Adiabatic demagnetization refrigerators could be replaced by small and inexpensive ^3He systems coupled to the solid-state refrigerator. The device is a superconducting analog of a Peltier cooler. Cooling is produced in the devices by the tunneling of electrons through normal-insulator-superconductor junctions. We have previously demonstrated refrigerators able to cool themselves from 260 to 130 mK with cooling powers well matched to microcalorimeter X-ray sensors. We have recently demonstrated refrigerators able to cool both the electrons and phonons of electrically separate pieces of thin-film electronics, such as a X-ray microcalorimeter. The solid-state refrigerator is fabricated on a silicon wafer using conventional thin-film and photolithographic techniques, has no moving parts, and operates continuously. Early prototypes produced 35 mK of cooling and significant increases are expected later this year. The work was featured on the cover of both *Applied Physics Letters* and *Physics Today*.

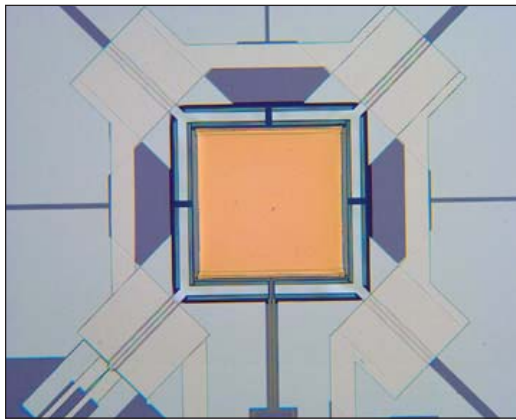


Figure 5. Micrograph of solid-state refrigerator. A TES X-ray detector (orange square) is surrounded by four pairs of normal-insulator-superconductor tunnel junctions. The junctions cool wishbone shaped fingers which surround the TES. The TES has dimensions of $400\ \mu\text{m} \times 400\ \mu\text{m}$.

- The NIST microcalorimeter EDS holds the world record for energy resolution for an EDS X-ray detector of $2.0\ \text{eV}$ at $1500\ \text{eV}$ (see Fig. 6), which is over 30 times better than the best high resolution semiconductor-based detectors currently available. This energy resolution was measured using a glass prepared by Dale Newbury of NIST to use as a test standard for EDS.

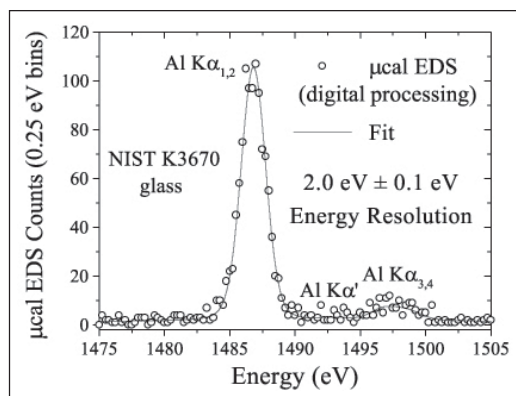


Figure 6. The Al-K α region of a microcalorimeter EDS spectrum of the multi-element NIST K3670 glass. The acquired spectrum is shown as well as a weighted least-squares fit of the Al K α and satellite lines convolved with a Gaussian instrument response, yielding an energy resolution of $2.0\ \text{eV} \pm 0.1\ \text{eV}$ FWHM.

- We created a chemical shift map showing the chemical bonding state of Al in a sample containing both Al and Al_2O_3 . An aluminum film was deposited on part of a sapphire substrate (see Fig. 7). A microcalorimeter EDS was used to measure the

X-ray spectrum as the electron beam was rastered to form the SEM image. The Al X-ray line position was shifted by a small amount (about $0.2\ \text{eV}$) in the regions containing Al_2O_3 as compared to the regions containing elemental Al. The high energy resolution of the microcalorimeter allowed the shift to be measured, resulting in the false-color image below. The map clearly demonstrates that microcalorimeter EDS can be used to discriminate the chemical bonding state using shifts in the positions of X-ray lines. The result also highlights the need for large-format arrays to increase the data-collection rate. The image shown here was acquired over several hours. Images such as this could be acquired much more quickly and with much sharper position resolution using an array microcalorimeter.

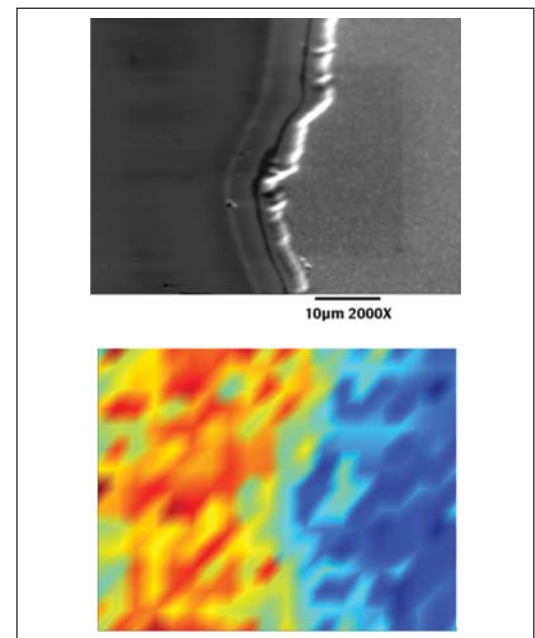


Figure 7. SEM photo (top) of an aluminum film partially covering a sapphire substrate and a false-color map (bottom) of the shift in the mean X-ray energy of the Al K α peak taken using a microcalorimeter EDS system. The shift in energy is due to the chemical bonding of the aluminum with the oxygen. The average energy shift is $\sim 0.2\ \text{eV}$.

COLLABORATIONS

Chemical Science and Technology Laboratory, NIST, Gaithersburg, Terry Jach, Lance King, Dale Newbury, John Small, and Eric Steel, the development of microcalorimeter EDS systems.

RECENT PUBLICATIONS

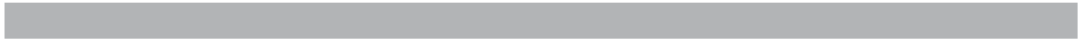
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DEVICE DESIGN AND CHARACTERIZATION PROGRAM

As microelectronics pushes into the nanoelectronics regime traditional CMOS reaches fundamental limits; new device structures such as FINFETs, fully depleted and partially depleted silicon-on-insulator, various alloys such as silicon-germanium and silicon-germanium-carbon, strained layers and other *exotica* such as carbon nanotube and molectronic device structures need to be characterized. To this end we have initiated a new program, “Device Design and Characterization.” One project that has to be highlighted because it will impact all the projects in the portfolio over time is the Advanced Measurements Nanofabrication Facility Support project. With the completion of the Advanced Measurements Laboratory on the Gaithersburg campus we have begun to populate a cleanroom facility with advanced processing and metrology equipment suitable for advancing into the nanotechnology era.



DEVICE CHARACTERIZATION AND RELIABILITY

GOALS

The goal of the Advanced Device Characterization and Reliability Project is to develop the metrology that will help enable near-term and future silicon technologies (such as Si-based quantum devices) to improve, supplement, or supplant conventional Complementary Metal Oxide Semiconductor (CMOS) devices. This involves determining the critical metrology needs for these exploratory technologies.

Near term goals are to provide electrical and reliability measurement techniques, data, physical models, and fundamental understanding for ultra-thin silicon dioxide and alternate (high- κ) gate dielectrics in advanced MOS devices. A specific focus is to increase the understanding of the relationship between the gate dielectric material/interface properties and device electrical and reliability measurements.

The Si microelectronics community is currently faced with major materials challenges to further scaling. The gate stack (*i.e.*, the gate dielectric, SiO₂, and the gate electrode, doped polycrystalline Si), which has served the industry for 35 years, must now be entirely replaced with one having a higher capacitance and lower power dissipation. Gate dielectrics having higher dielectric constants than SiO₂ will replace SiO₂, and metal electrodes will replace polycrystalline silicon. The enormous complexity of selecting the proper combinations of new gate dielectrics and gate metal electrodes can only be attacked using combinatorial materials methodologies. Therefore, we will be implementing this technology.

Further term targeted goals are to develop the precise metrology and characterization methods required for the systematic characterization of Si-based nanoelectronic devices.

CUSTOMER NEEDS

The MOSFET (Metal Oxide Field Effect Transistor), which is the current basis of ULSI (Ultra-Large-Scale Integration) circuits, is beginning to show fundamental limits associated with the laws of quantum mechanics and the limitations of fabrication techniques. The evolving decrease of the gate dielectric film thickness to an oxide-equivalent value of 2 nm is identified as a critical front-end technology issue in the Semiconductor Industry Association's (SIA's) International Tech-

nology Roadmap for Semiconductors (ITRS) with effective thickness values of 1.4 nm, or less, being projected in 2004, dropping to 0.8 nm or less by 2010. For effective gate dielectric thicknesses below ~ 2.0 nm, SiO₂ must be replaced, initially by oxynitrides or oxide/nitride stacks, and then by either metal-oxides or compounds such as metal-silicates or metal silicates.

Due to increased power consumption, intrinsic device reliability and circuit instabilities associated with SiO₂ of this thickness, a high permittivity gate dielectric (*e.g.*, Si₃N₄, HfSi_xO_y, ZrO₂) with low leakage current and at least equivalent capacitance, performance, and reliability will be required. The physics of failure and traditional reliability testing techniques must be reexamined for ultra-thin gate oxides that exhibit excessive tunneling currents and soft breakdown. Electrical characterization of Metal Oxide Semiconductor (MOS) capacitors and Field Effect Transistors (FET) has historically been used to determine device and gate dielectric properties such as insulator thickness, defect densities, mobility, substrate doping, bandgap, and reliability. Electrical and reliability characterization methodologies need to be developed and enhanced to address issues associated with both ultra-thin SiO₂ and alternate dielectrics including large leakage currents, quantum effects, and thickness dependent properties. As compared to SiO₂, very little is known about the physical or electrical properties of high dielectric constant gate dielectrics in MOS devices. The use of these films in CMOS technology requires a fundamental understanding of the relationship between the gate dielectric material/interface and device electrical and reliability measurements.

There are no known solutions for a variety of technological requirements including gate dielectric, gate leakage, and junction depth for the continual scaling of CMOS technologies. Therefore, it is expected that entirely new device structures and computational paradigms will be required to augment and/or replace standard planar CMOS devices. Si-based quantum electronic devices show promise to extend traditional scaling laws for increased computational performance beyond the limits of conventional CMOS. Research and development for silicon-based nanoelectronics (*e.g.*, wrap-around FETs, Si-based RTDs [resonant tunneling diodes], silicon quantum dots) for

Technical Contact:

J. Suehle
E. Vogel
M. Green

Staff-Years (FY 2003)

2 professionals
1 technician
3 guest researchers

the post-CMOS era are currently of interest due to their inherent compatibility with CMOS technology.

The project is concerned with fundamental research related to possible future devices that will replace or augment standard CMOS technology. In order to ensure that our research is technically relevant, we plan to align ourselves with research described by the Microelectronics Advanced Research Corporation (MARCO), alluded to in the SIA's Roadmap and other similar semiconductor industry organizations and documents.

The industry for these emerging nanoelectronic devices will require reference data, standards, precision measurement protocols, and standardized test structures and associated measurement protocols to develop into a viable commercial technology. The ultimate objective of this project is to provide the measurement infrastructure to aid this development. Through strong ties with industry leaders and cutting-edge researchers, we are accelerating the pace of our program and focusing our research on the most relevant technologies.

TECHNICAL STRATEGY

There are three main focus areas for this project:

- Developing electrical and reliability characterization techniques for ultra-thin SiO₂ and high dielectric constant gate dielectrics.
- Develop combinatorial (fast, local) measurement techniques to measure appropriate electrical properties on gate stacks consisting of new gate dielectric and gate metal electrode materials.
- Developing metrology for characterizing Si-based quantum electronics and other advanced device structures.

The first focus area is to develop robust electrical characterization techniques and methodologies to characterize charge trapping kinetics, V_t instability, defect generation rates and time-dependent dielectric breakdown (TDDB) for both patterned device samples and blanket films obtained from our collaborators. Many issues such as tunnel/leakage current and spatially dependent properties associated with metal oxide and silicate dielectrics are also present in ultra-thin oxide and oxide-nitride stacked dielectrics. Therefore, many of the characterization schemes will first be developed on the simpler ultra-thin oxide and oxide-nitride dielectrics and then be applied to the

metal oxide and silicate dielectrics for a variety of high-κ samples subject to different deposition and gate electrode processes. Studies will be conducted to determine the effect of multiple interfaces on stress-induced defect generation and wear-out. It will be determined what technique or combination of techniques provides the most consistent results for all films. The electrical results will be used to validate simulation models and compared to studies from various analytical materials characterization.

The Si-nanotechnology effort will focus on physical and electrical metrology of the basic building blocks of silicon quantum electronic devices (*e.g.*, quantum layers, wires, and dots of silicon surrounded by silicon dioxide). By identifying and addressing the critical metrology issues associated with these basic building blocks, the basis of metrology for future Si-based ULSI nanotechnology will be defined.

A major goal is to fabricate quantum dots and one-dimensional wires with controllable size. These will be used to establish the relationship between the key fabrication conditions, physical properties (such as the geometry of the quantum-dot and the tunneling barrier), and final electrical properties of these floating silicon devices (*i.e.*, metal-oxide-silicon-oxide-silicon [MOSOS] devices). Production of MOSOS capacitor structures is an intermediate step en route to this end goal. This research will provide the information necessary to help identify and address the necessary electrical and physical characterization methodologies.

DELIVERABLES: Experimental results of charge stability and trapping in HfO₂ films including defect generation rates due to constant voltage stress. 3Q 2004

DELIVERABLES: Conduct gate polarity dependent studies of the long-term wear-out and breakdown of advanced high-κ dielectrics. 3Q 2004

DELIVERABLES: Complete comparison study of various electrical techniques to determine interface trap spectra for a variety of control samples by 1Q 2005.

DELIVERABLES: Provide test technique(s) and analysis to quantify electrical trap densities at multiple interface stacks by 2Q 2005.

DELIVERABLES: Provide correlation study of electrical parameters to results from materials analysis on select number of samples by 3Q 2004.

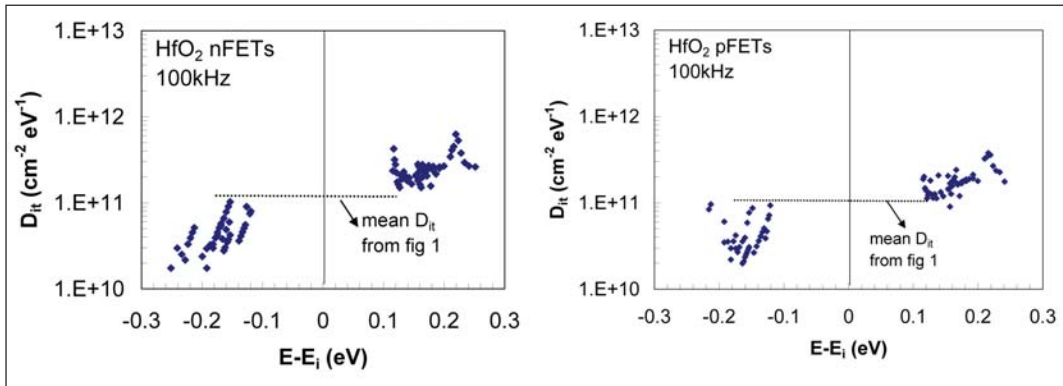


Figure 1. Energy distribution of interface traps as determined by rise/fall time dependence of charge pumping currents for HfO_2 -gated MOSFETs: (left plot) n-MOSFET, (right plot) p-MOSFET.

DELIVERABLES: Correlation of the physical properties of self-assembled quantum dots with the processing parameters used to fabricate them. 4Q 2004

DELIVERABLES: Report results of electrical and physical characterization of a functioning Si-based nanoelectronic device such as a Si-based SET or a one-dimensional Si-FET. 4Q 2004

DELIVERABLES: Identify suitable metal gate electrode compositions, based on barrier height and thermal stability criteria, for use with state-of-the-art gate dielectrics (e.g., Hf-Si-O-N). 2Q 2005

ACCOMPLISHMENTS

■ *Energy Dependence of Interface traps in HfO_2 Characterized.* A series of experiments were conducted to characterize the energy dependence of interface trap density in *n* and *p*-channel HfO_2 FETs supplied by IBM. The study demonstrated that the mobility reduction observed in *n*-channel devices is due to positions of interface traps in the upper half of the Si energy band (see Fig. 1).

New JEDEC standard, JESD-92, is published. The standard describes several techniques that can be used to detect soft breakdown in ultra-thin gate oxides where detection can be difficult. The standard also includes guidelines for designing test structures and data analysis procedures.

Mechanistic Study of Progressive Breakdown in Small Area Ultra-Thin Gate Oxides. A study was completed to investigate two competing post soft breakdown modes observed in ultra-thin gate oxides. One breakdown mode features a conducting filament that is stable until hard breakdown occurs and a second mode features a filament that continually degrades with time. The acceleration

factors are different for each mode, indicating different physical mechanisms are involved in the evolution and formation of the final hard breakdown event. Unstable filaments that result from the first soft breakdown progressively degrade and change physical structure until their leakage current becomes unacceptably large. A set of voltage and temperature acceleration parameters different from oxide wear-out are necessary to project the leakage current with time.

Prototypical Multiple-Quantum-Dot-Island Floating Body Devices. Processing parameters have been established to reproducibly control the size distribution, concentration, and shape of silicon quantum dots formed using LPCVD (Low Pressure Chemical Vapor Deposition). Two methodologies for forming silicon quantum dots have been explored. The first is by direct deposition of polycrystalline quantum dots using LPCVD at short deposition times. The second is by deposition of thin amorphous silicon layers using LPCVD followed by annealing. Quantum-dot island floating body capacitors and transistors will be made by using these quantum dot formation techniques (Fig. 2, 3, and 4). A simple two-level capacitor mask set and a four-level mask set to fabricate field-oxide isolated, polysilicon gated, field effect transistors (FETs) have been designed and purchased. Working polysilicon gated capacitors (without the floating quantum dots) have been fabricated with gate oxide thicknesses of approximately 5 nm, and processes have been developed to form gate oxides with thicknesses of approximately 2 nm.

Si-nanowire transistor structures fabricated. Quasi-one-dimensional Si-wires (~100 nm by ~30 nm in cross-section) have been fabricated from ultrathin-body SOI (silicon on insulator) substrates

by utilizing electron-beam lithography and reactive ion etching. To form nanowire transistor structures (Fig. 5), large area source/drain regions were doped and contacted, and the wires are covered by a thin (~3 nm) gate dielectric and a poly-Si gate

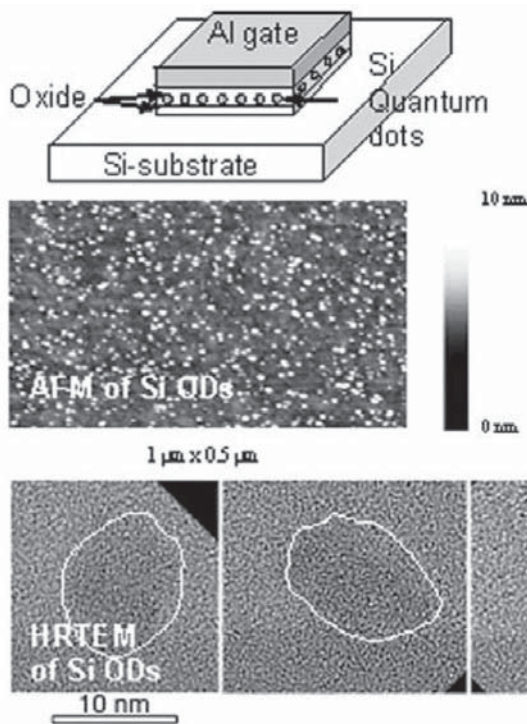


Figure 2. Schematic representation and HRTEM micrograph of quantum dot floating island capacitor.

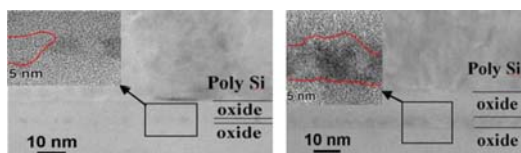


Figure 3. Cross sectional TEM image of nanocrystalline silicon which formed after oxidation of amorphous silicon layer. Original thickness of amorphous silicon layer was (left image) ~ 8 nm (right image) ~ 15 nm.

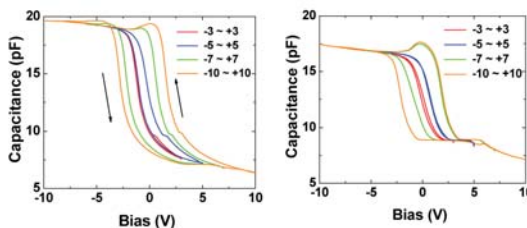


Figure 4. C-V characterization of MOS capacitors corresponding to TEM images in Fig. 3 (left image) and Fig. 2 (right image) respectively.

dielectric. This structure is nominally the same as devices typically referred to as FINFETs or tri-gate FETs.

STANDARDS COMMITTEE PARTICIPATION

JEDEC JC14.2 Committee on Wafer-Level Reliability, Dielectric Working Group, Chairman (John S. Suehle).

COLLABORATIONS

Agere Technologies, ultra-thin gate oxide reliability (John S. Suehle)

NIST EEEL Quantum Electrical Metrology Division (817) & NTT: Si-based single electron tunneling devices. (Eric M. Vogel and Curt A. Richter)

NIST Materials Science and Engineering Laboratory (MSEL): The goal is to establish the relationship between key fabrication conditions, physical properties as measured via TEM, SEM, and AFM, and final electrical properties of prototypical Si-based quantum devices.

NIST Precision Engineering Division (821): Exploring Si-based nanoelectronic applications of AFM-directed oxidation for use as a fabrication technique.

IBM, Alternative Gate Dielectrics (Eric M. Vogel)

N.C. State University (oxynitrides, nitrides, ultra-thin SiO₂), alternative gate dielectrics (Eric M. Vogel)

SEMATECH, Alain Diebold, Gate Oxide Metrology Task FEP Z001 (Eric M. Vogel, James R. Ehrstein, Nhan V. Nguyen, and Curt Richter)

Sharp Microelectronics, Dr. John Conley, Characterization of Hafnium-oxide dielectric films, summer 2000 to summer 2003 (James R. Ehrstein and John S. Suehle)

Texas Instruments, electrical and reliability characterization of ultra-thin gate oxides (John S. Suehle and Curt A. Richter)

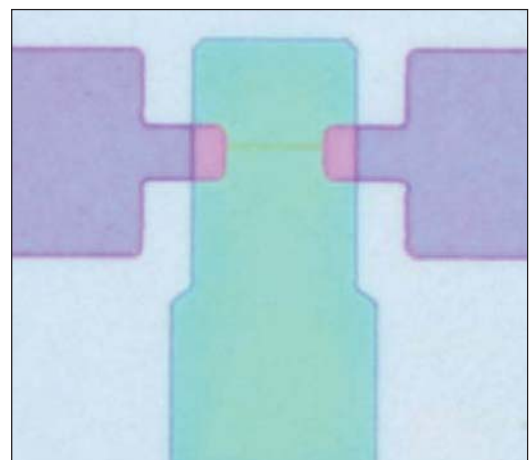


Figure 5. Optical micrograph of Si-nanowire transistor structure.

The Pennsylvania State University, Molecular Electronics (Curt A. Richter and John S. Suehle)

University of Maryland, College Park, ultrathin gate oxide reliability (John S. Suehle and Eric M. Vogel)

NIST Division 837, Dr. L. Richter, Optical characterization of semiconductor interfaces (Curt A. Richter)

NIST Division 837, John Henry Scott, high-resolution TEM studies of molecular test structures (Curt A. Richter)

U. Texas at Austin, Prof. Jack Lee, Optical properties of ZrO_2 and HfO_2 for use as high- κ gate dielectrics (Curt A. Richter and Nhan V. Nguyen)

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Han, J.-P., Vogel, E. M., Gusev, E. P., D'Emic, C., Richter, C.A., Heh, D. W., Suehle, J., "Energy Distribution of Interface Traps in High- κ Gated MOSFETs," 2003 *VLSI Tech. Symp.*

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J. S. Suehle, B. Zhu, Y. Chen, and J. B. Bernstein, "Acceleration Factors and Mechanistic Study of Progressive Breakdown in Small Area Ultra-Thin Gate Oxides," Proc. International Reliability Physics Symposium, vol. 42, p. 95 (2004).

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ADVANCED MEASUREMENTS NANOFABRICATION FACILITY SUPPORT

GOALS

The NIST Advanced Measurement Laboratory (AML) Nanofabrication Facility (NF) will:

- Enable fabrication of prototypical nanoscale test structures, measurement instruments, standard reference materials, electronic devices, MEMS, and bio-devices critical to NIST's Strategic Focus Areas (Nanotechnology, Homeland Security, Healthcare) and the Nation's Nanotechnology Needs
- Provide access to expensive nanofabrication tools, technologies and expertise in a shared-access, shared-cost environment to NIST and its partners
- Foster internal collaboration in Nanotechnology across NIST's Laboratories
- Foster external collaboration in Nanotechnology with NIST's partners.

CUSTOMER NEEDS

To continue to respond to U.S. science and industry's needs for more sophisticated measurements and standards in the face of heightened global competition, NIST is constructing one of the most technologically advanced facilities in the world—the Advanced Measurement Laboratory, or AML. The NIST Nanofabrication Facility (NF) is one of five buildings in the AML at the Gaithersburg, Maryland campus. The AML Nanofabrication Facility will provide researchers at NIST working on a variety of semiconductor and other nanotechnology research the ability to fabricate prototypical nanoscale test structures, measurement instruments, standard reference materials, and electronic devices.

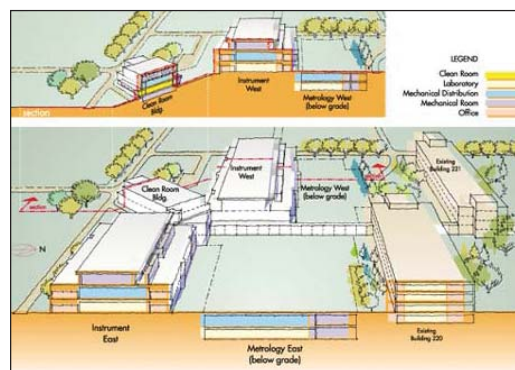
TECHNICAL STRATEGY

The AML contains two above-ground instrument buildings, two completely below-ground metrology buildings, and one class 100 clean room building that will house the NIST AML Nanofabrication Facility. The AML will provide NIST with superior vibration, temperature and humidity control, and air cleanliness. The NIST AML NF has approximately 18,000 sq. ft. of Class 100, raised floor, bay and chase, clean room space. NIST has invested in a complete suite of new equipment (capable of processing 150 mm wa-

fers) that will be installed over the upcoming year. This includes furnaces (two banks of four tubes each), LPCVD (poly, nitride, LTO), rapid thermal annealer, three reactive ion etchers (SF_6/O_2 , Metal, Deep), three metal deposition tools (thermal, e-beam, sputterer), contact lithography (front- and back-side alignment), e-beam lithography, focused ion beam, and numerous monitoring tools (FESEM, spectroscopic ellipsometer, contact profilometer, 4-point probe, microscope with image capture, etc.).

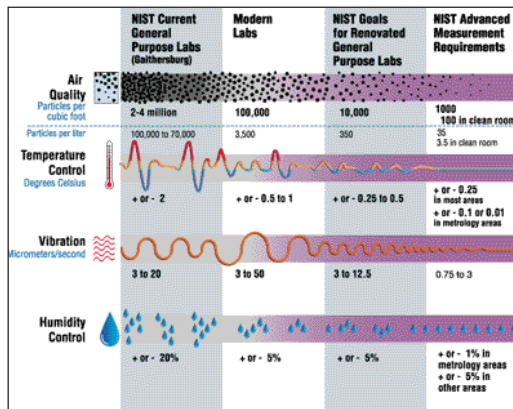
Technical Contacts:

E. M. Vogel
R. Hajdaj



Schematic of the NIST AML.

The NF will be operated as shared access user facility. This means that the staff of NIST and its partners, subject to provisions, training, and user fees, will be permitted to independently operate the equipment. The tools will be operated in a manner such that a wide variety of materials can be processed. The facility will be directed by NIST's Semiconductor Electronics Division. Unlike other NF, the NIST AML NF is unique in that it is located next to the most advanced metrology tools in the world, and its focus will be on fabricating nanoscale structures necessary for metrology and standards in support of the semiconductor industry, nanotechnology, biotechnology, and homeland security.



Building criteria for the NIST AML.

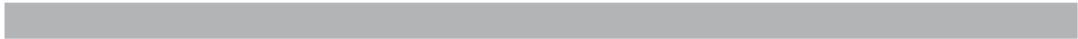
DELIVERABLES: Fit-up of facility and equipment completed by 1Q 2005.

DELIVERABLES: Facility fully operational by 4Q 2005.

SYSTEM DESIGN AND TEST METROLOGY PROGRAM

Lead counts of several thousand per chip and test frequencies in the microwave regime challenge current test methodologies. The addition of new functions to provide system on-chip solution pose additional testing challenges. The overall task is to develop test methodologies to address these new requirements.

Accurate at-speed test methodology of digital integrated circuits is a critical requirement. Traditional methods utilizing IC contact probing technology requires large contact pads incompatible with current IC designs. The development of alternative probing approaches through non-contact and intermittent probing techniques appear very promising. However, to implement these techniques, solving the at-speed test calibration issues is crucial. With the challenges facing designers and the rising costs of development, it is essential to develop accurate testing strategies.



METROLOGY FOR SYSTEM-ON-A-CHIP

GOALS

Develop solutions to key metrology issues confronting the semiconductor System-on-a-Chip (SoC) industry. These include development of measurement methods and standards for characterizing embedded-sensor (ES) Virtual Components (ES-VCs), a critical class of building blocks from which SoCs are developed. The goal of this project is to promote and support the development of hardware and software standards for specifying embedded-sensor (ES) virtual-components (VCs) compatible with the System-on-a-Chip (SoC) integration methodology used for digital IC design.

This NIST effort will enable ES-VCs to be included in SoC CAD libraries and enable integration of ES-VCs with the existing digital VCs used ubiquitously by industry to design large ICs. The methods and standards developed as a result of this work will be essential for the realization of integrated smart, low-cost homeland security and environmental sensor systems.

One focus is on delivering standards to facilitate the incorporation of multi-technology (MT) VCs including MEMS-based VCs into SoCs. The project activities include: multi-technology hardware description language (HDL) model development, VC interface standards, synthesis and scaling standards for ES-VCs compatible with digital methodologies, testing standards and verification standards. The NIST MEMS-based integrated gas-sensing VC will be used as a test bed to demonstrate the viability of these standards. In addition, the demonstration of general purpose gas-sensing VC methodologies will be used to facilitate the adoption of these MT-VCs into new Homeland Security and Industrial applications.

CUSTOMER NEEDS

The driving force in today's semiconductor industry is the need to maintain a rate of improvement of 2x every two years in high-performance components. Historically, these improvements have relied exclusively on advances made in semiconductor miniaturization technology. Achievement of this advancement in circuit and system design techniques is increasingly becoming dependent on integrating multiple technologies into a single chip referred to as System-on-a-Chip (SoC). The design challenges for SoC devices

will be overcome with the use of platform-based design approaches that emphasize design reuse, i.e. the development of ES-VCs that can be used as cost-effective building blocks for SoC devices.

The direct customers for this infrastructure building will be the makers of system design software, companies manufacturing ES-SoCs, and systems designers.

An article entitled "SoC creation requires rules" written by Thomas L. Anderson, EE Times states "While EDA vendors may provide detailed instructions and methodology guides for their specific tools, there has not been much industry activity in establishing more general rules, guidelines and best practices".

TECHNICAL STRATEGY

1. To successfully develop ES-VCs for SoC design methodology, the first step in this multi-step process is to develop the ability to produce the ES-VC devices via a standard CMOS compatible process. To demonstrate this capability we have chosen a MEMS microhotplate based ES-VC, including operational amplifiers, decoders, and analog-to-digital converter (ADC) to process the data.

DELIVERABLES: Develop post processing technology that will enable the microhotplate to scale to standard submicron mixed signal IC foundry processes. 2Q 2005

2. The second step in making the ES-VC is to make it compatible with the digital SoC design methodology. This approach will require ES-VC to have digital interface circuitry and to have DFT and BIST functionality features. To facilitate this approach we will develop methodologies and standards for adding digital shells to ES-VCs and demonstrate them on the gas sensor VC described above.

DELIVERABLES: Develop methodologies for designing digital interface shells, DFT and BIST functionality for ES-VCs and demonstrate their viability via our micro hotplate gas sensor technology. 3Q 2004

3. The predominant design approach used by industry for SoC devices is top-down design. This requires that high-level HDL models exist for the VCs that are candidates for use in any particular system of interest. Compared to those for digital

Technical Contacts:

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M. Y. Afridi

"NIST Microhotplate may help search for extraterrestrial life."

Science Daily

"The NIST-developed microhotplate gas sensor technology is the future for homeland security and military applications of toxic gas and trace explosive detection."

*Ernesto A. Corte,
Vice President,
Thermo Electron Corporation*

VCS, the methodology and standards for developing high-level models for ES-VCS is at best poorly developed. To address this need, high-level models are being developed for ES-VCS using Analog and Digital Hardware Description Languages, and methodologies are being developed to validate the models.

DELIVERABLES: Develop methodologies and standards for developing high-level models for ES-VCS and demonstrate their viability via our micro hotplate gas sensor technology. 4Q 2006

4. After the high-level simulation of the system in the top-down design process is successfully completed, the next step is to synthesize the individual VCs. Compared to those for digital VCs, the methodology and standards for ES-VC synthesis is at best poorly developed. To address the need for synthesizing ES-VCS, we are developing standards and metrologies for a non-digital synthesis like process that is compatible with digital synthesis. This process is based upon libraries of existing designs and the device design equations.

DELIVERABLES: Develop Gas Sensor SoC system architecture utilizing the ES-VC and synthesize system design demonstrating viability of ES-SoC methodology. 4Q 2005

5. The testability of ES-VCS represents another significant challenge since standards and methodologies for non-digital circuits do not exist. The most promising approach to address testability is to use Built-In-Self-Test (BIST) techniques. To facilitate this approach we will develop methodologies and standards for adding BIST to ES-VCS and interface them via the digital shell.

DELIVERABLES: Develop test bed for evaluation of gas sensor VC built-in self test function demonstrating DFT requirements for ES-SoC design methodology. 1Q 2005

ACCOMPLISHMENTS

- A monolithic micro-gas-sensor system was designed and fabricated in a standard CMOS process (see Fig. 1). The gas-sensor system incorporated an array of four micro hotplate-based gas-sensing structures. The system utilized a thin film of tin oxide (SnO_2) as a sensing material. The interface circuitry on the chip has digital decoders to select each element of the sensing array and an operational amplifier to monitor the change in conductance of the film. The chip is post-processed to create micro hotplates using bulk

micro-machining techniques. Detection of gas concentrations in the 100 parts-per-billion range was achieved. This represents a factor of 100 improvement in sensitivity compared to existing MEMS-based micro-hotplate gas sensors.

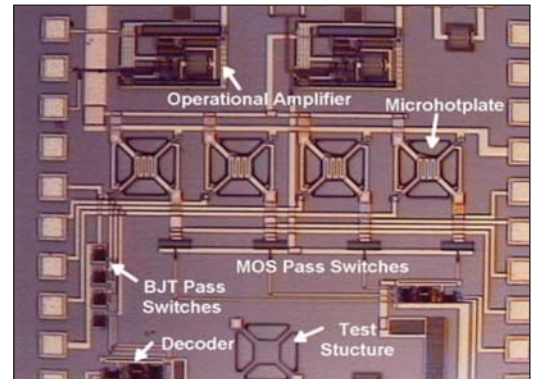


Figure 1. Micrograph of gas-sensor system to be used as demonstration vehicle.

- A monolithic CMOS four element gas sensor VC was designed and submitted for fabrication (see Fig. 2). The design includes both analog and digital integrated circuits. The digital part of the circuit has an 8-bit analog-to-digital converter (ADC). The objective of the design is to make it compatible with the SoC design methodology.

- The four element gas sensor VC was electrically characterized. The performance of the 8-bit ADC superseded the gas sensor VC design requirements.

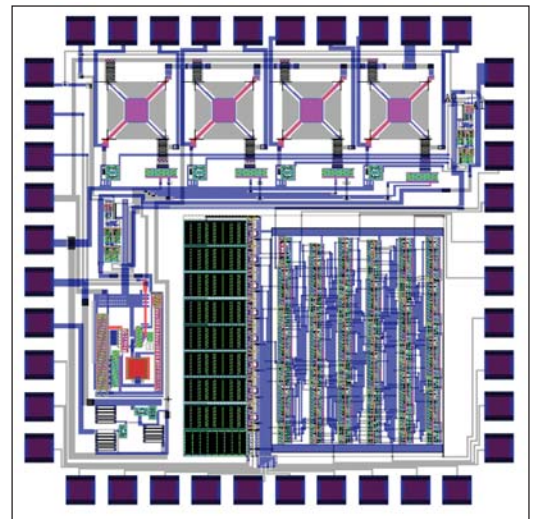


Figure 2. Layout of the four element gas sensor VC with analog-to-digital control.

- An initial design of a four-element gas sensor VC with electrostatic discharge (ESD) protection was implemented in 1.5 micron standard CMOS technology (see Fig. 3). The electrical characterization of the gas sensor VC showed leakage problems. The chip was re-designed and submitted for fabrication.
- New microhotplate test structures were designed and fabricated to improve thermal efficiency and their feasibility to be fabricated in the CMOS sub-micron technology (see Fig. 4).

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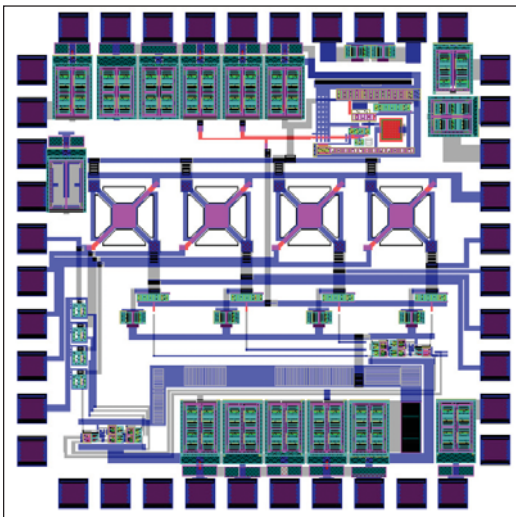


Figure 3. Layout of the four element gas sensor VC with electrostatic discharge (EDS) protection circuitry.

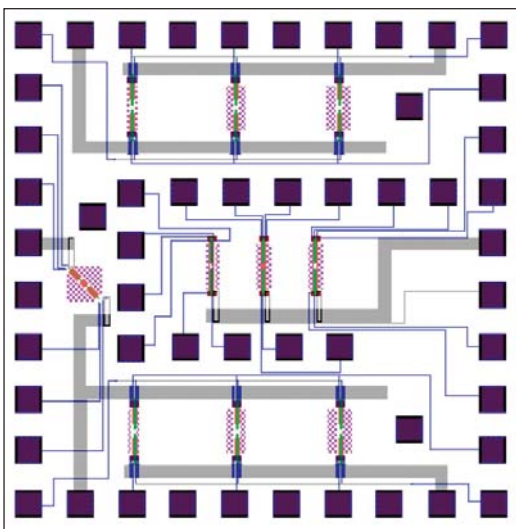


Figure 4. New microhotplate test structures layout.



AT-SPEED TEST OF DIGITAL INTEGRATED CIRCUITS

GOALS

Develop and demonstrate metrology for the at-speed test of digital integrated circuits. The program will resolve the essential metrology issues of at-speed digital integrated circuit test. It will apply its results to characterizing and calibrating high-impedance probes, develop atomic force microscopes (AFMs) capable of precisely positioning field probes above the surface of the integrated circuit, and push the current on-chip sampling technologies now being explored by the industry.

CUSTOMER NEEDS

In the device debug and characterization world, at-speed functional and analog test will continue to serve as a primary vehicle for root cause of design process errors and marginalities (2003 ITRS Test and Test Equipment Section, page 1). Traditional IC contact probing technology requires large contact pads incompatible with the operation and economic constraints of modern IC designs. Alternative probing approaches use high-impedance probes, non-contact probes, atomic-force microscopes, electron beams, optical beams, or on-chip samplers that respond to either electric or magnetic fields near transmission lines in the circuits. However, while the uncalibrated field measurements performed by these probing systems are suitable for field mapping, they are a far cry from the precise measurements of voltages and currents required for electrical design.

Solving the critical at-speed test calibration issues will add enormous value to the probing systems currently being used or developed for high-performance digital integrated circuits. Developing characterization and calibration methods for high-impedance probes, whether of the conventional type or mounted on atomic-force microscopes, will help speed the development and implementation of these new measurement tools, and so create a new paradigm for the at-speed test of high-speed digital integrated circuits.

The need for noninvasive waveform measurements in silicon integrated circuits is discussed in the Test and Test Equipment section, pages 1-5, 2001 (International Technology Roadmap for Semiconductors).



Figure 1. Universal test bed for electric and magnetic field probing on a nanoscale.

TECHNICAL STRATEGY

We will develop calibration artifacts with precisely known high-frequency voltages and currents suitable for characterizing and calibrating high-impedance probes and samplers of all types. We will focus on fundamental calibration issues: transforming the response of the probes to the electric and magnetic fields above the integrated circuit into accurate voltages and currents inside the circuit.

We will first apply the characterization and calibration procedures to conventional high-impedance probes. To facilitate the development and test of electric and magnetic probes with nanoscale resolution, we are constructing a universal AFM test bed for these probes (see Fig. 1). We will then apply our characterization procedures to miniature AFM probes suspended on custom cantilevers designed for high frequency measurements on the nanoscale. Finally, we will tie our metrology back to fully-characterized electro-optic sampling measurements.

NIST also is working on methods for calibrating and correcting imperfections in waveform measurement equipment that cause distorted or blurred measurements. These effects include instrument response, impedance mismatch, multiple reflections, dispersion, time-base distortion, jitter, and drift. After calibration and correction, the measurement has an improved fidelity and is traceable to fundamental physical principles. For example, Fig. 2 shows measurement of a short bit sequence, transmitted at 10 Gbit/s, and plotted in the form of an eye pattern. Before correction for time-base distortion and jitter (caused by the os-

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J. Kopanski
P. Hale

“As electronic devices shrink into the nanometer size scales and integrated circuits operate at multi-GHz clock rates, probing their internal characteristics is becoming both more critical and far more difficult than ever before.”

*Travis M. Eiles, Ph.D.
Intel Corp.*

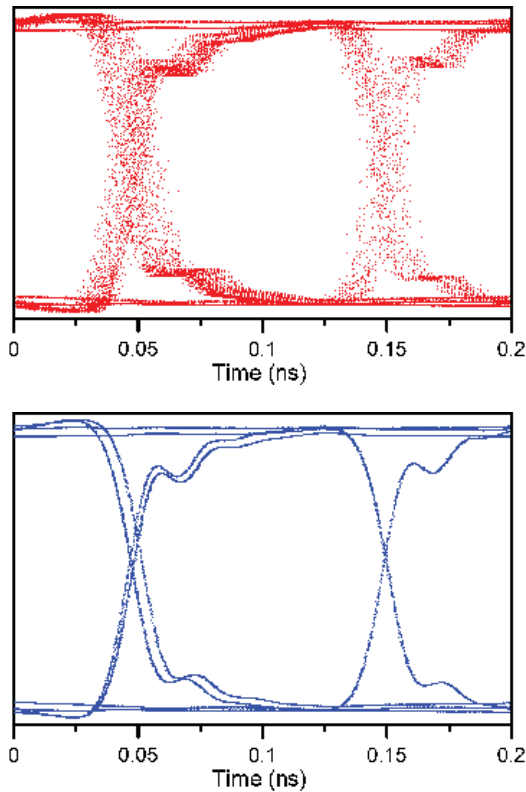


Figure 2. Measurement of 10 Gbit/s eye pattern before (a) and after (b) correction for oscilloscope time-base distortion and jitter using NIST developed techniques.

cilloscope) the eye pattern is blurred while after correction fine features in the eye pattern, such as pattern-dependant jitter, are clearly revealed. Traceability for frequency response is provided to 110 GHz (in coax) and beyond (on wafer) through the NIST electro-optic sampling system.

DELIVERABLES: Characterize novel active high-impedance probe. Attempt to extend bandwidth to 40 GHz with calibration. 4Q 2004

DELIVERABLES: Demonstrate calorimetric non-contacting field probe and measure invasiveness. 4Q 2004

ACCOMPLISHMENTS

- We have designed and tested a prototype sinusoidal waveform standard.
- We have constructed a high-speed electro-optic sampling system.
- We have developed, fabricated and tested a noninvasive AFM scanning probe for measuring local microwave power (see Fig. 3).

- We have developed a method of characterizing and calibrating conventional high-impedance probes for low-invasive waveform measurements (see Fig. 4).
- We have applied our high-impedance-probe characterization method to a probe mounted on an atomic-force microscope.
- We have constructed an AFM universal test bed.

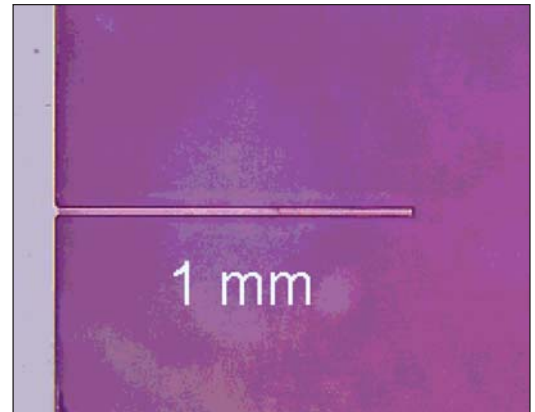


Figure 3. A 1 mm long dielectric bimaterial cantilever AFM probe fabricated at NIST for noninvasively measuring local microwave power.

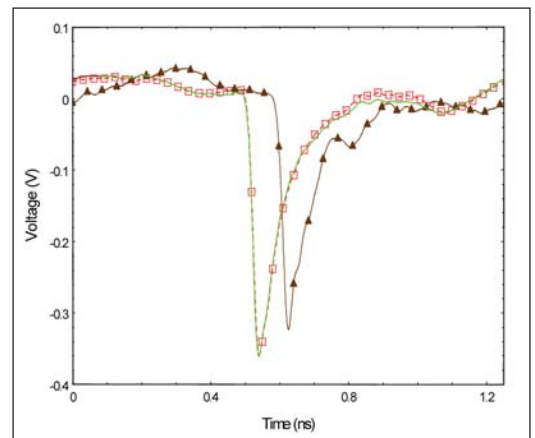


Figure 4. Waveform comparison at the tip of a commercial high-impedance probe. The red curve marked with red squares is the expected waveform. The brown curve marked with triangles is the measured waveform. The green curve is the measured waveform after correction by the new NIST algorithm.

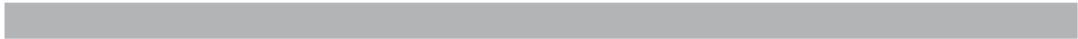
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NON-LINEAR DEVICE CHARACTERIZATION

GOALS

Develop new and general methods of characterizing non-linear devices used in digital wireless communications and high-speed microelectronics; refine and transfer these methods through interactions with industrial and academic research and development laboratories.

CUSTOMER NEEDS

Radio-frequency measurements are applied extensively in the deployment of commercial wireless communication systems and increasingly in high-speed microelectronics. They are crucial to all stages of development, from TCAD to circuit and subsystem design. NIST's RF and microwave measurement teams are addressing the critical need for accurate measurements of non-linear devices and are supporting industrial standards development.

TECHNICAL STRATEGY

The Non-Linear Device Characterization (NDC) Project is developing and verifying measurement-based descriptions of electronic devices and circuits that contain non-linear elements. Traditional rf and high-speed design has relied on the ability to cascade circuit elements through simple linear operations and transformations, but engineers lose the ability to predict circuit performance across operating environments, or states, when their circuits include a non-linear element. Presently, there is a critical need for fundamental RF measurement techniques to develop and validate non-linear models and commonly applied figures of merit. Contributions in this area will significantly improve design-cycle efficiency and trade between manufacturers, and will eventually facilitate improvements in communications through the full incorporation of non-linear models at the system design level.

The NDC Project recently established a new measurement facility known as the Large-Signal Network Analyzer (LSNA). The system provides the most general approach to measuring large-signal waveforms. It is a stimulus-response network analyzer that supplies periodic signals, and then acquires broadband incident and reflection waveforms at the device under test. The NIST facility will be used as a reference system in measurement and model comparisons. The project team is developing accurate calibration and

measurement techniques for the LSNA, including validation of phase-dispersion calibration techniques up to 50 GHz bandwidths. The project team is now refining the statement of measurement uncertainty in all LSNA calibrations and measurements.

The Non-Linear Network Measurement System is being applied first to canonical circuits to compare general measurements with predictions made by circuit simulators and new behavioral models. We have applied these techniques to identify stable verification circuits that will be used in NIST-sponsored interlaboratory comparisons. Second, the measurement system is being applied to develop and verify artificial neural network (ANN) models for non-linear circuits being developed in cooperation with the University of Colorado. LSNA data will be used to train ANN models, to verify circuit operation and model predictions, and to validate a circuit optimization approach.

RECENT ACCOMPLISHMENTS

- Completed study of measurement-based modeling for vector network calibration standards and non-linear microwave devices using artificial neural networks
- Developed new reference calibration for large-signal and traditional vector network analyzer with Vrije Universiteit Brussel
- Developed large-signal measurement method to extract conversion matrices for computer-aided design of RF mixer circuits
- Estimated measurement repeatability variance in harmonic phase reference standards used in commercial large-signal network analyzers
- Completed first phase of an interlaboratory measurement comparison of large-signal network analyzers
- Applied non-linear superconducting device to phase measurements of repetitive RF waveforms
- Defined consistent method for the defining the phase relation of signal components that are not at the same frequency.
- Expanded and clarified definition of large-signal scattering parameters, demonstration application to non-linear rf circuit design.

Technical Contact:
Don DeGroot &
Jeff Jargon

“Your work represents an important development in this area, opening a new application of ANNs to measurement standards.”

*Prof. Q. Y. Zhang,
Carlton University*

“The collaboration between NIST and Intel TCAD has been very beneficial for us to investigate various issues involved in RF characterization of sub-0.25um CMOS and to explore solutions for on-wafer measurement techniques with high accuracy.”

*Changhong Dai,
Intel Corp.
TCAD Division*

- Expanded numerical simulations of the Nose-to-Nose calibrations as the basis for an uncertainty statement on the NNMS phase alignment. There are no other methods of identifying the error terms due to the internal sampling electronics used by the Nose-to-Nose equipment. The simulator-based sensitivity study gives us the basis for a first-level uncertainty bound.
- Designed interlaboratory measurement comparison for non-linear network analyzer users. Designed and fabricated prototype verification circuits. Formulated initial comparison method and measures. Performed initial comparisons between NIST and Belgian research labs. Users of NNMS and related non-linear network analyzers will gain assurance in their ability to identify non-linear input-output transfer functions or extract model parameters.
- Developed non-linear models for verification devices. Developed and applied conventional compact diode models. Developed frequency-domain behavioral modeling strategy with the University of Colorado. Developed time-domain behavioral model with guest researcher from K. U. Leuven, Belgium. The interlaboratory comparison of non-linear network analyzers requires models since we do not have a generalized non-linear parameter to compare. The models can accurately represent the non-linear transfer functions of the verification circuits over the state-space that they are characterized, allowing participants to find the differences between their measurements and our model predictions.

COLLABORATIONS

Vrije Universiteit Brussel, Department ELEC. To develop stochastic calibrations for accurate radio-frequency circuit and device measurements.

University of Colorado, Electrical and Computer Engineering Department. To develop new measurement-based behavioral models of non-linear RF circuits and devices.

NIST ITL Statistical Engineering Division. To develop standard non-linearity, then use it to verify LSNA calibrations and modeling approaches.

K.U. Leuven, Belgium. To develop dynamic models for HEMTs, and to study instrument repeatability.

University of Florence, to develop new measurement-based models of rf and microwave mixer circuits.

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D. Schreurs, J. A. Jargon, K. A. Remley, D. C. DeGroot, and K. C. Gupta, "Artificial neural network model for HEMTs constructed from large-signal time-domain measurements," *59th ARFTG Conf. Dig.*, pp. 31-36 (June 7, 2002).



JITTER AND PROPAGATION DELAY MEASUREMENTS

GOALS

To develop methods for accurately measuring timing jitter in high bit rate (> 10 GB/s) telecommunication systems and develop systems and protocols for measuring and computing propagation delay through active circuits. This includes the development of artifact standards, data extraction and analysis procedures and algorithms, and measurement systems, each where necessary. Existing measurement methods will be examined to determine consistency amongst them, measurement limitations, and range of applicability. Measurement services will be developed for the measurement of different types of jitter and for propagation delay.

CUSTOMER NEEDS

Jitter is a limiting factor in the performance of high-frequency/high-speed telecommunications and computer systems. A typical eye diagram measurement is shown in Fig. 1. In a tele-communications system, where a series of clock-recovery circuits is typically used, jitter degrades data recovery performance. Jitter measurements on telecommunications components and equipment are needed to assure compatibility between manufacturers and to identify sources of jitter. For microprocessor chips, the jitter in the on-chip phase-lock-loop circuit is used by the manufacturer to sort the microprocessor for clock speed usage. Large errors in the measurement of clock jitter represent manufacturing yield loss. Furthermore, for some high-speed computers, the frequency of the microprocessor clock is a multiple of the system clock frequency, and jitter degrades the timing tolerance of the circuit. The data stor-

age industry is also concerned with jitter in recovery of data from the source media.

The calibration of jitter measurement equipment to an uncertainty of a few picoseconds is a difficult problem. Several types of jitter measurements that are important are: transition-to-transition jitter, jitter relative to a fixed clock, jitter spectrum, and data dependent jitter. These measurements are important for determining the source of jitter and component compatibility. To test components accurately, jitter generation is important. Industry has reported to NIST that they get inconsistent results from jitter measurements using different techniques and would welcome a neutral party to evaluate the limits of the many measurement methods.

The importance of jitter measurement capability is described in the 2003 International Technology Roadmap for Semiconductors on several pages. In particular, on page 11 of the Test and Test Equipment section, it states, "The jitter generated by a transmitter is the key parameter to guarantee transmitter quality. Currently, jitter measurement capability on ATE is in its infancy, there is no instrument available that simultaneously satisfied the noise floor, analog bandwidth and test time requirements for high performance interfaces."

Propagation Delay – Propagation delay in active circuits is defined as the difference between the occurrence of some event on an output signal relative to that of the input signal. The measurement of this type of delay is not straightforward because the characteristics of the input signal affect both the characteristics of the output signal and the time the output signal exits the circuit. Automated test equipment (ATE) from different manufacturers produce different input signals, and this results in different delays for a given circuit. Furthermore, the ATE results may not emulate actual delays because the ATE signal and/or electrical environment may not represent accurately what is expected by the circuit.

The ability to reproducibly measure propagation delay is an issue. This will require interaction with industry to develop an accepted reference signal and, perhaps, impedance environment. Furthermore, accurate (picosecond) delay measurements will require traceability over the delay ranges (several microseconds) required by

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D. I. Bergman

"Accurate characterization of the jitter on a signal, as well as a system's ability to tolerate jitter are critical... for the designer and manufacturer of communication systems and components."

Brian Scott,
Agilent Technologies

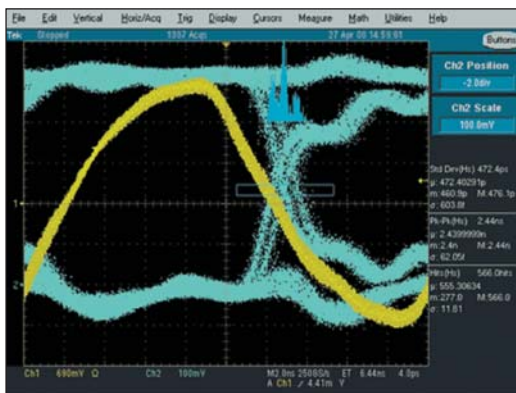


Figure 1. Eye diagram for jitter measurements.

industry. Measurement protocols will also have to be established.

TECHNICAL STRATEGY

To develop a precision differential delay system that will be used to measure jitter and propagation delay in electronic circuits and systems. The hardware for providing differential delays to 1 μ sec will be designed and developed, and the temperature sensitivity and repeatability of the differential delay settings will be measured. In addition, methods for accurately (uncertainties ± 1 ps) calibrating the discrete differential delays will be developed. A continuously variable differential delay from 0 ns to 1 ns and methods for accurately calibrating the delay transfer function and its temperature sensitivity will also be developed.

DELIVERABLES: Design calibration methods for and calibrate the precision differential delay system. 2Q 2004

DELIVERABLES: Write control software for coarse, medium, and fine delay subsystems. 3Q 2004

DELIVERABLES: Perform uncertainty analysis for precision differential delay system. 4Q 2004

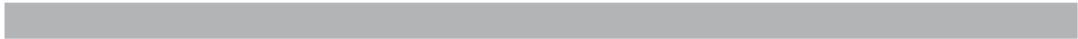
DELIVERABLES: Expand range and lower uncertainties for 65400S, Pulse Time Delay Interval. 2Q 2005

ACCOMPLISHMENTS

- Built coarse, medium, and fine delay subsystems.

MANUFACTURING SUPPORT PROGRAM

Cross-cutting all manufacturing disciplines is the need for supporting information technology and processing capabilities. The transition to 300mm fabs, single-wafer lots, and the extensive use of foundries has made efficient information handling and automation indispensable to the production process. Information technology touches nearly every aspect of semiconductor production and distribution, including process control, tool to tool interconnect, automated material handling and tracking, reticle management, and information interchange across the supply chain. NIST is working with International SEMATECH to provide and maintain an on-line engineering statistical handbook to support process control, and is working with industry on standards required to support information flow across the “engineering chain.”



TIME SYNCHRONIZATION AND TIME STAMPING NEEDS FOR DATA COLLECTION IN SEMICONDUCTOR MANUFACTURING

GOALS

The project's objective is to educate the industry about the requirements, related issues and potential methods to achieve reliable clock synchronization and time stamping capabilities for supporting e-Manufacturing needs, present and future.

CUSTOMER NEEDS

Increasing wafer sizes, decreasing critical dimensions, and new material introduction all challenge higher initial yield, lower manufacturing costs, and time to market demands. Among the key issues driving the challenges are monitoring and maintaining surface uniformity, decreasing process tolerance windows, as well as increasing process and equipment complexity.

Manufacturing of 300 mm semiconductors will require data to be collected and analyzed from a rising confluence of data streams, due to additional sources previously thought to have little impact on manufacturing. Some of the pertinent sources include process equipments and their operational subsystems, in-line metrology, and factory environmental conditions. The retrieved data is vital for designing new processes, maintaining optimal equipment and processing capabilities, controlling the equipment, providing information for rapid yield learning, and expediting handoff of process technology for volume production.

The exponential increase in data collection rates required to meet future technology goals has been a cross cutting issue in the International Technology Roadmap for Semiconductors (ITRS). One of the projected near term Factory Integration difficult challenges as specified by the 2003 ITRS is the:

"...Explosive growth of data collection/analysis requirements driven by process and modeling needs." 2003 ITRS, Factory Integration, p. 8.

Managing the data proliferation will be critical in realizing the anticipated benefits of greater data accessibility. Extrapolating intelligent correlations from volumes of data in a timely

manner requires a common, efficient method of merging the data. In the area of yield learning the 2003 Yield Enhancement group cites:

"Accessing the raw data in such a way as to generate meaningful correlations and results is going to be critical requirement in the 300 mm node The greatest challenge to a comprehensive data management system required for yield learning is the ability to deal with and integrate data streams that are continuous, periodic, sporadic, and interval based" 2003 ITRS, Yield Enhancement, pp. 13-14.

Indeed there are software-based algorithmic techniques for merging data streams, but they can only provide limited certainty to the results, without taking into account the scalability of the solution as data numbers proliferate in the future. To this day, the most robust, efficient and technically sound mechanism for merging different data streams is through the use of *accurate* time stamps. An inaccurate time stamp renders the data invalid for many data mining and other data analysis applications, yet there continues to be a wide variation in time stamping accuracy among semiconductor manufacturing systems. A robust infrastructure to support accurate time stamps will provide the means to better exploit the increased data availability in next generation semiconductor manufacturing. Such an infrastructure will require clock synchronization of all the related local clocks in the manufacturing site including the clocks within the process and metrology tools.

TECHNICAL STRATEGY

This project will investigate and document key issues and potential solutions related to clock synchronization and time stamping within manufacturing sites in order to ensure validity of the data for achieving intelligent analysis results. Current timestamp accuracy capabilities, issues preventing the dissemination of accurate timestamps and industry requirements are being gauged based on inputs from network engineers and information technology (IT) managers from chip manufacturers. Feedbacks from equipment makers also provide insight into current architec-

Technical Contacts:

Y. Li

tural issues preventing tools from providing accurate clock synchronization and time stamping. Software suppliers for process analysis tools will also be able to provide insight on current limitations due to inaccurate time stamps.

To achieve accurate timestamps, it is imperative to have a reliable and accurate clock synchronization methodology. The industry should understand how to obtain and distribute accurate time throughout their factory networks. Network Time Protocol (NTP) and IEEE 1588 Precision Time Protocol (PTP) for industrial sensor networks are two of the key protocols for potential use in the semiconductor industry. Consistent time stamping formats must also be established, and the project will look at some of the widely used formats available such as ISO 8601. Semiconductor Equipment Materials International (SEMI) standards will also need to be reviewed to determine which standards would be affected by future clock synchronization guidelines and time stamping standards.

DELIVERABLES: Assessment of industry time synchronization and time stamping issues and potential solutions will be reported. 4Q 2004

The project will assess both NTP and PTP to understand the inherent tradeoffs and provide some guidelines of best practices. Insights based on review of how other industries have addressed the clock synchronization and time stamping issue will also provide some guidelines of how the semiconductor industry can evolve to adopt an accurate time stamping mechanism. A small network of NTP servers will be established to estimate its accuracy capabilities under different configurations. Findings from the experiment will reveal some best methods for NTP use. The project will also continue to follow developments in PTP and participate in the IEEE 1588 User Requirements task force.

DELIVERABLES: Report on future standards and guidelines required along with recommendations for best methods and practices in time synchronization and time stamping. 4Q 2004

ACCOMPLISHMENTS

- The ISMT report on “Semiconductor Factory and Equipment Time Synchronization” was published to provide an overview of IEEE 1588 as a potential time synchronization protocol for the semiconductor industry.

- Informal interviews with chip manufacturers and an equipment maker revealed the critical clock

synchronization issues lie within the tool architecture. Within the equipment, time stamping delays can range from 100 milliseconds to 2 minutes. Equipment clock accuracies can also fluctuate significantly due to overloaded equipment processors.

- Researched and summarized methods for distributed time synchronization including NTP, PTP, and another proprietary solution, SynUTC. NTP appears to be a reliable interim solution as the industry becomes more attuned to future capabilities of PTP.

- A presentation was given on time synchronization issues and potential solutions at the SEMI International Equipment Engineering Task Force. Ensuing dialogue led to a motion to initiate a Time Synchronization Task Force to address the issues.

COLLABORATIONS

Brad Van Eck, International SEMATECH Manufacturing Initiative

ENGINEERING CHAIN MANAGEMENT IN THE SEMICONDUCTOR INDUSTRY

GOALS

This project will investigate and document key issues related to electronic data exchange, supply chain communication, and other automation standardization needs confronting the semiconductor industry. The objective of this project is to facilitate the evolution of an integrated semiconductor “Engineering Chain” which provides each partner with the data needed to make business decisions in a timely manner.

CUSTOMER NEEDS

Increasing technological requirements has led the semiconductor industry to seek further means of cost savings by improving factory productivity, streamlining business models, and accelerating their supply chain. The growing complexity of product development and manufacturing models in parallel with shrinking product lifecycles further exacerbates the challenges the industry faces. Maximizing interoperability among automation systems in the factory and throughout the supply chain will become a greater issue for realizing the semiconductor industry’s hopes to reduce time, inventory, and therefore costs.

Rapid changes in semiconductor technologies, business requirements, the need for faster product delivery, and volatile market conditions are making effective and timely factory integration to meet accelerated ramp and yield targets more difficult over time. 2003 International Technology Roadmap for Semiconductors Factory Integration (ITRS), p.1.

The transition to 300 mm fabs and single-wafer lots has challenged the semiconductor industry in nearly every aspect of production, such as: facility layout; the mix of R&D within a single fab; data analysis of small lots; tool to tool interconnect; automated material handling and tracking of product, non-product wafers and reticles; the division of the production process across a partnership of foundries, designers, production sites, distributors and equipment manufacturers. Chip manufacturers require greater visibility of end product demand to accurately schedule their factories, and require greater technical collaboration with designers, OEMs, and foundries to ensure the manufacturability of the product being

designed today using the generation of equipment that will be installed once production starts.

Cost of design is the greatest threat to continuation of the semiconductor roadmap. 2003 ITRS, p. 1.

According to the 2001 ITRS, design complexity has been growing exponentially due to the increasing density and number of transistors to meet performance goals. Intellectual Property (IP) reuse helps companies get complex systems to market quickly by eliminating redundant design effort. Standard formats for IP specifications and tool interfaces for the design of a System-on-a-Chip (SoC) would reduce time to market by eliminating the need for translations. Security mechanisms must also be incorporated to protect IP during transfers.

Other information-exchange gaps in design houses include standard data formats for timing and power to expedite timing closure, reduce design iterations, and promote interoperability among best-of-breed software tools.

The industry trend towards outsourcing is leading towards silos of expertise, exactly when technology advances require a multi-disciplinary approach to problem solving. The production process is being conducted across fabs – not only at the traditional point of packaging and test, but mid-stream in the IC fabrication process. As the wafers change hands, so must the information about that wafer which accumulated during its production life cycle.

TECHNICAL STRATEGY

To help the industry achieve their goal of effective partnerships within an Engineering Chain, this project will engage in industry efforts that would benefit from NIST’s neutrality, multi-industry expertise, and broad and detailed knowledge of the Information Technology (IT) standards development process.

DELIVERABLES: Contribute to the update of the Factory Integration component of the ITRS by co-leading the Engineering Chain Management subteam. 4Q 2004

Technical Contacts:

J. Messina
K. Brady

Attendance at workshops, conferences, and standards meetings held by key organizations in the semiconductor community such as International SEMATECH (ISMT), Semiconductor Equipment Materials International (SEMI) and RosettaNet provides opportunities to assess current areas of IT standards development. As the industry moves towards utilization of mainstream computing technologies including eXtensible Markup Language (XML) and Simple Object Access Protocol (SOAP), the project also provides guidance in leveraging existing best practices from other industries and to promote collaborations among industry partners for mutual benefit.

The investigation also includes an informal survey of semiconductor supply chain partners including designers, chip manufacturers, and equipment suppliers to gauge their existing practices, requirements and priorities. Site visits will provide an opportunity for key industry figures to share their vision of how IT standards would expedite advancement of new technologies and business models.

DELIVERABLES: Establish a working agreement with ISMT in order to identify top industry IT-standards related needs and develop potential solutions to the current challenges based on cross-industry solutions facing similar issues. 4Q 2004

As appropriate, the survey also provides an opportunity for providing insights and guidance from similar industry efforts in supply chain and equipment communication standards to facilitate existing standards developments.

In response to industry needs, the survey will validate internal NIST IT projects against the semiconductor industry's requirements. One potential project is the Infrastructure for Integrated Electronics Design and Manufacturing (IIEDM). IIEDM has facilitated neutral XML-based standards development in the electronic exchange of technical and business data in the electronic components supply chain. Similarities in challenges and technologies utilized may provide an opportunity for future collaborations. In addition, experience with standards development in various industries positions NIST to provide impartial cross-industry benchmarks for IT exchange strategies.

DELIVERABLES: Provide technical assistance to facilitate current IT standards development efforts within the semiconductor industry. 4Q 2004

ACCOMPLISHMENTS

- Assessed the current and future direction of IT use in semiconductor and mask manufacturing. Site visits conducted at four IC manufacturers, one design house, and one photomask supplier.
- NIST has been co-leading the Engineering Chain Management sub-team of the ITRS Factory Information and Control Systems team. Initial efforts are being made to determine the scope and identify the challenges of creating an effective Engineering Chain.
- Surveyed current standards development activities in semiconductor manufacturing and potential NIST roles in various task forces by participating in a variety of standards activities. Diagnostic Data Acquisition (DDA), XML, Process Control System (PCS), and Equipment Engineering Capabilities (EEC) are possible areas where NIST can play a future role. Leveraging use of mainstream technologies appears to be widely accepted. Data acquisition standards, including issues of data modeling, speed, bandwidth, quality and integrity, have become critical in advancing e-manufacturing efforts. Follow-up discussions with members of SEMI and ISMT indicated interest in enlisting NIST expertise and contacts to leverage best practices from other industries on specific issues such as XML-based standards development for manufacturing, timing and synchronization of equipment data, as well as data security issues.

COLLABORATIONS

Alan Weber, Alan Weber & Associates

ITRS Factory Integration Technical Working Group

SEMI XML Task Force

International SEMATECH (ISMT)

NIST/SEMATECH e-HANDBOOK OF STATISTICAL METHODS

GOALS

The goal of the NIST/SEMATECH e-Handbook of Statistical Methods project is to produce an online resource to help scientists and engineers incorporate statistical methods into their work more efficiently. Electronic publication and a practical, example-driven format were chosen to make the e-Handbook readily accessible to its target audiences in industry, including the semiconductor manufacturing industry in particular.

CUSTOMER NEEDS

Semiconductor manufacturing requires extraordinary discipline in process control. For example, a typical integrated circuit manufacturing process involves several hundred steps. These steps may include as many as thirty lithographic levels, which require extremely precise alignment with respect to one another. Tight process control is essential to produce a functional circuit. SEMATECH has recognized the importance of statistical process control in semiconductor manufacturing and has developed and maintained expertise in this field since its inception in 1988. Two of the more difficult issues impeding routine implementation of these techniques, however, include educating the users and making the tools easy to use.

TECHNICAL STRATEGY

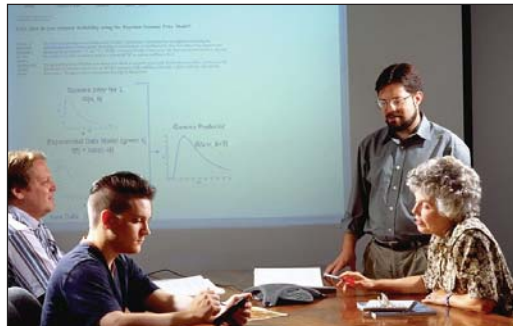
NIST and SEMATECH formed a collaboration under the umbrella Cooperative Research and Development Agreement (CRADA), combining the general expertise in engineering statistics at NIST with the semiconductor manufacturing expertise resident at SEMATECH.

DELIVERABLES: Update and maintain the e-Handbook on-line, and continue to distribute the e-Handbook on CD for off-line use. 4Q 2004

ACCOMPLISHMENTS

■ Since release of the final version, work has focused on publicizing the e-Handbook, responding to user feedback, and developing a CD version for off-line use. In the last year, over 3,000 e-Handbook CDs have been distributed to industrial, government, and academic users all over the world. Publicity on the e-Handbook has appeared in *Science*, *Quality Digest*, *MicroMagazine.com*, *States News Service*, *National Science Digital*

Library Report for Math, Engineering, and Technology, and American Statistician.



NIST e-Handbook of Statistical Methods team (left to right, Alan Heckert, Mark Reeder, Will Guthrie, and Carroll Croarkin) reviewing a page from the chapter on product reliability.

COLLABORATIONS

International SEMATECH, Paul Tobias, Jack Prins, Chelli Zey; project planning, organization, writing and editing.

AMD, Barry Hembree; project planning, organization, and writing.

Motorola, Pat Spagon; project planning, organization, and writing.

RECENT PUBLICATIONS

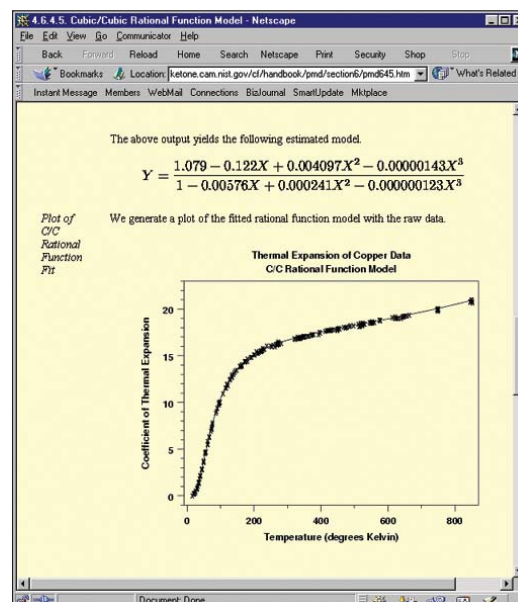
NIST/SEMATECH e-Handbook of Statistical Methods, M. Carroll Croarkin and Paul Tobias, editors, <http://www.nist.gov/stat.handbook/>.

Technical Contacts:

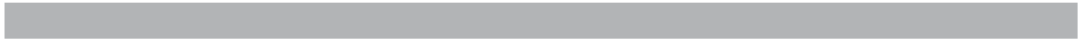
W. F. Guthrie
A. Heckert
J. J. Filliben

"I am thoroughly enjoying your Engineering Statistics Handbook. Thanks so much for adding real value to the information available on the Internet!!!"

Paul Zaremba,
Systems Engineer,
Agilent Technologies



Page from a case study in the process modeling chapter of the Handbook.



INVITED TALKS

Steve Knight, 10/24/03, invited talk

Overview of NIST Metrology Development for the Semiconductor Industry”
Presentation to ATP award recipients working on organic semiconductors, NIST,
Gaithersburg, MD

Steve Knight, 11/18/03, WEB Cast presentation

Metrology Challenges for the Semiconductor Industry”
Process Outlook Forum-2003 w/Dr. Jeff Butterbaugh

Steve Knight, 3/15/04, invited talk

”Development of Critical Dimension Metrology for Nanotechnology at the National Institute of
Standards and Technology”
SMAM, Tokyo, Japan

Steve Knight, 05/04/04, invited talk

”Semiconductor Metrology Development at NIST”
Presented to Axcelis
Beverly, MA

Steve Knight, 05/12/04, invited talk

“Office of Microelectronics Programs,”
Presented to National Research Council Sub-Panel on Semiconductor Microelectronics
Gaithersburg, MD

Jack Martinez, 09/17/04, invited talk

“Semiconductor Metrology Programs at NIST,”
SUFRAMA Manaus, Brazil

ABBREVIATIONS AND ACRONYMS

AC	alternating current
ADR	adiabatic demagnetization refrigerator
AEM	analytical electron microscopy
AES	Auger-electron spectroscopy
AFM	atomic force microscope
ALMWG	Analytical Laboratory Managers Working Group (ISMT)
AMAG	Advanced Metrology Advisory Group (ISMT)
ANSI	American National Standards Institute
ARXPS	angle resolved X-ray photoelectron spectroscopy
ASPE	American Society of Professional Engineers
ATP	Advanced Technology Program (NIST)
BCB	benzocyclobutene
BESOI	bond and etch-back silicon-on-insulator
BGA	ball-grid array
BIPM	Bureau International des Poids et Mésures
BIST	built-in self-test
BST	barium strontium titanate
C-AFM	calibrated atomic force microscope (NIST)
C-V	capacitance-voltage
CAD	computer-aided design
CCD	charge-coupled device
CD	critical dimension
CMOS	complementary metal oxide semiconductor
CMP	chem-mechanical polishing
CRADA	Cooperative Research and Development Agreement
CRDS	cavity ring-down spectroscopy
CSP	chip-scale package
CTCMS	Center for Theoretical and Computational Materials Science (NIST)
CVD	chemical vapor deposition
DC	direct current
DFT	design-for-test
DMA	differential mobility analyzer
DRAM	dynamic random-access memory
DSP	digital signal processing
DUV	deep ultraviolet

EBSD	electron backscatter diffraction
EELS	electron energy loss spectroscopy
EDC	embedded decoupling capacitance
EDS	energy-dispersive spectroscopy
EMC	electromagnetic compatibility
EMI	electromagnetic interference
EPMA	electron probe microanalysis
EUV	extreme ultraviolet
FIFEM	field ion field emission microscope
FIM	field ion microscope
FWHM	full-width half-maximum
GIXR/SE	grazing incidence X-ray reflection/spectroscopic ellipsometry
GIXPS	grazing incidence X-ray photoelectron spectroscopy
HRTEM	high resolution transmission electron microscope
HSQ	hydrogen silsesquoxane
I-V	current-voltage
IGBT	insulated-gate bipolar transistor
IPC	Association Connecting Electronics Industries
ISMT	International SEMATECH
ISO	International Organization for Standardization
ITRS	International Technology Roadmap for Semiconductors
LEED	low-energy electron diffraction
LER	line-edge roughness
LFPG	low frost-point generator
LOCOS	LOCal oxidation of silicon
LPP	laser-produced plasma
LPRT	light-pipe radiation thermometer
MBE	molecular beam epitaxy
MEMS	micro-electro-mechanical systems
MFC	mass flow controller
MMIC	millimeter and microwave integrated circuits
MOS	metal-oxide-semiconductor
MOSFET	metal-oxide-semiconductor field-effect transistor
MUX	multiplex
NCMS	National Center for Manufacturing Sciences
NDP	neutron depth profiling
NGL	next generation lithography

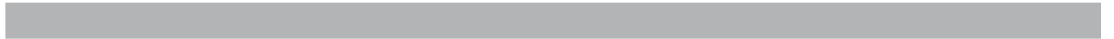
NEMI	National Electronics Manufacturing Initiative
NIST	National Institute of Standards and Technology
NSMP	National Semiconductor Metrology Program
NLO	non-linear optical
NSOM	nearfield scanning optical microscopy
OMAG	Overlay Metrology Advisory Group (ISMT)
PED	Precision Engineering Division (NIST)
PLIF	planar laser-induced fluorescence
PMI	phase-measuring interferometer
PTB	Physikalisch-Technische Bundesanstalt
PZT	lead zirconium titanate
QM	quantum mechanics
RAM	Random-access memory
RGA	residual gas analyzer
RTA	rapid thermal annealing
RTP	rapid thermal processing
SANS	small-angle neutron scattering
SBIR	Small Business Innovative Research
SCM	scanning capacitance microscope
SEM	scanning electron microscope
SHG	second harmonic generation
SIA	Semiconductor Industry Association
SIMOX	separation by implantation of oxygen
SIMS	secondary-ion mass spectrometry
SoC	system-on-chip
SOI	silicon on insulator
SPM	scanning probe microscope
SRC	Semiconductor Research Corporation
SRM [®]	Standard Reference Material
SSHG	surface second-harmonic generation
SSIS	surface-scanning inspection system
SURF III	Synchrotron Ultraviolet Radiation Facility III
TCAD	technology computer-aided design
TDDDB	time-dependent dielectric breakdown
TDR	time-domain reflectometry
TEM	transmission electron microscope
TFTC	thin-film thermocouple

TOF	time-of-flight
TMAH	tetramethyl ammonium hydroxide
UHV	ultra-high vacuum
UV	ultraviolet
WMS	wavelength modulation spectroscopy
VUV	vacuum ultraviolet
XPS	X-ray photoelectron spectroscopy

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Interconnect Materials and Reliability Metrology	M. Gaitan B. Keller M. Cresswell	(301) 975-2070 (303) 497-7651 (301) 975-2072	michael.gaitan@nist.gov keller@boulder.nist.gov michael.cresswell@nist.gov
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