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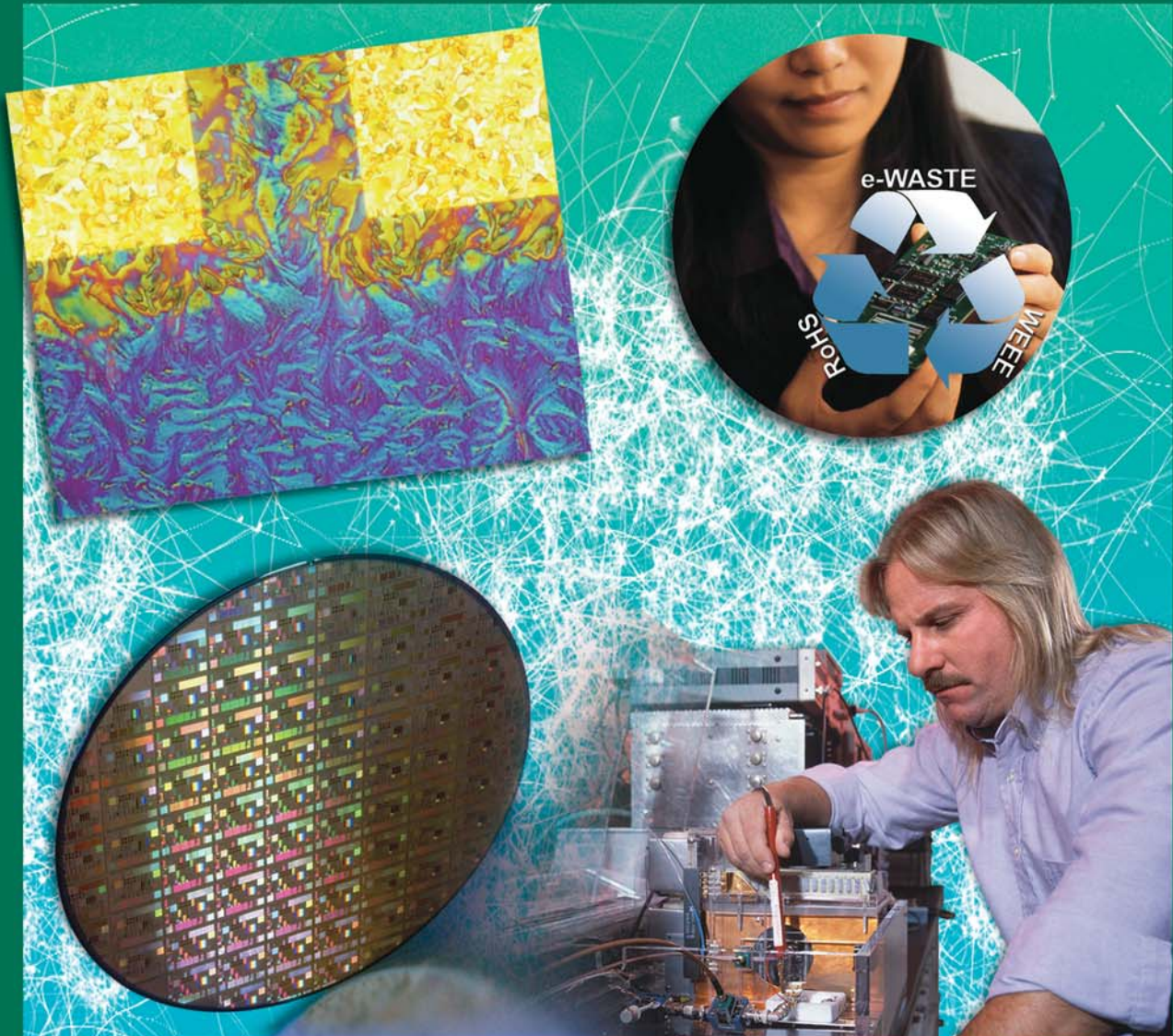
NISTIR 7368

January 2007

**ELECTRONICS AND ELECTRICAL
ENGINEERING LABORATORY**

SEMICONDUCTOR ELECTRONICS DIVISION

**PROGRAMS, ACTIVITIES, AND
ACCOMPLISHMENTS**



THE ELECTRONICS AND ELECTRICAL ENGINEERING LABORATORY

One of NIST's seven Measurement and Standards Laboratories, EEEL conducts research, provides measurement services, and helps set standards in support of: the fundamental electronic technologies of semiconductors, magnetics, and superconductors; information and communications technologies, such as fiber optics, photonics, microwaves, electronic displays, and electronics manufacturing supply chain collaboration; forensics and security measurement instrumentation; fundamental and practical physical standards and measurement services for electrical quantities; maintaining the quality and integrity of electrical power systems; and the development of nanoscale and microelectromechanical devices. EEEL provides support to law enforcement, corrections, and criminal justice agencies, including homeland security.

EEEL consists of four programmatic divisions and two matrix-managed offices:

Semiconductor Electronics Division

Optoelectronics Division

Quantum Electrical Metrology Division

Electromagnetics Division

Office of Microelectronics Programs

Office of Law Enforcement Standards

This document describes the technical programs of the Semiconductor Electronics Division. Similar documents describing the other Divisions and Offices are available. Contact NIST/EEEL, 100 Bureau Drive, MS 8100, Gaithersburg, MD 20899-8100, Telephone: (301) 975-2220, On the Web: www.eeel.nist.gov

Cover caption: (clockwise from lower left) an IBM 200 mm EDRAM Wafer (photo by Tom Way, courtesy of International Business Machines Corporation, unauthorized use not permitted); optical micro-graph showing the complex film structure of a solution processed organic field effect transistor; visualization of the Electronic Information Group's efforts on developing standards for the manufacture of Semiconductor Electronics and Printed Circuit boards that are environmentally friendly; Division researcher Allen R. Hefner, Jr., performs high-speed, high-voltage silicon carbide device characterization using NIST-developed, specialized equipment; (background) nanowires grown on square-pattern gold thin film catalyst.

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U.S. DEPARTMENT OF COMMERCE

Carlos M. Gutierrez, Secretary

Technology Administration

Robert Cresanti, Under Secretary of Commerce for Technology

National Institute of Standards and Technology

William Jeffrey, Director



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David G. Seiler,
Division Chief

“Industry views SED’s contributions as unique and essential to efficiently providing measurement techniques and standards.”

NRC Panel Report, An Assessment of the National Institute of Standards and Technology Measurement and Standards Laboratories: Fiscal Year 2003

WELCOME

It is my great pleasure to introduce you to the Semiconductor Electronics Division (SED) and share some of our exciting technical work. As the semiconductor industry continues its move toward silicon nanoelectronics and beyond, the introduction of new materials, efficient and reliable processing techniques, novel devices, and new metrology is essential. We have entered an era where nanotechnology is impacting our drive to smaller, faster, cheaper, and more complex chips. Innovative metrology is critical in providing solutions for long-term reliability and repeatability for these new technologies and chips. As a NIST metrologist, I welcome this opportunity to show you how the SED is helping shape the future direction of metrology for the semiconductor industry. Great opportunities exist for those of us in the metrology community to provide innovative solutions to industry’s key measurement needs. I want to learn about the most important issues you are facing, as well as how improved measurements can help you innovate. Please contact us if we can be of assistance.

The primary mission of the Division is to provide the measurement and software infrastructure to U.S. industry for mainstream silicon CMOS (complementary metal-oxide semiconductor) and beyond CMOS technologies, as well as other advanced semiconductor technology needs. The Division provides necessary measurements, physical standards, and supporting data and technology; associated generic technology; software for improving interoperability; and fundamental research results to industry, government, and academia. Its programs also respond to industry measurement needs related to MicroElectroMechanical Systems (MEMS), power electronics, organic/plastic electronics, and various sub-areas of nanotechnology including nanoelectronics, nanocharacterization, nanoreliability, nanobiotechnology, and nano- and micro-fluidics.

The Division has extensive interactions with individual companies, industry organizations, professional societies, and universities; these activities enable the development of a research agenda responsive to the needs of industry and the nation. Active participation in industry roadmapping, such as the Semiconductor Industry Association’s International Technology Roadmap for Semiconductors (ITRS), and standards development activities for the Semiconductor Equipment and Materials Institute (SEMI) are practiced by the Division to prioritize and establish programs with the highest potential impact. Division researchers work with SEMI on new standards to help guide the future path of our industry in areas such as MEMS, high- κ dielectrics, e-diagnostics, e-manufacturing, time synchronization, traceability, and metrics. Why not become involved yourself and help shape the future direction of technology and metrology? We need innovative metrology breakthroughs that will propel our industry forward. The Division widely disseminates the results of its research, especially in the areas of standardized test methods and Standard Reference Materials (SRMs), through a variety of channels: publications, software, conferences and workshops, and participation in standards organizations and consortia.

The Division, with a staff of about 80 including full-time and part-time employees as well as guest researchers, post-doctoral associates, contractors, and students, is based in Gaithersburg, Maryland, and is one of four divisions within the Electronics and Electrical Engineering Laboratory at NIST. The Division’s technical activities are organized into three groups: the Enabling Devices and ICs Group, the CMOS and Novel Devices Group, and the Electronic Information Group. The Division assists industry by providing tools such as new or improved measurement methods, SRMs, test structures and chips, standard reference data, and software that support the needed measurement infrastructure. Division personnel visit industrial sites, host a variety of visitors, and make available tutorial material on an as-needed basis. We also are active in conference and workshop activities that directly benefit the industry.

The Division, in cooperation with the National Research Council (NRC), offers competitive awards for post-doctoral research for U.S. citizens in a variety of technical fields related to the semiconductor electronics industry. For additional details, including field descriptions and qualification guidelines, please see page 52.

The technical programs, their goals, technical strategies, activities, and accomplishments described here for each Division project clearly demonstrate the impact of the SED's leadership and effective service as it continues to respond to the needs of industry and to contribute to the scientific and engineering communities. Please take an opportunity to visit our Division website, which provides further details on our Division, shows up-to-date project information, and has interactive tutorials on the Hall effect (www.eeel.nist.gov/812/hall.html) and MEMS standard test structures based on e-standards (www.eeel.nist.gov/812/test-structures/). Please also be sure visit the Systems Integration for Manufacturing Applications website (www.nist.gov/sima) on product data exchange standards.

Thank you for your interest in our Division and its technical programs! I welcome your comments and suggestions.



David G. Seiler
Division Chief



Semiconductor Electronics Division Staff

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On the Web: www.eeel.nist.gov/812/

“The nature of the vision’s purpose is not only to achieve a meaningful strategic or company goal, but also to build a dedicated community...”

Jay A. Conger, The Brave New World of Leadership Training, IEEE Eng. Mgmt. Review (1996)

MISSION

The **Semiconductor Electronics Division** provides technical leadership to industry, government, and academia in research and development of the semiconductor measurement and software infrastructure needs essential to the silicon microelectronics industry, advanced semiconductor materials technologies, and advanced electronic devices based upon molecular or quantum structures.

VISION

The **Semiconductor Electronics Division** strives to be recognized as a dynamic, world-class resource for semiconductor measurements, data, models, software, and standards focused on enhancing U.S. technological competitiveness in the world market.

VALUES

The **Semiconductor Electronics Division** values its commitment to identify and meet crucial measurement technology needs. The Division values its collaboration with all segments of the semiconductor community. It strives for integrity, excellence, objectivity, responsiveness, and creativity, while maximizing and utilizing the potential of its employees.

GOALS

The Division will:

- Aggressively pursue and achieve select metrology needs as identified in the International Technology Roadmap for Semiconductors for mainstream silicon.
- Develop new and improved process-monitoring tools, methodologies, and data for the more efficient manufacture of silicon and compound-semiconductor devices.
- Develop cooperative, multidisciplinary projects within the Division and synergistic external collaborative efforts to better meet the critical needs of the semiconductor industry.
- Support novel research that has high potential for providing breakthroughs in materials, process, devices, and measurement technologies for the semiconductor industry.

NIST MISSION

NIST promotes U.S. innovation and industrial competitiveness by advancing measurement science, standards, and technology in ways that enhance economic security and improve our quality of life.

SEMICONDUCTORS: BACKBONE OF THE NANOELECTRONICS REVOLUTION

The semiconductor electronics industry is vital to the U.S. economy and affects every aspect of our daily lives. Semiconductors are pervasive in the microelectronic components used in computers, MP3 players, video game consoles, HDTVs, automotive electronics, medical instrumentation, telecommunications, space technology, cell phones, and many other information technologies. Every hospital, school, factory, car, airplane, office, bank, and household contains transistors, microprocessors, and other semiconductor devices. The communications revolution, perhaps the defining social and economic transition of our time, is fueled by the invention of ever smaller, ever cheaper, ever faster chips. The explosive demands of the wireless, broadband Internet, and optical networking industries have crowned the communications chip as the dominant end market for semiconductors.

Advances in the semiconductor electronics industry are possible because of the continuing miniaturization of the transistor dimensions, which allows the construction of compact systems with tremendous computing power and memory. Miniaturization, in turn, is possible because of the perfection of fabrication techniques that allow the *integration* of circuits and thus the production of chips containing millions of elements per square centimeter. The foundation stone of this complex technology is silicon. Meeting the demands for these large-scale, complex, integrated circuits (ICs) continues to require technological advances in materials, processing, circuit design, characterization, testing, and standards.

The semiconductor electronics industry is outstripping the measurement capability needed for maintaining and improving U.S. international competitiveness. Important factors affected include product performance, price, quality, compatibility, and time to market. The Semiconductor Electronics Division provides the measurement capability needed to support the efforts of U.S. industry to improve its competitiveness. In order to support this effort, the Division also engages in technology development and fundamental research, making the findings available to industry.

The Division focuses the largest part of its resources on the development and delivery of measurement capability for two principal reasons: measurement capability has a very high impact on U.S. industry because it helps manufacturers address many of the challenges they face in realizing competitive products in the marketplace, and NIST is the official lead U.S. Government agency for measurements/metrology.

The Division focuses on developing measurement capability that is beyond the reach of the broad range of individual companies. Companies seek NIST's help for several reasons:

- The companies need NIST's special technical capability for measurement development.
- The companies need NIST's acknowledged impartiality for diagnosing a measurement problem affecting the industry broadly or for achieving adoption of a solution across the industry.
- The companies cannot develop the measurement capability needed by the industry broadly because they cannot individually capture the returns of the cost of development.
- Industry's quality standards require that key measurements be traceable to the national measurement reference standards that NIST maintains. This is a requirement of growing importance in export markets.

“The centrality of the semiconductor industry to development in the 21st century and to the continued technological preeminence of the United States cannot be exaggerated. That semiconductors have become fundamental to modern life is apparent. ... semiconductors have become the seminal technology, the vital core of an entire ecosystem that drives innovation and growth in all sectors of our economy.”

Semiconductor Industry Association (SIA) Annual Report 2006.

“NIST research in metrology is critical to reaching accuracy levels outlined in the International Technology Roadmap for Semiconductors. These measurement accuracy levels must be met to manufacture ever smaller circuits on tomorrow’s semiconductor chips.”

SIA applauds Congressional funding for key agencies and Focus Centers, press release, SIA, June 15, 2006.

The Division interacts and collaborates with a wide variety of companies, consortia [such as Semiconductor Manufacturing Technology (SEMATECH), Semiconductor Equipment and Materials International (SEMI), and the Semiconductor Research Corporation (SRC)], academia, and other government labs to accomplish its mission. Specific details are given in the project descriptions that follow. Work in the Division results in extensive outputs or deliverables that cover knowledge and improvements in physical understanding, test methods and measurements, Standard Reference Materials (SRMs), standards, test structures and test chips, software, measurement accuracy and traceability, publications and reports, patents and Cooperative Research and Development Agreements (CRADAs), round robins, data and models, talks and short courses, company visits, conferences and workshops, consortia participation, and various activities and leadership roles on committees and working groups.

Division staff serve the semiconductor community in leadership roles on standards committees such as Semiconductor Equipment and Materials Institute (SEMI), the American Society for Testing and Materials (ASTM), and the Electronic Industries Alliance (EIA) / Joint Electron Device Engineering Council (JEDEC), societies such as IEEE, ECS, and APS, and numerous semiconductor conferences/workshops. Many test methods and standards have been developed and written over the years by NIST staff for ASTM and EIA/JEDEC, including ones for resistivity, oxygen in silicon, thin dielectrics, electromigration, and device characterization. Staff serve on various Technical Working Groups to help put together the International Technology Roadmap for Semiconductors (ITRS). These groups are Process Integration, Devices, and Structures; Assembly and Packaging; Lithography; Interconnect; Front End Processes; and RF and Analog Mixed Signal. The ITRS provides targets for equipment, material, and software suppliers; provides targets for researchers; and serves as a common reference for the semiconductor industry.

The Division also has impacted the semiconductor community by producing a number of SRMs. To date, nearly 3,000 SRMs have been sold and distributed for resistivity, oxygen in silicon, and optical thickness by ellipsometry. Hundreds of companies throughout the world have purchased these SRMs to maintain and improve their measurement capabilities.

For the future, the Division has identified nanotechnology and its various sub-areas, including nanoelectronics, nanocharacterization, nanobiotechnology, and plastic electronics, as emerging areas of research to address. There is an increasing recognition in industry that metrology is becoming more crucial for the nanotechnology era that industry has entered.

“The semiconductor industry is rapidly reaching a point in its evolution where its ability to build smaller nodes will encounter serious difficulties in the form of quantum effects and atomic level statistical fluctuations ... nanotechnology will both help keep CMOS scaling on track and enable new materials/technology platforms that satisfy market needs better than CMOS ... as current lithography methods reach their limit, the tools used in the development, manufacture, and testing of CMOS will increasingly be based on nanotechnology.”

*- from L. Gasman,
“Why Nanotechnology Is So Important for the Semiconductor Industry,”
NanoMarkets White Paper, p. 2.*

INDUSTRY AND DIVISION RESEARCH DIRECTIONS

NANOELECTRONICS: EXTREME CMOS AND BEYOND

Moore's law (the doubling of transistor density on integrated circuits approximately every 2 years) has provided smaller, faster, and cheaper logic and memory for over 30 years. This has been driven by the ability to continue scaling the device dimensions of the CMOS field-effect transistor (FET). Most industry analysts predict that "extreme CMOS" scaling will continue to drive the industry for at least another 10 years. However, the 15 year horizon of the International Technology Roadmap for Semiconductors (ITRS) is reaching a point which challenges the most optimistic projections for the continued scaling of CMOS. Replacing or extending CMOS with emerging devices (Beyond CMOS) is an important aspect of continuing the information revolution. These possible Beyond CMOS technologies span the realm from transistors made from silicon nanowires to devices made from nanoscale molecules.

HETEROGENEOUS INTEGRATION AND UBIQUITOUS ELECTRONICS

The concept of multi-technology system-on-a-chip where optical, RF, MEMS and even molecular manipulation is performed on a CMOS platform to provide electronics with greater functionality is an increasingly important paradigm. The concept of ubiquitous electronics, such as organic electronics, in which electronics are cheaply incorporated in everyday items (clothes, packaging, etc.) is also an increasingly important paradigm.

ELECTRONIC INFORMATION

The electronics industry is continually striving to reduce manufacturing costs in order to remain internationally competitive. More efficient design and manufacturing standards can lower the cost of manufacturing and promote open markets and a level playing field. Environmental legislation is becoming an urgent priority for the Electronics Industry. Countries are rushing to enact legislation restricting substances used in the manufacture of printed circuit boards and IC chips to promote environmental and recycling efforts. Electronics suppliers must cope with compliance with these new regulations and enact standards to be used throughout the supply chain. Outsourcing has identified the need for more widely accepted manufacturing and design standards for the printed circuit board industry, and new standards need to be developed for the Semiconductor Industry. The standardization effort must continue in order for U.S. manufacturing to remain competitive.

NANOBIO TECHNOLOGY

A small but growing market already exists in the merging of semiconductor- and bio-technology. Biochips have become a focus area in biotechnology in recent years. These possibilities have not gone unnoticed by others, and major semiconductor companies and laboratories such as Agilent, Intel, Infineon, IMEC, and others have significant biotechnology research efforts underway. Our Division is working to apply micro and nanofabrication technologies to advance the state-of-the-art of single molecule measurements, single cell measurement, and DNA separations for forensic applications. Additionally, we are applying experimental and theoretical methods to advance the state-of-the art in measurements of biological and biomimetic molecules.

SEMICONDUCTOR ELECTRONICS DIVISION

ORGANIZATION

DIVISION OFFICE (812.00)

2054	SEILER, David G., Chief	2097	HARMAN, George G., Scientist Emeritus
2054	GUARIGLIA, Lori A., OM	2050	SECULA, Erik M., Information Specialist
4514	COOK, Sharon W., AO	2067	THURBER, W. Robert (GR)
2079	BENNETT, Herbert S., NIST Fellow		

ENABLING DEVICES AND ICs GROUP (812.05)

2070	GAITAN, Michael (GL)
2052	KROFT, Terri, OM

NANO-STRUCTURES FOR CD AND INTERCONNECT METROLOGY (FA)

2072	CRESSWELL, Michael W. (FL)
5026	ALLEN, Richard A.
8193	MURABITO, Christine E.
2234	SCHAFFT, Harry A. (CNR)
2182	YARIMBIYIK, Emre (GR)

METROLOGY FOR SYSTEM-ON-A-CHIP (FA)

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5484	GEIST, Jon (CNR)
2236	HOOD, Colleen E.
6018	ORTIZ, Jose (CNR)
6757	VARMA, Ankush (GR)

POWER DEVICE AND THERMAL METROLOGY

2071	HEFNER, Allen R., Jr. (PL)
8777	AKUFFO, Adwoa (CNR)
2081	DUONG, Tam (CNR)
8776	HERNANDEZ, Madelaine (CNR)
4998	HILLKIRK, Leonardo (CNR)
2236	HOOD, Colleen E.
6018	ORTIZ, Jose (CNR)
6018	RIVERA-LOPEZ, Angel (CNR)

MICRO-NANO-TECHNOLOGY (MNT)

2070	GAITAN, Michael (PL)
5026	ALLEN, Richard A.
3095	AUROUX, Pierre-Alain (CNR)
5484	GEIST, Jon (CNR)
4796	HONG, Jennifer
4710	JAHN, Andreas (GR)
2049	MARSHALL, Janet C.
4110	McGRAY, Craig (CNR)
6367	MIJARES, Geraldine I.

MICRO-NANO-TECHNOLOGY (MNT) CONT'D

2045	MORGAN, Nicole (GR)
2492	NABLO, Brian (PD)
6347	POLK, Brian
4739	RACIC, Milena (CNR)
5466	REYES-HERNANDEZ, Darwin
2506	ROBERTSON, Joey (PD)
4630	SANKARAN, Bharat (GR)
2305	SHAH, Jayna (GR)
2052	STAVIS, Sam (CNR)

NANOBIOTECHNOLOGY

5853	KASIANOWICZ, John (PL)
5787	CHAN, Elaine (PD)
4709	HROMADA, Louis (CNR)
2492	NABLO, Brian (PD)
4358	REINER, Joseph (PD)
2506	ROBERTSON, Joey (PD)
6115	RUBINSON, Kenneth (GR)
2426	MISAKIAN, Martin (GR)

WIRE BONDING TO CU/LOW-K SEMICONDUCTOR DEVICES (FA)

2097	HARMAN, George G. (FL)
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CMOS AND NOVEL DEVICES GROUP (812.06)

2247	SUEHLE, John S. (GL, Acting)
2053	JORDAN, Melissa, OM

NANOELECTRONIC DEVICE METROLOGY

2082	RICHTER, Curt A. (PL)
2078	EDELSTEIN, Monica D.
8755	GERGEL-HACKETT, Nadine (PD)
2233	HACKER, Christina
2087	KIRILLOV, Oleg
2089	KOPANSKI, Joseph
3241	LI, Qiliang (CNR)
2247	SUEHLE, John S.
3377	WANG, Wenyong (CNR)
2088	XIONG, Hao (CNR)

MACRO ELECTRONICS

2048 GUNDLACH, David (PL)
2087 KIRILLOV, Oleg
2089 KOPANSKI, Joseph
2044 NGUYEN, Nhan V.
2082 RICHTER, Curt A.
2247 SUEHLE, John S.

ADVANCED MOS DEVICE RELIABILITY AND CHARACTERIZATION

2247 SUEHLE, John S. (PL)
2078 EDELSTEIN, Monica D.
8687 GURFINKEL, Moshe (CNR)
2044 NGUYEN, Nhan V.
2088 XIONG, Hao (GR)

THEORETICAL SOLID-STATE PHYSICS FOR SEMICONDUCTORS (FA)

2079 BENNETT, Herbert S. (FL)

ELECTRONIC INFORMATION GROUP (812.07)

3644 BRADY, Kevin G. (GL)
2053 JORDAN, Melissa, OM

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8778 ARONOFF, Matthew
4951 BABOUD, Julien (GR)
5108 BERTON, Dominique (GR)
3644 BRADY, Kevin G.
2432 GRIESSER, Art
8581 KHALILI, Neda (S)
3263 KOSTICK, Jennifer A.
5319 LI, Ya-Shian
8436 MAI, Cuong (S)
2404 OTEMA, Eric (GR)
3956 SIMMON, Eric
5319 SMITH, Nathan (S)

KNOWLEDGE FACILITATION

3263 KOSTICK, Jennifer A. (PL)
4229 MARIE, Mylene (S)
8193 MURABITO, Christine E.

Legend:

AO = Administrative Officer
CNR = Contractor
FA = Focus Area
FL = Focus Area Leader
GL = Group Leader
GR = Guest Researcher
OM = Office Manager
PD = Post Doctoral
Appointment
PL = Project Leader
S = Student

Telephone numbers are:
(301) 975-XXXX, (the four-digit extension as indicated)



NANOSTRUCTURES FOR CD AND INTERCONNECT METROLOGY

GOALS

Contribute to a test-structure infrastructure relevant to state-of-the-art interconnect-system needs according to the International Technology Roadmap for Semiconductors (ITRS) Interconnect Report 2005, which states that the function of an interconnect system is to distribute clock and other signals and to provide power/ground to the circuits and systems functions on a chip; develop test-structure-based reference materials with emphasis on supplying traceable ITRS-compliant physical standards for critical-dimension (CD) and overlay metrology-tool calibration; and contribute to organizations supporting the development of interconnect materials and standards for CD and overlay metrology applications in the semiconductor industry.

CUSTOMER NEEDS

The Semiconductor Industry Association's ITRS states that it is critically important to have suitable reference materials available when a measurement is first applied to a technology generation, especially during early development of materials and process-equipment. This project is concerned specifically with ensuring a source of such reference materials to satisfy the stated need throughout the near-term years.

Each generation of ICs is characterized by the transistor gate length whose control to specifications during IC fabrication is a primary determinant of manufacturing success. The roadmap projects the decrease of gate microprocessor unit (MPU) physical gate lengths used in state-of-the-art IC manufacturing from present levels of 28 nm to 13 nm during the near-term years. Scanning electron microscopes (SEMs) and other systems used for traditional linewidth metrology exhibit measurement uncertainties exceeding specifications for these applications. It is widely believed that potentially adverse consequences can be at least partially managed through the use of reference materials with traceable linewidths with nanometer-level uncertainties. Until now, such reference materials have been unavailable because the technology needed for their fabrication and certification has not been implemented. The technology that the project has developed for fabricating CD reference materials is known as the Single-Crystal CD Reference-Material (SCCDRM) implementation.

Interconnect technology is becoming the principal factor that determines the maximum performance that can be attained with emerging generations of integrated circuits. The dramatic reversal from performance which is limited by transistor delay, to performance which is limited by interconnect delay, challenges the approach of continuing to scale the conventional metal/dielectric system to meet future interconnect requirements. Future advances in IC performance will be governed increasingly by the advances in interconnect technology, at least as much as by advances in active devices. As aluminum is replaced by hybrid copper/barrier-metal conductors, the benefits of the higher conductivity of copper are becoming problematic as a result of the predominance of contributions of the barrier metal to the effective conductor resistance. There are two mechanisms. When barrier metal, with its higher resistivity, replaces more highly conducting copper, the proportion of the total CD, which is allocated to copper, is reduced dramatically as CD is scaled. Confounding the phenomenon, higher clock speeds favor conduction by the outer regions of the composite conductor, which render it adversely non-linear. Modeling the generalized binary-metal interconnect conductors at high frequencies is therefore a central issue. This is a very complex task on which no known reports exist in the technical literature. However, we have been able to make a start on providing a tool for dealing with this issue by drawing on NIST resources in other Divisions.

Whereas there is no simple global solution to the challenge of electrical metrology for the extracting the CDs of binary-metal interconnect conductors at this time, advances being pursued by this project are likely to play a leading role. Finally, a metrology challenge that is attributable more to scaling per se, than to the materials selected for interconnect implementation, is overlay. Overlay metrology is being challenged by exacerbation of the tool- and wafer-induced shifts that are generally manageable for technology generations introduced prior to the present time.

TECHNICAL STRATEGY

For addressing customer needs in the interconnect arena, our four-part technical strategy builds on opportunities afforded by the project's unique SCCDRM experience. The same substrates that

Technical Contact:
Michael W. Cresswell

Staff-Years (FY 2006):
1.5 professionals
0.5 guest researchers

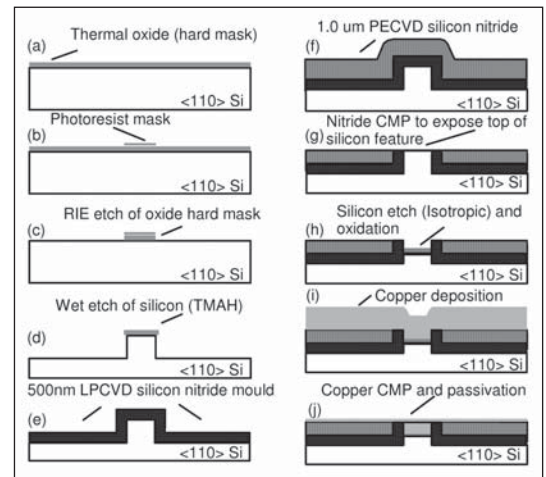
"It is critically important to have suitable reference materials available when a measurement is first applied to a technology generation, especially during early materials- and process-equipment development"

International Technology Roadmap for Semiconductors, 2005 Edition. Available online at <http://public.itrs.net/>

have been developed for CD reference-material applications are being applied to the fabrication of single-metal, initially copper-only, test structures with features having lateral dimensions in the 20 nm to 100 nm range. The novel process-flow, which has been reported in our joint paper with the University of Edinburgh at a recent conference, is illustrated in the figure (right). The approach shown enables a definitive assessment of the impact of feature-dimension scaling on the fundamental physics of electron transport in narrow features patterned from copper, without the complications resulting from having other metal species that serve as barrier layers. The information so provided enables modeling the performance of features that are replicated with copper-cored binary-metal technology and will aid in the verification of dimensional parameter extraction for process-control purposes.

We have initiated a study of the interaction of skin effect with high-resistance barrier metal alloys near the surfaces of conducting features at frequencies up to ≈ 100 GHz. This higher upper limit is driven by near-term year clock speeds having rising and falling edge components that substantially exceed 20 GHz. As mentioned above, higher clock speeds favor conduction by the outer regions of the binary-metal interconnect conductor through the so-called “skin effect” phenomenon, which renders it adversely non-linear. The technical strategy is to model the RLCG (Resistance Inductance Conductance Capacitance) parameters of a selection of binary-metal interconnect-conductor architectures over the stated range of frequencies using finite-element Maxwell software, which is available at NIST. This approach is quite ambitious, and there are no known analytical solutions for generalized binary-metal interconnect conductors. Since there is no report of such analyses in the scientific literature, we have chosen first to verify our Maxwell solutions for a selection of single-metal architectures for which analytical solutions do exist.

A class of test structures for process maintenance, where the need for innovation is driven by scaling, is overlay standards. This project has been granted a patent on an electrically calibrated test structure to serve as a process- and tool-specific overlay standard that avoids all the limitations of other approaches. The strategy is to reduce the concept to practice by replicating the test structures with a bi-level polysilicon-metal process and conduct parametrical testing.

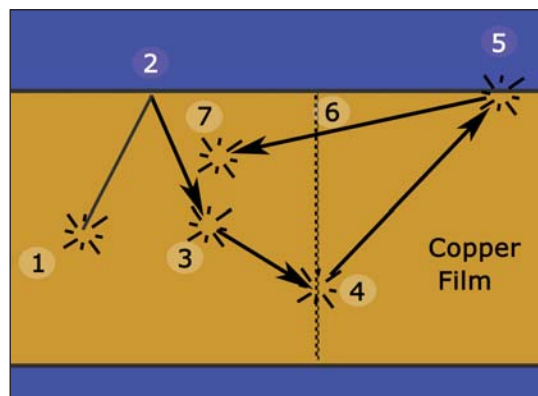


The process flow which was devised for the fabrication of single-metal, copper-only, test structures with features having lateral dimensions in the 20 nm to 100 nm range.

Among the test structures that we are fabricating for modeling-parameter extraction are strip lines for rf-testing from DC to 40 GHz, consistent with clock speeds of road-map integrated circuits over the next several years. The strategy is the computation of rf-impedance parameters from S-parameter measurements. An important spin-off from this activity is the application of rf-measurement to validating key dimensional parameters of masks which are patterned for interconnect fabrication, another application which has been sought by the mask-vendor and mask-user industries. This work will be done initially on binary masks but, if successful, will be extended to opportunities in dimensional metrology for more complex phase-shift-mask applications. Further into the future, the experience gained here may be useful for development of a non-contact electrical-CD metrology, which is understood to be of great interest to the photo-mask industry.

The 2005 ITRS relates how both grain-size and feature dimensions affect the effective resistivity of copper in the electrical wiring of integrated circuits. The consequences are of growing concern because new technologies require ever-smaller dimensions that contribute to greater resistance and power dissipation. The project strategy is to develop an easy-to-use, versatile effective-resistivity simulation program that is superior to other approaches in use for studying size effects. It shows how the scattering of electrons by surfaces, grain boundaries, and impurities increases the effective resistivity of copper in thin films and lines as dimensions approach and become shorter than the mean free path of electrons in bulk copper. In related experi-

mental work, copper films are fabricated, their sheet resistances and physical thicknesses are measured, and the predictions of the simulation program are compared to experimental results. The figure below shows the various scattering events that are included in the simulation program, reported in a recent NIST news release, to simulate size effects in copper.

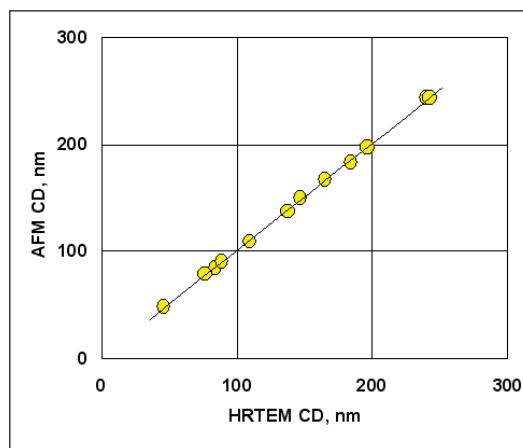


The scattering events that are included in the simulation program to simulate dimensional effects in copper.

The project is also providing technical support to JEDEC Committee JC14.2 of the JEDEC Solid State Technology Association on Wafer Level Reliability to enhance the reliability of copper interconnect implementations. This support is for revising interconnect standards, which were originally written for aluminum interconnects, so that they will be applicable to copper metallization. The primary focus is in writing a new JEDEC standard for constant current and temperature stress testing for electromigration, assisting in revising the JEDEC standard for isothermal stress testing for electromigration, assisting in preparing a new JEDEC stress test for stress voiding, and preparing JEDEC guidelines for designing stress-voiding test structures.

The fundamental SCCDRM reference-material strategy is to pattern SOI device layers with lattice-plane selective etches of the kind used in silicon micro machining, which provides reference features with quasi-atomically planar side-walls. This unique attribute is highly desirable for the intended applications, particularly if the quasi-atomically planar sidewall smoothness can be further extended to reference-feature segment lengths of up to 2 μm . Essential elements of the implementation include both bulk and SOI (Silicon on Insulator) starting silicon wafers having a (110) orientation; alignment of the reference features to specific lattice vectors; and lithographic patterning with lattice-plane selective

etches of the kind used in silicon micro-machining. However, the difficulty of obtaining satisfactory SOI material in larger diameters is driving us towards a bulk-wafer starting-material strategy. The roadmap states that measurement and certification of reference materials must be carried out using standardized or well-documented test procedures. The traceability path for dimensional certification of the project's SCCDRMs is responsive to this requirement and makes measurements of a selection of reference-feature CDs on multiple chips with both Atomic-Force Microscopy (AFM) and high-resolution transmission electron microscopy (HRTEM) imaging. The former technique is highly repeatable and of manageable cost while the latter enables a lattice-plane count that allows expression of each CD in terms of a traceable distance, which is the periodicity of silicon (111) lattice planes. However, HRTEM is totally destructive and thus is not useful for supplying reference features to end users. The project's traceability strategy thus features state-of-the-art AFM as a transfer metrology to deal with this constraint. Transfer metrology relates CDs extracted by, in this case, AFM to be traced to SI units through the construction of a so-called calibration curve. An example of such a curve is shown in the figure below.



Transfer metrology relates CDs extracted by AFM to be traced to values SI units through the construction of a so-called calibration curve.

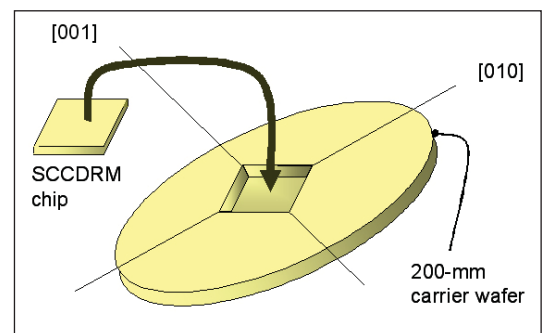
To maintain the maximum possible accuracy in the transfer-metrology operation, an elaborate reference-feature selection protocol has been established to identify reference features that qualify by virtue of their CD-uniformity, as contributors to the construction of the calibration curve, or for delivery to end users. Multiple reference features on a large set of as-patterned test chips are identified initially

by high-power optical inspection. This procedure checks primarily for continuity, cosmetics, and apparent uniformity of the narrowest-drawn of sets of six features that are incorporated into test structures, which are called HRTEM targets. Drawn feature linewidths range from 350 nm to 600 nm, and the “process bias” typically decreases these to etched CDs of between 50 nm and 300 nm. The “best” 10 % of the AFM targets passing optical inspection, and having estimated replicated CDs in the range 50 nm to 200 nm, are then SEM-imaged at 20KX to narrow the selection process further. Digitized profiles of the CDs of top-down SEM images are then extracted at 25 nm intervals. The measurements are transferred to a database, which is then interrogated to identify chips, and the AFM targets on them, that have more uniform SEM-CD profiles at the narrower CDs – typically less than 150 nm. Candidate AFM targets so identified on each chip are then CD-profiled by AFM. Chips having AFM targets with all six features having superior uniformity are then partitioned into a *calibration* sub-set and a *product* subset. All six features of the selected targets on the chips on the calibration sub-set are then subjected to HRTEM imaging. These are the chips whose designated AFM targets are to be used as contributors to the calibration curve. The design of all HRTEM targets enables the capture of six HRTEM images in a single dual-beam FIB-and-thinning operation. Since such operations are very costly, this capability is economically advantageous. Moreover, since the features on each target are designed such that they are systematically staggered in CD by increments of 30 nm, HRTEM inspection of a single target enables the generation of a 6-point calibration curve spanning a 150 nm range.

Since 200 mm (110) starting material, which is preferred by end-users in industry, is unobtainable at an acceptable cost, this project’s technical strategy has been to dice each 150 mm (110) wafer after lithography and to mount the separate chips in micro-machined standard 200 mm carrier wafers to accommodate the product reference-feature chips. The scheme is shown in the figure (right). The result is that finished units are rendered metrology-tool-compatible at an acceptable cost.

The project’s technical strategy in reference materials is now evolving in the ways listed below. In summary, it is responding to industry push to implement measures that make the SCCDRMs more compatible with end-user requirements. These activities include:

- replacing the carrier-wafer with a monolithic 200 mm wafer implementation
- replacing the buried oxide of SOI wafers with a buried boron diffusion having an epitaxial silicon layer deposited over it
- further reducing the CDs of calibrated features to 20 nm and the uncertainties of the calibrated CD to less than 1.0 nm through systematic process-refinement experiments
- improving the reference feature’s CD uniformity to enable certifying the CD of an extended length
- improving on-wafer navigation for the end user convenience
- calibrating a selection of optical-CD (OCD) gratings that are replicated at the same time as the isolated lines that have been supplied so far
- improving management of the organic residues that sometimes impair the cosmetic appearance of the reference features and their environment on the wafer and to some extent adversely affect the uncertainty values of the delivered product
- exploring the potential of OCD gratings patterned with SCCDRM technology to assess the uncertainty and usefulness of this implementation
- conducting extensive studies of the wafer processing and identifying which process parameters provide superior cross-section uniformity and narrowness



The technical strategy has been to dice each 150 mm (110) wafer after lithography and to mount selected chips in micro-machined standard 200 mm carrier wafers to accommodate the product reference-feature chips.

Implementing these aggressive measures requires wafer-processing facilities that require innovative teaming with other laboratories. Our strategy takes a page from the roadmap that explicitly states that standards institutions need rapid access to state of the art development and manufacturing capability to fabricate relevant reference materials. Likewise, the roadmap states that metrology, process, and standards research institutes, standards organizations, metrology tool suppliers, and the university community should continue to cooperate on standardization and improvement of methods and on production of reference materials.

DELIVERABLE: Report results of modeling the distributed resistance and capacitance values of interconnect conductors that can be simulated by both analytical solutions and a commercial Maxwell solver.

DELIVERABLE: Fabricate and test chemically stable test structures having copper-only features and make electrical-CD (ECD) measurements.

DELIVERABLE: Report initial electrical measurements made on second-generation SCCDRM test structures that have been converted to single-crystal nickel-silicide.

DELIVERABLE: Design, model, fabricate, and test a selection of co-planar waveguide test structures on chrome-on-glass photo-masks to evaluate the efficacy of developing a non-contact ECD method for sampling printed features.

DELIVERABLE: Conclude and report on the screening experiment to identify which combinations of six pattern-transfer process factors drive down reference feature CDs and their uncertainties.

DELIVERABLE: Fabricate and conduct AFM metrology of trenches patterned into (110) SOI device layers for their evaluation as micro fluidic channels for MEMS-based bio-applications.

DELIVERABLE: Devise and demonstrate a hybrid optical-e-beam-direct-write lithography-process to pattern of a selection 100 mm or 200 mm bulk-silicon (110) wafers with SCCDRM test structures with CDs at or below the 20 nm level.

DELIVERABLE: Design a test chip for, and apply 193 nm lithography to the patterning of, a selection of 200 mm bulk-silicon (110) wafers with SCCDRM test structures having reference-feature CDs at or below the 20 nm level.

DELIVERABLE: Extend tests and analyses for the evaluation SEM-CD measurements as a SCCDRM transfer metrology.

DELIVERABLE: Fabricate and SEM-inspect a large selection of OCD grids patterned on SCCDRM wafers as an OCD reference material.

DELIVERABLE: Initiate the implementation of a plan to fabricate and calibrate a selection of isolated-line CD-SRMs.

ACCOMPLISHMENTS

■ This project, in collaboration the NIST Precision Engineering and Statistical Engineering Divisions, has recently designed and implemented a screening experiment to identify which combinations of six pattern-transfer process factors drive down SCCDRM (Single-Crystal CD Reference-Material) reference-feature CDs and their uncertainties. Initial results include CD reductions to 25 nm with superior uniformities.

■ SCCDRM chip layouts have been designed for three new fabrication ventures featuring 200 mm wafer monolithic implementations. One of these is for a new hybrid optical/e-beam-direct-write process designed to reduce CDs to below 20 nm. Another is to take advantage of an offer by SEMATECH to collaborate on the fabrication of a new generation of SCCDRMs using state-of-the-art 193 nm lithography. The third is to respond to an interest expressed by other NIST operating units to sponsor a joint SRM venture.

■ Our SCCDRM implementation is well suited to the fabrication of calibrated reference materials for the emerging metrology known as optical-CD (OCD). We have now accomplished the first-ever fabrication and extensive inspection by SEM of gratings suitable for this purpose.

■ A paper that describes a new simulation program and its use to study the effects of surface and grain-boundary scattering on the effective resistivity of copper in thin planar films and small cross-section lines was completed. The paper was published by the Microelectronics Reliability journal in July 2006.

■ Project staff completed for publication a new JEDEC standard for electro-migration stress testing with constant current and temperature.

■ Project staff prepared a comprehensive manuscript on second-generation SCCDRM reference-materials for publication as the lead article in the May-June 2006 issue of the NIST Journal of Research.

■ As a result of close extended collaboration with the University of Edinburgh, the project has been able to develop and report a unique copper damascene process for the fabrication of a scaled electrical-CD test structure having copper-only features. The purpose is to facilitate studies of electron transport in pure copper without having to correct for the complexities of the interaction of copper with barrier-metal films. This implementation enables the separation of the effects of surface

“A great team effort. Quality is high to be able to achieve multiple (6) linewidth standards certified to about a 1 nm uncertainty.”

IBM response to 2006 survey sent by the Office of Microelectronics Programs.

“The semiconductor fabrication engineer who is responsible for metrology perennially struggles to determine whether his tool — be it an atomic force microscope (AFM), SEM or anything else — is properly calibrated. This requires a highly dependable, traceable linewidth standard, which is something that is not always easily available.”

A. Braun, Linewidth Standard to Calibrate AFMs, SEMs and OCD Tools, Semiconductor International, August 1, 2006.

and grain-boundary scattering, as a function of the cross-section dimensions of the conductor by electrical testing. Our joint paper describing the accomplishment was presented at the ICMTS 2006 conference in Austin, Texas, on March 8, 2006.

■ In close collaboration with the Laboratory for Interconnect and Packaging at the University of Texas at Austin, test structures for the investigation of the effect of linewidth scaling on electron transport in nickel mono-silicide features have been designed and fabricated. The features were patterned on (110) silicon-on-insulator wafers with i-line lithography that replicated test structures from which voltage/current (V/I) measurements could be extracted. Subsequently, the patterning of single-crystal features with direct-write electron-beam lithography has been developed in order to facilitate future reduction of the linewidths of NiSi features, which have a highly controlled surface microstructure, to linewidths below 40 nm. Our joint paper illustrating these results was also presented at the ICMTS 2006 conference in Austin, Texas, on March 8, 2006.

■ Work has continued on a new CD metrology based on coplanar waveguide test structures. Extensive e-m field modeling of characteristic impedance and distributed capacitance, which we have conducted in collaboration with the Department of Electrical and Computer Engineering at George Washington University, indicates that the extraction of these values from S-parameter measurements can be applied to sampling CDs of test-structure features that are printed on photomasks. At this time, the design of a set of thru and de-embedding structures has been designed, and a supplier of the substrate has been identified. Our joint abstract on the results has been accepted for presentation at the SPIE Bay Area Chrome-Users Symposium in September 2006. It now seems possible that coplanar waveguide test structures may provide a means of extracting electrical and dimensional information of copper interconnect features fabricated with barrier-metal coatings.

■ A new JEDEC standard, JESD202, was completed and published in March 2006. The standard describes an accelerated stress test method for determining sample estimates and their confidence limits of the median-time-to-failure, sigma, and early percentile of a log-normal distribution, which are used to characterize the electromigration failure-time distribution of equivalent metal lines subjected to a constant current-density and temperature stress. Procedures are provided to analyze complete and singly, right-censored failure-time data.

■ The computer-aided design (CAD) of a new test chip for the fabrication of test structures that can be electrically calibrated to serve as an overlay reference material for high-density interconnect fabrication has been completed. A program to simulate and validate the calibration of the standard has been applied to the design, and the fabrication of a wafer-lot has been initiated.

■ In collaboration with NIST operations in Boulder, Colorado, we applied Maxwell software to the calculation of RLGC parameters of cylindrical copper conductors with diameters ranging from 50 nm to 5000 nm, which were coated with TaN barrier metal of thicknesses typical of state-of-the-art IC-interconnect applications. At frequencies above 10 GHz, significant increases in resistance were observed as a consequence of the skin-effect induced amplification of transmission losses caused by barrier-metal coatings. A selection of these results have now been compared with those obtained for copper-only wires that were obtained from exact solutions of Maxwell-based Bessel equations. Initial results indicate close comparisons for the cases that have so far been compared.

FY OUTPUTS

COLLABORATIONS

We are interacting with the staff of the ISMI Subsidiary of SEMATECH, who have invited us to share space on their new “CMAG6” reticle for their SVGL 193 nm Step-and-Scan lithography tool to fabricate an advanced generation of SCCDRMs for distribution to the member companies, as well as for possible calibration and distribution from NIST as SRMs. Our most-recently initiated joint activity is automated SEM image analysis for calibrating OCD gratings.

The Scottish Microelectronics Centre at the University of Edinburgh (SMC) is continuing to work with us on a selection of the project’s wafer-fabrication needs, especially i-line lithography and damascene-copper processing. This collaboration continues to generate multiple joint publications.

Our collaboration with two senior professors and their graduate students at the Electrical Engineering and Computer Sciences Department at George Washington University contributes special expertise in rf test-structure design, microwave parameter extraction from network-analyzer measurements, and the physics of modeling electron transport in metallic nanostructures.

We interact very regularly and closely with NIST’s MEL, Physics, and ITL Laboratories. We share an ongoing intramural ATP program to reduce the certified CDs and uncertainties of SCCDRMs through fabrication refinements with ITL and MEL.

A new collaboration with the Microelectronics Research Center Department at the University of Texas at Austin has resulted in the transformation of narrow SCCDRM features to silicide material. They are also contributing very desirable ultra-narrow-line lithography for our next-generation SCCDRM fabrication.

STANDARDS COMMITTEE PARTICIPATION

Electrical Test Structures Task Force, Co-chair (Richard A. Allen)

SEMI International Standards Micro-lithography Committee, member (Richard A. Allen)

JEDEC JESD33B standards (Harry A. Schafft)

PRESS RELEASE

“NIST Unveils Atom-based Standards for Measuring Chip Features Under 50 Nanometers,” NIST News Release, February 24, 2005.

RECENT PUBLICATIONS

E. Yarimbiyik, H. A. Schafft, R. A. Allen, M. E. Zaghloul, “Modeling and Simulation of Nanometer Scale Copper Resistivity,” IEEE Device and Materials Reliability, Vol. 46, No. 7, pp. 1050-1057 (01-JUL-2006)

E. Yarimbiyik, H. A. Schafft, R. A. Allen, M. Zahgoul, D. L. Blackburn, “Implementation of Simulation Program for Modeling the Effective Resistivity of Nanometer Scale Film and Line Interconnects,” NIST Interagency/Internal Report (NISTIR) 7234, (01-FEB-2006)

R. G. Dixon, R. A. Allen, W. F. Guthrie, M. W. Cresswell, “Traceable Calibration of Critical-dimension Atomic Force Microscope Linewidth Measurements with Nanometer Uncertainty,” J. Vacuum Sci. Technol. B, Vol. 23, No. 6, pp. 3028-3032 (30-NOV-2005)

M. W. Cresswell, R. G. Dixon, W. F. Guthrie, R. A. Allen, C. E. Murabito, B. Park, J. V. Martinez, A. Hunt, “Critical Dimension Reference Features with Sub-Five Nanometer Uncertainty,” SPIE 30th International Symposium Micro-lithography, Metrology, Inspection, and Process Control, Feb 27, 2005 to Mar 04, 2005, San Jose, California, Vol. 5752, pp. 288-303 (30-MAY-2005)

R. A. Allen, A. Hunt, C. E. Murabito, B. Park, W. F. Guthrie, M. W. Cresswell, “Extraction of Critical Dimension Reference Feature CDs from New Test Structure Using HRTEM Imaging,” ICMTS IEEE International Conference on Micro-electronic Test Structures, Apr 04-07, 2005, Leuven, Belgium, 6 pp. (18-APR-2005)

M. W. Cresswell, B. Park, R. A. Allen, W. F. Guthrie, R. G. Dixon, W. Tan, C. E. Murabito, “Comparison of SEM and HRTEM CD-Measurements Extracted from Monocrystalline Test-Structures Having Feature Linewidths from 40 nm to 240 nm,” ICMTS 2005 International Conference on Microelectronic Test Structures, Apr 04-07, 2005, Leuven, Belgium, Select State, 6 pp. (18-APR-2005)

M. W. Cresswell, R. A. Allen, R. G. Dixon, W. F. Guthrie, C. E. Murabito, B. Park, J. V. Martinez, “Report of Investigation of RM 8111: Single-Crystal Critical Dimension Prototype Reference Materials,” (02-MAR-2005)

METROLOGY FOR SYSTEM-ON-A-CHIP (SoC)

Technical Contact:

A. R. Hefner, Jr.
M. Y. Afridi

Staff-Years (FY 2006):

1 professional
1.75 guest researchers
0.5 students

“... the trend toward digitisation notwithstanding, the analogue content of SoCs is likely to increase.”

Ron Wilson, *Electronic Design News (EDN)*, 2006

GOALS

One of the key metrology issues confronting the semiconductor System-on-a-Chip (SoC) industry is the development of measurement methods and standards for characterizing embedded-sensor (ES) Virtual Components (ES-VCs), a critical class of building blocks from which SoCs are developed. The goal of this project is to promote and support the development of hardware and software standards for specifying ES-VCs compatible with the SoC integration methodology used for digital IC design. This goal has been extended to include SoC compatibility with the IEEE 1451 series of sensor communication network standards at the request of one of the project sponsors.

This NIST effort will enable ES-VCs to be included in SoC computer-aided design (CAD) libraries and enable integration of ES-VCs with the existing digital VCs used ubiquitously by industry to design large ICs. The methods and standards developed as a result of this work will be essential for the realization of integrated, low-cost, smart homeland security and environmental sensor systems. One focus is on delivering standards to facilitate the incorporation of multi-technology (MT) VCs including MEMS (Micro-Electro-Mechanical Systems)-based VCs into SoCs.

The project activities include the development of: multi-technology hardware description language (HDL) models, VC interface standards, synthesis and scaling standards for ES-VCs compatible with digital methodologies, testing standards, verification standards, and high-level models of system components. The NIST MEMS-based integrated gas-sensing VC is used as a test bed to demonstrate the viability of these standards. In addition, the demonstration of general purpose gas-sensing VC methodologies is used to facilitate the adoption of these MT-VCs into new Homeland Security and industrial applications.

CUSTOMER NEEDS

Recent advances in high density CMOS integration and the ability to co-integrate MEMS-based sensor devices enable cost effective complex system designs fabricated on a single chip. The need for standards arises when the SoC is designed using IP (Intellectual Property) cores from multiple vendors. These cores must be compatible for design success, thus demanding standards in the area of

interoperable interfaces, models, and verification strategies for multi-technology SoC designs.

The SoC design challenges include managing increasing system complexity, achieving system-level verification, and bridging the separate disciplines of system architecture and chip design. These challenges are being overcome with the use of platform-based design approaches that emphasize design reuse; *i.e.*, the development of ES-VCs that can be used as cost-effective building blocks for SoC devices and standards for ES-VC IP interoperability with the SoC design flow.

One set of customers for this infrastructure building will be the makers of system design software, ES-SoC IP designers, SoC manufacturers, and systems designers. This is generally recognized by the chip designers, manufacturers, and electronic design automation (EDA) tool developers:

- *“What is the most recent development that promises to truly enable a system on a chip? It is the ability to combine CMOS and MEMS structures into one process flow.”*

- Randy Frank and Dave Zehrbach, Motorola, in *Sensors Online*

- *“Definitely, System-on-a-chip is the driving paradigm in our space, and there are some fundamental differences in culture and engineering mentality as well as some new technical skills that need to be developed in engineering. At the highest level, system-on-a-chip implies that you need to think like a system designer but implement like a chip designer, and those traditionally have been different disciplines...”*

- Shane Robison, Executive Vice President of Engineering, Cadence Design Systems, Inc., EDAcase.com

Another set of customers for ES-VC SoCs are the ultimate users of these chips. Compatibility with existing and emerging sensor communication standards such as IEEE 1451 will be essential so that the SoCs can be utilized in law enforcement and homeland security applications.

TECHNICAL STRATEGY

To successfully develop ES-VCs for SoC design methodology, the first step in this multi-step process is to develop the ability to make the ES-VC devices via a standard CMOS compatible process. To exercise this capability we have chosen a MEMS microhotplate-based embedded gas-sensor,

including operational amplifiers, decoders, and an analog-to-digital converter (ADC), and a microcontroller for control and data processing.

The second step is to make ES-VCs compatible with the standard digital SoC design methodology. This approach will require ES-VC to incorporate digital interface circuitry and to have the DFT/BIST (Design For Test/ Built-In Self Test) functionality required by SoC standards. To facilitate this approach we will develop methodologies and standards for adding digital shells to ES-VCs and demonstrate them on the gas-sensor VC described above.

DELIVERABLE: Develop and fabricate a fully digital gas-sensor VC in a standard CMOS 0.5 μm technology to demonstrate a standard digital interface and SoC Design-For-Test functionality.

The predominant design approach used by industry for SoC devices is top-down design. This requires that high-level models (in SystemC/HDL) exist for the VCs that are candidates for use in any particular system of interest. Compared to those for digital VCs, the methodology and standards for developing high-level models for ES-VCs are at best poorly developed. To address this need, high-level models are being developed for ES-VCs using Analog and Digital Hardware Description Languages and higher-level system description languages such as SystemC. We are also developing methodologies to validate these models. The digital systems industry has standards set by organizations such as OCP-IP, VSIA, and OSCI to foster large-scale interchange and interoperability of modular digital IP, and we believe that such standards in the ES-VC field are a key factor for the growth of an ES-VC IP industry.

DELIVERABLE: Compare high-level model simulation results for microhotplate-based gas-sensor ES-VCs with measured data from a fully digital ES-VC.

The synthesis process is well defined for the digital SoC design and is well supported by a large number of design libraries. Currently the libraries, methodology, and standards for ES-VC synthesis do not exist. We are developing standards and metrologies for ES-VCs that will be compatible with standard digital synthesis tools.

DELIVERABLE: Synthesize and fabricate a microcontroller IP core with an IEEE 1451 compatible interface in a standard 0.25 μm CMOS process VC.

DELIVERABLE: Develop methodology and standards to allow ES-VC to be synthesized by standard MT-synthesis tools and demonstrate their viability via our microhotplate gas-sensor VC.

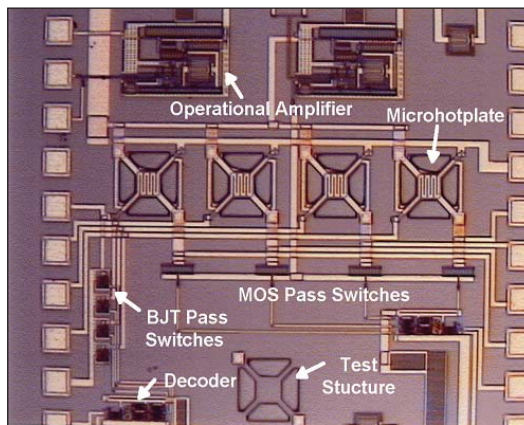
Scaling digital circuitry is a key capability used by digital designers to reduce costs and ensure compatibility with different fabrication technologies. Since most systems that would use ES-VCs will be predominantly digital, it is important that there be an equivalent scaling capability for the ES-VCs. To address the need for scaling ES-VCs, we are developing metrologies for digital-compatible scaling processes.

DELIVERABLE: Develop methodologies and standards for an equivalent ES-VC scaling approach and demonstrate its viability via our microhotplate gas-sensor technology.

The testability of ES-VCs represents another significant challenge since standards and methodologies for non-digital circuits do not exist. The most promising approach to address testability is to use BIST techniques. To facilitate this approach, we will develop methodologies and standards for adding BIST to ES-VCs and interface with them via the digital shell.

DELIVERABLE: Develop methodologies for built-in self test of ES-VC devices and demonstrate their viability via our microhotplate gas-sensor technology.

NIST is a natural home for this work because NIST has advanced measurement capabilities across the spectrum of sensor technologies.

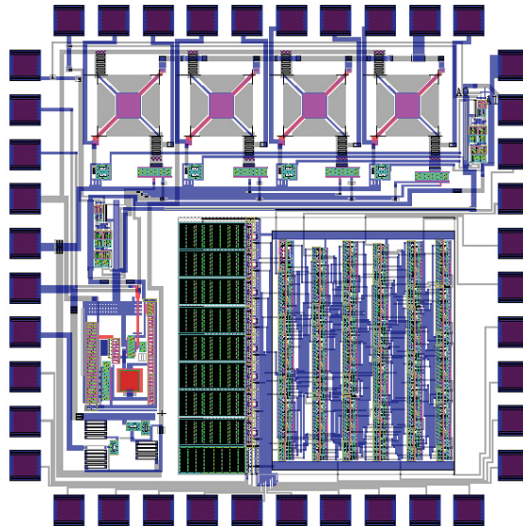


Micrograph of gas-sensor system to be used as demonstration vehicle.

ACCOMPLISHMENTS

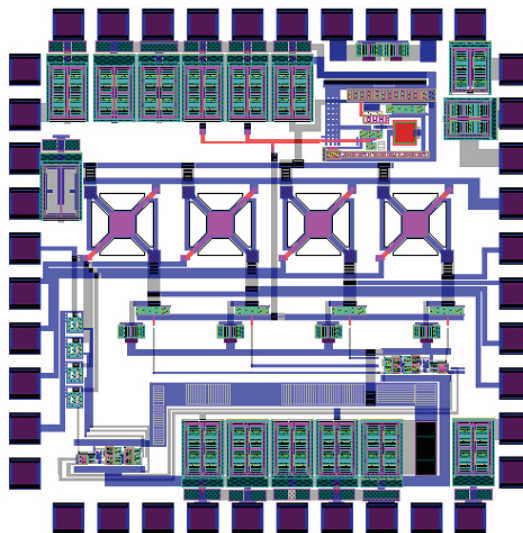
- Investigated existing and emerging SoC design methodologies and adapted digital SoC design tool-flow to enable integration of mixed-signal MEMS VCs.
- A four element gas-sensor VC was successfully designed, fabricated, and electrically characterized to demonstrate that the design approach

was compatible with SoC design methodology. The performance of the 8-bit analog-to-digital converter (ADC) exceeded the gas-sensor VC design requirements.



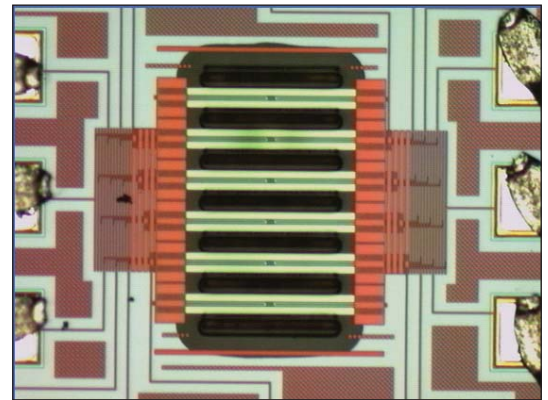
Layout of the four element gas-sensor VC with analog-to-digital control.

■ Electrostatic discharge (ESD) protection structures were added to the gas-sensor and successfully tested. These ESD test structures are based on multi-finger thyristor-type devices and are designed to achieve optimum performance and reduced area.



Layout of the four element gas-sensor VC with electrostatic discharge (ESD) protection circuitry.

■ A new post-process etching technique was developed to integrate MEMS devices with standard submicron CMOS processes and a new microhotplate design that scales with standard CMOS structures and voltage levels. This will enable co-integration of MEMS sensor devices with high density submicron digital systems using cost effective standard CMOS foundries. The submicron gas-sensor test chip was characterized. Characterization data showed the new scalable microhotplate will provide the temperature required for gas-sensor operation at 3.3 V.



New microhotplate design implemented in standard submicron CMOS technology.

■ Methodologies for designing digital interface shell functionality for ES-VCs were developed and demonstrated by designing the gas sensor SoC architecture.

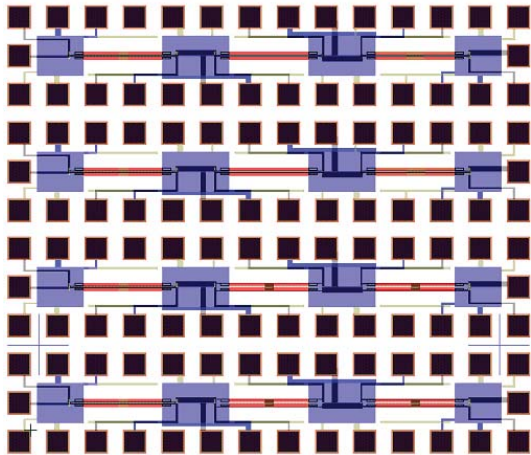
■ A high-level model of the microhotplate gas sensor ES-VC was developed. A HDL-based microcontroller core was synthesized for a 0.25 μm standard CMOS fabrication process. High-speed SystemC models of the microcontroller and microhotplate were developed to facilitate SoC software design and protocol development. This is the first time a MEMS device has been modeled in SystemC, and the results demonstrated the importance of including MEMS-device models in high level system modeling

■ Microhotplate-based gas-sensor yield was improved by adopting a new chromium etchant.

■ A computer-controlled gas-delivery system was designed, assembled, and tested. The gas delivery protocols for calibrating the microhotplate-based gas sensors were designed and implemented.

■ A submicron-microhotplate test-structure chip was designed to compare the performance of different CMOS compatible temperature sensors and

to measure the contact resistance between different types of post-processed gas sensor electrodes. This chip also supports the extraction of more accurate microhotplate thermal-model parameters.



Layout of new microhotplate test-structure chip with different types of temperature sensors and four point electrodes for gas-sensor film contact-resistance studies.

FY OUTPUTS

RECOGNITION

2005 George Abraham Outstanding Paper Award:

Y. Afridi, A. Hefner, C. Ellenwood, R. Cavicchi, and S. Semancik "Characterization System for Embedded Gas-sensor Systems-on-a-Chip," GOMACTECH 2005, pp. 94-97, 2005.

RECENT PUBLICATIONS

J. Salcedo, J. J. Liou, M. Y. Afridi, A. R. Hefner Jr., "On-Chip Electrostatic Discharge Protection for CMOS Gas Sensor Systems-on-a-Chip (SoC)," IEEE J. Solid State Circuits, Vol. 46, No. 8, pp. 1285-1294 (01-AUG-2006)

J. Geist, M. Y. Afridi, A. Varma, A. R. Hefner Jr., "Simple Thermal Efficiency Model for CMOS-Microhotplate Design," Journal of Research (NIST JRES), Vol. 111, No. 3, pp. 243-253 (31-MAY-2006)

M. Y. Afridi, A. R. Hefner Jr., C. H. Hood, R. E. Cavicchi, S. Semancik, "Characterization System for Embedded Gas Sensor Systems-on-a-Chip," GOMAC Digest of Technical Papers, GOMACTech, Apr 04-07, 2005, Las Vegas, Nevada, pp. 94-97 (01-DEC-2005)

M. Y. Afridi, A. R. Hefner Jr., J. Geist, C. E. Hood, A. Varma, B. Jacob, "Microhotplate-Based Sensor Platform for Submicron SoC Designs," 2005 International Semiconductor Device Research Symposium, Dec 07-09, 2005, Bethesda, Maryland, pp. 260-261 (09-DEC-2005)

J. A. Salcedo, J. J. Liou, M. Y. Afridi, A. R. Hefner Jr., "Novel Electrostatic Discharge Protection Structure for a Monolithic Gas Sensor Systems-On-A-Chip," Proc., Conference Proceedings - IEEE International Symposium on Circuits and Systems, IEEE International Symposium on Circuits and Systems, May 23-26, 2005, Kobe, Japan, (01-MAR-2005)

POWER SEMICONDUCTOR DEVICE AND THERMAL METROLOGY

Technical Contact:
A. R. Hefner, Jr.

Staff-Years (FY 2006):
1.0 professional
4.8 contractors

"In 2002, Dr. Calvin Carter of Cree Inc. received the US National Medal of Technology from President George W. Bush for: "his exceptional contributions to the development of Silicon Carbide wafers, leading to new industries in wide band-gap semiconductors and enabling other new industries in ... more efficient/ compact power supplies, and higher efficiency power distribution/transmission systems."

GOALS

The goals of the project are to (1) develop electrical and thermal measurement methods and equipment in support of the development and application of advanced power semiconductor devices and (2) develop advanced thermal measurements methods and standards for characterizing integrated circuits (ICs) and devices.



Allen Hefner, Jr., performs high-speed, high-voltage silicon carbide device characterization using NIST-developed, specialized equipment. Copyright Robert Rathe

CUSTOMER NEEDS

The electronics industry faces significant technical challenges in developing more thermally efficient ICs and power semiconductor devices. Power consumption and heat removal within IC devices are becoming critically important as expressed in the 2005 ITRS: *"Power consumption is now the major technical problem facing the semiconductor industry. As feature sizes shrink below 0.1 micron, static power is posing new low-power design challenges."* The need for efficient power semiconductor devices stems from a range of application requirements including more efficient switch-mode power supplies for computers and consumer appliances, to motor drives for electric automobile and higher power traction applications, and finally to more efficient power generation, transmission, and distribution.

Recent advances in single crystal SiC material and fabrication technology have ushered in a new era of wide band-gap power semiconductor devices. This has led to the commercialization of SiC power Schottky diode products in the 400 V to 1200 V range and to the development of High-Voltage, High-Frequency (HV-HF) power devices with 10 kV, 20 kHz power switching capability. The emergence of HV-HF devices with such capability is expected to revolutionize power distribution and conversion by extending the use of switch-mode power conversion technology to high voltage applications. With the introduction of this new SiC power device technology comes new requirements for metrology and standards that are being addressed by NIST.

NIST is playing a lead role in industry and government programs to accelerate the development and application insertion of SiC power devices. The Defense Advanced Research Projects Agency (DARPA) Wide-Band-gap Semiconductor Technology High Power Electronics Program (WBST-HPE) is developing power semiconductor modules with 15 kV, 110 A, 20 kHz switching capability. The recently announced WBST-HPE Phase 3 effort (www.darpa.mil/baa/baa06-30.html) anticipates that this semiconductor technology will enable the HV-HF switching required for a Solid State Power Substation (SSPS) in future Naval aircraft carriers. The Electric Power Research Institute (EPRI) seeks to utilize SiC power devices for advanced distribution automation using solid-state distribution transformers. The Department of Energy has also recently identified HV-HF power devices as an enabling technology for future alternative energy sources and power plants.

While overcoming thermal limitations has always been at the forefront of power semiconductor technology, this has only recently become a critical issue for IC devices. The major issues include: (1) power levels in CPUs have reached the same levels as in power devices; (2) high-performance IC Functional Unit Blocks (FUBs) are leading to non-uniform dynamic heating of IC chips; and (3) shrinking dimensions and increasing operating frequencies of ICs are causing significant power dissipation in the interconnects. The ITRS 2005 states that *"there is strong need to establish industry wide transient thermal measurement technique standard."* NIST is addressing these

needs by developing methods for measuring static and dynamic temperature distribution of IC and power devices, as well as methods to calibrate the measurement systems.

TECHNICAL STRATEGY

The NIST strategy is to support the measurement infrastructure of the semiconductor industry by developing and evaluating measurement methods and standards where suitable ones do not exist for characterizing critical electrical and thermal properties of power devices and ICs. This includes electrical, thermal, and safe operating limit characterization, establishing performance metrics, and developing methods for extracting device model parameter data to aid in application insertion. NIST is also playing a leadership role in industry and government programs to accelerate the development and application insertion of SiC power devices.

SUPPORT PROGRAMS TO DEVELOP HV-HF SEMICONDUCTOR DEVICES AND APPLICATIONS

A major driving force spearheading the development of HV-HF power devices is the ongoing DARPA WBST-HPE program focused on developing the technology deemed necessary to enable a SSPS for future Navy warships. Substantial benefits in power quality enhancement, advanced functionality, size, and weight are anticipated by replacing the conventional transformer (6 ton, 13.8 kV, 2.7 MVA) with an all solid state design. NIST played a key role in WBST-HPE Phase 1 and has been selected to be the exclusive device and package evaluation and metrology lab for the Phases 2 and 3 programs for 2005 through 2008.

DELIVERABLE: Participate in planning future government and industry high power generation, transmission, and distribution programs enabled by emergence of HV-HF power semiconductor devices including WBST-HPE Phase 3, EPRI Intelligent Universal Transformer Program, and the DOE Fuel Cell Power Plant program.

METROLOGY HIGH-VOLTAGE HIGH-FREQUENCY SWITCHING DEVICE PERFORMANCE

The emergence of HV-HF power devices presents unique challenges in metrology and specification of device electrical and thermal requirements. NIST has recently developed unique world-class laboratory facilities for characterization of HV-HF SiC power switching devices including: a) 25 kV variable-pulse-width curve tracer, b) 15 kV 100 A 50 ns inductive and resistive load switching tester,

c) 4 kV, 80 A, 10 ns diode reverse recovery tester, d) pulsed and multi-channel long term diode forward current stress and monitoring systems, e) high-speed high-power Temperature Sensitive Parameter (TSP) module package measurement system, and f) rapid thermal cycling/shock module package stress system.

DELIVERABLE: Apply NIST high-voltage, high-frequency power device test systems to evaluate the performance the 10 kV, 100 A, 50 ns half-bridge power modules produced by the DARPA WBST-HPE program and assess the potential for enabling advance commercial and military power distribution systems.

METROLOGY FOR SiC DEVICE DEGRADATION AND RELIABILITY

Although significant progress has been made in improving the quality of the SiC starting material and the fabricated devices, a major concern for devices with minority carrier injection is the degradation in the electrical characteristics after prolonged forward bias conduction. The degradation occurs from latent material defects such as Basel Plane Dislocations (BPDs) that result in the formation and growth of stacking faults activated by excess-carrier recombination. NIST has recently developed automated stress and degradation monitoring systems to assess degradation of SiC devices. The monitoring methods include forward conduction voltage drop, switching reverse recovery characteristics, and pulsed thermal imaging of current uniformity.

DELIVERABLE: Use NIST forward-bias stress and degradation monitoring systems to assess progress of WBST-HPE program in producing degradation-free PIN diodes using Low-BPD technology.

DELIVERABLE: Develop a long term application-like 20 kHz switching test system to evaluate HV-HF application reliability and use to evaluate reliability of DARPA WBST-HPE.

SiC POWER DEVICE MODELS FOR HV-HF POWER CONVERTER SIMULATION

Accurate and robust circuit simulator models for HV-HF semiconductor devices are needed to evaluate the impact of the new semiconductor technology on power converter system performance. NIST develops the generic physics-based models for the SiC power semiconductor devices that are provided in commercial circuit and system simulation software. In addition, NIST also develops model parameter extraction methods needed to measure the physical and structural parameters of specific devices. The NIST model parameter extraction

“Power consumption is now the major technical problem facing the semiconductor industry. As feature sizes shrink below 0.1 micron, static power is posing new low-power design challenges. ITRS predicts a decrease in dynamic power per device over time. However, the doubling of on-chip devices every two years would force an increase of current leakage on a per-chip basis.”

International Technology Roadmap for Semiconductors, 2005 Edition. Available online at <http://public.itrs.net/>.

“As the thermal resistances are made smaller and smaller for high power devices, thermal metrology with better resolution and capabilities is required. For example there is strong need to establish industry wide transient thermal measurement technique standard.”

International Technology Roadmap for Semiconductors, 2005 Edition. Available online at <http://public.itrs.net/>.

tools have recently been used to characterize SiC power MOSFETs and diodes introduced by the DARPA WBST-HPE Phase 2 program, and the models were used to predict the performance of the Phase 3 SSPS.

DELIVERABLE: Collaborate with industry and government programs to simulate the performance of HV-HF devices in power conversion system applications.

DEVELOP THERMAL METROLOGY FOR POWER SEMICONDUCTOR PACKAGE AND COOLING SYSTEM

High speed TSP measurements are required for in-situ evaluation of the heat transport through the interface of multi-layer package systems. Recently NIST developed a high speed transient thermal impedance system using a TSP for multi-chip power modules. This enables assessment of die attach and voltage isolation layer attach degradation after thermal cycling and thermal shock stress. This system also enables validation of electro-thermal device models needed for electrical and thermal system design.

DELIVERABLE: Perform thermal cycling and thermal shock stress on DARPA Wide-Bandgap High Power Electronics program devices and American Competitiveness Institute ManTech devices. Use unique NIST high speed, high current TSP system to evaluate die attach and voltage isolation layer attach integrity before and after thermal stress.

HIGH-SPEED THERMAL IMAGE MICROSCOPY FOR CHIP SURFACE TEMPERATURE

A limitation of commercially available infrared (IR) thermal imaging systems is their inability to make high speed transient measurements. NIST has modified a commercial IR system to enable measurement of high speed temperature maps of the chip surface with 1 μ s temporal resolution and 15 μ m spatial resolution. The NIST system permits the measurement of the chip heat source distribution before the heat diffuses to surrounding regions. This enables the measurement of transient heating of reduced power IC FUBs (using clock gating, dynamic voltage scaling, and Vdd gating), transient current constriction failure events in RF and high power devices, and current uniformity in large area power devices.

DELIVERABLE: Apply high speed thermal imaging system to characterize localized dynamic heating of reduced power FUBs in advanced digital integrated circuits.

DELIVERABLE: Improve the spatial resolution of the NIST high speed transient thermal imaging system from 15 μ m to 3 μ m while maintaining the 1 μ s time resolution.

TRANSIENT THERMAL IMAGING STANDARDS

There is a strong need to establish industry wide transient thermal measurement technique standards as described in the 2005 ITRS roadmap. NIST recently developed and tested a transient thermal calibration test structure with 1 μ s temporal resolution using microhotplates with integrated electrical temperature sensors.

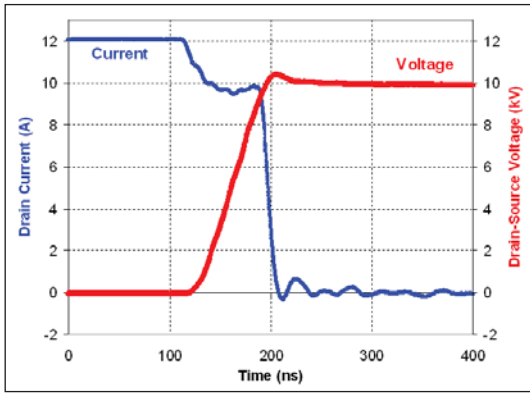
DELIVERABLE: Complete development of prototype IR transient thermal imaging calibration test chip.

ACCOMPLISHMENTS

■ *NIST played a key role in planning and coordinating government and industry programs and activities on high voltage SiC power devices including:* evaluated contractor performance for DARPA WBST HPE Phase 2; participated in planning and writing a Broad Area Announcement (BAA) for DARPA WBST HPE Phase 3 programs and presented status of SiC power devices at the Phase 3 Industry Bidder Briefing day; served as Member of DARPA/ONR SSPS Government Independent Design Panel; participated in planning ONR Mantech SiC Power Device manufacturability program; and served as panel member for DoE Program on SiC-Based Inverters in Near Zero Emission Fuel-Cell-Based Power Plants Fueled with Coal-Derived Gas.

■ *High voltage clamped inductive and resistive switching test bed developed.* A low parasitic inductance 15 kV switching test system for clamped inductive and resistive load characterization was developed and integrated into the NIST 25 kV safety-interlocked curve-tracer system. A low parasitic capacitance temperature-controlled test fixture with 25 kV voltage isolation and 350 °C maximum controllable temperature was also included to enable HV-HF device characterization at elevated operating temperatures.

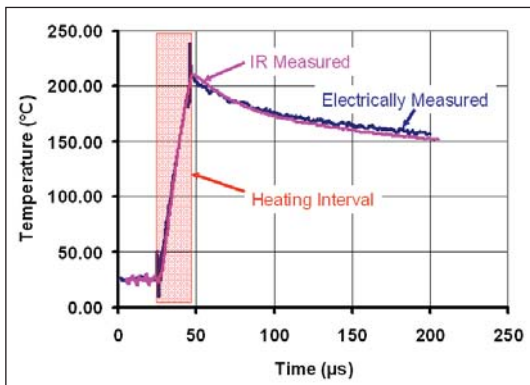
■ *The NIST unique high voltage curve tracer and high- HV- HF switching test system was used to demonstrate the unprecedented performance of DARPA WBST-HPE MOSFETs.* 10 kV, 12 A, 50 ns inductive load switching was demonstrated for the first time. Typical high voltage silicon devices require several microseconds to switch at 6.5 kV maximum.



NIST measurement of the unprecedented performance of the SiC power MOSFETs switching at 10 kV, 12 A, and 200 °C in less than 50 ns.

■ NIST HV-HF SiC models were used to simulate system performance impacts. NIST’s metrology, device modeling, and parameter extraction tools have resulted in software models for the SiC power devices produced by the DARPA WBST HPE program. These models are being used by industry and government to simulate the performance of future power distribution and conversion systems enabled by the new HV-HF SiC technology.

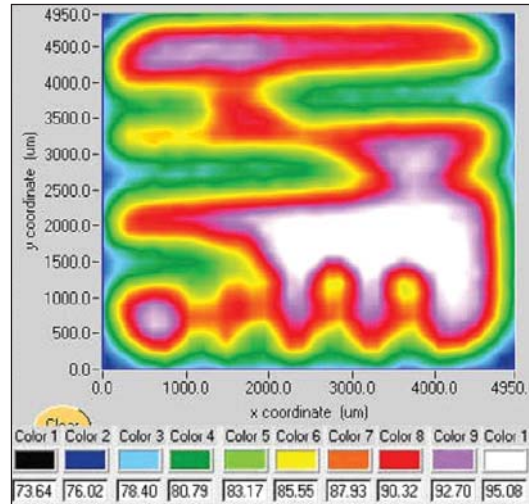
■ NIST recently developed and tested a transient thermal calibration test structure with 1 μs temporal resolution using microhotplates with integrated temperature sensors. This specially designed temperature-reference microhotplate structure is calibrated and used to verify the results of the transient IR thermal imaging system.



Comparison of transient IR thermal measurement with electrically measured value from thermal calibration test structure for a 20 μs heating pulse.

■ As low-degradation rate SiC PiN diodes are beginning to emerge, the NIST transient thermal imaging system is being used to determine the current uniformity after various levels of stress up to 1000 hours of operation. The NIST transient

thermal image system previously demonstrated that the SiC PiN current density is relatively uniform before degradation and that only 1 % of the chip is conducting all of the current after substantial degradation. Degradation of SiC diodes remains highly variable, and recent low-degradation devices show a 0 % to 30 % area reduction after 1000 hours of operation.



Pulsed thermal image of Low degradation rate SiC PiN diode showing 30 % area reduction after 500 hours of operation.

FY OUTPUTS

COLLABORATIONS

Synopsys Inc., Compact models and parameter extraction for power semiconductor devices.

UPRM, Characterization of SiC devices and thermal modeling of electronic packages.

Cree, SiC power device development and characterization.

Northrop Grumman Corp, SiC power device development and characterization.

Naval Research Lab, DARPA HPE deliverable evaluation.

Navsea/ONR/DARPA, SiC HPE program management and contractor monitoring.

Univ. California Irvine, Application testing of HV-HF SiC power devices.

Virginia Tech. Future Electronic Energy Center, SiC power device applications for power distribution.

DOE National Energy Technology Laboratory, SiC-based inverters in near zero emission fuel cell based power plants.

DOE Oak Ridge National Laboratory, SiC motor drives for electric vehicles.

General Electric, SiC device design and characterization for DARPA Robust Integrated Power Electronics Program.

Army Research Lab, Simulation of SiC thyristors for pulsed power applications.

RECENT PUBLICATIONS

D. W. Berning, A. R. Hefner Jr., J. J. Rodriguez, C. E. Hood, A. Rivera, "Generalized Test Bed for High-Voltage, High-Power SiC Device Characterization," Proc., IEEE Industrial Applications Society Meeting, Oct 09-12, 2006, Tampa, Florida (01-OCT-2006)

A. R. Hefner Jr., R. Sei-Hyung, H. Brett, D. W. Berning, C. E. Hood, J. M. Ortiz-Rodriguez, A. Rivera-Lopez, T. Duong, A. Akuffo, M. Hernandez, "Recent Advances in High-Voltage, High-Frequency Silicon-Carbide Power Device," Proc., IEEE Industry Applications Society (IAS) Annual Meeting, IEEE Industrial Applications Society Meeting, Oct 08-12, 2006, Tampa, Florida (01-OCT-2006)

R. Sei-Hyung, K. Sumi, B. Hull, J. Richmond, A. Agarwal, A. R. Hefner Jr., "10kV, 5A 4H-SiC Power DMOSFET," IEEE Transactions on Electron Devices, ISPSD (01-MAY-2006)

J. M. Ortiz-Rodriguez, A. R. Hefner Jr., D. W. Berning, C. E. Hood, S. Olcum, "Computer-Controlled Characterization of High-Voltage, High-Frequency SiC Devices," Proceedings of the IEEE COMPEL Workshop 2006, IEEE COMPEL 2006, Jul 16-19, 2006, Troy, New York (01-JUL-2006)

T. Duong, A. R. Hefner Jr., D. W. Berning, "Automated Parameter Extraction Software For High-Voltage, High-Frequency SiC Power MOSFETs," Proceedings of the IEEE COMPEL 2006 Workshop, IEEE COMPEL Workshop (COMPEL06), Jul 16-19, 2006, Troy, New York (01-JUL-2006)

A. R. Hefner Jr., "Status of High-Voltage, High-Frequency Silicon-Carbide Power Devices," GOMACTech-06, Mar 20-23, 2006, San Diego, California, California, pp. 232-235 (22-MAR-2006)

J. Lai, H. Yu, J. Zhang, Y. Li, K. Sheng, J. H. Zhao, A. R. Hefner Jr., "Characterization of Normally-off SiC Vertical JFET Devices and Inverter Circuits," IEEE Transactions on Industry Applications, pp. 44-49 (01-OCT-2005)

MICRO-NANO-TECHNOLOGY (MNT)

GOALS

The Micro-Nano-Technology (MNT) Project works to apply micro and nanofabrication technologies to advance the state-of-the-art of single molecule measurements, single cell measurements, and DNA separations for forensic applications. In addition, we support domestic and international MicroElectroMechanical systems (MEMS) standardization by working with standards groups to develop and provide the MEMS industry with test structures, test methods, measurement standards, and standard manufacturing practices.

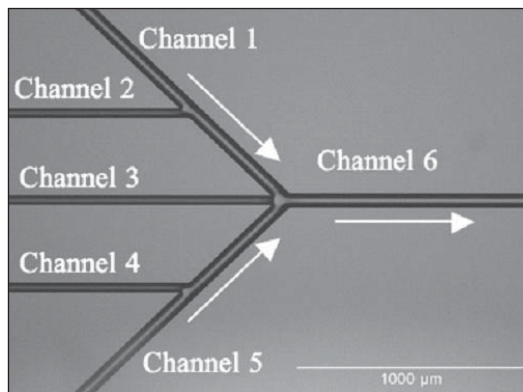
CUSTOMER NEEDS

Micro-Nano-Technology (MNT), including MEMS and microfluidics, continues to mature, resulting in growing opportunities for U.S. industry and new opportunities for laboratory research. Hand-in-hand with the growth in this field is an increasing need for measurement standards and artifacts. Our project aligns its efforts with NIST's core mission and strategic growth areas in nanotechnology, biosystems, and homeland security. The MNT Project has developed four focus areas: single molecule manipulation and measurement (SM³), bioelectronics, MEMS standards, and DNA separations for forensic applications.

SINGLE MOLECULE MANIPULATION AND MEASUREMENT

The biotechnology and healthcare industries require measurements of large sample arrays as part of their combinatorial approach to disease recognition and drug development. For example, manufacturers of technologies such as DNA and protein arrays are striving to make larger arrays that can more efficiently support larger combinatorial measurements. As the size of the sensors is decreased, the sample size (and hence the number of molecules present in the sample) also decreases. Since biological molecules are expected to have variations in their behavior, questions arise concerning whether the statistical variation of biological molecules will affect the accuracy of those measurements; *e.g.*, is there a minimum sample size that is required to yield a result that is comparable to traditional ensemble measurements. The ability to measure the structure and function of single biomolecules will yield the statistical behavior of their large populations.

A critical need for making single molecule measurements is the ability to capture, isolate, and position single molecules for direct observation. A technique commonly used is to bind them on a surface at a low concentration and then probe them using optical microscopy. Another approach, which we are developing, would be to encapsulate them in a "nano-vial" so that they can be moved to a position for observation by, for example, laser tweezers. We have developed a microfluidic device that will form liposome "nano-vials" for this purpose.



A photomicrograph of a new microfluidic device for continuous flow formation of liposome nano-vials.

BIOELECTRONICS

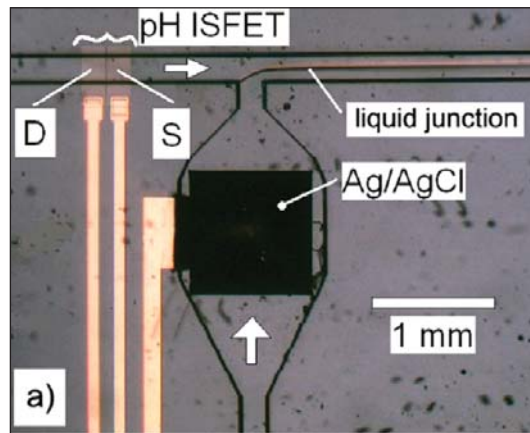
Experiments in cell biology have been virtually unchanged for many decades, involving manual handling of cell culture flasks, changing the cell media (feeding the cells), exposing the cell culture to a compound of interest, and observing cell response and viability using a microscope. For this reason, cell biology experiments are typically very time consuming and labor intensive. Recently, the trend has been to conduct studies that involve large arrays of small cell cultures by automating these steps as much as possible using robotic instrumentation, but the experiments are still essentially the same. A true paradigm shift is to utilize micro-nano-technologies to perform these experiments on single cells or small cell clusters.

Our vision for bioelectronics is directed towards the exploration of the electronic interfaces between integrated circuit technologies and biological systems. We have developed a focused research effort to evaluate the metrology issues associated with electronic measurements of small cell populations and investigate the performance of "active"

Technical Contact:
Michael Gaitan

Staff-Years (FY 2006):
4.5 professionals
1.0 post doc
4.75 guest researchers

electrodes, where microelectrodes integrated with operational amplifiers and digital electronics could be placed right at the point of measurement.



Prototype Ion-Sensitive Field-Effect Transistor (ISFET) device with integrated reference micro-electrode for measurement of pH in a microfluidic network.

MEASUREMENTS AND STANDARDS FOR MEMS

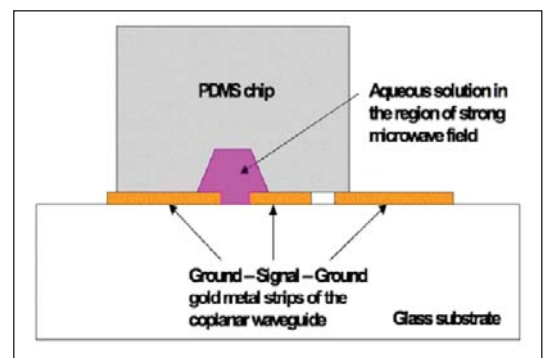
MEMS is a rapidly growing technology with a forecasted annual growth rate that exceeds that of the semiconductor electronics industry as a whole. Manufacturers of MEMS products, such as acceleration sensors for automotive air bags and deformable mirror displays for video projection, are producing these devices in Integrated Circuit (IC) manufacturing lines. This integration of mixed technologies is part of the semiconductor industry's revolution towards "system-on-a-chip." System-on-a-chip links the functionality of the IC (an information processor) with information gathering (sensing the environment) and actuation (acting on decisions). New test structures, test methods, and standards are required for device characterization to improve manufacturing and design.

In support for the need of measurement standards for MEMS, the project is working with ASTM Task Group E08.05.03 on Structural Films for MEMS and Electronic Applications. This task group has undertaken sponsorship of a round robin experiment for measuring in-plane length, residual strain, and strain gradient. MEMS test structures used in these experiments are designed and then fabricated on a test chip that is passed among participating laboratories. These dimensional and film properties are important to the fabrication of MEMS devices. Participation in the ASTM Task Group

gives NIST a leadership role in the development of measurement standards for the industry.

The MEMS Project is also working with SEMI's new MEMS Materials Characterization Task Force to develop standardization for MEMS technology. Our prime effort with this group is working to support the development of compact models for MEMS devices that can accurately simulate their response in advanced circuit simulators.

The project played a leadership role in the recent NIST study of the U.S. Measurement System (USMS) by contributing to two workshops on MNT needs. The first USMS Workshop was held in Pittsburgh, PA, on September 22, 2005, immediately after the Metric 2005 Conference. Representatives from a number of companies with interest in MNT technologies attended and were asked to help define and prioritize the metrological needs of the MNT community. From the gathered workshop inputs and subsequent discussions, seven measurement needs (MNs) were crafted. One need of particular interest to this project concerns material property measurements for "fabless" microelectromechanical systems (or MEMS). The concept of fabless MEMS is one in which a company can produce devices via a foundry rather than their own, expensive (over \$100 million) fabrication facility. This is similar to the foundry model, which has been successfully implemented in the semiconductor industry. A report describing the outputs of this USMS Workshop is in preparation and will be published in the MEMS Industry Group (MIG) 5-year anniversary report.



A schematic of the coplanar waveguide (CPW) device developed for microwave dielectric heating in a microfluidic network.

The second USMS Workshop was held on March 15, 2006, during Pittcon, in Orlando, FL. This meeting was targeted on metrology needs for microfluidics applications. Representatives from

seven companies presented their metrology needs in this rapidly growing field. During this meeting, a need for dimensional metrology was stated. Many of the proposed microfluidic applications depend upon accurately knowing the dimensions of the measurement device.

MEMS-based IC test structures allow, for the first time, the measurement of strain in multilayer structures in fully fabricated ICs. These measurements can be used to characterize the mechanical stress in these multilayer films. Results can then be used to verify finite element models of the stress in the films and correlate mechanical stress data with reliability testing. MEMS-based test structures being developed in this project offer new ways to characterize the mechanical stress in multilayer films.

DNA SEPARATIONS FOR FORENSIC APPLICATIONS

The Department of Justice recognizes an urgent need to improve the efficiency, speed, and accuracy of DNA testing in order to alleviate a growing backlog of forensic DNA testing for criminal cases. Results of DNA testing have become a critical component of criminal investigations and are often used as evidence in court proceedings. NIST has played a key role in the validation and standardization of forensic DNA testing protocols over the past decade that has facilitated a growing acceptance of this type of analysis for criminal investigations.

Microfluidic technology is a promising alternative to current capillary-based techniques due to its great potential to miniaturize, simplify, integrate, automate, and multiplex the analysis with higher throughput and speed. This technology has already shown that it is the next revolution in DNA technology, with analysis often complete in ten percent of the time required for more traditional capillary technology. Although DNA analysis systems based on microfluidics technology have been recently commercialized, these systems do not meet the specific needs of the forensic community due to poor separation resolution of the relatively long fragments (on the order of 100 bps to 400 bps) as well as incompatibility with the standard test procedures.

We have also initiated a new effort in this task on sample preparation. We are investigating the feasibility of using microwave power delivered to specific points in a microfluidic network to heat, create temperature gradients, and cycle temperature. This capability would be used for cell lysis

(extract DNA), Polymerase Chain Reaction (PCR) DNA amplification, and purification steps that could be integrated with the microfluidic separation system. The ability to carry out these sample preparation steps would greatly speed-up the process of DNA fingerprinting.

TECHNICAL STRATEGY

NanoBioTechnology is a new and rapidly growing field that is focused on the development of nanotechnology for biomedical research and applications. The Semiconductor Electronics Division sees a new opportunity for the application of nanofabrication methods to create structures to probe biological systems at the single cell and single molecule level. The top-down nano-fabrication methods that have been developed by the semiconductor electronics industry can be coupled with bottom-up self-assembly techniques to create new tools to probe life's processes. We believe that the ability to measure the behavior of individual cells or biological molecules, which are traditionally characterized by ensemble measurements, will provide fundamentally new information about how those biological processes work. We have three main focus areas in our nanobiotechnology effort: Single Molecule Manipulation and Measurement (SM³), where we seek to develop new tools to probe the structure of DNA electronically and optical methods to characterize the structure and conformations of proteins; Bioelectronics, where we seek to sense single cell behavior electrochemically; and DNA separations for forensic applications, where we seek to develop a plastic-based microfluidic device that will decrease the time to perform a separation at a lowered cost. Our work is carried out with multidisciplinary teams that span laboratories within NIST and the National Institutes of Health.

SINGLE MOLECULE MANIPULATION AND MEASUREMENT

The semiconductor electronics industry has driven the development of fabrication tools that are capable of patterning structures that are smaller than cellular dimensions (*i.e.*, on the order of 100 nm). In combination with micro-machining methods developed by MEMS research, it is possible to create three-dimensional structures that are commensurate with the size of biomolecules. We will utilize nanofabrication methods and enhanced surface coatings to develop novel solid-state structures for the control and manipulation of single biomolecules. These methods will be based

on electrofluidic, electro-mechanical, optical, and magnetic transport of biomolecules in confined nanometer-scale environments.

Interactions of single molecules with nanoscale mechanical structures, restriction elements, and other single molecules will be probed by electronic, electromechanical, and optical techniques. The effort will result in a well-characterized SM³ platform integrated with atomic force microscopy (AFM), FRET (Fluorescence Resonance Energy Transfer), optical microscopy, and electronics, thereby enabling a wide variety of single-molecules studies. DNA structure determination will be performed by directly interrogating ordered bases as they are threaded through a well-characterized nanopore.

DELIVERABLE: Develop and characterize the performance of a 5-channel device for formulation of liposome nanovials and determine the optimal conditions to minimize free dye in solution.

DELIVERABLE: Develop methods and optimize formulation conditions for vesicle-templated alginate nanoparticles.

BIOELECTRONICS

Recent scientific reports describe the ability to stimulate electronically and probe single cell activity and to transport, sort, and position single cells. These capabilities have resulted in significant advances in biological sciences and medicine. An excellent example is patch clamp technology that has revolutionized the field of electrophysiology. Advances in microfabrication methods have recently led to the development of patch clamp arrays and other automated on-chip techniques; however, the widespread adoption of more complex integrated systems for biologically relevant measurements continues to face technological hurdles. These include complicated materials integration issues (maintaining a biocompatible environment for cells within the *in vitro* measurement systems, developing stable and drift-free electrodes for accurate measurements, invaried buffer solutions, etc.), the difficulty of accurately determining the electrical/electromagnetic response of integrated electronic/MEMS/fluidic systems, and issues related to the reproducible fabrication of integrated devices. By addressing these critical measurement infrastructure needs, NIST will accelerate the development of powerful new bioelectronic platforms and techniques.

Our technical approach is to integrate microelectronics, MEMS, and microfluidic systems with cells in order to achieve a new level of control over the

electronic/biological interfaces under study. We will develop methods to adhere and grow cells in defined patterns in a biological hybrid *in vitro* environment that incorporates microelectronic circuits, both electrochemical and RF, to stimulate and sense cell activity. Microchannel networks will be used to transport the biological specimens to exact locations and deliver precise amounts of chemicals or drugs to the local cellular environment. These techniques will allow us to apply precise electrical, electro-magnetic, and chemical stimulation to the cells and to measure their metabolic, electrical, and physiological responses. We will focus our initial research efforts on the study of retinal (neuronal) cells and will later progress to other cell systems.

DELIVERABLE: Design, fabricate, and test a prototype device for accurate pH measurements in a microfluidic network.

DELIVERABLE: Fabricate and characterize covalently bound polyelectrolyte multilayers. Evaluate their potential as a nanogel for trapping or separating biomolecules (proteins, DNA, etc.).

MEMS TEST STRUCTURES AND STANDARDS

Micro-machining techniques, test structures, and test methods are being developed to characterize the stress, elastic modulus, and adhesion properties in the thin films comprising ICs. These test structures are fabricated in the standard IC process on fully fabricated ICs. Fixed-fixed beam and cantilever test structures with and without interconnect layers are micro-machined in the fully processed IC. Measurements of deflection of buckled beams give information on the strain in each layer. Measurements of mechanical resonance give information on the elastic modulus of the films. These test structures can also be integrated with micro heating elements for accelerated testing.

The MEMS technical community, composed of companies, universities, and government laboratories, has developed many types of test structures to characterize the fabrication process and device performance. The MEMS Project plays an active role in ASTM Task Group E08.05.03 on Structural Films for MEMS and Electronic Applications and in SEMI's MEMS Materials Characterization Task Force to supply the community with standardized test methods.

DELIVERABLE: MIG anniversary report, "Standardization and the Study of the U.S. Measurement System for Micro Nano Technologies."

DELIVERABLE: Identify and develop MEMS “Living Standards” (*i.e.*, continuously evolving/updated standards) with SEMI.

DNA SEPARATIONS FOR FORENSIC APPLICATIONS

Our team will draw on our extensive expertise in microfluidics, microfabrication, DNA separations, as well as state-of-the-art optics and detection to build a prototype system that can be used as a model to demonstrate the advantages of applying these latest technologies for forensic identification. There are two overall requirements that must be satisfied to meet the needs of the Department of Justice: (1) development of a reliable, easy-to-use, high-throughput, microfluidics-based system that is smaller and faster than capillary-based techniques; and (2) validation of the system that would support the adoption of this technology by the judicial system.

DELIVERABLE: Complete development of a prototype microfluidic forensic DNA separation system for demonstration to forensic scientists.

DELIVERABLE: Develop an integrated microwave transmission line with a microfluidic network and investigate the feasibility of using microwave power to heat fluid in specific points in the channel.

DELIVERABLE: Investigate the feasibility of using microwave power to lyse cells in a microfluidic device.

ACCOMPLISHMENTS

■ *Develop and characterize the performance of a 5-channel device for formulation of liposome nanovials and determine the optimal conditions to minimize free dye in solution.* Previously we demonstrated liposome formation using hydrodynamic focusing in a microfluidic network which enables us to produce liposomes of a controlled size and size distribution in a reproducible fashion. Liposomes were characterized with batch dynamic light scattering (DLS) and multi angle laser light scattering (MALLS) of unfractionated samples. However, this measurement only provides ensemble averages. In the past year, we have implemented a more detailed and accurate measurement technique that allows for precise characterization of liposome populations using asymmetric flow field flow fractionation (AFFFF) before MALLS and DLS. Details about liposome size and size distribution allow further elucidation about the liposome self-assembly process.

■ *Develop methods and optimize formulation conditions for vesicle-templated alginate nanoparticles.* Biology is rife with the motif of molecules

self-assembling into larger functional elements. In fact, a human being can be thought of as the product of the directed self-assembly of cells into a functional person. We have taken a simple biologically inspired system, the liposome, and used it to template the self-assembly of biomolecules into nanoparticles of controlled size and architecture. We have demonstrated that liposomes can be used to template the gelling of alginate into nanoparticles that have a size equivalent to that of the parent liposome. This allows for the control of the nanoparticle size through modulation of the templating liposome’s size. In contrast to liposomes and other vesicles, these nanoparticles appear to be extremely stable to temperature variations, detergent treatment, and changes in buffer osmolarity and pH.

■ *Design, fabricate, and test a prototype device for accurate pH measurements in a micro-fluidic network.* Lab-on-a-Chip (LOC) systems might enjoy more widespread use if reliable and accurate electronic chemical sensors are more closely integrated with the microfluidic networks. In this work, an ion-sensitive field-effect transistor (ISFET) and an Ag/AgCl quasi-reference electrode were integrated with a polymeric surface-mounted microfluidic network in order to demonstrate electrochemical measurement of pH in the planar microfluidic format. The gate insulator of the n-type ISFET was an SiO₂ / Si³N₄ stack (85 nm / 38 nm). The device was observed to be temperature sensitive, and several time-varying electronic characteristics were explained in terms of resistive heating of the FET channel. The drain current (ID), drain voltage (VDS) transfer characteristics were recorded, and the drain-to-source impedance was measured while the device was exposed to flowing aqueous solutions. Transfer characteristics from VDS = 0 V to 3 V indicated that the device functioned as a depletion-type FET. At steady-state, the drain-to-reference voltage (VDR) gave linear calibrations for flowing buffer solutions from pH 3 to pH 11 of approximately 63 mV pH⁻¹. The ISFET was shown to be a viable all-electronic pH sensor for planar microfluidics. With additional characterization, the device may lead to improved pH measurement traceability for portable LOC systems.

■ *Fabricate and characterize covalently bound polyelectrolyte multilayers. Evaluate their potential as a nanogel for trapping or separating biomolecules (proteins, DNA, etc.).* A unique method for layer-by-layer patterning and crosslinking of polymers with dissimilar cell attachment charac-

teristics is presented. Polyelectrolyte multilayers (PEMs) were deposited and exposed with UV light through a binary photomask to form a patterned upper stratum where cells are not viable and a lower cytophilic stratum. This work describes the facile synthetic procedures used to make crosslinkable polyelectrolytes, demonstrates photopolymerization of the functionalized polyelectrolytes, and reveals the cytophobic character of the new synthesized polyelectrolytes for future cell culture applications.

■ *MIG anniversary report, "Standardization and the Study of the U.S. Measurement System for Micro Nano Technologies."* Two NIST U.S. Measurement System (USMS) workshops have recently been held relating to MNT metrology. The first USMS Workshop was held in Pittsburgh, PA, on September 22, 2005, immediately after the Metric 2005 Conference. Representatives from a number of companies with interest in MNT technologies attended and were asked to help define and prioritize the metrological needs of the MNT community. From the gathered workshop inputs and subsequent discussions, seven measurement needs (MNs) were crafted. One need of particular interest to this project concerns material property measurements for "fabless" microelectromechanical systems (or MEMS). The concept of fabless MEMS is one in which a company can produce devices via a foundry rather than their own, expensive (over \$100 million) fabrication facility. This is similar to the foundry model, which has been successfully implemented in the semiconductor industry. A report describing the outputs of this USMS Workshop is in preparation and will be published in the MEMS Industry Group (MIG) 5-year anniversary report. The second USMS Workshop was held on March 15, 2006, during Pitcon, in Orlando, FL. This meeting was targeted on metrology needs for microfluidics applications. Representatives from seven companies presented their metrology needs in this rapidly growing field. During this meeting, a need for dimensional metrology was stated. Many of the proposed microfluidic applications depend upon accurately knowing the dimensions of the measurement device.

■ *Identify and develop MEMS "Living Standards" with SEMI.* The MNT Project is currently championing MNT standardization efforts in two venues: ASTM and SEMI. Highlighting the need for MNT standardization is the number of companies and other organizations participating in these standards activities. The first four MNT standards (on in-plane lengths, residual strain, strain gradient, and terminology) originated in the

ASTM E08.05.03 Task Group on Structural Films for MEMS and Electronic Applications. Also within this task group, standards for determining Young's modulus, ultimate strength, and fatigue for a surface micromachining process are being developed at Penn State. The MNT standardization efforts being actively pursued in SEMI's North American MEMS Standards Committee include recently-published SEMI Standard MS1-0306 on wafer-to-wafer bonding alignment targets. Other SEMI MNT standardization efforts include a proposed guide (PR9-0705) on microfluidic interfaces; a proposed standard (PR11-1105) on MEMS terminology; and work on stiction, wafer specifications, wafer bond inspection techniques, wafer bond strength, and RF MEMS qualification. An additional activity in SEMI's MNT standardization effort is the identification of standards related to MNT technology. SEMI is attempting to identify these standards and incorporate them into SEMI's "Living Standard." This Living Standard, which will list MNT standards from all standardization bodies and be maintained by the North American MEMS Standards Committee, will serve to guide industry and researchers to existing standards and highlight areas where standards may be needed.

■ *Complete development of a prototype microfluidic forensic DNA separation system for demonstration to forensic scientists.* The goal of this effort was to develop a plastic microfluidic-based system for high-speed electrophoretic analysis of DNA fragments for forensic applications. The development of this device has been completed, and we have approached several companies in the DNA analysis community to present this technology for future commercial development. We have formalized a Collaborative Research and Development Agreement (CRADA) with Network Biosystems, Inc., and are currently working with them to transfer this technology to a commercially available product, thus expediting the availability of this instrumentation to the forensics community.

■ *Develop an integrated microwave transmission line with a microfluidic network and investigate the feasibility of using microwave power to heat fluid in specific points in the channel.* Rapid thermocycling and localized and selective heating of fluids on-chip is important for micro total analysis system (microTAS) applications. We have developed a new approach to accomplish this by microwave dielectric heating using an integrated microwave transmission line to deliver heat to a specific region in a microfluidic network. An elastomeric microfluidic channel was positioned over a coplanar waveguide (CPW) that was fabricated

on a glass substrate. S-parameter and temperature measurements of the device were used with a theoretical analysis to fully characterize the temperature rise of the fluid by microwave power absorption. In this unoptimized exploratory device, a 0.95 °C per mW temperature rise was observed at 15 GHz. Our theoretical analysis confirms that classical microwave absorption theory is valid at this scale.

■ *Investigate the feasibility of using microwave power to lyse cells in a microfluidic device.* Cell lysis is a method used to disrupt the cell membrane and release the intracellular components such as proteins, DNA, and RNA, among others. Chemical, mechanical, and thermal lysis methods are used to lyse cells conventionally. The technique of choice will be dictated by the cell origin, the difficulty in cell membrane and/or wall disruption, and its compatibility with the bio-molecules or organelles to be recovered or extracted in the subsequent steps. Thermal lysis is the method (among the above mentioned methods) that is compatible only with nucleic acids analysis, since the high temperature attained will denature the cell proteins, and the organelles will likely be disrupted. We have successfully demonstrated the application of microwave power to lyse cells in a microfluidic device. Microwave heating presents a technique to heat aqueous solutions in a very rapid way since the media is heated directly and heat does not need to be conducted through the walls of the container to the media. Integrating microwave guides in a microfluidic system should allow for the rapid lysing of cells and quick transport of the cell components to clean up, PCR, and separation steps that are necessary down the road in a micro total analysis system.

FY OUTPUTS

COLLABORATIONS

National Eye Institute of NIH, S. Patricia Becerra, Patterning neural (retinal) cells on surfaces to improve the understanding and treatment of diseases associated with vision.

Instrumentation Research and Development Group of NIH, Paul Smith and Tom Pohida, Development of optical detection methods for forensic DNA separations.

National Cancer Institute of NIH, David Robert, Liposome nano-vials for cancer detection and treatment.

NIST Division 844, Lori Goldner and Angela Hight-Walker, Single molecule nano-vials.

NIST Division 842, Kris Helmerson, Single molecule nano-vials.

NIST Division 839, Laurie Locascio and Wyatt Vreeland, Liposome nanovials.

University of Maryland/Georgia Tech, Measuring and modeling bonding temperature rise.

STANDARDS COMMITTEE PARTICIPATION

ASTM Task Group E08.05.03, round robin in progress to determine the precision and bias of the three recently published MEMS standards (Janet C. Marshall)

SEMI's MEMS Materials Characterization Task Force, working on bringing forward compact models for MEMS devices for standardization (Janet C. Marshall)

STANDARDS PUBLISHED

ASTM E 2444-05e1, "Standard Terminology Relating to Measurements Taken on Thin, Reflecting Films," January 2006.

ASTM E 2245-05, "Standard Test Method for Residual Strain Measurements of Thin, Reflecting Films Using an Optical Interferometer," December 2005.

ASTM E 2246-05, "Standard Test Method for Strain Gradient Measurements of Thin, Reflecting Films Using an Optical Interferometer," December 2005.

EXTERNAL RECOGNITION

Chief U.S. Delegate of the International Micromachine Summit to be held in Venice, Italy, May 2005 (Michael Gaitan)

RECENT PUBLICATIONS

S. P. Forrey, D. R. Reyes, M. Gaitan, L. E. Locascio, "Cellular Immobilization within Microfluidic Microenvironments: Dielectrophoresis with Polyelectrolyte Multilayers," *J. Am. Chem. Soc.*, 2 p. (30-SEP-2006)

J. Shah, J. Geist, L. Locascio, M. Gaitan, R. Mulpuri, W. Vreeland, "Surface Modification of PMMA for Application of Wall Coating Polymers for Microchip Electrophoresis," *Electrophoresis*, 8 pp. (01-SEP-2006)

S. P. Forry, D. R. Reyes, M. Gaitan, L. E. Locascio, "Facilitating the Culture of Mammalian Nerve Cells with Polyelectrolyte Multilayers," *Langmuir*, 6 p. (19-MAY-2006)

J. Shah, J. Geist, L. Locascio, M. Gaitan, R. Mulpuri, W. Vreeland, "Capillarity Induced Solvent? Actuated Bonding of Polymeric Microfluidic Devices," *Anal. Chem.*, Vol. 78, No. 10, pp. 3348-3353 (12-APR-2006)

B. J. Polk, A. Stelzenmuller, G. I. Mijares, W. A. MacCrehan, M. Gaitan, "Ag/AgCl Microelectrodes with Improved Stability for Microfluidics," *Sensors and Actuators B, Chemical*, Vol. 114, No. 1, pp. 239-247 (30-MAR-2006)

J. C. Marshall, R. I. Scace, W. A. Baylies, "MEMS Length and Strain Round Robin Results with Uncertainty Analysis," NIST Interagency/Internal Report (NISTIR) 7291, (01-FEB-2006)

D. R. Reyes, L. E. Locascio, M. Gaitan, "Polyelectrolyte Multilayers," 15 pp. (23-JAN-2006)

S. Shivesh, M. Gaitan, J. Yogendra, G. G. Harman, "Wire Bonding Process Monitoring Using Thermopile Temperature Sensor," *IEEE Tran on Advanced Packaging*, Vol. 28, No. 4, pp. 685-693 (17-NOV-2005)

S. P. Forry, D. R. Reyes, M. Gaitan, L. Locascio, "Generating Cell Arrays Inside Microfluidic Networks," *Proceedings of the 230th American Chemical Society National Meeting, 230th American Chemical Society National Meeting, Aug 28, 2005 to Sep 01, 2005, Washington, District of Columbia*, pp. U384-U385 (01-SEP-2005)

NANOBIOTECHNOLOGY

Technical Contact:
John J. Kasianowicz

Staff-Years (FY 2006):
1.25 professionals
3.0 post docs
1.0 guest researcher
0.5 graduates

GOALS

For over a decade, single molecule detection has enabled the study of biological systems in remarkable detail. Such measurements permit direct observation of molecular behavior that can be obscured by ensemble averaging. This project seeks to use single molecule electronic and optical measurements to understand the structure and function of biological molecules. The development of new nanoscale technologies for detecting and characterizing biological and biomimetic molecules is paramount to achieve these goals.

CUSTOMER NEEDS

The biotechnology and healthcare industries require measurements of large sample arrays as part of their combinatorial approach to disease recognition and drug development. For example, manufacturers of technologies such as DNA and protein arrays are striving to make larger arrays that can more efficiently support larger combinatorial measurements. These and similar efforts require further development.

The ability to sequence DNA rapidly and cheaply is an important goal both for the health care industry and for academic studies of genomics. NIST was a pioneer in the invention and development of the nanopore technology supporting that goal and will continue to innovate in this field.

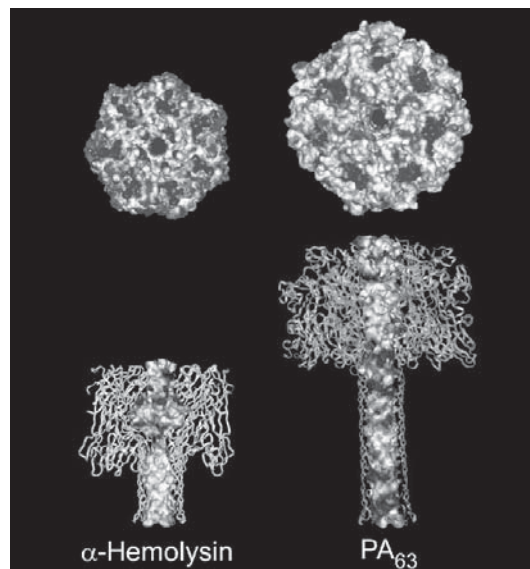
Recent terrorist acts underscore the need to better understand the mechanism of action for biowarfare agents and to develop more effective therapeutic agents against them. For example, anthrax infection, which leads to cell death, is caused by the interaction of several toxins secreted by the bacteria *Bacillus anthracis*. There is good agreement about how two of the toxins exert their lethal effects inside cells. But, how these molecules are transported across cell membranes is not completely understood. Because of NIST's experience with similar bacterial pore-forming toxins, the DoD sought NIST as a partner on this research.

TECHNICAL STRATEGY

Nanobiotechnology is a new and rapidly growing field that is focused on the development of nanotechnology for biomedical research and applications. The Semiconductor Electronics Division sees a new opportunity for the application of nanofabrication methods to create structures to

probe biological systems at the single molecule level and to use novel methods to better understand how biomolecules function.

Our core competencies include electrophysiology, electrochemical impedance spectroscopy, cyclic voltammetry, microbiology, single molecule fluorescence, optical tweezers, surface plasmon resonance, MEMS, molecular simulation, and microfluidics. Due to the highly multidisciplinary nature of the research, the Nanobiotechnology Project members also collaborate with teams of scientists with expertise in advanced statistical signal processing, atomic force microscopy (AFM), cell biology, chemical synthesis, molecular biology, neutron reflectance, theory and computer simulation, and protein biochemistry. Our partners are located at other government agencies (DoD, NIH), universities (Carnegie Mellon, U. Pittsburgh, Columbia, Vilnius), and other NIST Laboratories (Information Technology, Chemical Sciences and Technology, Physics, National Center for Neutron Research).



*Nanometer-scale pores formed by proteinaceous toxins secreted by *Staphylococcus aureus* (left) and *Bacillus anthracis* (right). The former is ~ 10 nm tall and has a limiting aperture of 1.6 nm. Both channels are being studied for their mechanism of action and potential use in the detection and characterization of other molecules.*

Because the sizes of biological molecules are nanometer-scale, the tools that best determine their structure and function should be of similar dimen-

sions. Thus, the Nanobiotechnology Project is using ionic and molecular probes that are commensurate with the length scales of the objects of interest.

A major focus of the project is to determine the structure and function of nanoscale pores formed by bacterial toxins (see left figure). The nanopores can then be used for scientific and technological applications. These include:

- understanding the mechanisms of bacterial toxin virulence,
- developing novel methods for mass spectrometry, and
- creating devices for low-cost, ultra-rapid DNA sequencing.

DELIVERABLE: Develop a top-down, bottom-up hybrid platform that integrates solid-state chips and biomimetic/biological molecules for the detection, characterization, and manipulation of single DNA, RNA, and protein molecules.

DELIVERABLE: Extend the use of a single nanopore as a mass spectrometer.

DELIVERABLE: Develop nanopore-based arrays for the detection of a wide variety of analytes.

DELIVERABLE: Test physical theories for ion transport through bacterial pore-forming toxins. The results will provide constraints for models of the channel structures.

DELIVERABLE: Use AFM, single molecule fluorescence techniques, electrochemical impedance spectroscopy, and neutron reflectance to a) test a model for the anthrax PA₆₃ nanopore structure, b) determine the binding stoichiometry of anthrax Lethal Factor (LF) and the PA₆₃ channel, and c) determine whether LF bound to the PA₆₃ channel undergoes significant structural change under conditions that catalyze its transport across endocytotic vesicle membranes.

DELIVERABLE: Determine how well a single nanopore can distinguish between subtly different DNA molecules. These studies will aid efforts to rapidly sequence DNA with a single nanopore.

ACCOMPLISHMENTS

■ *Assessment of the USMS measurement needs in Nanobiotechnology.* The first U.S. Measurement System (USMS) Workshop on Measurement and Standards Needs in Nanobiotechnology was held on Jan. 19, 2006, at Rice University in Houston, Texas. The meeting was organized by NIST scientists and an external steering committee comprised of university faculty and industrial scientists.

Approximately 100 workshop attendees heard introductory talks by Kathleen Matthews (Dean of the Wiess School of Natural Sciences and Stewart Professor of Biochemistry and Cell Biology), S.

Ward Casscells (John Edward Tyson Distinguished Professor of Medicine, Cardiology, and Public Health, and Vice President for Biotechnology, the University of Texas Health Science Center at Houston), and Hratch Semerjian (then Deputy Director of NIST).

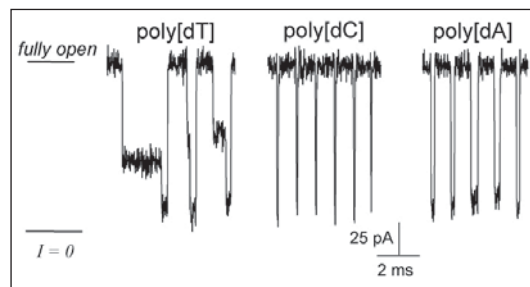
Plenary talks on a wide range of topics in nanobiotechnology were given by Scott McNeil (director, Nanotechnology Characterization Laboratory, NCI), David Luzzi (director, Nanotechnology Institute, University of Pennsylvania), Nakissa Sadrieh (associate director for Research Policy and Implementation, Food and Drug Administration), Nigel Walker (National Institute of Environmental Health Sciences, Toxicology Operations) and Vicki Colvin (Director, Center for Biological and Environmental Nanotechnology and Chair of ASTM Committee E56 on Nanotechnology).

To help identify specific measurement and standards needs in nanobiotechnology, the workshop attendees participated in five concurrent sessions on topics that included Medical/Clinical/Pharmaceutical Issues (drug delivery, targeted therapeutic agents, nanomaterials devices drug discovery), Medical Imaging (nano-based contrast agents, other imaging modalities), manufacturing (nanoparticle handling, manufacturing, safety, scale-up), basic science (structure and dynamics of biomolecules, sensing at the single molecule level), and physical characterization (dimension, composition, purity, surface chemistry, instrumentation). The suggestions obtained from these breakout sessions will aid NIST's USMS road mapping efforts. The workshop provides direct stakeholder input to the comprehensive USMS assessment process.

■ *Probing the structure of single nanometer-scale pores with DNA molecular rulers.* Over a decade ago, NIST demonstrated that individual molecules of single stranded DNA can be driven electrophoretically through a single *Staphylococcus aureus* α -hemolysin ion (α HL) channel. Polynucleotides thread through the channel as extended chains, and the polymer-induced ionic current blockades exhibit stable modes during the interactions. Recently, polynucleotides were used to probe structural features of the α -hemolysin nanopore. Specifically, both the pore length and channel aperture profile were estimated by using different length polynucleotides with a large macromolecule tethered to one end. The results are consistent with the channel's crystal structure and suggest that polymer-based "molecular rulers" may prove useful in deducing the structures of

other nanometer-scale pores, including solid-state varieties.

Electronic readout of information in polymers aided by advanced statistical signal processing. The electronic signatures caused by threading single-stranded DNA through a single nanometer-scale pore are characteristic of the polymer's type and length (see figure below). A method for characterizing these signals using ergodic, but persistent Hidden Markov Models was developed. Gaussian mixture models were used as output distributions to obtain a maximum likelihood estimate of state sequence and lifetime. The results are consistent with the known structure of the nanopore and suggest an approach to decode information stored in DNA and other polymers. This technology may ultimately provide the basis for rapid DNA sequencing with single nanopores.



Identical length homopolynucleotides of thymine, cytosine, and adenine are driven electrophoretically through a single α -hemolysin nanopore. The polymers cause characteristic blockades in the single channel ionic current that otherwise flows freely. Decoding these signals provides information about the nanopore structure and the polymer identities.

■ *Proof-of-concept for a single molecule mass spectrometer.* Preliminary results suggest that a solitary protein nanometer-scale pore provides the basis for single molecule mass spectrometry. The pore conductance is reduced in proportion to the size of individual polymers that enter the pore. Specifically, each molecule that partitions into the pore gives rise to a well-defined conductance state that corresponds to its molecular weight. Because the polymer and nanopore sizes are commensurate, the conductance states caused by differently sized polymers are well separated. With this calibrated solution phase mass spectrometry technique, individual molecules could be further analyzed or sorted. This research is being performed in collaboration with colleagues at the Universidade Federal de Pernambuco in Brazil.

■ *Test of a model for the structure of the anthrax toxin nanopore.* Non-electrolyte polymers of poly(ethylene glycol), PEG, are being used to estimate the diameter of the PA₆₃ ion channel. Based on the ability of different molecular weight PEGs to partition into the channel, the PA₆₃ pore appears to be narrower than the one formed by *Staphylococcus aureus* α -hemolysin. These results are consistent with a recent model for the PA₆₃ channel and the crystal structure of α -hemolysin. The results place a significant constraint on models for this molecule's mechanism of action.

■ *Functional reconstitution of protein nanopores in tethered bilayer membranes: structural studies.* The crystal structures of many transmembrane proteins remain elusive. In an effort to partially address this issue, neutron reflectance is being used to obtain moderate resolution structural information about pore-forming toxins. The α -hemolysin ion channel was used as a model system because its X-ray structure is known. The technique requires reconstituting the proteins into stable, tethered bilayer membranes on a solid support. Electrochemical Impedance Spectroscopy (EIS) measurements demonstrate that the pores have the same properties as those formed in free-standing lipid bilayer membranes. Neutron reflectometry (NR) shows that the channel's large protein cap domain is located outside the membrane yet significantly affects both the lipid head group region and the alkyl chains of the outer membrane leaflet. An analysis of the neutron reflectance data, in conjunction with the channel's X-ray crystal structure, provides high-resolution structural information about the interaction between the channel and the membrane. The results suggest that the combination of EIS and NR could be used to probe the structure of other ion channels.

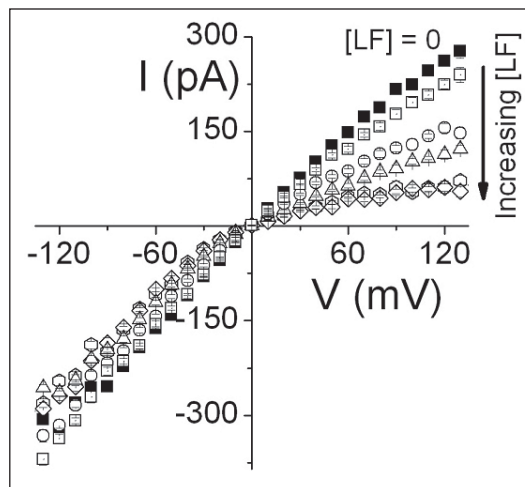
■ *Comparison of theory and experiment for ionic conduction through protein ion channels.* In collaboration with researchers at U. Pittsburgh, theoretical current-voltage (I-V) relationships for the *Staphylococcus aureus* α -hemolysin channel are being obtained via three-dimensional Poisson-Nernst-Planck (PNP) computations. The molecular structure of the channel employed is the X-ray crystal structure obtained by E. Gouaux's group at Columbia University. The theoretical predictions are being compared to NIST's experimental data for single α -hemolysin channels at several different electrolyte concentrations and pH values. When solution phase pKa values are used to fix the charge state of titrating amino acids in the protein channel, PNP results at both neutral and low pH show

large deviations from the experimental I - V data. These large deviations are reduced significantly when shifts in the pK_a 's of amino groups at the channel Rim domain are included in the model. The theoretical results suggest that the ionic permeation through the channel can be controlled by fixed charges at the channel entrance. This was verified experimentally. Similar studies are underway to test the model for the *Bacillus anthracis* PA₆₃ ion channel structure. The latter project is a joint effort between Carnegie Mellon University, the National Cancer Institute (NCI), and NIST.

■ *Mechanism of ionic conductance and ion selectivity of a mesoscopic protein nanopore probed with cysteine scanning mutagenesis.* To better understand the structure-function relationship of protein nanopores, the ion conducting properties of channels formed by wild-type and genetically engineered versions of *Staphylococcus aureus* α -hemolysin (α HL) reconstituted into planar lipid bilayer membranes were studied. The ion selectivities and current-voltage relationships of channels formed with 24 different α HL point cysteine mutants (before and after derivatizing the cysteines with positively and negatively charged sulfhydryl-specific reagents) were measured. Novel negative charges convert the selectivity of the channel from weakly anionic to strongly cationic, and new positive charges increase the anionic selectivity. The extent of these changes depends on the channel radius at the position of the novel charge (predominately affects ion selectivity) or on the location of these charges along the longitudinal axis of the channel (mainly alters the conductance-voltage curve). The results suggest that the net charge of the nanopore wall is responsible for cation-anion selectivity of the α HL channel and that the charge at the pore entrances is the main factor that determines the shape of the conductance-voltage curves.

■ *Electronic measurement of the interaction between anthrax lethal toxins.* Previous biochemical assays performed elsewhere demonstrated that full-length anthrax Lethal Factor (LF) binds strongly to the *Bacillus anthracis* PA₆₃ ion channel. A electronic assay was developed at NIST to rapidly measure the binding constant for the interaction. The binding of LF to the PA₆₃ channel converts the pore's I - V relationship from slightly nonlinear to strongly rectifying (see right figure). This method also provided the basis for a high-throughput screening assay for therapeutic agents against anthrax toxins. It was also used to demonstrate that the apparent binding constant for the complex is ~ 40 pM at pH 7.2 and is ~ 3 -fold weaker when the pH is decreased to a value similar to that in endo-

somal vesicles. These and similar results suggest that a simple reversible reaction between LF and the PA₆₃ channel is altered by changes in the local electrostatic potentials on the two proteins. This work is a collaborative effort with the U.S. Army Medical Research Institute for Infectious Diseases (USAMRIID) and the NCI.



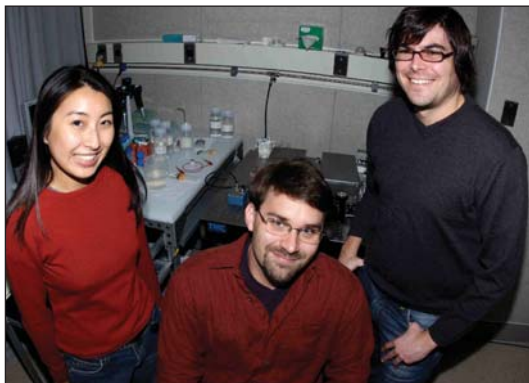
*The binding of anthrax Lethal Factor (LF) to the *B. anthracis* PA₆₃ channel markedly alters the latter's current-voltage relationship. The apparent binding constant for the interaction (~ 40 pM) is determined from the ratio of the currents in the presence and absence of LF for positive applied potentials.*

■ *Characterizing ultra-thin films for the practical use of protein nanopore technology.* Conventional planar lipid bilayer membranes permit the functional reconstitution of many transmembrane proteins. However, they are not sufficiently robust for use in practical applications. To address that issue, the ability of α -hemolysin and *Bacillus anthracis* PA₆₃ to form ionic channels when the membranes were in the fluid phase was demonstrated. In addition, the α HL channel remained functional even after UV-induced lipid polymerization. The ability to stabilize nanopores in robust films could lead to their use in a wide variety of applications including single molecule sensing, rapid DNA sequencing and single molecule mass spectrometry. However, more must be known about the state of the lipid under polymerizing conditions.

■ *The use of biomimetic membranes on solid supports to characterize enzymatic activity.* Using phospholipase as a sensitive amplifier of defect states, the structural order in the surfaces of tethered lipid bilayers on solid substrates was characterized using electrochemical impedance spectroscopy. The defect-mediated enzyme activity

on palmitoyl-oleoylphosphocholine is ~2 orders of magnitude larger than on diphytanoyl-phosphocholine surfaces and is consistent with the known mechanism of action of the lipase.

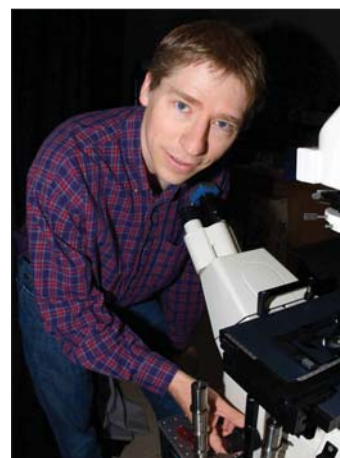
■ *NIST was awarded a patent on the use of designed protein nanopores as components for biosensors.* Based on the work initially conducted at NIST in the early 1990s, and then further developed in collaboration with a research group at Texas A&M University, a patent was awarded in 2004 for the use of engineering protein nanometer-scale pores for the electronic detection of analytes in the solution phase. Since then, NIST has made significant advances in both the types of analytes that can be detected with this method and in the information that can be extracted from polymers that interact with a nanopore.



NRC Post-doctoral fellows Elaine Chan, Brian Nablo and Joey Robertson are combining experiment and theory to study the structure and function of proteins and DNA. They are also developing novel methods for the detection and characterization of a wide variety of analytes.

■ *Personnel.* Dr. Brian Nablo (NRC Research Associate) is studying the mechanism of interactions between anthrax toxins. He is also developing new methods to probe structural features of the *Bacillus anthracis* PA₆₃ channel. Dr. Joseph W.F. Robertson (NRC Research Associate) is developing novel technical applications for single nanopore analysis of DNA and other polymeric molecules. He recently demonstrated a new method for single molecule mass spectrometry based on the interaction between individual molecules and a solitary nanopore. Dr. Elaine Chan (NRC Research Associate), who recently joined the Nanobiotechnology Project, is investigating experimentally and theoretically the physical basis of ionic conduction through the anthrax PA₆₃ channel. Dr. Joseph Reiner, formerly a NRC Research Associate in

the NIST Physics Laboratory was recently hired in our project. He is developing single molecule optical methods that will complement and extend electronic measurements on single protein and solid-state nanopores. Dr. Martin Misakian, who retired from NIST EEEL and later returned as a Guest Researcher in our project, has been using nonelectrolyte polymers to experimentally test a model for the PA₆₃ channel structure. Dr. Kenneth Rubinson (Guest Researcher) is using his expertise in chemical synthesis and analytical chemistry to further develop new technical applications based on nanopores. Louis Hromada (graduate student) is developing a microfluidic system to automate the formation of lipid bilayer membranes.



Joseph Reiner, who recently joined the Semiconductor Electronics Division, is using his expertise in single molecule detection and manipulation to better understand the mechanisms of infection by anthrax.

FY OUTPUTS

COLLABORATIONS

Carnegie-Mellon University, Dept. of Chemistry, M. Kurnikova, Comparison between theory and experiment for ion conduction through the anthrax PA₆₃ ion channel.

Carnegie-Mellon University, Dept. of Physics, and the NIST NCNR, M. Lösche, Structure of pore-forming toxins via neutron reflectivity.

Institute of Biochemistry & Vilnius Gedimino Technical University, G. Valincius, Electrochemical impedance studies of pore-forming toxins on tethered bilayer membranes.

University of Pittsburgh, Dept. of Chemistry, R. Coalson, Critical test of a theory for ion conduction through the *S. aureus* α -hemolysin ion channel.

Universidade Federal de Pernambuco, Dept. of Biophysics and Radiobiology, Recife, Brazil, O.V. Krasilnikov, Nanobiotechnological applications for protein nanopores.

National Cancer Institute, SAIC, NIH, R. Gussio, R.G. Panchal, and T.L. Nguyen, Structure and function of the anthrax PA₆₃ ion channel.

USAMRIID, Fort Detrick, Frederick, MD. S.M. Bavari, Novel methods for the rapid screening of potential therapeutic agents against anthrax toxins.

USACEHR, Fort Detrick, Frederick, MD. Major K.M., Development of nanopores for chemical detection.

University of Maryland, D. DeVoe; NIST, EEEL, SED, M. Gaitan, Development of a microfluidic device to automate the formation of planar lipid bilayer membranes.

Max Planck Institute for Polymer Research, Mainz, Germany, W. Knoll, R. Neumann, and I. Köper, Characterization of proteins and lipids using electrochemistry, surface plasmon resonance, and neutron reflectivity.

Naval Research Laboratory, D.K. Shenoy, Functional reconstitution of pore-forming toxins in polymerizable lipids.

NIST Division 831, D.J. Vanderah, Reconstitution of protein nanopores in tethered bilayer membranes for structure-function studies and biotechnological applications.

NIST Division 894, V.M. Stanford, Advanced signal processing of individual molecular interactions with single nanopores; decoding information stored in molecules.

STANDARDS COMMITTEE PARTICIPATION

Chaired the USMS committee to assess measurement needs in Nanobiotechnology (J.J. Kasianowicz)

STEERING COMMITTEE PARTICIPATION

Steering committee for the 2nd International Workshop on the Electronic Detection of Biomolecules, Urbana, IL, September 2005 (J.J. Kasianowicz)

Steering committee for the 3rd International Workshop on the Electronic Detection of Biomolecules, Liege, Belgium, September 2006 (J.J. Kasianowicz)

Steering committee for the International Workshop on Fluctuation and Noise in Biological, Biophysical, and Biomedical Systems. Florence, Italy, May 2007 (J.J. Kasianowicz)

RECENT PUBLICATIONS

J. J. Kasianowicz, T. L. Nguyen, V. M. Stanford, "Enhancing Molecular Flux Through Nanopores Via Attractive Interactions," *Proc. Natl. Acad. Sci.*, Vol. 103, No. 31, pp. 11431-11432 (01-AUG-2006)

G. Valincius, D. J. McGillivray, W. Febo-Ayala, D. J. Vanderah, J. J. Kasianowicz, M. Losche, "Enzyme Activity to Augment the Characterization of Tethered Bilayer Membranes," *J. Phys. Chem. B*, Vol. 110, pp. 10213-10216 (10-MAY-2006)

W. Pisula, M. Kastler, D. Wasserfallen, J. Robertson, F. Nolde, C. Kohl, K. Mullen, "Pronounced Supramolecular Order in Discotic Donor-Acceptor Mixtures," *Angewandte Chemie-International Edition*, Vol. 45, pp. 819-823 (23-JAN-2006)

L. H. He, J. Robertson, J. Li, I. Karcher, S. M. Schiller, W. Knoll, R. Naumann, "Tethered Bilayer Lipid Membranes Based on Monolayers of Thiolipids Mixed with a Complementary Dilution Molecule," *Langmuir*, Vol. 21, pp. 11666-11672 (06-DEC-2005)

P. Merzlyak, M. P. Capistrano, A. Valeva, J. J. Kasianowicz, O. V. Krasilnikov, "Conductance and Ion Selectivity of a Mesoscopic Protein Nanopore Probed with Cysteine Scanning Mutagenesis," *Biophysical J.*, Vol. 89, pp. 3059-3070 (01-NOV-2005)

D. H. Kim, K. A. Lau, J. Robertson, O. J. Lee, U. Jeong, J. I. Lee, C. J. Hawker, T. P. Russell, J. K. Kim, W. Knoll, "Thin Films of Block Copolymers as Planar Optical Waveguides," *Advanced Materials*, Vol. 17, pp. 2442-2444 (01-OCT-2005)

D. K. Shenoy, W. Barger, A. Singh, R. G. Panchal, M. Misakian, V. M. Stanford, J. J. Kasianowicz, "Functional Reconstitution of Ion Channels in Polymerizable Lipid Membranes," *Nano-technol. Lett.*, Vol. 5, pp. 1181-1185 (01-JUN-2005)

R. G. Panchal, K. Halverson, W. Ribot, D. Lane, T. Kenny, T. G. Abshire, J. W. Ezzell, T. A. Hoover, B. Powell, S. Little, J. J. Kasianowicz, S. Bavari, "Purified Bacillus Anthracis Lethal Toxin Complex Formed In Vitro and During Infection Exhibits Functional and Biological Activity," *Journal of Biological Chemistry*, Vol. 280, No. 11, pp. 10834-10839 (18-MAR-2005)

NANOELECTRONIC DEVICE METROLOGY

Technical Contact:
C. A. Richter

Staff-Years (FY 2006):
3.5 professionals
3.5 guest researchers
0.5 technicians

GOALS

The overall goal of the Nanoelectronic Device Metrology (NEDM) Project is to develop the metrology that will help enable emerging information processing technologies (such as Si-based quantum devices and molecular electronics) to extend electronic device performance improvements beyond the incremental scaling of Complementary Metal Oxide Semiconductor (CMOS) devices. This involves determining the critical metrology needs for these exploratory technologies. One specific goal is to develop test structures and methods to measure the electrical properties of small ensembles of molecules reliably. Another targeted goal is to develop the precise metrology and characterization methods required for the systematic characterization of Si-based nanoelectronic devices. Both of these goals involve the development of an integrated and interdisciplinary suite of sophisticated measurement capabilities that enable correlations between nanoelectronic device performance and the structure, properties, and chemistry of critical materials and interfaces within the devices.



Curt Richter loads a molecular electronic sample for electrical characterization. Copyright Robert Rathe

CUSTOMER NEEDS

The CMOS FET (Field Effect Transistor), which is the current basis of ULSI (Ultra-Large-Scale Integration) circuits, is beginning to show fundamental limits associated with the laws of quantum mechanics and the limitations of fabrication technology. The Semiconductor Industry Association's (SIA's) International Technology Roadmap for Semiconductors (ITRS) shows no known solutions in the short term for a variety of technological requirements including gate dielec-

tric, gate leakage, and junction depth. Therefore, it is expected that entirely new device structures and computational paradigms will be required to augment and/or replace standard planar CMOS devices. Two promising beyond-CMOS technologies that each take a very different fabrication approach are molecular electronics and Si-based quantum electronic devices. Molecular electronics is based upon bottom-up fabrication paradigms, while Si-based nanoelectronics are based upon the logical continuation of the top-down fabrication approaches utilized in CMOS manufacturing. These two approaches bracket the possible manufacturing techniques that will be used to make future nanoelectronic devices.

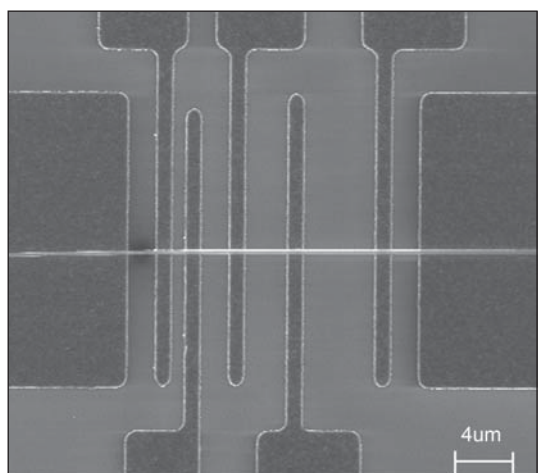
Molecular electronics (ME) is a field that many predict will have important technological impacts on the computational and communication systems of the future. In ME systems, molecules perform the functions of electronic components. Research and development for silicon-based nanoelectronics (*e.g.*, Si-nanowire FETs, Si-based RTDs [resonant tunneling diodes], and silicon quantum dots) for the post-CMOS era are currently of interest due to their inherent compatibility with existing CMOS technology.

In order to ensure the technological relevance of the NEDM Project's ongoing fundamental research associated with future devices to replace or augment standard CMOS technology, plans are aligned with research referenced in the SIA's Roadmap and other similar semiconductor industry organizations and documents as well as that described by the Microelectronics Advanced Research Corporation (MARCO). The industry for these emerging nanoelectronic devices will require reference data, standards, precision measurement methods, and standardized test structures and associated measurement protocols. The ultimate objective of this project is to provide the measurement infrastructure to aid this development. Through strong ties with industry leaders and cutting-edge researchers, the NEDM Project is accelerating the pace of its program and focusing its research on the most relevant technologies.

TECHNICAL STRATEGY

The NEDM Project investigates and is developing metrology for two specific areas of nanotechnology: (1) Si-based quantum electronics and (2) molecular electronics. The focus of the Si-based

nanoelectronics is the physical and electrical metrology of the basic building blocks of silicon quantum electronic devices (*e.g.*, quantum layers, wires, and dots of silicon surrounded by silicon dioxide). Research into emerging nanoelectronic devices is a rapidly changing and high-profile technical arena. To avoid investing too much time into a specific device geometry which may end up being an unrealistic technology, we are concentrating on the basic building blocks of such devices (such as Si-nanowires and molecular monolayers). The metrology tools and methods developed and the material and device information extracted can be applied to whichever of the myriad of possible technologies ends up being commercially preferred, positioning us to provide the necessary manufacturing metrology in a timely fashion. By identifying and addressing the critical metrology issues associated with these basic building blocks, the basis of metrology for future ULSI nanotechnology will be defined.



A silicon nanowire grown by chemical vapor deposition integrated into a transfer length method test structure to determine nanowire contact resistance.

A major goal of the Si-based quantum electronics task is to fabricate and fully characterize Si nanowires with controlled dimensions. The resulting devices will be used to establish the relationship between the key fabrication conditions, physical properties (such as the diameter of the nanowire), and final electrical properties of these Si-based nanoelectronic devices. Characterization of nanowire FETs fabricated by both (a) etching of SOI wafers (top-down methods) and (b) forming devices from chemical vapor deposition (CVD) grown Si-nanowires (a bottom-up method) is a major step en route to this end goal. This research will provide the information necessary to help identify

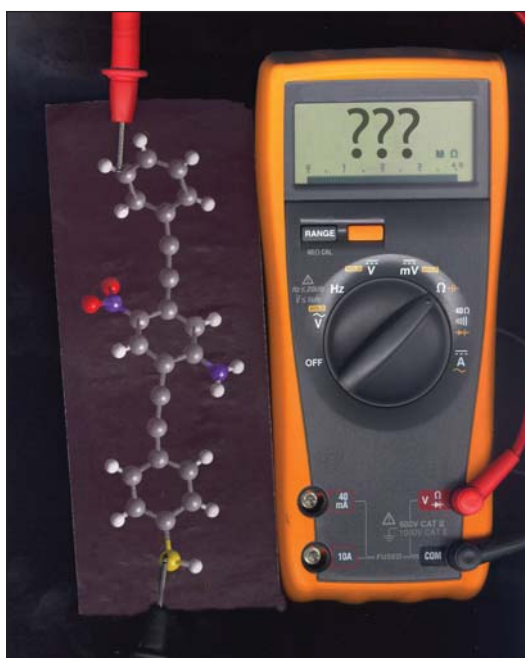
and address the necessary electrical and physical characterization methodologies.

DELIVERABLE: Complete investigation of the fundamental properties of dual-gated Schottky-contact Si-nanowire FET test structures nanofabricated from SOI wafers including two-dimensional electrostatics; prepare and submit manuscript.

DELIVERABLE: Complete development of a simple single nanowire manipulating system (SNMS) to precisely transfer and align individual nanowires into test structures for electrical characterization; prepare and submit manuscript.

DELIVERABLE: Complete systematic study of the electronic noise properties of semiconducting nanowires and nanotubes; prepare and submit manuscript.

In molecular electronics, our major objectives are a NIST standard suite of molecular test structures and a fundamental understanding of charge transport through molecules and molecular ensembles.



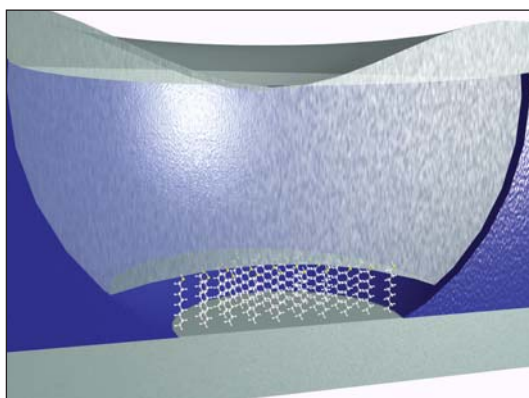
Electrically measuring molecules: the concept.

We are developing robust molecular test structures in order to use them to measure the electrical properties of molecules. Specifically, we are developing nanofabricated test-structures for assessing the electrical properties and reliability of molecular molecules. These in-house test structures and prototypical ME devices obtained from leading researchers outside of NIST are thoroughly assessed to determine if they are viable test vehicles. In addition to the complexity of the nanofabrication

of test structures, the challenges associated with measuring the electrical properties (such as current-voltage and capacitance-voltage as functions of temperature and applied fields) of these small molecular ensembles are daunting. The measured electrical properties are correlated with systematic characterization studies by a variety of advanced analytical probes and the results used in the validation of predictive theoretical models.

DELIVERABLE: Complete and document a DARPA-sponsored "round-robin" type comparison of widely-used molecular electronic test structures.

DELIVERABLE: Assess the ability of SixNy membrane nanopore-based molecular electronic test structures to characterize spin-dependent inelastic tunneling processes in molecular magnetic tunnel junctions – devices that combine features of moletronics and spintronics; prepare and submit manuscript.

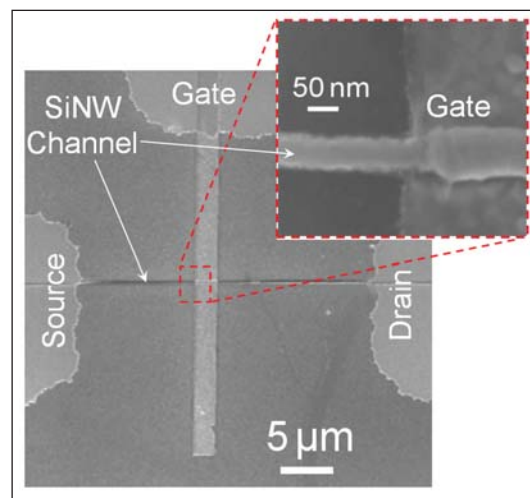


Schematic overview of a suspended SixNy membrane nanopore-based molecular electronic test structure.

A fundamental thrust of the NEDM Project is improved characterization and control of the fundamental building block of all molecular electronic devices, the molecular junction (a monolayer of molecules assembled on a conducting substrate and then contacted by a conductive top-contact material). This characterization leads to a better fundamental scientific understanding and subsequently control of the formation of the junction. Ultimately, this information is necessary to make molecular electronics a commercially viable mass-produced technology. Technically innovative devices (such as molecular spintronic devices) and characterization approaches (*e.g.*, on-chip CMOS circuitry for ME device characterization) are also being pursued.

DELIVERABLE: Determine metal/molecular-monolayer interactions by utilizing our novel backside FTIR-based technique to thoroughly characterize top-metal/molecular interfaces and correlate the results with electrical device performance; prepare and submit manuscript.

Developing the metrology for emerging nano-electronic devices is a challenging and multi-disciplinary task; therefore, it is important to be teamed with strong collaborators. By working with established leaders in new technologies (such as HP Research Labs, Harvard, and IBM – see more complete list below), we can more quickly shift to new areas as they arrive and establish ourselves at the scientific forefront.



A dual-gate Si nanowire field-effect transistor.

ACCOMPLISHMENTS

■ *Spin-polarized Inelastic Electron Tunneling Spectroscopy of a Molecular Spintronic Device Investigated by EEEL Researchers.* Molecular-monolayer magnetic tunnel devices have been fabricated and characterized via sophisticated tunneling spectroscopy. Molecular spintronic systems were fabricated by sandwiching a self-assembled monolayer of octanethiol between two ferromagnetic electrodes in a nanopore, demonstrating that single molecules can be used as the ultimate building blocks for spintronic devices. By using inelastic electron tunneling spectroscopy (IETS), **the first unambiguous experimental evidence of the existence of molecular species in such magnetic tunnel junctions was obtained.** Tunneling spectroscopy was also utilized to investigate the spin-polarized inelastic electron tunneling processes in the molecular devices. The measurements revealed that inelastic scattering due to molecular vibrations is likely the main cause of an observed junction

magnetoresistance bias-dependence. These results illustrate that such inelastic scattering events must be accounted for when predicting the performance of practical molecular spintronic devices. Molecular electronic devices with spin-dependent tunneling transport behavior offer an innovative and extremely enticing direction towards spin electronics, both from fundamental and technological points of view. Due to the weak spin-orbital and hyperfine interactions in molecules, the spin coherence over time and distance could be preserved much longer in molecular nanosystems than in traditional semiconductors, which makes them a suitable playground for spin manipulations.

■ *Novel Approach to Investigate Buried Metal-Organic Interfaces for Molecular Electronics Developed and Utilized.* In collaboration with CSTL, researchers in the NEDM have co-developed a novel characterization approach based upon backside-incident FTIR spectroscopy to investigate the top metal contact in metal-organic monolayer devices. In the emerging arena of molecular electronics, detailed characterization of organic monolayers encapsulated between two electrodes is necessary to correlate the electrical responses of molecular devices with the fundamental physical properties of the monolayers. The technique developed at NIST takes advantage of the natural infrared transparency of Si wafers to enable vibrational characterization of monolayer films after deposition of a technologically relevant metal electrode. The samples, as prepared, encapsulate the organic layer in exactly the same manner as fully fabricated devices. IR and electrical samples were fabricated simultaneously, allowing direct comparison of the spectroscopic results with electrical device performance.

■ *Characterization of Interfaces in Molecular-Monolayer/SiO₂ Based Molecular Junctions.* The results of dc-current-voltage (IV) and ac-capacitance-voltage (CV) measurements were correlated with vibrational spectroscopy of Au/monolayer/SiO₂/Si structures to establish an improved understanding of the interactions at the buried metal/monolayer and dielectric/silicon interfaces. Towards the goal of observing and characterizing electrical device behavior based upon intrinsic molecular effects, the role of test structures and their interfaces must be understood and eventually effectively controlled. The novel backside-incidence Fourier-transform infrared-spectroscopy technique previously developed by members of the NIST research team was used to characterize the buried metal/molecule interface to probe the interaction of the top-metallization with the organic monolay-

ers. Both the spectroscopic and electrical results indicate that Au has a minimal interaction with alkane monolayers deposited on SiO₂ via silane chemistry. An intriguing negative-differential-resistance and hysteresis was observed in the IV measurements of Au/alkane/SiO₂/Si devices. It is unlikely that this behavior is intrinsic to the simple alkane monolayers in these structures. Based on the results of extensive electrical characterization, the observed IV features are attributed to charge trapping and detrapping at both the alkane/SiO₂ and the Si/SiO₂ interfaces. These data illustrate that the dielectrics and other materials used when fabricating molecular devices must be made at the highest level of control to avoid impurities and defects which are likely to lead to spurious device behavior.

■ *Process Developed to Align Single Nanowires and Form Electrical Test Structures.* A system to precisely maneuver and align individual nanowires has been developed and successfully experimentally demonstrated. This system, in which a single nanowire can be picked up and transferred to a pre-defined location by electrostatic force, overcomes a significant research challenge: the integration of semiconductor nanowires into electrical test structures. Compatible fabrication processes have been developed to simultaneously pattern multiple aligned nanowires by using one level of photolithography to fully integrate the nanowires into test devices for electrical characterization. Representative devices and test structures including bottom-gated silicon nanowire field-effect transistors and both transfer-length-method and Kelvin test structures have been fabricated and characterized. In addition, novel Si-nanowire-based nanoelectromechanical (NEMS) switches were made and observed to have large on/off current ratios. All these devices were fabricated from Si-nanowires grown by NEDM staff in-house at NIST by using a catalytically controlled chemical-vapor process. The fabrication of various test structures and devices by using one regular photolithographic step indicates that this novel single nanowire manipulation approach is an attractive strategy to integrate nanowires for research device applications.

■ *Silicon nanowires as enhancement-mode Schottky-barrier field-effect transistors.* We have shown that SiNWs with Schottky contacts can be used as enhancement-mode FETs with an excellent on/off current ratio. The process does not require any source and drain doping or silicide formation, thereby allowing for a simple process without thermal annealing. Silicon nanowire field-effect

transistors (SiNW FETs) were fabricated with a highly simplified integration scheme to function as Schottky barrier transistors with excellent enhancement-mode characteristics and a high on/off current ratio $\sim 10^7$. SiNW FETs show significant improvement in the thermal emission leakage ($\sim 6 \times 10^{-13}$ A/ μm) compared to reference FETs with a larger channel width ($\sim 7 \times 10^{-10}$ A/ μm). The drain current level depends substantially on the contact metal work function as determined by examining devices with different source-/drain- contacts of Ti (≈ 4.33 eV) and Cr (≈ 4.50 eV). The different conduction mechanisms for accumulation- and inversion-mode operation were determined and confirmed by comparison with two-dimensional numerical simulation results. Schottky barrier FETs are of great interest in their own respect as an alternative to traditional doped source and drain device structure, because sub-100 nm range scaling encounters fundamental problems including high leakage current and parasitic resistance. Schottky barrier FETs have a number of advantages including simple and low-temperature processing, good suppression of short-channel effects, and the elimination of doping and subsequent activation steps. These features are particularly desirable for SiNW devices because they can circumvent difficult fabrication issues such as an accurate control of the doping type/level and the formation of reliable ohmic contacts.

■ *Two-dimensional Electrostatics Enhance Channel Modulation in Dual-gated Silicon Nanowire Devices.* Enhanced channel modulation in dual-gated SiNW FETs has been experimentally observed. SiNW FETs were fabricated by using electron-beam lithography to investigate the electrostatic control of current in semiconductor nanowire devices. These novel top- and bottom-gated FETs are based upon simple top-down test structures that rely upon self-aligned Schottky-contacts to enable the electronic properties of SiNWs to be readily studied. Improved device performance is observed for the dual-gated SiNW FETs when compared to simultaneously fabricated large area control FETs. The SiNW devices (with widths down to approximately 60 nm) exhibit an on/off current ratio greater than 106, which is more than 3 orders of magnitude higher than that of control devices prepared simultaneously having a large channel width (5 μm). In addition, the top gate is found to suppress ambipolar conduction effectively, which is one of the factors limiting the use of nanotube or nanowire FETs for complimentary logic applications. Two-dimensional numerical simulations have confirmed an important physical

insight illustrated by this work: due to the reduced dimensionality of SiNWs, electrostatic control is enhanced when compared to larger channel width devices.

■ *Enhanced Inversion Mobility in Silicon Nanowire Field Effect Transistors Demonstrated.* Dr. Sang-Mo Koo and colleagues have demonstrated that SiNW FETs fabricated by a standard ‘top-down’ approach exhibit substantially enhanced transport performance. A systematic study on the inversion electron transport properties of SiNWs with different channel geometries has shown that a SiNW device exhibits enhanced inversion channel current density: the extracted electron inversion mobility of the 20 nm width nanowire channel (1000 cm^2/Vs) is found to be 2 times higher than that of the reference MOSFET of large dimension ($W > 1 \mu\text{m}$). The enhancement is attributed to the possible suppression of inter-valley phonon scattering due to strain in SiNW caused by the oxidation process. As the feature sizes of FETs are scaled downward, the semiconductor industry is working to meet the increasing challenges of nanoscale devices that are smaller and yet can be manufactured with minimal deviation from today’s standard manufacturing processes. These results strongly suggest that lithographically fabricated SiNW FETs, which are compatible with Si ULSI technology, can bring about significant performance benefits in nanoscale electronics, preserving the basic silicon technology infrastructure upon which current industry relies.

■ *Joint NIST/HP Research Progresses Toward Critical Molecular Electronics Measurements.* Research at the NEDM and Hewlett Packard (HP) Laboratories is progressing toward reliable methods for measuring the electrical behavior of molecular electronic devices, an emerging nanotechnology eyed for future integrated circuits. By using a crossbar test structure consisting of a molecular monolayer sandwiched between a series of perpendicular metal wires, collaborators at separate facilities recorded nearly identical electrical measurements. This step, along with others taken to eliminate potential sources of error, ensures that the measured behavior is directly attributable to the device and not the experimental set up. Electrical (current-voltage, or IV) measurements of crossbar devices containing eicosanoic acid exhibit a controllable, two-state switching behavior that is due to the presence of the molecular layer. However, the molecular monolayer is not the sole cause. Rather, the switch-like behavior most likely arises from the interaction of the molecules with the electrodes. This example illustrates that the properties of mo-

molecular electronic devices are often determined not by the molecule alone, but by the entire device that consists of both the molecules and the attachment electrodes. This two-state behavior was independently measured in two separate laboratories, indicating that it is not a measurement artifact and illustrating that these devices are robust enough to ship via conventional methods and remain active. In addition to IV measurements, what we may be the first capacitance-voltage (CV) measurements of molecular monolayer-based devices were taken at NIST. These CV curves also show two-state behavior.

■ *Improved Methods to Attach Long-Chain Aliphatic Molecules to Silicon Developed.* Dr. Christina Hacker and colleagues have developed an improved solution-based method for the direct attachment of long-chain aliphatic molecules to Si. In this method, ultraviolet (UV) radiation is used to assist the attachment of alcohols to the hydrogen-terminated Si(111) surface to form molecular monolayers successfully. To investigate the quality of these organic monolayers, they were physically and chemically characterized with infrared spectroscopy, spectroscopic ellipsometry, and contact angle measurements. The electrical properties of these organic films were probed by using IV and CV measurements obtained from a metal-organic-silicon test structure fabricated by post-monolayer metal deposition.

FY OUTPUTS

COLLABORATIONS

Gwangju Institute of Science and Technology (GIST), Korea, Prof. Takhee Lee, Properties of novel nanoelectronic devices.

Harvard University, Prof. Charlie Lieber, Characterization of semiconductor nanowire devices.

Hewlett-Packard, R. Stanley Williams, Interface properties of molecular electronic test structures.

IBM, Joerg Appenzeller, Noise properties of CNT-based nanoelectronic devices.

Kwangju University, Korea, Prof. Sang-Mo Koo, Metrology for Si-nanowire field effect transistors.

NIST Division 817, Dr. Neil Zimmerman, Metrology for nanoelectronic devices.

NIST Division 837, Dr. L. Richter, Optical characterization of molecular and organic interfaces.

NIST Divisions 836 and 837, Dr. Roger van Zee and James Kushmerick., Molecular electronics.

NIST Division 854, Dr. Eric Lin et al., Applications for conducting polymers.

NTT, Akira Fujiwara, Si-nanowire metrology.

Texas A&M University, Prof. James Batteas, Electrical characterization of self-assembled nanoelectronics.

Yale University, Prof. M. A. Reed, Robust molecular electronic test structures.

RECENT PUBLICATIONS

Q. Li, S.-M. Koo, C. A. Richter, M. D. Edelstein, J. E. Bonevich, J. J. Kopanski, J. S. Suehle, E. M. Vogel, "Precise Alignment of Single Nanowires and Fabrication of Nanoelectromechanical Switch and Other Test Structures," IEEE Transactions on Nanotechnology (Accepted for Publication, August 5, 2006)

W. Wang, C. A. Richter, "Inelastic Electron Tunneling Spectroscopy of Molecular Magnetic Tunnel Junctions," Applied Physics Letters (09-OCT-2006)

S. M. Koo, C. A. Richter, Q. Li, M. D. Edelstein, E. M. Vogel, "Schottky-contact Silicon Nanowire Field Effect Transistor Test Structures," 2006 IEEE Silicon Nanoelectronics Workshop, Jun 11-12, 2006, Honolulu, Hawaii, pp. 821-822 (01-AUG-2006)

Q. Li, S. M. Koo, C. A. Richter, M. D. Edelstein, J. J. Kopanski, J. S. Suehle, E. M. Vogel, "Precise Manipulation and Alignment of Single Nanowires for Device Fabrication," 2006 IEEE Silicon Nanoelectronics Workshop, Jun 11-12, 2006, Honolulu, Hawaii, pp. 1011-1012 (01-AUG-2006)

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C. Hacker, C. A. Richter, L. J. Richter, "IR Spectroscopic Characterization of the Buried Metal Interface of Metal-Molecule-Silicon Vertical Diodes," *Characterization and Metrology for ULSI Technology*, Mar 14-18, 2005, Richardson, Texas, pp. 610-614 (28-SEP-2005)

S. Koo, M. D. Edelstein, Q. Li, C. A. Richter, E. M. Vogel, "Silicon Nanowires as Enhancement-mode Schottky-barrier Field-effect Transistors," *Nanotechnology*, Vol. 16, pp. 1482-1485 (29-JUN-2005)

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MACRO ELECTRONICS

GOALS

The overall goal of the Macro Electronics Project is to develop the metrology that will help enable broad commercialization of macro electronic technologies, such as printed organic electronics. This involves determining the critical metrology needs for emerging macro electronic device technologies as well as established ones to be employed in entirely new applications. The project is currently focused on organic-based thin film transistor (OTFT) technology which makes use of soluble organic semiconductors for fabricating transistors on arbitrary substrate materials such as flexible plastic films. The near term goals include the establishment of the infrastructure necessary to fabricate organic devices with state-of-the-art performance, temperature-dependent current-voltage measurement capability to correlate device performance with the film microstructure, and numerical modeling of devices to evaluate the impact of parasitic effects and device design on the device operation and extrinsic performance. Long term goals include the development of expanded interdisciplinary measurement capabilities which enable correlations between organic electronic device performance and the structure, properties, and chemistry of critical materials and interfaces.

CUSTOMER NEEDS

Silicon (Si) CMOS FET (Field Effect Transistor) technology has provided a cost-effective high performance solution to many electronic needs. Cost reductions and improvements in performance rely on continued miniaturization of the individual FETs comprising the CMOS circuitry; following a decades old scaling trend commonly referred to as Moore's Law. A growing number of current and new electronic applications however do not benefit from the high performance of state-of-the-art Si CMOS and nanometer scale device geometries achieved through continued Moore's Law scaling. This is particularly true for macro electronic applications such as printable large-area displays, wearable electronics, paper-like electronic newspapers, low-cost photovoltaic cells, ubiquitous integrated sensors, and radio-frequency identification (RFID) tags. For many of these applications the use of or integration with Si CMOS is often technologically prohibitive or too costly. Organic electronics are expected to revolutionize the future of macro electronics through the development of new appli-

cations that leverage advantages in low-cost, high volume manufacturing, nontraditional substrates, and chemically-tailored functionality.

To address industrial stakeholder needs and facilitate the commercialization of macro electronic applications, the Macro Electronics Team actively participates in industrial roadmap activities, such as the drafting of one specific to printed and organic electronics which is now being considered for adoption by iNEMI. Early identification of the required material, device, and system properties for the different macro electronic applications is crucial to establishing a competitive, robust, and profitable industry. Industrial roadmaps play a critical role in focusing attention and resources on potential roadblocks related to manufacturing and ones intrinsic or fundamental to the different device technologies.

The timely development of metrology to meet industry's needs is also of paramount importance. In March 2006, the Macro Electronics Team co-organized a workshop held at NIST on *Metrology Needs for Flexible Electronics*. Representatives from industry and academia attending the workshop identified the following device and circuit specific metrology needs as critical for commercializing flexible electronics: 1) accelerated lifetime testing and reliability physics, 2) accurate physical models for predicting and simulating the electrical characteristics of thin film devices, and 3) characterization techniques to determine the electronic structure at critical device interfaces.



Modular glove box system in which organic electronic devices are fabricated and their initial current-voltage characteristics measured.

Technical Contact:
David Gundlach

Staff-Years (FY 2006):
1.3 professionals
0.5 technicians

"We're very optimistic about the demand for printed electronics. IDTechEx estimates that printed electronics will grow to \$30 billion in 2015 and reach \$250 billion by 2025"

*Peter Gammel, CTO
Advance Nanotech*

"The non-Moore's Law progress to come will be as stunning as the Moore's Law progress has been"

*Tom Jackson, Professor of
Electrical Engineering,
Penn State University*

TECHNICAL STRATEGY

The Macro Electronics Project is currently focused on developing metrology specific to printed organic electronics. The present state of organic electronics is analogous to the early stages of the silicon semiconductor industry, with the concurrent development of multiple material platforms and processes, no standardization of measurements between laboratories, and a lack of diagnostic probes, tools, and methods necessary to address critical technological challenges. A principal goal of the organic electronics program is to determine experimentally the correlation between device performance and the structure, properties, and chemistry of critical materials and interfaces. A prerequisite to meeting this goal is to develop a set of test structures, fabrication techniques, and measurement methodologies to characterize the electrical properties of OTFTs.

To do this, the Macro Electronics Team is developing electronic test (E-test) structures capable of being reproducibly fabricated in different research laboratories to allow results from the different research groups to be better evaluated. We are establishing the infrastructure needed to reproducibly fabricate devices with state-of-the-art performance and to perform detailed characterization of their electrical properties.

DELIVERABLE: Establish infrastructure to fabricate solution processed OTFTs with state-of-the-art electrical performance.

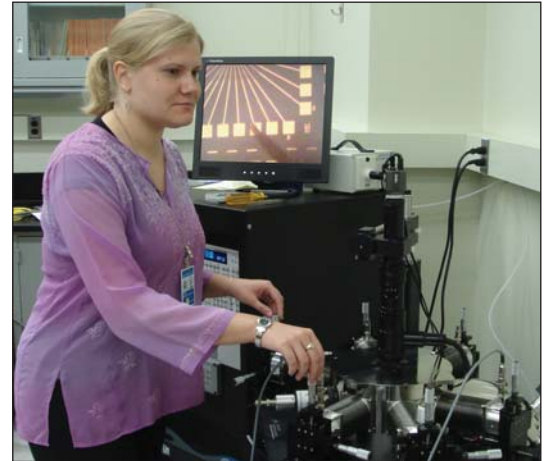
Studying the temperature dependence of the electrical properties is crucial to understanding fundamental electronic processes such as charge injection, transport, and trapping, and correlating the device performance with the microstructure, molecular design, and chemistry at critical interfaces.

DELIVERABLE: Develop measurement infrastructure needed to characterize the temperature dependence of the electrical characteristics of macro electronic devices, and correlate microstructure and performance.

Parasitic contact effects related to charge injection and the device design (inherent to the 2-dimensional device structure) all contribute to deviations from ideal FET behavior. Simplistic equations used to model the electrical characteristics of OTFTs do not adequately account for such effects; making device parameterization and comparison of results among laboratories exceeding challenging. We are using finite element 2-dimensional drift-diffusion numerical simulations to better understand parasitic effects related to the contacts, charge injection,

and device design as they relate to OTFT device operation and limitations to the use of conventional methods for device parameterization.

DELIVERABLE: Perform numerical simulations for different OTFT designs and OTFTs with source/drain contacts having different work functions.



Vacuum cryogenic probe station used to characterize the electrical properties of macro electronic devices (OTFTs in particular), as well as nano-scale devices (molecular devices and nanowire FETs).

Trap/defect spectroscopy techniques were critical to developing a detailed knowledge of the electronic structure of Silicon and played a central role in advancing Silicon as the dominant technology in the microelectronics industry. In contrast, there is surprisingly little known about the electronic structure of organic semiconductor materials. Thus, developing similar metrology to quantify the density and distribution in energy of electrically active states in the mobility gap and their origin (chemical or structural) is crucial to improving organic semiconductor device performance and reliability. Long term program goals will focus on the development of transient current-voltage and photo-current spectroscopy techniques to address the metrology needs related to defect spectroscopy. Integral to developing these techniques is the concurrent development of appropriate test structures, measurement protocols, and models for accurate data analysis.

DELIVERABLE: Perform numerical simulations for OTFTs of different designs and for OTFTs with source/drain contacts having different work functions.

Stable and reliable electronic performance is required for the commercialization of organic macro electronic applications. Instabilities in the electronic properties of organic devices related

to environmental exposure and bias temperature stress has not been well-studied. Consequently, physical models which accurately describe instabilities and can predict the operational lifetime of organic devices remain under-developed and largely empirical. To address this, the Organic Electronics Team is establishing the infrastructure, test protocols, and data analysis methodology to conduct accelerated lifetime testing of organic devices with the goal of identifying intrinsic and extrinsic failure mechanisms, and developing the necessary reliability physics and models needed to describe device instabilities and predict device operation lifetime.

DELIVERABLE: Develop the accelerated life testing methodology and reliability physics necessary for commercializing organic devices.

There is renewed interest in existing and new forms of solar energy. Organic-based photovoltaic (OPV) devices are of particular interest given their potential to be manufactured at low-cost on light weight plastic sheets using print and roll-to-roll processing. OPV devices are currently in a R&D phase, and substantial improvements in performance are needed if OPV devices are to contribute to realizing the Solar America Initiative (SAI) goal of making photovoltaics cost-competitive with other forms of renewable electricity by 2015. The Organic Electronics Team looks to develop the metrology needed to characterize charge pair generation, diffusion, dissociation, and transport, which are inherent to efficient device operation, and correlate these processes with the molecular design and device fabrication methods. To do this, the Team will establish the infrastructure to fabricate high performance hybrid OPV test structures and characterize their electronic properties using transient microwave conductivity spectroscopy.

DELIVERABLE: Establish infrastructure needed to fabricate hybrid organic devices.

DELIVERABLE: Develop measurement infrastructure needed to characterize fundamental processes crucial to efficient OPV device operation.

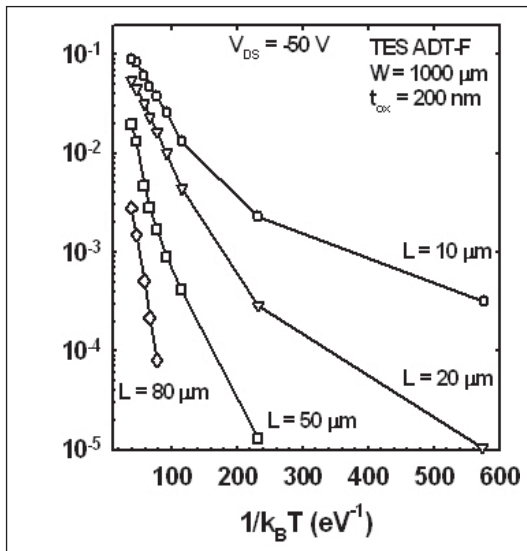
ACCOMPLISHMENTS

■ *Establishing Infrastructure for the Macro Electronics Project.* In FY 2006, the Macro Electronics Project was established and integrated the joint MSEL/EEEL/CSTL Organic Electronics Competence (started FY 2005, originally under the Nanoelectronic Device Metrology Project). There are two areas of infrastructure that have been improved: personnel and equipment. Specifically,

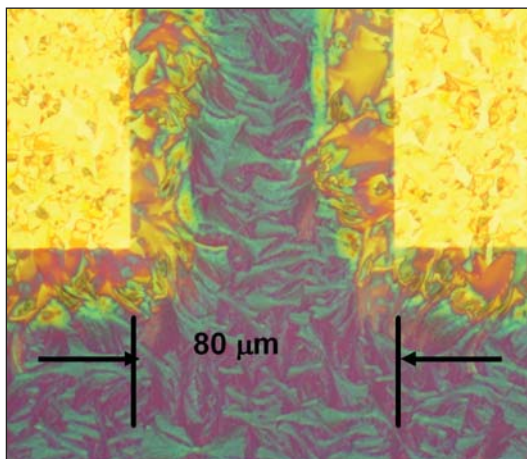
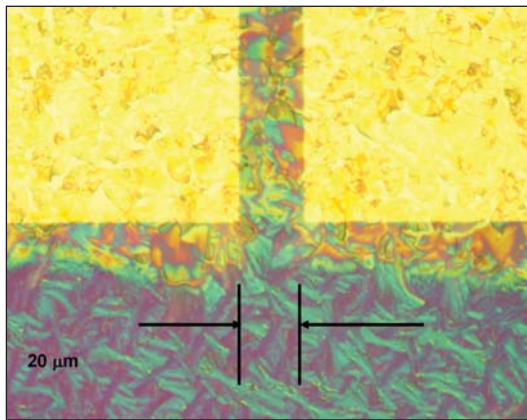
one full-time researcher joined NIST and the Macro Electronics Project, and the infrastructure needed to reproducibly fabricate organic devices with state-of-the-art performance and characterize the temperature dependence of their electronic properties was established.

■ *Joint NIST/Penn State U./U. Kentucky Study on Solution Processed Small-Molecule Thin Film Transistors.* Research between the Macro Electronics Project, Penn State U., and U. Kentucky is progressing towards solution processed small-molecule TFTs with performance suitable for commercial applications. Organic semiconductors with chemically tailored properties are synthesized for improved molecular packing, chemical stability, and charge injection by the U. Kentucky Group. The semiconductor materials are used to fabricate discrete devices on NIST designed E-test structures. The temperature dependence of the electrical properties is measured, and key device parameters, such as field-effect mobility, are extracted for correlation with the device processing methods and film microstructure. The results of these studies are used by the Penn State U. Group to fabricate simple logic circuits and ring oscillators and are used in verifying and validating results from discrete devices fabricated by either group.

Through this collaboration we have fabricated solution processed OTFTs with state-of-the-art performance in our laboratory. The soluble small-molecule organic semiconductor materials synthesized by the U. Kentucky Group have strong crystal forming properties, even when deposited by spin casting. Modifying the surface energy of the silicon dioxide gate dielectric and the source/drain contacts using molecules that form a self-assemble monolayer was found to strongly influence the film forming properties. For certain process conditions, highly ordered regions (large grains) were found to form along the contact edges and extend 10's of micrometers into the channel region of the device. The temperature dependence of the extracted extrinsic field-effect mobility and the film microstructure in the channel were strongly correlated.

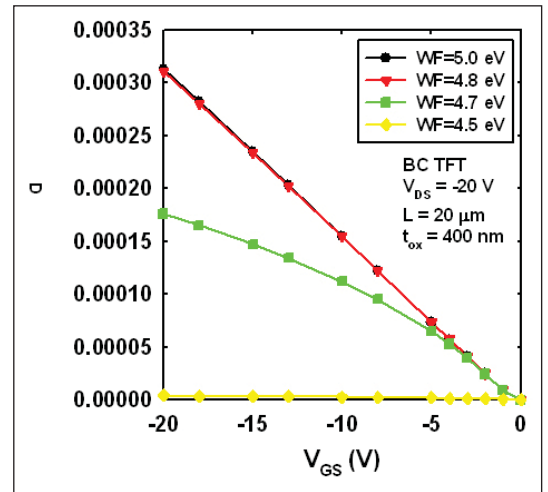


The temperature dependence of the extracted effective field-effect mobility plotted for OTFTs with different channel lengths.



Optical micrographs showing film crystallization along the source/drain contact edge. The top micrograph shows the OTFT channel to be comprised of large grains. The bottom micrograph shows a region of poorly-ordered film between the crystalline regions for an OTFT with a longer channel length (4X longer).

■ *Numerical Simulations of Design and Contact Related Effects for Organic Thin Film Transistors.* Field-effect mobility for OTFTs is most often extracted for devices biased in the saturation regime. Plotting the square-root of the drain current as a function of the gate voltage yields a straight line for a well-behaved square-law device (ideal FET). It is from the slope of a line fitted to the linear part of this curve that the field-effect mobility is calculated. The threshold voltage is given by intercept. Using the 2-dimension drift diffusion program PISCES 2B numerical simulations were made for organic devices employing the NIST OTFT E-test structure and source and drain contacts with different work functions (WFs). For an organic semiconductor with a valence band edge located 5 eV below the vacuum level, a contact with a work function smaller than 4.8 eV causes a significant deviation from ideal square-law behavior; preventing the determination of values for field-effect mobility and threshold voltage which reflect the intrinsic properties of the organic semiconductor.



Numerical simulations of the transistor characteristics for OTFTs with source and drain contacts having different work functions.

■ *Personnel.* Since the project was formed in 2006, one full-time researcher has joined NIST and the Macro Electronics Project. Dr. David J. Gundlach (Penn State U.) was hired as the project leader after working on organic light emitting devices as a post-doctoral candidate at IBM Research Laboratory in Zürich, Switzerland, and leading an organic electronics research group at ETH, Zürich, Switzerland. Two post-doctoral researchers are expected to join the project in the 2007 fiscal year.

FY OUTPUTS

COLLABORATIONS

Penn State University, Tom Jackson, Fabrication of solution processed organic transistors.

University of Kentucky, John Anthony, Organic semiconductor material design and synthesis.

University of Texas at Austin, Lynn Loo, Segregated polymer/small-molecule blends for solution processed organic transistors.

Merck, Iain McCullough et al., Organic semiconductor material design and synthesis.

NIST Division 854, Dr Eric Lin et al., Organic Electronics Competence Project.

NIST Division 837, Dr. L. Richter et al., Organic Electronics Competence Project.

EXTERNAL RECOGNITION

Technical Program Committee Member, Device Research Conference 2006 to present (David J. Gundlach)

Organic Field Effect Transistor Conference Co-Chair, SPIE 2005 to present (David J. Gundlach)

RECENT PUBLICATIONS

D. M. DeLongchamp, B. D. Vogt, C. M. Brooks, K. Kano, J. Obrzut, C. A. Richter, O. Kirillov, E. K. Lin, "Influence of a Water Rinse on the Structure and Properties of poly(3,4-ethylene dioxothiophene):poly(styrene sulfonate) Films," *Langmuir*, Vol. 21, No. 24, pp. 11480-11483 (22-NOV-2005)

D. M. DeLongchamp, B. M. Vogel, Y. Jung, M. C. Gurau, C. A. Richter, O. Kirillov, J. Obrzut, D. A. Fischer, S. Sambasivan, L. J. Richter, E. K. Lin, "Variations in Semiconducting Polymer Microstructure and Hole Mobility with Spin-Coating Speed," *Chemistry of Materials*, Vol. 17, No. 23, pp. 5610-5612 (15-NOV-2005)

ADVANCED MOS DEVICE RELIABILITY AND CHARACTERIZATION

Technical Contact:
John S. Suehle

Staff-Years (FY 2006):
2 professionals
1 technician
3 guest researchers

GOALS

The goal of this project is to provide electrical and reliability measurement techniques, data, physical models, and fundamental understanding for advanced materials and devices in future Metal Oxide Semiconductor (MOS) devices. The project specifically aims to increase the understanding of the relationship between the gate dielectric material/interface properties and device electrical and reliability measurements.



The project's renovated laboratory space.

CUSTOMER NEEDS

The MOSFET (Metal Oxide Field Effect Transistor), which is the current basis of ULSI (Ultra-Large-Scale Integration) circuits, is beginning to show fundamental limits associated with the laws of quantum mechanics and the limitations of fabrication techniques. The evolving decrease of the gate dielectric film thickness to an oxide-equivalent value of 2 nm is identified as a critical front-end technology issue in the Semiconductor Industry Association's (SIA's) International Technology Roadmap for Semiconductors (ITRS) with effective thickness values of 0.9 nm or less being projected in 2008, dropping to 0.65 nm or less by 2010. To achieve these effective gate dielectric thicknesses, SiO₂ must be replaced by either metal-oxides or compounds such as metal-silicates.

Due to increased power consumption associated with SiO₂ of this thickness, a high permittivity gate dielectric (*e.g.*, Si₃N₄, HfSixOy, ZrO₂) with low leakage current and at least equivalent capacitance, performance, and reliability will be required. The physics of failure and traditional reliability testing techniques must be reexamined for advanced gate

oxides comprised of high- κ dielectric materials. Electrical characterization of Metal Oxide Semiconductor (MOS) capacitors and Field Effect Transistors (FETs) has historically been used to determine device and gate dielectric properties such as insulator thickness, defect densities, mobility, substrate doping, bandgap, and reliability. Electrical and reliability characterization methodologies need to be developed and enhanced to address issues associated with alternate dielectrics including large leakage currents, quantum effects, and thickness dependent properties. As compared to SiO₂, very little is known about the physical or electrical properties of high dielectric constant gate dielectrics in MOS devices. The use of these films in CMOS technology requires a fundamental understanding of the relationship between the gate dielectric material/interface and device electrical and reliability measurements. Defects, as well as interfacial reaction products, at the metal gate electrode/high- κ gate dielectric interface may impact the work function of the gate electrode and the band offset between the gate dielectric and the electrode. Therefore, the development of methodologies to determine the band structure and barrier heights of the high- κ /gate metal electrode stack is required.

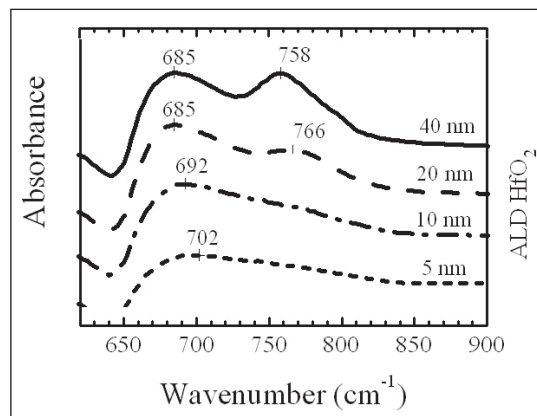
The project is also investigating the reliability of the SiO₂/SiC material system and top and bottom gated nanowire MOSFET devices.

TECHNICAL STRATEGY

The strategy of this effort is to develop robust electrical characterization techniques and methodologies to characterize charge trapping kinetics, V_t instability, defect generation rates, and time-dependent dielectric breakdown (TDDB) for both patterned device samples and blanket films obtained from our collaborators. The need for ultrafast measurements becomes more important to avoid relaxation effects when characterizing charge trapping in complicated stacked dielectric systems. Such techniques are also required to compensate transient electron trapping occurring at the remote high- κ /SiO₂ interface, which has been shown to interfere with electrical characterization associated with negative bias temperature instability (NBTI), positive bias temperature instability (PBTI), and defect generation due to voltage stress.

Studies will be conducted to determine the effect of multiple interfaces on stress-induced defect generation and wear-out. It will be determined what technique or combination of techniques provides the most consistent results for all films. The electrical results will be used to validate simulation models and compared to studies from various analytical materials characterization methods. A study of the methodologies required to extract the work functions and band offsets of the metal electrode/high- κ gate dielectric system will be performed. Because of limitations associated with any single technique, we believe that determination of band offsets and work functions requires the use of an array of techniques and the broad expertise available at NIST. We will focus our efforts on the following measurements: standard Capacitance-Voltage (CV) and tunneling current-voltage (IV) measurements, internal photoemission (IPE), and Scanning Kelvin Probe Microscopy (SKPM).

The understanding generated in this research will be used to continue generating standard measurements through a NIST-coordinated collaboration between EIA-JEDEC (Electronic Industries Association-Joint Electron Device Engineering Council) and the ASTM (American Society for Testing and Materials). Studies on the reliability of high dielectric constant dielectrics also will be performed.



IR absorption measured by enhanced sensitivity Attenuated Total Reflectance Fourier Transform Infrared (ATR-FTIR) spectroscopy. The plot shows that the thicker 20 nm and 40 nm HfO₂ films contain a substantial fraction of polycrystalline material.

DELIVERABLE: Develop ultra-fast current-voltage and “On-the-fly” characterization of charge trapping in high- κ and SiO₂/SiC MOSFETs.

DELIVERABLE: Use scanning Kelvin probe microscopy (SKPM), CV, and IPE to determine band diagram and barrier heights of high- κ stacks on III-V substrates.

DELIVERABLE: Characterize 1/f noise and random telegraph signals in Si and ZnO nanowire MOSFET devices.

DELIVERABLE: Improve efficiency of internal photo emission system and demonstrate performance on metal/high- κ /Si structures to determine band offsets.

DELIVERABLE: Conduct comprehensive time-dependent dielectric breakdown (TDDB) study on SiO₂/SiC devices.

ACCOMPLISHMENTS

■ *Fundamental Understanding of Metal Gate Workfunction and Barrier Height Measurements using CV analysis.* CV measurements were performed on TaN/TaSiC/HfO₂/SiO₂, TaN/TaCN/HfO₂/SiO₂, TaN/TaSiC/SiO₂, and TaN/TaCN/SiO₂ stacks provided by SEMATECH. The HfO₂ films were deposited on a single wafer with a SiO₂ interfacial layer that varied in thickness such that the metal workfunction could be obtained by extrapolating the CV flatband voltage to 0 EOT (equivalent oxide thickness). The CV curves were modeled using the NCSU CVC program (CV analysis software developed by the North Carolina State University), and the workfunction was obtained from the SiO₂ thickness dependence. The effective workfunction of 4 nm TaSiN (4.13 eV) is approximately 0.25 eV smaller than that of 4 nm TaCN (4.38 eV). The effective workfunction of these metals on HfO₂ is observed to be \approx 0.3 eV smaller than on SiO₂.

■ *Film thickness dependence of sub-bandgap defect states observed in polycrystalline hafnium oxide.* We compare hafnium-based high- κ dielectric films grown by MOCVD (metalorganic chemical vapour deposition) and ALD (Atomic Layer Deposition). MOCVD-grown HfO₂ films are mostly monoclinic, while HfSiO films are amorphous. Thin ALD-grown HfO₂ films are amorphous, while thick films are monoclinic, with traces of orthorhombic or tetragonal phase present. The sub-bandgap absorption is observed in polycrystalline, but not in amorphous, films. We note that sub-bandgap states may be the underlying cause for gate leakage via Frenkel-Poole hopping. The addition of Si to HfO₂ reduces the tendency for crystallization, mitigating such issues. However, such sub-bandgap states likely will not be a limiting factor in high- κ based CMOS technologies, since they line up close to the band edge and are

“The success of this project’s methodologies and its ability to provide standards for the entire U.S. industry is attested to by the fact that the same standards are now being adopted internationally and are being used in the qualification of offshore foundries.”

NRC Panel Report, An Assessment of the National Institute of Standards and Technology Measurement and Standards Laboratories: Fiscal Year 2003

therefore not accessible at the low gate voltages employed.

■ *Optimization of Scanning Kelvin Probe Microscopy for determining metal work function.* A series of modifications and optimizations were performed with the SKPM methodology to improve the determination of metal work functions for a variety of different metal samples prepared at NIST. The work function of the PtIr5 probe tip was corrected (4.9 eV) from contact potential measurements performed on specially prepared samples. The initial assumption for the work function of n+-Si was recalculated based on the actual Scanning Kelvin Probe Microscope tip resistivity. Finally, the cleaning of the metal samples was optimized using acetone, methanol, HF, and DI H₂O. The extracted metal work functions for a variety of metals were compared to literature values obtained from different contact potential difference techniques. The agreement is very good.

■ *Characterization of the High-κ/Metal Gate Barrier Height Using Internal Photoemission (IPE)* Metal gates have been intensively searched in the past few years to replace the traditional polysilicon for the next generation of MOSFET devices. One of the most important parameters used to select an appropriate metal is the barrier height (Φ_0) at the metal gate and the gate dielectric. Two important ternary metals, TaSiN and TaCN on either SiO₂ or HfO₂, were studied. Using internal photoemission, we were able to determine the barrier heights between these metals and dielectrics. As a result, $\Phi_0 = 3.36$ eV and 3.55 eV for TaSiN/SiO₂ and TaCN/SiO₂ interfaces, respectively. It is observed that $\Phi_0 = 2.24$ eV and 2.47 eV for TaSiN/HfO₂ and TaCN/HfO₂ interfaces, respectively. It is also observed that the difference in the barrier heights of both metals is about 0.2 eV on either of the dielectrics. This indicates that no Fermi pinning is evident at the HfO₂ interfaces.

FY OUTPUTS

COLLABORATIONS

SEMATECH, Characterization of metal gate/high-κ systems.

University of Maryland, College Park, Ultra-thin gate oxide reliability.

MSEL, Characterization of metal gate/high-κ systems.

IBM, Electrical characterization of high-κ systems.

Intel, Electrical characterization of high-κ systems.

Texas Instruments, Electrical characterization of high-κ systems.

Rutgers University, Characterization of metal gate/high-κ systems.

Yale University, Electrical characterization of high-κ systems.

Micron, Boise, ID, Characterization of metal gate dielectric systems.

ARL, Characterization of defects and reliability of SiC gate dielectric systems.

GE, Reliability characterization of SiC gate dielectric systems.

Lucent Technologies, Reliability Characterization of ultra-thin gate dielectrics.

University of Maryland, College Park, ultrathin gate oxide reliability.

U. Texas at Austin, Optical properties of ZrO₂ and HfO₂ for use as high-κ gate dielectrics.

STANDARDS COMMITTEE PARTICIPATION

JEDEC JC14.2 Committee on Wafer-Level Reliability, Dielectric Working Group, Chairman (John S. Suehle)

INVITED PRESENTATIONS

J. S. Suehle, "Reliability Challenges for Advanced Gate Dielectrics and Implications for Lifetime Projection," 2004 Microelectronics Reliability Qualification Workshop, Manhattan Beach, CA, Dec 2004.

J. S. Suehle, "Reliability Challenges for Advanced Semiconductor Devices," SEMICON West, San Francisco, CA on July 11, 2005.

E. M. Vogel, "Characterization of electrically active defects in high-κ gate dielectrics using charge pumping," *Invited*, NATO Advanced Research Workshop on Defects in Advanced High-κ Dielectrics (<http://www.ioffe.ru/natoarw/2005/index.htm>), St. Petersburg, Russia, July 11-14, 2005.

E. M. Vogel, "Electrical Characterization of MOS Devices with Advanced Gate Stacks," *Invited Tutorial*, 2005 MIGAS International School on Advanced Microelectronics, Physical and Electrical Characterization of Materials and Devices for Silicon Nanoelectronics, (www.migas.inpg.fr/), Grenoble, France, June 11-17, 2005.

E. M. Vogel, "Physical Mechanisms of Ultra-thin Silicon Dioxide Degradation and Breakdown," *Invited*, 8th International Symposium on Silicon Nitride, Silicon Dioxide Thin Insulating Films and Other Emerging Dielectrics, 207th Electrochemical Society meeting, Quebec City, Canada, May 15-20, 2005.

RECENT PUBLICATIONS

D. Heh, E. M. Vogel, J. B. Bernstein, C. D. Young, G. A. Brown, P. Y. Hung, A. Diebold, G. Bersuker, "Spatial Distributions of Trapping Centers in HfO₂/SiO₂ Gate Stacks (Accepted for Publication in Appl. Phys. Lett.)

M. T. Postek, J. J. Kopanski, D. Wollman, "Accomplishments in Nanotechnology," NIST Special Publication 1052 (01-AUG-2006)

S. Park, N. V. Nguyen, J. J. Kopanski, J. S. Suehle, E. M. Vogel, "Comparison of scanning capacitance microscopy and scanning Kelvin probe microscopy in determining two-dimensional doping profiles of Si homostructures," *Ultra Shallow Junction* 2005, Jun 05-08, 2005, Daytona Beach, Florida, Vol. 24, No. 1, pp. 404-407 (01-FEB-2006)

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- S. Sayan, N. V. Nguyen, J. R. Ehrstein, J. J. Chambers, M. R. Visokay, M. Quevedo-Lopez, L. Colombo, Yoder, I. Levin, D. Fischer, M. Paunescu, O. Celik, E. Garfunkel, "Effect of Nitrogen on Band Alignment in HfSiON Gate Dielectrics," *Appl. Phys. Lett.*, Vol. 87, pp. 212905-1-212905-3 (22-NOV-2005)
- N. V. Nguyen, M. M. Frank, A. Davydov, D. Chandler-Horowitz, "Sub-bandgap Defect States in Polycrystalline Hafnium Oxide and Their Suppression by Admixture of Silicon," *Appl. Phys. Lett.*, Vol. 87, pp. 192902-1-192903-3 (17-NOV-2005)
- S. Sayan, N. V. Nguyen, J. R. Ehrstein, T. Emge, E. Garfunkel, M. Croft, X. Zhao, D. V. Vanderbilt, I. Levin, E. P. Gusev, H. Kim, P. J. McIntyre, "Structural, Electronic, and Dielectric Properties of Ultrathin Zirconia Films on Silicon," *Appl. Phys. Lett.*, Vol. 86, pp. 152902-1-152902-3 (17-NOV-2005)
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INFRASTRUCTURE FOR INTEGRATED ELECTRONICS DESIGN & MANUFACTURING

Technical Contact:
John Messina

Staff-Years (FY 2006):
6.0 professionals
1.0 guest researcher

“I have never seen so much interest in any industry standard as there has been with the Material Declaration documents; IPC-1751 and IPC-1752 and the accompanying PDF forms.”

Dieter Bergman, IPC, Director-Technology Transfer

“Over the last decade, some individuals have quietly made a unique contribution to the electronic industry. These experts work for a part of the U.S. government and do their magic at the National Institute of Standards and Technology (NIST) in Gaithersburg, MD.”

IPC Review, “NIST, an Unsung Industry Contributor,” p14-17, June 2005

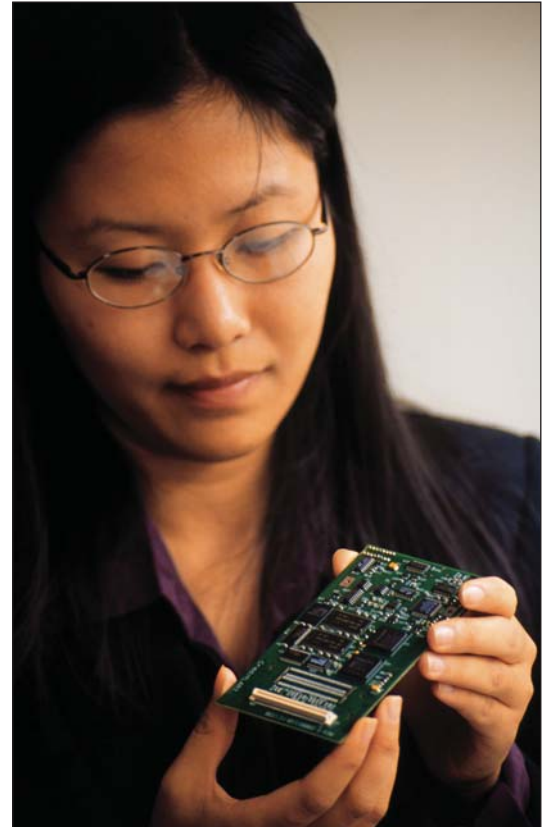
GOALS

The Infrastructure for Integrated Electronics Design & Manufacturing (IIEDM) project contributes actively to the technical development of neutral data exchange specifications in order to support distributed supply chain integration and e-manufacturing activities. The IIEDM Project aids the growth of the electronics and semiconductor industries by providing technical expertise in an impartial forum in the development of standards and assistance in resolving interoperability issues between similar, and often conflicting, standardization efforts. The neutral nature of NIST allows industry consortia, academic institutions, and standards bodies to utilize the technical expertise of the IIEDM staff to improve their data exchange standards without concerns of favoritism or bias towards one particular technology or standard. This impartiality enables the IIEDM project to work with industry to solve data exchange issues the industry must deal with as a whole. Also, the IIEDM project focuses on helping the industry deal with multiple, conflicting, and often overlapping standards. Due to the nature of the Electronics industry, with no single organization dictating standards development, companies are often faced with no clear optimal choice when choosing data exchange standards. The IIEDM staff focus on creating environments in which companies can evaluate newly emerging standards and technologies and demonstrate how differing standards can interoperate successfully.

CUSTOMER NEEDS

To maintain a globally competitive posture, semiconductor and electronics manufacturers are quickening their pace of production and innovation. Electronic products are transitioned rapidly to a commodity status, production sites are constructed and decommissioned in shorter timeframes, and manufacturers are globally outsourcing an expanding scope of production processes – and in some cases, the entire design and production of the product. To achieve the flexibility and quick turn-around they require, manufacturers rely on a distributed supply network and the ability to “mix and match” hardware and software within their own enterprise. This rapid reconfigurability needed by industry depends upon a robust IT infrastructure consisting of standards for collaboration, business process integration, and the exchange of technical

data. Industry also needs neutral test beds in which to evaluate new standards and the risks associated with technology adoption.



Ya-Shian Li holds a printed circuit board. The project brings standards development techniques and technologies to the semiconductor industry.

TECHNICAL STRATEGY

This project is working with industry to enable the infrastructure needed to support electronic commerce for both electronic components and manufacturing. The technical areas being addressed by this project are: the ability to accurately describe electronic components and their attributes, how this data is organized and packaged, and how it is accessed and used through a product’s lifecycle (from the product design, through its manufacturing, and, ultimately, to its recycling). Development of standards within this domain is crucial in order for U.S. electronics and semiconductor manufacturers to take advantage of the global marketplace. This project assists industry in the development

of standards that are critical to the infrastructure, but that no single company will pursue because of the broadbased benefit. Industry and standards groups in Japan and Europe are actively working on electronic commerce and manufacturing related projects. In working with these groups, NIST will try to minimize the overlapping standards development and ensure interoperability between U.S. and international standards.

The IIEDM Project continues to work with the electronics manufacturing industry, identifying and addressing new electronic data exchange needs. One aspect of the project's continuing work with the electronic industry is working with the National Electronics Manufacturing Initiative (NEMI) on their biennial roadmapping activity. NEMI's roadmap seeks to survey the electronics industry and identify the major development trends for the industry for the next two years. By working with NEMI on the roadmapping activity, the IIEDM Project has the ability to work with industry to identify future needs and start developing solutions to those needs early enough to be in place by the time they are needed.

One such area, in the electronics industry, is in the growing field of environmental compliance. Environmental legislation designed to protect the environment from hazardous materials is being enacted throughout the international community. These new laws and directives, such as the European Unions Restriction on Hazardous Substances (RoHS), are designed to identify potentially hazardous substances within products to minimize the negative impact the substances might have on us or our environment. In order to ensure compliance with these new regulations, the U.S. economy (starting with the electronics industry) will need to be able to identify, measure, and track these substances as they are used in the production of products throughout the entire supply chain from base materials to final products. Working with several U.S. companies and trade associations, the IIEDM Project is working to develop a complete solution to the electronics industry. This includes both new material declaration data exchange standards and basic implementations that can be used by small and medium-sized manufacturers that cannot afford to develop complex and costly in-house solutions.

DELIVERABLE: Provide technical support in the development of IPC 1752 Material Declaration standard version 2.0 to support RoHS and WEEE (waste electrical and electronic equipment) efforts.

Going beyond road mapping and standards development, the IIEDM Project works to speed the adoption and acceptance of these new standards. Two methods commonly used by the project include developing reference software implementations and software translators. The first method, reference software implementations, seeks to mitigate the risk of adopting a new standard by providing freely available software that demonstrates that the new standard works and how it can be implemented. The second method, software translators, eases the cost of migrating to the new standard by ensuring that legacy data can be exchanged back and forth with the new data formats.

DELIVERABLE: Lead the Product Lifecycle Information Management (PLIM) Technical Working Group (TWG) for the iNEMI 2006 Roadmap.

In addition to its activities within the electronics manufacturing industry, the IIEDM Project is taking its technical expertise in designing electronic data exchange specifications and applying it to the semiconductor industry. In the Printed Circuit Board (PCB) industry, the move toward outsourcing over the last several years has pushed the development of data standards that can accurately exchange product information between any two partners in a manufacturing design chain. This exchange of information can occur anywhere in the process from trading purchase order information between trading partners to exchanging design information for factory floor equipment. The semiconductor industry is now facing the same need to outsource various manufacturing and design activities that the PCB industry faced several years ago. While the actual standards needs are different for the semiconductor industry due to the differing manufacturing process and the products being developed, the design process for making the needed standards is still the same. Toward that end, the IIEDM Project is teaming up with leading industry consortiums and companies in the semiconductor industry in order to address their data exchange needs. The project's activities include becoming involved in standards development activities, developing prototype software systems to test new standards, and leading roadmapping activities to help identify future industry problems.

DELIVERABLE: Work through SEMI to complete a new specification for Time Synchronization and define the clock object.

ACCOMPLISHMENTS

- Awarded NIST's Rosa Award for outstanding contributions to the development of meaningful

"NIST provides unique capabilities that have greatly improved the definition of industry standards that are required for useful implementation of data collection software capabilities for e-Manufacturing"

International SEMATECH letter to NIST, July 8, 2004

and significant engineering, scientific, or documentary standards for the IIEDM Project's work on the IPC 1752 standard, Sept. 2006. IPC 1752 *Material Declaration Management* was done in conjunction with IPC and iNEMI to help the electronics industry comply with the European Union's Restriction of Hazardous Substances (RoHS) directive.

- Invited talk on Material Declarations at the MEP National Conference in Orlando, FL, 2006.
- Taught several classes "Implementing Electronic Material Data Exchange" for the IPC RoHS Summer School series.
- Chaired the Product Lifecycle Information Management working group for the development of the iNEMI 2006 Road mapping effort.
- Invited talk "Software Interoperability – Enabler of Emerging Technologies" at the Technology Market Research Council (TMRC) Spring Conference in Baltimore, MD, May 2005.
- Developed a software translator tool that converts Gerber board layout files to IPC 2581 (OffSpring) format and back again.
- "Next Generation Simulation-based Design Technologies for Electronics Product Realization" presented at PDE 2005 (The 7th NASA-ESA Workshop on Product Data Exchange).
- Chaired the IEC Technical Committee (TC) 93 (Design Automation) Working Groups 3 (Product Data Exchange), 5 (Conformance Testing), and 6 (Data Dictionaries).

FY OUTPUTS

COLLABORATIONS

We are currently working with ISMI, a leading semiconductor industry consortium, by providing technical expertise in the development of data exchange specifications and reference software implementations.

We are working with the IPC on the development of software tools to assist the industry in the exchange of data information ranging from material declarations to printed circuit board designs.

We are currently working with a group of organizations (RosettaNet, ECCMA, ISO, IEC, IPC, and JISSO) on a variety of electronic data exchange specifications.

EXTERNAL RECOGNITION

Eric Simmon was asked to assist MEP in the development of a material declaration package that would be used at MEP training centers to train small and medium electronic manufacturing companies how to comply with RoHS.

Ya-Shian Li was asked to give a keynote speech on Time Synchronization at the Network Performance Workshop at the University of Michigan in April 2006.

John Messina was appointed IEC TC 93 US TAG Technical Advisor (TA) by ANSI.

Journal article "NIST, an Unsung Industry Contributor" in the June 2005 issue of IPC Review magazine.

RECENT PUBLICATIONS

M. Aronoff, "Focus 3D Telemodeling Tool: GUI Design for Iteration 1," NISTIR 32470 (28-SEP-2006)

M. Bajaj, R. Peak, D. Zwemer, T. Thurman, L. Klein, G. Liutkus, K. G. Brady, J. V. Messina, M. Dickerson, "Automating Thermo-Mechanical Warpage Estimation of PCBs/PCAs Using a Design-Analysis Integration Framework," Proceedings of the Mentor Graphics International User2User Conference, 2006 Mentor Graphics International User2User, May 02-05, 2006, San Jose, California, (18-AUG-2006)

H. Wohlwend, Y. Li, "New Industry Requirements for Clock Synchronization and Time Stamping," European AEC/APC Symposium, Mar 27-31, 2006, Aix En Provence, France, (27-MAR-2006)

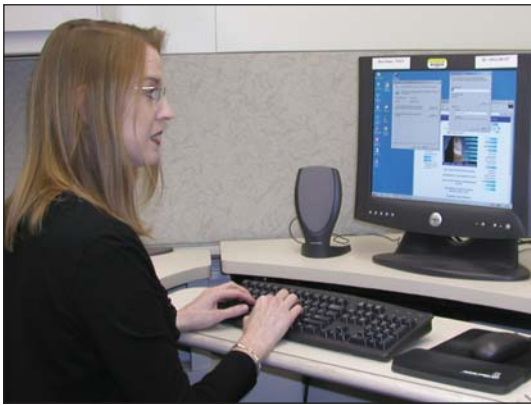
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M. Bajaj, D. Zwemer, R. Peak, M. Dickerson, T. Thurman, K. G. Brady, J. V. Messina, "Next Generation Simulation-based Design Technologies for Electronics Product Realization," The 7th NASA-ESA Workshop on Product Data Exchange (PDE), Mar 19, 2005 to Apr 22, 2005, Atlanta, Georgia, (01-MAY-2005)

KNOWLEDGE FACILITATION

GOALS

- To eliminate paper-intensive and manual operations by automating tasks, decreasing the administrative requirements of the technical and support staff, increasing responsiveness to customers, and implementing a secure eNIST paperless environment.
- To provide Information Technology security policies, procedures, guidelines, and baselines and ensure compliance with Federal Information Security Management Act (FISMA) requirements.



Jennifer Kostick configures a machine to use the Lan-desk centralized support software in order to increase security and centralize PC support.

CUSTOMER NEEDS

Scientists need time to work on their research, testing, calibrations, etc. However, managers need project plans, statuses, and similar information, and customers should have access to information in a timely manner. To best enable all of these functions, we have developed several web-based applications to minimize the time and efforts of technical staff and project leaders, while providing customers with up-to-date information.

As more and more of our data is stored electronically, it is natural to progress towards sharing the information, maximizing the benefits while minimizing the number of times it has to be entered.

As we grow to rely on the data in our computers, and that data is shared more frequently, the need for security of that data also grows. Our customers depend upon the confidentiality, integrity, and availability of the information. Confidentiality refers to allowing access to our data only to the people who should have it. Integrity refers to ensuring the

data is what it should be and no one has tampered with it. And, availability refers to making sure the data is there when it is needed.

The Federal Government has established FISMA Guidelines that allow agencies to provide more secure information systems within the Federal Government including the critical infrastructure of the United States. These guidelines provide a framework for us to develop and implement policies and procedures, implement training and awareness programs, and secure our assets.

TECHNICAL STRATEGY

A web-based application has been created to store and track all of the Electronics and Electrical Engineering Laboratory's publications and reports provided to management. Management is able to obtain access to the information they need easily, and the administrative burden on the technical staff has been alleviated. Generation of required paperwork has been automated, removing that responsibility from the support staff. The applications also serve as a warehouse for all publications and reports.

We developed the Information System to Support Calibrations (ISSC), which is a structured-query language database-driven application. The ISSC stores all of the administrative, technical, and financial data involved with items calibrated at NIST. The system has over 250 NIST users and provides status information to over 1400 calibration customers. The web-based system allows access from an unlimited number of different machines and operating systems used by personnel at NIST. The ISSC has reduced the time to complete the required paperwork by automating the entire workflow process. The ISSC was migrated to Technology Services for maintenance in 2003. We are collaborating with Canada's National Research Council (NRC) Institute for National Measurement Standards (INMS) to assist them in the development of an application similar to the ISSC.

A project reporting system, also developed as a web application, has been created to reduce the duplication of the storage of information while providing management with immediate access to project data without interrupting project staff. This application contains all project-related information such as funding, milestones, staff, etc. Access to the application is controlled by a role-based access

Technical Contact:
Jennifer A. Kostick

Staff-Years (FY 2006):
2.25 professionals
2 guest researchers

control—what you have access to is contingent upon who you are.

A web-based information system is being developed to support the clean rooms. Scientists will use the system to reserve equipment in the clean rooms. The system will automatically keep track of the time that equipment is used. Access will be limited to staff with proper training. This is being developed in collaboration with Stanford University.

A web-based information system was created to log and track all paper documents through the administrative process. Status of required paperwork can be easily determined.

A web-based information system was developed for use by NIST's Conference Facilities personnel to automate all the processes of conferences from registration to billing.

To ensure the security of our systems, we have developed and implemented IT Security policies and procedures and a training and awareness program. We have met all FISMA requirements, such as developing detailed security plans, risk assessments, self assessments, security tests and evaluations, rules of behavior, business impact analysis, contingency plans, plans of actions and milestones, asset inventories, and architecture and network diagrams for all of the systems within EEEL.

ACCOMPLISHMENTS

- Implemented Information System to Support Calibrations (ISSC) NIST-wide.
- Transitioned ISSC to Technology Services.
- Met annual FISMA requirements.
- Developed Bibliography Information System.
- Developed NIST Conference Registration System.
- Created Electronic Logbook.
- Created Document Information System.

FY OUTPUTS

COLLABORATIONS

Kevin Brady is collaborating with Stanford University in the creation of the Clean Room Information System.

Jennifer Kostick is collaborating with other IT Security Officers within the Federal Government to develop consistent policy, procedures, guidance, and best practices.

MAJOR FACILITIES / LABORATORIES

NIST NANOFAB FACILITY

The Nanofab, part of NIST's Center for Nanoscale Science and Technology, provides state-of-the-art facilities for the fabrication of nanoscale devices, structures, standard reference materials, MEMs, and bio-devices. It also provides access to a wide variety of measurement and characterization tools, technologies, and expertise to NIST and its partners.

MATERIALS CHARACTERIZATION LABS

High-Resolution Optical:

Spectroscopic Ellipsometry, High-Resolution Fourier Transform Infrared Spectroscopy, Photoluminescence, Raman Scattering, Photorefectance, and other Modulation Spectroscopies

Electrical:

Resistivity, Spreading Resistance, Lifetime, Hall Effect, Charge-Pumping Measurements, Capacitance-Voltage (high frequency & quasi-static), Surface Photovoltage, AC Impedance Analysis, Low-Temperature I-V, and Scanning Capacitance/Atomic Force Microscopy

DEVICE AND TEST STRUCTURE CHARACTERIZATION LABS

Electrical and Thermal Package Evaluation
Power Device Model Extraction and Validation
Packaging, Assembly, and Bonding Evaluation
Package Interconnect
Scanning-Probe Microscope
Automatic Wafer-Level Measurement
Gate Dielectric Integrity
MEMS Electrical, Mechanical, Optical, and Microwave
Photocurrent Spectroscopy/Time of Flight (ToF) Measurements

COMPUTER-AIDED DESIGN LABS

Test Structure Layout and Design
Integrated Circuit Layout, Design, and Simulation
Finite Element Thermal Analysis Tools and Computational Fluid Simulations
System, Device, Process, Interconnect, and Virtual Fabrications Simulations

NATIONAL RESEARCH COUNCIL (NRC) POST-DOCTORAL OPPORTUNITIES

The Semiconductor Electronics Division at the National Institute of Standards and Technology (NIST), in cooperation with the National Research Center (NRC), offers awards for post-doctoral research for American citizens in the fields described below. The Division conducts research in semiconductor materials, processing, devices, and integrated circuits to provide, through both experimental and theoretical work, the necessary basis for understanding measurement-related requirements in semiconductor technology.

NIST affords great freedom and an opportunity for both interdisciplinary research and research in well-defined disciplines. These technical activities of NIST are conducted in its laboratories, which are based in Gaithersburg, a large complex in a Maryland suburb of metropolitan Washington, DC. Applications for NIST Research Associateships are evaluated by the panels during February and August. Application deadlines are Feb. 1 and Aug. 1 of each year.

DNA TRANSPORT IN SINGLE NANOPORES

We are studying the mechanism by which DNA partitions into and threads through single nanometer-scale pores. This experimental and theoretical effort focuses on understanding how genetic information is exchanged between organisms (*e.g.*, between virus and host cells or between bacteria) and on adapting single nanopores for novel biological and biotechnological applications. It was recently shown that the interaction between polymers and a single nanopore provides the physical basis of a multi-analyte sensor. Work is also underway to determine whether this system could be used as a tool to rapidly sequence long strands of DNA and RNA.

Contact: John Kasianowicz, 301-975-5853

ELECTRICAL AND OPTICAL CHARACTERIZATION OF SEMICONDUCTORS AND DEVICES

Research focuses on understanding the electronic, optical, and magneto-optical behavior of semiconductor materials and devices. Areas of interest include the role of impurities and native defects in bulk crystals, and novel and useful properties induced by quantum confinement in reduced dimensional structures (heterostructures, quantum wells, superlattices, and quantum wires and dots). A broad range of optical techniques is available for reflection, transmission and absorption, and modulation spectroscopy; photoluminescence and photoluminescence excitation; Raman and resonant-Raman scattering; spectroscopic ellipsometry, and surface photovoltage. A wide variety of

electrical and magnetotransport techniques is also utilized to characterize the electronic properties. Emphasis is placed on understanding fundamentals and technologically relevant properties as well as developing accurate measurement techniques.

Contact: David Seiler, 301-975-2054

ELECTRICAL OVERLAY- AND CD-METROLOGY DEVELOPMENT FOR CHARACTERIZATION OF ADVANCED LITHOGRAPHY INSTRUMENTS FOR INTERCONNECT APPLICATIONS

Projected critical dimension (CD) and overlay control-tolerances for new generations of ICs are reducing metrology uncertainty tolerance down to the several-nanometer region. However, the development of CD and overlay metrology standards are not keeping pace with lithographic resolution capabilities of advanced imaging systems. The Enabling Devices and ICs Group seeks individuals interested in conducting further research in: (1) the design and optimization of reference materials for scatterometry metrology; (2) noncontact electrical CD-measurement and extraction methodologies; and (3) design, fabrication, and certification of CD standards in the range 20 nm to 100 nm. We also encourage applicants with research experience in noncontact/nonintrusive electrical CD extraction and multimode overlay-sensor development for novel CD reference-material implementations. The project is also initiating a study of unique materials and metrology issues associated with copper interconnect for ultra-high speed IC applications.

Contact: Michael Cresswell, 301-975-2072

FUNCTIONALIZING SEMICONDUCTOR SURFACES

Combining organic monolayers with semiconductor surfaces is of interest for many differing applications including molecular electronics, sensors, and bio-electronics. Monolayers on semiconductor surfaces take advantage of the increased electrical functionality, chemical and structural robustness, wealth of fabrication knowledge, and present a less disruptive technology compared with monolayers on typically used metal substrates. We are investigating various experimental approaches to form organic monolayers on semiconductor surfaces. The resulting films are characterized by using Fourier-transform infrared spectroscopy, spectroscopic ellipsometry, contact angle measurements, and atomic force microscopy. Key aspects of this work involve examination and optimization of alternative functionalization pathways for monolayer formation and thorough characterization of the resulting monolayer. More advanced applications include formation of biorepellent monolayers in addition to monolayers specifically tailored to bind differing biological moieties.

Contact: Christina Hacker, 301-975-2233

MICROELECTROMECHANICAL SYSTEMS

The MicroElectroMechanical Systems (MEMS) project focuses on the development of new MEMS-based sensors and actuators for measurement applications. It functions in a multidisciplinary environment with collaborations in the NIST laboratories in Chemistry, Materials Science, Physics, Biotechnology, and Building and Fire Research. Current activities in the project include thermal-based elements, mechanically resonant structures, microwave elements, and microfluidic systems. The project is also developing MEMS test structures, test methods, and standards to characterize device properties for device performance and reliability testing. These MEMS-based test structures are being utilized to characterize thin-film properties in mainline semiconductor fabrication processes. We are interested in postdoctoral applications not only from individuals who have specialized in MEMS research but also from individuals of other science disciplines who wish to learn microfabrication methods and apply their expertise for new measurement applications.

Contact: Michael Gaitan, 301-975-2070

MODELING ADVANCED SEMICONDUCTOR DEVICES FOR CIRCUIT SIMULATION

Accurate circuit simulator models for advanced semiconductor devices are required for effective computer-aided design of electronic circuits and systems. However, the semiconductor device models provided in most commercial circuit simulators (*e.g.*, simulation program with integrated circuit emphasis) are based on microelectronic devices, and they do not adequately describe the dynamic behavior of advanced semiconductor devices. Therefore, research focuses on the following: (1) physics-based models-for advanced semiconductor devices such as power and compound semiconductor devices; these models are implemented into available circuit and system simulation programs; (2) parameter extraction algorithms-for obtaining model parameters from terminal electrical measurements; and (3) characterization procedures-for verifying the models' ability to simulate the behavior of the devices within application circuits. NIST also works closely with commercial software vendors to make the new models available to circuit design engineers, and has established the NIST/IEEE Working Group on Model Validation to develop comprehensive procedures for evaluating the performance of circuit simulator models.

Contact: Allen Hefner, Jr., 301-975-2071

MOLECULAR ELECTRONICS: ELECTRICAL METROLOGY

In Molecular Electronics-a field that is predicted to have important technological impacts on the computational and communication systems of the future-molecules perform the functions of electronic components. We are developing methods to reliably and reproducibly measure the electrical properties of small ensembles of molecules in order to investigate molecular conduction mechanisms. Specifically, we are developing test-structures based on nanofabrication and MicroElectroMechanical Systems processing techniques for assessing the electrical properties and reliability of molecular molecules. In addition to the complexity of the nanofabrication of test structures, the challenges associated with measuring the electrical properties (such as current-voltage and capacitance-voltage as functions of temperature and applied fields) of these small molecular ensembles are daunting. The measured electrical properties will be correlated with systematic characterization studies

by a variety of probes and the results used in the validation of predictive models. This task is part of a cross-disciplinary, interlaboratory effort at NIST whose overall role is to develop the measurement science that will enable molecular electronics to blossom into a viable industry.

Contacts: Curt Richter, 301-975-2082, Christina Hacker, 301-975-2233, or John Suehle, 301-975-2247

NANOBIO TECHNOLOGY FOR SINGLE CELL AND SINGLE MOLECULE MANIPULATION AND MEASUREMENT

Our work focuses on developing microfluidic systems and nanofluidic restrictions for cell and biomolecule transport and detection. We are interested in methods to pattern cells on surfaces, cell adhesion, sorting, and electronic and electrochemical monitoring of cell activity. We are also interested in nanofluidic systems for DNA, RNA, and protein transport and detection to determine the structure and function. This project is part of a multidisciplinary program with collaborations in the NIST laboratories in Chemistry, Materials Science, Physics, and Biotechnology. Research would focus on the development of new fabrication methodologies, design and fabrication of new and novel nanofluidic systems, and measurement methods.

Contact: Michael Gaitan, 301-975-2070

NOVEL TEST STRUCTURES FOR CHARACTERIZING THE PERFORMANCE OF ADVANCED MULTILEVEL INTERCONNECTION SYSTEMS

As the complexity of advanced integrated circuits continues to increase, new materials (copper, low- κ dielectrics) need to be systematically characterized in order to perform parameter extraction for modeling on-chip interconnect systems at clock frequencies. The Enabling Devices ICs Group seeks individuals interested in developing new test structures, measurement methods, and analysis models needed to evaluate copper based, multilevel interconnection systems for high-frequency environments. Of particular importance are new methods for dimensional metrology, interfacial contact resistance, stress effects, median-time-to-failure, and high-frequency performance. In particular, we are interested in applying electrical parameters such as resistance and capacitance per unit length that are extracted by rf probing of stripline test struc-

tures to the extraction of dimensional parameters such as CD and overlay.

Contact: Michael Cresswell, 301-975-2072

OPTICAL AND PHYSICAL CHARACTERIZATION OF THIN FILMS USED IN INTEGRATED-CIRCUIT DEVICES

The continued scaling of integrated-circuit (IC) technology requires more stringent precision and accuracy for the optical and physical measurements of thin films. Our research involves the development of optical measurement techniques, specifically spectroscopic ellipsometry, and internal photoemission and the enhancement of data analyses and modeling. Input from various physical, optical, and electrical techniques are needed to improve our knowledge of the electronic and optical properties of these thin films and their interfaces. With a broad collaboration from various thin-film measurement groups within NIST, our research will focus on relating the analyses of HR-TEM, scanning probe methods, x-ray reflectance, Fourier-transform infrared, photo reflectance, Raman scattering, and various electrical techniques to improve our understanding of these films and also validate some of the optical models used in the analysis of the ellipsometric data. Simple actual IC devices can be fabricated in-house for electrical test structures.

Contacts: Curt Richter, 301-975-2082, or Nhan Nguyen, 301-975-2044

ORGANIC ELECTRONIC TEST PLATFORMS

The NanoElectronic Device Metrology Project at NIST is addressing critical metrology issues associated with OFETs, one of the critical building blocks for the emerging technology of organic electronics. The NEDM is developing OFET test structures and test methodologies to extract the fundamental electrical properties of organic semiconductors. This task is part of a large interdisciplinary team of physicists, chemists, engineers, and material scientists at NIST whose goal is to develop an integrated measurement platform to predict the performance of organic electronic devices based on composition, structure, and materials properties. The approach is to correlate the results of unique, world-class characterization techniques such as NEXAFS and cold-neutron scattering with the electrical behavior of OFET structures to determine

the relationship between device performance and the structure, properties, and chemistry of critical materials and interfaces.

Contacts: David Gundlach, 301-975-2048, or Curt Richter, 301-975-2082

ORGANIC ELECTRONICS

We are interested in organic-based electronic devices for use in large-area low-cost electronic applications, such as displays, radio frequency identification (RFID), and sensor arrays. Thin films of organic semiconductors, insulators, and conductors are used to fabricate integrated devices and circuitry, and it is expected that printing and inexpensive roll-to-roll processing will be developed to manufacture low-cost electronics on large-area flexible plastic substrates. The organic thin-film transistor (OTFT) is a core device since most electronic applications require active switches or circuitry. Although research on the OTFT has spanned nearly 20 years, we still lack a physically accurate, concise microscopic understanding of its electrical operation.

Developing predictive and physically-accurate models and theories is critical to establishing organic electronics as a mature and manufacturable technology. Core challenges hindering further development include: (1) a poor understanding of the electronic structure at critical device interfaces; (2) a lack of detailed knowledge about defect generation, device reliability, and device lifetime; and (3) the extended use of inappropriate device structures, test methodologies, or models for extracting device parameters from measured electrical characteristics. The goal of this project is to solve these challenges by developing the appropriate electrical/optoelectrical characterization methods, test structures, and test methodology to quantitatively extract device properties and parameters, and to develop the microscopic models needed to describe the device operation and reliability.

Contact: David Gundlach, 301-975-2048

PHYSICAL AND ELECTRICAL PROPERTIES OF ADVANCED GATE DIELECTRIC FILMS

It is increasingly difficult to characterize ultrathin gate dielectric films (typically 0.1 nm to 3.0 nm) used in metal-oxide-semiconductor (MOS) devices as technology drives them ever thinner. We are developing electrical test methods (using conventional techniques such as I-V and C-V, as well as

low-temperature magnetotransport techniques) to measure the physical properties (*e.g.*, film thickness and permittivity) of alternate gate dielectric materials such as high- κ metal oxides as well as ultrathin SiO₂. Electrical results are compared with those of optical and other measurement methods, and fundamental physical models are developed to be effective for more than one measurement technique. Because the interface between the dielectric film and the silicon substrate is critical to understanding these measurements, we are developing techniques to characterize buried interfaces (*i.e.*, interface roughness) and are determining how the interface and physical properties affect device performance and reliability.

Contact: John Suehle, 301-975-2247

PHYSICS OF SEMICONDUCTOR DEVICES AND C AND BN NANOTUBES

Theoretical solid-state physics research for nanoelectronic applications is in progress in order to understand the operation of advanced electronic and molecular electronic devices and to provide more physically correct and numerically robust carrier transport models. Such transport models are used to interpret measurements and to enable predictive computer simulations of nanoelectronic devices. For example, topics include densities of states, band structures, high-concentration effects, carrier lifetimes, and carrier mobilities. The approach involves careful experimental verification of the device models for elemental and compound semiconductors; for metallic, semiconducting, and insulating nanotubes; and for molecular electronics. We are interested in extending our theoretical research to include magnetic semiconductors (spintronics) such as manganese-doped GaAs, nanotubes, ultrathin nanolayers, and confined electrons and photons in semiconductor nanostructures.

Contact: Herbert Bennett, 301-975-2079

RELIABILITY OF INTEGRATED CIRCUIT DIELECTRIC FILMS

Aggressive scaling of gate oxide thickness used in silicon integrated circuits necessitates the understanding of physical mechanisms responsible for dielectric degradation and breakdown. We are particularly concerned with the reliability of ultrathin gate oxides that are in the direct tunneling regime during circuit operation. Research focuses on: (1) identifying parameters to determine the physics of time-dependent dielectric breakdown of ultrathin dielectric films in the tunneling regime,

(2) determining the effectiveness of highly accelerated stress tests to predict long-term reliability of thin dielectric films, (3) relating analytical characterization of oxide bulk and interfaces to electrical behavior, (4) identifying and controlling fabrication process parameters that affect intrinsic and extrinsic failure modes, and (5) characterizing and evaluating alternate dielectrics for use as substitutes for silicon oxide in advanced circuit technologies.

Contact: John Suehle, 301-975-2247

SCANNING PROBE METROLOGY

We are developing scanning probe microscopes to characterize and manipulate the physical and electrical properties of electronic devices, semiconductors, and related materials at the nanometer resolution scale. Projects are aimed at impacting silicon technology 5 to 10 years in the future or at characterization problems unique to compound semiconductors, molecular electronic devices, or quantum devices. We recently developed scanning capacitance microscopy as a tool for measuring the two-dimensional dopant profile across a silicon p-n junction. We are particularly interested in projects to develop techniques to measure material properties in three dimensions and that have spatial resolution below 1-nm. Our interests extend to other scanning probe techniques, including variable temperature scanning tunneling microscopy in UHV, surface photo-voltage microscopy, and other optically pumped probes.

Contact: Joseph Kopanski, 301-975-2089

SILICON BUILDING BLOCKS FOR BEYOND-CMOS CIRCUITS

The complementary-metal-oxide-semiconductor (CMOS) field-effect-transistor is showing fundamental limits associated with the laws of quantum mechanics and the limitations of fabrication techniques. This is driving research on innovative solutions to augment or replace CMOS technologies. Our goal is to develop the metrology that will enable emerging information processing technologies to extend electronic device performance improvements beyond the incremental scaling of CMOS. Quantum devices compatible with Si technologies such as silicon nanowires (Si-NW), resonant tunneling devices, and single-electron transistors, deliberately exploit quantum and size effects. We are developing the electrical and physical metrology of the basic building blocks of these confined-silicon devices (*e.g.*, quantum layers, wires, and quantum

dots). Much of our focus has been on the fabrication of Si-NW FET devices. We are making and characterizing “top-down” fabricated Si-NW FETs based on pushing the fabrication limits of silicon-on-insulator (SOI) technology as well as Si-NWs grown using CVD then positioned and contacted to form “bottom-up” test structures and devices. Our interests include, but are not limited to, fabrication, simulation, and characterization of device structures and constituent materials/processes. Our primary expectation is to be able to identify and address critical metrology issues for this emerging technology of silicon-based quantum devices.

Contact: Curt Richter, 301-975-2082

SED INSTRUMENTAL IN NEW MATERIAL DATA EXCHANGE STANDARDS

Semiconductor Electronics Division Researchers, led by Art Griesser and Eric Simmon of the Electronic Information Group, provided critical leadership in the development of two new Material Data Exchange Standards. These standards were critical to enable the U.S. Electronics Industry to comply with the "Restriction of Hazardous Substances (RoHS) Directive," which would have potentially limited future electronics exports to Europe. For example, iNEMI in a March 2006 press release stated that second published standard (IPC-1752) "is a cornerstone in the overall industry strategy for standardization of materials content declarations across the supply chain. This standard integrates and leverages several industry efforts, establishing a common solution that is shaped not only by regulatory guidelines but also by industry needs and requirements."



The Electronics Information group is working on standards for the manufacture of Semiconductor Electronics and Printed Circuit boards that are environmentally friendly. New environmental legislation requires reporting for the manufacture and proper disposal of all electronic sub-assemblies. Standards help make this possible up and down the industry supply chain.

The RoHS Directive regulates material content used in electronics. This legislation, which was enacted by the European Union (EU) and designed to help protect the environment, went into effect on July 1, 2006. It restricts the use of six substances within electronics products sold anywhere within the EU and affects billions of dollars worth

of electronic goods. In order to help companies implement systems to capture, archive, and transfer the substance data that is necessary to comply with the directive, material data exchange standards were needed.

To assist industry in complying with the RoHS directive, NIST has been working with IPC-Association Connecting Electronics Industries® and the International Electronics Manufacturing Initiative (iNEMI) to develop a data exchange standard to help companies capture and exchange the material composition data between stakeholders in the supply chain. The collaboration has resulted in two new IPC data exchange standards: IPC-1751, *Generic Requirements for Declaration Process Management* and IPC-1752, *Materials Declaration Management*.

The final set of standards will include NIST's contributions which include a UML design model defining the data types and relationships, an XML implementation of this model, and two (software enabled) PDF forms which act as both a container for the data and a simple data entry tool for small and medium businesses.

"This will probably be the fastest that IPC has built and published a standard, but we had a running start," Abrams observed, acknowledging the work that was done earlier by groups such as Jedec and iNEMI, as well as the help it has received from the National Institute of Standards and Technology and Adobe Systems Inc."

Fern Abrams, IPC, Director - Environmental Policy, Electronic News Network, EDN Article, <http://www.edn.com/article/CA6301761.html?text=1752>

"I have never seen so much interest in any industry standard as there has been with the Material Declaration documents; IPC-1751 and IPC-1752 and the accompanying PDF forms."

Dieter Bergman, IPC, Director - Technology Transfer

DIVISION LEADS ASSESSMENT OF MEASUREMENT NEEDS OF THE SEMICONDUCTOR INDUSTRY

WILL ITS FUTURE MEASUREMENT NEEDS FOR INNOVATION BE MET?

“The economic value of Moore’s Law is that it has been a powerful deflationary force in the world’s macro-economy. Inflation is a measure of price changes without any qualitative change—so if price per function is declining, it is deflationary.”

Semiconductor Industry Association 2005 Annual Report, page 12

“The semiconductor industry is important not just for the direct contribution in jobs, exports, and efficiencies created but also because semiconductors have become the seminal technology, the vital core of an entire ecosystem that drives innovation and growth in all sectors of our economy.”

Semiconductor Industry Association 2006 Annual Report, page 8

As the U.S. national measurement institute, NIST assists all stakeholders in selected fields with their measurement and standards needs. NIST recently accepted the challenge to see whether the U.S. measurement system (USMS) is meeting the nation’s measurement needs. The semiconductor industry was one of the areas considered in terms of its measurement needs for accelerating technological innovation.

Dr. Herbert S. Bennett, NIST Fellow, led the assessment of the ability of the nation’s measurement system to meet future metrology needs of the semiconductor industry. Searching for an acceptable metric for assessing the health of metrology for the semiconductor industry, he collaborated with industry leaders to identify a limited set of unmet measurement needs that are barriers to technological innovation. Assuming that this set of needs may serve as a proxy for the galaxy of semiconductor measurement needs, he examined it from the perspective of what will be required to continue the semiconductor industry’s powerful impact in the world’s macro-economy and to maintain its exceptional record of technological innovation.

The successes of the semiconductor industry has led to major impacts on many other industries, such as those that support computers, networks, information technologies, entertainment, healthcare, and defense. Advances powered by semiconductors give businesses and consumers new flexibility, freedom, and opportunity. The semiconductor industry contributes substantially to overall global economic health.

Ways to strengthen the measurement system for the semiconductor industry include:

- Forming International collaborations, consortia, and partnerships to strengthen the measurement system: No one region, country, or company has the R&D resources to provide the solutions on its own.
- Meeting the measurement needs requires improved fundamental understanding of chemistry, materials, and condensed matter physics over several lengths of scale from microscopic to atomic dimensions. As devices shrink in size to

nanometers, performing measurements on them becomes more costly and time-consuming. This means that computer simulations are now very critical for advances in semiconductors and other nano-technologies:

- decreasing the time to perform measurements, especially those used in manufacturing, and
- shortening the time to develop new measurement technologies and to deploy new measurement instrumentation.

This analysis of the measurement needs of the semiconductor industry was in terms of the following attributes that are indicated in italics:

- Measurement Barriers – 79 % of the needs cite accuracy as a barrier; 43 % of the needs arose from a *Lack of Fundamental Knowledge*; and 64 % arose from the requirement that the *Speed for Making Measurements* must be increased.
- Solution Providers – All of the needs cited that *Industry Consortium and Partnerships* would be needed to provide solutions whereas 71 % and 21 % cited respectively that Government and Universities would be needed.
- Measurement Solutions – The measurement part of the solution for 86 % of the needs involve *Development of Measurement Technology*; 50 % involve *Research for Measurement Science*; and 64 % involve *Measurement Instrumentation*.
- Stage of Technological Innovation – The stage for the technological innovation for all of the needs is *Applied Research*.
- NIST’s Role as One of the Measurement Solution Providers – In 57 % of the measurement needs, NIST’s role would be the *Development of Measurement Technology*; in 28 % of the needs, it would be *Third party Verification*; and in 7 % of the needs, it would be establishment of *Standards*.

RESEARCHERS TEACH NANO-ELECTRONICS AND RELIABILITY THROUGH TUTORIALS

John Suehle and Curt Richter, both of the Semiconductor Electronics Division's CMOS and Novel Devices Group, have recently and independently presented separate tutorials to share their expertise in their perspective fields with industry.

Dr. John Suehle, Leader of the Advanced MOS Device Reliability Characterization Project and Acting Director of the CMOS and Novel Devices Group, presented a short course entitled "Reliability Challenges for Advanced Semiconductor Devices" during the annual SEMICON West tradeshow in San Francisco, CA, in July 2005 and again in 2006. The SEMICON West tradeshow is the largest exposition in North America devoted to semiconductor and related microelectronics manufacturing. Dr. Suehle's short course was sponsored by Semiconductor International and Semitracks Inc. During the full day course, Dr. Suehle covered reliability issues relating to front end dielectrics, including time-dependent dielectric breakdown, negative bias temperature instability, and high- κ dielectrics. Dr. Suehle co-instructed the course with Dr. Ennis Ogawa from Texas Instruments, who discussed reliability issues associated with advanced metallizations.

Among the course attendees were representatives from test equipment manufactures, semiconductor manufacturers, and fabless companies. The course was well received with requests for the course to be taught again in the United States and other countries.



John Suehle outside of his 2005 reliability short course at SEMICON West, San Francisco, CA.



Curt Richter, shown loading a molecular electronics sample for electrical characterization, collaborated with HP to present a tutorial on molecular electronics.

Dr. Curt Richter, Leader of the Nanoelectronic Device Metrology Project, collaborated with Duncan Stewart of Hewlett-Packard (HP) Research Labs to present a joint tutorial on molecular electronics at the 2005 IEEE International Reliability Physics Symposium (IRPS). Approximately 100 people attended the tutorial. Molecular electronics (ME) – which has been defined as “electronics whose behavior is dictated by the chemical, physical, and electronic structure of molecules” and has features on the 1 nm to 3 nm size scale – is emerging as a technology that may enable a future generation of much smaller, more densely integrated devices which will be more powerful, sophisticated, and portable than today's. In the concept of molecular electronics, molecules are used to implement the functionality of electrical devices (such as transistors or memory cells) that are currently made from semiconductor devices.

For more than 40 years, the IRPS has been the premier meeting for engineers in the area of electronic component reliability. The IRPS promotes the comprehension of reliability and performance of integrated circuits and microelectronic assemblies and provides the latest developments in the reliability and performance of circuits and devices to the microelectronics industry. The tutorial sessions are a major component of this leading symposium and cover a broad range of both introductory and advanced topics. IRPS continues to explore the cutting edge of the state of the art in the microelectronics industry through contributed papers and tutorials such as “Molecular Electronics” in the Beyond CMOS session.

“John presented an in-depth analysis that was theoretical and informative.”

“John presented a wealth of information and references that I will be digging into for weeks!”

Attendees at Dr. John Suehle's reliability short course, held at SEMICON West, San Francisco, CA.

SED LEADS MAJOR NANOELECTRONICS METROLOGY CONFERENCE IN 2007

“If you want to meet, greet, and learn from the world’s experts in metrology, this is the place to be.”

Dan Hutcheson,
VLSI Research, “Essential Events,” *The Chip Insider*,
October 27, 2006.

“[The Conference] was extremely successful, assembling more than 250 attendees from industry, government and university backgrounds representing the United States and more than 10 other countries.”

Alexander Braun, Senior Editor, “The Metrology Corner,” *Semiconductor International Magazine*, May 1, 2005.

The 2007 International Conference on Frontiers of Characterization and Metrology for Nanoelectronics (formerly titled *Characterization and Metrology for ULSI Technology*) will be held in March 27-29, 2007, at the National Institute of Standards and Technology (NIST), Gaithersburg, Maryland. This conference, the sixth in the series, represents a paradigm shift from the previous conferences in that emphasis is on frontiers and innovation in characterization and metrology. This and all previous conferences in the series were coordinated under the leadership of the Semiconductor Electronics Division, NIST. Additional sponsors for the 2007 event include Semiconductor Manufacturing Technology (SEMATECH), Semiconductor Equipment and Materials International (SEMI), the Semiconductor Research Corporation (SRC), Semiconductor International, and the National Science Foundation (NSF).

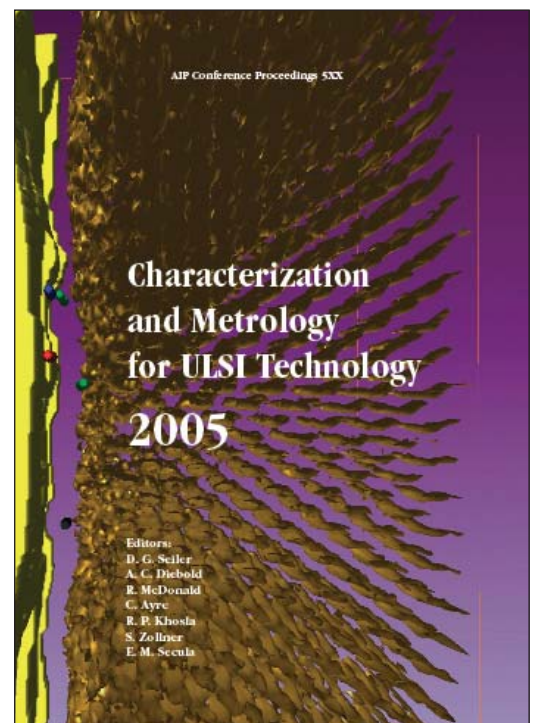
The goal of the conference is to bring together scientists and engineers interested in all aspects of the technology and characterization techniques for nanoelectronic materials and device research, development, manufacturing, and diagnostics. All approaches are welcome: chemical and physical, electrical, optical, in-situ, and real-time control and monitoring. The conference is dedicated to summarizing major issues and giving critical reviews of important semiconductor techniques that are needed by the semiconductor industry as we move to silicon nanoelectronics and beyond.

The 2007 Conference will consist of formal invited presentation sessions by high-level industry leaders, led by Mark Durcan, COO, Micron, and poster sessions for contributed papers. The poster papers will cover new developments in characterization/metrology technology especially at the nanoscale. Additional information on the upcoming 2007 Conference, including details on registration, accommodations, and other program information, are available on-line at www.eeel.nist.gov/812/conference/.

The highly regarded 2005 Conference was held the University of Texas at Dallas, Richardson, TX. Michael Polcari, President and CEO of International SEMATECH, Hans Stork, CTO of Texas Instruments, and Dan Hutcheson, CEO and President of VLSI Research Inc., presented keynote talks while Bernard Meyerson, IBM Fellow and

Chief Technologist and VP of STG, spoke at an evening banquet.

The proceedings for the previous five conferences in this series were published as hardcover volumes by the American Institute of Physics, New York. The most recent proceedings, *Characterization and Metrology for ULSI Technology: 2005* (pictured below), was published in September 2005 and is available for purchase at proceedings.aip.org/proceedings/confproceed/788.jsp.



Cover of the proceedings for the 2005 International Conference on Characterization and Metrology for ULSI Technology, which was published in September 2005.

STRONG STUDENT OUTREACH

The Semiconductor Electronics Division recognizes the importance to our country of motivating students and increasing their interest in science and engineering. It is critical to help our young students develop a love of science, and to foster this love, giving the students an opportunity to grow academically.

As such, the Division offers opportunities for students in primary and secondary schools to visit and to learn some of the fundamentals of what we do in fun, informative presentations and demonstrations. College students interested in pursuing careers in science and engineering are welcomed to join our research teams as Summer Undergraduate Research Fellowship (SURF) Program students or guest researchers. The students enjoy the luxury of having mentors who are among the best in the world in their fields.



The Division as well as CSTL brought in several students from the University of New Orleans who were displaced by Hurricane Katrina. The students are pictured above, along with Division and CSTL staff.



The Division's 2006 Summer Undergraduate Research Fellowship (SURF) Program students.



Twenty-four students from the Church of the Redeemer School gather in the Division's conference room to learn about NIST, electricity, science history, computer chips, biology, and nanotechnology.



During a visit by the Lancaster Mennonite School, the Division's John Suehle presents his work of electrical characterization and reliability to the students.

“Education in science, mathematics, and technology has become a focus of intense concern within the business and academic communities. The domestic and world economies depend more and more on science and engineering. But our primary and secondary schools do not seem able to produce enough students with the interest, motivation, knowledge, and skills they will need to compete and prosper in such a world”

Rising Above the Gathering Storm: Energizing and Employing America for a Brighter Economic Future, pg. 3-25.

DIVISION STAFF RECOGNIZED WITH ROSA AND SILVER MEDAL AWARDS

GRIESSER, MESSINA, SIMMON, AND ARONOFF RECEIVE ROSA AWARD

Arthur Griesser, John Messina, Eric Simmon, and Matthew Aronoff of the Semiconductor Electronics Division were recognized with the 2006 Edward Bennet Rosa Award. The research team was recognized for spearheading the development and release of a critical standard to help U.S. electronics manufacturers comply with new European Union environmental regulations, which threatened to block sales of noncompliant products. The standard they produced, IPC-1752, has been downloaded by more than 3,200 people in 50 countries while still in draft format, making it the most downloaded standard IPC has ever published.

The team provided key technical contributions and was instrumental in establishing the standards committee, which brought together multiple companies and consortia, including RosettaNet and iNEMI, to develop this critical material declaration standard. Additionally, the team helped execute a low-cost implementation of the standard for economically vulnerable small and medium manufacturers to decrease their cost of complying with the new legislation.

BRADY, BUCK, EDELSTEIN, HAJDAJ, HENEIN, KIRILLOV, OWEN, ROPPOLO, SUEHLE, AND VOGEL RECEIVE 2006 SILVER MEDAL

Kevin Brady, Larry Buck, Monica Edelstein, Russ Hajdaj, Gerard Henein, Oleg Kirillov, James Owen, Rich Roppolo, John Suehle, and Eric Vogel, all of (or formerly of) EEEL's Semiconductor Electronics Division, were recognized with a Department of Commerce Silver Medal Award for Scientific/Engineering Achievement. This Nanofab Team laid the foundation for a state-of-the-art facility to enable NIST and its partners to advance nanotechnology through the fabrication of advanced devices and measurement artifacts.

The team is recognized "for developing a vision, strategy, equipment fit-up, fabrication processes, policies, protocols and a safety program for the NIST AML Nanofab."

The team is praised for its vision and dedication in the introduction and development of the Nanofab, which is being further developed and operated by the Nanofab Facility Group of the NIST Center for Nanoscale Science and Technology. This facility provides a critical state-of-the-art infrastructure enabling the fabrication and measurement of a wide variety of nanoscale prototypical devices, test structures, measurement instruments, and reference materials for NIST and its partners.

KASIANOWICZ RECEIVES SILVER MEDAL AWARD

John Kasianowicz of the Semiconductor Electronics Division was recognized with a 2006 Department of Commerce Silver Medal Award for Scientific/Engineering Achievement.

Dr. Kasianowicz' novel use of protein nanopores as a "nanotool" has provided new approaches to probing the structure and function of DNA, screen for anthrax, and has spawned a new field of research. Kasianowicz is recognized "for pioneering the use of nanopores to electronically probe the structure and function of single biomolecules, and for the rapid detection of anthrax."

Dr. Kasianowicz discovered that by applying an electric field across a single biological nanopore embedded in a lipid membrane, the passage of individual single-stranded DNA molecules created a characteristic signature. This work spawned an entirely new field of science that is being applied to measuring the structure and function of single molecules, developing solid-state nanopores for the electronic sequencing of DNA, and developing new drugs and diagnostics. Dr. Kasianowicz has demonstrated how nanopore technology can be used to rapidly screen for anthrax lethal factor.

HARMAN RECEIVES IMAPS LIFETIME ACHIEVEMENT AWARD

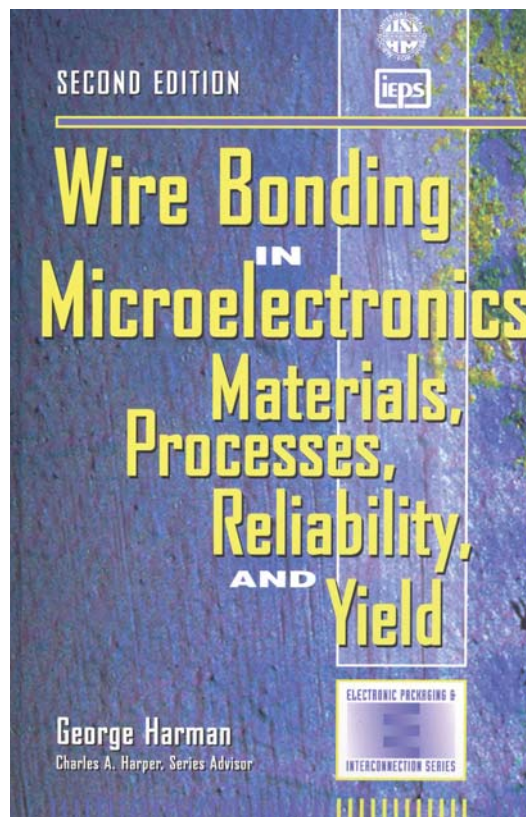
George G. Harman, EEEL Scientist Emeritus, was selected to receive the Lifetime Achievement Award in recognition of his outstanding work in EEEL's Semiconductor Electronics Division. Harman is cited for his "exceptional, visible, and sustained impact on the microelectronics packaging industry in technology..." According to the award criteria, this recognition "is to be given for sustained and notable accomplishment over the candidate's career that is beyond that normally expected of industry notables." Harman's award will be presented by the International Microelectronics And Packaging Society (IMAPS) at their San Diego symposium in Oct. 2006. This prestigious award requires the consent of the four most recent IMAPS presidents and unanimous approval of all council members.

Harman is an internationally acclaimed expert in the area of wire bonding and packaging of semiconductor chips. He is a retired NIST Fellow and a former president of IMAPS. He is considered the world's foremost authority on wire bonding. Harman presents numerous seminars and short courses on wire bonding, packaging reliability, and acoustic emission testing in electronics. He is a Fellow of the IEEE and IMAPS and has received numerous domestic and foreign awards and recognition.

Harman currently is working on the third edition of his *Wire Bonding in Microelectronics* book. The previous editions (McGraw Hill, 1989 and 1997) are considered to be the "bible" in terms of wire bonding information.



George G. Harman, EEEL Scientist Emeritus, the Semiconductor Electronics Division, NIST.



Harman's Wire Bonding in Microelectronics, Second Edition (McGraw Hill 1997).

NIST's GAITHERSBURG, MARYLAND, CAMPUS AND SURROUNDING AREA

NIST MISSION –

To develop and promote measurement, standards, and technology to enhance productivity, facilitate trade, and improve the quality of life.

NIST VISION –

To be the global leader in measurement and enabling technology, delivering outstanding value to the nation.

“Washington is located in a region that is rich in historic lore and natural beauty. From the bustling sounds of a Chesapeake Bay harbor to the utter stillness of a Blue Ridge mountaintop, from the small, old tobacco farms of southern Maryland to the grand estates of Virginia’s hunt country, you will find a richness of scenery and history.”

“Welcome to Washington” brochure, National Park Service, U.S. Department of the Interior

ABOUT NIST

The National Institute of Standards and Technology (NIST) is an agency of the U.S. Department of Commerce’s Technology Administration. NIST was established in 1901 by Congress “to assist industry in the development of technology ... needed to improve product quality, to modernize manufacturing processes, to ensure product reliability ... and to facilitate rapid commercialization ... of products based on new scientific discoveries.”

LOCATION

Located approximately 40 km northwest of Washington, D.C., on a 234 hectare campus, NIST Gaithersburg, Maryland, offers the advantages of being in close proximity to government offices, while maintaining the seclusion of a rural setting. The site is beautifully landscaped and features mature trees and ponds, as well as a herd of white-tailed deer and gaggles of Canada geese. Walking paths and picnic areas provide easy and pleasant access for outdoor repasts, biking, walking, and jogging. The campus also is easily accessible, with a shuttle service to a nearby metro (subway) station, and is in close proximity to three major airports.



NIST’s 11-story Administration Building.

STAFF

NIST employs about 2,900 scientists, engineers, technicians, and support and administrative personnel. About 1,800 NIST associates complement the staff. In addition, NIST partners with 1,400 manufacturing specialists and staff at nearly 350 affiliated centers around the country.

SOME NEARBY ATTRACTIONS

Landmarks

Bureau of Engraving and Printing
Capitol Building
Ford’s Theater
Franklin Delano Roosevelt Memorial
I.R.S. Building
J. Edgar Hoover F.B.I. Building
Jefferson Memorial
Library of Congress
Lincoln Memorial
National Archives
Supreme Court
Union Station
Vietnam Veterans Memorial
Washington Monument
White House



The NIST Gaithersburg campus is home to many different types of wildlife.

Museums and Other Attractions

Capital Children’s Museum
Corcoran Gallery
Kennedy Center
MCI Center
National Geographic Society
National Sports Gallery
National Theater
Smithsonian Institute
United States Holocaust Memorial Museum

Outdoor Attractions

Antietam National Battlefield Site
C&O Canal National Historical Park
Clara Barton National Historic Site
Eisenhower National Historic Site
Fort McHenry
Fort Washington
Gettysburg National Military Park
Glen Echo Park
Great Falls Park
Greenbelt Park
Mount Vernon
Oxon Hill Farm
Prince William Forest Park
Rock Creek Park
Shenandoah National Park
Wolf Trap Farm Park for the Performing Arts

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