PRF_{INT} = PRF of the interfering radar

PRF_{DSR} = Design PRF of the receiver

r and s are integers

The integer, r, indicates minimum number of times an interfering pulse must circulate through the integrator before it will coincide with another interference pulse.

Generally, a more thorough investigation than the application of Equation D-14 is required to determine if partial integration will occur. This is due to the fact that all aeronautical radionavigation radars in the 2.7 to 2.9 GHz band operate in a staggered PRF mode to suppress blind speeds in the radar MTI channel. For radars operating in the stagger mode, both the interfering and desired signal stagger pulse train must be investigated. Aeronautical radionavigation radars in the 2.7 to 2.9 GHz band have two, three, four, and six stagger modes. Figures D-14 and D-15 show the six stagger modes of the ASR-7 (AN/GPN-12) and the four stagger modes of the ASR-8 (AN/GPN-20), respectively. An examination of these figures indicates that partial integration of an interfering signal is very unlikely. Also, most aeronautical radiolocations radars in the 2.7 to 2.9 GHz band have several PRF modes which are not integral multiples of each other. Therefore, it is very unlikely that partial integration of an interfering signal will occur between aeronautical radionavigation radars in the 2.7 to 2.9 GHz band. The height finding radars in the 2.7 to 2.9 GHz band have a PRF of 250 to 400, and could potentially cause partial integration interference.

Figures D-16 through D-18 show the simulated response of a feedback integrator to a single interfering pulse for normal channel asynchronous interference. The first interfering pulse at the integrator output is slightly greater than the integrator input limit level setting (V_L) due to the addition of noise, and each recirculated pulse has an amplitude of K times the preceding pulse. Figure D-18 shows that an input limit level setting of 0.34 volts will suppress asynchronous normal channel interference. For comparison purposes, Figures D-19 through D-21 show a measured ASR-8 normal channel feedback integrator (enhancer) output signal response to asynchronous interference for integrator input limiter switch settings of 63, 15, and 7, respectively. Figure D-21 shows that for an integrator input limiter switch setting of 7, asynchronous normal channel interference will be suppressed to a one volt peak noise level, and will not be visible on the PPI display.

Figure D-22 shows a simulated normal channel radar unintegrated output for three interference sources (ASR-5, INR = 10 dB; ASR-8, INR = 15 dB; and AN/FPS, INR = 20 dB), and a desired target signal-to-noise ratio of 15 dB. Figure D-23 shows for the same interference condition the radar output after feedback integration for an input limit level setting of 0.34 volts. The asynchronous interference has been suppressed (compare Figure D-23 with D-10) by the feedback integrator.

Figure D-14. ASR-7 Six Stagger Sequence

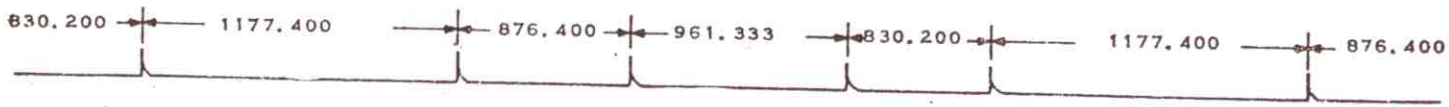

Figure D-15. ASR-8 Four Stagger Sequence

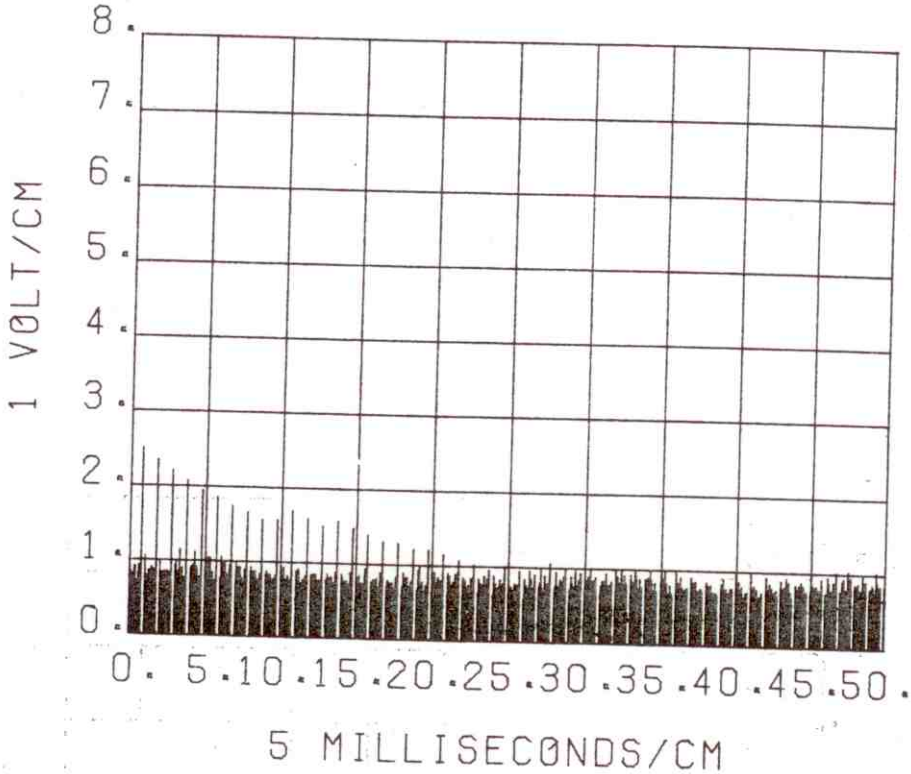

Figure D-16. Simulated Feedback Integrator Output for Asynchronous Normal Channel Interference (V_L = 2.0, INR = 30 dB)

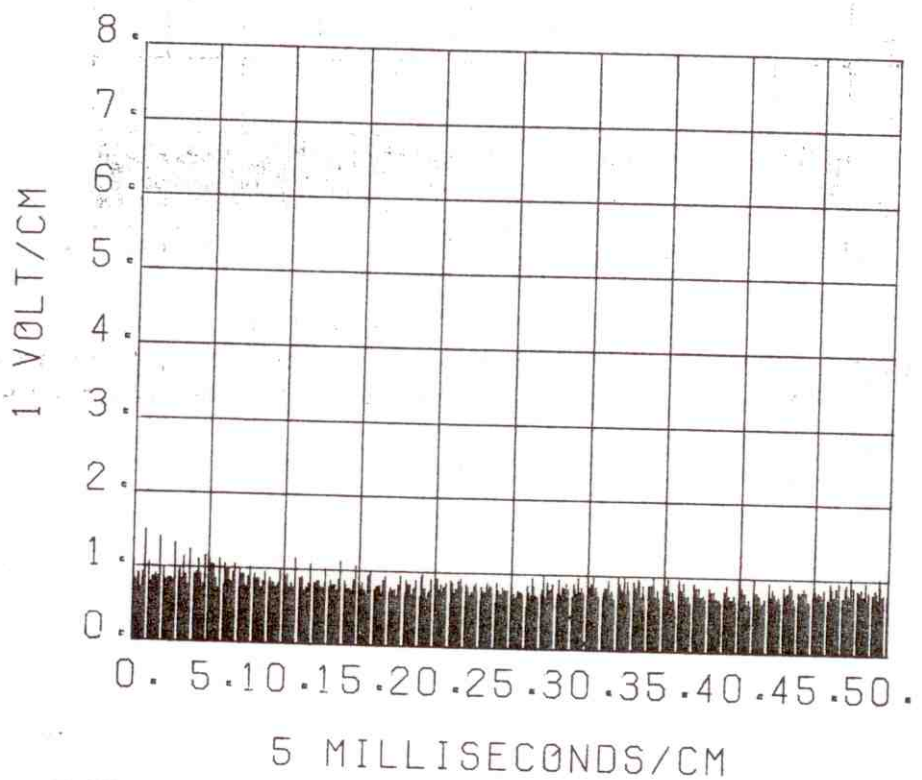

Figure D-17. Simulated Feedback Integrator Output for Asynchronous Normal Channel Interference (V_L = 1.0, INR = 30 dB)

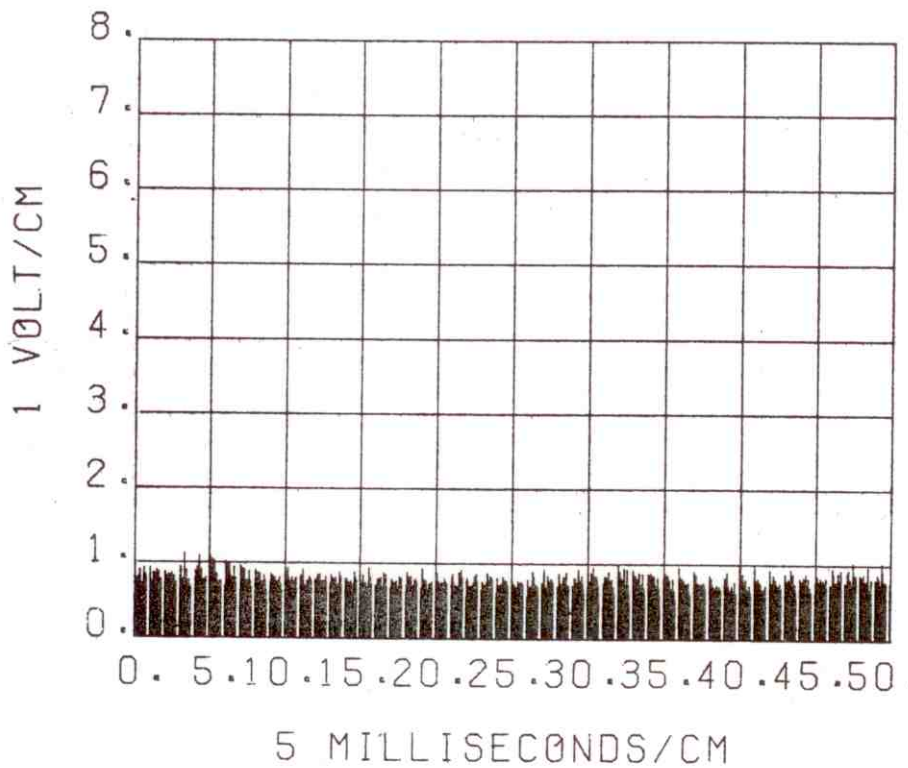

Figure D-18. Simulated Feedback Integrator Output for Asynchronous Normal Channel Interference (V_L = 0.34, INR = 30 dB)

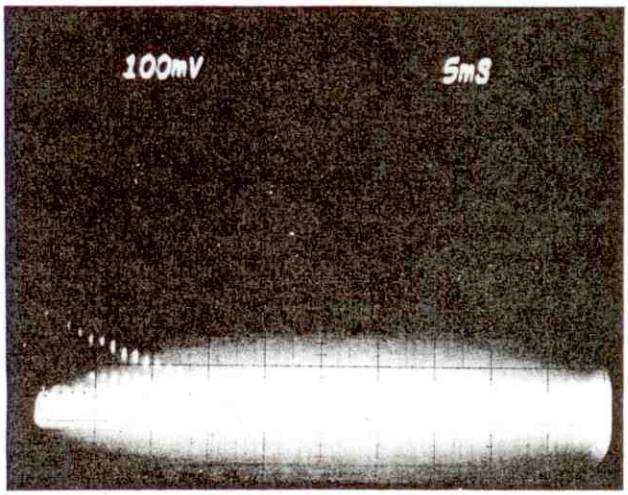

Figure D-19. Measured ASR-8 Integrator Output for Asynchronous Normal Channel Interference

Limit Adjust = 63
I = -80 dBm

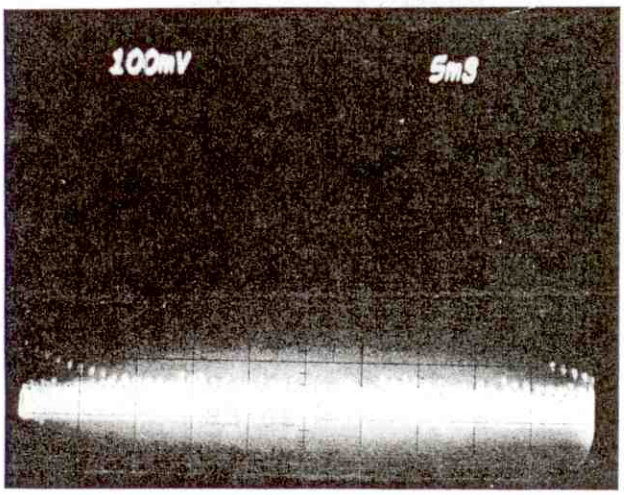

Figure D-20. Measured ASR-8 Integrator Output for Asynchronous Normal Channel Interference

Limit Adjust = 15
I = -80 dBm

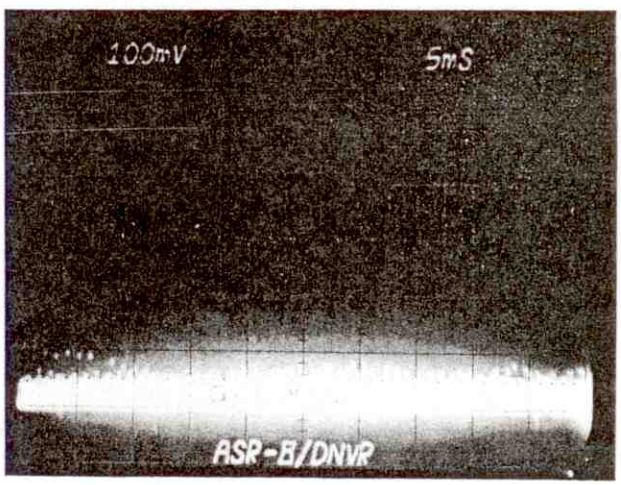

Figure D-21. Measured ASR-8 Integrator Output for Asynchronous Normal Channel Interference

Limit Adjust = 7
I = -80 dBm

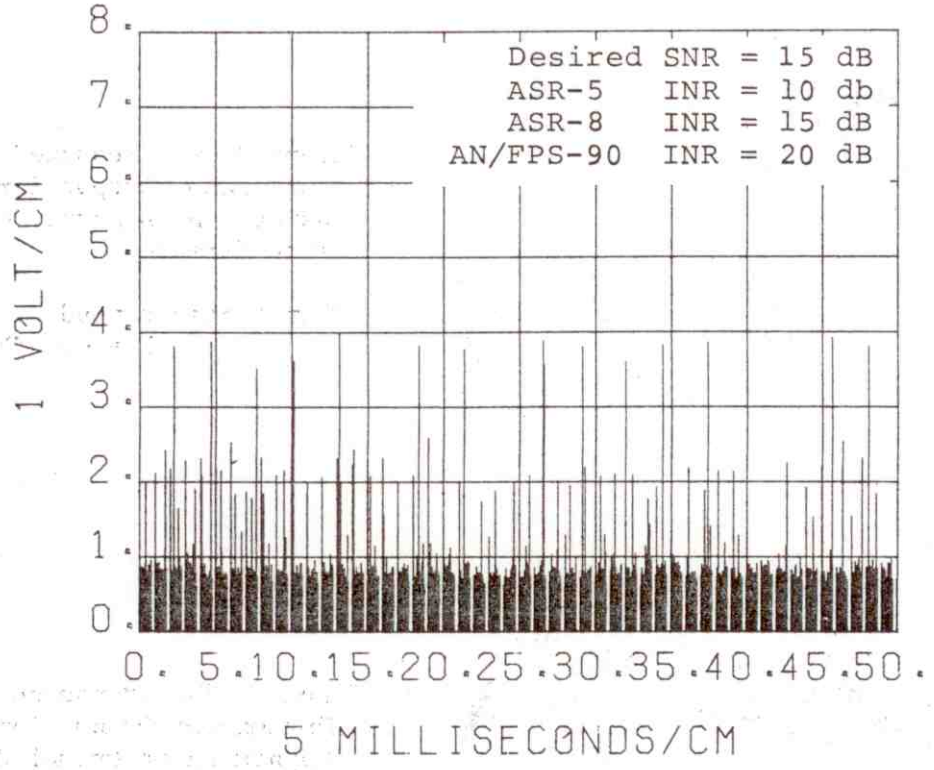

Figure D-22. Simulated Normal Channel Unintegrated Radar Output with Interference

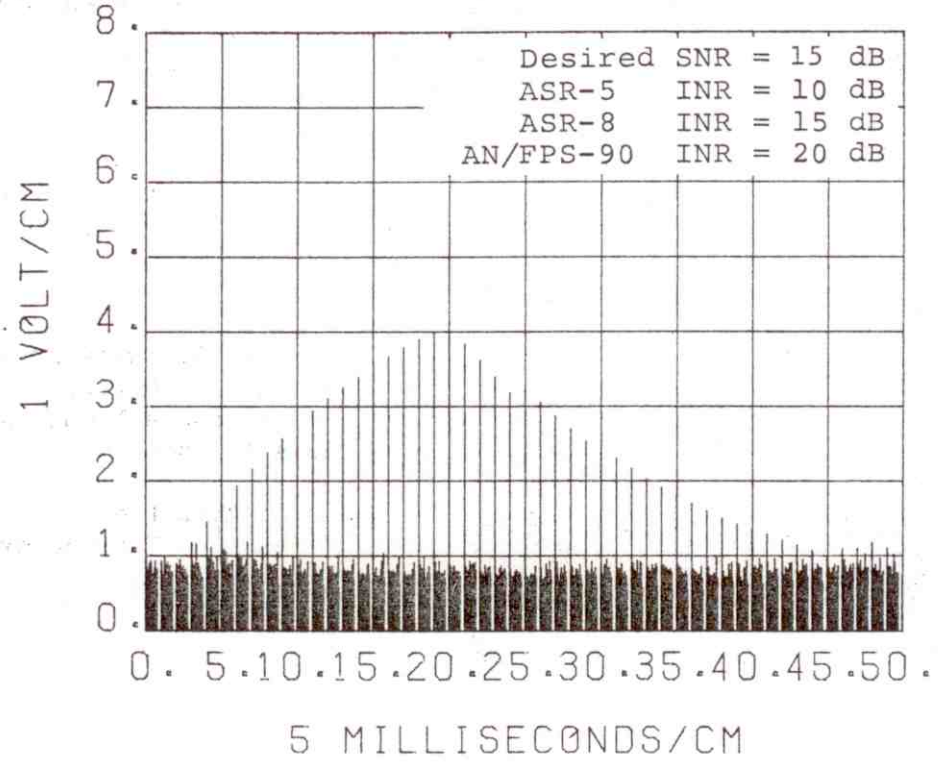

Figure D-23. Simulated Normal Channel Integrated Radar Output with Interference

Figures D-24 through D-26 show the simulated response of a feedback integrator to a single interfering pulse for MTI channel asynchronous interference. The MTI channel is simulated for a double stage canceller without feedback (1 and 2 CASC mode). As mentioned in Appendix C, for asynchronous interference a double stage MTI canceller will cause three synchronous pulses at the MTI canceller output for each asynchronous interfering pulse. Thus, asynchronous MTI channel interference will be enhanced by the feedback integrator unless the integrator input limit level is properly adjusted. This MTI channel asynchronous integration effect is shown in Figures D-24 through D-26. These figures show a three pulse integration, and then a pulse train decay of K times the previous pulse. For a radar operating in a single stage MTI canceller mode, only two pulses would be integrated. If the radar is operating in a MTI mode where canceller feedback is used for velocity response shaping, several pulses will be integrated for each asynchronous interfering pulse. Figure D-26 shows that for asynchronous interference in a double stage MTI canceller channel, a feedback integrator input limit level (V_L) setting of .34 volts will suppress the asynchronous interference level at the integrator output to 1.0 volts. In order to suppress the interference to the 1.0 volt level, additional subtraction (0.5 volts for the MTI channel as compared to 0.3 volts for the normal channel) was required at the integrator input. This additional subtraction reduces the noise level below the standard one volt level. A discussion of the additional circuitry prior to the feedback integrator is given in Appendix E.

Figures D-27 through D-29 show for comparison with the simulated integrator model (Figures D-24 through D-26) measured ASR-8 MTI channel integrator (enhancer) output signal response to asynchronous interferenece for integrator input limit switch settings of 63, 15, and 5, respectively. Figures D-27 and D-28 show the enhancement of the asynchronous interference by the integrator due to the three pulse synchronous response of the MTI double canceller circuitry. Figure D-29 shows that for an integrator (enhancer) limiter switch setting of 5, asynchronous MTI channel interference will be suppressed to the one volt peak noise level, and thus will not be visible on the PPI display. It should also be noted that the MTI channel required a limiter switch setting of 5 to suppress the asynchronous interference as compared to a limiter switch setting of 7 to suppress normal channel asynchronous interference. This is to be expected because of the synchronous pulse output response of the MTI channel to asynchronous interference. Also a comparison of Figure D-19 with Figure D-27 shows that the feedback integrator will enhance the MTI channel interference if the feedback integrator is not adjusted properly.

Figure D-30 shows a simulated single channel MTI canceller radar unintegrated output for three interfering sources (ASR-5,INR = 10 dB; ASR-8, INR = 15 dB; and AN/FPS-90, INR = 20 dB), and a desired target signal-to-noise ratio (SNR) of 20 dB. As discussed previously the asynchronous MTI channel interference can be enhanced if the feedback enhancer is not adjusted properly. Figure D-31 shows a simulated output of a

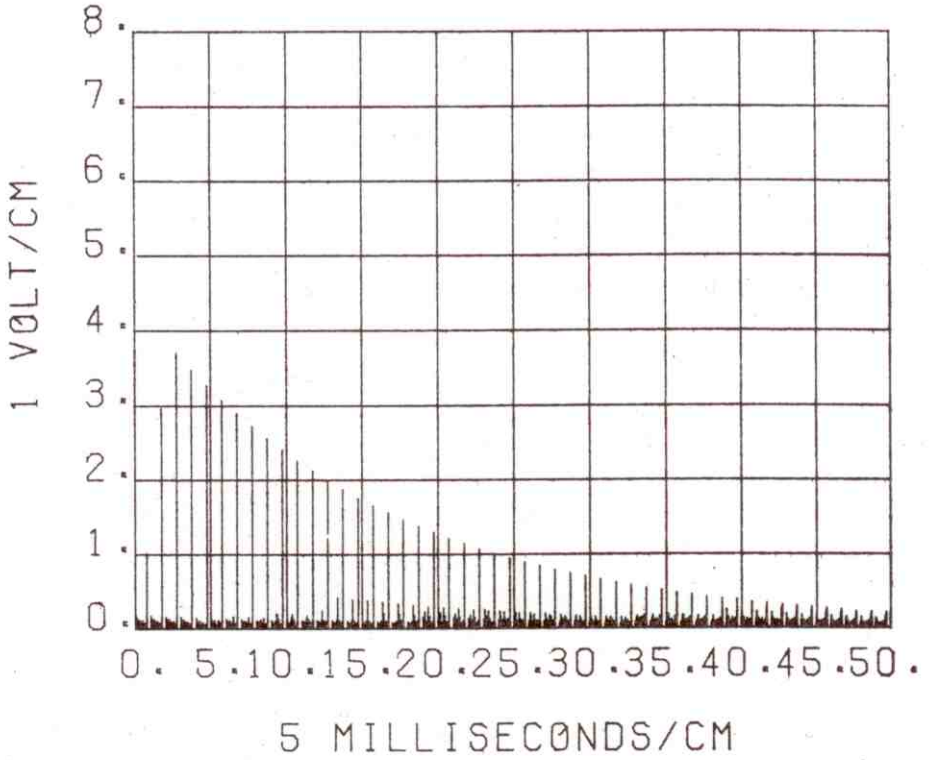

Figure D-24. Simulated Feedback Integrator Output for Asynchronous MTI Channel Interference (V_L = 2.0, INR = 30 dB)

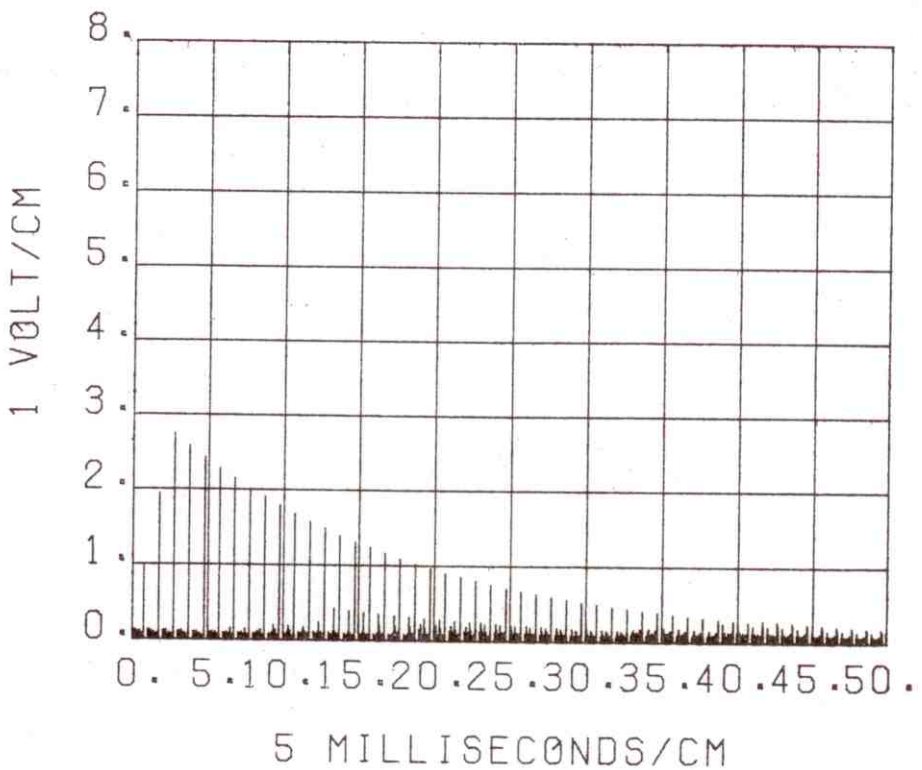

Figure D-25. Simulated Feedback Integrator Output for Asynchronous MTI Channel Interference (V_L = 1.0, INR = 30 dB)

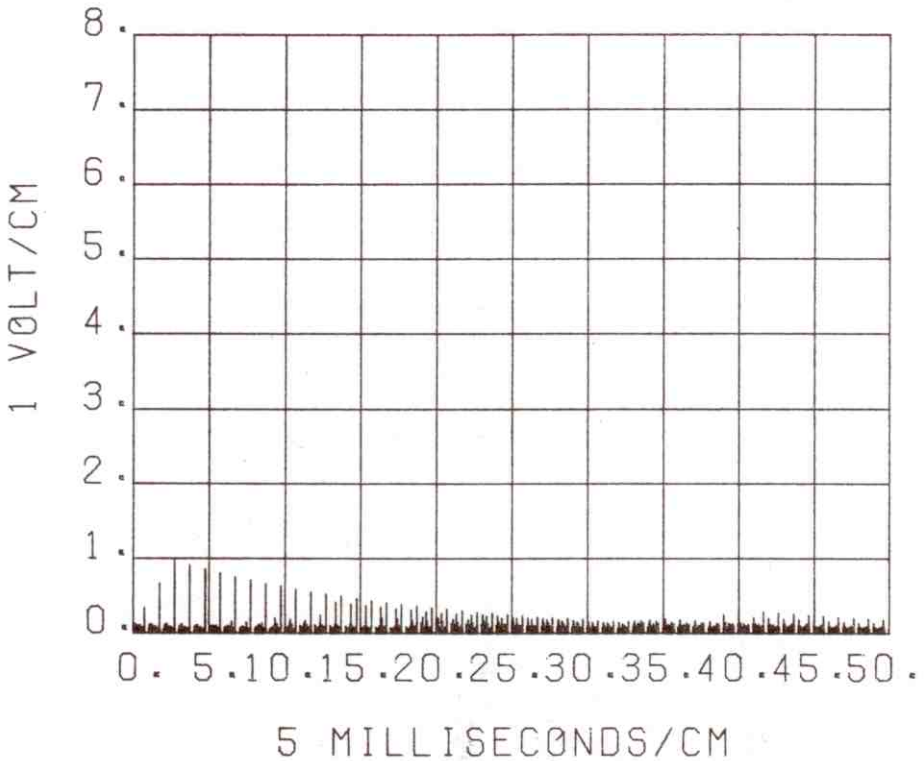

Figure D-26. Simulated Feedback Integrator Output for Asynchronous MTI Channel Interference (V_L= 0.34, INR 30.0 dB)

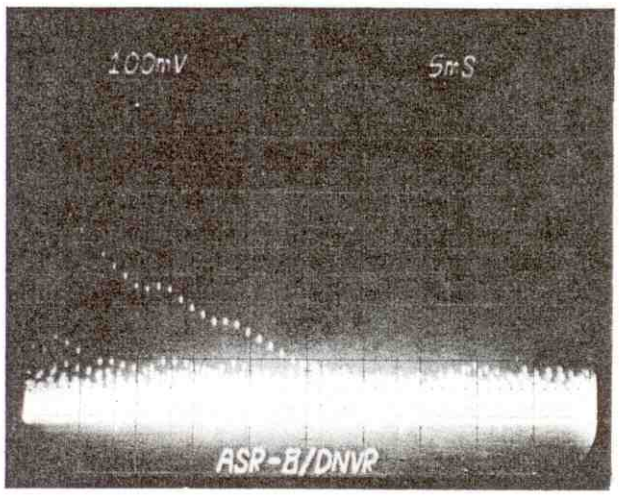

Figure D-27. Measured ASR-8 Integrator Output for Asynchronous MTI Channel Interference

Limit Adjust = 63
I = -80 dBm

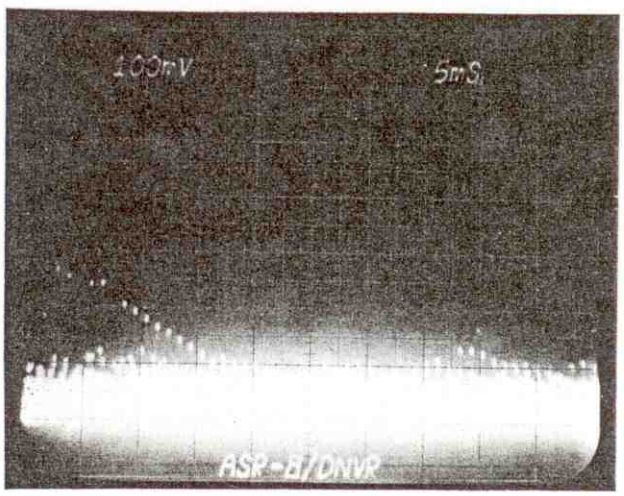

Figure D-28. Measured ASR-8 Integrator Output for Asynchronous MTI Channel Interference

Limit Adjust = 15
I = -80 dBm

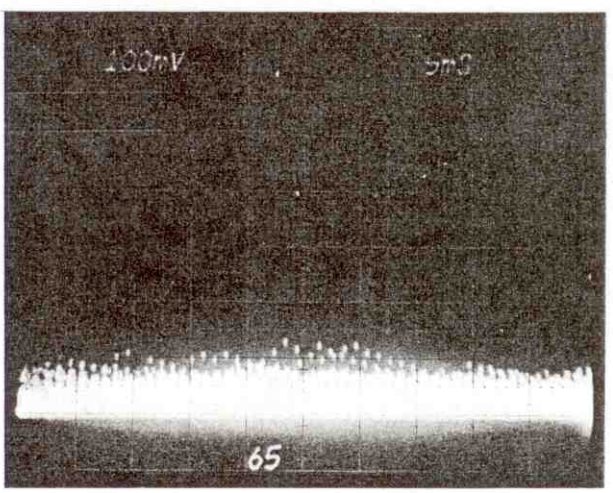

Figure D-29. Measured ASR-8 Integrator Output for Asynchronous MTI Channel Interference

Limit Adjust = 5
I = -80 dBm

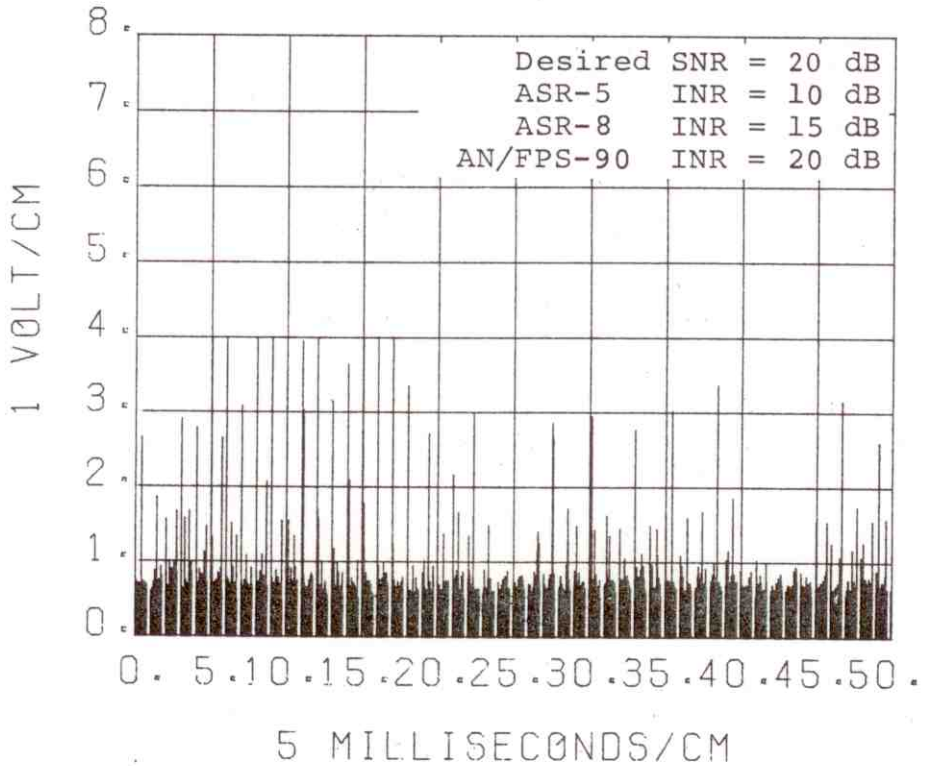

Figure D-30. Simulated MTI Channel (mode 1 & 2 CASC) Unintegrated Radar Output with Interference

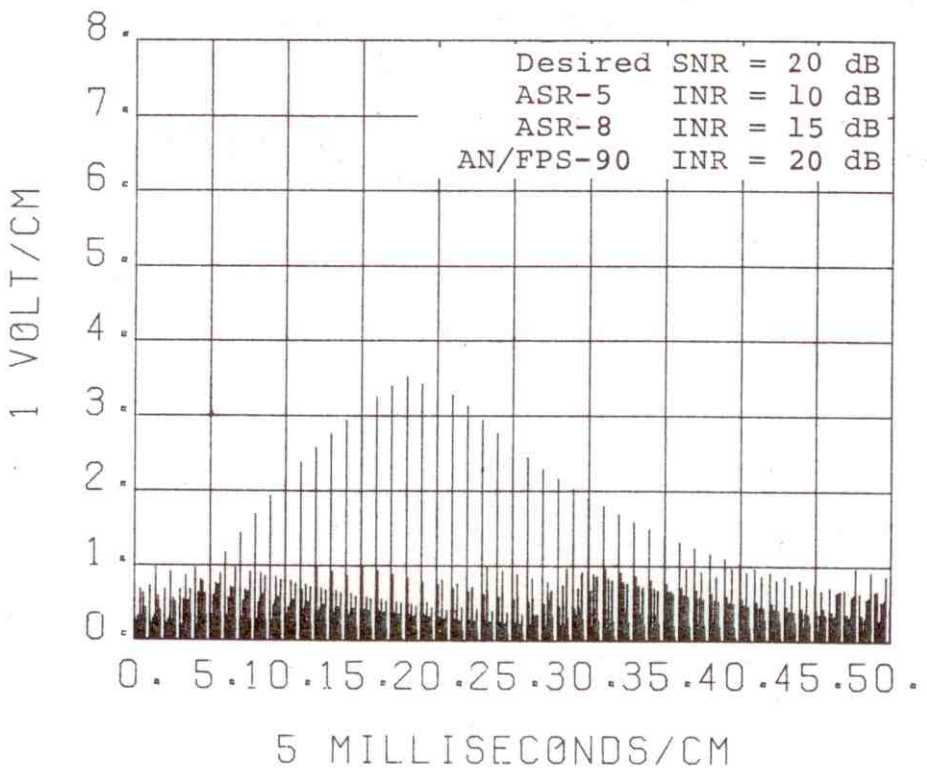

Figure D-31. Simulated MTI Channel (mode 1 & 2 CASC) Integrated Radar Output with Interference

feedback integrator for the feedback integrator input limit level adjusted at .34 volts for the same interference condition shown in Figure D-30. The asynchronous interference has been suppressed by the feedback integrator.

In summary, the simulation of the feedback integrator has shown that asynchronous interference can be suppressed by a feedback integrator if adjusted properly. Measurements made on the Stapleton Airport ASR-8 radar in Denver, Colorado, also showed that on-tune interference levels of 50 dB above the receiver noise level (approximately -60 dBm) could be suppressed in both the normal and MTI channels so that they did not appear on the PPI display. The ASR-8 radar has a feedback integrator (enhancer) and dual channel (Inphase and Quadrature) MTI channel processing. The measured change in target detection sensitivity in suppressing the asynchronous interference was found to be 1 dB or less. Also given that the feedback integrator is going to be used, the trade-offs in target azimuth shift, angular resolution and target detection sensitivity to suppress asynchronous interference are minimal.

BINARY INTEGRATOR

The ASR-7 and AN/GPN-12 radars are made by the same manufacturer, and the enhancer used in the two radars are electronically identical. The integrator (enhancer) used in the two radars can be represented by the block diagram shown in Figure D-32. The binary integrator consists of a threshold detector or comparator, binary counter (adder/subcontractor circuit), a five bit shift register memory, and a digital-to-analog (D/A) converter. Each PRF period is divided into range bins of .625 μs. If a pulse of a target return pulse train exceeds the comparator threshold level, the enhancer stores a one level digital signal in the shift register memory for that range bin. If the successive pulses of the target return pulse train continue above the comparator threshold in the given range bin, the binary counter will add one level to the stored digital signal in the shift register memory in each PRF period until a maximum integrator level of 31 is reached. If in any PRF period the signal fails to exceed the comparator threshold, the binary counter subtracts one from the stored integrator state in the given range bin until a digital signal level of zero is reached. The subtraction provides the target return pulse train signal decay required after the antenna beam has passed the target, and also enables the suppression of asynchronous interfering signals. The voltage amplitude at the enhancer D/A converter output is determined by the binary counter level (0 to 31) for the particular range bin times .125 volts. Therefore, for a binary counter level of 31, the maximum enhancer output voltage would be 3.875 volts (31 x .125).

FAA Integrator Modification

The following is a discussion on the modification the FAA made to the ASR-7 integrator (enhancer) to improve the desired signal probability of detection, target azimuth shift, and angular resolution loss caused by the conventional integrator used in the ASR-7 radar.

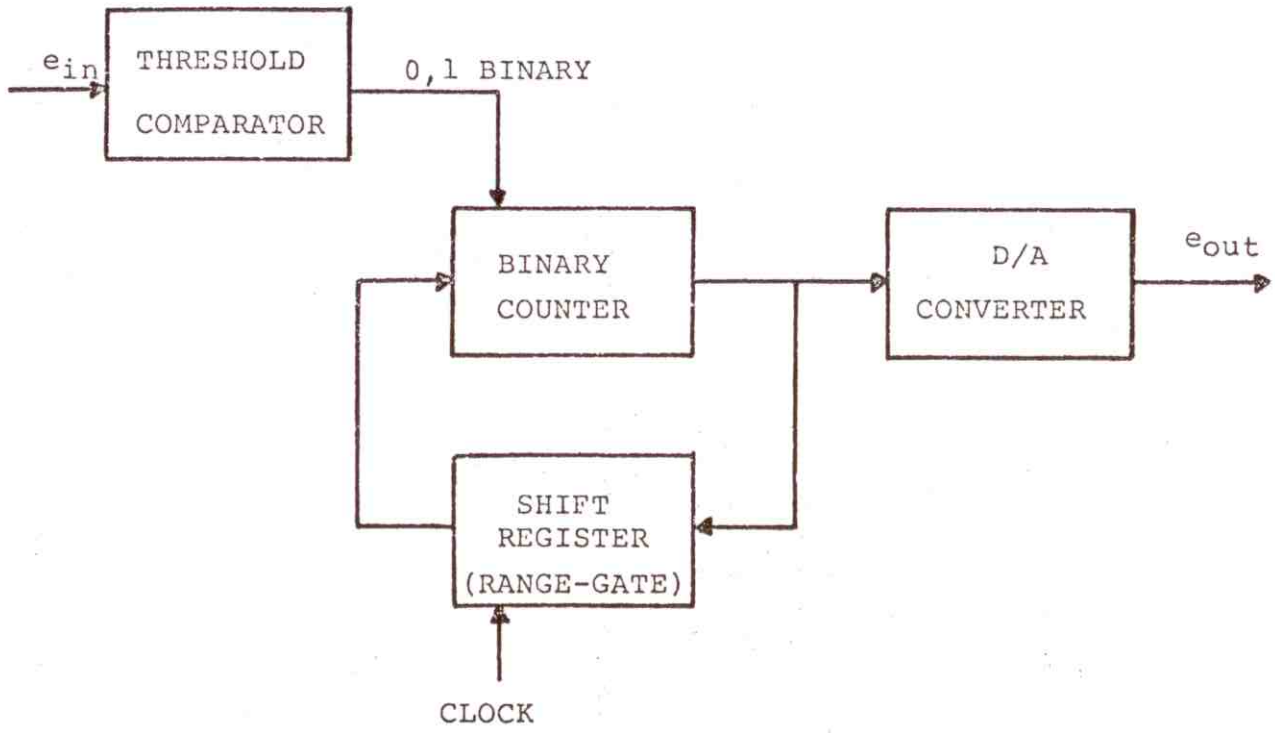

Figure D-32 ASR-7 (AN/GPN-12) Binary Integrator Block Diagram

The FAA made modifications to the manufacturer's integrator (enhancer) printed circuit board due to deficiencies that were observed on the ASR-7 video enhancer at operational field sites. Deficiencies that were observed were: (1) loss of weak targets due to design of the enhancer integrator, and (2) excessive azimuth shift of the target (NAFEC Letter Report, FAA-MA-76-39-LR, 1976).

Figure D-33 shows a block diagram of the FAA modified video enhancer. The major modification made by the FAA is the replacement of the binary counter (IC's) with a programmable read-only-memory (PROM) logic. The PROMS permit the bypassing of some of the intermediate levels (E_j = 0 to 31), depending on the PROM programming. Figure D-34 shows the FAA standard hit/miss characteristic curve which is programmed into the PROMS. The figure shows that the enhancer state is a nonlinear function of the target hits above the comparator threshold level. It only takes four hits to get to level 8 (one volt noise level), and six hits to get to level 31 (3.875 volts). This results in a strong target enhancement with only a few hits. The primary advantage of the PROM enhancer is that, due to its programmable feature, it permits a radar site flexibility in selecting a hit-count sequence based on the radar sites environment (interference and clutter). Similarly, the miss-count sequence can be precisely controlled to minimize target azimuth shift and maximize angular resolution. In this way, the video enhancer performance can be optimized to give improved performance in a variety of environmental conditions.

The following discussion will center on the particular signal processing characteristics of the conventional integrator deployed in the ASR-7 and AN/GPN-12 and the modified ASR-7 integrator to noise, desired target return pulse train, and asynchronous interference.

Noise

The noise amplitude distribution at the normal or dual MTI channel integrator (enhancer) input is Rayleigh distributed, and the noise amplitude distribution at a single MTI channel integrator input is one-sided Gaussian distributed. The noise amplitude distributions at the normal or dual MTI channel output can be expressed as:

$$p(v) = \frac{v}{\sigma^2} e^{-v^2/2\sigma^2}; \quad 0 \leq v \leq +\infty \qquad \text{(D-15)}$$

where the rms noise level is $\sqrt{2}\sigma$. The noise amplitude distribution at the output of a single channel MTI canceller after rectification can be expressed as:

$$p(v) = \frac{2}{\sqrt{2\pi}\sigma} e^{-v^2/2\sigma^2}; \quad 0 \leq v \leq +\infty \qquad \text{(D-16)}$$

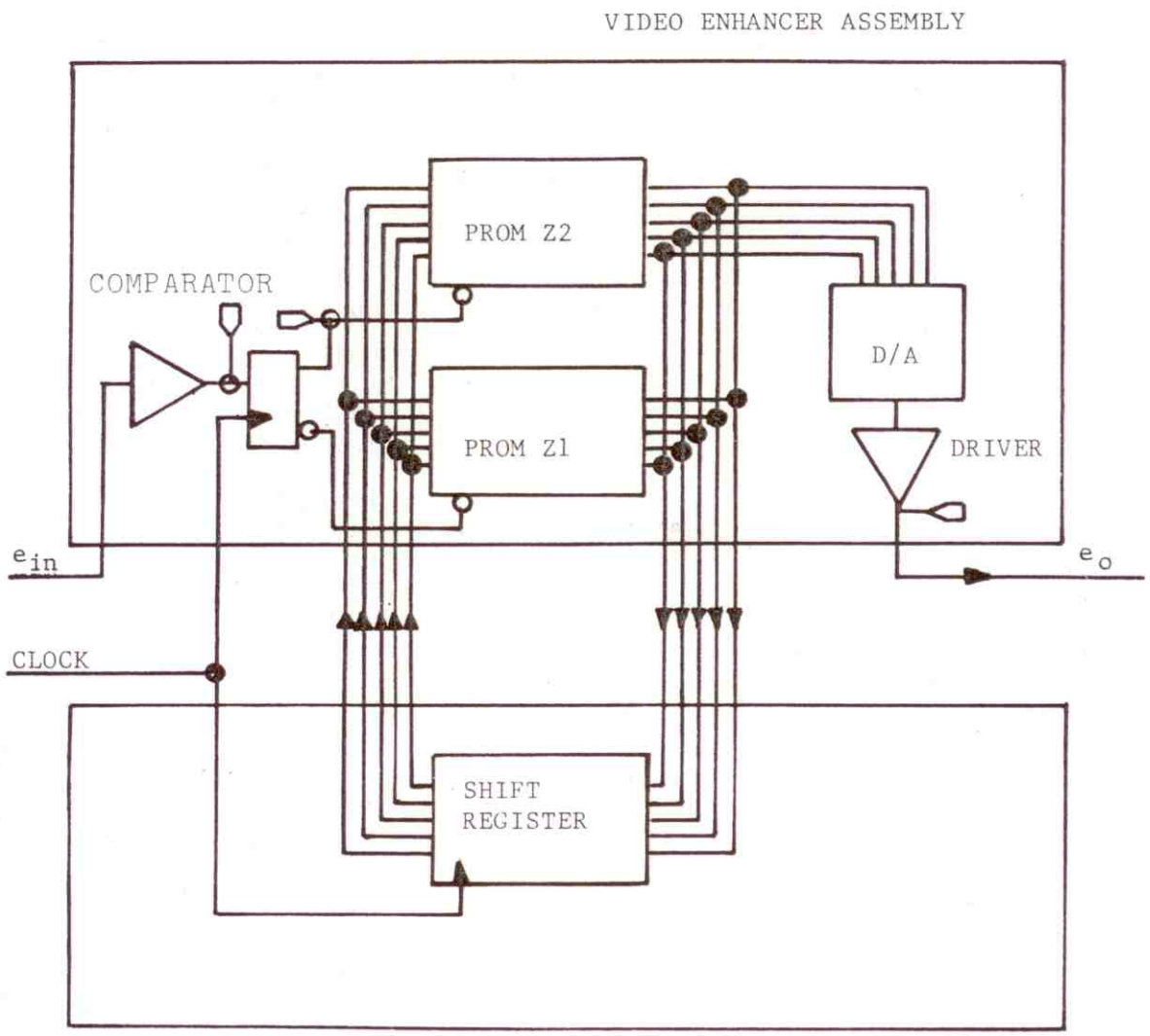

Figure D-33 FAA Modified ASR-7 Enhancer Block Diagram

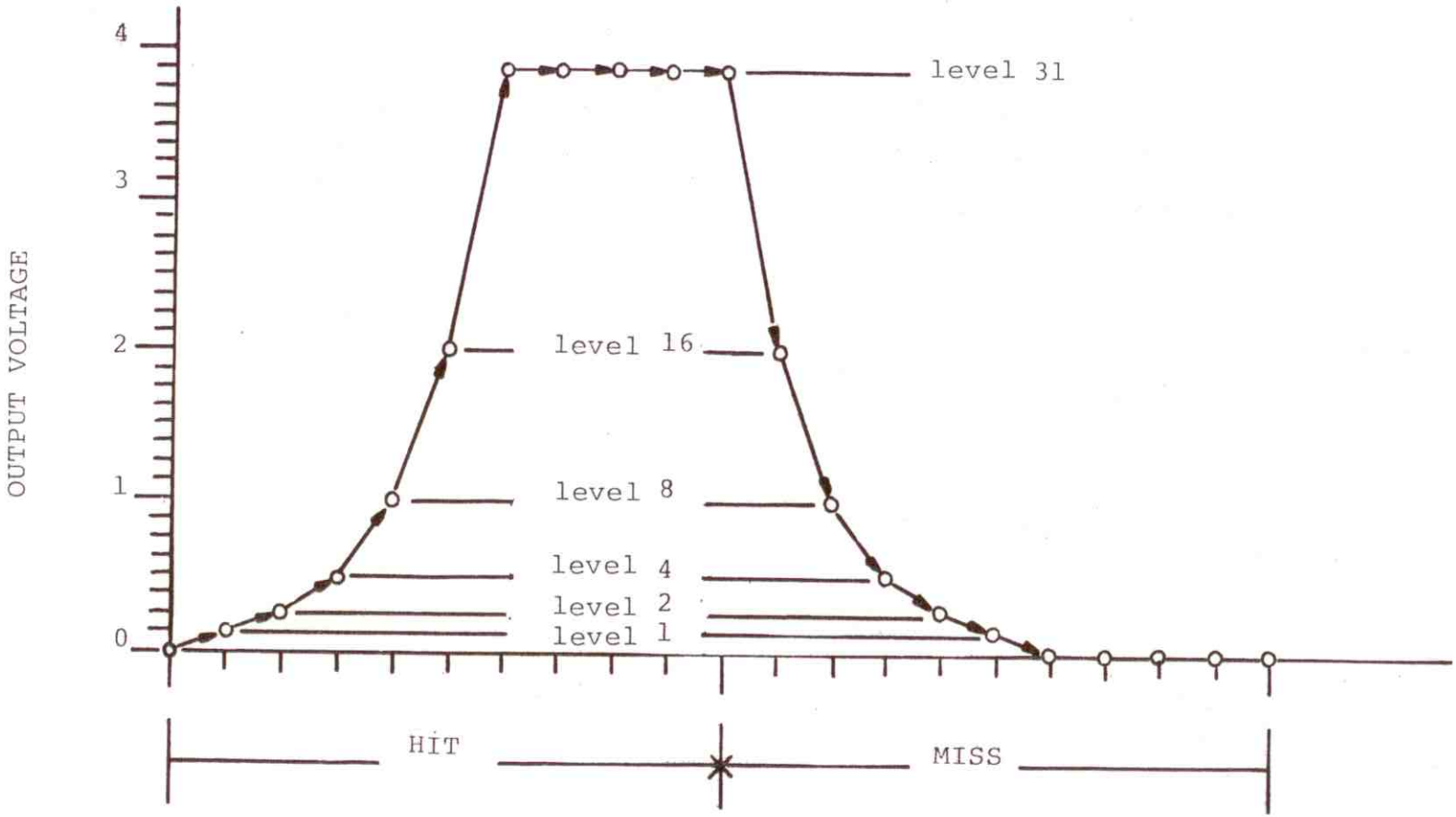

Figure D-34. Hit/Miss Characteristic Curve for FAA Modified ASR-7 Enhancer

where the rms noise level is σ.

The probability of noise causing the threshold comparator to put out a binary one in a range bin, P_{N1}, can be found for the normal and MTI channels by integrating Equations D-15 and D-16 from the threshold voltage level, T, to plus infinity. Figure D-35 shows the probability of noise causing a binary one, P_{N1}, at the threshold comparator output as a function of the threshold comparator threshold-to-rms noise ratio in dB for the normal and MTI channels.

The probability of the receiver noise causing the binary counter in the integrator to reach state E_j can be modeled by a one-dimentional random walk with reflecting barriers where levels 0 and 31 are the reflecting barriers. That is, the first and last rows of the Markov chain transition matrix are defined by (P_{N0}, P_{N1}, 0, ...) and (0, ..., 0, P_{N0}, P_{N1}). Since the noise is continually summed in the binary integrator the number of steps (k) in the random walk is infinite. It can be shown that a one-dimentional random walk with reflecting barriers model for an infinite number of steps is identical to a truncated single channel queue. The arrival rate, λ, and the departure rate, μ, of the queuing system is given by:

$$\lambda = \frac{P_{N1}}{\Delta T} \qquad \text{(D-17)}$$

$$\mu = \frac{1-P_{N1}}{\Delta T} = \frac{P_{N0}}{\Delta T} \qquad \text{(D-18)}$$

Where:

P_{NO} = Probability of the noise causing a 0 at threshold comparator output

P_{N1} = Probability of the noise causing a 1 at threshold comparator output

ΔT = Period of the radar range bin

$1/\lambda$ = False alarm time

The probability that the binary counter is in state, E_j, at epoch $t + \Delta T$ can be expressed as (Suaty, 1968):

$$P_j(t+\Delta T) = P_j(t)[1 - \lambda\Delta T - \mu\Delta T] + P_{j-1}(t)\ \lambda\Delta T + P_{j+1}(t)\ \mu\Delta T \qquad \text{(D-19)}$$

It can be shown that the probability of the binary counter being in any state, E_j (from the difference equation solution) due to noise P_{nj}, can be expressed as:

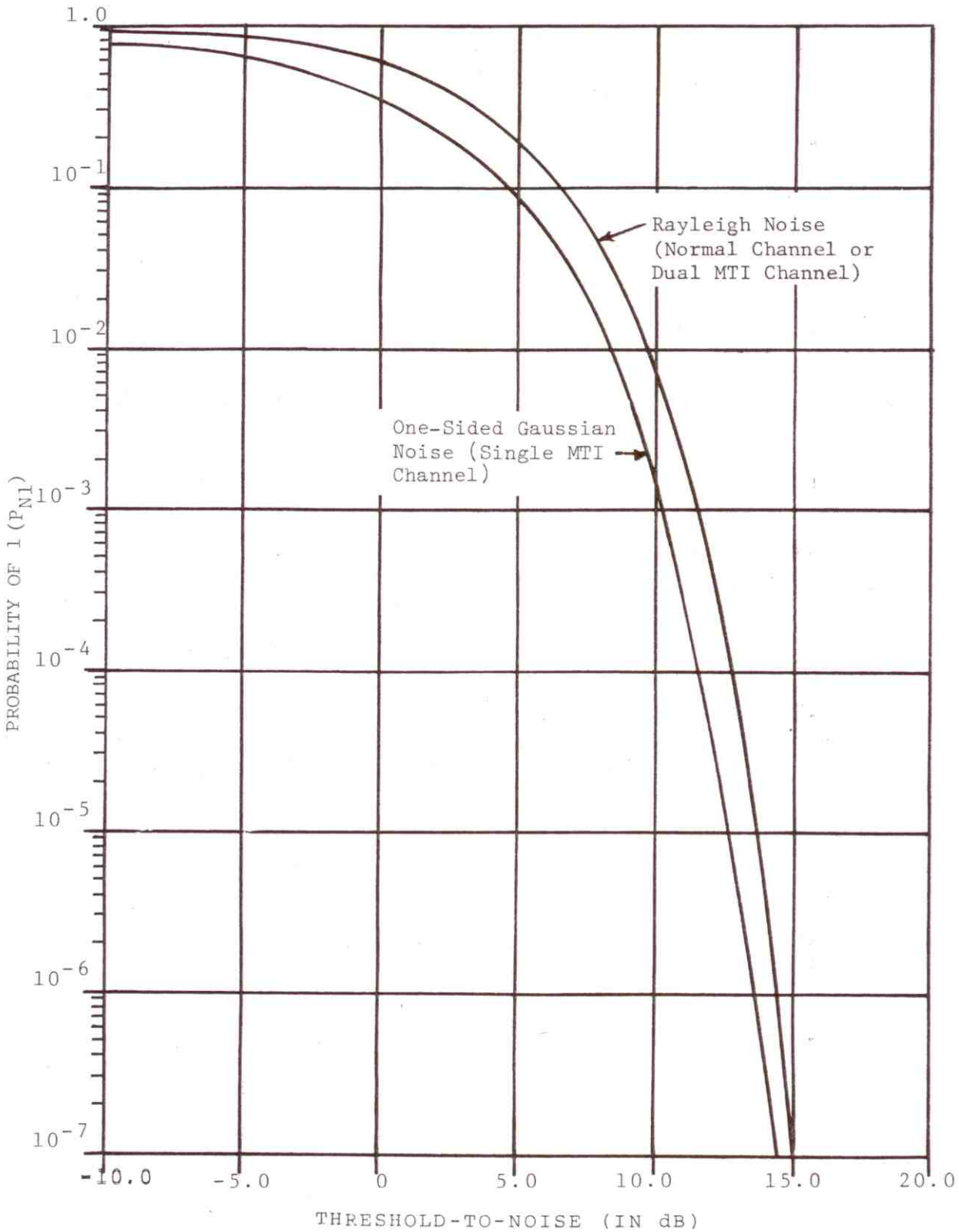

Figure D-35. Probability of Noise Causing a Binary 1 at the Threshold Comparator Output

$$P_{nj} = \lim_{t \to \infty} P_j(t) \qquad \text{(D-20a)}$$

$$= \frac{(\lambda/\mu)^{j-1}}{\sum_{j=1}^{\rho} (\lambda/\mu)^{j-1}} = \frac{(P_{N1}/P_{N0})^{j-1}}{\sum_{j=1}^{\rho} (P_{N1}/P_{N0})^{j-1}} \qquad \text{(D-20b)}$$

Where:

ρ = Number of states (function of counter level sequence)

The values for P_{N1} as a function of the threshold-to-rms noise ratio are obtained from Figure D-35 for the various channels, and $P_{N0} = 1-P_{N1}$. It should also be noted that the integrator output noise amplitude distribution is independent of the noise amplitude distribution at the input to the integrator. Since the integrator output noise distribution is independent of the noise amplitude distribution at the input of the integrator, an analytical expression for the integrator noise gain can not be expressed. However, the integrator output rms noise level can be expressed as:

$$N_{Io} = \sqrt{\sum_{j=1}^{\rho} [\,0.125(j-1)P_{nj}]^2} \qquad \text{(D-21)}$$

The rms noise level at the integrator output is a function of the threshold comparator threshold level setting. Normally the threshold comparator threshold level is adjusted to produce a peak noise level at the integrator outputs of one volt. Therefore, the binary counter level should not exceed counter level 8 (8 x .125 = 1.0 volts) with a probability of .0001 for a probability of false alarm of 10^{-4}. That is:

$$\sum_{j=1}^{c} P_{nj} \geq .9999 \qquad \text{(D-22)}$$

where:

c = State corresponding to counter level 8

TABLE D-3 shows the probability of the binary counter reaching each state due to noise, P_{nj}, and the cumulative probability of P_{nj} for comparator threshold settings with a probability of binary one, P_{N1}, of 10^{-2}, 10^{-1}, and .2625.

TABLE D-3

PROBABILITY OF NOISE CAUSING THE INTEGRATOR TO BE IN STATE E_j

State E_j	Counter Level	$P_{N1} = 10^{-2}$		$P_{N1} = 10^{-1}$		$P_{N1} = .2625$	
		P_{nj}	ΣP_{nj}	P_{nj}	ΣP_{nj}	P_{nj}	ΣP_{nj}
1	0	.989898990+000	.989898990+000	.888888891+000	.888888891+000	.644067805+000	.644067805+000
2	1	.999897957-002	.999897970+000	.987654306-001	.987654321+000	.229244467+000	.873312273+000
3	2	.100999792-003	.999998969+000	.109739365-001	.998628258+000	.815954864-001	.954907759+000
4	3	.102019991-005	.999999990+000	.121932626-002	.999847584+000	.290424606-001	.983950220+000
5	4	.103050495-007	.100000000+001	.135480693-003	.999983065+000	.103371467-001	.994287366+000
6	5	.104091408-009	.100000000+001	.150534101-004	.999998118+000	.367932332-002	.997966690+000
7	6	.105142835-011	.100000000+001	.167260109-005	.999999791+000	.130958963-002	.999276279+000
8	7	.106204882-013	.100000000+001	.185844562-006	.999999977+000	.466125110-003	.999742405+000
9	8	.107277657-015	.100000000+001	.206493955-007	.999999997+000	.165908933-003	.999908313+000
10	9	.108361269-017	.100000000+001	.229437723-008	.100000000+001	.590523308-004	.999967366+000
11	10	.109455826-019	.100000000+001	.254930799-009	.100000000+001	.210186257-004	.999988384+000
12	11	.110561439-021	.100000000+001	.283256438-010	.100000000+001	.748120557-005	.999995866+000
13	12	.111678219-023	.100000000+001	.314729370-011	.100000000+001	.266280192-005	.999998528+000
14	13	.112806281-025	.100000000+001	.349699294-012	.100000000+001	.947776931-006	.999999476+000
15	14	.113945737-027	.100000000+001	.388554765-013	.100000000+001	.337344323-006	.999999814+000
16	15	.115096702-029	.100000000+001	.431727509-014	.100000000+001	.120071705-006	.999999934+000
17	16	.116259294-031	.100000000+001	.479697223-015	.100000000+001	.427373856-007	.999999976+000
18	17	.117433629-033	.100000000+001	.532996905-016	.100000000+001	.152116115-007	.999999992+000
19	18	.118619826-035	.100000000+001	.592218773-017	.100000000+001	.541430225-008	.999999997+000
20	19	.119818004-037	.100000000+001	.658020847-018	.100000000+001	.192712448-008	.999999999+000
21	20	.121028285-039	.100000000+001	.731134262-019	.100000000+001	.685925647-009	.100000000+001
22	21	.122250792-041	.100000000+001	.812371388-020	.100000000+001	.244143021-009	.100000000+001
23	22	.123485647-043	.100000000+001	.902634859-021	.100000000+001	.868983613-010	.100000000+001
24	23	.124732975-045	.100000000+001	.100292760-021	.100000000+001	.309299244-010	.100000000+001
25	24	.125992903-047	.100000000+001	.111436398-022	.100000000+001	.110089559-010	.100000000+001
26	25	.127265557-049	.100000000+001	.123818218-023	.100000000+001	.391844183-011	.100000000+001
27	26	.128551066-051	.100000000+001	.137575796-024	.100000000+001	.139469960-011	.100000000+001
28	27	.129849560-053	.100000000+001	.152861993-025	.100000000+001	.496418490-012	.100000000+001
29	28	.131161170-055	.100000000+001	.169846655-026	.100000000+001	.176691323-012	.100000000+001
30	29	.132486028-057	.100000000+001	.188718503-027	.100000000+001	.628901303-013	.100000000+001
31	30	.133824269-059	.100000000+001	.209687221-028	.100000000+001	.223846221-013	.100000000+001
32	31	.135176028-061	.100000000+001	.232985797-029	.100000000+001	.796740767-014	.100000000+001