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CIS Modules Process R&D

Final Technical Report
October 2005 — June 2006

D.E. Tarrant and R.R. Gay
Shell Solar Industries
Camarillo, California

Subcontract Report
NREL/SR-520-40242
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NREL Technical Monitor: Harin S. Ullal

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303-275-3000 • www.nrel.gov

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Preface

Shell Solar Industries (SSI), formerly Siemens Solar Industries, has pursued the research and development of $CuInSe_2$-based thin film PV technology since 1980. At the start of subcontract activities with NREL, SSI had demonstrated a 14.1% efficient 3.4 cm^2 active-area cell, unencapsulated integrated modules with aperture efficiencies of 11.2% on 940 cm^2 and 9.1% on 3900 cm^2, and an encapsulated module with 8.7% efficiency on 3883 cm^2.

Research on High-Efficiency, Large-Area $CuInSe_2$-Based Thin-Film Modules

SSI began a 3-year, 3 phase cost-shared subcontract (No. ZN-1-19019-5) [***1***] on May 1, 1991 with the overall project goal of fabricating a large area, stable, 12.5% aperture efficient encapsulated CIS module by scaleable, low-cost techniques on inexpensive substrates. Subcontract accomplishments were facilitated by addressing module reproducibility issues using small area test devices and mini-modules. Statistical process control disciplines were adopted to rigorously quantify process reproducibility. SSI addressed uniformity and reproducibility of absorber formation, interactions of the substrate with the absorber, and performance losses near interconnects. Subcontract accomplishments included demonstration of encapsulated module efficiencies that were at that time the highest reported mini-module efficiencies for any thin film technology (encapsulated 12.8% efficient mini-module on 68.9 cm^2 and an NREL-verified 12.7% efficient unencapsulated circuit on 69 cm^2 with a prismatic cover), demonstration of a champion large area (3860 cm^2) encapsulated module efficiency of 10.3% that was the first thin film module of its size to exceed the 10% efficiency level, and delivery to NREL of a one kilowatt array of large area (~3890 cm^2) approximately 30 watt modules.

TFPPP-1

From September 1995 through December 1998, SSI participated in a 3-year, 3 phase cost-shared Thin Film Photovoltaics Partnership Program subcontract (No. ZAF-5-14142-03) [***2***]. The primary objective of this subcontract was to establish reliable high-throughput, high-yield thin film deposition processes in order to make CIS a viable option for the next generation of photovoltaics. Outdoor testing, accelerated environmental testing, and packaging development progressed throughout all phases of this subcontract. During Phase 1, SSI rigorously demonstrating process reproducibility and yield for a 10x10-cm monolithically interconnected "mini-module" baseline process and demonstrated a 13.6% aperture area efficient mini-module. During Phase 2, SSI demonstrated the need to replace an existing large area reactor with a reactor based on a more direct scale-up of the baseline reactor, built a new large area reactor, and demonstrated comparable performance for the mini-modules baseline and larger 28x30-cm circuit plates. SSI developed products and prototype large area modules using a new package designed to integrate small circuit plates into larger modules. A one kilowatt array of $Cu(In,Ga)(S,Se)_2$ modules was delivered to NREL replacing a previously installed array based on an older absorber formation technology without sulfur incorporated in the absorber ($Cu(In,Ga)Se_2$). This array demonstrated significant improvements in efficiency and the temperature coefficient for power. SSI introduced two new 5-watt (ST5) and 10-watt (ST10) CIS-based products designed for use in 12 V systems, and NREL confirmed a new world-record efficiency of 11.1% on a SSI large area (3665 cm^2) module. During Phase 3, substrate size was scaled from ~30x30 cm to ~30x120 cm and good process control was demonstrated with an

average efficiency of 10.8%. Commercial product samples were delivered to NREL and a second set of ~30x120 cm modules (32 modules totaling ~1.2 kW) was delivered to the NREL Outdoor Test Facility. The NREL measured average efficiency at standard test conditions of 11.4% was at that time the highest large area efficiency for any thin-film technology and NREL confirmed a world-record 11.8% large area (3651 cm^2) efficiency for the champion module.

TFPPP-2

From August 1998 through November 2001, SSI participated in a 3-year, 3 phase cost-shared TFPPP subcontract (No. ZAF-5-14142-03) [***3***]. The primary objectives of this subcontract were to scale-up substrate size and to increase production capacity of the baseline CIS module process while introducing CIS-based products. These objectives were pursued to demonstrate fabrication of efficient and stable thin-film modules made by scaleable, manufacturable, low-cost techniques. An additional mid- to longer-term objective was to advance CIS based thin-film technology thereby assuring future product competitiveness by improving module performance, cost per watt produced, and reliability. Throughout this subcontract, SSI capabilities were leveraged as a Technology Partner participating in NREL team oriented TFPPP activities to address near-term to longer-term R&D topics. The SSI approach to this work was to apply design of experiment and statistical process control methodologies. SSI was the first company in the world to produce PV modules based on CIS thin-film technology. R&D Magazine recognized this major milestone in the development of PV by awarding the prestigious R&D 100 Award to the SSI family of CIS solar modules. NREL, the California Energy Commission and SSI shared this award. SSI expanded the CIS product line in 1999 to include 20-Watt "ST20" modules and 40-Watt "ST40" modules. Also during the first subcontract phase, a record-breaking efficiency of more than 12% was verified by NREL for an ST-40 module. This result in 1999 far surpassed the DOE year 2000 goal for a commercial CIS module above 10%. During the second subcontract phase, SSI delivered 20 ST-40 large area modules, all with efficiencies over 11%, to meet the subcontract deliverables defined as large area modules with efficiencies over 10%. The average efficiency based on a Gaussian fit to the main portion of the circuit plate efficiency distribution was increased from 10.8% prior to this subcontract to 11.6% for this subcontract. These advancements were due to continuous improvement of all process along with particular attention to process research for two critical processes – CIS formation in new large area reactors and the quality of molybdenum deposited in new high capacity sputtering equipment. Process development improved adhesion, decreased breakage, addressed control of raw materials, and decreased failures associated with patterning. Further R&D of all CIS processes for part size and capacity scale-up was pursued during the third subcontract phase. Major accomplishments included addressing process issues for implementation of high quality high throughput Mo deposition and patterning, high throughput precursor deposition, and higher throughput reaction of the precursor. Circuit plate production capacity was increased by more than an order of magnitude from the beginning of this subcontract while circuit and module efficiencies were steadily improved. The second subcontract milestone – to achieve a pilot production rate of 500 kW per year by the end of subcontract – was first achieved in March of 2001.

TFPPP-3

From April 2002 through April 2005, SSI participated in a 3-year, 3-phase cost-shared TFPPP subcontract (No ZDJ-2-30630-16) [***4***]. The primary objectives of this subcontract were to:

- Address key near-term technical R&D issues for continued CIS product improvement
- Continue process development for increased production capacity
- Develop processes capable of significantly contributing to DOE 2020 PV shipment goals
- Advance mid- and longer-term R&D needed by industry for future product competitiveness including improving module performance, decreasing production process costs per watt produced, and improving reliability
- Perform aggressive module lifetime R&D directed at developing packages that address the DOE goal for modules that will last up to 30 years while retaining 80% of initial power

During the performance of this subcontract, production volume per year was ramped up to 1 MW and capacity was increased to about 3 MW. Laminate efficiency distribution was tightened to a peak of 11% with full width of 11% of the average. Line yield improved from about 60% to 85%. A new "sputter-dosed" process was implemented which improved cosmetics and improved thermal stability. NREL confirmed a 12.8% champion aperture area efficiency for an ST40 production module. A glass/glass package was designed and equipment was procured to implement the processing. SSI worked with the CIS team in the TFPPP to address longer-term topics, but focused on the thermal transient effect. Efforts to certify the commercial CIS product through the IEC 61646 were not successful during the contract period.

TFPPP-4

Starting in October 2005, SSI entered a 3-year, 3-phase cost-shared TFPPP subcontract (No ZXL-5-44205-04). The primary objectives of this subcontract were to:

- Address key near-term technical R&D issues for continued improvement in thin-film PV products
- Continue process development for increased production capacity
- Pursue long term R&D contributing to progress toward the MYTP goals for 2020 to increase the conversion efficiency to 15% and reduce module manufacturing costs to less than $50/m2, thus enabling PV systems with a 30-year lifetime at an installed cost of under $2.00/W
- Advance the understanding of the requirements needed to achieve better thin-film PV cell and module performance, greater reliability and market acceptance, and investigate materials systems and new devices that can improve the cost/performance ratio of future thin-film PV factories

In February 2006, Shell announced its decision to divest its crystalline silicon solar business activities to SolarWorld AG, including all the manufacturing and support activities in Camarillo. However, because Shell continues to believe that CIS technology is likely to become competitive with retail electricity in the coming years, it announced the signing of a Memorandum of Understanding with Saint-Gobain to further explore the Shell CIS technology and to consider joint development. In Camarillo today, the silicon and CIS businesses are integrated in one company, supported by a common infrastructure. Since the CIS business is not part of the sale of the silicon assets to SolarWorld, a new infrastructure would need to be put into place to support the remaining CIS activities. In the discussions between Shell and Saint-Gobain, it was decided that the high cost of duplicating the support infrastructure could not be justified at this time. As a consequence, the CIS business activity in Camarillo is being brought to a close. This is the Final Technical Report for this contract, and will summarize the work done for the period October 2005 through April 2006. Also included is a retrospective, providing some insight into the lessons learned over the course of these subcontracts.

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The Shell Solar Industries CIS Team:

O. Frausto
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H. Nguyen
A. Ramos
C. Rischmiller
R. Steeman
D. Tarrant (Principal Investigator)
R. Wieting
D. Willett

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Summary

The primary objective of this subcontract were to:

- Address key near-term technical R&D issues for continued improvement in thin-film PV products
- Continue process development for increased production capacity
- Pursue long term R&D contributing to progress toward the MYTP goals for 2020 to increase the conversion efficiency to 15% and reduce module manufacturing costs to less than $50/m2, thus enabling PV systems with a 30-year lifetime at an installed cost of under $2.00/W
- Advance the understanding of the requirements needed to achieve better thin-film PV cell and module performance, greater reliability and market acceptance, and investigate materials systems and new devices that can improve the cost/performance ratio of future thin-film PV factories

Emphasis during this subcontract was on developing and producing a CIS product targeted for the grid-connected rooftop market and meeting IEC certification standards. To that end, an 80-watt product was designed and released. Called the "Eclipse 80-C", this product incorporates two ST40-sized circuits in a glass/glass laminate sharing a common coverglass. Both module package design and circuit plate fabrication development led to a product that passed the IEC 61646, the first CIS product in the market with this certification. As a refinement to the product strategy, the product line was split into 85-watt and 75-watt products designated the Eclipse 85-C and Eclipse 75-C, both of which also carry the IEC certification.

The Eclipse line of products were being produced in the CIS pilot manufacturing line in Camarillo, with a capacity of 3 MW. Production rate was about 2.0 MW p.a., with a line yield of about 85%. The safety record for this facility was outstanding; there were no recordable incidents or accidents for 1153 days. Process development activities during this subcontract included: improved CIG ratio control, lower cost indium targets, increased gallium content in the absorbers, simplified molybdenum deposition, improved mechanical scribing and improved lead attachment.

During prior subcontracts, the ST40 was the flagship product for the CIS manufacturing line. This single-substrate design continued to be produced during 2005. The peak of the distribution for these ST40 modules is 11.25% with a mean efficiency of 11.1%. The standard deviation of the distribution is less than 1% (corresponding to only 8.6% of the mean). During this subcontract, the Eclipse 80-C product was released. The peak of the distribution for these Eclipse 80-C modules is 11.0% with a mean efficiency of 10.8%. The standard deviation of the distribution is less than 1% (corresponding to only 7% of the mean). SSI accomplishments prior to 2003 far exceed the 2003 DOE EERE Multi-Year Technical Plan technical target of 8% module conversion efficiency for thin-film modules. SSI delivered modules to NREL to meet the Joule goals for thin films for each year from 2003 through 2006.

Long-term outdoor stability has been demonstrated at NREL where ~30x30 cm and ~30x120 cm modules with multiple prototype package designs and multiple absorber formation have

undergone testing for over seventeen years. Field failures for previous product were also observed but only for particular production timeframes. Some failures were clearly related to particular package designs or errors during production. Additional circuit plate or packaging process variables were suspected but not clearly demonstrated to have affected durability. Multiple past and present module deployments have demonstrated stability and when losses have been observed, the losses correlated with date of deployment or a particular prototype module configuration. SSI developed the "glass/glass" package primarily to decrease packaging costs. This package design was used for the Eclipse product line, which passed ALL accelerated testing and test standards defined by the IEC 61646 and received IEC qualification.

The demonstrated and maintained high production yield is a major accomplishment supporting attractive cost projections for CIS. Process R&D at successive levels of CIS production has led to the continued demonstration of the prerequisites for commitment to large-scale commercialization. Process and packaging R&D during this and previous subcontract has demonstrated the potential for further cost and performance improvements.

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Introduction

Overview

Multinary $Cu(In,Ga)(Se,S)_2$ absorbers (CIS-based absorbers) are promising candidates for reducing the cost of photovoltaics well below the cost of crystalline silicon. CIS champion solar cells fabricated at NREL have exceeded 19% efficiency [***5***]. Small area, fully integrated modules exceeding 13% in efficiency have been demonstrated by several groups [***6***]. Record breaking efficiencies of over 12% for a commercial large area module have been verified by NREL [***7***]. Long-term outdoor stability has been demonstrated at NREL by ~30x30 cm and ~30x120 cm SSI modules which have been in field-testing for over seventeen years. Projections based on current processing indicate production costs well below the cost of crystalline silicon [***6***].

Compared to traditional wafer-based crystalline silicon technologies, new thin film technologies yield products of comparable performance but with significant advantages in manufacturing [***6***, ***8***]:

- Lower consumption of direct and indirect materials
- Fewer processing steps
- Easier automation

Lower consumption of direct and indirect materials results in part from the thin-film structure for the semiconductor used to collect solar energy. All three of these manufacturing advantages are in part due to an integrated, monolithic circuit design illustrated in Figure 1. Monolithic integration eliminates multiple process steps that are otherwise required to handle individual wafers and assemble individual solar cells into the final product.

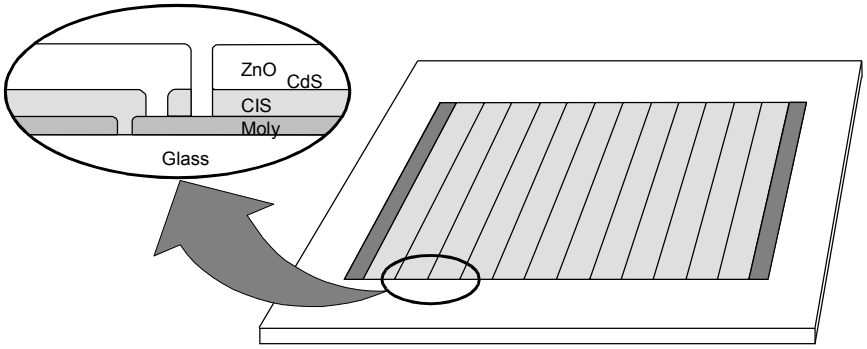


Figure 1. Structure of SSI monolithically integrated thin-film circuits.

A number of thin film photovoltaic technologies have been developed as alternatives to the traditional solar cells based on crystalline silicon wafers [***6***]. The technologies with the greatest potential to significantly reduce manufacturing costs are based on alloys of amorphous silicon (a-Si), cadmium telluride (CdTe), CIS, and film silicon (Si-film). These photovoltaic thin film

technologies have similar manufacturing costs per unit area since all share common elements of design and construction:

- Deposition of typically three layers on a suitable substrate – window/electrode, absorber, and back electrode
- Patterning to create monolithically integrated circuit plates
- Encapsulation to construct modules

Cost per watt is a more appropriate figure of merit than cost per unit area [***6***]. All thin film technologies have similar manufacturing costs per unit area since they all use similar or equivalent deposition, patterning, and encapsulation processes. About half of the total module cost – material, labor, and overhead – originates in the encapsulation scheme that is for the most part independent of the thin film technology. Costs for alternative substrates and encapsulation schemes are similar or even higher. The average efficiency of large, ~30x120 cm modules in pilot production at Shell Solar is approximately 11%. This performance is at the lower end of the range for products based on crystalline silicon. The lowest cost per peak watt will result from the technology with the highest efficiency, CIS technology, since most thin film technologies have similar cost per unit area.

SSI CIS Process

The structure of an SSI CIS solar cell is shown in Figure 2. An SEM of the crossection of a typical absorber structure is show in Figure 3.

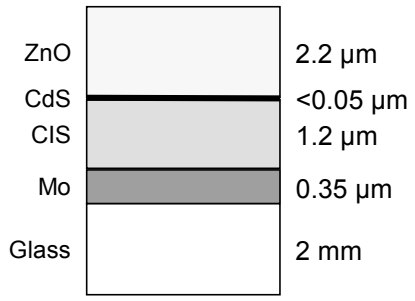


Figure 2. SSI CIS cell structure (not to scale).

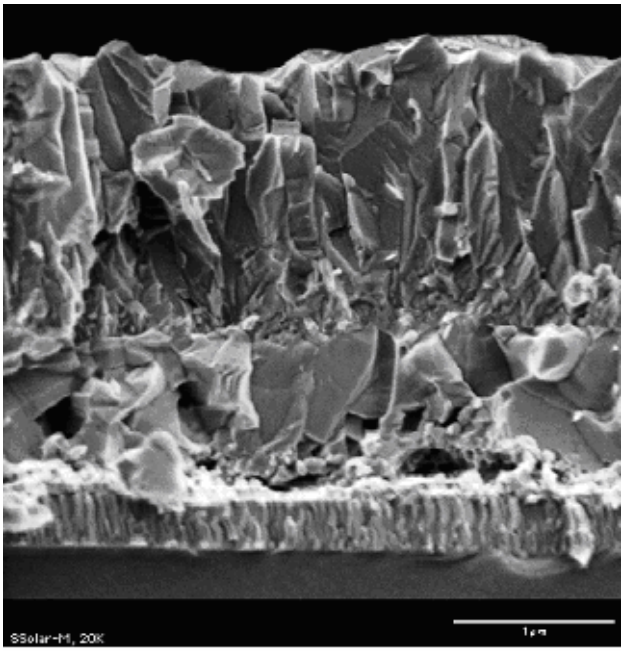


Figure 3. SEM image of the cross-section of a CIS device.

Most photovoltaic products are designed for 12-volt or higher applications, but the output voltage of an individual solar cell is typically about 0.5 volts. Wafer-based technologies build up the voltage by connecting individual solar cells in series. In contrast, CIS circuits at SSI are fabricated monolithically; the interconnection is accomplished as part of the processing sequence to form the solar cell by alternately depositing a layer in the cell structure and patterning the layer using laser or mechanical scribing. The full process to form CIS circuit plates, including monolithic integration, is outlined in Figure 4.

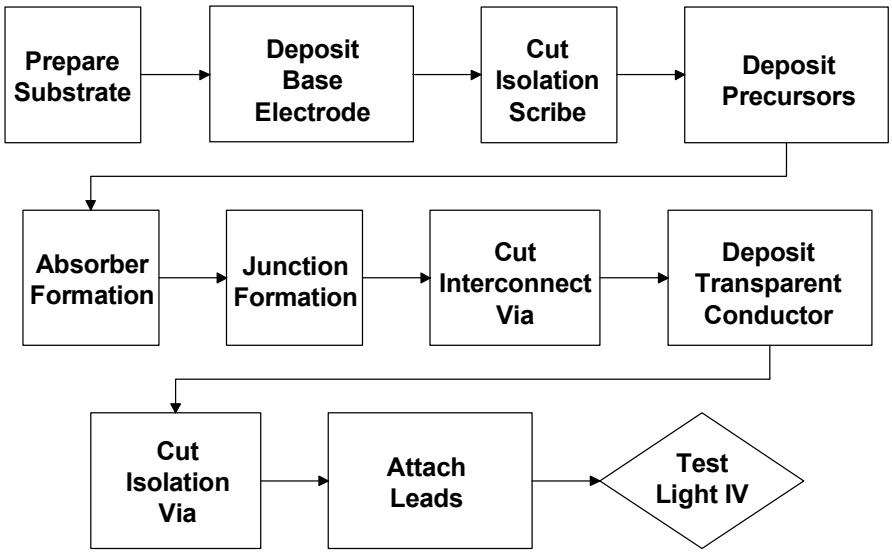


Figure 4. SSI CIS Circuit Processing Sequence.

This process starts with ordinary sodalime window glass. An SiO_2 barrier layer is deposited to minimize sodium diffusion from the substrate and thereby improve adhesion between the CIS

and the molybdenum (Mo) base electrode, which avoids dead areas at pinholes and at the patterns in the Mo. The Mo base electrode is sputtered onto the substrate. This is followed by the first patterning step (referred to as "P1") required to create monolithically integrated circuit plates – laser scribing to cut an isolation scribe in the Mo electrode.

Good P1 patternability can be judged from optical micrographs and profilometry (Dektak). Poor quality scribes have a characteristic ragged, partially debonded, and lifted edge. The lifted edge is revealed in Dektak traces as a spike at the scribe edge, which can cause shunts between ZnO and Mo. Adequate patternability and electrical performance was initially obtained by using a molybdenum bi-layer structure consisting of a thin first layer deposited at low pressure followed by a "bulk" layer deposited at higher pressure, e.g. in a 1:10 thickness ratio at 3x10-3 and 13x10-3 mbar respectively. While scribe quality is influenced by laser set-up, molybdenum properties dominate scribe quality, particularly lifting at the edges, and consistency of this process was problematic. This cumbersome dual pressure process was replaced by a multi-target process at a single pressure (13x10-3 mbar) in which the first thin layer was deposited through a honeycomb-form screen, or collimator, to force the molybdenum atom flux into a more normal angle of incidence [***9***]. Deposition system and process influences were identified and process development lead to improved consistency while transferring the process to higher volume production equipment. Pattern quality was controlled by addition of a small amount of water or oxygen to the argon sputter gas (in the range 2-15%) during deposition of the first, thin layer.

Copper, gallium and indium precursors to CIS formation are then deposited by sputtering. Deposition of the precursors occurs sequentially from two targets in an in-line sputtering system, first from a copper-gallium alloy target (15 at% Ga) and then from a pure indium target. Sodium is introduced by a "sputter dose" process in which a compound containing sodium is sputtered on the Mo base electrodes prior to deposition of the copper-gallium and indium. Process feedback is provided by a combination of measurements using quartz crystals and XRF. For each precursor deposition campaign, quartz crystals on a glass carrier are run through the sputtering system twice, the first pass for deposition of the copper-gallium film, and the second for deposition of the indium film. The thickness of each layer is determined based on crystal resonant frequency differences before and after the depositions. XRF measurements are used to measure the consistency of precursor deposition throughout a precursor deposition campaign.

As seen in the following photograph of a reactor for 1x4-foot circuit plates, Figure 5, a group of substrates is loaded in a carrier, placed into the tube reactor, and processed as a batch. CIS formation is accomplished by sequentially heating the precursors in H_2Se and H_2S to form the CIS absorber. This deposition of copper and indium precursors followed by reaction to form CIS is often referred to as the two-stage process. Beginning at room temperature, furnace temperature was ramped to around 400ºC for selenization via H_2Se, ramped again to around 500ºC for subsequent sulfidation via H_2S and followed by cool-down to room temperature. The concentration and uniformity of sodium across the substrates is controlled using the sputter dose process to supply sodium, using the SiO_2 barrier layer to minimize sodium diffusion directly from the substrate and by facing absorber layers toward one another to minimize the contribution of sodium transported through the reactor by sodium selenide from the uncoated side of adjacent substrates [***9***].

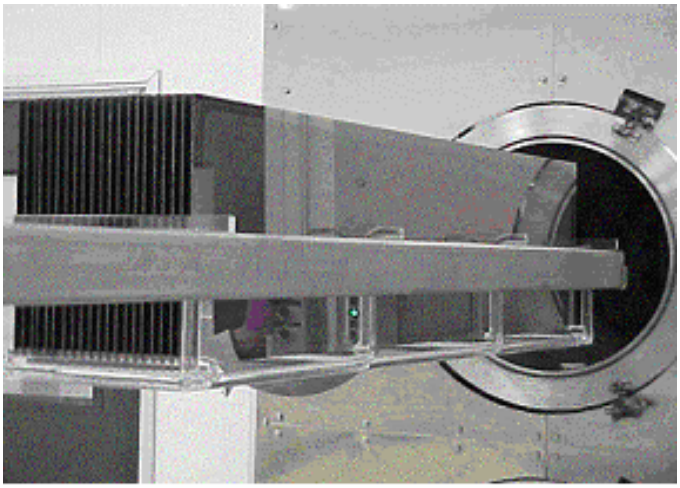


Figure 5. Photograph of 1x4-ft circuits in front of absorber formation reactor.

A very thin coating of cadmium sulfide (CdS) is deposited by chemical bath deposition (CBD). This layer is often referred to as a "buffer" layer. Good devices but with strong "transients" (changes in power with light soaking) were demonstrated for the same overall structure but without the CdS layer. A second patterning step (P2) is performed by mechanical scribing through the CIS absorber to the Mo substrate thereby forming an interconnect via. A transparent contact is added by chemical vapor deposition (CVD) of zinc oxide (ZnO), simultaneously depositing on the exposed part of the Mo substrate in the interconnect via and thereby connecting the Mo and ZnO electrodes of adjacent cells. A third and final patterning step (P3) is performed by mechanical scribing through the ZnO and CIS absorber to isolate adjacent cells.

The CIS-based absorber referred to in this report is composed of the ternary compound $CuInSe_2$ combined with sulfur and gallium to form the multinary compound $Cu(In,Ga)(S,Se)_2$. Gallium and sulfur are not uniformly distributed throughout the absorber but the concentrations are graded; hence, this structure is referred to as a "graded absorber." The graded absorber structure is a graded $Cu(In,Ga)(Se,S)_2$ multinary with higher sulfur concentration at the front and back and higher gallium concentration at the back. Elemental profiles typical of the SSI graded absorber structures are presented in Figure 6. Efficiency, voltage, and adhesion improvements have been demonstrated for the SSI graded absorber structure [***10***, ***11***].

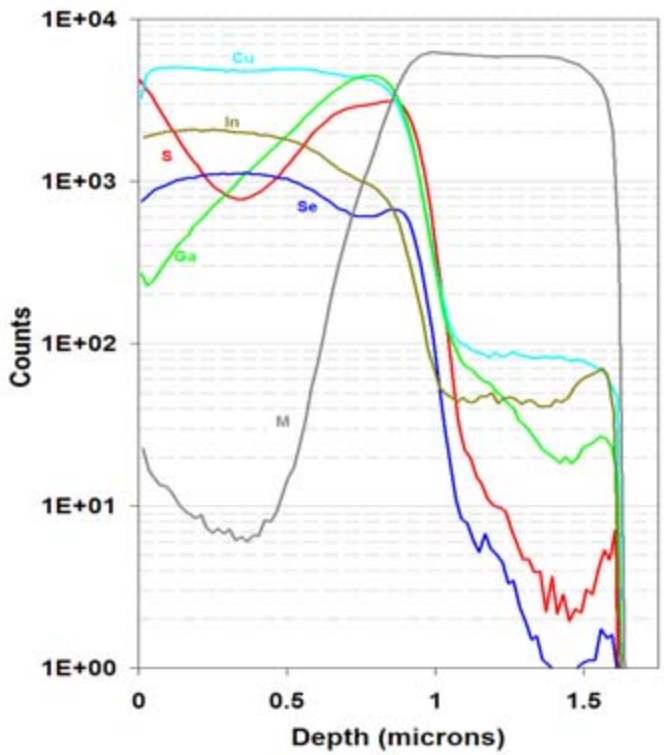


Figure 6. Typical elemental profile for the SSI graded absorber (SIMS from NREL).

Figure 7 illustrates the module configuration used for prototypes and products during this subcontract. EVA is used to laminate circuit plates to a tempered cover glass and a Tedlar/polyester/Al/Tedlar (TPAT) backsheet provides a hermetic seal. Aluminum extrusions are used to build frames for the modules. In addition to providing a hermetic seal, the combination of the TPAT backsheet and the offset between the circuit plate and the frame provides electrical isolation from the frame.

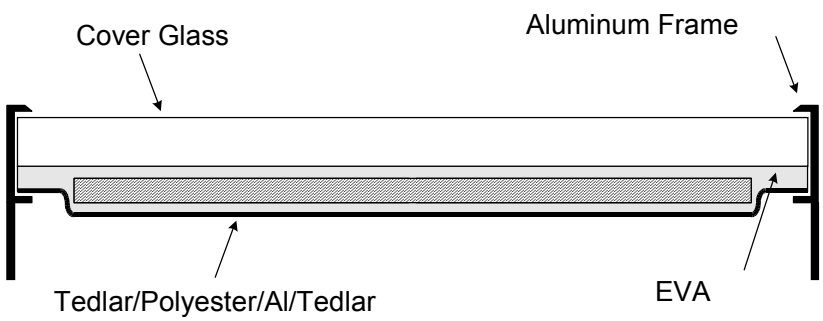


Figure 7. Single circuit plate module configuration with a TPAT backsheet.

The SSI CIS processing facility produces nominally 1x4 ft. circuit plates for production and process R&D. Full size 1x4 ft. circuit plates are used for ST40, 40W product. Smaller modules in the ST series of products are cut from identical circuit plates; processing through all CIS device fabrication and monolithic integration process steps is the same for full size 1x4 ft. and smaller modules.

Most production infrastructure, with the exception of absorber formation reactors, is compatible with larger circuit plates - up to nominally 2x5 ft. Overall capacity increases could be achieved by increasing the substrate size; however, higher power products are now fabricated using multiple circuit plates rather than larger circuit plates; prototype modules using two 1x4 ft. circuit plates were tested and the approach adopted for a new product – the "Eclipse 80-C".

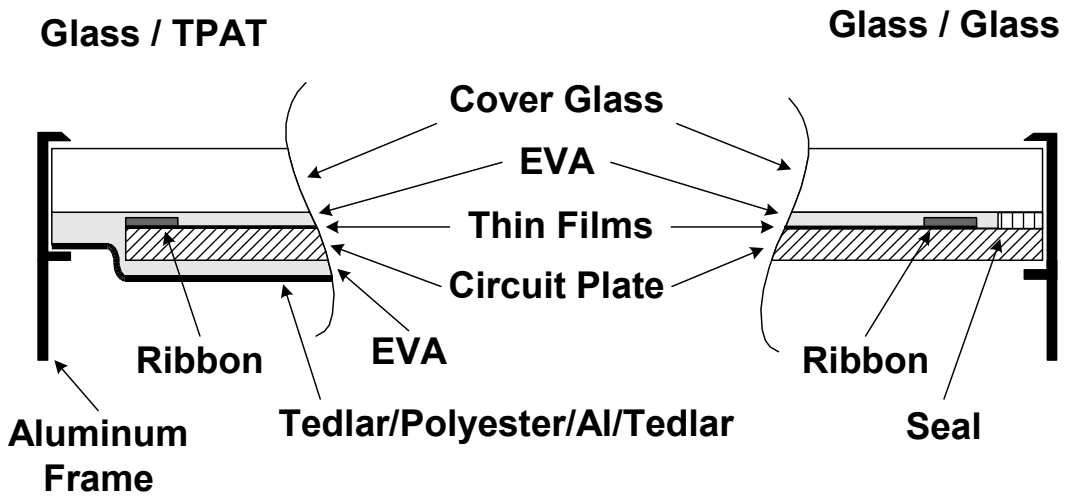


Figure 8. "TPAT" backsheet and "glass/glass" package designs.

The Eclipse 80-C was the outgrowth of "glass/glass" package designs primarily to decrease packaging costs. Simplification of the package and decreased operating temperature were additional potential advantages. Figure 8 is a sketch comparing ST40 and "glass/glass" package designs. Figure 9 is a sketch of the Eclipse 80-C glass/glass package, which was designed for cost reduction and marketability. Two nominally 40W circuit plates are laminated to a common tempered glass front sheet. Laser edge deletion to remove all of the thin films forms an approximately 1 cm border and provides electrical isolation from the frame. An edge seal selected in collaboration with the NREL sponsored National Thin-Film PV Module Reliability Team (TFMRT) is used at the perimeter of both plates [*12*]. A screen in front of the ribbons is included to achieve an aesthetically pleasing uniform black appearance.

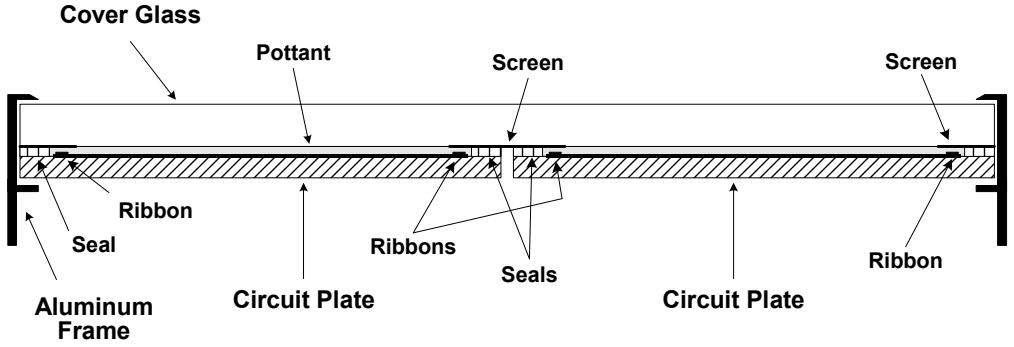


Figure 9. Proposed Eclipse 80-C glass/glass package.

Elimination of the TPAT backsheet for the glass/glass package was planned in combination with polishing off contaminates on the back of the circuit plate. However, a back cleaning system purchased for this task proved unable to remove all traces of contamination of the back side of the glass. An alternative plan using a low-cost Tedlar backsheet and a lower cost adhesive was implemented (Figure 10). Long-term options and initial subcontract work include sealing the back of the circuit plate with a low cost coating applied during or after lamination or eliminating the CdS.

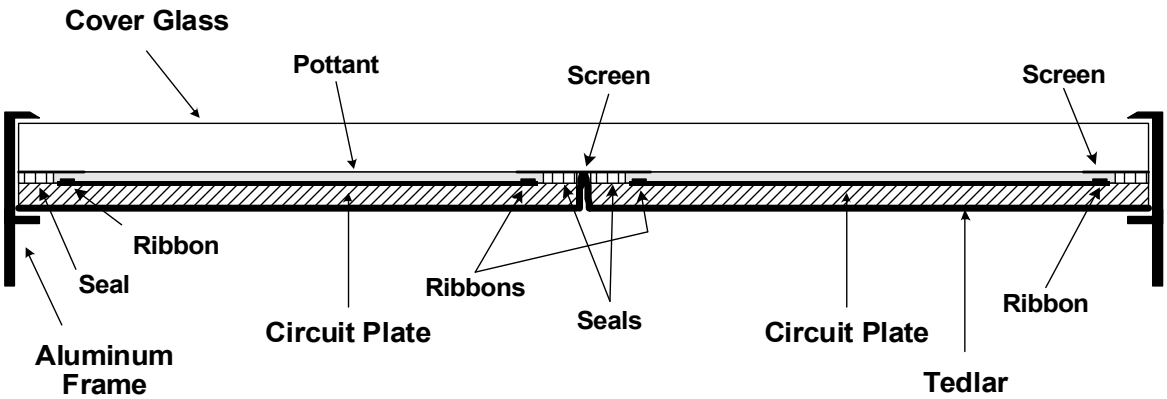


Figure 10. Eclipse 80-C glass/glass package.

Figure 11 illustrates the layout of the circuit plates, buss bar ribbons and a printed circuit board (PCB) that connects the circuit plates and routes power to a junction box on the back of the module. A black screen printed aperture on the cover glass covers the ribbons, the film-deleted edge and the the edge seal, to achieve an aesthetically pleasing uniform black appearance, as shown in Figure 12.

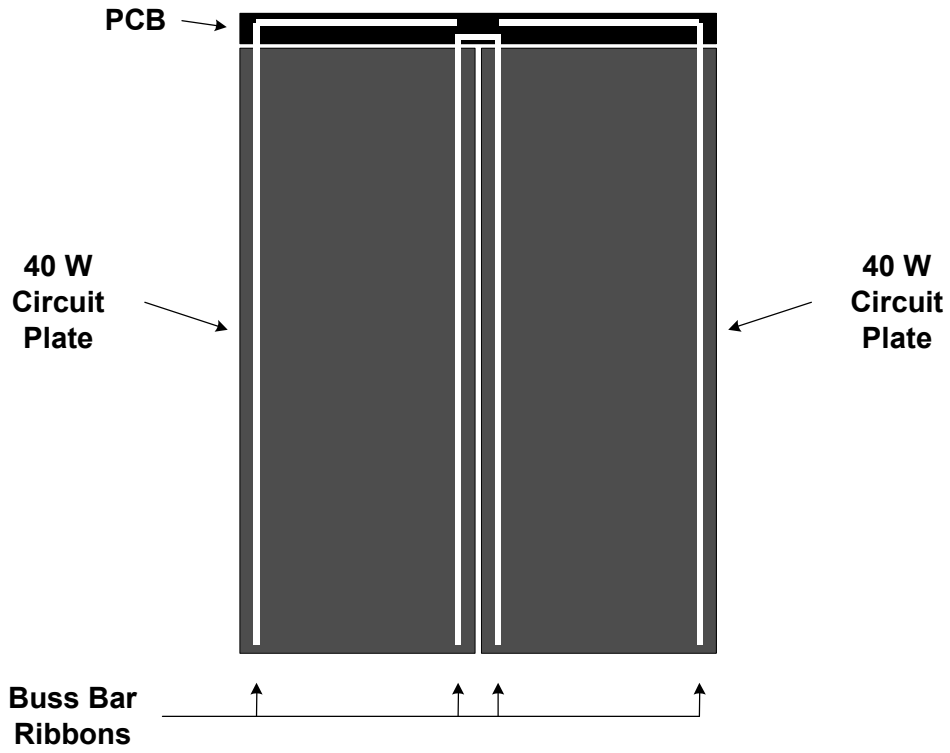


Figure 11. Lay-up of two circuit plates.

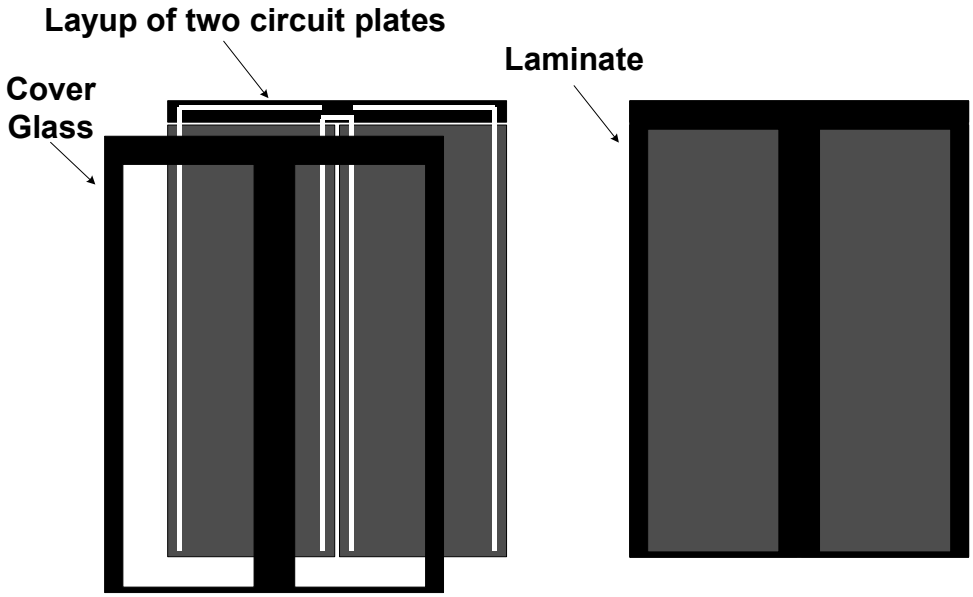


Figure 12. A cover glass with screen achieves an uniform black appearance.

SSI R&D Approach

From the industrial perspective, the full process sequence anticipated for use in large-scale production must be mastered and rigorously demonstrated. The SSI research approach is composed of two main elements:

- Experimentation and development using structures that exercise all aspects of large area module production [***13***]
- Application of statistical process control (SPC) as the discipline to rigorously quantify process reproducibility, and application of statistical methods such as analysis of variation (ANOVA) to rigorously quantify experimental results [***14***, ***15***].

Process predictability is a prerequisite for commercialization of thin-film PV since product performance ratings, yields and costs must be known before committing to produce products. Also, process predictability is essential for proper interpretation of process development efforts since experimental results may be ambiguous or misleading if compared to an unpredictable baseline process. SSI has adopted SPC methodologies because SPC was developed to rigorously quantify process reproducibility and process capability; the essence of SPC is predictability. Equally significantly, SPC provides the measure of systematic progress as processes are developed. Communication of this progress is typically best expressed in the language of the SPC discipline [***16***]. For example, process characterization results are demonstrated to be "statistically significant" based on knowledge of process repeatability as measured using the SPC discipline and compared to a predictable baseline process. Confidence in the appropriate interpretation of experimental results is gained through application of statistical methods such as ANOVA to demonstrate statistically significant results.

Subcontract Activities and Milestones

Background

NREL supports thin-film R&D and National R&D Team activities with team members from academia, the thin-film photovoltaic (PV) industry, NREL, the National Center for Photovoltaics (NCPV), and the Center of Excellence for Thin Film Photovoltaics at the Institute of Energy Conversion, University of Delaware. The purpose of the Thin-Film Photovoltaics Partnerships Program (TFPPP) is to accelerate the progress of thin film solar cell and module development as well as to address mid- and long-term research and development issues. The long-term objective of the TFPPP is to demonstrate commercial, low-cost, reproducible, high yield and robust PV modules of 15% aperture-area efficiency, about $50/m2 area cost, and thirty-year lifetimes. These goals are stated explicitly for thin films in the US DOE Solar Energy Technology Program's "Multi-Year Technical Plan (MYTP), 2003-2007 and Beyond" (Table 4.1.1-1, page 50). They are consistent with reaching the DOE long-term goal (2020) of cost-effective PV electricity at about 6 cents/kWh levelized energy cost. The purpose of this subcontract effort, in the Technology Partners Category, is to accelerate progress of thin film solar cells and module development as well as to address mid and long-term research and development issues by achieving aggressive interim goals for thin film module efficiencies; cell and module processing; cell and module reliability; and the technological base that supports these key areas. This subcontract was executed on October 3, 2005.

Objectives

The primary objectives of this subcontract effort are to:

- Address key near-term technical R&D issues for continued improvement in thin film PV products
- Continue process development for increased production capacity
- Pursue long term R&D contributing to progress toward the MYTP goals for 2020 to increase the conversion efficiency to 15% and reduce module manufacturing costs to less than $50/m2, thus enabling PV systems with a 30-year lifetime at an installed cost of under $2.00/W
- Advance the understanding of the requirements needed to achieve better thin-film PV cell and module performance, greater reliability and market acceptance, and investigate materials systems and new devices that can improve the cost/performance ratio of future thin-film PV factories

Goals

The primary goals of this subcontract effort are to:

- Meet the 2007 MYTP technical target of 12% module conversion efficiency for large area Copper Indium Diselenide (CIS) production modules
- Demonstrate progress toward development of a commercial, low-cost, reproducible, high yield and robust module process capable of meeting the MYTP goals for 2020 to increase the conversion efficiency to 15%
- Provide subcontract deliverables including CIS-based products and representative modules delivered to the NREL Module Testing Team for outdoor testing and evaluation
- Properly document progress for the thin film PV community

Technical Review

Production Review

Performance and Capacity

Outstanding progress has been made in the initial commercialization of high performance thin film CIS technology. During the previous subcontract, predictability of the SSI CIS process was demonstrated by continuously executing the process while increasing throughput. Cumulative production for 2002 exceeded 1 MW - about twice the production rate for 2001. Capacity in 2003 increased to somewhat below 3 MW per year and production for 2003 was just over 1.2 MW. Introducing a new minimodule product accounts for the main difference between production and capacity. As charted in Figure 13, the laminate efficiency distribution for 2003 peaked at 11.0% with a full width of only 11% of the average. This distribution is nominally the same as the distribution for 2002 but with an approximately 33% increase in large area laminate production volume.

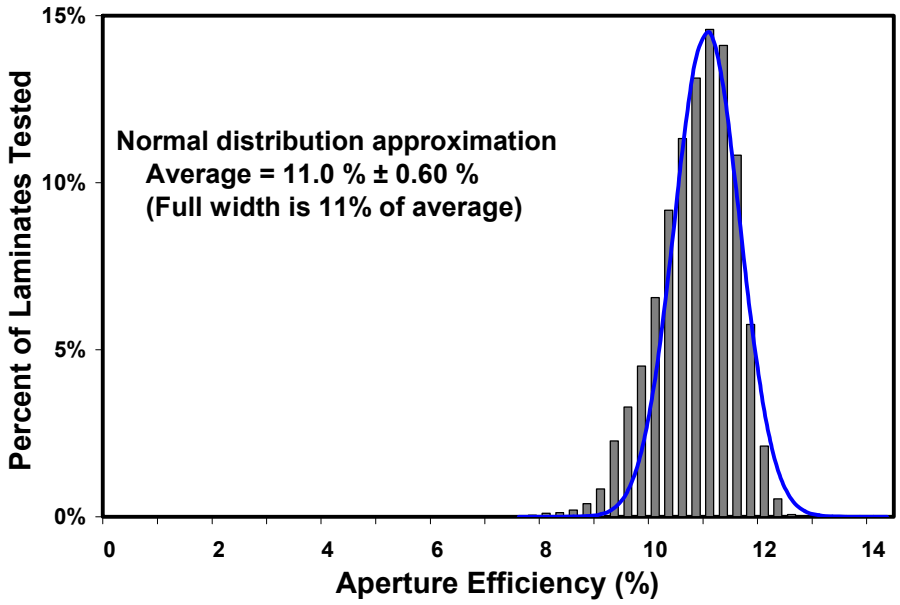
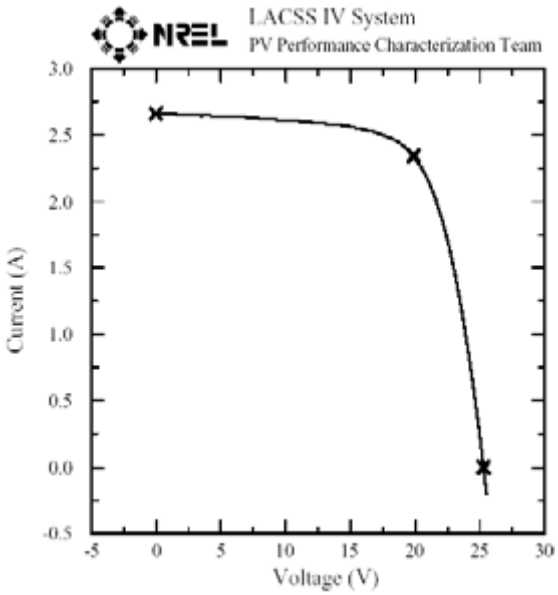


Figure 13. Production distribution for 1x4-ft. laminates produced during 2003.

During the previous subcontract NREL confirmed a champion 12.8 percent aperture area conversion efficiency for a large area (3626 cm^2) CIS module (Figure 14). The aperture area for this champion module was defined by taping off the approximately 1 cm inactive boarder surrounding the monolithically integrated CIS circuit in a ST40, 40W, production module. Other than definition of the aperture area, this module is simply one module from the upper end of the production distribution for standard modules. Similar modules made using the sputter dosed absorber formation process were submitted to NREL for measurement as champions and for later use as reference modules. Measurements for one of these modules on the NREL Large Area

Constant Source Simulator (LACSS) were within 2% of the NREL measurements of the previous champion.



	Module	per Cell	
Eff	12.8		%
Pmax	46.5		W
Voc	25.3	0.601	V
Isc	2.7		A
Jsc		30.8	mA/cm^2
FF	69.2		%
Area*	3626	86.3	cm^2
Cells	42		

* Aperture area - including interconnect loss

Figure 14. Champion ST40 module from the upper end of the production distribution.

The DOE "Solar Energy Technologies Program, Multi-Year Technical Plan 2003-2007 and Beyond" (MYTP) defines technical targets for specific PV technologies that are deemed necessary to achieve national significance for PV industries [*17*]. A progression of targets are defined for assumed "baseline systems" that are deployment scenarios developed for 2020 goals. The 2003 MYTP technical target for the baseline system incorporating thin-film modules is 8% average module conversion efficiency (Table 4.1.1-1). The distribution data in Figure 13 demonstrates that at least a year in advance, with production modules rather than champion modules, SSI accomplishments far exceed the 2003 DOE EERE Multi-Year Technical Plan technical target of 8% module conversion efficiency for thin-film modules. The following quote from the EERE Multi-Year Technical Plan (MYTP) recognizes previous SSI accomplishment, "After two decades of R&D, CIS is being introduced to the market, with prototype modules made by Shell Solar (Camarillo, CA) consistently reaching efficiencies greater than 11%—beating a goal set in the last PV Subprogram 5-year plan by more than a year."

Production during this subcontract period was initially the 40 W single circuit plate ST40 with the relatively new sputter dose process. This was followed by production of the 80 W Eclipse 80-C glass/glass package made using two nominally 40W circuit plates laminated to a common tempered glass front sheet. Figure 15 is the module distribution for 10,947 ST40 modules produced between February 2005 and August 2005. The peak of the distribution for these ST40 modules is 11.25% with a mean efficiency of 11.1%. The standard deviation of the distribution is less than 1% (corresponding to only 8.6% of the mean).

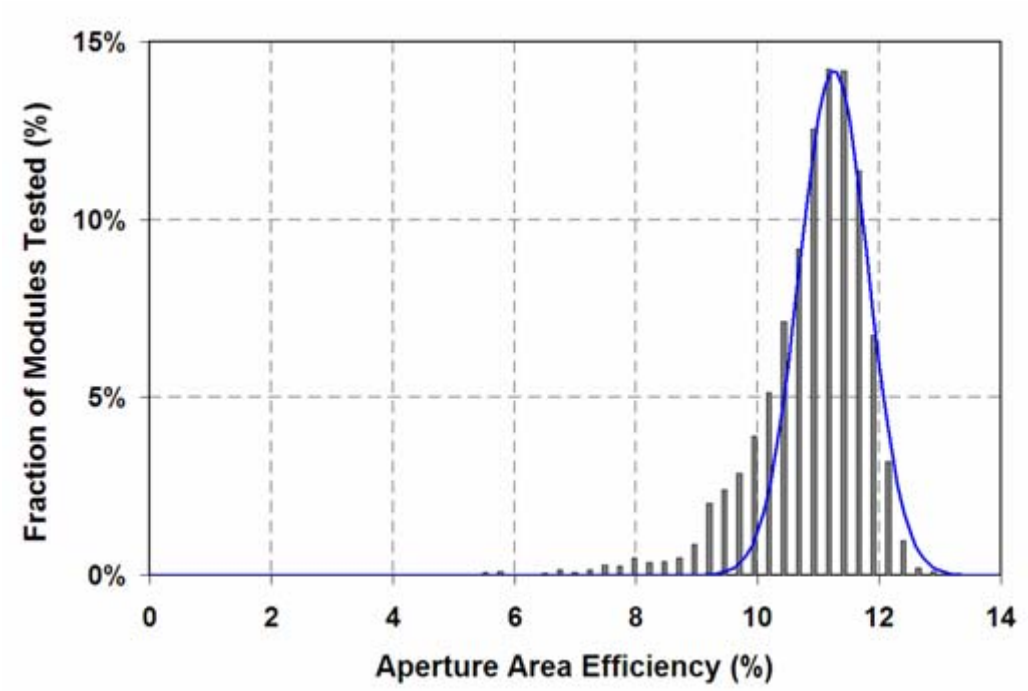


Figure 15. Efficiency distribution of all ST40 modules produced in 2005.

The distribution for 9,011 Eclipse 80-C modules is charted in Figure 16. The peak of the distribution for these Eclipse 80-C modules is 11.0% with a mean efficiency of 10.8%. The standard deviation of the distribution is less than 1% (corresponding to only 7% of the mean).

The lower efficiency for the Eclipse 80-C distribution is in part due to decreasing the absorber sulfur content to decrease transients and thereby, as discussed in more detail below, pass the IEC 61646 certification standard.

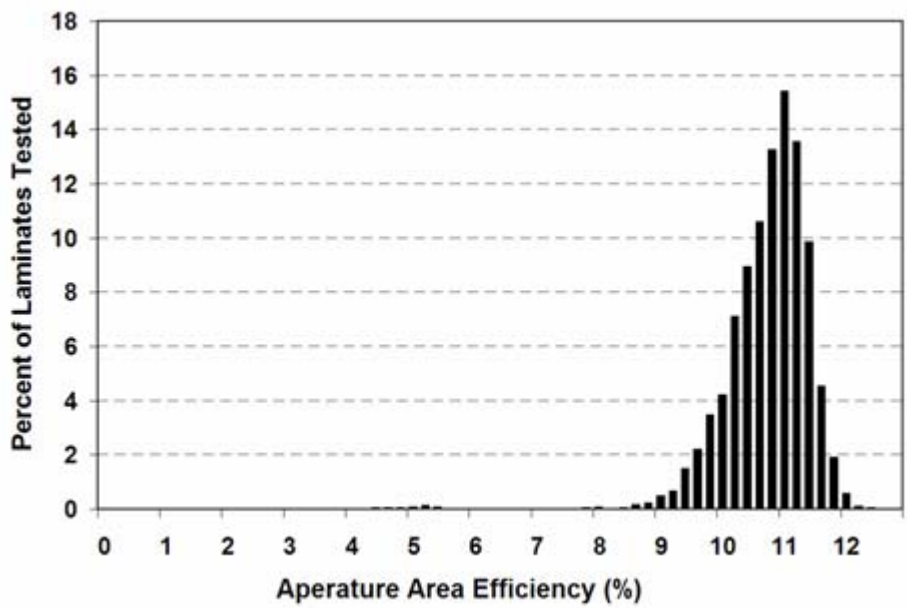


Figure 16. Efficiency distribution of all Eclipse 80-C modules produced in 2005-2006.

Line yield is defined as the ratio of two areas – the area of product produced divided by the area of glass started through the production line, average over time. This is a total yield including both electrical yield and mechanical yield through all processing required to produce products. Figure 17 illustrates yield improvements over approximately the last five years. Yield data from 1999 through 2003, through the beginning of minimodule production, is plotted on a monthly basis. Line yield increased from about 60% in 2000 to about 85% in 2002 and high yields were demonstrated throughout 2003. These dramatic yield improvements were due to continuous improvement of all processes and this major accomplishment supports attractive cost projections for CIS.

Yield since restarting large area module production late in 2004 (after a campaign of minimodule production) has been tracked for each product in the ST product line rather than based on total area for all products. Also, yield is posted weekly rather than monthly which inherently introduces more variability in the statistics. Another difference between yield data for previous and the present baseline with the sputter does process is that aesthetic criteria have become more stringent. Yield has been good but variable. Estimates for total area yield made to be more consistent with earlier data, but still on a weekly basis, are plotted in Figure 17 for the last quarter of 2004 and the first quarter of 2005. Weekly total area yield ranges from about 60% to about 90%. This variability is expected for increasing capacity, introducing a new product, restaffing and retraining. Implementation of the sputter dose process also introduced variability as process parameter updates were made based on R&D to decrease transients and data from the first production scale experience.

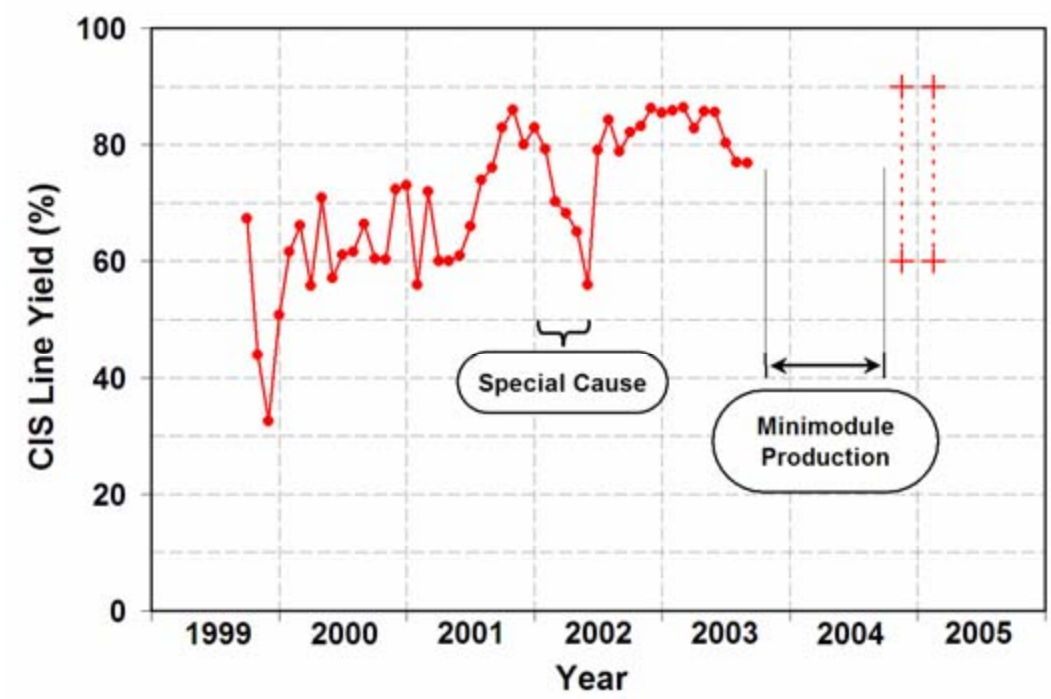


Figure 17. Yield improvements.

Total line yield for the Eclipse 80-C production was not tracked on an area basis. Eclipse-75C, Eclipse 80-C, and Eclipse-85C modules were produced and with changes throughout this subcontract period in the designated cutoff efficiencies and product mix. Combined with process changes, these issues make it impossible to directly compare yield for the multiple Eclipse 80-C product line with the previously used area based yield. Also, restaffing and retraining occurred twice during this production period. However, electrical yield based on production data for all timeframes and the cutoff efficiency used at the end of the subcontract for two rather than three product designations is presented in Table 1.

Table 1. Electrical yield by product

Model	Number of Modules	Yield	Average Power (W)
Eclipse-85C	4175	46.3	82.5
Eclipse-75C	4462	49.5	76.5
Total	9011	95.8	

Electrical yield for the product line exceeded 95%.

Process Development

The Approach to Manufacturing — a Retrospective

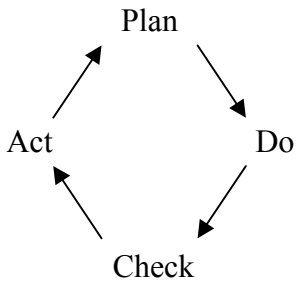
Manufacturing thin-film PV modules requires reproducible good results, on large areas and volumes, day-in, day-out. This is the ultimate goal of every thin-film PV R&D program, but the path is difficult from the first interesting research results — usually good efficiencies on small area solar cells — to megawatt-scale manufacturing. This section reflects on the method and philosophy employed at SSI to guide this transition.

The method does not dwell on performance of "champions". Champions often utilize special processing that is not practical for production or special processing or structures that are completely incompatible with the requirements for a real product. While champion performance is exciting, it demonstrates only that a certain combination of materials in a certain device structure can produce that exceptional level of performance. This is an often-misunderstood point. Every process produces a distribution of results. A champion result is by definition an exception, an outcome at the extreme positive end of the statistical distribution of outcomes when the process is repeatedly performed. A champion most certainly does not demonstrate that the process employed can routinely deliver that level of performance.

The method is not based on hope. Often new approaches are proposed because a particular processing technology promises low cost (e.g. high throughput, non-vacuum, novel, etc.) with the presumption that "we'll develop a process". Without the prior solid foundation of reproducibly good results, one is left with hope for scale-up.

First, research should concentrate on reproducibility with an adequate level of performance; only when this is demonstrated is there a basis for scaling-up a process. At SSI this began by focussing efforts on a single test device format, the 10x10cm^2 monolithically integrated "minimodule". These small circuits contained all of the elements whose mastery was necessary

for large-area production. Early on the circuit design was frozen — most importantly the cell width — guided by simple modeling for minimization of the geometric and ohmic power losses incurred when constructing an integrated circuit. Next, the circuit fabrication process was thoroughly documented and likewise frozen — all process changes were avoided unless deliberately targeted by an experiment. Adopting this orientation is particularly difficult for an R&D group, essentially the motto: "Don't just do something, stand there"! It was nevertheless essential to enable focus on finding and understanding sources of variation in process outcome. Tools such as statistical process control (SPC) and analysis of variation (ANOVA) were especially powerful in this context [***14***]. Once understood, a source of variation could be eliminated, or sometimes exploited if it led to a reproducible improvement. Moreover, by minimizing variation in process outcome, it was easier to validate that a process change actually resulted in a statistically significant, reproducible improvement. This systematic approach of gathering statistically meaningful data and acting accordingly is often summarized in the cycle:



Work toward area scale-up can sensibly commence when the small area research process has reached the acceptable level of reproducibility and performance. The guiding principle for this next step has two parts. First, characterize each process on a local level, along the lines of "if I am a small piece of CIG, or CIS, etc., what environment do I see or feel"? This means thoroughly characterizing the process conditions through measurement of substrate temperature, process gas concentrations, sputter deposition rates, voltages, etc. This knowledge forms the foundation for specification of production processing machines, the second part of the effort.

Processing machines must be designed which can replicate those conditions uniformly on a sufficiently large area. Often this can be accomplished by copying the design principles of small processing equipment into a larger format. For example, large area reactive annealing furnaces (for selenization-sulfurization) were built around large diameter quartz tubes fashioned after the small diameter quartz tube furnaces used for research processing. Likewise, equipment for CVD of ZnO was scaled in a straightforward way from the small research CVD reactors. In other cases, the processing "tool" (laser or mechanical scribe tip fixture) remains the same but the "travel" built into the processing machine is increased to accommodate larger dimensions.

It is also very important to employ a rigorous machine specification, design, and procurement process. Here participation from both the research engineer and the future production personnel is essential—it's not sufficient to delegate the task to a project engineer who, on completion of the project, will then "toss it over the wall" to manufacturing. Instead, it is vital to incorporate several stages of review and acceptance into the procurement process, most especially after completion of the detailed design before actual construction begins. Finally, a rigorous system for release of new equipment to production ensures that new machines are usable and sustainable

as well as functional. A process qualification plan verifies that the machine yields results that fulfill requirements, and provides a mechanism for trouble-shooting and improvement if this is not initially the case. Equipment release must also encompass safety requirements, manufacturing documentation, maintenance methods and software control, integration into information management systems.

Also note that first-of-a-kind equipment will inevitably suffer from design mistakes and that there will be lessons learned while evaluating new equipment in production. It is valuable to allow flexibility in procurement so that improvements can be incorporated into later versions of the equipment.

Manufacturing is also based on far more than just a process and a set of equipment; it requires a quality system in the broadest sense. This quality system must encompass the definition and release of both equipment and processes in the form of process procedures and work instructions. In addition it must define and release methods for machine preventative maintenance, for safe trouble-shooting and repair, for replenishment of process materials, and for calibration of gauges and instruments on the equipment. It must provide a system for controlling and implementing revisions to procedures and other documents. It must include a system for tracking flow of substrates through the production line (like the SSI SWIP system, a real-time production control system), ideally integrated with process history and product test databases. And finally, possibly most importantly, it must include a system for rigorous training of production and maintenance personnel, including refresher training and training of revisions.

CIG Ratio Control and Indium Target Development

The CIG ratio, Cu/(In+Ga), is a key parameter in production of high efficiency CIS devices. In two-stage processing of CIS semiconductors, where reactive annealing follows the sputter deposition of the metallic elements, this ratio is governed by careful control of target sputter rates. At SSI one indium and one copper-gallium [15at% Ga] alloy target were employed for in-line sputtering of the metallic elements.

In earlier work we described this problem, the measurement tools employed for deposition rate measurement, and showed how methods from statistical process control (SPC) can be used to maintain good control as target sputtering rate changes with target age [***18***]. Since that earlier work we have gained experience with the use of more than 20 copper-gallium targets and more than 50 indium targets.

Performance of Copper-Gallium Targets

As a general rule copper-gallium targets, typically provided by Heraeus Materials, exhibited very stable sputtering characteristics. For somewhat more than half of the targets, the sputtering rate did not change at all for the entire life of the target. This is a very convenient situation! For the remaining targets only slightly poorer characteristics were found, with the sputtering rate stable during the first half of target life and then drifting slowly but steadily lower toward the end of target life. However, the drift was sufficiently slow that over a 12-hour production shift even worst case drift produced only a negligible 0.6% decline in copper-gallium thickness

(corresponding to a mere 0.005 shift in CIG ratio). Moreover, downward drift causes the CIG ratio to trend slightly lower, i.e. in the "safe" direction. Obviously, there is some opportunity for further refinement through collaboration with the target vendor.

Consequently the copper-gallium sputter rate could in practice be checked once prior to a production run (with the sputtering power adjusted if necessary) and then the sputtering power left constant during the entire run. In fact, instances where the copper-gallium sputter rate was found outside specification limits were sufficiently rare that changing sputtering power was not allowed without investigation by engineering.

Performance of Indium Targets

Stability of indium targets was significantly more problematic. Early targets suffered from serious arcing and other variability. However, with further development of the target casting process by the vendor (Unaxis) improved targets were produced that gave good uniformity and, while exhibiting significant drift in sputter rate over the target's life, were at least reasonably consistent from one target to the next.

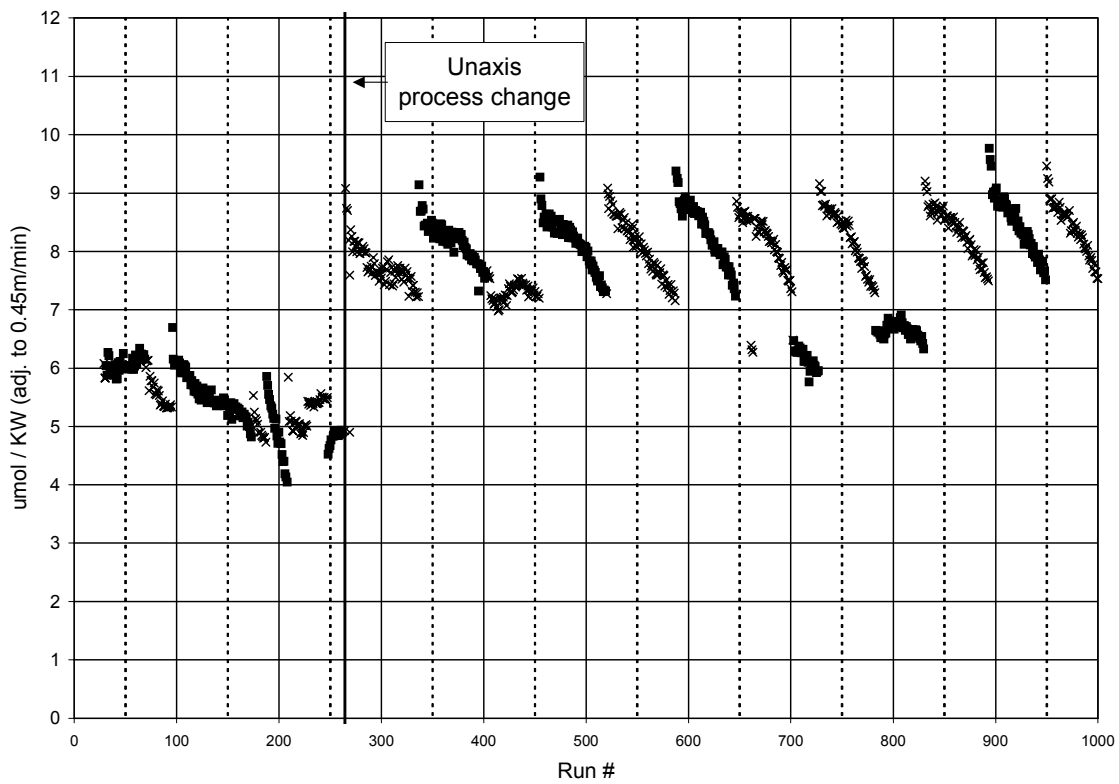


Figure 18. Sputter yield of early indium targets

Indium target performance during this early development is illustrated in Figure 18. Sputter yield is defined as the quantity of material deposited at a specified substrate transport speed (here, 0.45m/min) per KW of power applied to the sputtering target. (For historical reasons the quantity of material deposited is presented in μmoles of indium per 37.5cm^2). Each cluster, or stripe, of points corresponds to results from an individual target, with each data point in the

cluster being the yield measured for one run. In order to distinguish between the histories of successive targets, the symbol alternates between an "**x**" and a "■" with each new target.

Significant drift in sputter yield over the life of the target was characteristic of these indium targets, typically a drop of nearly 20%, from about 9µmol/KW to about 7µmol/KW as shown in Figure 18. This typical behavior is three times worse than the absolute worst cast observed for any copper-gallium target. As a consequence, the relatively poor stability necessitated correspondingly frequent measurements to control the sputter rate and, if necessary, to adjust the target power. This could cause significant operational inefficiencies, both in lost production time—as much as 1 hour out of 6—as well as indium target material spent during the control measurements.

The vendor Heraeus (reorganized from Unaxis) subsequently developed a modified casting process (later transferred to a second vendor, Thermal Conductive Bonding) that resulted in much improved stability of the sputter yield over the target lifetime. In Figure 19 it is immediately apparent that these new targets are typically much more stable over their life.

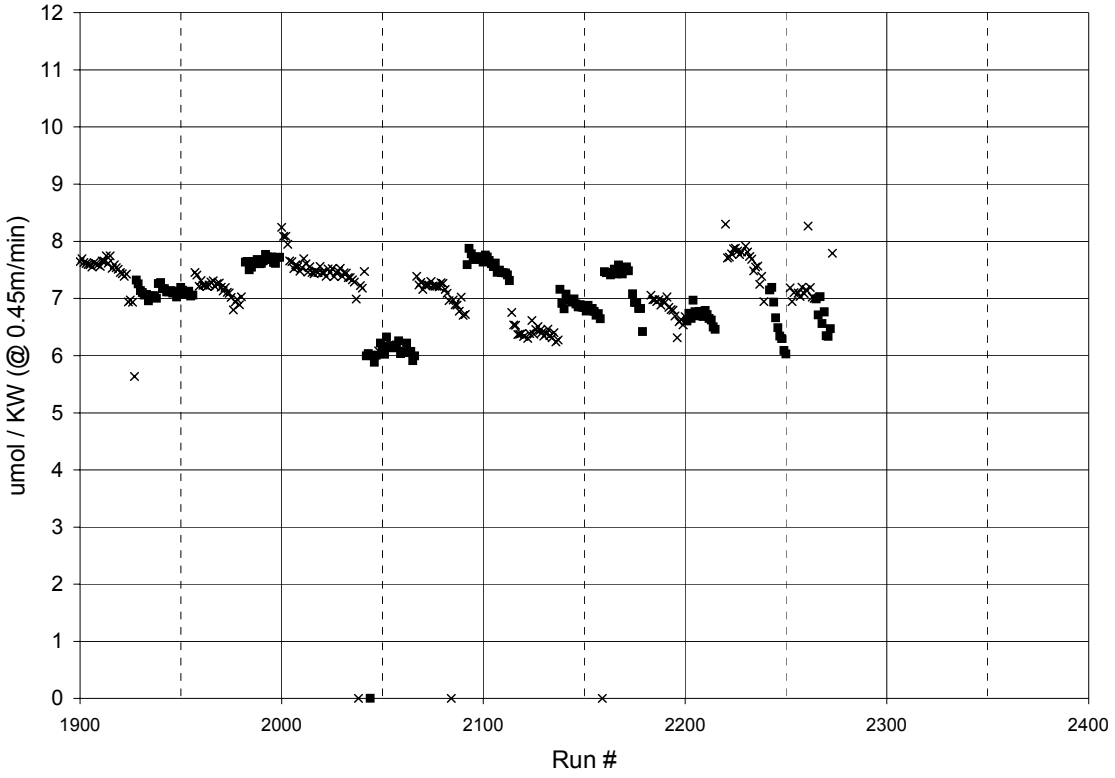


Figure 19. Sputter yield of improved indium targets

Several characteristics of these improved targets are revealed by closer inspection of the data used for Figure 19:

- Yield varies from target to target by as much as ± 10%, e.g. initial sputter power to achieve the aimpoint thickness is typically 10KW but can be as low as 9KW or as high as 11KW.
- Of the seventeen targets presented, about half exhibit constant yields over the full target life. However, the others exhibit decreasing yield with target age.

- Even the least stable TCB targets are about three times more stable than the typical Unaxis targets used in the earlier period.

The improved stability allowed a very significant reduction in production time lost in making control measurements.

Development to reduce indium target cost

In addition to working with vendors to improve the sputtering characteristics of the indium targets we also sought ways to reduce the cost of the target manufacture. To place this effort in context, first consider the standard method of target manufacture:

1. The customer returns a used target retaining 50-60% of the original indium in the backing plate to the vendor.
2. The vendor melts and removes the residual indium, crediting the customer for the indium but at a discount to full market price.
3. The vendor fills the backing plate with a full charge of fresh indium and casts the target.
4. The vendor machines away the top surface of the as-cast to produce a smooth surface and target to remove any surface layer impurities.

The simplest, lowest cost approach would be to eliminate steps 2 and 4, that is, simply refill a used target with the necessary weight of fresh indium and re-cast it. The target user would install the target as-is and begin the target burn-in from the unmachined as-cast surface. Would this work? Several potential drawbacks come to mind. The relatively irregular as-cast surface might cause unstable sputtering or arcing. Since the impurity distribution in the target is unaffected by machining, not machining off the surface may simply increase the duration of burn-in period. Repeated recasting could result in some concentration of copper impurity from the backing plate (though this might be reduced by nickel plating the backing plate).

In practice, positive results were obtained in intial trials. The first two as-cast targets performed exactly like conventional targets, exhibiting stable sputtering characteristics and yielding normal, high CIS modules. Somewhat surprisingly, the duration of new target burn-in (the time until the sputter yield has stabilized) was no longer for these targets than for conventional (machined) targets.

However, the next two as-cast targets gave poor uniformity on initial use and were removed without being used for production. The fifth as-cast target initially performed very well—like the initial pair—but after about 20% of its projected life the uniformity deteriorated and it too was removed. In fairness it must be noted that in this time period three conventional targets also had poor uniformity.

The problem of poor uniformity appears to originate in not yet understood variations in target casting conditions but is not obviously related to recasting. Can inhomogeneity in targets be detected? The erosion groove, or racetrack, etched into the target by the sputtering process—appeares to reveal variations in internal grain structure between different targets.

- For targets that gave good uniformity the indium in the racetrack was fairly consistent in appearance across the width of the target, not smooth, but with a sub-millimeter roughness or texture somewhat like medium grit (e.g. 120) sandpaper.

- In contrast, for targets that gave poor uniformity, the indium varied significantly in appearance from one end of the racetrack to the other. Typically showing much coarser structure than observed in a good target, the roughness or texture was on a sub-centimeter scale and somewhat reminiscent of the texture coatings sometimes applied to walls in "dry-wall" construction. Regions of coarser texture tended to give lower sputtering rates

Thus, non-uniformity correlated with the texture, or internal "grain" size revealed in the target raceway, presumably due to variation in target casting process. Solution of this problem will require more collaboration between vendor and target user.

Sodium and Sulfur Variations

Variations in the amount of Na introduced by the sputter dose process and S profile variations in the graded absorber were explored to potentially improved module efficiency and to reduce thermal transient behavior. Module performance and NREL provided SIMS analysis was considered for a matrix of two sputter dose levels (0.73 and 1.3 relative sputter dose) and three levels of H_2S concentration during sulfidation (100%, 33%, 10% relative to baseline). The results of this matrix are summarized as follows:

- Module efficiency increases smoothly from 11% to 12% with [H_2S] increasing from 10% to 100% - Voc increases faster than Jsc drops.
- Thermal transients generally decrease with increasing Na sputter dose and decreasing [H_2S] but with little difference between 10% and 33% H_2S.
- Efficiency is independent of sputter dose level except at 10% H_2S where the FF is better for the lower sputter dose level.
- Adhesion is excellent at the higher S levels and slightly poorer adhesion for 10% [H_2S].
- Adhesion is independent of Na sputter dose level.

For each variation, SIMS analysis included samples from the center and within the active area near the top edge (both from near the center relative to the long dimension). Data from the SIMS analysis is plotted in Figure 20 through Figure 23. SEM images are presented in Figure 24 through Figure 26. The following summarizes SIMS and SEM observations:

- Sulfur profiles are similar in shape (log scale) but shifted in concentration for the three [H2S] conditions.
- Sodium sputter dose conditions have little effect on the sulfur concentration in the front and center of the absorber but do have some impact the profiles at the back.
- A large, highly variable increase in the Na concentration is observed in the Mo for some edge samples that may be related to Na transported through the reactor or roughness and SiO_2 area or step coverage.
- Increasing Na levels and implementing the sputter dose process minimizes the "fine grain region" and increases the "grain" size.
- SEM and SIMS data indicate that the improvement in transient effects by adopting the sputter dose process may be related to improvements in absorber structure - minimization of the "fine grain region" and increasing the "grain" size.
- The Na content in the absorbers did not change dramatically with sputter dose process or [H_2S]; the Na levels near the CIS/Mo interface and through the high Ga region are not

significantly different and differences in Na levels near the front are relatively small but might be important or be a remnant indicative of reaction pathway.

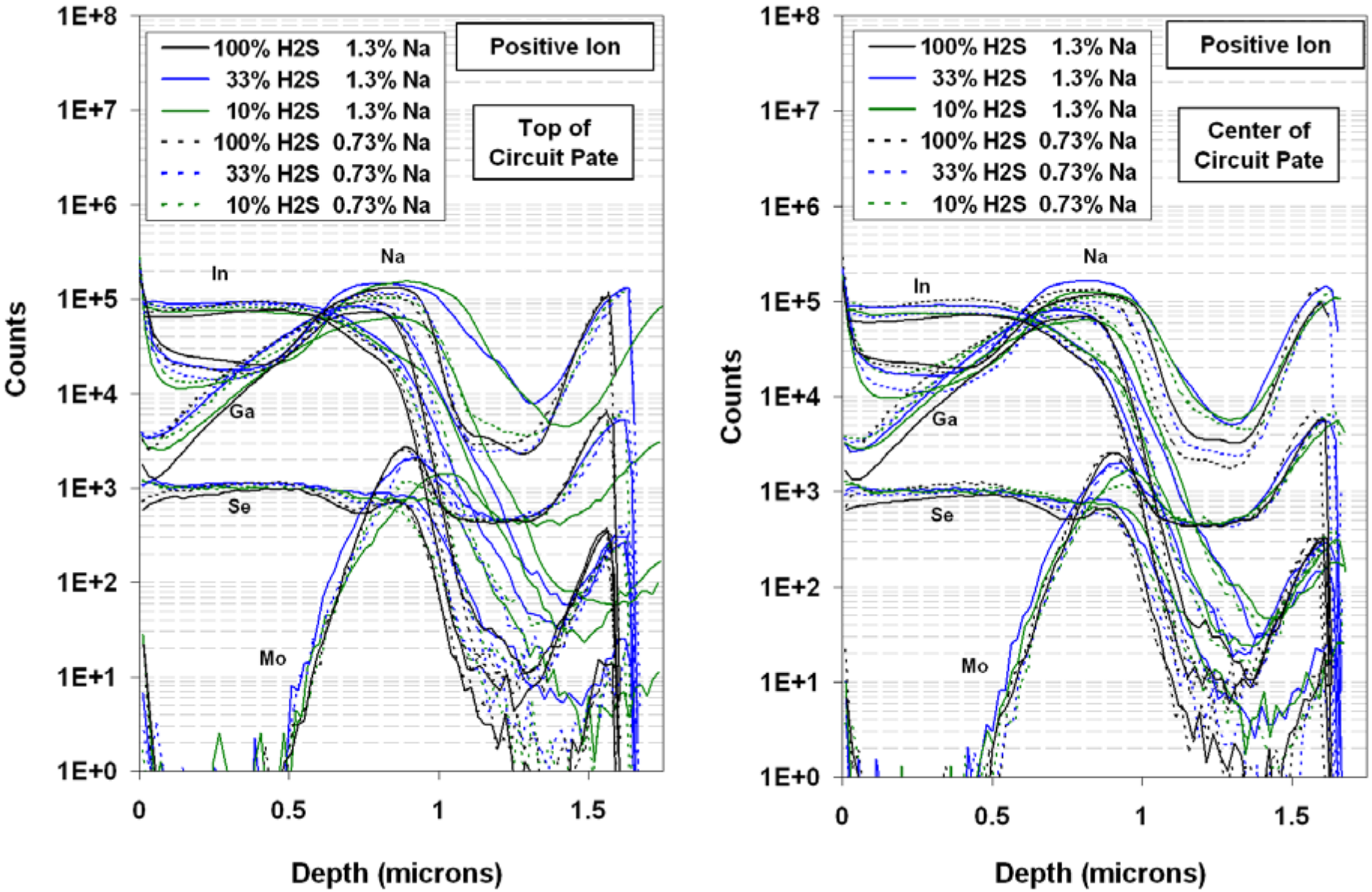


Figure 20. Positive ion SIMS profiles - top and center, all elements.

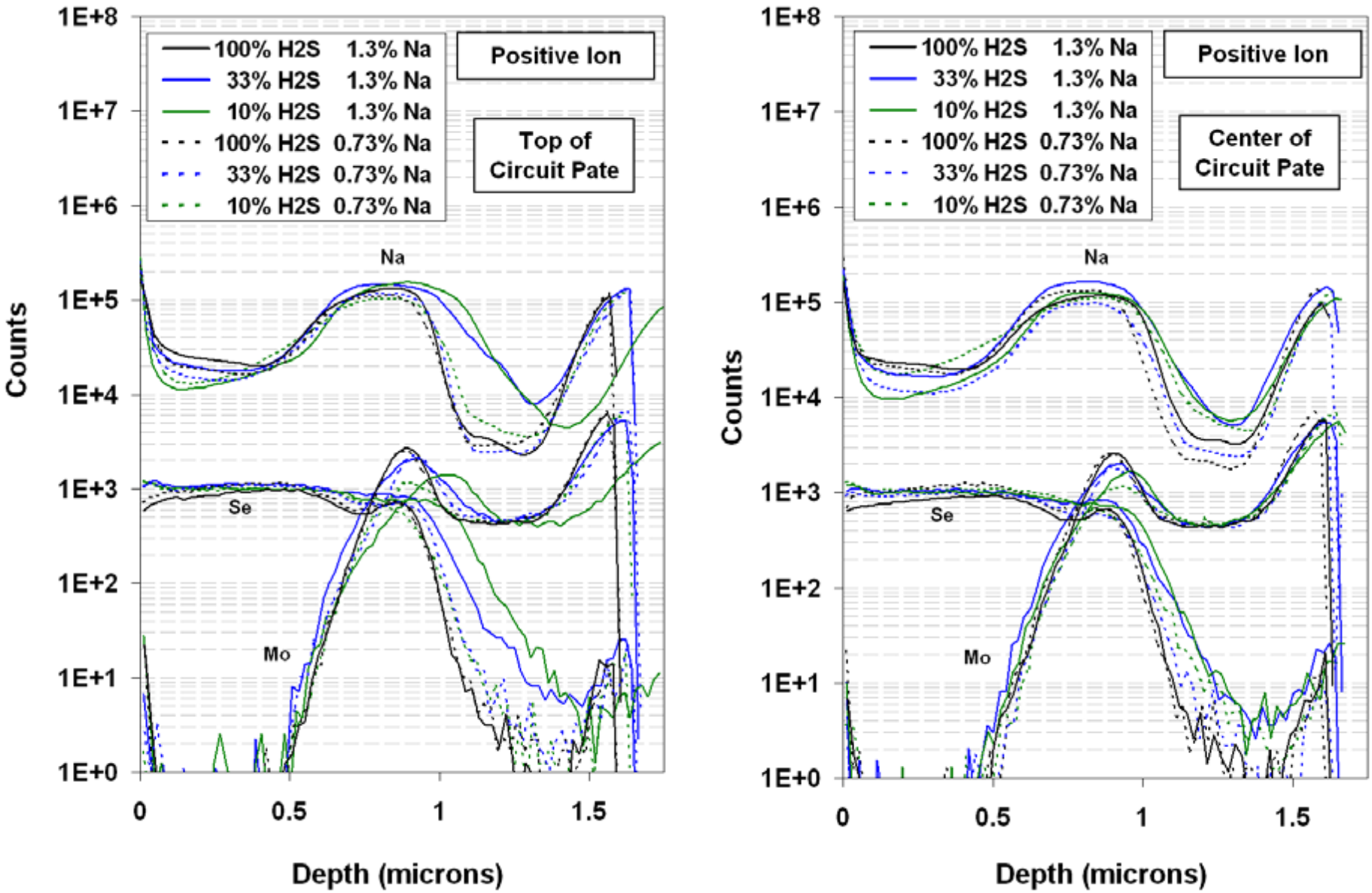


Figure 21. Positive ion SIMS profiles - top and center, emphasizing Na.

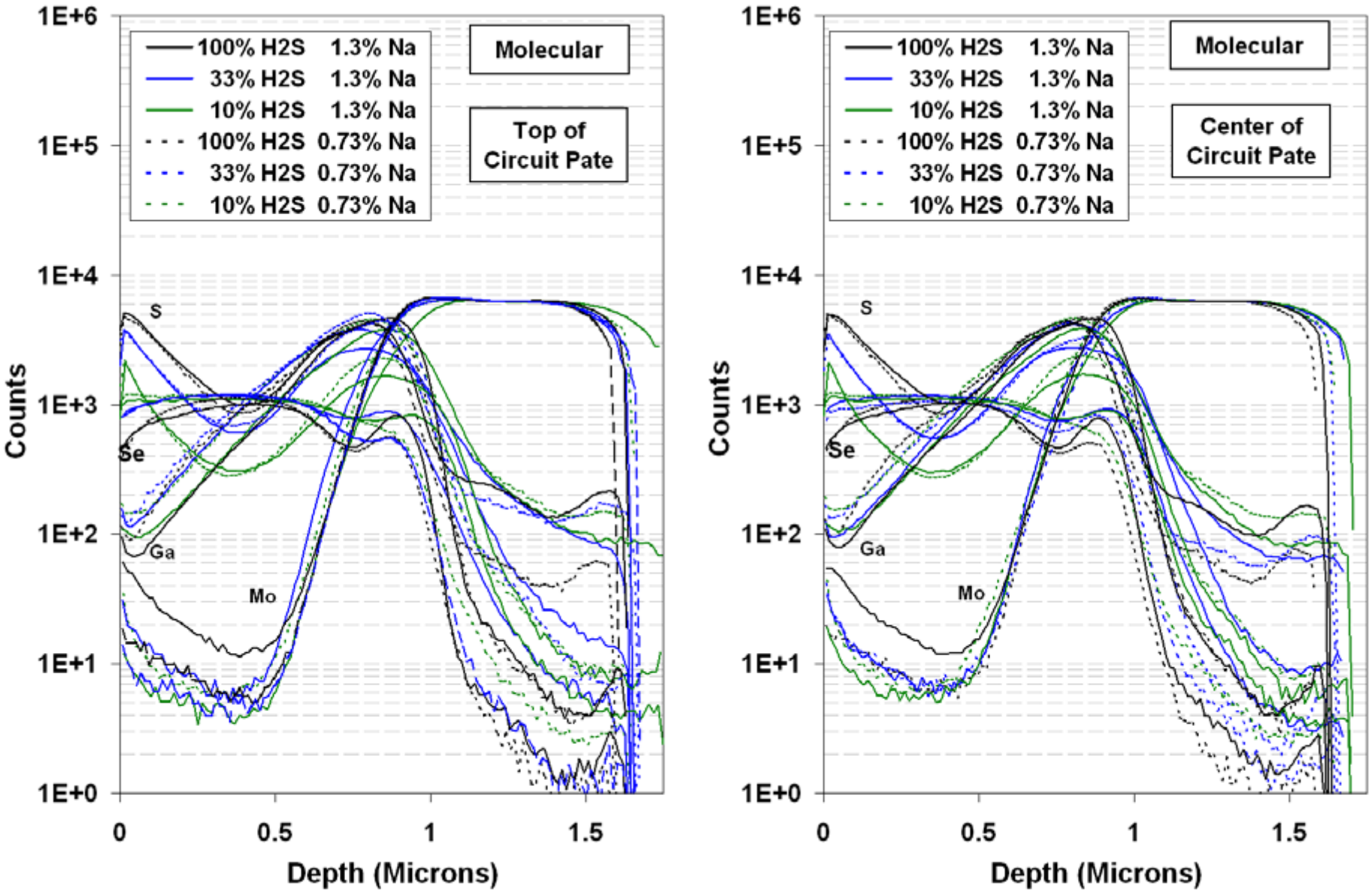


Figure 22. Molecular SIMS profiles – top and center.

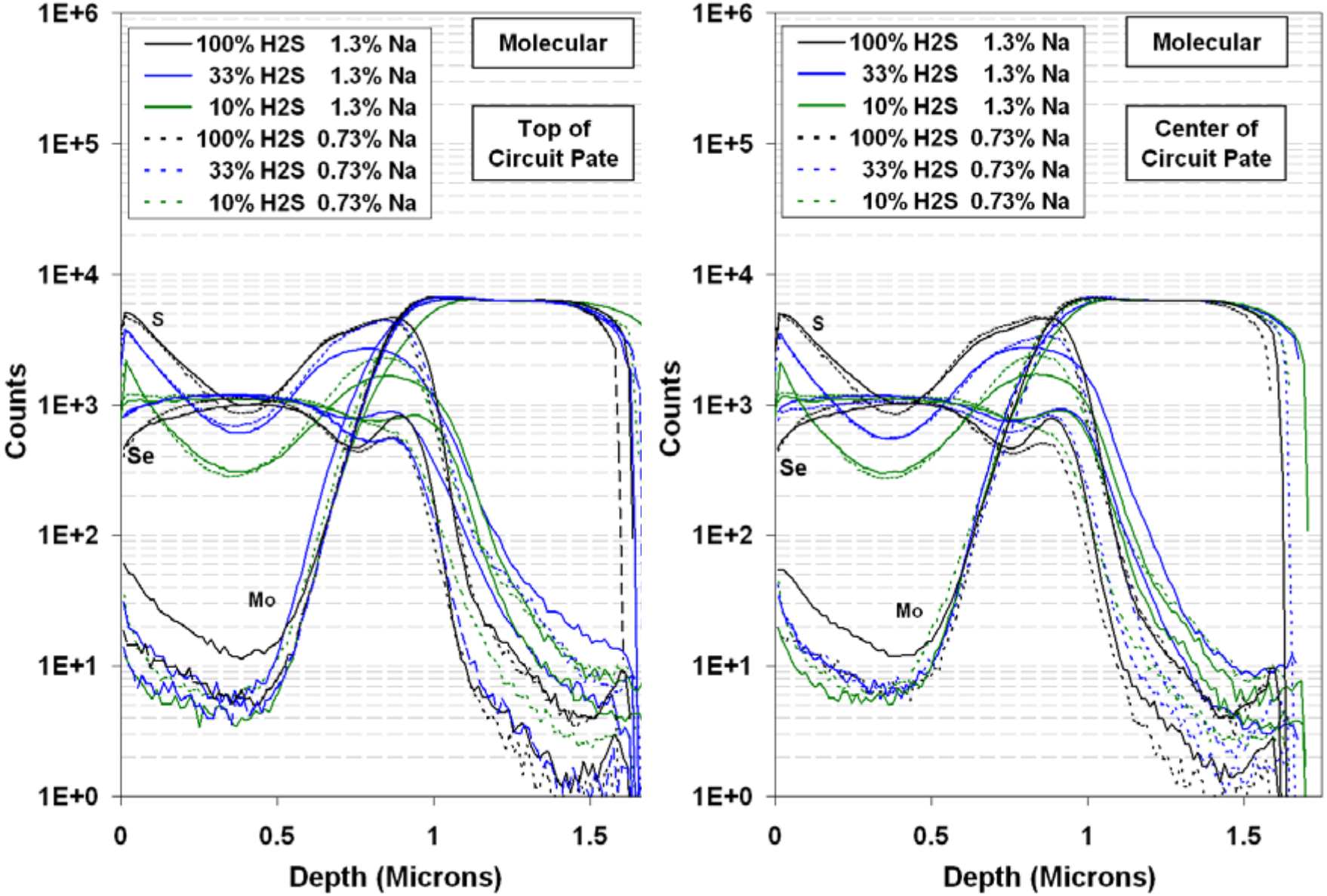


Figure 23. Molecular SIMS profiles - top and center, emphasizing sulfur.

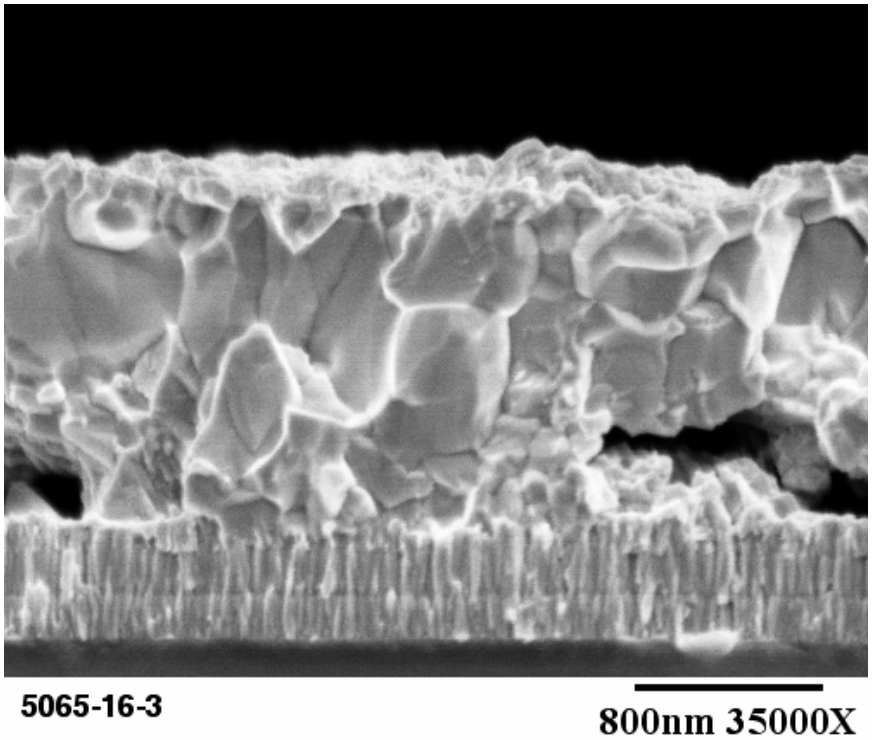


Figure 24. SEM of pre sputter dose baseline absorber.

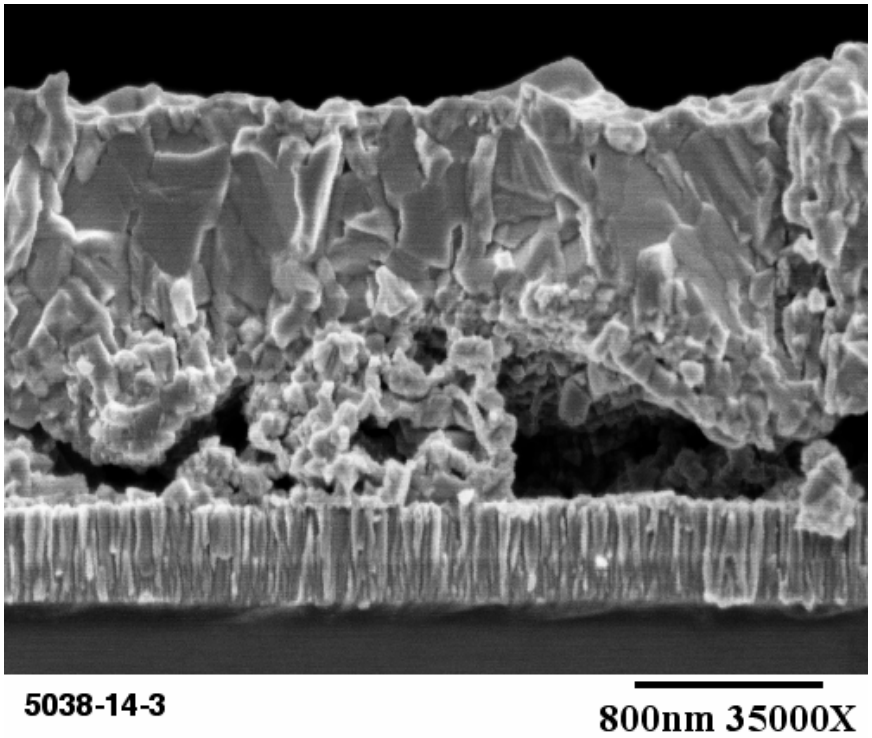


Figure 25. SEM image of pre sputter dose baseline absorber with lower than normal Na.

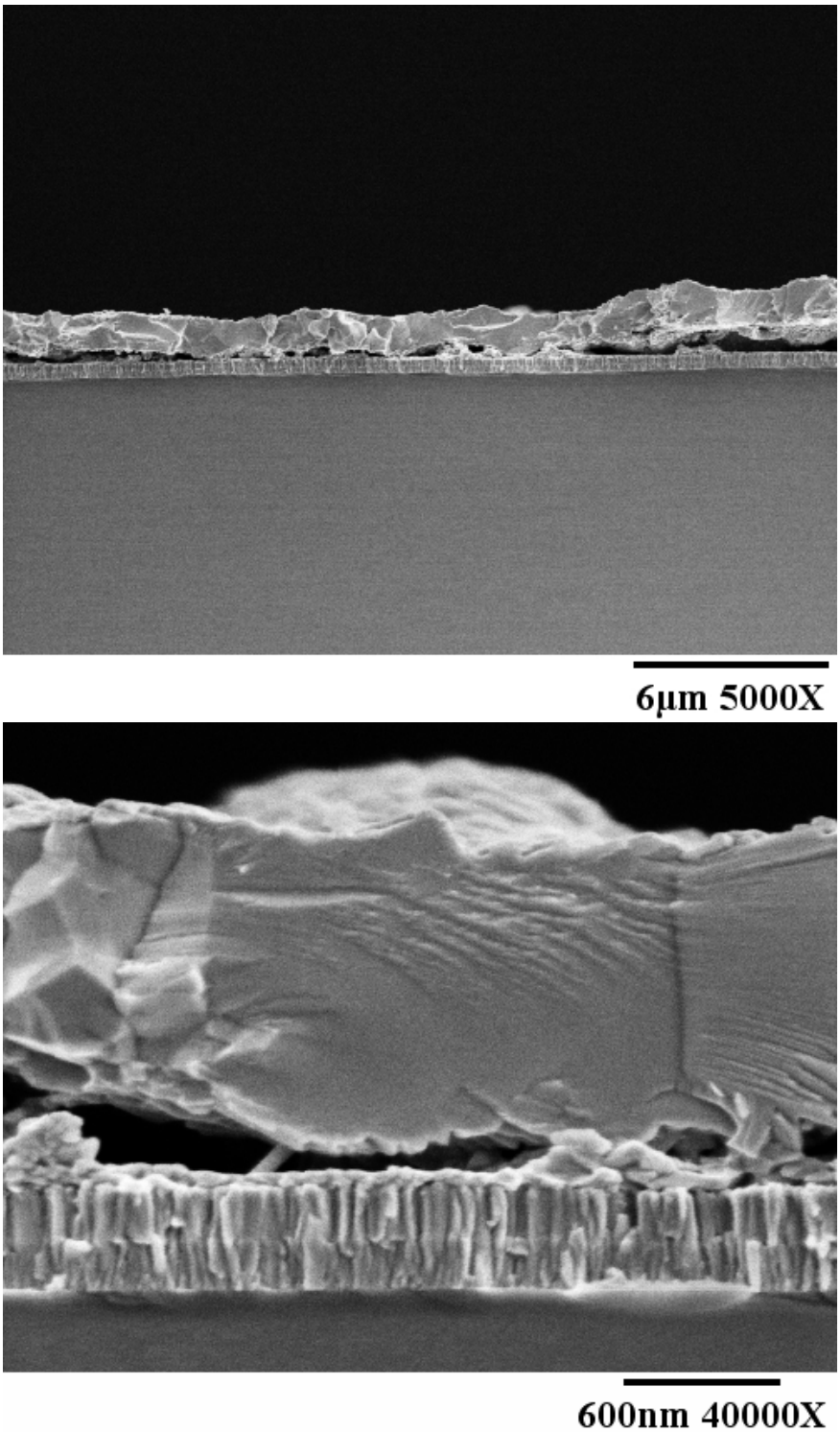


Figure 26. SEM images of a sputter dosed absorber.

High Ga absorbers

Increasing the Ga content in the absorber was pursued for improvements in module efficiency, improvements in the temperature coefficient of efficiency, and for potential improvements in adhesion. Precursors with both 15% and 25% Ga content were included in two sets of reaction runs. For the first set the temperature of the selenization plateau was increased relative to the baseline. For the second set the temperature during sulfidation was increased.

Performance was similar for both sets and dominated by lower and highly variable FF. Higher Ga content led to small losses in Jsc relative to baseline as expected for higher Ga content in the SSI graded absorber structure; the thickness of the higher bandgap, nominally CuGa(Se,S) without In, region is increased. If any gain in Voc was achieved for the higher Ga content it was masked by the lower and highly variable FFs. Sun soaking laminates did not significantly improve FF. Hillocks (bumps in the CIS absorber) were observed for the high Ga absorbers and lower performance is possibly related to the presence of these hillocks.

Sally Asher at NREL coordinated SIMS and SEM analysis of these absorbers with temperature variations during reaction and increased Ga content along with baseline samples selected from two reactor locations. Figure 3 (Introduction) is an example of this SEM work. There may be differences in the extent of the "fine grain region", at the CIS/Mo interface or the grain structure; however, additional follow-up would be required for unambiguous conclusions.

Figure 27 through Figure 34 summarize the SIMS analysis where two or more charts are presented for each of the scans – molecular, positive ion and negative ion. The first chart for each scan type presents the data color coded by element and follow on charts present the same data but with the data color-coded according to experimental conditions. The samples included absorbers with 15% Ga – baseline temperature, 15% Ga – elevated temperature and 25% Ga – elevated temperature. The samples produced at an elevated temperature were prepared by etching off the ZnO from a completed device whereas all other samples were selected prior to CdS deposition.

The following summarizes results emphasizing the absorber rather than the Mo layer:

- The Se and In data is consistent with trends in S and Ga.
- The high Ga region at the back is thicker and has higher Ga content for 25% Ga.
- The Ga content at the front of the absorber (0 to ~0.3 μ) is higher for higher reaction temperature and for 25% Ga.
- S content at the back and middle of the absorber may be slightly higher for the higher reaction temperature.
- S content at the front of the absorber may be slightly lower for 25% Ga.
- Na content at the front of the absorber is higher for the lower reaction temperature or related to sample preparation and analysis.
- Na content is not clearly related to the Ga or S content for this data, which includes a broad range of concentrations through the absorber. However, Na may be higher in the middle of the absorber corresponding to the higher but relatively low Ga content in the middle of the absorber for the 25% Ga.

- Oxygen concentration is relatively high through the Mo and the peak at the Mo/glass interface is related to the measurement method and the nonuniformity of the absorber.
- There may be less Na in the Mo for 25% Ga.

These results suggest follow-up including modification of absorber thickness and absorber reaction conditions.

Three samples of absorbers made using baseline conditions from two locations within a reactor were analyzed. Two of the samples were from edges and one from the center of each circuit plate. The S content was low for one of the samples from an edge for the reactor location that typically give slightly lower module performance. Otherwise there were no clear trends related to reactor or circuit plate position.

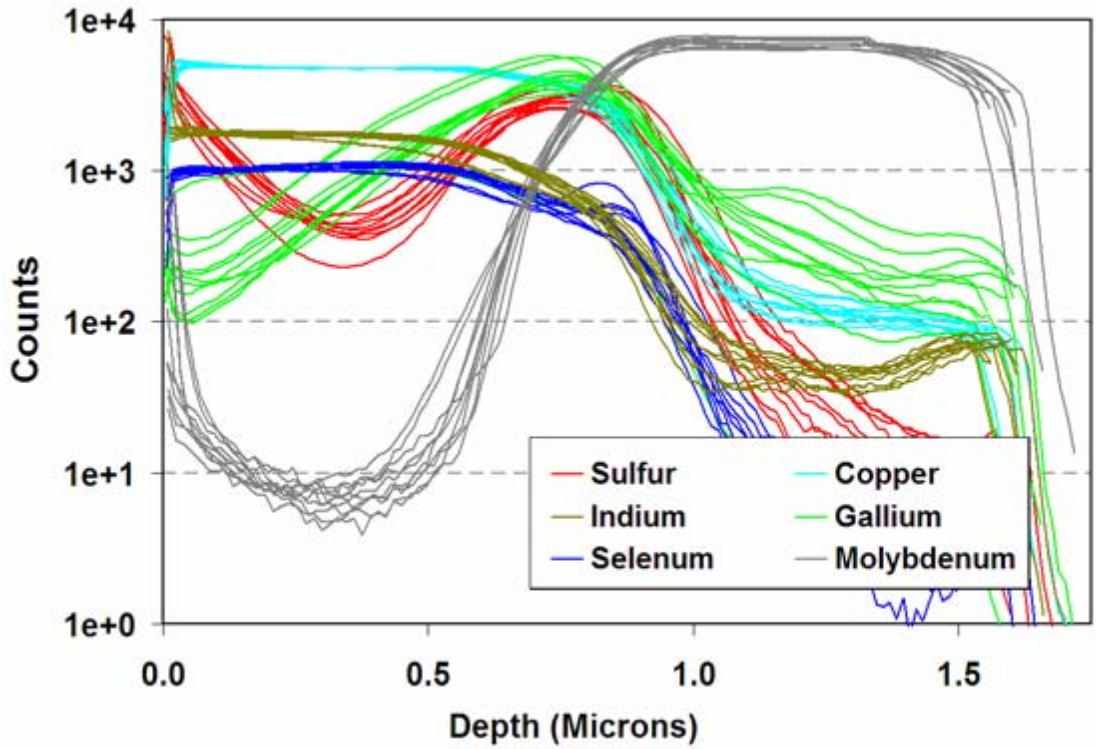


Figure 27. SIMS molecular scan color-coded by element.

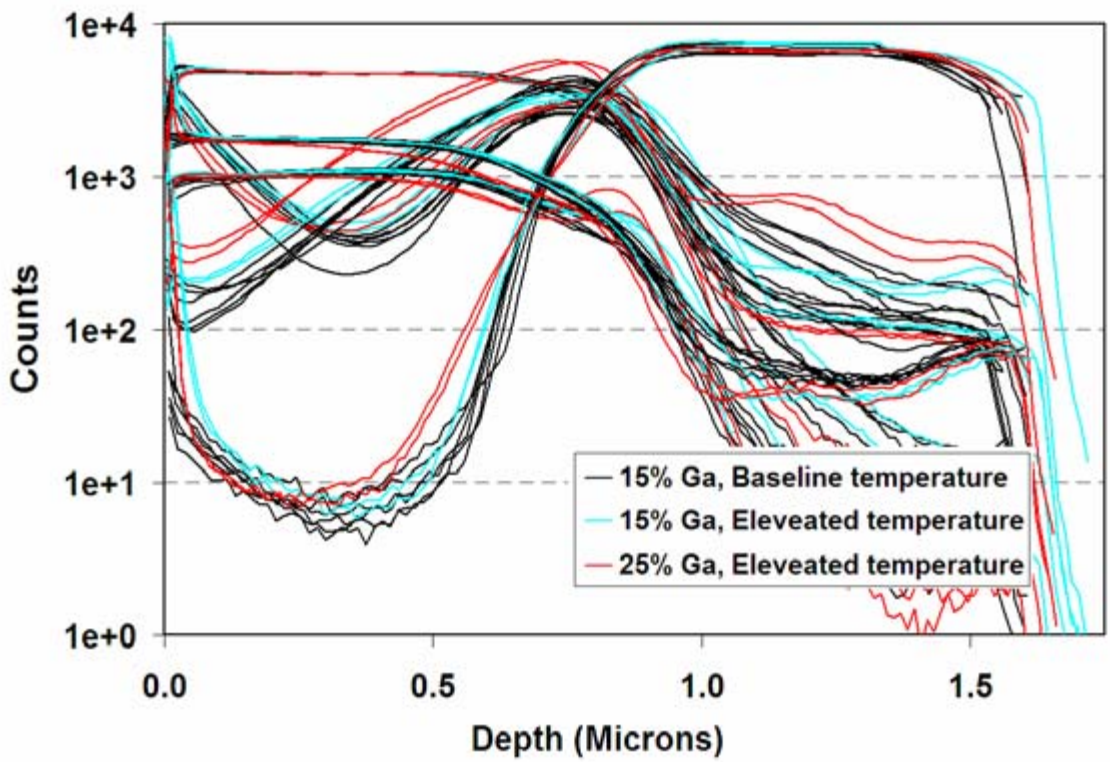


Figure 28. SIMS molecular scan color-coded by process variant.

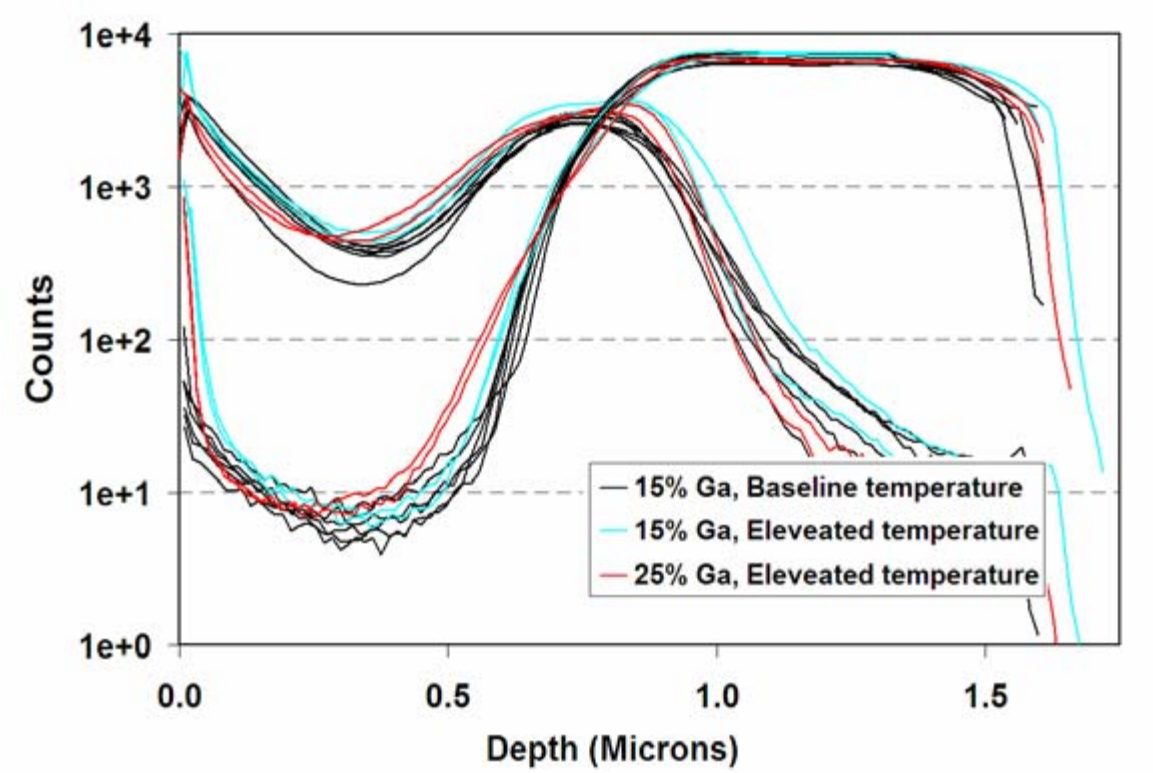


Figure 29. SIMS molecular scan color-coded by process variant, emphasizing sulfur.

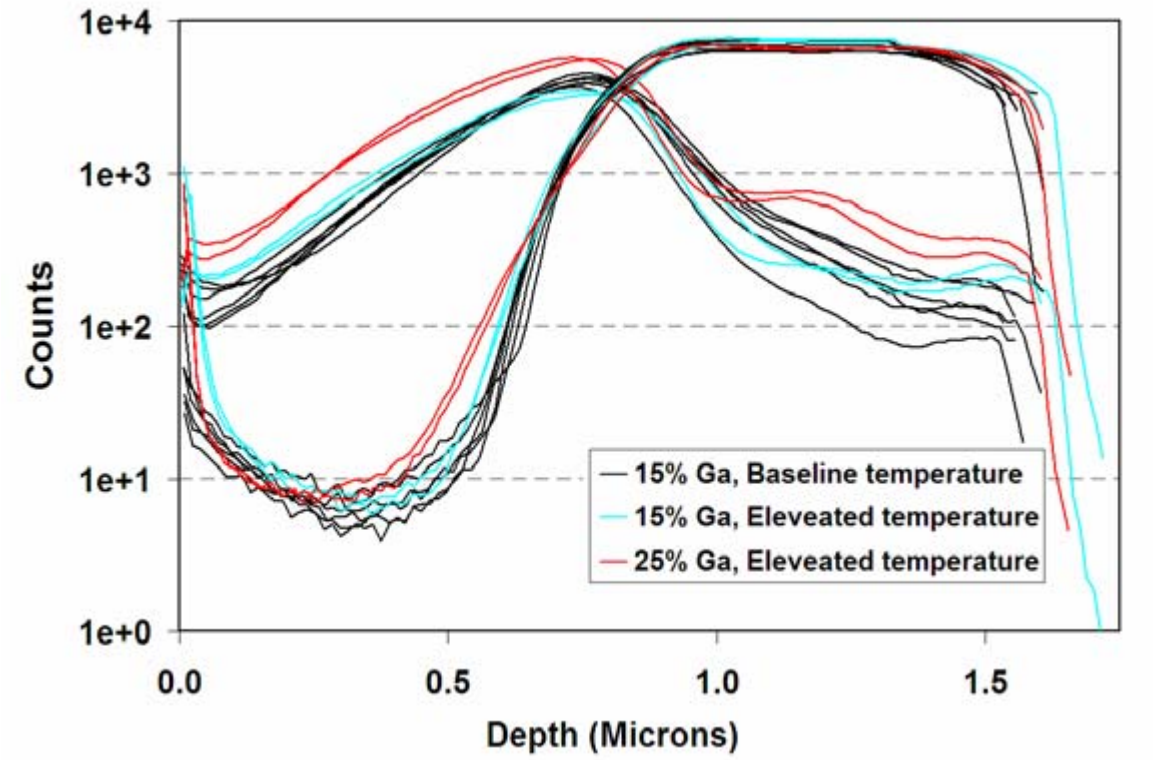


Figure 30. SIMS molecular scan color-coded by process variant, emphasizing gallium

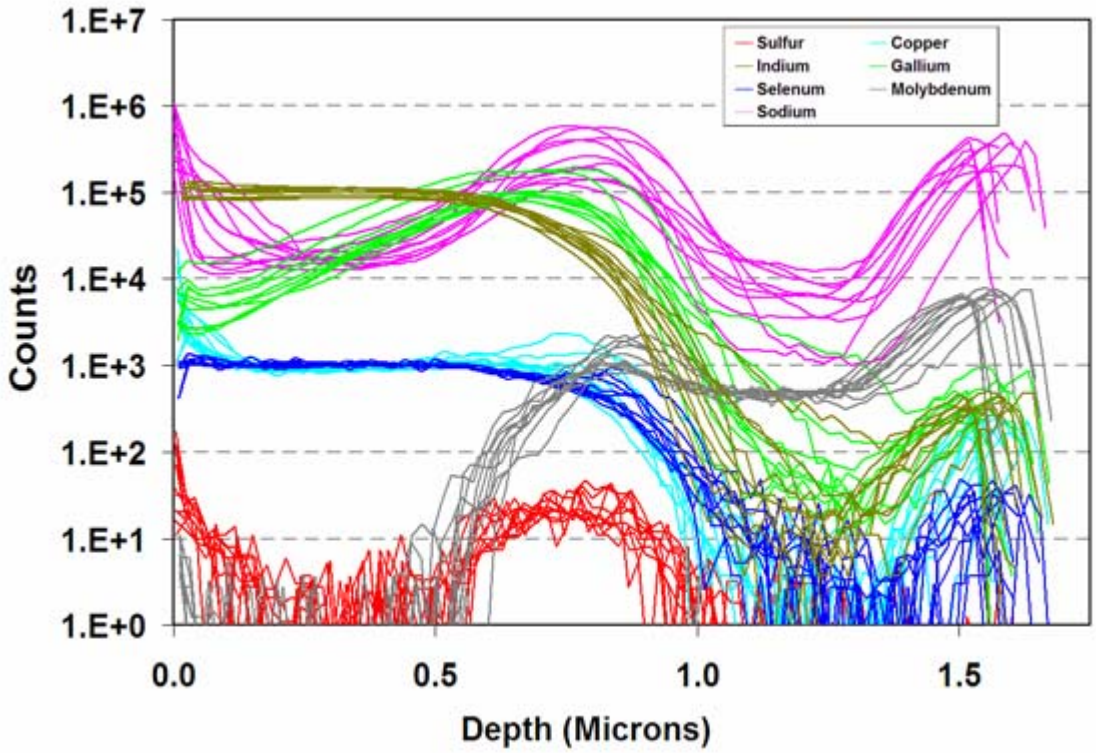


Figure 31. SIMS positive ion scan color-coded by element.

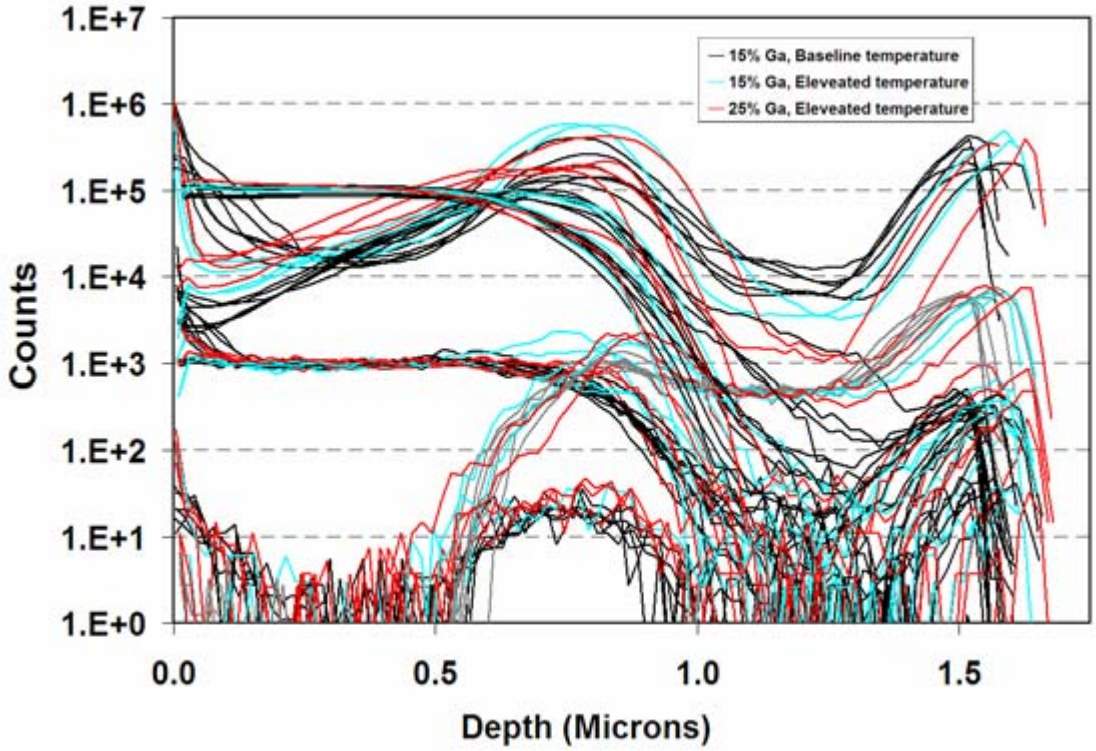


Figure 32. SIMS positive Ion scan color-coded by process variant.

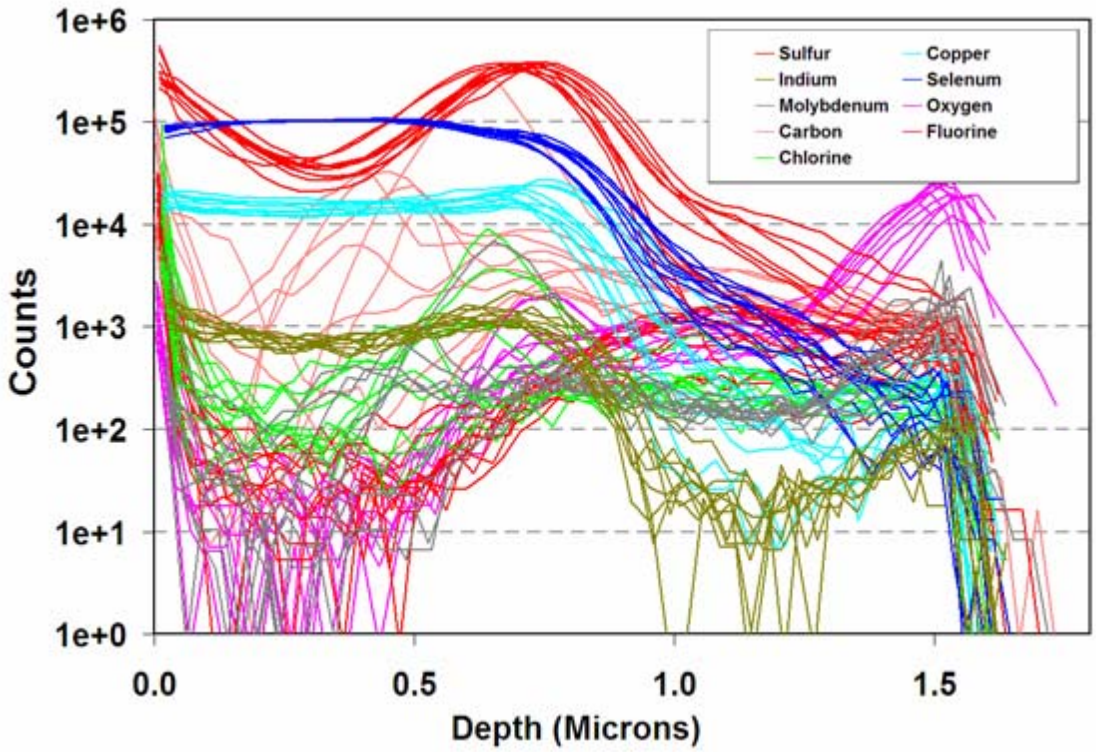


Figure 33. SIMS negative ion scan color-coded by element.

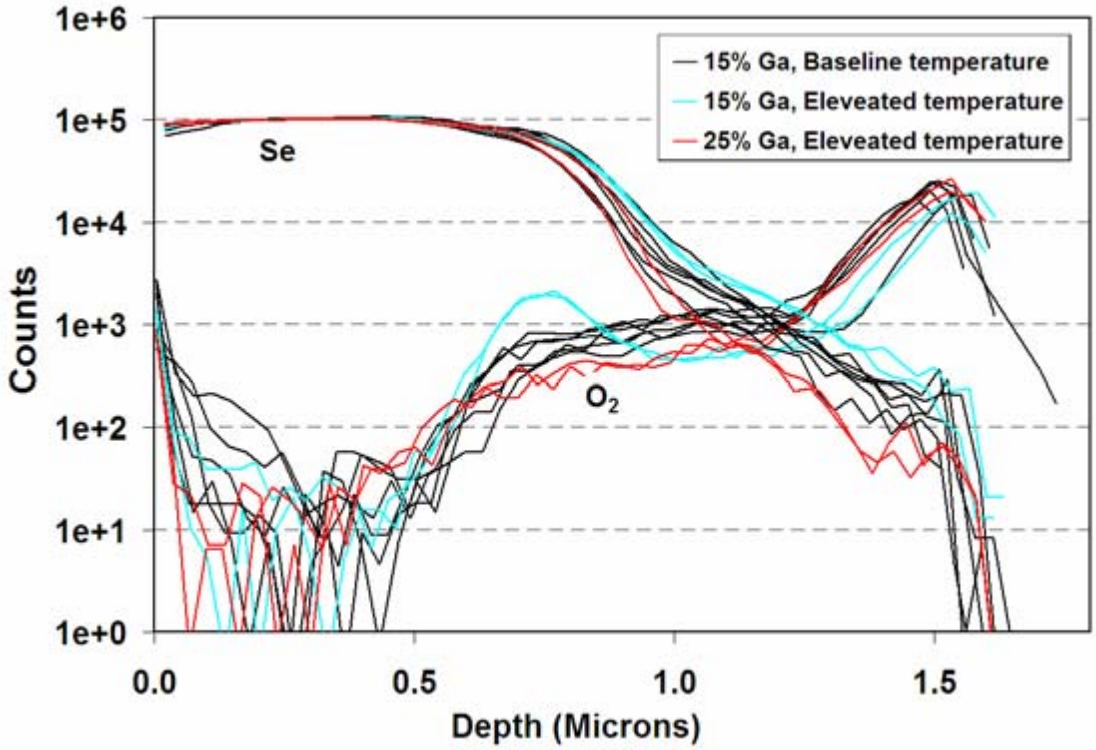


Figure 34. SIMS negative ion scan color-coded by process variant, emphasizing oxygen.

Non-Collimator Moly Deposition

As described in the Introduction, the SSI CIS base electrode consisted of a ca. 500Å thick SiO_2 barrier layer followed by a 3500Å Mo electrode, deposited using a specially modified sputtering technique to guarantee good patternability by laser scribing [***9***]. While the bulk of the Mo coating (perhaps 3300Å) is subsequently provided by deposition from two conventionally configured targets, the first thin layer is deposited from a separate target through a "collimator" with O_2 added to the sputter gas mix. This method, while effective, increases cost due to poor Mo utilization (about 90% is intercepted by the collimator) and associated costs related to maintenance. In addition, Mo accumulation on the collimator causes process variation, with the thickness of the first thin layer ranging from 200Å with a new collimator to as little as 50Å before the collimator is replaced. Remarkably, this systematic variation does not produce discernable change in patternability or module performance.

With the aim of decreasing the cost of the first thin Mo layer (and avoiding process variability), alternative process conditions (sputtered without a collimator) were explored and developed. Since P1 scribe quality is influenced by both laser set-up and, to much greater extent, the molybdenum properties, P1 process conditions were also later explored. The criteria for selection of an improved process were laser-scribe quality and, finally, circuit performance.

First, a significant number of base electrode substrates were made using a relatively broad range of Mo sputtering power and O_2 flow rates, and all were then patterened using baseline laser conditions. Optical micrographs and Dektak profiles of resultant P1 scribes were compared to look for evidence of lifting or partial separation of the Mo film at the scribe edges, a sign of poor pattern quality and probable shunting [***19***]. Minimal lifting at the edges was indicated for all explored process conditions, although some minimal cracking was observed for relatively low power and high O_2 flow rates. Based on these results, circuit plate production and P1 pattern optimization was then pursued for two selected Mo non-collimator deposition process conditions, one with lower and one with higher O_2 flow.

Patternability was explored on the two selected candidates by varying the laser power and checking the scribe lines for consistent isolation, lifting at the edges that could cause shunting, and damage to the underlying glass. For typical setups, the P1 scribe conditions do not have an impact on breakage or the amount of Na in the absorber [***20***]. The interaction between the laser beam and the Mo is a probe of Mo properties and the run-to-run repeatability of these properties. Therefore, process selection criteria included process depth of field and the impact of Mo deposition conditions on the interaction between the laser and the base electrode. This interaction can be quantified with a model that assumes the crater or scribe diameter is determined by a Gaussian intensity profile for the laser beam and threshold intensity for removal. Fitting data for crater diameter versus intensity (or power for otherwise fixed beam properties) yields both the beam diameter and the threshold power for Mo removal. Figure 35 is an example of scribes made with a progression of scribe widths made by varying laser power.

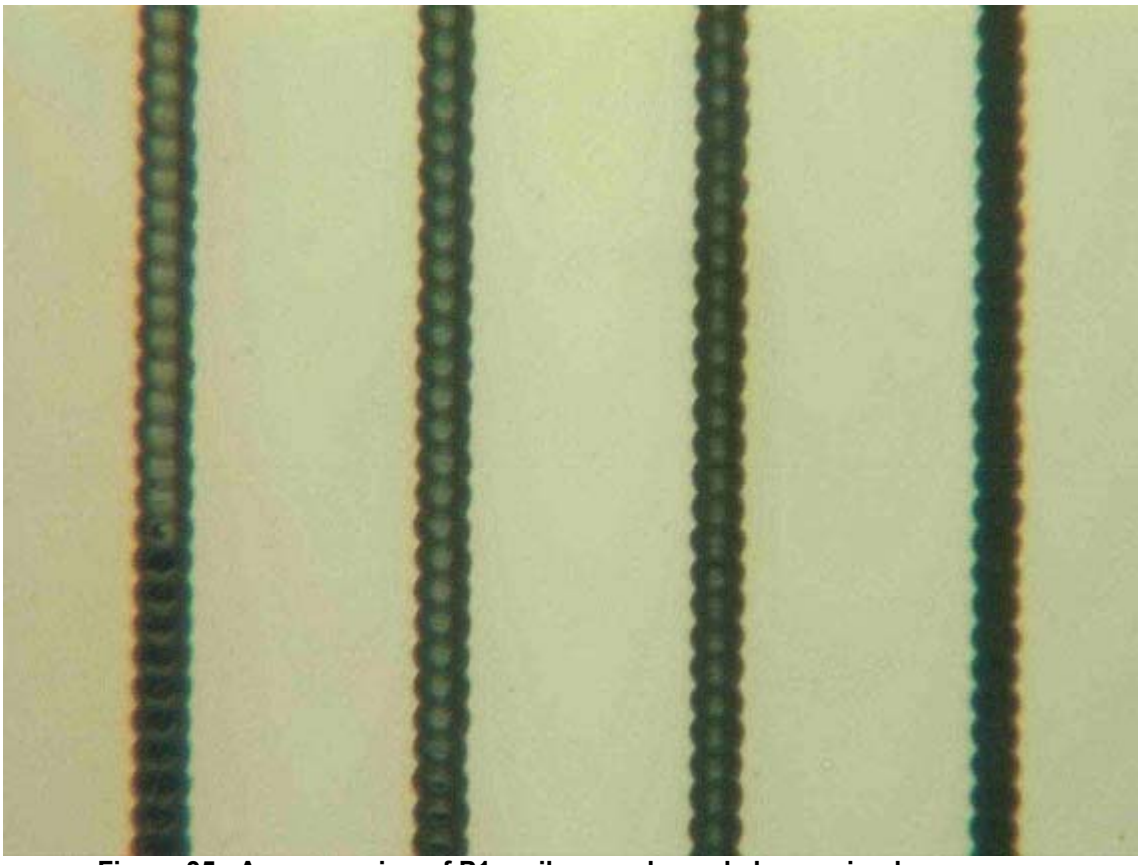


Figure 35. A progression of P1 scribes made made by varying laser power

Results for baseline Mo deposition conditions, thin Mo, an electrode without the thin Mo, and two experimental Mo deposition process conditions are presented in Figure 36. The relative positions (or intercepts in alternative data presentations) of the data for different deposition conditions and the associated fit curves indicates that the threshold for removal of thin Mo is the lowest and baseline Mo is the highest. Repeatability of the relative thresholds for removal is indicated by consistency with repeated runs – "Run A" and "Run B". A process depth of field (sensitivity to focus, power or Mo deposition conditions) can be determined by expanding on this approach.

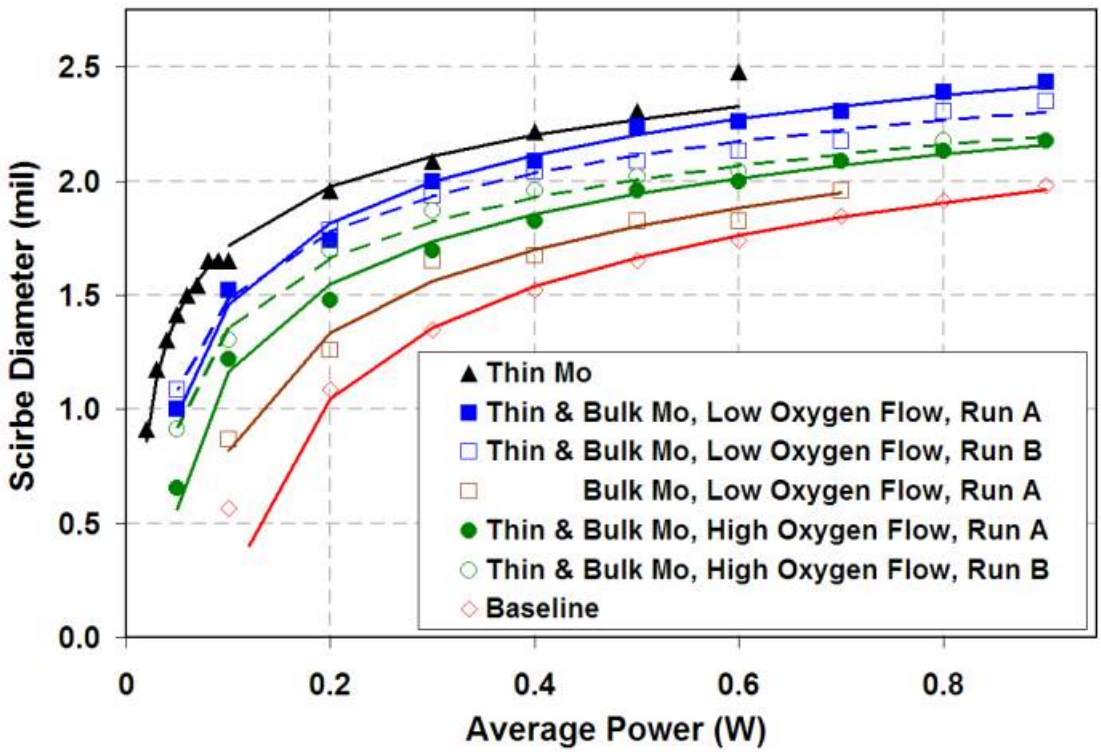


Figure 36. P1 scribe diamater vs. Mo process and P1 power

Thus, both candidate non-collimator Mo processes were found to have robust, good quality P1 patternability. However, initial circuits fabricated on these substrates were found to have Voc systematically low compared to control circuits fabricated on baseline substrates. Since molybdenum and sodium concentrations can influence Voc, the experiment was broadened to include circuits prepared from precursors with an elevated as well as a baseline sodium dose. Surprisingly, increased sodium dosing level was also ineffective in regaining the lost Voc, as seen from average circuit performance in Table 2, summarized from 18 baseline and 36 non-collimator circuits.

Table 2. Average circuit performance vs. Mo method and sodium dose

Mo	**Na dose**	**Eff** (%)	**Voc** (V)	**Jsc** (mA/cm^2)	**FF**	**Pm** (W)
Non-Collimator Mo						
lower O2	130% Bsl	11.6 +/- 0.2	0.507 +/- 0.007	36.4 +/- 0.7	0.629 +/- 0.013	42.1 +/- 0.8
	Bsl	11.5 +/- 0.4	0.499 +/- 0.008	36.7 +/- 0.5	0.626 +/- 0.011	41.6 +/- 1.5
higher O2	130% Bsl	11.6 +/- 0.6	0.500 +/- 0.009	37.1 +/- 0.8	0.623 +/- 0.014	42.0 +/- 2.1
	Bsl	11.5 +/- 0.3	0.497 +/- 0.007	36.9 +/- 0.7	0.627 +/- 0.010	41.7 +/- 1.0
Baseline Mo with collimator						
	130% Bsl	12.2 +/- 0.5	0.520 +/- 0.007	37.4 +/- 0.9	0.627 +/- 0.017	44.2 +/- 1.7
	Bsl	12.2 +/- 0.3	0.521 +/- 0.002	36.7 +/- 0.5	0.638 +/- 0.006	44.3 +/- 1.0

A t-test showed that only the 4-point difference in Voc is statistically significant. This study shows that the base electrode Mo structure influences device performance in ways still not understood.

Cadmium-Free modules

Development of high efficiency cadmium-free CIS modules is an important world-wide research focus. At SSI this has been achieved by simply skipping the CdS "dip" process step, entirely omitting the "buffer layer" conventionally applied between the CIS semiconductor and ZnO transparent conductor. (This is the only process change—the modules are in all other ways baseline processed). This remarkable result appears to be a consequence of the unique properties of CVD ZnO, possibly the gentle, "low-energy" deposition process. It should also be recognized that CVD produces a kind of "inherent" buffer—it is known from earlier studies that the first few tenths of a micron of deposition are highly resistive and have a different crystal structure from the bulk of the conductive window layer [*21*]. (This is true even when the entire film is uniformly doped).

However, it must be noted that modules produced in this way show relatively poor performance initially but improve strongly with sun exposure to a normal level. Since implementation of the new sodium sputter-dose process produced modules with reduced light-dark performance transients, it was interesting to produce a new set of modules without the CdS "Dip" process to test if these would also show reduced transient behavior.

In general, the new sputter-dosed cadmium-free modules exhibited the same behavior as the inherent (gas-phase) sodium-dosed modules [*22*] made earlier: tested without lightsoaking, initial module performance was low, but improved strongly with sunsoaking. Figure 37 shows initial, pre-sunsoak efficiency ranging between 8% to 10%.

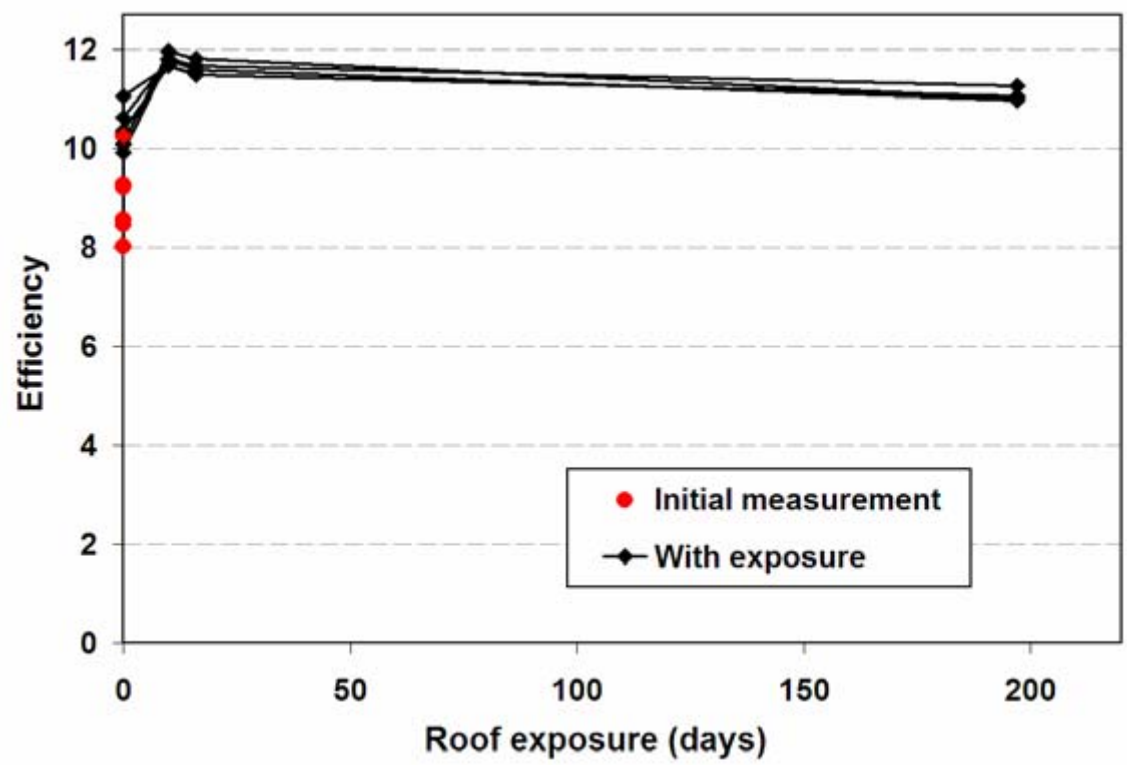


Figure 37. Performance of cadmium-free CIS modules—as built and after rooftop exposure

After 2 hours of sunsoaking, efficiency improved to between 10% and 11%. When next tested after 10 days of sunsoaking, the average efficiency of the whole group had improved to 11.6%, indistinguishable from baseline modules incorporating the CdS layer! This dramatic improvement resulted from strong gains in Voc and FF partly offset by a drop in Jsc (likely a result of solarization of cover glass and UV-induced increase in ZnO conductivity).

Figure 37 also shows that after 198 days the efficiency of the group had declined slightly to 11.1%, with the drop from small but equal declines in the Jsc and FF, while Voc remained completely stable. Additional measurements and tracking would be necessary to determine how much of this change is from measurement variability and if the performance has stabilized.

Three conclusions can be drawn:
1. High efficiency cadmium-free CIS modules are possible
2. CVD ZnO offers a means to achieve this goal without any additional buffer layer
3. The transient mechanism reduced by sputter-dosing is probably not the transient mechanism reduced with the CdS "dip" process.

Narrower Patterning

Experience with the mechanical pattern machine led to confidence in its reliability and repeatability. The baseline total pattern width had been 19 mils for 0.27-inch wide cells. Each of the 14 tips of the MS2 machine were carefully aligned and the patterning software was modified to reduce the total interconnect width to 12 mils resulting in 2.6% more active area. Modules with the narrower interconnects demonstrated 2.7% better Jsc at the 95% confidence level. There were no losses due to pattern mistakes or pattern crossover.

Mechanical Scribing - Diamond Tipped Needles

Mechanical scribing reliability, reproducibility and productivity were improved by increasing scribe tip lifetime. Mechanical scribing is done using needle like tips to scribe lines in the films parallel to laser scribes in the Mo (P1). The tips are fixed and touch the film surface while the plate moves under the tips. The tips are oriented at about a 70 degree angle to the plates, aligned with the direction of plate motion. For the baseline method, the first stroke is a "rake" - the tip points in the same direction as the motion of the substrate. This is followed with a "plow" stroke - tips pointing into the approaching material.

With use, the tip wears, producing a flat spot at the contact area. Eventually this flat spot causes the tip to ride along the top of the film and to not scratch through. This failure to scribe typically happened after one to two thousand "Rake/Plow" cycles during a ZnO (P3) scribe. When the scribe failure is seen, the errant tip is rotated 90 degrees and the tip number and rotation state is noted. When the fastest wearing tip has been rotated 360 degrees, i.e. back to the initial flat spot, the whole tip set is replaced and the number of total cycles for that tip set is recorded.

Two modifications improved this process: change from carbide tips to diamond tips and change from first executing a rake stroke to first executing a plow stroke. Tip set life data in terms of

the total number of passes made with a set is presented in Figure 38 for before and after these changes. Starting at tip set 21, diamond tips replaced carbide tips leading to last much longer tip life.

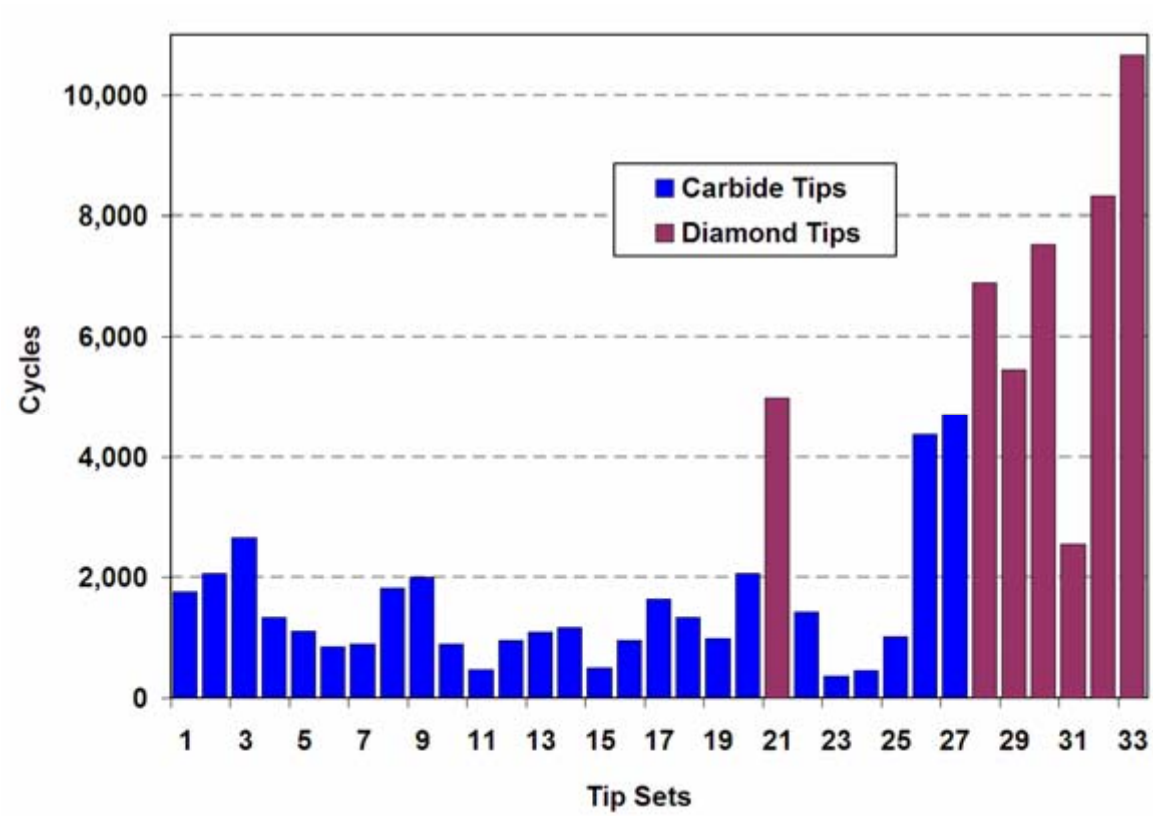


Figure 38. Lifetime comparison of carbide and diamond tips for mechanical scribing.

For tip sets 26 and 27, the patterning method was changed to the "plow-first" stroke. This also improved tip life. The "rake-first" approach apparently led to ware from the tip riding up onto a chip of the broken out ZnO and riding along the relatively abrasive ZnO surface. With the "plow-first" method the ZnO chips are immediately pushed up and away from the tips. At tip set 28 both "plow-first" and diamond tips became the baseline method. At tip set 31 the metal shafts of the diamond tips were found to be more malleable than the carbide tips and they could be more readily bent or damaged. The longer run cycles of tip sets 32 and 33 resulted from better training in the method to install and rotate the diamond tips.

Indium/Silver Solder – Secondary Vendor

During the contract period, a secondary supplier of indium / silver solder (97% In, 3% Ag) was evaluated. A series of performance tests was conducted to verify that the material from the new vendor was equivalent to the previous material. Specifically, all dimentional requirements were duplicated:

- Solder bead width 2.5 +/- 0.5 mm (by direct measurement)
- Solder bead thickness 2.0 +/- 0.5 mils (by direct measurement)

- Adhesion met spec of 200 grams average (pull test verified bond strength of 351 to 385 grams)
- Equivalent electrical performance (electrical distributions of 20-part populations showed equivalent powers)

Furthermore, the new solder did not discolor with idle time on the tinning machine and was delivered more reliably to the solder heads. As a consequence, maintenance was reduced and productivity increased. The new solder has been adopted as the standard material, displacing the previous solder.

Production Experience with Diethylzinc (DEZ) for CVD ZnO

The organometallic compound diethylzinc (DEZ) is the zinc reagent employed in chemical vapor deposition of ZnO transparent conducting film [***23***]. This material, produced by Akzo Chemicals, is a pyrophoric liquid with vapor pressure (14.5 torr @ 20 C) and density (1.2) similar to those of water. DEZ is supplied in large (roughly 100 L) tanks, from which the liquid is transferred as required to a vapor generator, generally referred to as a "bubbler" because an inert "carrier" gas such as nitrogen is metered though the liquid to promote evaporation and help transport the generated vapor to the deposition reactor.

This method for supplying the process chemical is elegant in that it is essentially a distillation process, purifying the DEZ as it is delivered. This works because the anticipated impurities have substantially lower vapor pressure. However, in sufficient concentration this could with time cause a different problem: impurities could accumulate to a significant amount in the bubbler, even ultimately filling the bubbler! If this actually occurred, it would be necessary to periodically drain the bubbler, with the attendant engineering and equipment complexity.

In practice this proved to be a negligible problem. During decommissioning of the two CVD systems the opportunity arose to inspect the contents of the bubblers after the DEZ was removed. First, the DEZ bubbler of each was (presumably) emptied by passing nitrogen through it for an extended period of time, well past the time where net weight of the bubbler reached zero. Then, the nitrogen in the bubbler was carefully displaced with air—no evidence of any reaction was seen. Finally, the bubblers were opened and inspected. An oily residue, probably no more than 10cc of liquid, was found at the bottom of each bubbler. The residue was slightly air-reactive, transforming after a number of minutes into a thin solid crust. These are exactly the characteristics expected for organometallic impurities.

Each reactor processed about 1.9 metric tons of DEZ over several years of production service, during which the bubblers were never emptied or purged. The small residue found at the end of this cumulative production implies that the diethylzinc contained only about 10 ppm impurity.

Reliability

Reliability will be addressed from the following perspectives:
1. IV Measurements
2. Certification testing
3. Test to failure
4. Outdoor testing
5. Warranty considerations

IV Measurements

The techniques used to measure the IV curves of PV modules are defined in IEC 904-1, with temperature corrections defined by IEC 891. These procedures assume that the IV properties of the devices behave like crystalline silicon. CIS, however, has the additional complication that the measurement of the IV curve is sensitive to the recent history of the module [***24***]. The measurement is sensitive to factors that are less important for crystalline silicon (putting aside LID effects):
- Recent (forward) voltage bias
- Recent light exposure
- Recent exposure to high temperatures (over 80°C).

Exposure of CIS laminates to elevated temperatures during processing (or during accelerated environmental testing) causes a decrease in the measured fill factor. The loss is reversible, and light exposure or forward bias accelerates the recovery. This initial loss and subsequent recovery of fill factor is called the "thermal transient effect" (almost the inverse of the Stabler-Wronski effect in amorphous silicon) and is the largest problem for reliability testing of CIS modules.

The measurement is also sensitive to the sweep rate of the voltage bias used to measure the IV curve. Outdoor measurements are typically very slow compared to pulsed "flasher" measurements made indoors.

Any discussion of reliability testing must therefore begin with a decision regarding the testing methodology. Given the sensitivity of the measurement of CIS devices to their previous exposure to voltage bias, thermal exposure or light exposure, the most defensible choice is to use outdoor measurements, with a relatively slow voltage sweep, corrected back to standard test conditions. However, outdoor measurements are impractical for routine, high volume testing. Outdoor testing is tedious to perform and can only be done for a short time around noon, provided there are clear skies. Therefore, methodologies were developed to use a pulsed solar simulator as the standard. A minimum outdoor exposure (at open circuit) of two hours at 1/3 sun or more (even under overcast skies) prior to the pulsed simulator measurement was adopted. Forward voltage biasing to Voc immediately before the measurement was found to be necessary to minimize short-term transients [***24***]. The difference between the outdoor and such indoor measurements was found to be small, particularly for more stable devices.

Calibration

Primary calibration of the pulsed solar simulator was based on outdoor measurements using a Daystar tester. A set of temperature coefficients was developed to correct the measurements back to standard test conditions. Good agreement has historically been demonstrated between SSI and NREL measurements. In order to recheck simulator calibration, and to estimate the difference between simulators, SSI, NREL and FSEC measurements were compared for 60 CIS modules provided to NREL for the High Voltage Array testing. These modules first went to NREL, where they were measured on the SOMS, LACSS and Spire testers, then to FSEC where they were measured outdoors with a Daystar tester. For the purpose of comparing the measurements, the data from the NREL SOMS was used as a reference value, and ratios of the numbers from the other testers were compared to this reference. Figure 39 through Figure 42 show the comparison of these measurements. The NREL SOMS is an outdoor measurement corrected to STC, the NREL LACSS is a large-area indoor constant light source simulator, and the NREL Spire is a commercial indoor pulsed tester. The SSI measurements were made using an indoor pulsed simulator after 2 hours of outdoor sun soaking.

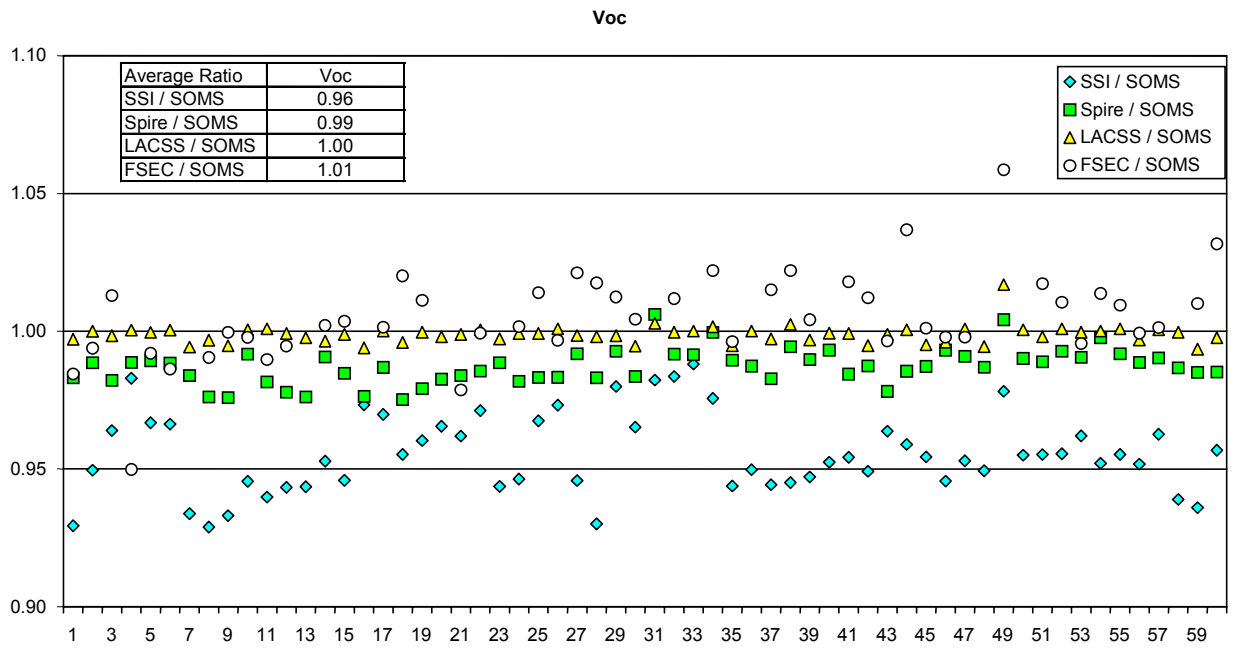


Figure 39. The ratio of the Voc measured on the SSI LAPSS, the NREL Spire, the NREL LACSS and the FSEC Daystar are compared to the Voc measured on the NREL SOMS.

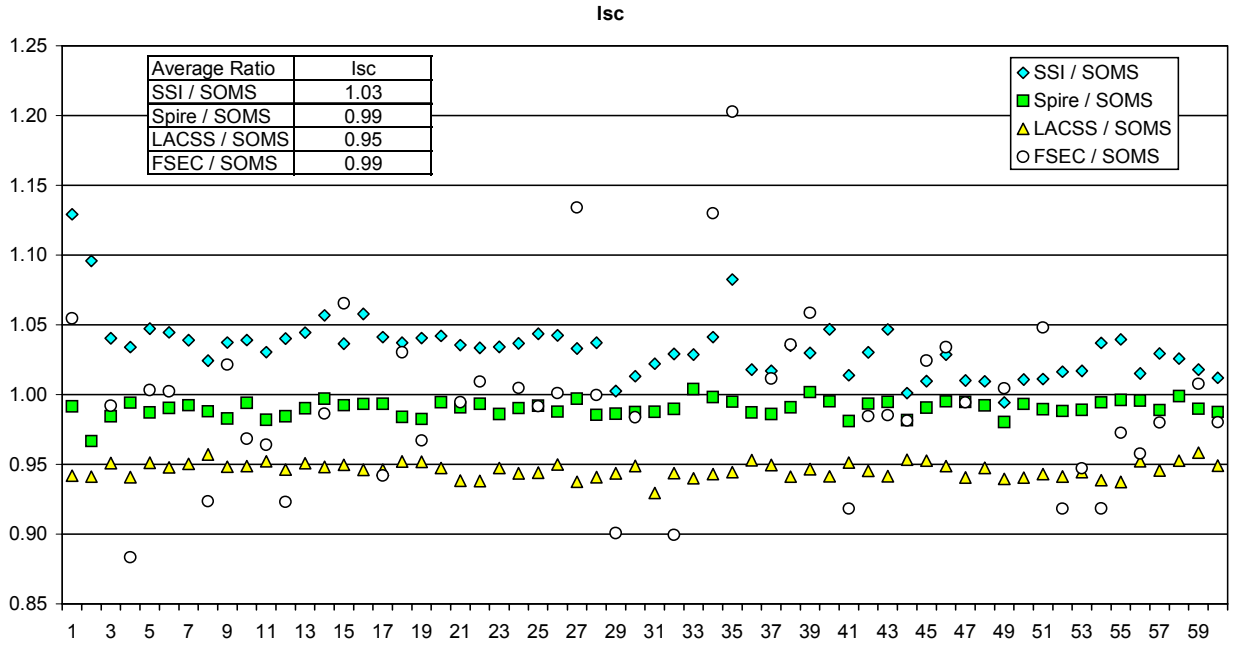


Figure 40. The ratio of the Isc measured on the SSI LAPSS, the NREL Spire, the NREL LACSS and the FSEC Daystar are compared to the Isc measured on the NREL SOMS.

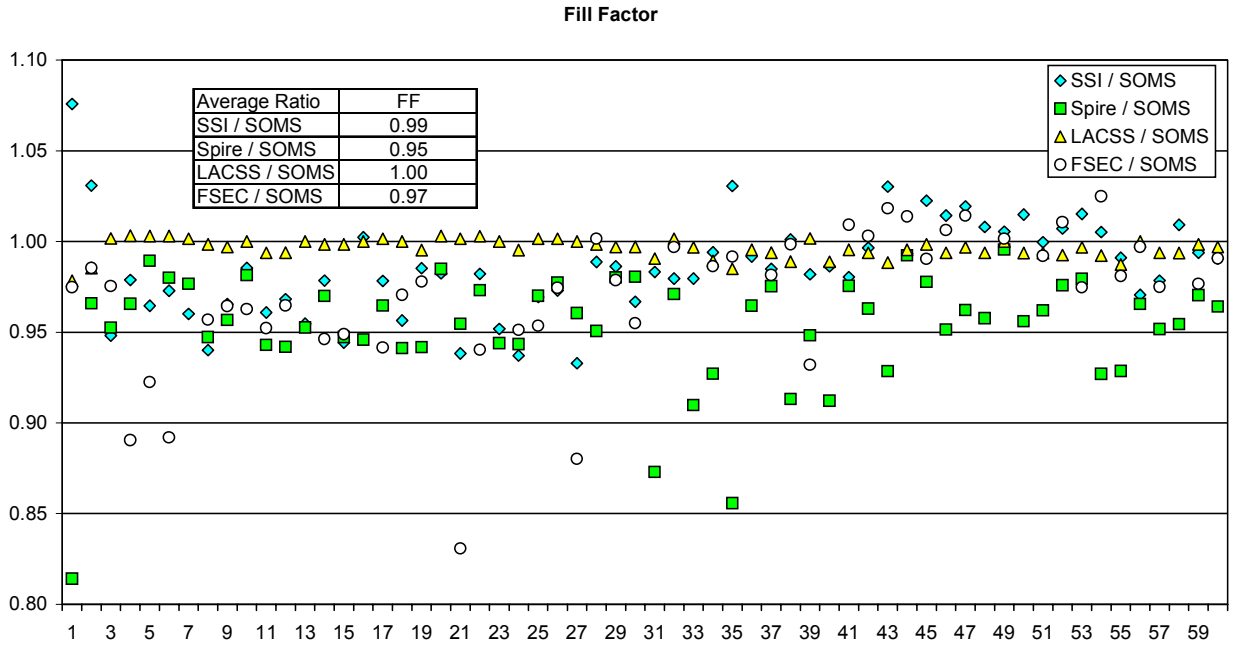


Figure 41. The ratio of the Fill Factor measured on the SSI LAPSS, the NREL Spire, the NREL LACSS and the FSEC Daystar are compared to the Fill Factor measured on the NREL SOMS.

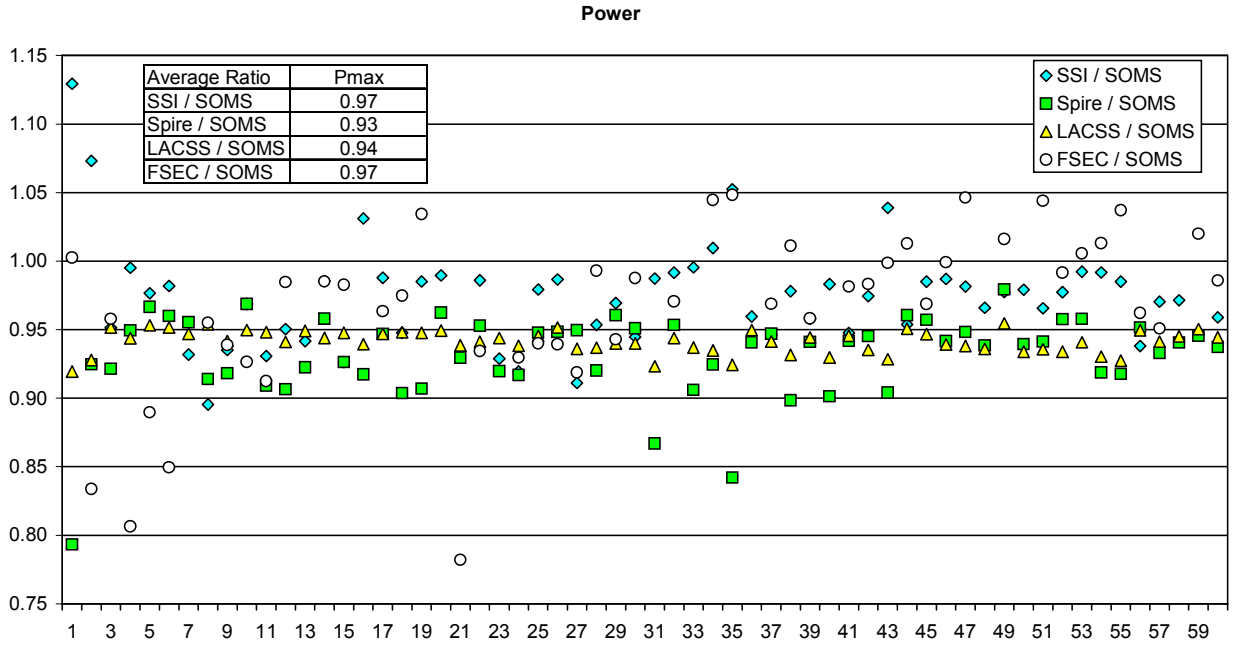


Figure 42. The ratio of the Power measured on the SSI LAPSS, the NREL Spire, the NREL LACSS and the FSEC Daystar are compared to the Power measured on the NREL SOMS.

A summary of these results for the measured cell parameters is presented in Table 3.

Table 3. Average ratios of the IV parameters from a set of 60 ST40 modules measured at SSI, NREL and FSEC compared to the NREL SOMS values.

Average Ratios	Voc	Isc	FF	Pmax
SSI / SOMS	0.96	1.03	0.99	0.97
Spire / SOMS	0.99	0.99	0.95	0.93
LACSS / SOMS	1.00	0.95	1.00	0.94
FSEC / SOMS	1.01	0.99	0.97	0.97

All four testers measure power, on average, lower than the NREL SOMS outdoor measurements. As seen from the individual charts, there is variation in the IV measurements even for properly maintained equipment with controlled testing procedures.

This experiment was repeated for a set of 18 Eclipse 80-C modules sent to NREL as a deliverable for this subcontract. The data for this comparison, shown in Table 4, looks very similar to the previous measurements.

Table 4. Average ratios of the IV parameters from a set of 18 Eclipse 80-C modules measured at SSI and NREL compared to the NREL SOMS values.

Average Ratios	Voc	Isc	FF	Pmax
SSI / SOMS	0.98	1.02	0.99	0.99
Spire / SOMS	0.99	0.99	0.99	0.97
LACSS / SOMS	0.99	0.95	1.00	0.94

Temperature Coefficients

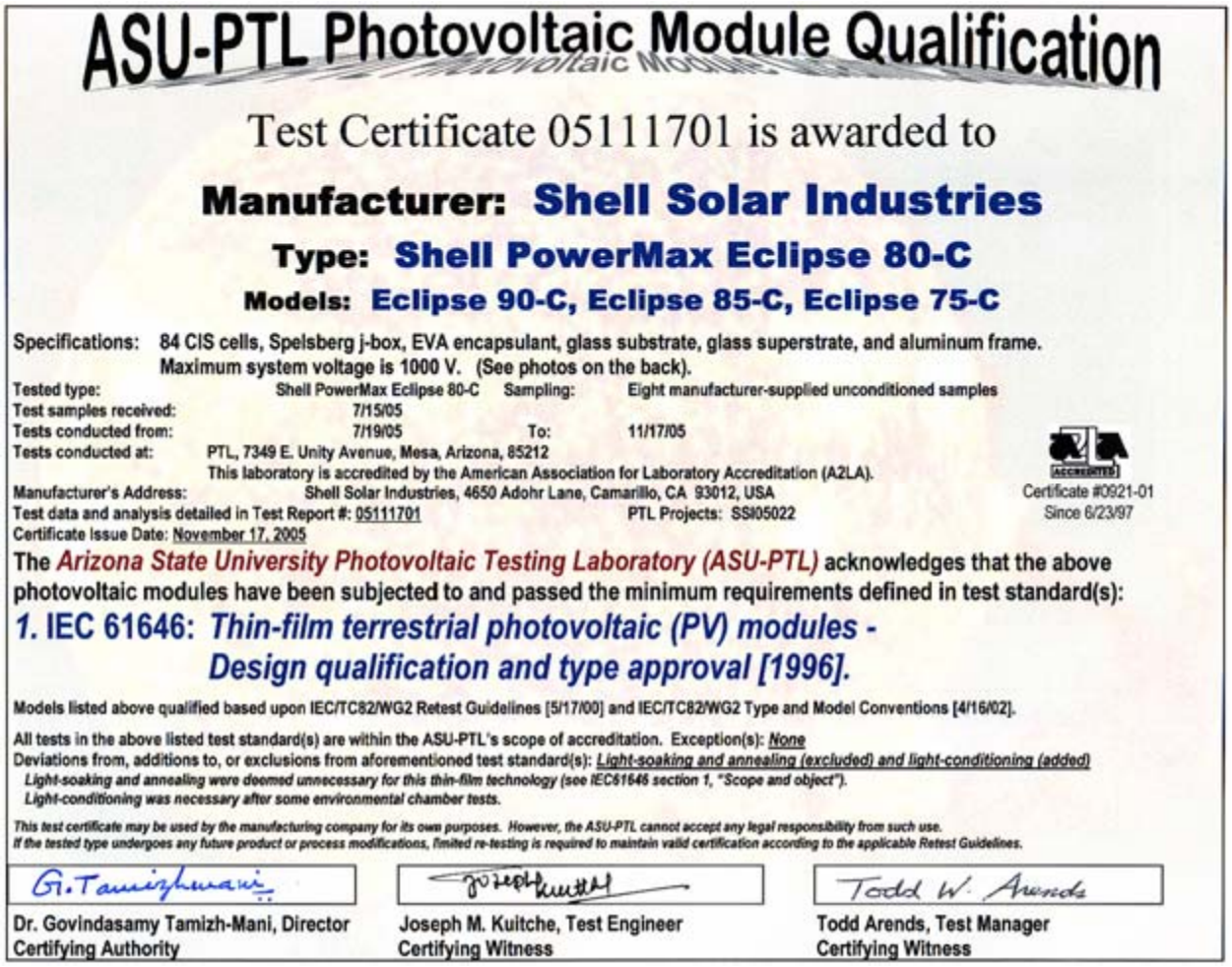
Temperature coefficients for CIS modules appear to vary slightly from module to module. This may be a consequence of the slight variation in band structure from one absorber to another as a function of the degree of sulfur incorporation. It also appears that the temperature coefficients may change slightly with outdoor exposure or stress testing. The values shown in Table 5 are the average of two ST40 modules tested at TUV. We quote these values in our specification sheets, but quite a range of values has been reported.

Table 5. Average temperature coefficients of the IV parameters measured at TUV for two ST40 modules.

Temperature Coefficients	Units	Value	+/-
α Voc	[%/°C]	-0.38	0.02
α Isc	[%/°C]	0.01	0.00
α Pmpp	[%/°C]	-0.49	0.03
α Vmpp	[%/°C]	-0.42	0.09
α Impp	[%/°C]	-0.09	-0.06
NOCT	[°C]	45.4	0.10

Certification testing

CIS modules need to have the same product certifications as crystalline silicon to be competitive. The standard test for certification of CIS modules is the IEC 61646 "Thin-film terrestrial photovoltaic (PV) modules – Design qualification and type approval". The current standard is the First edition, 1996-11. This standard was derived from the IEC 61215 "'Crystalline silicon terrestrial photovoltaic (PV) modules - Design qualification and type approval" (currently released as Edition 2), but was adapted to meet the requirements for testing amorphous silicon modules and therefore lacks appropriate considerations for CIS technology. Extension of this standard to the testing of other thin-film PV technologies is anticipated by the guidance that "Modifications to this test sequence may be necessary due to the specific characteristics of these other new technologies". SSI Eclipse modules have passed the IEC 61646. See certificate in Figure 43.



ASU-PTL Photovoltaic Module Qualification

Test Certificate 05111701 is awarded to

Manufacturer: Shell Solar Industries

Type: Shell PowerMax Eclipse 80-C

Models: Eclipse 90-C, Eclipse 85-C, Eclipse 75-C

Specifications: 84 CIS cells, Spelsberg j-box, EVA encapsulant, glass substrate, glass superstrate, and aluminum frame. Maximum system voltage is 1000 V. (See photos on the back).

Tested type: Shell PowerMax Eclipse 80-C Sampling: Eight manufacturer-supplied unconditioned samples

Test samples received: 7/15/05

Tests conducted from: 7/19/05 To: 11/17/05

Tests conducted at: PTL, 7349 E. Unity Avenue, Mesa, Arizona, 85212

This laboratory is accredited by the American Association for Laboratory Accreditation (A2LA).

Manufacturer's Address: Shell Solar Industries, 4650 Adohr Lane, Camarillo, CA 93012, USA

Certificate #0921-01 Since 6/23/97

Test data and analysis detailed in Test Report #: 05111701 PTL Projects: SSI05022

Certificate Issue Date: November 17, 2005

The *Arizona State University Photovoltaic Testing Laboratory (ASU-PTL)* acknowledges that the above photovoltaic modules have been subjected to and passed the minimum requirements defined in test standard(s):

1. IEC 61646: *Thin-film terrestrial photovoltaic (PV) modules - Design qualification and type approval [1996].*

Models listed above qualified based upon IEC/TC82/WG2 Retest Guidelines [5/17/00] and IEC/TC82/WG2 Type and Model Conventions [4/16/02].

All tests in the above listed test standard(s) are within the ASU-PTL's scope of accreditation. Exception(s): None

Deviations from, additions to, or exclusions from aforementioned test standard(s): Light-soaking and annealing (excluded) and light-conditioning (added)

Light-soaking and annealing were deemed unnecessary for this thin-film technology (see IEC61646 section 1, "Scope and object").

Light-conditioning was necessary after some environmental chamber tests.

This test certificate may be used by the manufacturing company for its own purposes. However, the ASU-PTL cannot accept any legal responsibility from such use.

If the tested type undergoes any future product or process modifications, limited re-testing is required to maintain valid certification according to the applicable Retest Guidelines.

Dr. Govindasamy Tamizh-Mani, Director Certifying Authority	Joseph M. Kuitche, Test Engineer Certifying Witness	Todd Arends, Test Manager Certifying Witness

Figure 43. IEC 61646 certificate for the SSI CIS module Eclipse 80-C family.

Working Group 2 of Technical Committee 82 of the IEC is currently revising the IEC standard. This will be a major revision in the details of the sequence, particularly in the definition of the pass/fail criteria. The old standard required that *relative* measurements, before and after an exposure, be within 5% of each other. The revised standard requires that at the end of the test sequence, all modules measure within 10% of the manufacturer's minimum rated power (an *absolute* measurement), after a sun-soak exposure. The change in the requirements shifts the emphasis of the test from identifying failure mechanisms to verifying product quality. This change will make the standard more general and it should be straightforward for CIS modules to pass this revision.

Test to Failure

Another kind of accelerated test is to subject a module to a test, such as damp heat, until it fails. The number of hours until failure is a gauge of the "robustness" of the design. While it is not possible to predict field lifetime from such experiments, the mechanism of the failure can provide insight into what elements of the design are the weakest and may suggest approaches to improve the package. Experiments with this kind of testing have begun, with an emphasis on comparing the results on CIS modules with silicon modules.

Accelerated testing beyond the normal damp heat test, 1000 hours of exposure to 85ºC and 85% relative humidity, was pursued to identify potential weaknesses in glass/glass package designs (Figure 44). Control modules were exposed for the same duration at 85° C but without humidity thereby allowing distinction between humidity induced effects and solely thermally induced transient effects. There was no significant difference in electrical performance and no visible corrosion after 1000 hours of exposure. Variable corrosion from none to up to 3 cm in from the edge was visible only after 3000 hours in damp heat. One module failed catastrophically after 3500 hours of damp heat exposure due to failure of solder connections and the majority of modules failed after 4000 hours due to this failure mechanism or breakage. The glass/glass package provides protection from humidity ingress well beyond the standard 1000-hour accelerated environmental test.

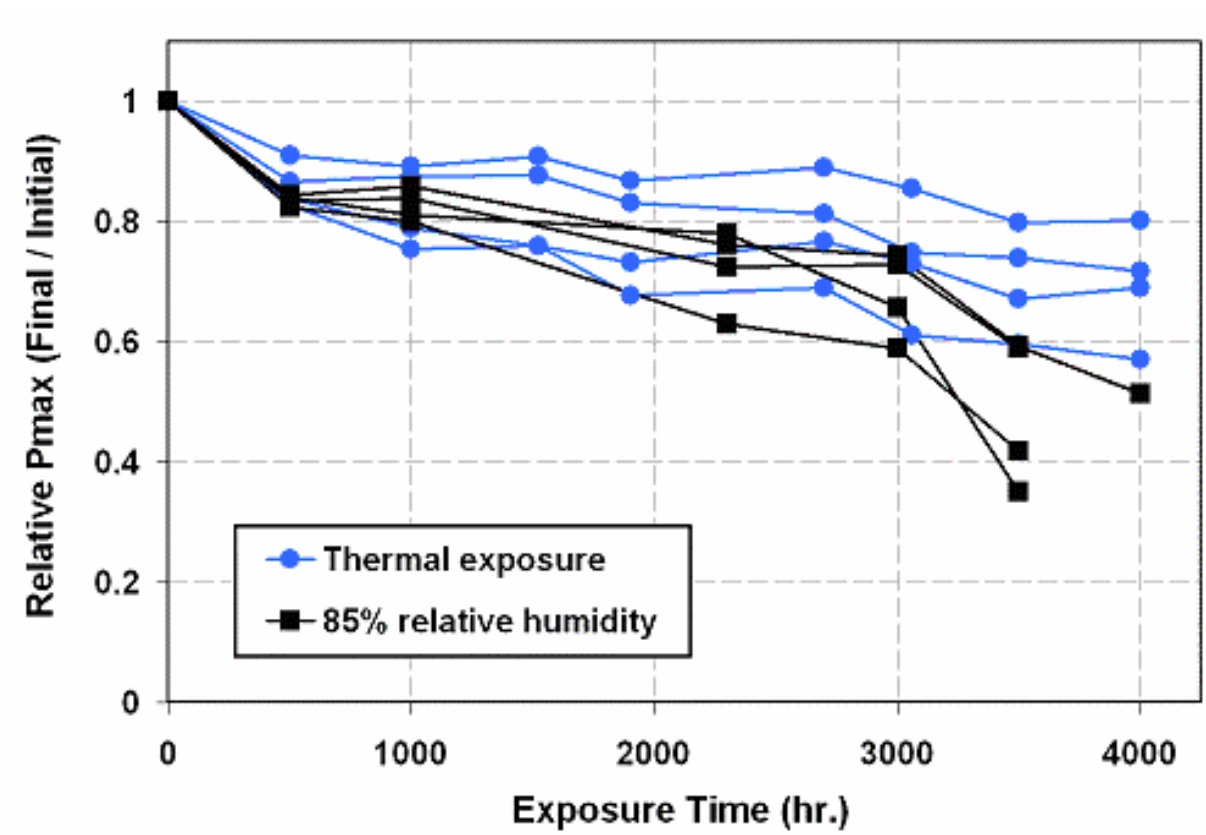


Figure 44. Test to failure shows good protection from humidity ingress well beyond the standard 1000-hour accelerated test.

Outdoor Testing

While IEC certification is generally *necessary* to validate product design from a marketing standpoint, it is clearly not *sufficient* for lifetime prediction. Certification tests may accelerate mechanisms that do ***not*** occur in the field (such as corrosion of coverglass, once a common failure in damp heat that is not observed in the field) and may completely miss mechanisms that ***do*** occur in the field (such as corrosion of circuits or frames). The only way to find out what

kinds of failures will actually occur in the field is to deploy products and see what happens. While such testing may take a very long time, some failure mechanisms may be detected in a relatively short time.

To interpret the data from this kind of testing, we have found that it is most useful to deploy CIS products in a side-by-side arrangement with crystalline silicon products. This provides a kind of internal standard for comparison. While accurate absolute measurements of PV modules is quite difficult, relative measurements provide a simple means of comparing CIS to the de facto industry standard, crystalline silicon.

Outdoor measurements for our CIS modules have shown mixed results. In some tests, CIS modules have shown field degradation, in some cases as high as 2.8% per year [***25***]. Other tests have shown very little change with time. In side-by-side testing with silicon products in both Camarillo and Munich, the long-term behavior of the CIS modules have been at least as good as the silicon controls.

Long-term Outdoor Exposure Testing

SSI has provided NREL with samples of CIS modules since 1988. These modules have been deployed outdoors at the NREL Outdoor Test Facility during all the subsequent years. The modules are measured at periodic intervals, both using the indoor Spire tester and an outdoor tester. Shown below are two sets of data from these modules. The first set of data (Figure 45) was measured indoors, using a Spire 240A; the second set of data (Figure 46) was measured outdoors and corrected to STC. While the trends in the data are similar, they are not identical. As explained above, we believe that the outdoor measurements are more accurate than the indoor measurements.

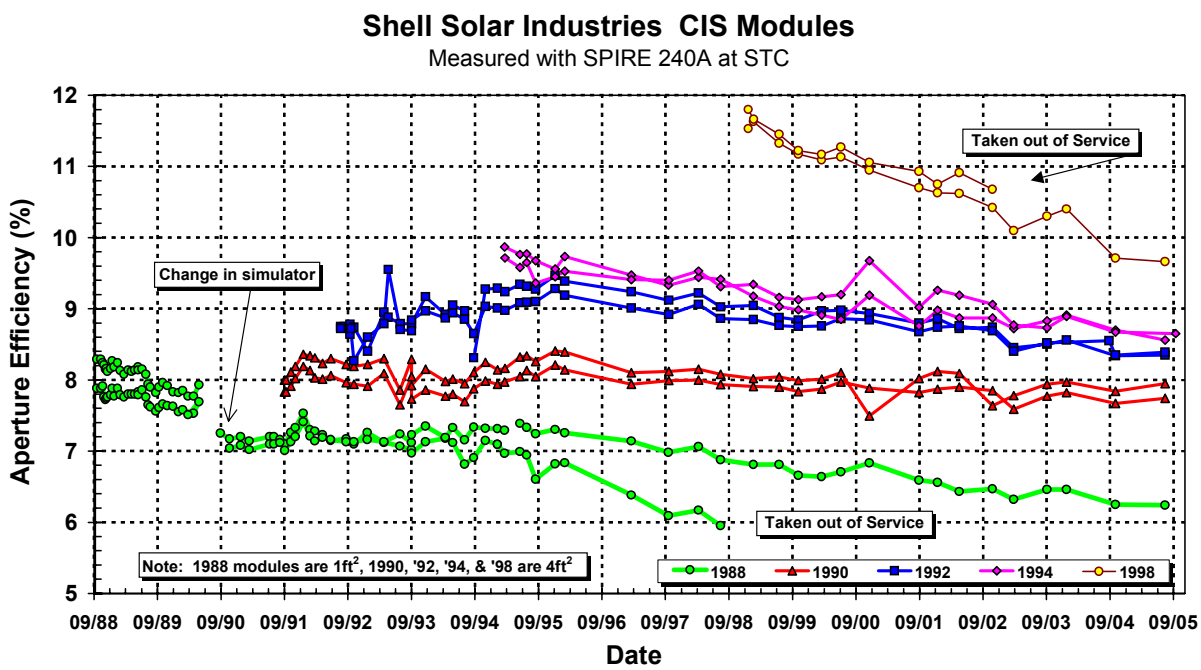


Figure 45. Efficiency measured using an indoor Spire tester on CIS modules deployed outdoors at NREL.

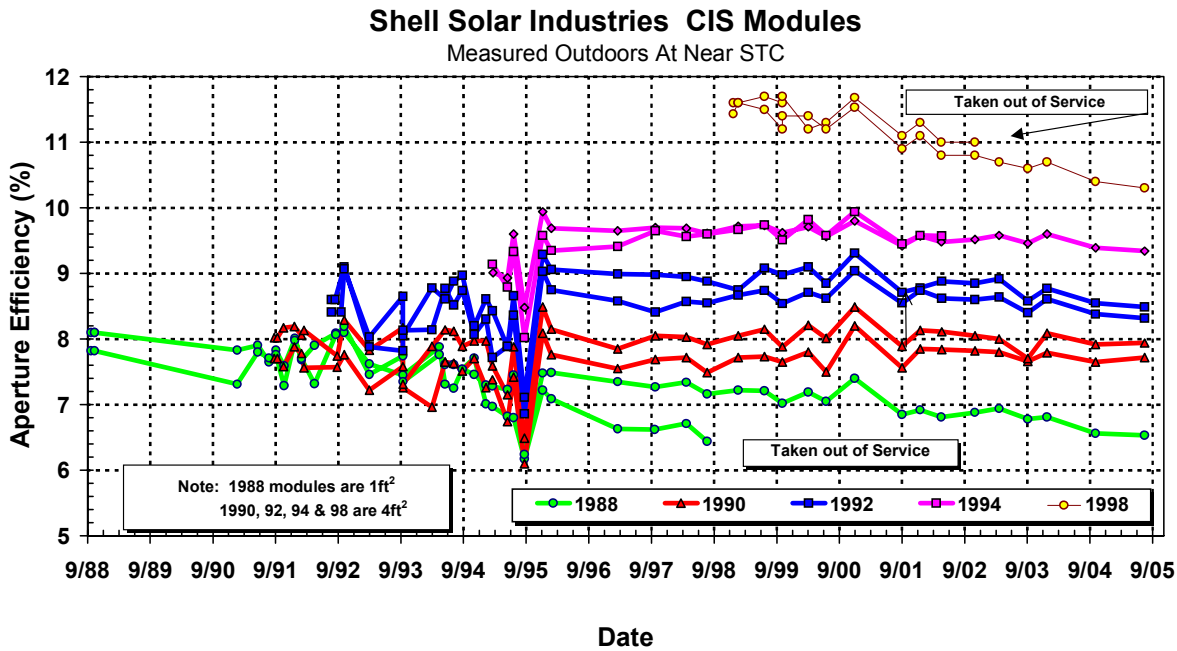


Figure 46. Efficiency measured using outdoors on CIS modules deployed at NREL.

What we see in the outdoor data is the evolution of our CIS products as they became larger and more efficient. The two green curves show data for modules deployed in 1988 that were 1 ft^2 in size and about 8% in starting efficiency. Both modules show loss in efficiency and had visible evidence of yellowing of the EVA by the mid-1990's. One module was taken out of service for additional diagnostics, but no other damage was found. The average annual changes for the modules, based on the outdoor measurements from 1996 to date, are shown in Table 6.

Table 6. Average annual percent change for CIS modules deployed at the NREL OTF, based on outdoor measurements from February 1996 to date.

Deployment Date	Average Change [% per year]
Jan-99	-1.67
Jan-99	-1.48
Mar-95	-0.34
Mar-95	-0.23
Aug-92	-0.49
Aug-92	-0.13
Sep-91	0.18
Sep-91	-0.10
Oct-88	-1.16

Outdoor Exposure Testing, 1-kW Arrays

SSI has provided four 1-kW CIS arrays to NREL. These arrays have been deployed in the Outdoor Test Facility and characterized for extended periods. In each case, a newer generation

of modules has been used to replace the previous design using the same test site. The first two arrays demonstrated stability and that thermally induced transients, which are observed after exposure to high temperatures during accelerated environmental testing, are not observed in the field despite daily and seasonal changes in module temperature.

Data acquisition began on November 18, 1998 for the third 1kW array of prototype modules. The system was comprised of 28 modules with an average aperture efficiency of 11.4% at STC. The aperture area of each module was 0.3651m^2 and of the total array is 10.2 m^2. The array was fixed at a 40° tilt aligned true south and was connected to a resistive load through three maximum power trackers. Continually logged data was corrected for temperature. Only data for incident solar irradiance of between 950 and 1050 W/m^2 was used for array characterization. NREL measurements indicated array performance over 1kW.

With time, the array data indicate that the third array began exhibiting power losses. (See Figure 47) As reported in the Final Report for the previous subcontract [***4***], array data from test sites throughout the country and from individual modules illuminated this issue with the array at NREL. Field failure mechanisms related to particular package designs and errors during production were clearly identified. Additional circuit plate or packaging process variables may have affected durability during particular production timeframes; when losses were observed, the losses correlated with date of deployment or prototype module configuration. For comparison, crystalline silicon arrays typically show annual losses of 1 to 2 percent per year [***26***, ***27***].

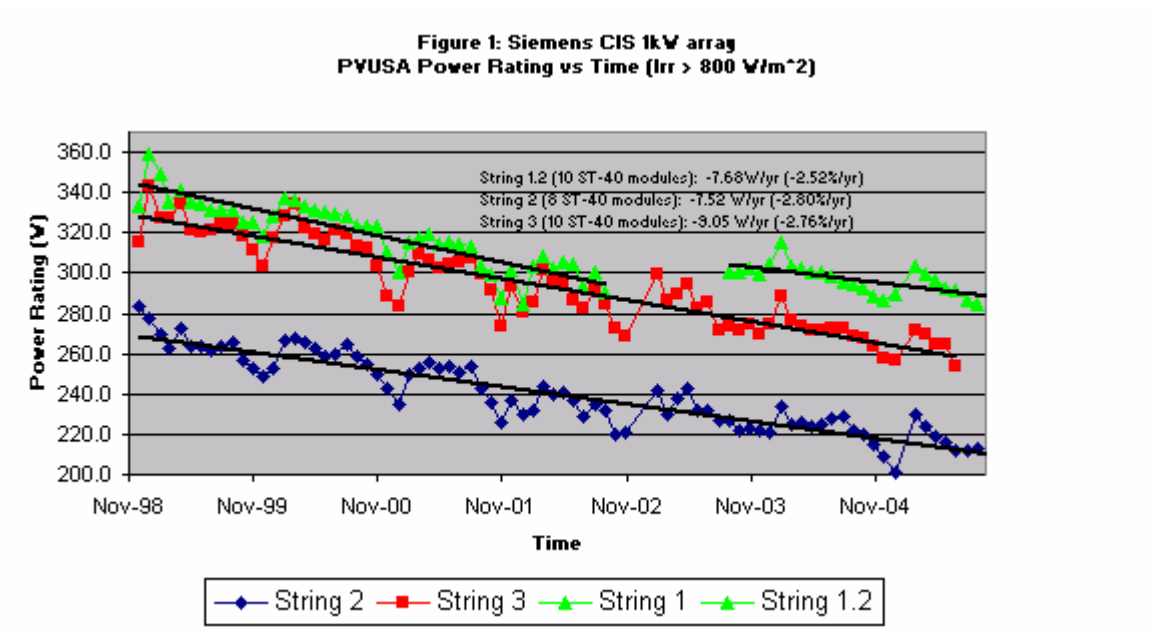


Figure 47. Outdoor measurements of the third CIS array delivered to NREL. Power losses of 2.5 to 2.8 percent per year were observed.

Fourth 1-kW Array

As deliverables for the previous subcontract, SSI shipped 22 Eclipse 80-C prototype modules to NREL for deployment as a 1 kW array and for other testing at the OTF. As seen in following picture, Figure 48, the array consists of two strings of seven modules and is oriented at a 40-

degree tilt facing true south. The modules are oriented so that the long thin cells are oriented vertically thereby avoiding shadowing problems associated with dirt buildup previously seen for deployment with cells in the horizontal orientation and aggravated by an earlier module design with a deep frame (which concentrated the dirt over the edge cells).

Figure 48. The fourth 1-kW array provided to the NREL Outdoor Test Facility. The array is comprised of 14 Eclipse 80-C modules.

NREL IV measurements of the array are shown in Table 7. These modules are Eclipse 80-C designs, which have a frame aperture and a window aperture defined by a screen-printed mask on the coverglass. The following areas have been used for calculating the efficiency:

Inside the frame	8281 cm^2
Aperture defined by the coverglass mask	7358 cm^2
Aperture defined by the circuit dimensions	7275 cm^2

Table 7. IV measurements of the modules provided to NREL as a deliverable under this subcontract.

	Area (cm^2)	Voc (V)	Isc (A)	FF (%)	Vmax (V)	Imax (A)	Pmax (W)	Aperture Eff. (%)
Average for 18 modules								
SPIRE 240A	8281	45.3	2.76	64.5	33.4	2.41	80.6	9.7
LACSS SpectroLab X200	"	45.3	2.65	64.9	33.8	2.30	77.9	9.4
OUTDOORS SOMS	"	45.9	2.78	64.9	34.3	2.40	82.9	10.0
SSI Measurements								
Aperture area	7275	45.1	2.83	64.3	33.2	2.47	82.0	11.3
Front glass aperture	7358							11.1
Inside frame	8281							9.9
Individual module measurements								
SPIRE 240A	7331	45.7	2.77	65.0	34.2	2.41	82.3	11.2
LACSS SpectroLab X200	"	45.6	2.66	64.9	34.3	2.29	78.8	10.7
OUTDOORS SOMS	"	46.3	2.80	64.8	34.9	2.38	83.9	11.4
SPIRE 240A	7376	46.6	2.78	65.3	34.6	2.44	84.4	11.4
LACSS SpectroLab X200	"	46.2	2.63	66.0	34.7	2.31	80.1	10.9
OUTDOORS SOMS	"	46.9	2.77	66.2	35.2	2.38	86.1	11.7

Communication with Jill Adelstein (NREL) provided array power measurements based on PVUSA measurement criteria. For these measurements with the array at the nominal operating temperature rather than for correction to standard test conditions at 25ºC, three measurements made between January and March, 2006 averaged 989 W.

Effects of rain washing

SSI deployed a 245kW CIS array on the rooftop of one of its manufacturing buildings [***28***]. This array is monitored for energy delivery and the company is compensated for the excess power produced. The buildings are located next to agricultural fields and the arrays are mounted at a very shallow angle. The effect of rain washing the dirt off the modules can be seen in Figure 49. The loss in power caused by the soiling of the modules is estimated at 60% based on the step increase after they were cleaned. Note that these modules are installed in the "landscape" orientation with a nearly horizontal tilt angle. As a consequence, dirt accumulation is severe, obscuring entire cells and groups of cells.

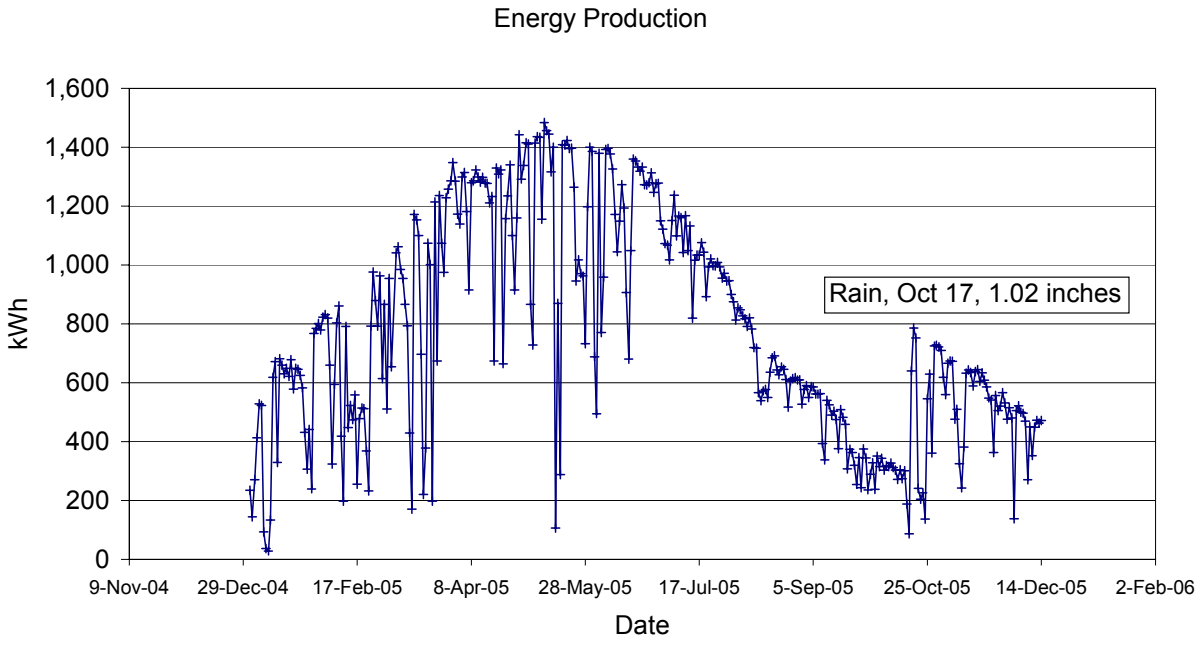


Figure 49. Daily energy production from the 245-kW rooftop array. It rained 1.02 inches of water on October 17, 2005, resulting in a dramatic increase in production.

Side-by-Side Arrays

Shell Solar has set up two side-by-side arrays to directly compare CIS and silicon technologies. One is located on the grounds of the Shell Solar R&D facility in Munich Perlach [***29***], where single-crystal silicon, polycrystalline silicon and CIS modules are monitored for their daily energy output (Figure 50).

Figure 50. Photo of the outdoor test facility in Munich-Perlach. Several technologies are compared in a side-by-side arrangement.

The energy production data was analyzed by calculating the ratio of the energy produced by each array relative to the energy produced by a silicon array (the SE160 modules). From the chart below, Figure 51, the energy produced by the CIS array is within 1% of the energy produced by the silicon array over the lifetime of the experiment.

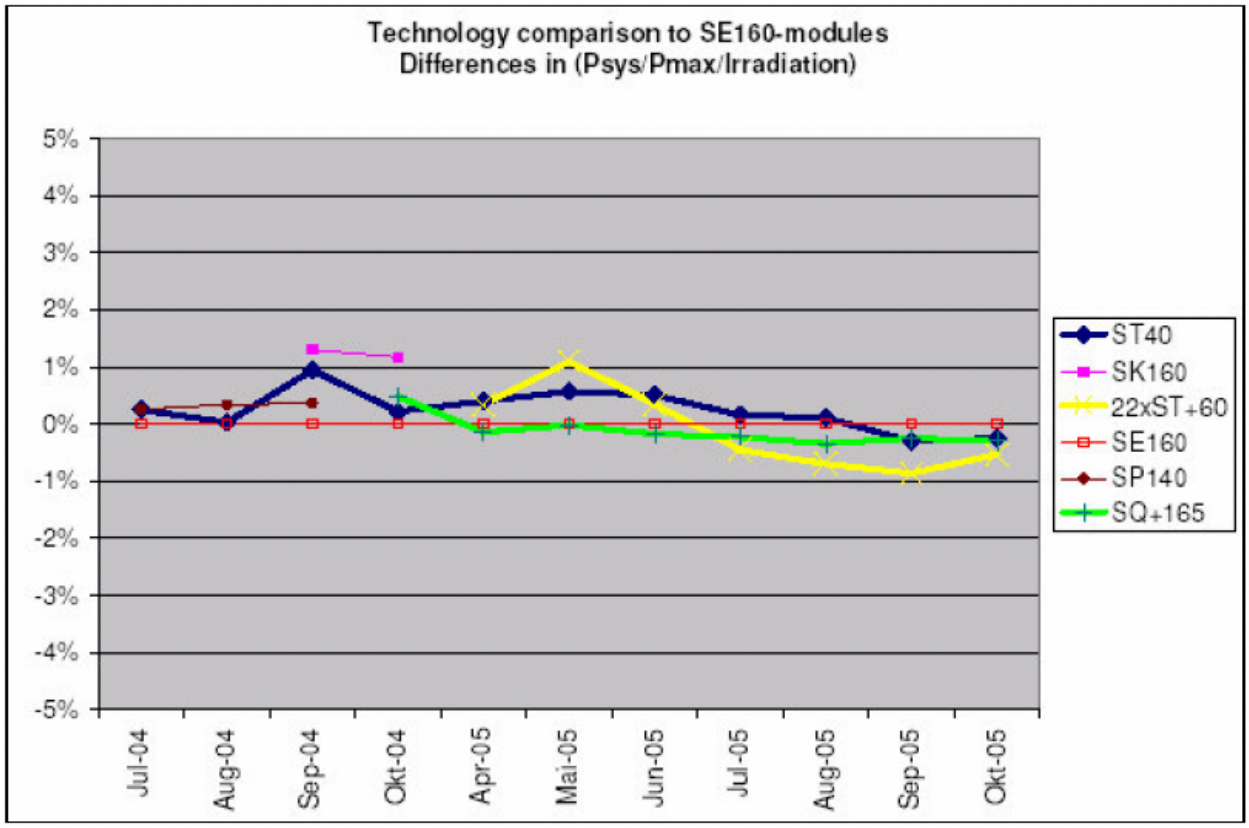


Figure 51. The ratio of the energy produced by several technologies compared to the energy produced by a silicon array (the SE 160 array). The CIS ST40 modules show no difference from the silicon array within 1%.

In another side-by-side test, an array of 80 ST36 modules (2.88 kW) and 40 SP75 single-crystal silicon modules are installed on the roof of the R&D building in Camarillo. (see Figure 52). Two power trackers log the energy output from each array. The ratio of the energy produced by the CIS array is then normalized by the size of the arrays and compared to the energy produced by the silicon array.

Figure 52. On the left is a 2.88 kW CIS array of 80 ST36 modules. On the right is a 3.0 kW CZ array of 40 ST75 modules.

This data is shown in Figure 53. The offset in the energy production by 20% is likely due to differences in the initial rating of the two products. The increase that starts in June of 2005 is not yet explained.

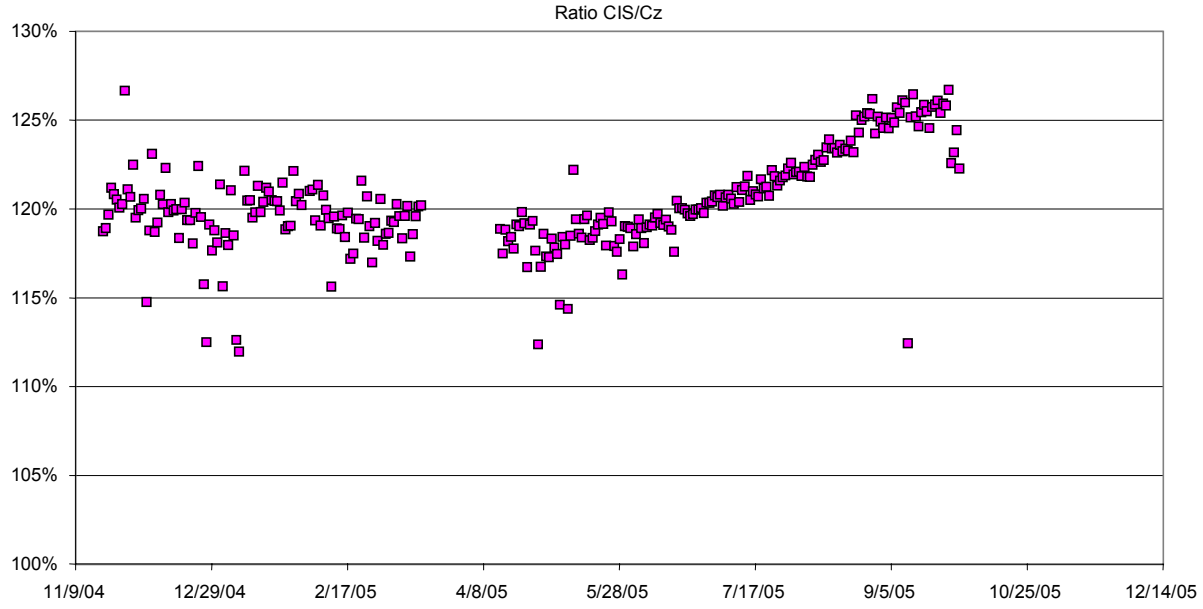


Figure 53. The ratio of the energy produced by a CIS array compared to a silicon array in a side-by-side test on the roof of the R&D building in Camarillo.

Warranty considerations

Typical PV module warranties guarantee a minimum amount of power for a fixed period of time. For example, in addition to the 2-year warranty on materials and workmanship, the warranty on SSI CIS modules reads as follows:

For the PV-modules (excluding the inverter/converter) ST5, ST10, ST20, ST36, and ST40, Shell Solar additionally warrants:

If, within ten (10) years from date of sale to the Customer any PV-module(s) exhibits a power output less than 90% of the minimum Peak Power at STC as specified at the date of delivery in Shell Solar's Product Information Sheet, provided that such loss in power is determined by Shell Solar (at its sole and absolute discretion) to be due to defects in material or workmanship, Shell Solar will replace such loss in power by either providing to the Customer additional PV-modules to make up such loss in power, or by repairing or replacing the defective PV module(s), or by refunding the Purchase Price taking into account a yearly depreciation of ten (10)% of the Purchase Price, at the option of Shell Solar.

In other words, if a customer buys an array of modules from us, and the power of the array falls below 90% of the specified minimum power, we are responsible for making up the lost power. The minimum power for our CIS modules is 90% of the rated power. For an ST40 module, the rated value is 40 watts and the minimum power is 36 watts. If the power falls below 32.4 watts within 10 years, we will make up the missing power.

Many PV module warranties today have been extended to over 20 years. While this makes them easier to sell by providing a basis for calculating a long-term financial return, there have been very few modules (of any technology) which have been in the field long enough to determine their service lifetimes. Additional field deployment and monitoring is needed to establish a better understanding of lifetime prediction.

Conclusions

Outstanding progress has been made in the initial commercialization of high performance thin film CIS technology. The following are highlights of accomplishments during this subcontract:

- Executing the CIS process continued to demonstrate process predictability.
- ST40 (40 W) products were initially produced and then obsoleted with production of the Eclipse 80-C, (80 W) product fabricated using two 1x4 ft. circuit plates.
- SSI Eclipse 80-C modules with a new glass/glass package passed ALL accelerated testing and test standards defined by the IEC 61646 standard and received IEC qualification.
- The peak of the distribution for 40 W single circuit plate ST40 modules produced during this subcontract period is 11.25% with a mean efficiency of 11.1%. The standard deviation of the distribution is less than 1% (corresponding to only 8.6% of the mean).
- The peak of the distribution for Eclipse 80-C modules is 11.0% with a mean efficiency of 10.8%. The standard deviation of the distribution is less than 1% (corresponding to only 7% of the mean).
- Electrical yield for the Eclipse 80-C product line exceeded 95%. Line yield, defined as the ratio of the area of product produced divided by the area of glass started through the production line, increased from about 60% in 2000 to about 85% in 2002. High line yield was again demonstrated in this subcontract period.
- High efficiency cadmium-free CIS modules were demonstrated with performance indistinguishable from baseline modules (incorporating CdS) after outdoor light exposure.
- SSI accomplishments prior to 2003 far exceed the 2003 DOE EERE Multi-Year Technical Plan technical target of 8% module conversion efficiency for thin-film modules. SSI delivered modules to NREL to meet the Joule goals for thin films for each year from 2003 through 2006.
- Extended accelerated testing of the glass/glass package at 85ºC and 85% RH demonstrated protection from humidity ingress well beyond the standard 1000-hour exposure.
- The long-term behavior of CIS modules deployed in side-by-side testing with silicon products has demonstrated performance that is at least as good as the silicon controls.
- Process development activities during this subcontract included: improved CIG ratio control, lower cost indium targets, increased gallium content in the absorbers, simplified molybdenum deposition, improved mechanical scribing and improved lead attachment.
- Deliverables for this subcontract included 20 Eclipse 80-C modules for evaluation, 8 ST10 modules for exhibits, 36 six inch square mini circuits for lamination experiments at NREL, and samples with laser edge deletion for surface roughness analysis at NREL related to packaging development.
- Long-term outdoor stability has been demonstrated at NREL where multiple prototype package designs have undergone testing for over seventeen years.

Further device and production R&D can lead to higher efficiencies, lower cost, and longer product lifetime. Production volume, efficiency and yield data supports attractive cost projections for CIS. Prerequisites for commitment to large-scale commercialization have been demonstrated at successive levels of CIS production. Remaining R&D challenges are to scale the processes to even larger areas, to reach higher production capacity, to demonstrate in-service

durability over longer times, and to advance the fundamental understanding of CIS-based materials and devices with the goal of improvements for future products.

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Shell Solar Industries
4650 Adohr Lane
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14. ABSTRACT *(Maximum **200 Words**)*

The primary objectives of this subcontract were to: address key near-term technical R&D issues for continued improvement in thin-film PV products; continue process development for increased production capacity; pursue long-term R&D contributing to progress toward the MYTP goals for 2020 to increase the conversion efficiency to 15% and reduce module manufacturing costs to less than $50/m^2$, thus enabling PV systems with a 30-year lifetime at an installed cost of under $2.00/W; and advance the understanding of the requirements needed to achieve better thin-film PV cell and module performance, greater reliability and market acceptance, and investigate materials systems and new devices that can improve the cost/performance ratio of future thin-film PV factories. The demonstrated and maintained high production yield is a major accomplishment supporting attractive cost projections for CIS. Process R&D at successive levels of CIS production has led to the continued demonstration of the prerequisites for commitment to large-scale commercialization. Process and packaging R&D during this and previous subcontracts has demonstrated the potential for further cost and performance improvements.

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