Low Thermal Resistance IGBT Structure

Daniel Benhammou
Email: daniel_benhammou@nrel.gov
Phone:303-275-4458
National Renewable Energy Laboratory

Vahab Hassani (NREL)

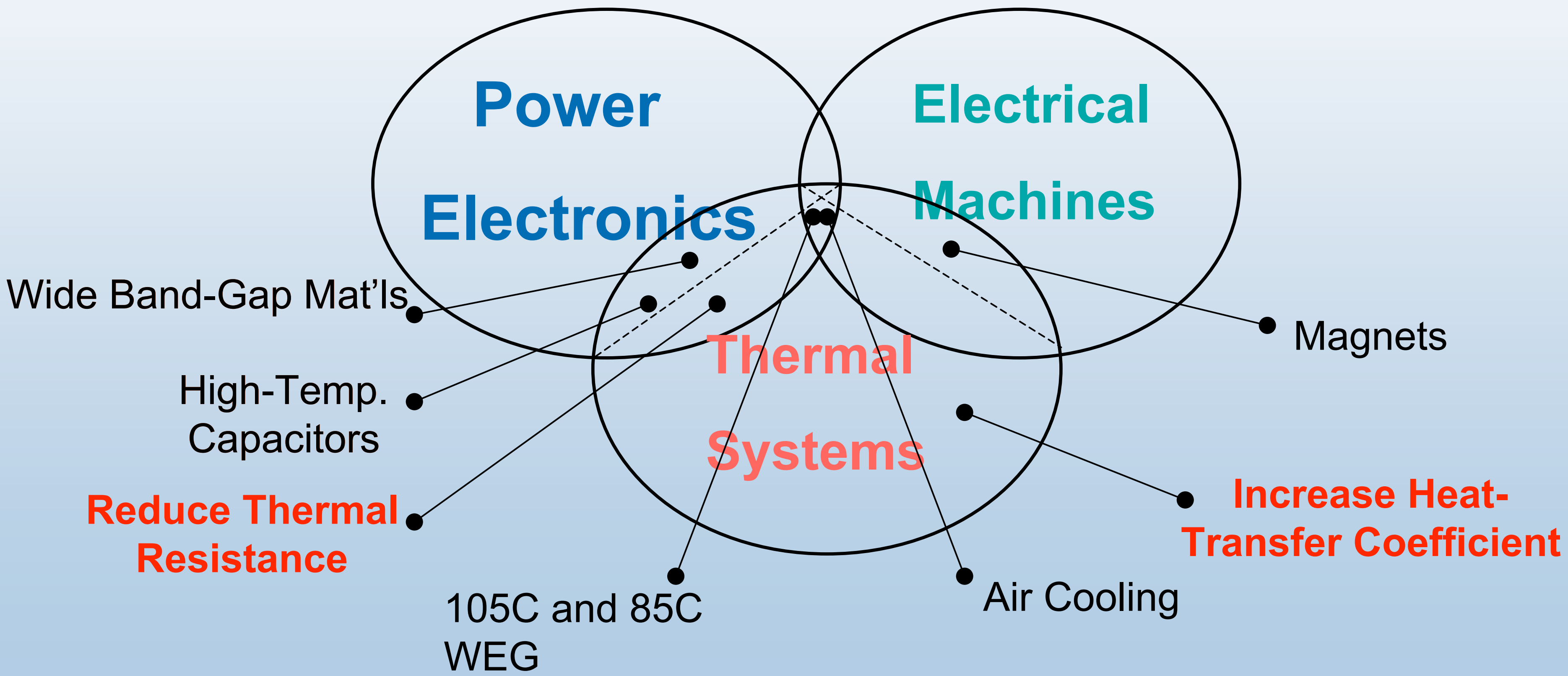
FY05 Budget: $ 400K
FY06 Budget: $ 500K
Project Duration: FY05 to FY06

FreedomCAR APEEM FY05 Wrap-up/FY06 Kick-off Meeting
Oak Ridge National Laboratory
National Transportation Research Center

November 2, 2005

Where Does This Project Fit?

Low Thermal Resistance IGBT Structure

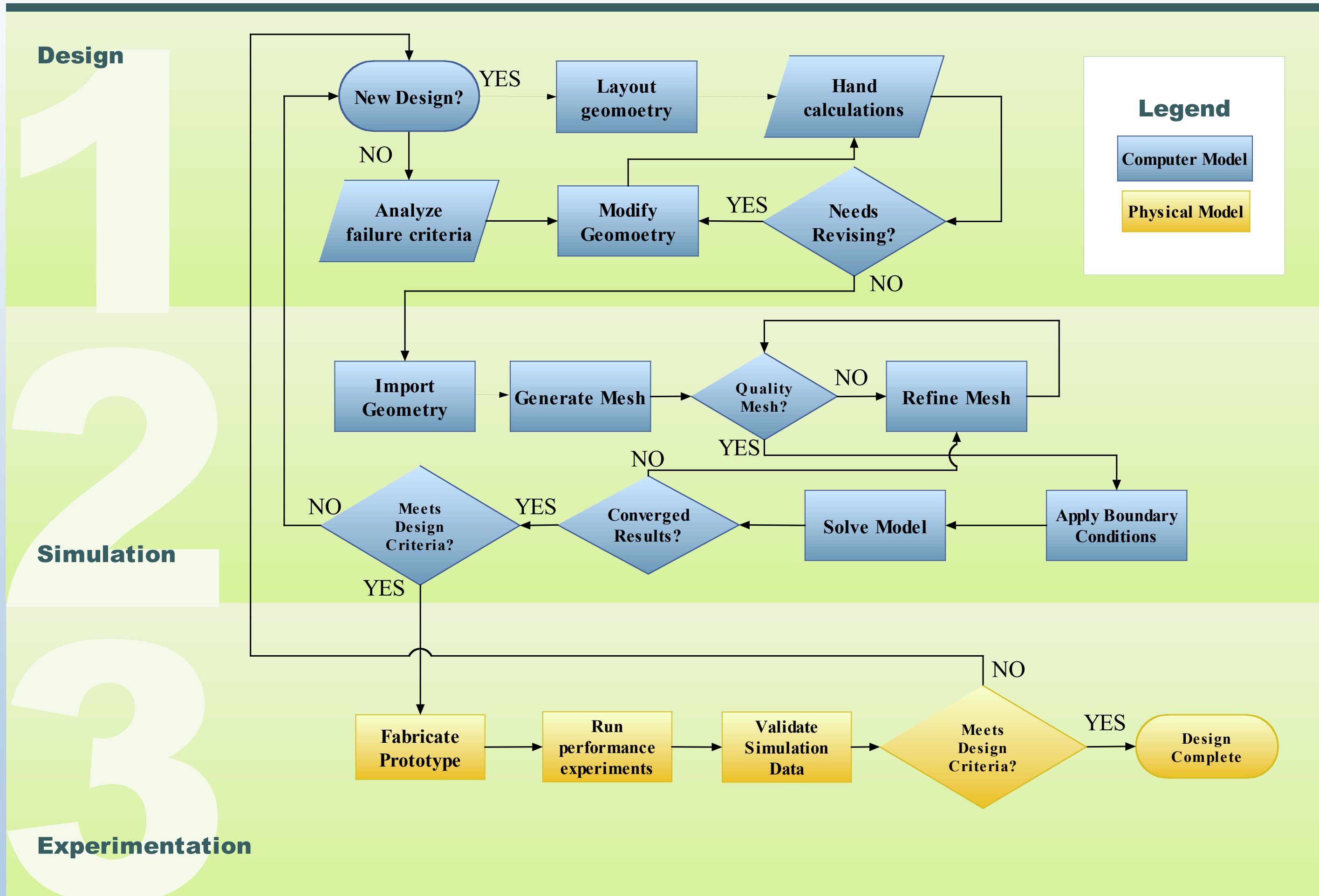


What is This Project?

- Maximize heat transfer from IGBT structures by removing layers of greatest thermal resistance. By doing this, we can cool inverter power electronics by means of jet impingement cooling directly on DBC.

Technical Approach

Design Process



Technical Approach

Design Simulation Experimentation	How do we address positives and negatives?
Positives • Cost Effective • Fewer physical prototypes	•Modeling capability allows multiple design revisions without the high cost of fabrication and experimental validation. •Low thermal resistance IGBT structures provide a cost effective solution to meet DOE program goals.
Negatives • Time Consuming	Multiple design iterations and numerical models result in longer lead time to first run prototypes.

Goal

- Reduce thermal resistance between silicon die and coolant
- Produce a fully operating prototype ready for commercialization
  - 105°C inlet temperature
  - 125°C maximum die temperature
  - Heat flux: 200 W/cm^2

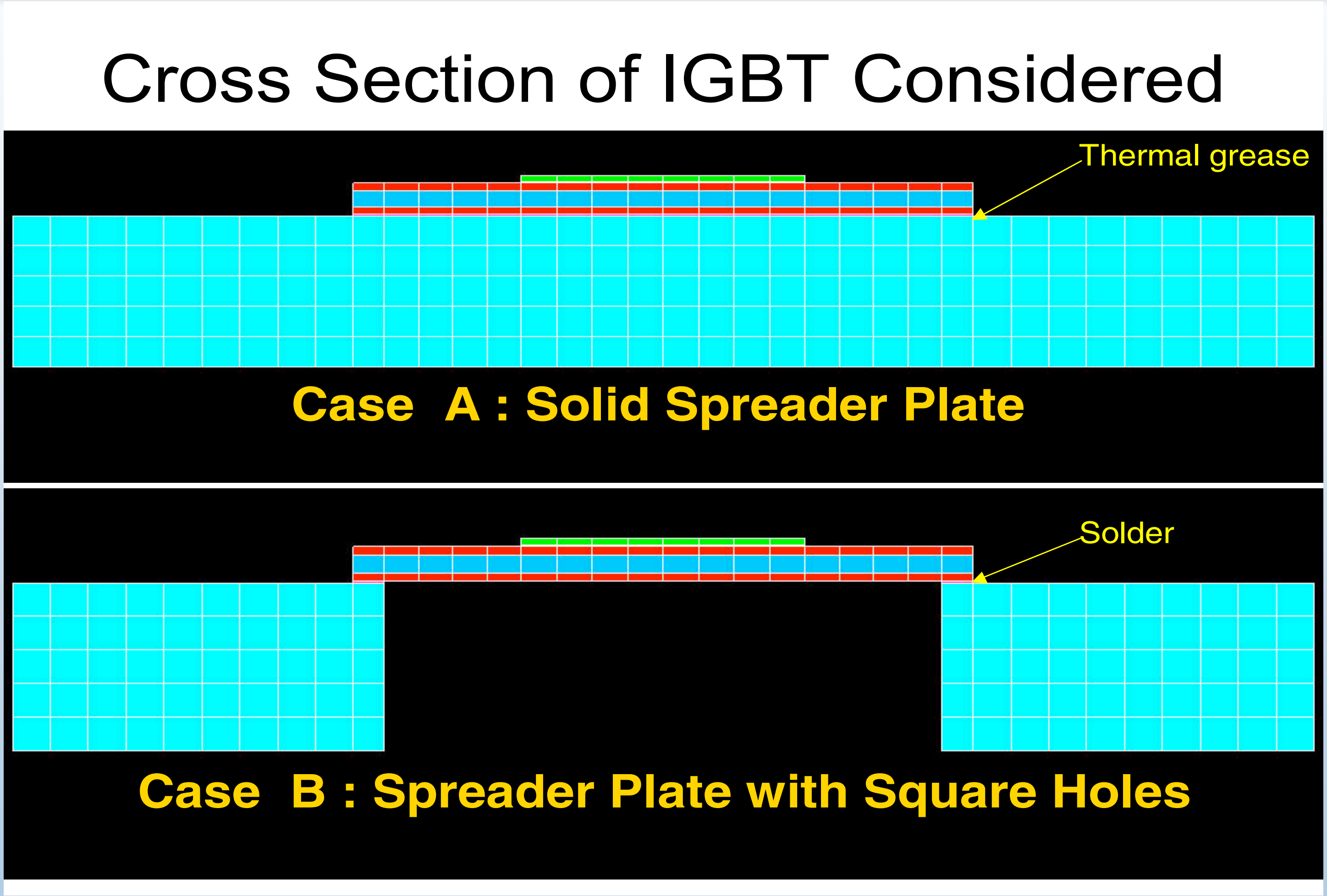
Approach for FY05

- Establish industry partner
- Model physics
  - Structural analysis
  - Thermal analysis
  - CFD simulations
- 6 resistor proof of concept
- Iterate design

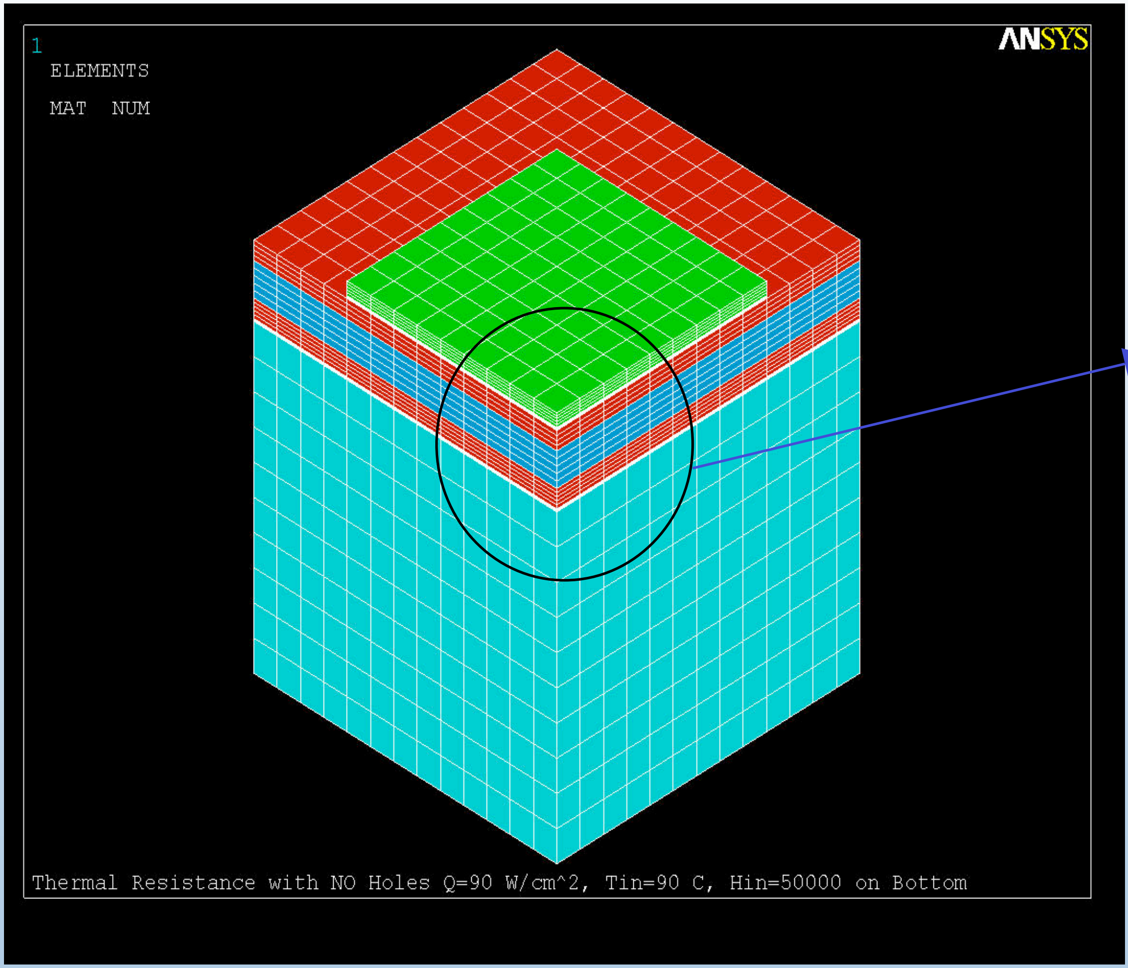
Major Accomplishments for FY05

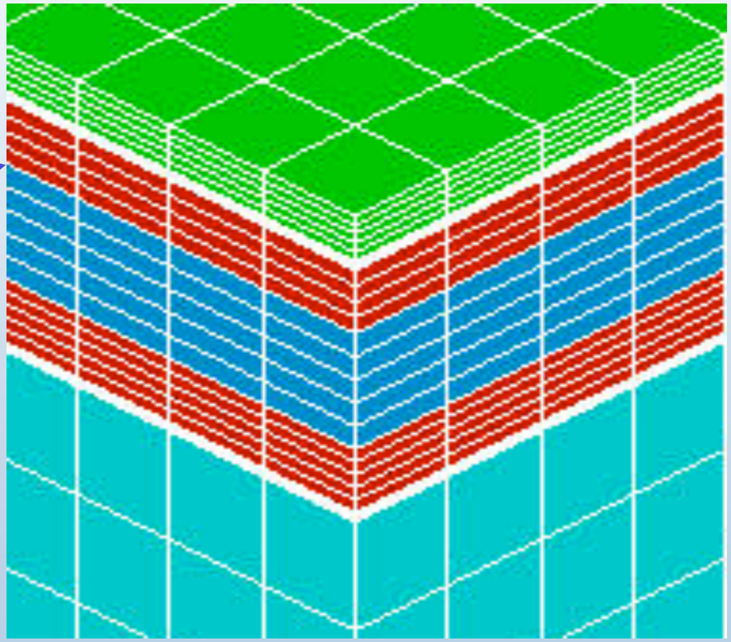
- CRADA in place with Semikron
- Numerical simulations corroborate feasibility of cut-through IGBT structure
- Experimental High Heat Flux (HHF) test loop built for experimental validation
- Currently in 8^{th} generation of design

Low Thermal Resistance IGBT Structure



Conventional IGBT Structure





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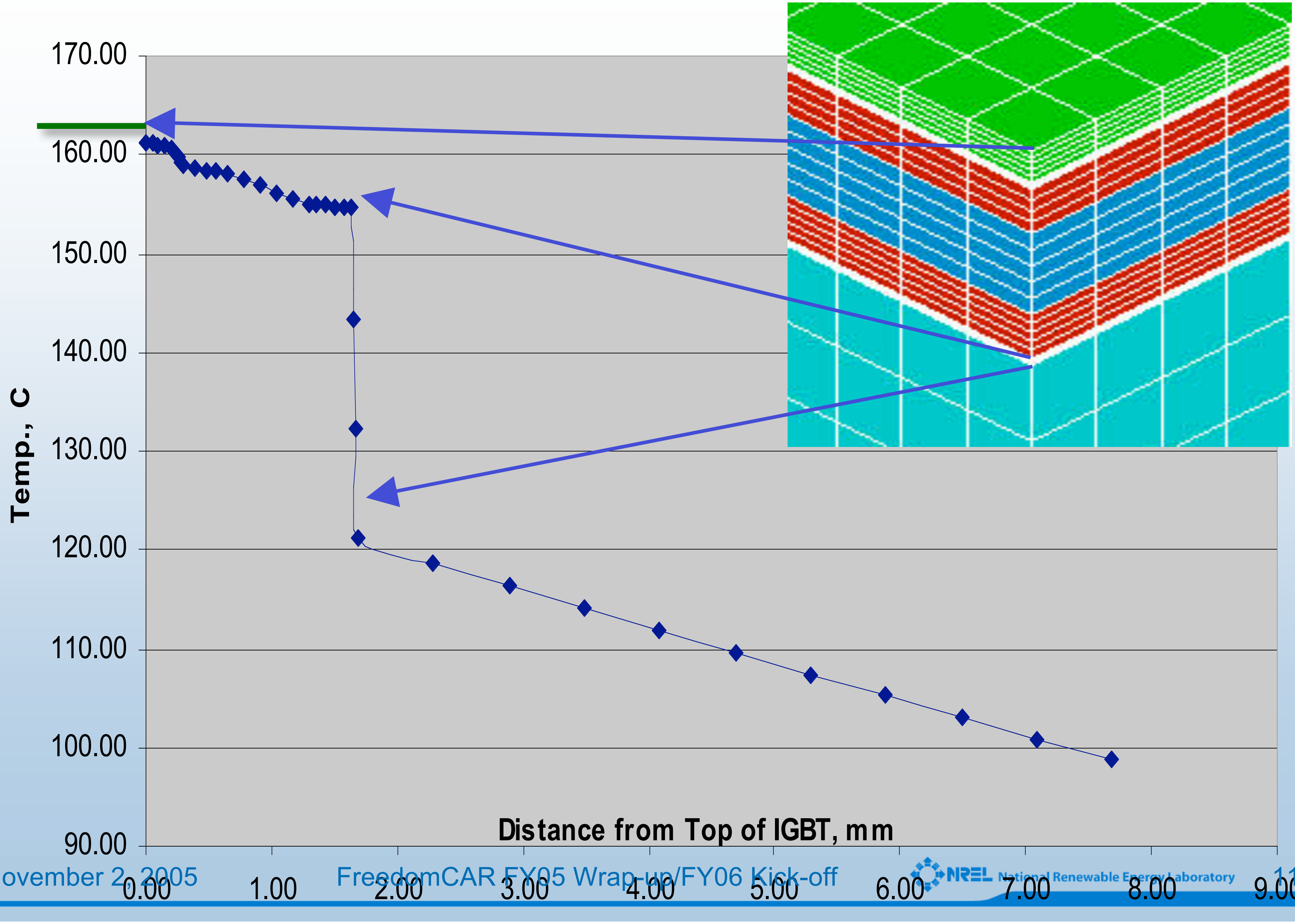
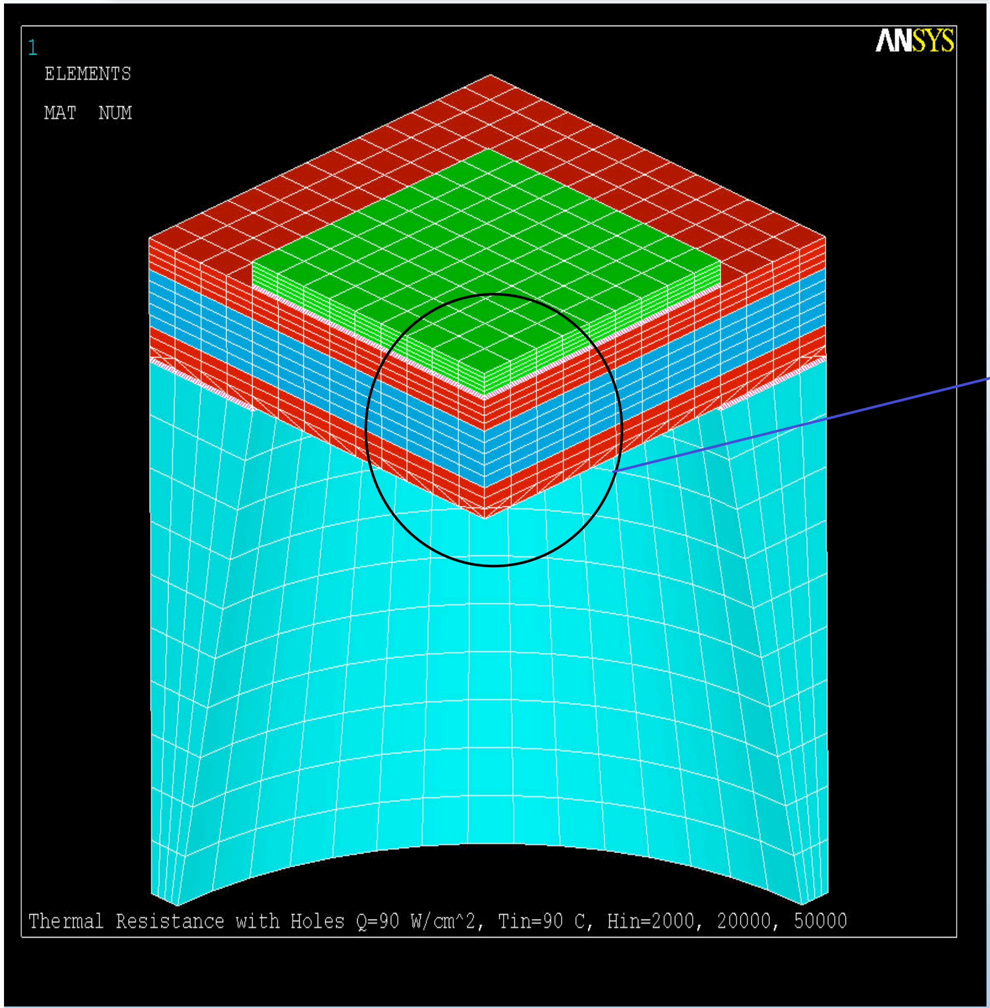
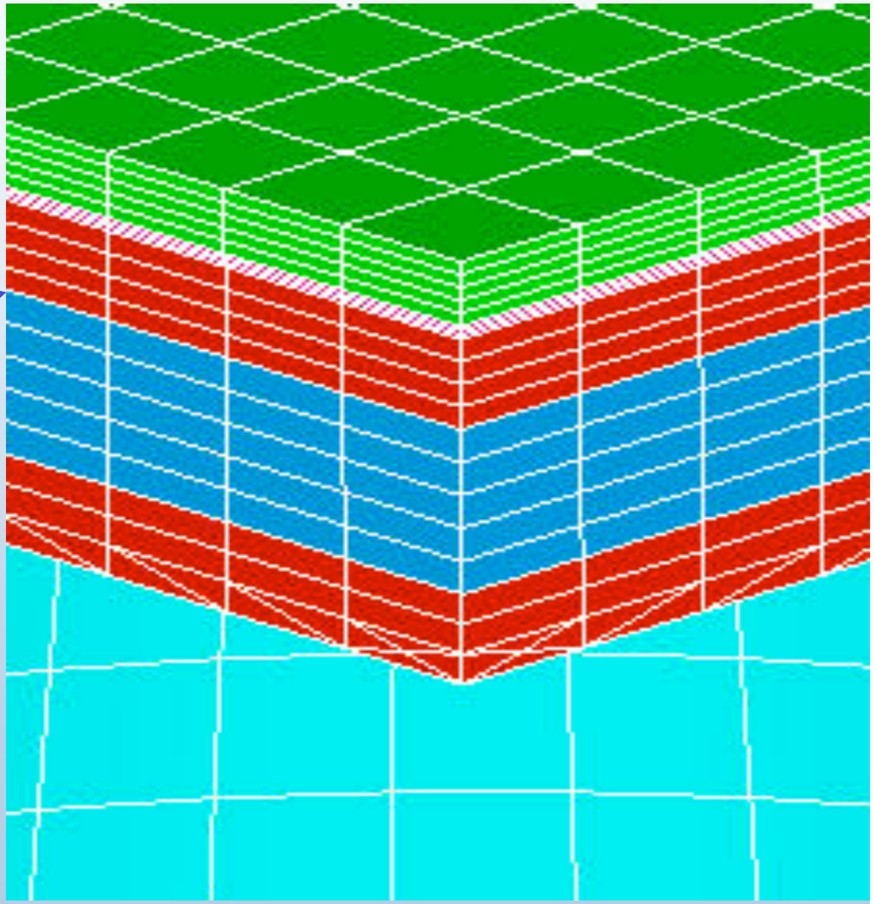
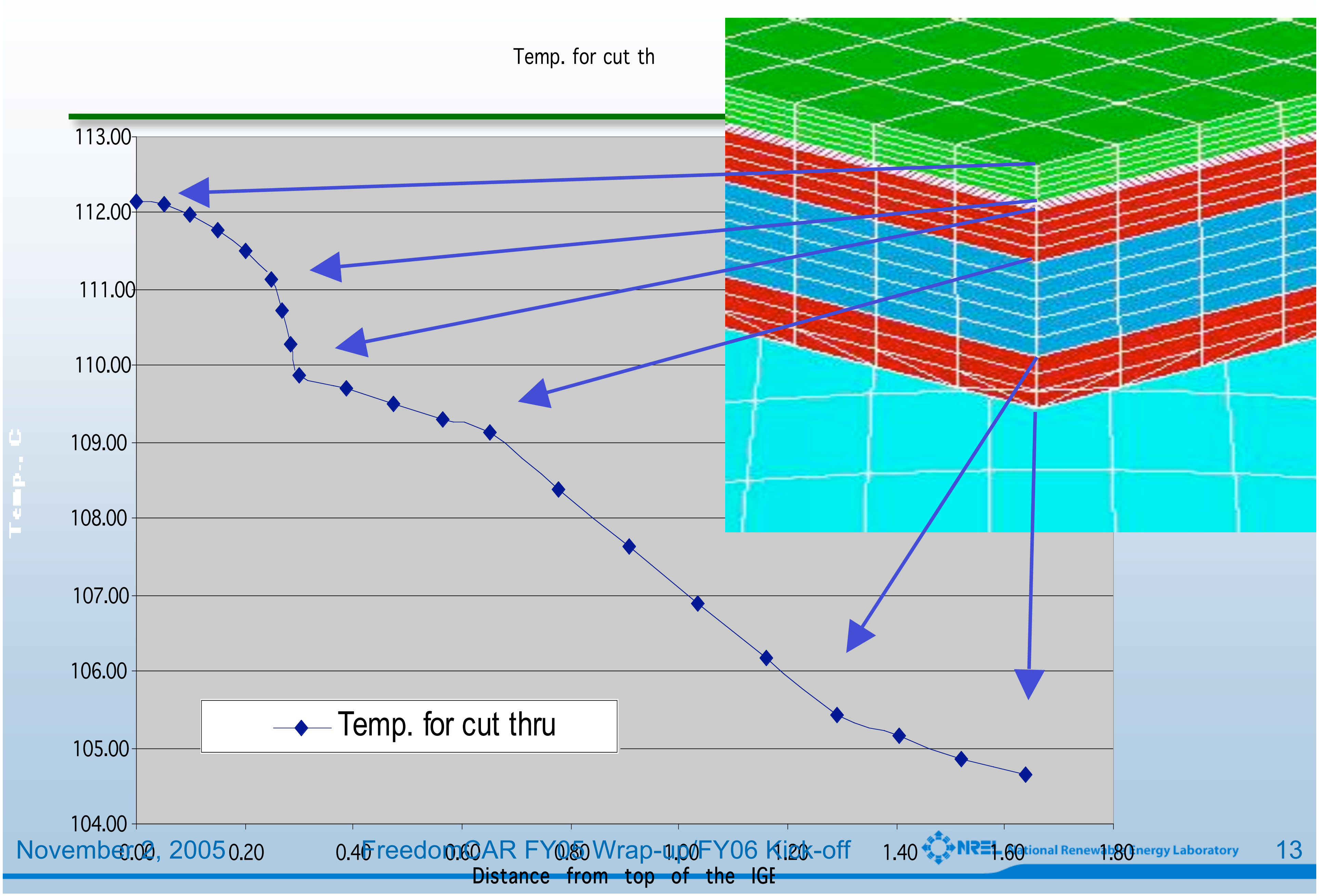


Low Thermal Resistance IGBT Structure

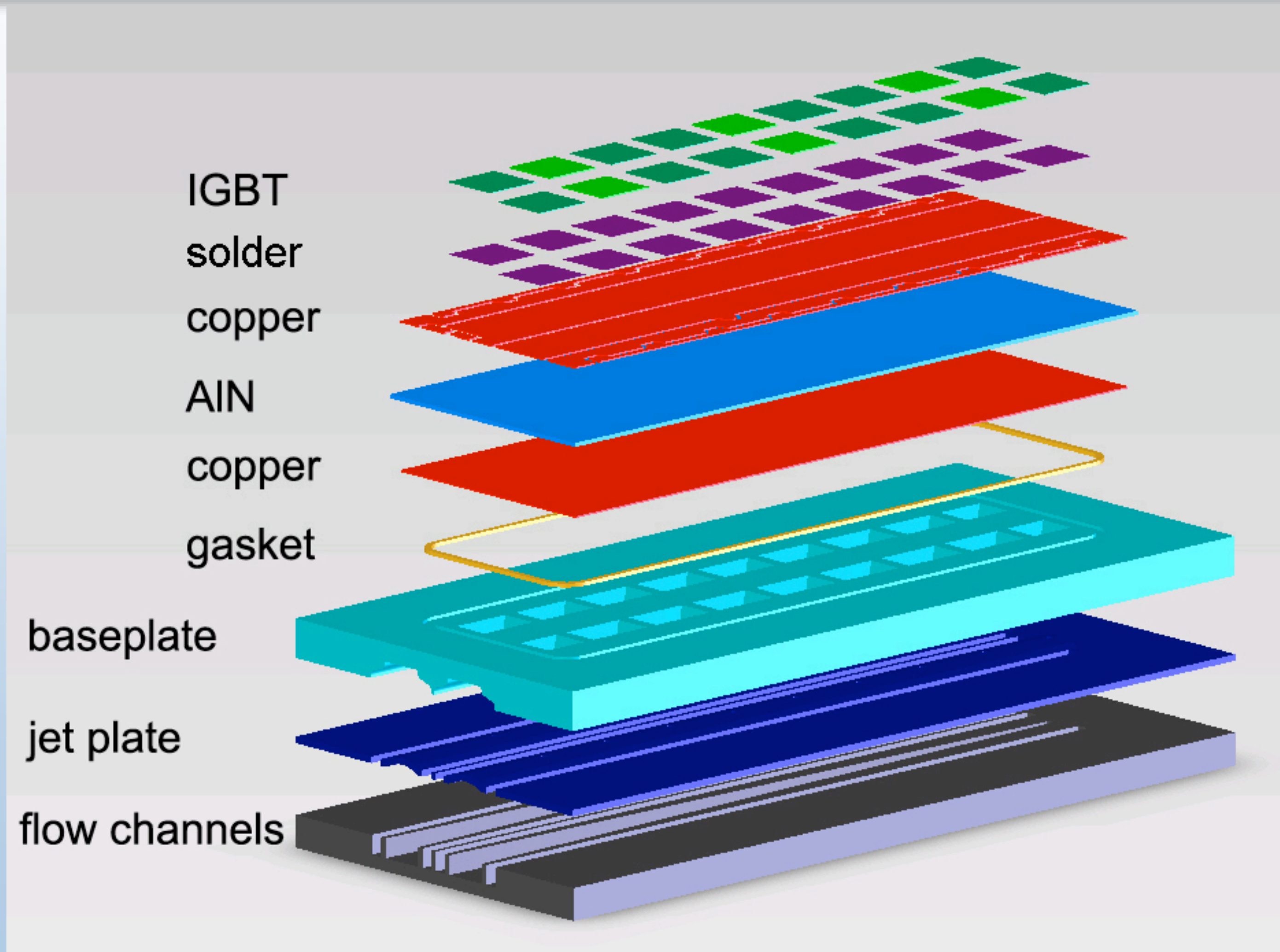




Low Thermal Resistance IGBT Structure

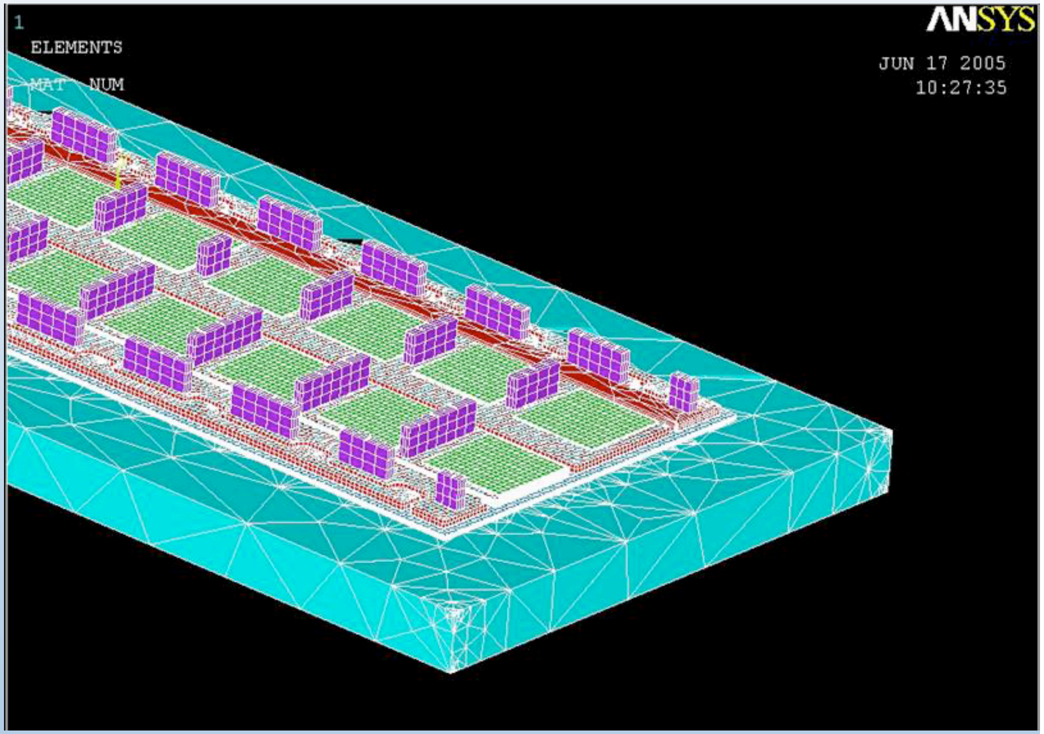


Exploded view of design



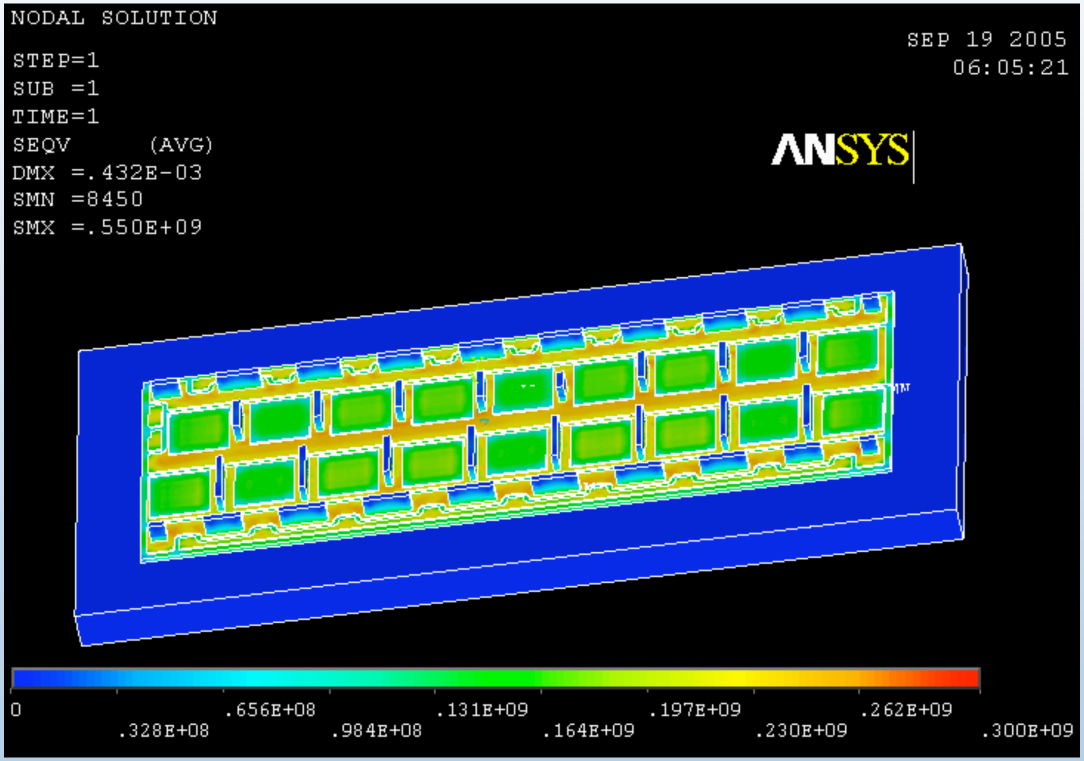
Finite element mesh of Semikron inverter phase

- Mesh must represent physical body
  - Refinement needed in areas of steep gradients
- Optimize mesh to reduce computation time

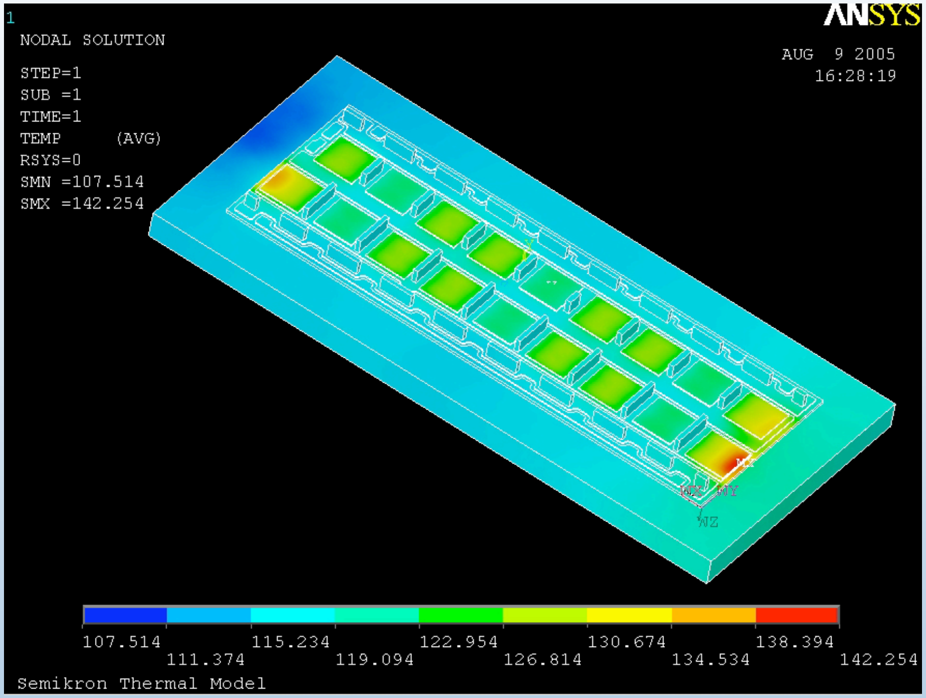


Structural Analysis

- Analyze stress
  - Applied
  - Thermally induced
- Boundary conditions
  - T_{ref} = 125°C
  - T_{unif} = -40°C
  - P = 15 MPa



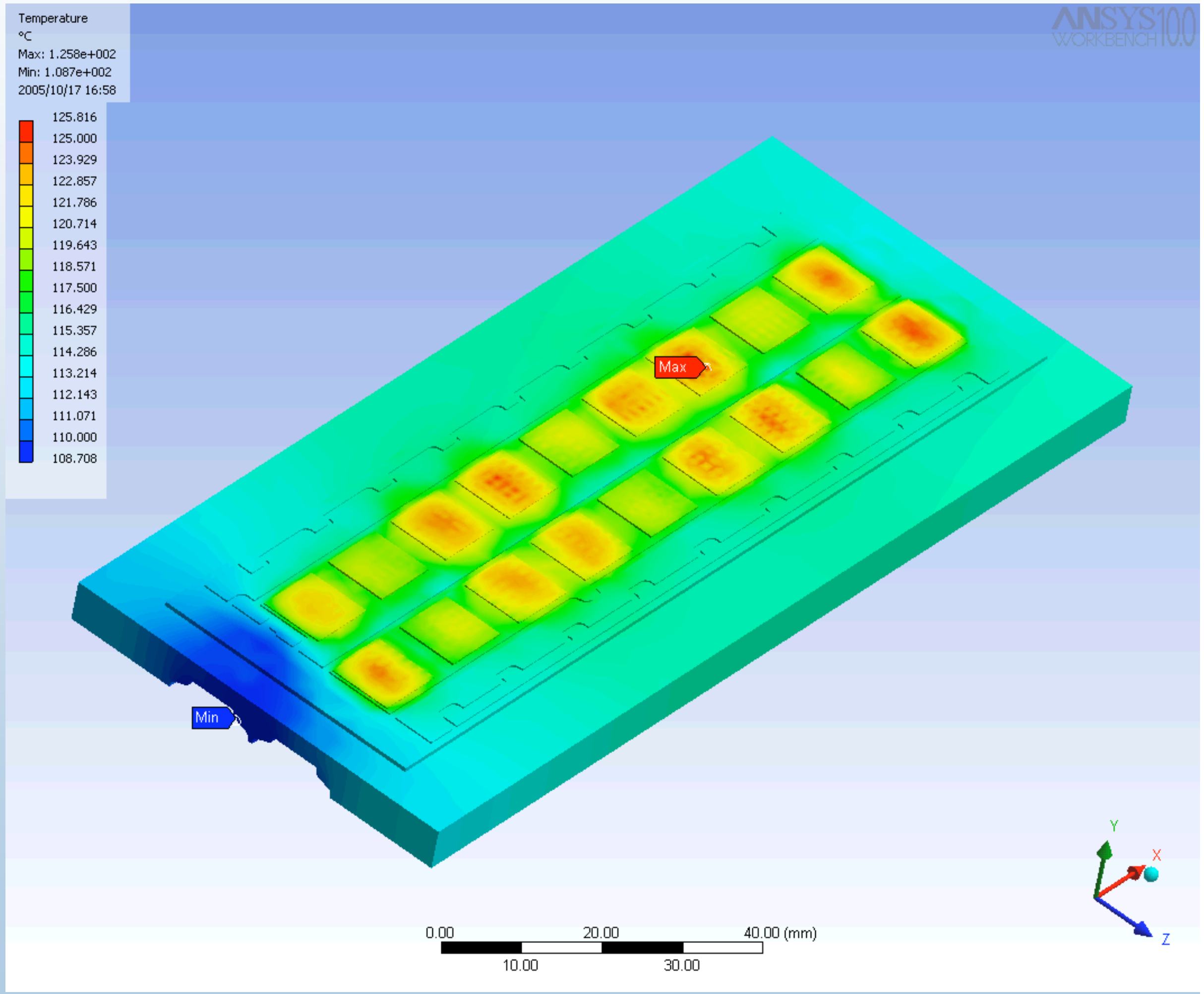
Thermal Analysis



- Boundary Conditions
  - Inlet Temp: 105°C
  - h_{jet}=*65,000 W/m*^{2} °C
  - h_{wall}=*15,000 W/m*^{2} °C
- Max Temp: 142.2°C
- *Why?*
  - *O-ring overlaps IGBT*
  - *Diminishes cooling capability*

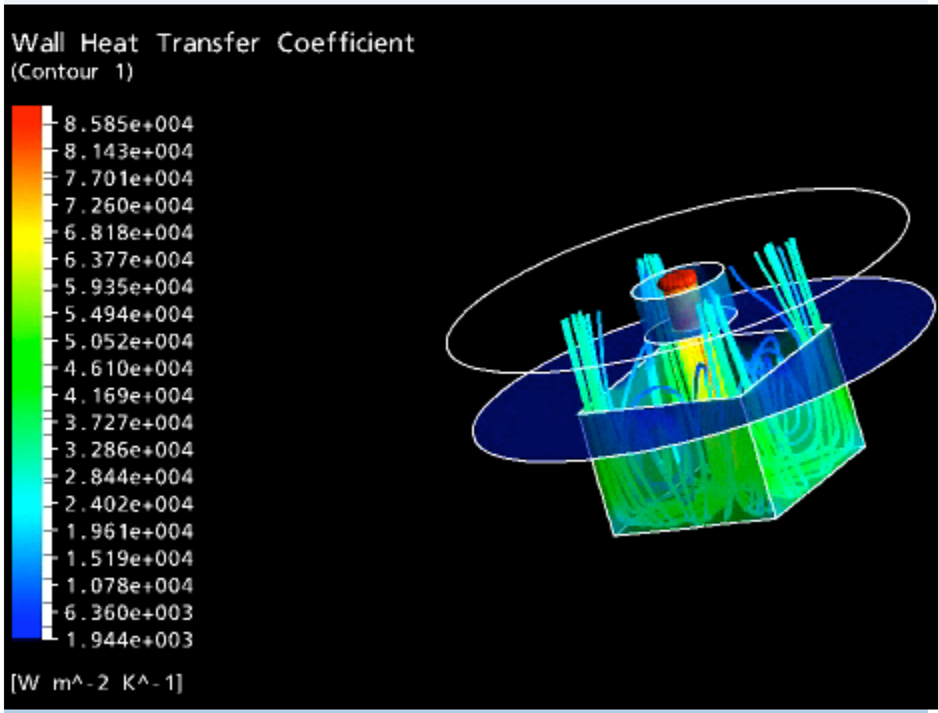
Proposed modification

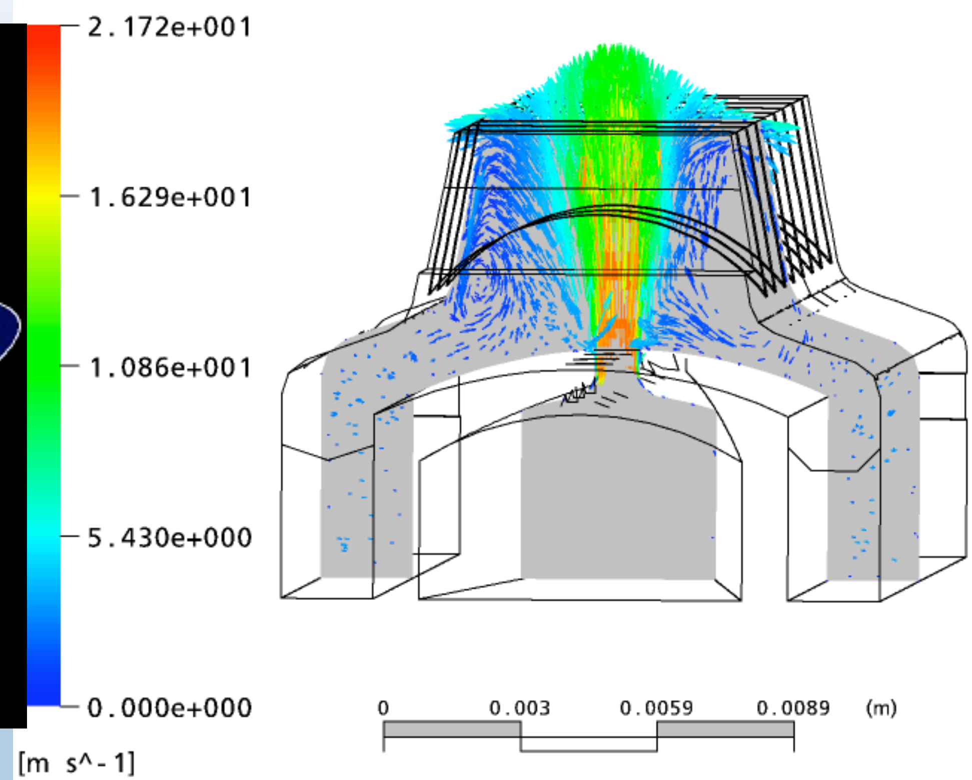
- DBC extended 5mm
  - O-ring no longer blocks flow
- Increased cooling
  - Flux: 100 W/cm^2
  - Inlet: 105°C
  - Max Temp: 125.8°C



CFD modeling

- Single / multiple jets
- Visualize flow paths
- Identify problematic geometry

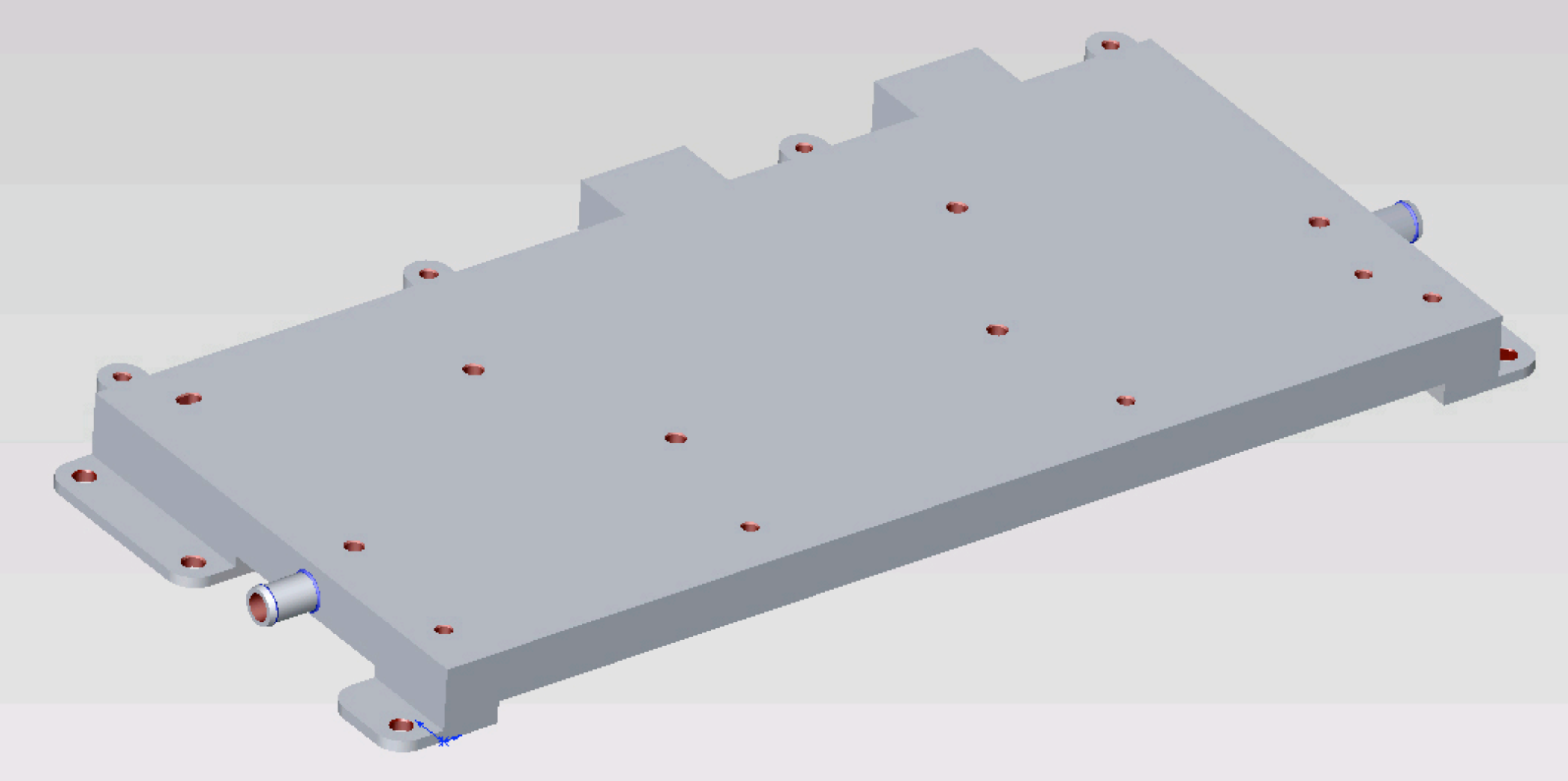




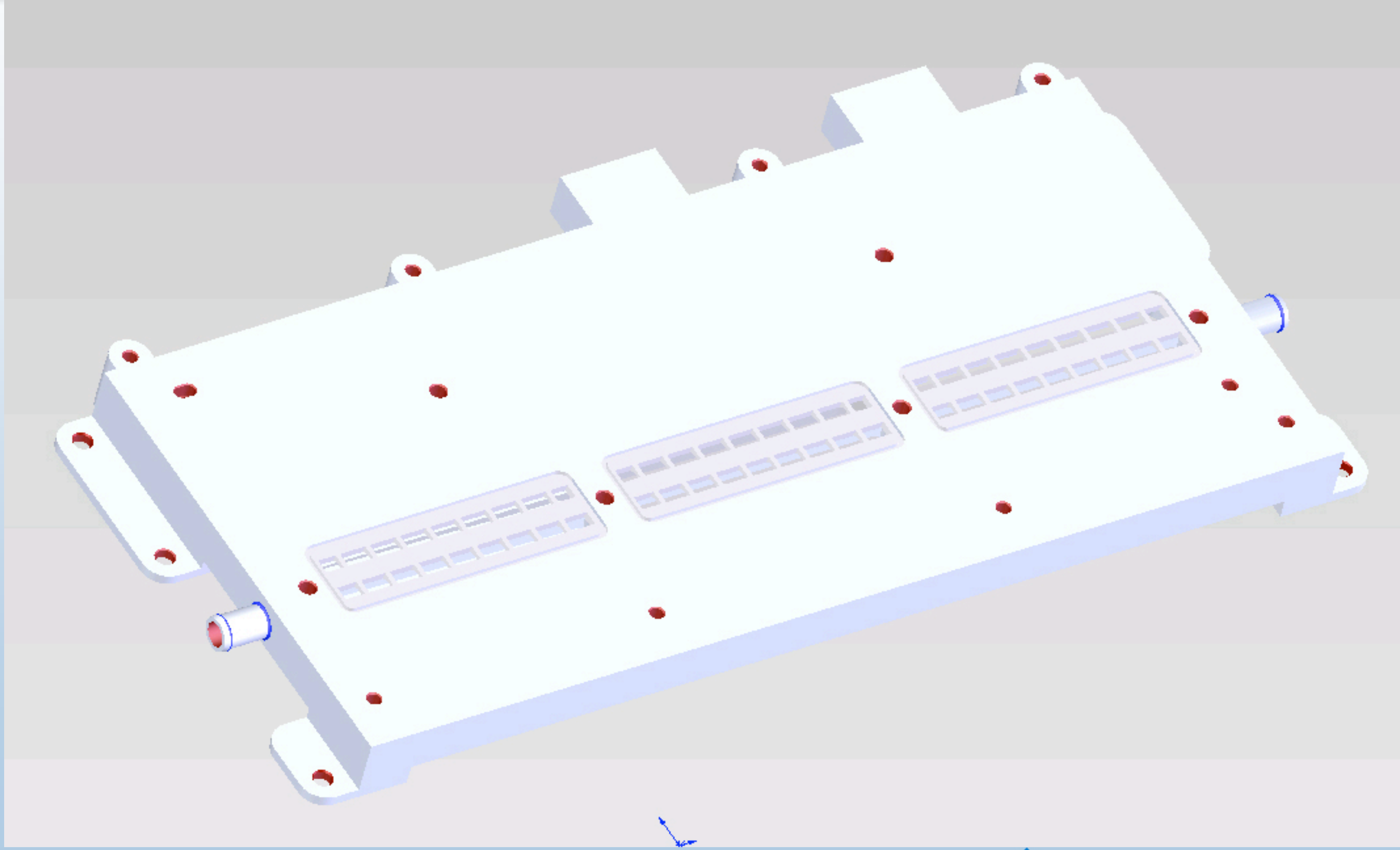
Approach for FY06

- Complete 6-resistor experiments
- Fabricate 1st prototype heat exchanger plate for experimental validation
- Continue to optimize configuration
  - Jet dimensions
  - Nozzle configurations
  - Impingement geometry

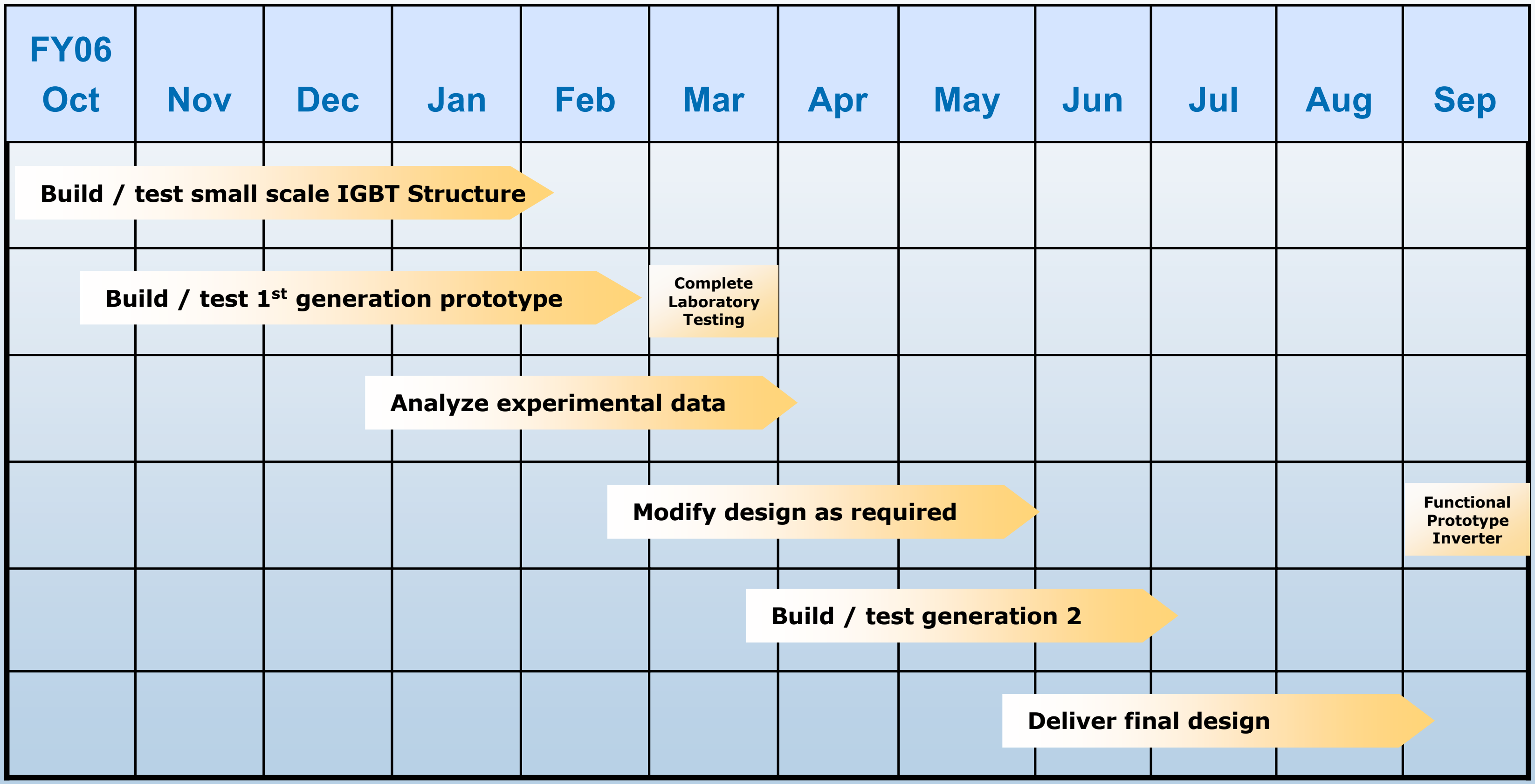
Semikron heat exchanger plate



Integrated heat exchanger plate



Timeline for FY06



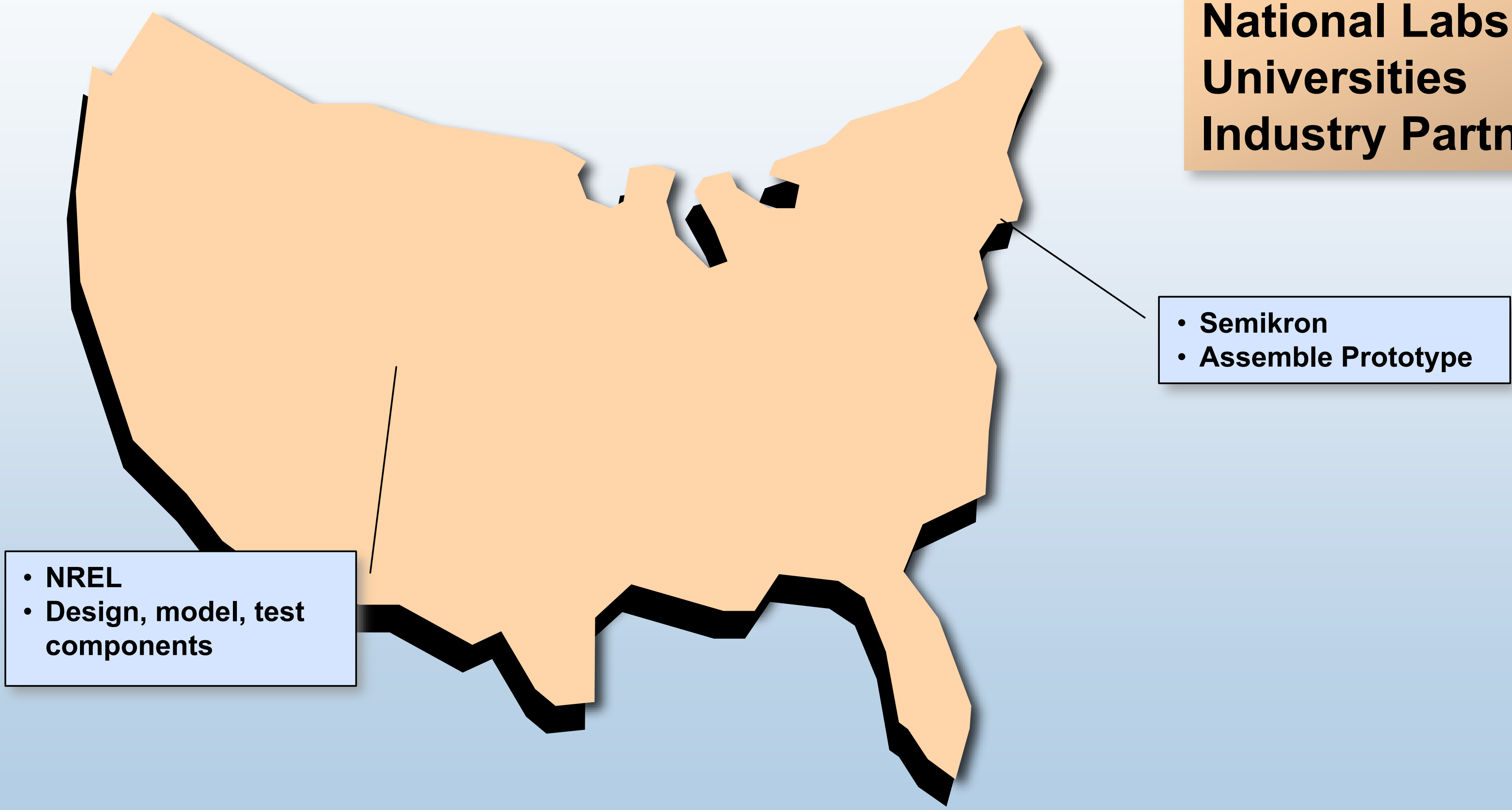
Key task | **Milestone/ Deliverable**

Barriers/Challenges

- Fabrication considerations
  - Cost effective manufacturing solutions
    - Cast parts
    - Minimize machining time
    - Minimize components
- Material Limits
- Erosion

Interactions and Collaborations

National Labs
Universities
Industry Partners



Questions