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A New Family of Multilevel Matrix Converters for Wind Power Applications: Final Report

July 2002 — March 2006

R. Erickson, S. Angkititrakul, and K. Almazeedi
University of Colorado
Boulder, Colorado

Subcontract Report
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December 2006

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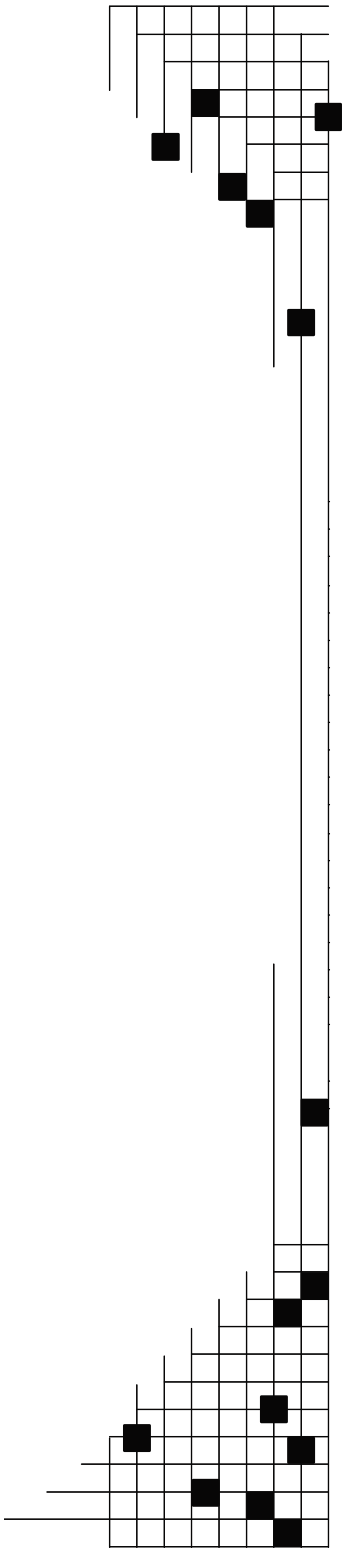

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Executive Summary

This project proposes the use of a new modular multilevel matrix converter for wind power applications. This modular approach allows the module size to be optimized with power semiconductor devices that have the best combinations of high performance and low cost. Multilevel switching reduces system switching loss and improves converter efficiency in the low wind speed conditions where typical variable-speed wind turbines commonly operate. In addition, the multilevel modular approach is well suited for scaling up to future wind farm applications that require the converter to interface with medium (4160 V) voltage AC.

The goal of this project was to develop the fundamental theory and practice of the multilevel matrix converter approach and to demonstrate a working scale model in the laboratory. This report documents the results and include several key contributions briefly described below.

Although the operation of a three-phase converter containing many modules initially appears to be quite complex, we show the converter operation can be understood through adaptation of the well-known space vector approach. In addition, we show how this approach is well suited to low-cost implementation using modern digital hardware, including field-programmable gate arrays (FPGA's), and flash memory lookup tables. Because the modular approach also employs simple, well understood power-stage circuits such as H-bridge circuits, the key issue is control rather than operation of the power stage. The theory and practice of this control are the key contributions of Part I of this report.

The controller performs two basic functions. First, it commands the switch modules to synthesise the AC input and output waveforms. Second, it balances the stresses between the modules; in the case of multilevel converters, this requires regulation of multiple switch module capacitor voltages. For paralleled converter modules, balancing of module currents may also be required. Part I of this report shows how the space vector control approach can be applied to solve both of these issues. It also documents the hardware implementation and laboratory verification of this proposed approach. Specifically, it describes the algorithms for both two-level and three-level synthesis of the AC waveforms. It proposes that the converter low-wind efficiency be improved by switching to three-level operation when the generator voltage output is low. Also, a capacitor voltage-balancing algorithm is developed and experimentally demonstrated that balances the internal capacitor voltages of all nine switch modules in the proposed modular converter system. This algorithm is based on an extension of the space vector modulation approach, and its stability is proven by Lyapunov theory. A laboratory prototype design is extensively documented; this prototype vindicates both the practicality of the control approach with up-to-date digital hardware and the correctness of the underlying theory.

Part II of this report demonstrates how to obtain torque control of the generator and power factor control of the utility-side output of the converter. It describes small-signal and large-signal averaged models of the proposed converter. These models are transformed to the *d-q* domain, and hence they are well suited for both converter space-vector control and generator field-oriented control. Part II also investigates multivariable control systems based on both the pole placement approach and the optimal control approach and finds that the optimal control approach is superior for this application. A gain scheduling algorithm leads to good performance over a wide range of operating points. This controller is added to the laboratory prototype of Part I, and is shown to provide both control of the converter terminal current magnitudes and power factors as well as the average capacitor voltage.

Listings of FPGA, flash memory, and microcontroller code, as well as several tables of the underlying modular matrix converter theory, are included in the appendices.

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Nomenclature

AC	alternating current
ADC	analog-to-digital converter
BRAM	block RAM
DC	direct current
DCM	digital clock management
FPGA	field programmable gate array
HDL	hardware description language
IGBT	insulated gate bipolar transistor
LTI	linear time invariant
OPB	on-chip peripheral bus
PCB	printed circuit board
PLB	processor local bus
PWM	pulse-width modulation
RMS	root mean square
SVM	space-vector modulation
VA	volt-ampere

1 Introduction

This research demonstrates a multilevel matrix converter suited to variable-speed wind turbine applications. Such a demonstration requires development of real-time control schemes for the new matrix converter. The control schemes for the converter must achieve two major tasks simultaneously: (1) synthesizing terminal AC voltage waveforms, and (2) maintaining fixed voltages across all midpoint capacitors.

An advantage of the proposed multilevel matrix converter is its ability to exhibit high efficiency over a wide range of operating points while converting variable-magnitude, variable-frequency voltages generated from a wind generator into fixed-magnitude, fixed-frequency voltages supplied to a utility grid. Attaining high converter efficiency over a wide range of operating points, especially at low operating power (low wind speed), is necessary to improve the energy capture of the variable-speed wind turbine system because this is where the system operates most of the time.

In this chapter, we review the wind turbine system configurations and three-phase converter topologies that are generally employed in wind turbine systems. We also review the performances of the power semiconductor converters that enhance the energy capture of the variable-speed wind turbine system. Next, we explain the approach used to increase the energy capture in the multilevel matrix converter. Finally, we summarize the characteristics of the multilevel matrix converter.

1.1 Overview of Wind Turbine Systems

In a wind turbine system, the kinetic energy in the wind is converted into rotational energy in a rotor of the wind turbine. The rotational energy is then transferred to a generator, either directly or through a gearbox for stepping up the rotor speed. The mechanical energy is then converted to (often variable-frequency, variable-voltage) electrical energy by the generator. From the generator, the electrical energy is transmitted to a utility grid either directly or through an electrical energy conversion stage that produces constant-frequency, constant-amplitude voltage suitable for interface to the utility.

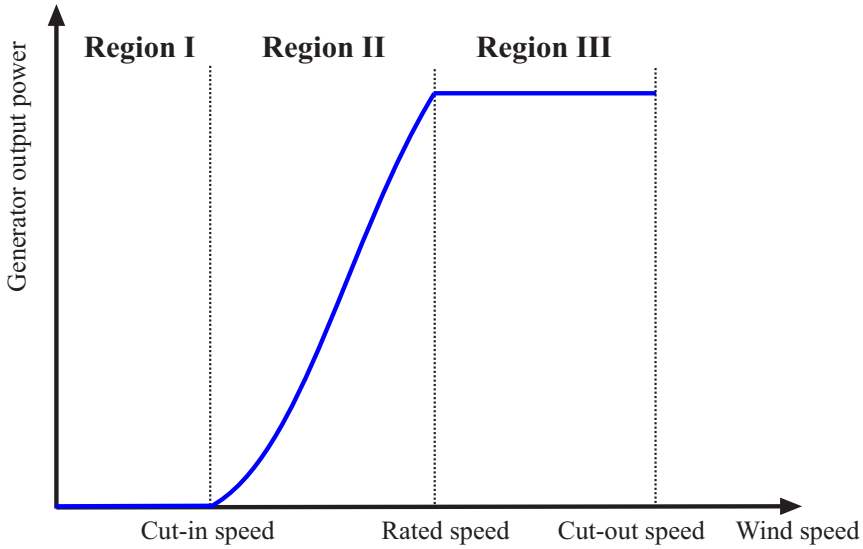


Figure 1.1: Ideal characteristic of a wind turbine generator

1.1.1 Ideal Characteristic of Wind Turbine Conversion

The ideal power characteristic for a wind turbine system is illustrated in Fig. 1.1. Operation of the wind turbine system is traditionally divided into three regions, as follows:

Region I where the wind speed is below the cut-in speed. The power in the wind is insufficient to overcome the power losses within the turbine system.

Region II where the wind speed is between the cut-in speed and the rated wind speed. Generally, the rated wind speed is the wind speed at which the maximum output power of the generator is reached. In region II, the power transmitted to the wind turbine rises rapidly with the wind speed and can be expressed as follows:

$$P = C_p \times \frac{1}{2}\rho A_r V_w^3 \tag{1.1}$$

where C_p = power performance coefficient,

ρ = air density (kg/m^3),

A_r = area swept by the rotor of the wind turbine (m^2),

V_w = wind speed (m/s).

Region III where the wind speed is between the rated wind speed and the cut-out speed. The cut-out speed is the maximum wind speed at which the turbine is allowed to deliver energy. Usually, the cut-out speed is limited by engineering design and safety constraints. In this region, the rotational speed of the wind turbine hub is kept approximately constant at the rated wind speed.

The relation of wind speed and turbine output power in Eq. (1.1) is not exactly a cubic relationship because of the power performance coefficient [1]. The power performance coefficient, C_p, is a nonlinear function depending on the ratio of rotor tip speed to wind speed. In general, the energy capture of the wind turbine system can be optimized by operating the wind turbine system at the maximum value of the power performance coefficient.

1.1.2 Wind Turbine Configurations

For a constant-speed wind turbine system, the configuration using a squirrel-cage induction generator that is directly coupled to the grid, as shown in Fig. 1.2, is usually employed. This configuration is popular because induction generators are rugged, inexpensive, and easy to connect to a utility grid. A gearbox is required for stepping up the rotational speed of the rotor to a range that the induction generator can use to produce an AC voltage at utility frequency (1500 rpm for a 50 Hz system and 1800 rpm for a 60 Hz system). The rotor speed variations in this configuration are small, approximately 1 to 2%.
The main disadvantage of the constant-speed configuration is the poor energy capture of the wind turbine system. Because the energy capture of the wind turbine system is a nonlinear function depending on rotor tip speed and wind speed as described in Eq. (1.1), at wind speeds above or below the rated wind speed the energy capture of the system does not reach the maximum value.

Another drawback of the wind turbine system with the directly grid-coupled configuration is the power quality of the system. This configuration is sensitive to fluctuations in the wind speed resulting from the steep torque speed characteristic of the induction generator. Any transient in the wind speed is transmitted through the drive train to the grid. This generally causes voltage flicker in the utility grid. In addition, the

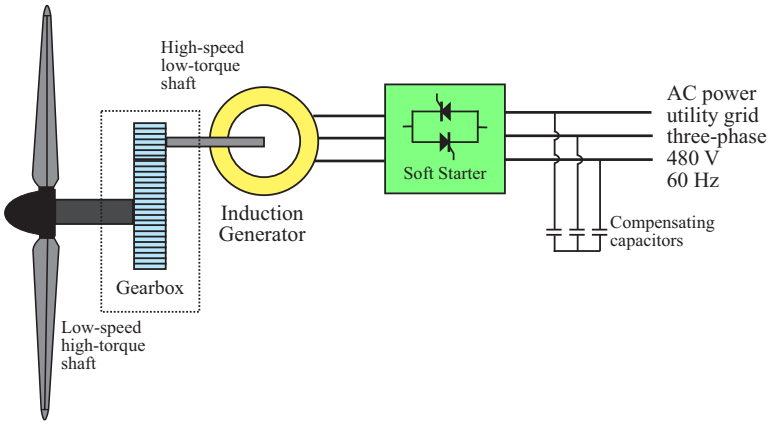


Figure 1.2: Constant-speed wind turbine configuration with a squirrel-cage induction generator that is directly coupled to the grid

induction generator always consumes reactive power from the utility grid. To compensate for the reactive power consumption of the induction generator, a capacitor bank is normally inserted in parallel with the generator to obtain close to unity power factor. Furthermore, a soft starter is also required to reduce mechanical stress and to reduce the interaction between the utility grid and the wind turbine during connections and startups of the turbine.

Configurations using variable-speed drives are normally employed to improve the energy capture of the wind turbine system. In a variable-speed wind turbine system, the rotational speed of the turbine rotor is continuously adjusted such that the tip speed ratio remains constant at the level of the maximum power performance coefficient. As a result, the overall efficiency of the wind turbine system is significantly increased. Configurations for variable-speed wind turbine systems are illustrated in Fig. 1.3. A power semiconductor converter is required to convert variable-frequency, variable-magnitude voltages generated from a generator into fixed-frequency, fixed-magnitude voltages supplied to a utility grid. Power factors at both generator and utility sides can be controlled through the operation of the power semiconductor converter.

In the system with a full-power converter (Fig. 1.3[a]), all output energy of the generator passes through a power semiconductor converter, which allows the wind turbine system to operate over a broad range of variable wind speeds. This configuration is generally employed with a permanent-magnet or a singly-fed induction generators, With new FERC ride-through requirements, this approach is increasingly attractive.

For the configuration using a doubly-fed induction generator with a reduced VA rating power semiconductor converter (Fig. 1.3[b]), the converter is connected to the rotor of the generator and directly controls currents in the rotor windings. Consequently, the mechanical and the electrical rotor frequencies are decoupled; the electrical stator and the rotor are matched independently of the mechanical rotor speed. Only a fraction of the rated generator power passes through the converter. This enables control of the whole generator by using a switching converter with rated power at only 20%-40% of the rated generator power. The generator can be operated at both sub- and super-synchronous speeds. The operational speed range of the generator depends only on the converter rating.

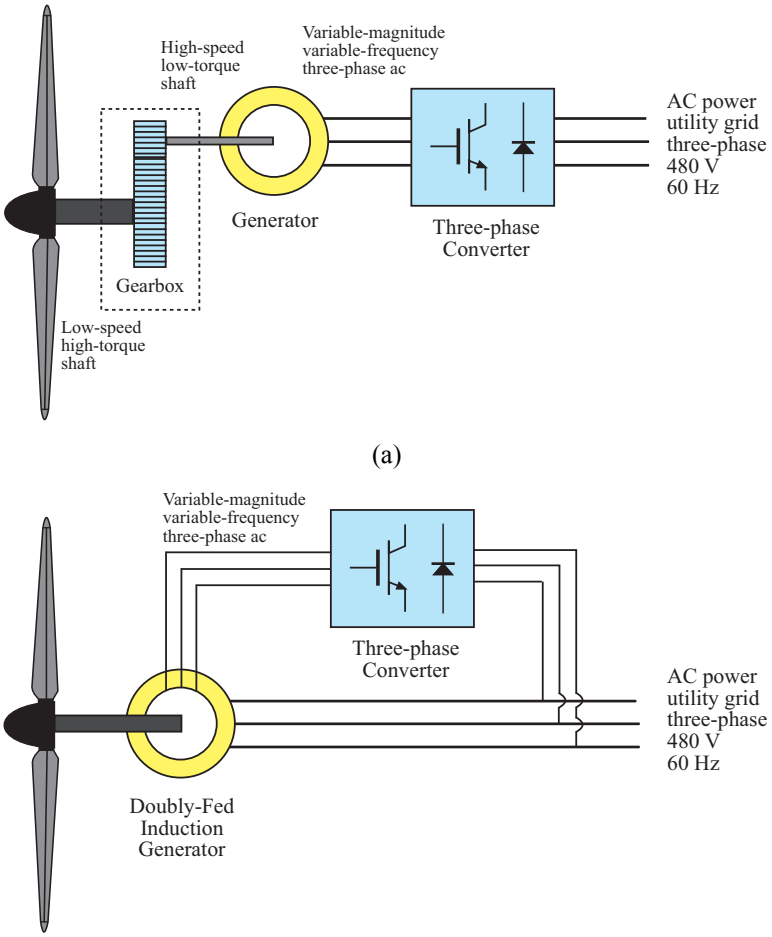


Figure 1.3: Variable-speed wind turbine configurations: (a) with full-scale converter, (b) with reduced VA converter

1.2 Overview of Three-Phase AC-AC Converters

A variable-speed wind turbine system for generating electricity requires a power semiconductor converter to convert variable-magnitude, variable-frequency voltages from the generator into fixed-magnitude, fixed-frequency voltages supplied to a utility grid. Several approaches to apply power semiconductor converters to wind turbine systems have been proposed [2]. Typical three-phase to three-phase voltage source converters can be categorized by their conversion characteristics into two families (Fig. 1.4):

1. AC-to-AC converter without a DC link
   In this type of converter, input AC voltages are converted directly into output voltages by proper operation of four-quadrant switches connected between the input and the output phases. In other words, the output voltages are chopped from the input voltages.

2. AC-to-AC converter with DC links
   In these converters, input AC voltages are converted into intermediate DC voltages, which are stored in storage links such as capacitors. Then, the intermediate DC voltages are converted into output AC voltages.

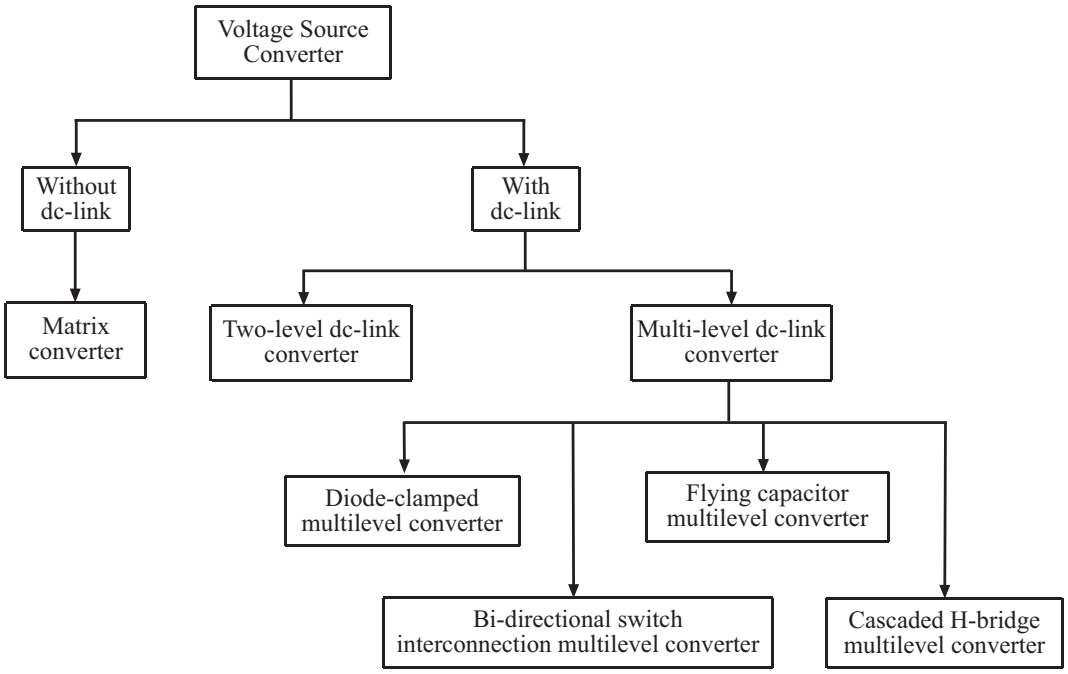


Figure 1.4: Classification of three-phase to three-phase voltage source converter topologies

1.2.1 Matrix Converter

The matrix converter has nine of the four-quadrant switches connected in a matrix configuration, so that any input phase can be connected to any output phase. Figure 1.5 illustrates the configuration of a conventional matrix converter. Each four-quadrant switch employed in the matrix converter is typically implemented from two two-quadrant switches (Fig. 1.6). Ideally, the matrix converter, which consists of only silicon switching devices in the power stage, can be considered a "generalized solid-state transformer" [3]. In practice, for the best performance, the converter should generate smooth waveforms; therefore, filter elements are necessary. Capacitors are employed at the input side of the converter, and inductors are employed at the output side.

The basic operation concept of the matrix converter is that the desired input currents (either to or from a three-phase source) and the desired output voltages with arbitrary frequency can be obtained by properly connecting the output phases to the input phases.

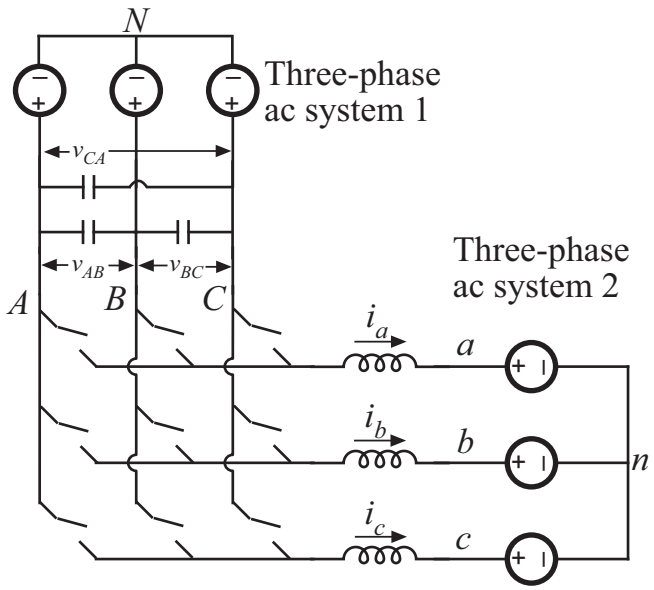


Figure 1.5: Conventional matrix converter topology

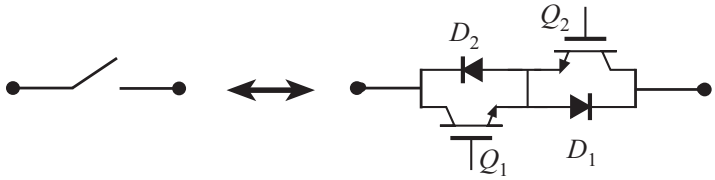


Figure 1.6: Conventional four-quadrant switch used in the matrix converter

With inductors as filter elements at the output side and capacitors at the input side, two constraints are imposed in the operation of the matrix converter. First, because the inductor currents cannot be interrupted, at least one of the three switches connected to each inductor (output phase) must conduct the inductor current at any given time. Second, switches must not short circuit any capacitor voltage (input phase). These two constraints imply that exactly three switches conduct currents at any instance and limit combinations of the four-quadrant switches into 27 cases [4]. To prevent violations of these constraints, especially during switching transitions, multi-stepped switching procedures for safe commutation are usually employed [5, 6]; sometimes soft-switching techniques are also considered [7, 8].

Modulation algorithms for the matrix converter can be categorized into scalar modulation [9, 10, 11, 12] and space-vector modulation [4, 5]. Both modulation algorithms can generate an arbitrary output frequency and an arbitrary input displacement power factor. Extended modulation algorithms, such as adaptive space-vector modulation (SVM) and selected harmonic-elimination pulse-width modulation [13, 14] were also proposed to improve specific features of the matrix converter.

The scalar modulation involves direct matrix computation of the input voltages (currents) and the output voltages (currents). The unfiltered output line-line voltages are synthesized by sequential, piecewise sampling of the input line-line voltages. As a result, the output voltages are bounded by the input voltages. With the scalar modulation algorithm, the matrix converter can generate output voltages with the maximum gain ratio of 0.5 when the output voltages consist of only fundamental frequency. The gain can be increased to 0.75 by injecting the third harmonic of the input frequency into the desired output-

phase voltages. The gain can be further increased to 0.866 by an additional injection of the third harmonic of the output frequency [12]. However, improving the gain ratio involves a significant amount of additional calculations.

The SVM technique was adapted for the matrix converter by employing a basic concept of indirect modulation using a fictitious DC bus, then dividing the converter into a rectification stage and an inversion stage [4]. The side having capacitors as filter elements performs rectification, and the side having inductors as filter elements performs inversion. The input currents and the output voltages are controlled by separate SVMs. The SVM technique also allows the maximum gain ratio of 0.866. An output voltage waveform of the matrix converter using the SVM technique is shown in Fig. 1.7. Furthermore, this modulation technique allows simplifying a converter model, making it easier to control the converter under imbalanced and distorted power supply conditions. More details of the SVM will be discussed in Chapter 2.

Matrix converters do not require intermediate energy storage and have lower switching losses. Although the matrix converter has six additional switching devices, compared to the back-to-back, two-level, DC-link converter, the absence of the DC-link capacitor may increase the efficiency of the converter. Also, the power semiconductor devices in the matrix converter are switched at average voltages lower than those in the two-level, DC-link converter.

The major disadvantage of the matrix converter is the limitation of the voltage gain ratio, which leads to poor semiconductor device utilization. Another drawback is the large number of semiconductor devices required to make the matrix converter functional. Although devices with smaller current rating can be employed, they still lead to a large number of gate driver circuits. In addition, with the absence of the DC-link, there is no decoupling between the input and output sides. Any distortion in the input voltage is reflected in the output voltage at different frequencies; as a consequence, subharmonics can be generated.

Many soft-switching techniques have been proposed to improve the efficiency of the matrix converter. A low-loss four-quadrant switch was proposed with the ability to be turned on with zero current switching

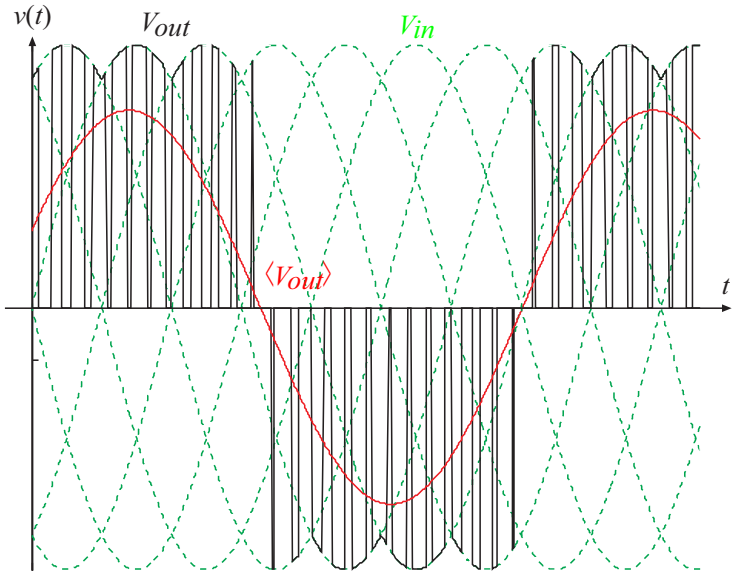


Figure 1.7: Output voltage waveform generated from matrix converter using the SVM technique

and turned off with zero voltage switching [15]. The proposed four-quadrant switch has a disadvantage of high current stress through the resonant inductors because the inductors are placed on the power transfer paths. A soft-switching technique based on a fictitious DC-link technique, using an active commutation auxiliary circuit, was also proposed [7, 8]. With this technique, soft commutations at all switches, zero-voltage transition for main switches, and zero-current transition for auxiliary switches can be achieved independently of load.

Several approaches for applying the matrix converter to a variable-speed wind turbine system have been proposed [16, 17, 18]. The proposed approaches aim to maximize the energy capture of wind turbine systems by controlling terminal voltages and frequencies of the generators so that the power performance coefficients, $C_{p,}$ of the systems can be obtained at the optimal point.

1.2.2 Multilevel DC-Link Converter

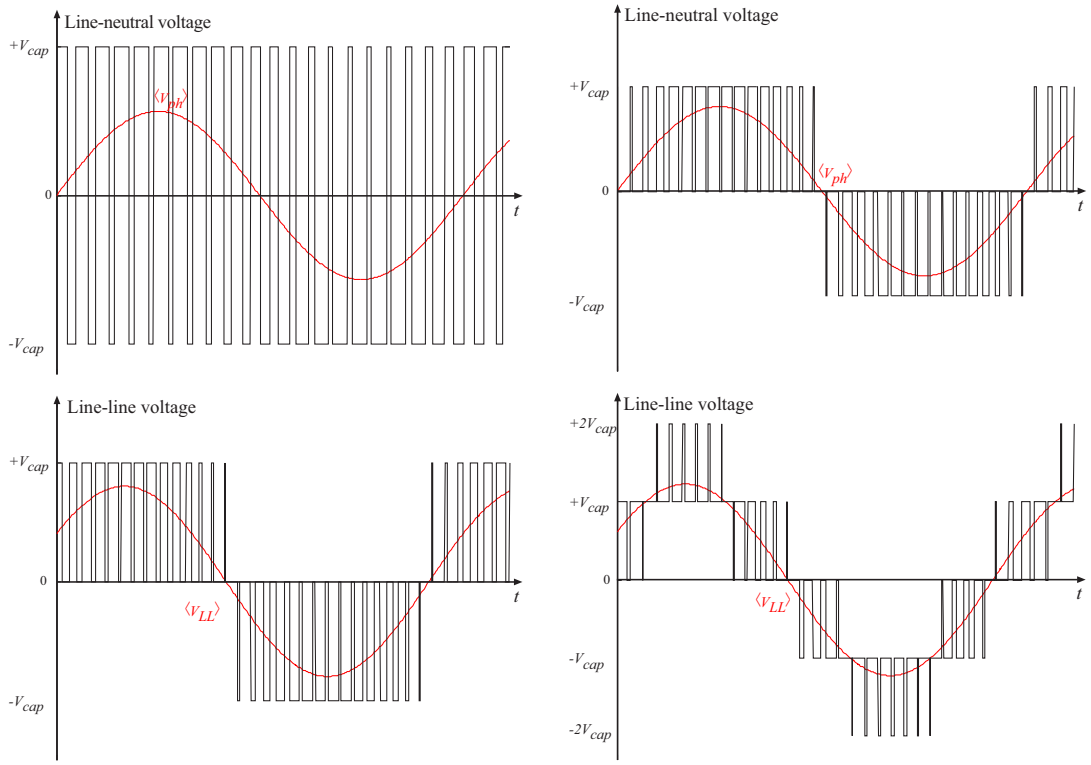
Multilevel conversion has attracted significant attention as a way to construct a relatively high-power converter using relatively low-power semiconductor devices [19, 20, 21, 22, 23, 24, 25]. The general concept involves producing AC voltage waveforms from several small DC voltages. The smaller voltage steps yield lower harmonic distortion at AC voltage waveform, lower switching loss, lower voltage change rate (dv/dt), as well as smaller filter element requirements.

The lower voltage change rate can extend the lifetime of the AC machine connected to the converter. The converter's high-voltage change rates induce circulating currents, dielectric stresses, voltage surge, and corona discharge between the winding layers, which cause "motor bearing breakdown" and "motor winding insulator breakdown" problems in the AC machines [26, 27]. These problems become more significant as the switching speeds of power semiconductor devices are increased.

Figure 1.8 compares waveforms of conventional pulse-width modulation (PWM) of two-level switching voltage and three-level switching voltage. In the two-level switching-voltage waveform, the line-neutral voltage is switched between two voltage levels: positive DC bus voltage and negative DC bus voltage. While in the three-level switching-voltage waveform, the line-neutral voltage is switched among voltage levels of positive voltage of DC bus, negative voltage of bus voltage, and mid-point voltage of DC bus.

The major disadvantages of the multilevel conversion are its complexity of control and its complexity of bus-bar interconnection. A larger number of semiconductor devices are required. This does not lead to an increase in semiconductor costs because lower-rated devices can be used; however, it does require significantly more gate-driver circuits and leads to a more complex layout. Furthermore, the presence of DC-link capacitors is considered a drawback because they are heavy and bulky. As the number of voltage levels increases, the bus-bar structures of the multilevel DC-link converter become more complex and difficult to fabricate.

The capacitor voltage-balancing problem in the multilevel converter is also an eminent disadvantage. During converter operation, capacitor voltages in the converter deviate because the currents flowing through the capacitors are different. Several topologies and control algorithms of the multilevel converter have been proposed to overcome this problem. The problem of capacitor voltage balancing also becomes more difficult to overcome as the number of voltage levels increases.



(a) Two-level switching (b) Three-level switching

Figure 1.8: Comparison of PWM waveforms for (a) conventional two-level switching and (b) three-level switching

SVM is extensively employed to synthesize AC waveforms in the multilevel DC-link converter [28, 29, 30, 31, 32, 33]. The modulation can be efficiently associated with a capacitor voltage-balancing scheme. It is easy to extend the modulation to operate at higher voltage levels.

The following converter topologies are examples of commonly used multilevel converters.

1.2.2.1 Diode-Clamped Multilevel Converter

Figure 1.9 shows a schematic of a back-to-back three-level diode-clamped converter. Identical legs of power semiconductor devices are employed for each input and output phase. The DC bus voltage in the converter is divided by two equal capacitors. The midpoint junction of two capacitors is referred as the neutral point.

In the neutral-point diode-clamped PWM converter, power semiconductor devices are clamped to capacitor voltages via diodes [24, 34, 35]. Hence, device voltage stresses can be reduced to one-half the magnitude of the DC bus voltage. However, the inner power semiconductor devices of each phase are not directly clamped to the DC capacitors. These devices may encounter more blocking voltages.

The capacitor voltage unbalancing problem in the neutral-point clamped three-level converter can be solved using additional control algorithms without any additional hardware [36, 37, 38, 39, 40]. The capacitor voltage unbalancing problem becomes more difficult to overcome as the switching level increases.

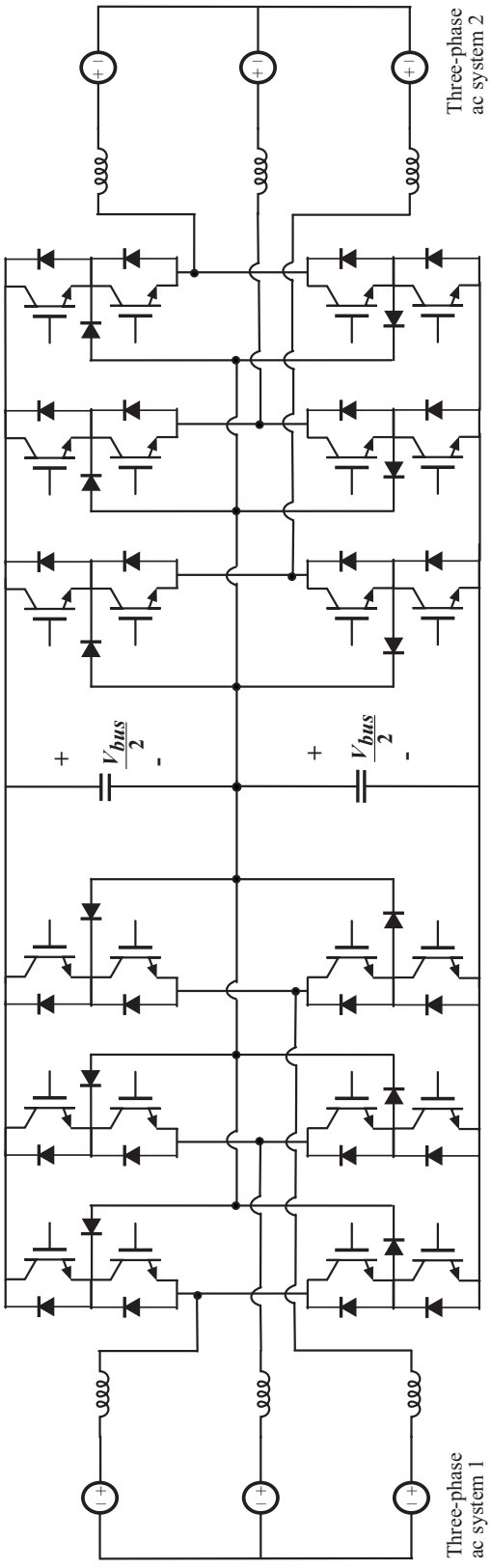


Figure 1.9: Back-to-back three-level diode-clamped converter

1.2.2.2 Multilevel Converter with Bi-Directional Switch Interconnection

A schematic of switching a device for one phase of a three-level converter with bi-directional switch interconnection is illustrated in Fig. 1.10. The bi-directional switch provides a means to clamp the output voltage to the midpoint level [41]. The voltage rating of power semiconductor devices in the bi-directional switch is half of the DC bus voltage, while the voltage rating of the main switching devices is the full DC bus voltage.

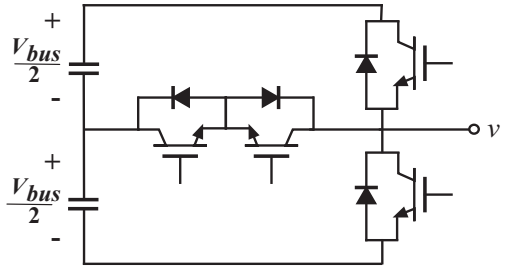


Figure 1.10: Switching device configuration for one phase of a three-level converter with bi-directional switch interconnection

The converter operates with conventional two-level PWM algorithms, while using the midpoint voltage level only during switching transitions. This can be considered "quasi three-level" operation. The main switching devices hard-switch at half of DC bus voltage; therefore, switching loss is reduced compared to the conventional two-level switching converter.

1.2.2.3 Flying-Capacitor Multilevel Converter

Figure 1.11 shows the switching-device configuration for one phase of a three-level flying-capacitor converter. The difference in component count between the diode-clamped multilevel converter and the flying-capacitor multilevel converter is that two diodes per phase are replaced by one capacitor [42, 43]. Voltages across open-circuited switches are constrained by clamping capacitors instead of clamping diodes. The flying-capacitor configuration also alleviates the voltage clamping problem of the inner devices in the diode-clamped converter. A high-frequency small capacitor clamps two inner devices of one phase at $V_{bus}/2$. Devices between the upper part and the lower part conduct current complementarily.

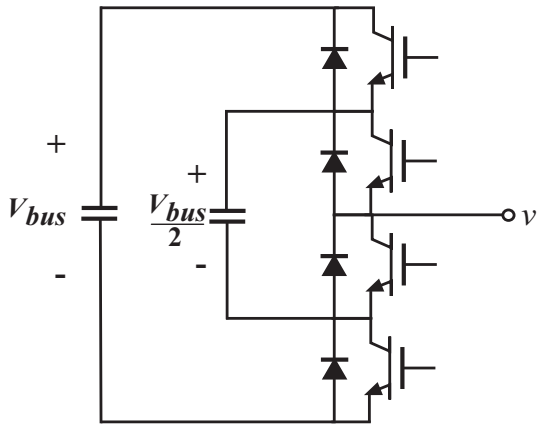


Figure 1.11: Switching device configuration for one phase of a three-level flying capacitor converter

The benefit of the capacitor-clamped converter is that the voltage-balancing problem is relatively easy to solve, compared to the diode-clamped converter.

1.2.2.4 Multilevel Converter with Cascaded H-Bridge Cells

The structure of one phase of a seven-level converter with cascaded H-bridge cells is illustrated in Fig. 1.12. The remaining phases have the same switch configuration. The configuration was proposed to eliminate the neutral-point balancing problem in the multilevel converter, with a simplifying bus-bar structure [44, 45]. The DC voltage sources are supplied from isolated DC sources, such as isolated three-phase rectifier circuits. Each H-bridge switch can generate three different voltage levels: $+V_{dc}$, 0, and $-V_{dc}$. H-bridge switches are connected in series such that the synthesized AC voltage waveform is the summation of all voltages from cascaded H-bridge cells. The number of phase-voltage levels can be defined as $m = 2s + 1$, where m is the number of H-bridge switches in each leg. One disadvantage of this configuration is that the converter requires multiple isolated DC sources, which makes it an expensive solution.

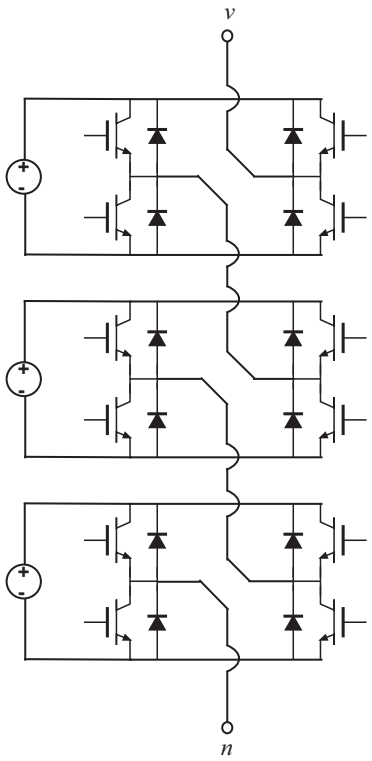


Figure 1.12: One-phase structure of a multilevel converter with H-bridge inverter leg

A modified configuration of this topology to achieve more voltage levels was also proposed [22]. By employing non-identical DC voltage sources in a binary arrangement, the number of switching voltage levels can be increased without increasing the number of the H-bridge switch cells.

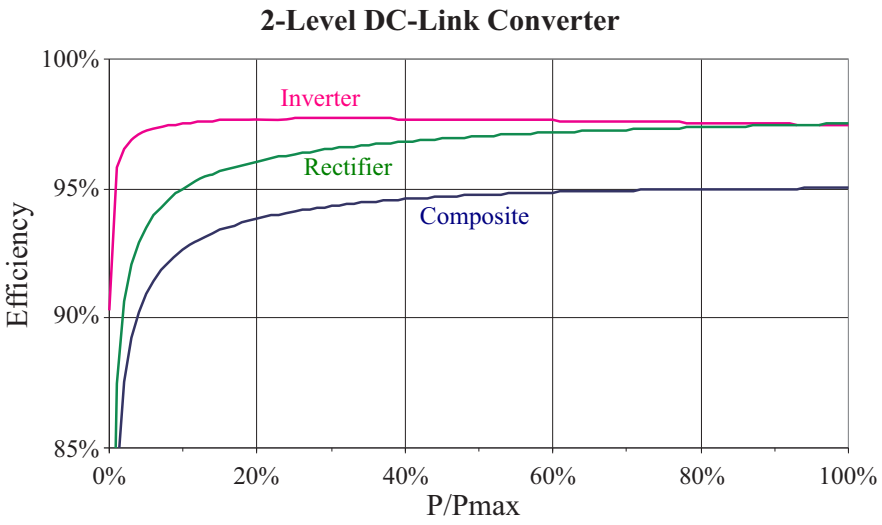
1.3 Efficiencies of Power Semiconductor Converters

The requirement for high efficiency at low power and low voltage is unique to the variable-speed wind turbine system. A typical way to design a converter is to optimize the performance at the rated operating

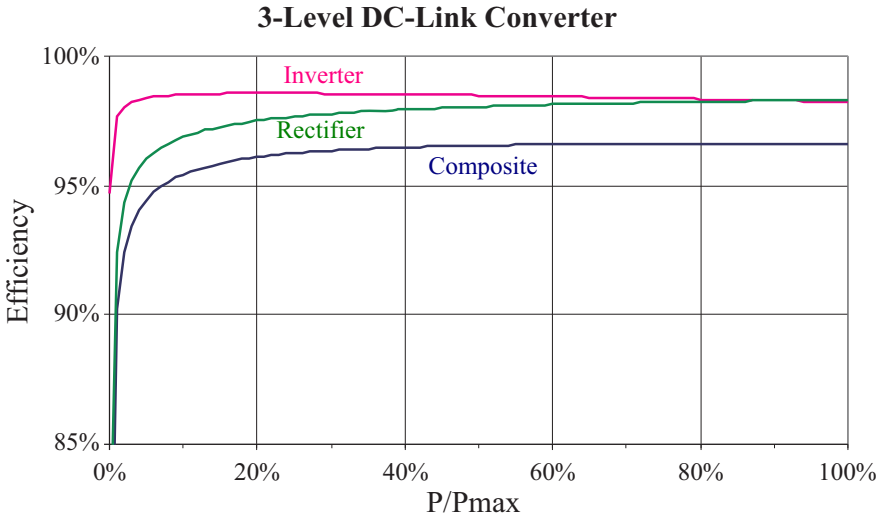
point. This minimizes the cost of the converter by minimizing the component stresses and losses. However, the efficiency of the converter is decreased rapidly at reduced power, reduced voltage. This behavior can significantly degrade the energy capture of variable-speed wind turbine systems when they operate at low wind speed (Region II in Fig. 1.1). Achieving high converter efficiency under low wind speed is crucial for improving energy capture in variable-speed wind turbine systems because typical wind energy systems operate primarily at low wind speeds.

Figure 1.13 summarizes efficiencies of DC-link converters with two- and three-level switching from experimental results [46]. Both results were obtained from the converters converting variable-magnitude input voltages from a synchronous generator into fixed-magnitude output voltages at a utility grid side, simulating a variable-speed wind turbine system. The DC-link voltages of the converters are fixed at a magnitude slightly greater than the utility voltage magnitude. Both converters employ the same power semiconductor devices and use identical models of the switching and conduction losses.

The results show that the converter efficiencies are dominated by the efficiencies of the rectifier parts of the converters. In addition, at lower operating power or lower operating voltage, the efficiencies of the rectifier parts decrease more rapidly than those of the inverter parts. Because the voltage produced by the generator is proportional to the wind speed, the reduced voltage produced by the generator under low-wind-speed conditions causes the rectifier parts to "work harder" in stepping up the voltage magnitude. This requires a greater proportion of indirect power. In the rectifier portion of the DC-link system, the indirect power consists of energy that is first stored in the inductors and later released to the DC link. In contrast, the direct power consists of power that flows directly from the input side to the output side, without going through the intermediate step of being stored. Hence, the indirect power conversion incurs additional losses. This problem of low efficiency at low operating voltage can also be observed in the boost converter.



(a)



(b)

Figure 1.13: Efficiencies of three-phase DC-link converters: (a) two-level switching, (b) three-level switching

It can also be seen from the results that, as the number of switching levels increases, the converter efficiency at full load improves. The efficiency at light load also improves, and the knee of the efficiency curve shifts to the left. The range of high efficiency is extended into lower operating points. Effectively, the range of power levels over which the high full-load efficiency is maintained is extended by a factor of approximately two (for example, the value of $P/P_{\max}$ at the knee is reduced by 50%). The reason for this is that the rectifier part converts the voltage generated from the generator into lower magnitude as the number of switching levels increases. As a result, the switching losses in the converter are reduced. The switching loss for a switching device is defined as follows:

$$P_{SW} = f_s(\Delta V_{ds})Q_{loss} \tag{1.2}$$

where f_s is the switching frequency of the converter, ΔV_{ds} is the voltage change during each switching, and Q_{loss} is charge associated in each switching. As the switching loss is proportional to the voltage change ΔV_{ds}, the efficiency of the rectifier increases as the number of switching levels increases.

For a converter using insulated gate bipolar transistors (IGBTs) and diodes as switching devices, the switching losses in the converter are dominated by the IGBT current tailing and the diode reverse recovering [46]. Therefore, with reduced switching voltage, three-level switching converters exhibit lower switching losses than those of two-level switching converters. However, the two-level switching converters were reported to exhibit better overall efficiency when the overall losses (conduction loss, switching loss, and loss in filter elements) were considered. Because the switching loss in the three-level switching converter is much lower than that in the two-level switching converter, the switching frequency of the three-level switching converter can be increased to reduce the loss in filter elements. To optimize the converter efficiency in the wind turbine system, the DC-link converter with the three-level switching structure at the grid side and the two-level switching structure at the generator side is recommended [48].

Another approach to improve the converter efficiency is to employ a reconfigurable structure concept. The reconfigurable converter concept for variable operating points applied in a boost double rectifier has shown significant improvement in efficiency at low voltage (low power) [49]. When the boost double rectifier operates in the double mode, the rated power is doubled; however, the switching losses are not double. Hence, the rectifier exhibits higher efficiency. The reconfigurable structure concept requires finer control of the semiconductor devices so that the power conversion mechanism can be effectively reconfigured and better optimized at a wide range of operating points.

1.4 The New Multilevel Matrix Converter

The multilevel matrix converter was proposed to solve the problem of low converter efficiency at low voltage, low power [49, 50]. A schematic of the converter with basic configuration is illustrated in Fig. 1.14(a). The converter is a hybrid of multilevel and matrix technologies. The conversion approach of the converter is based on H-bridge switch cells, resembling the structure in Fig. 1.12. The use of a matrix configuration eliminates the need for DC voltage sources to supply average power. Therefore, the DC voltage sources can be replaced by simple DC capacitors, as shown in Fig. 1.14(b).

The multilevel matrix converter synthesizes the input and the output voltages by PWM of the DC capacitor voltages of the H-bridge switch cells. This operation differs from that of the conventional matrix converter in which the voltages are synthesized on one side and currents on the other. Therefore, inductors can be used as filter elements at both sides of the converter. Because of the symmetry of the multilevel matrix converter structure, both step-up and step-down of the voltage magnitude are possible.

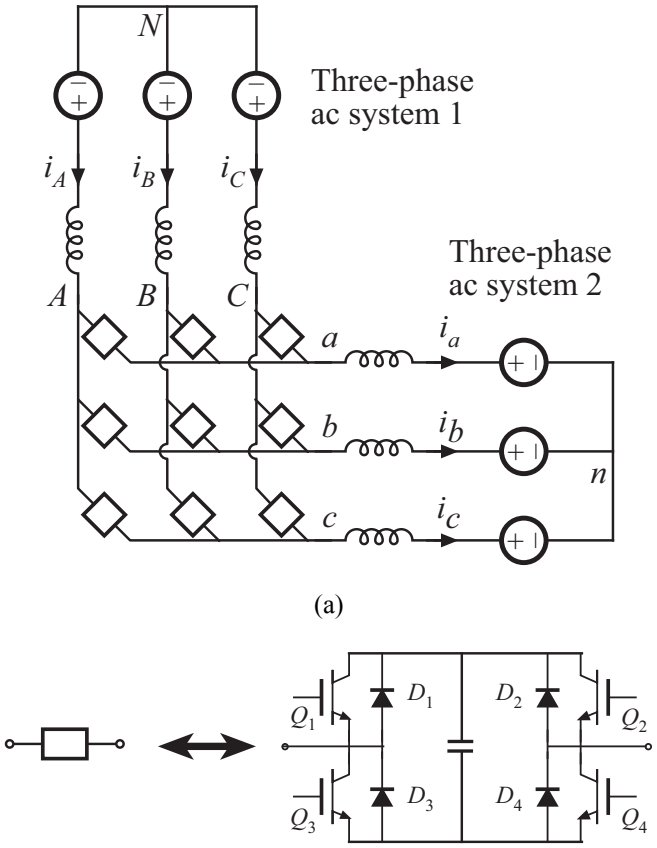


Figure 1.14: Basic configuration of a multilevel matrix converter: (a) converter topology, (b) schematic of an H-bridge switch cell

Table 1.1: Comparison of a Conventional Matrix Converter and a Multilevel Matrix Converter

Factor	Conventional Matrix Converter	Multilevel Matrix Converter
Voltage conversion ratio (V_{out} / V_{in})	Buck only: $V_{out} \leq 0.866 V_{in}$	Buck-Boost: $0 \leq V_{out} \leq V_{in}$
Switch commutation	Coordination of four-quadrant switches	Simple transistor plus freewheeling diode
Bus-bar structure	Complex	Modular and simple
Multilevel operation	No	Possible
Filter elements	AC capacitors and inductors	Inductors

The multilevel matrix converter is fundamentally different from the conventional matrix converter, as well as the multilevel DC-link converter, in several respects. Table 1.1 summarizes these differences. First, the conventional matrix converter can only step-down voltage, with the maximum voltage magnitude at the low-voltage side of 0.866 times the voltage magnitude at the high-voltage side. Therefore, in a wind turbine system, the voltage magnitude produced by the generator must be less than 0.866 times the voltage magnitude of the utility grid. In contrast, the multilevel matrix converter can both step-up and step-down the voltage magnitudes, with arbitrary power factors.

Switch commutations for the conventional matrix converter must be carefully coordinated with independent control of anti-parallel transistors. These control schemes introduce an additional level of complexity. In the multilevel matrix converter, a simple method for coordinating switch transitions, "break before make" operation, can be employed. This method requires that all transistors that are to be switched off must first be turned off; after a short delay, the transistors that are to be switched on are then turned on. During the dead-time of switch transitions, inductor currents are not interrupted because the anti-parallel diodes can conduct currents and provide flow paths for the inductor currents. Energy stored in the inductors is then transferred to the switch-cell capacitors. A soft-switching scheme or a safe-commutation scheme can also be applied in the multilevel matrix converter.

Bus-bar structures of the conventional matrix converter are quite complex, as are those of the multilevel DC-link converter. To avoid excess voltage transients during switch transitions, it is necessary to minimize the parasitic wiring in all circuit loops that carry high-frequency currents. A practical approach for the bus-bar structures that resemble multi-layer printed circuit boards is to overlap the conducted current and the return current so that the magnetic fields of the currents are nearly canceled, and the parasitic inductance is thereby minimized. The modular approach of the H-bridge switch cell in the multilevel matrix converter simplifies the complexity of the bus-bar structures. The bus bars in the H-bridge switch cells can be locally overlapped within the switch cells. This modular approach also allows the switch cells to be constructed using printed circuit boards. Such construction leads to further benefits of automated fabrication of the circuitry.

The modularity of the converter approach also provides a way to directly scale the design to higher voltage and power levels. The power-stage voltage and power level can be increased by series-connecting identical switch modules in each branch of the matrix connection. The power-stage elements are otherwise unchanged. All that is needed is modification of the controller to properly switch the additional modules.

Finally, the conventional matrix converter requires the use of AC capacitors at the high-voltage side and inductors at the low-voltage side. This configuration implies that exactly three switch branches conduct at any instant. In contrast, the multilevel matrix converter employs inductive elements on both sides and then requires five conducting branches at any instant.

1.5 Research Motivations and Contributions

Software developed for simulating the operation of the multilevel matrix converter has demonstrated that the converter can regulate all nine capacitor voltages while synthesizing terminal voltages [49]. The algorithm employed in the software is based on a lookup table that contains pre-calculated currents flowing through switch-cell capacitors for all possible switching-device combinations of the multilevel matrix converter. During the simulation, the software searches through the lookup table for switching-device combinations that have proper currents flowing through the desired capacitors. However, this approach is not practical for a real-time control because it requires significant time to choose one proper combination from a decidedly huge lookup table.

To enable use of the new multilevel matrix converter in variable-speed wind turbine applications, an objective of this research is to develop real-time control schemes for the multilevel matrix converter. The control scheme for the multilevel matrix converter consists of two tasks that must be performed simultaneously:

(1) Synthesizing terminal AC voltages

(2) Regulating switch-cell capacitor voltages.

To synthesize the terminal voltages of the multilevel matrix converter, the space-vector control technique is applied because of its simplicity when implemented with another control scheme. The space-vector control requires that the three-phase variables must be converted in the dq variables. The multilevel matrix converter with the basic configuration is able to generate, for each side, 19 combinations of three-phase line-line voltages in terms of the capacitor voltage, corresponding to 19 space vectors: a null-state space vector, six space vectors with magnitude $2V_{cap}/\sqrt{3}$, six space vectors with magnitude $2V_{cap}$, and six space vectors with magnitude $4V_{cap}/\sqrt{3}$. A dq diagram of the 19 space vectors obtained from a multilevel matrix converter is shown in Fig. 1.15. There are similar dq diagrams for voltage modulation of each side of the converter. The dq diagram can be divided into three regions according to the converter operations.

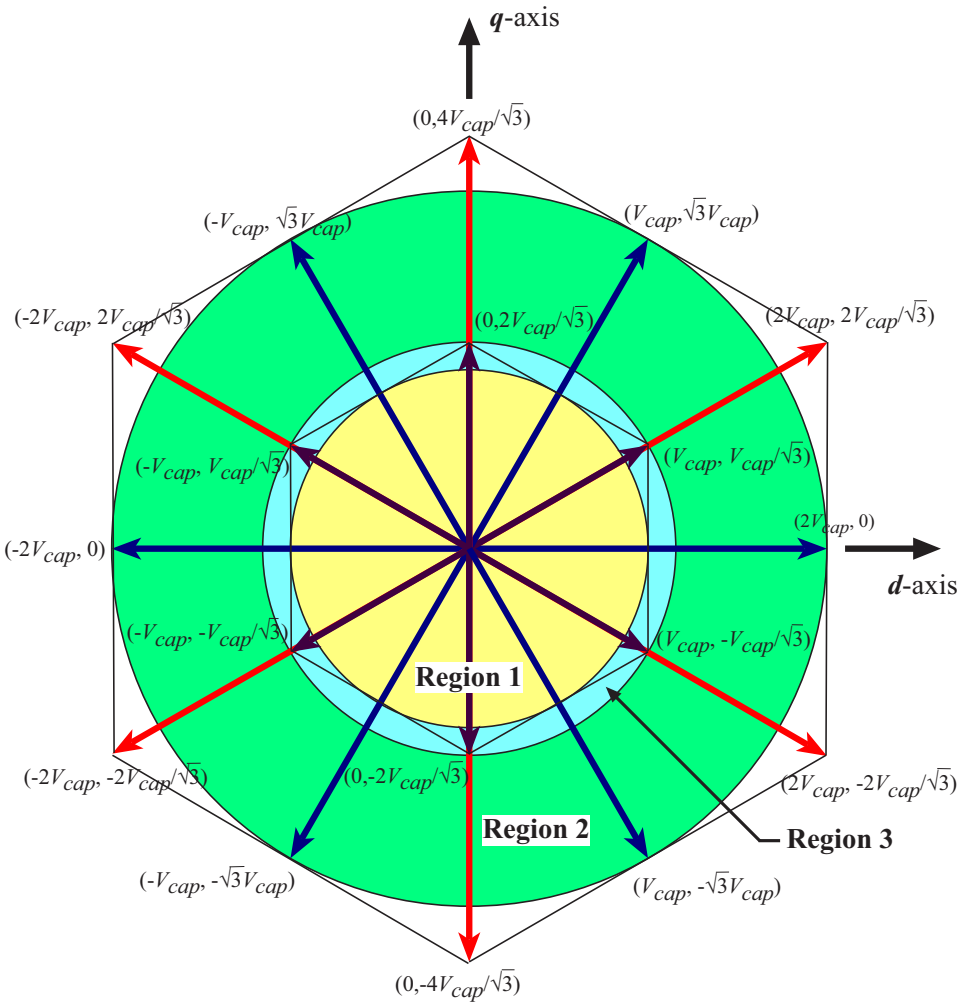


Figure 1.15: Operating regions of the multilevel matrix converter in dq diagram

To generate terminal voltages with two-level switching, the space-vector control involves the null-state space vector and the six space vectors with magnitude $2V_{cap}/\sqrt{3}$. The reference space vector must lie within the circular area inside the hexagon formed by the six space vectors with magnitude $2V_{cap}/\sqrt{3}$ (Region 1 in Fig. 1.15). In this region, the converter generates terminal line-line voltages with the maximum magnitude equal to the switch-cell capacitor voltage.

The single-capacitor control scheme and the capacitor voltage-balancing scheme have been proposed to control the converter when operating with the two-level switching. The single-capacitor control scheme is the first step to reduce the complexity of the converter. With the single-capacitor control scheme, only one switch-cell capacitor is employed to synthesize terminal AC voltages in each switching period. This allows the multilevel matrix converter to be modeled as a two-level DC-link converter. Charge balance of the single capacitor can be achieved in one complete switching period; hence, capacitor voltages in the converter are theoretically stable.

However, as a result of disturbances in the capacitor voltages caused by stray inductances inside the circuits, the capacitor voltage-balancing scheme is required to regulate and balance all nine capacitor voltages. The proposed capacitor voltage-balancing control is based on the modification of the SVM such

that two switch-cell capacitors can be charged and discharged in each switching period. The capacitor voltage-balancing control is orthogonal to the process of terminal voltage synthesizing; therefore, it can be employed with the single-capacitor control scheme. The stability of the capacitor voltages with the proposed control scheme can be confirmed by a Lyapunov's approach.

To generate terminal voltages with three-level switching, the space-vector control uses all 18 space vectors except the null-state space vector. The reference space vector must lie in the outermost band of the *dq* diagram (Region 2 in Fig. 1.15). In this operating region, the converter can generate terminal voltages with a maximum magnitude of twice the capacitor voltage. With the constraint to avoid excess voltages across open-circuited switch cells, when terminal voltages with three-level switching are generated at one side of the converter, the terminal voltages with two-level switching must be generated at the other side. Experiment validations are used to prove the capability of the converter in the three-level switching.

When operating in Region 3 of Fig. 1.15, the multilevel matrix converter generates AC voltages with both two-level switching and three-level switching in one line cycle. The approaches for the converter operating in Regions 1 and 2 are still valid for applications where capacitor voltages can be kept constant but terminal voltage magnitudes are varied. However, in the wind turbine system where the terminal voltage magnitude at one side of the converter is fixed at the utility voltage magnitude, to operate in this region the capacitor voltages must be varied with the terminal voltages. To solve this problem, two approaches can be employed.

First, by applying an over-modulation control scheme [13, 51, 52, 53] on the two-level switching when the multilevel matrix converter operates in Region 3 of Fig. 1.15, capacitor voltages can be kept constant at the utility voltage magnitude. The over-modulation control scheme allows the converter to generate terminal voltages with magnitudes 15% higher than the capacitor voltages. However, the control scheme involves a nonlinear modulation technique. As a result, the converter terminal voltages with this scheme incur more distortions and harmonics. Moreover, the nonlinear modulation requires more complex calculations.

Second, operation of the multilevel matrix converter in the Region 3 of Fig. 1.15 can be avoided by employing the proposed capacitor voltage as shown in Fig. 1.16(a). The shaded area in the figure demonstrates valid points of capacitor voltages. However, the capacitor voltages should be kept as low as possible to minimize switching losses of the semiconductor devices. When the converter operates with two-level switching at both sides, voltage magnitudes at the generator side are close to the utility voltage magnitude, and the capacitor voltages are regulated at slightly greater than the magnitude of the utility voltage. The single-capacitor control scheme and the capacitor voltage-balancing scheme are proposed for these operating points. When the voltage magnitude generated from the wind generator drops significantly below the voltage magnitude of the utility, the multilevel matrix converter can operate with three-level switching at the utility side and two-level switching at the generator side. In this operation, the capacitor voltage can be reduced below the magnitude of the utility voltage; however, it must be greater than the average of the input and output line-line voltage magnitudes. It is also possible to divide the range within which the converter operates with three-level switching into smaller ranges having different capacitor voltage levels. This will further reduce the switching losses of the converter. Hence, the prospective efficiency curve of the converter can be as shown in Fig. 1.16(b).

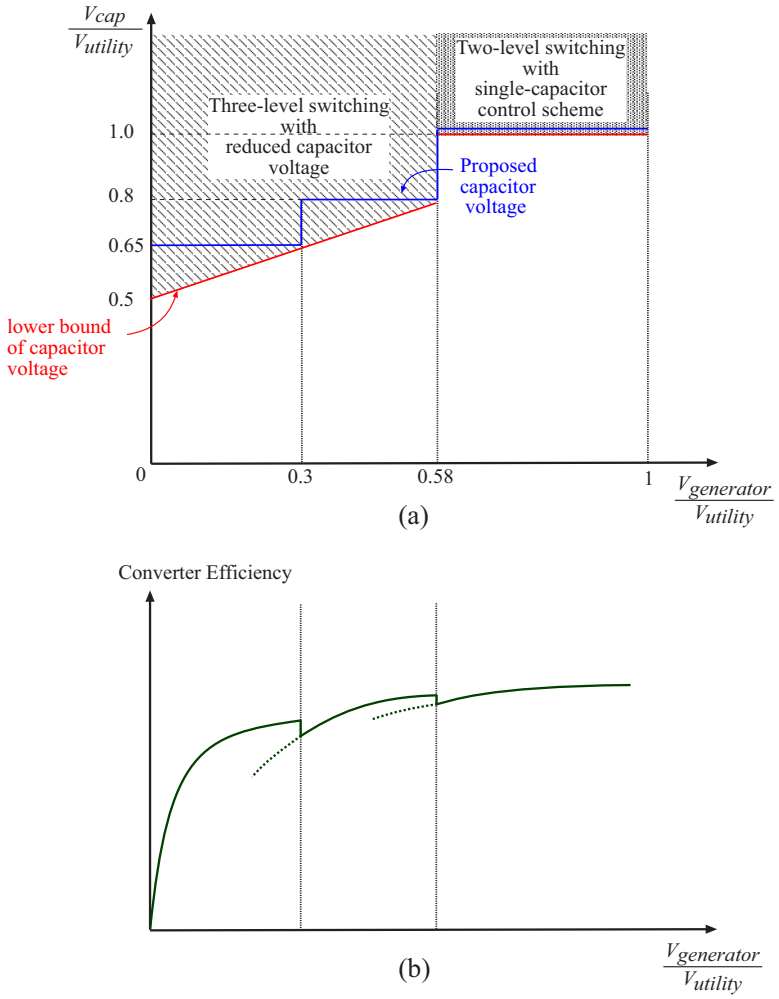


Figure 1.16: (a) Proposed capacitor voltage of the multilevel matrix converter in the wind turbine system, (b) prospective converter efficiency

1.6 Outline of Discussion

This report is divided into two major parts. Part I documents the basic operation, design, and open-loop control of the converter system. Part II extends this work to the closed-loop control of generator torque and utility-side power.

Part I is composed of six chapters. Chapter 2 describes details of the multilevel matrix converter configurations and operations. The operations and derivations of basic converter configuration, in which one switch cell is used for each branch of the matrix connection, are used to demonstrate the concepts. Chapter 2 also describes the SVM, which is employed as an approach to synthesize the terminal AC voltages of the multilevel matrix converter.

Chapter 3 explains the SVM technique for two-level switching. The proposed control schemes—the eight-capacitor control scheme and the single-capacitor control scheme—for the multilevel matrix converter operating in the two-level switching mode are described in this chapter. Experimental results to verify the proposed control scheme are also included. The experimental results also show that well-regulated capacitor voltages are necessary. A capacitor voltage-balancing control, which is based on the space-vector control technique, is described in Chapter 4.

The operations and limitations of the multilevel matrix with the three-level switching are described in Chapter 5. Experimental validations are included to show the capability of the multilevel matrix converter with the three-level switching. A possible control scheme for the converter operating in three-level switching mode is also discussed.

Implementations of the first working laboratory prototype are described in Chapter 6. The prototype was constructed to demonstrate the operation of the converter and to verify the proposed control schemes. The power stage of the multilevel matrix converter consists of the modular H-bridge switch cells and the filter inductors. The modular H-bridge switch cells were constructed in printed circuit boards. The power semiconductor devices used in the H-bridge switch cells were fast-switching Insulated Gate Bipolar Transistors (IGBTs) with anti-parallel diodes. The digital control circuit was implemented using Xilinx's Vertex II Pro, which consists of a PowerPC microprocessor and Field Programmable Gate Arrays (FPGAs), and flash memory chips as a lookup table. The control schemes for the multilevel matrix converter were implemented in the PowerPC microprocessor with Assembly language. The pulse-width modulation (PWM) control unit and the gate signal control circuits were implemented in the FPGAs using hardware description language (HDL). The use of FPGAs and lookup tables to control highly modular converters is quite attractive because it allows high-speed complex control schemes to be easily implemented in HDL code, leading to a low-cost high-performance solution to the control issue. Chapter 7 summarizes the key results of Part I.

Part II is composed of five chapters. Chapter 8 introduces the closed-loop control issues. In Chapter 9, a state-space model of the converter is developed, including transformation to stationary *d-q* coordinates and linearization about a quiescent operating point. The result is a small-signal equivalent circuit model of the converter.

Chapter 10 develops a controller design methodology that is suitable for the new multilevel matrix converter. A multi-input, multi-output controller designed using optimal control, with gain scheduling, is shown to be well suited to this application. This controller is able to regulate the generator current magnitudes and phase angles with space-vector control and, hence, is well suited to torque and vector control of the generator. It can also simultaneously regulate the utility-side power factor and the internal capacitor voltage magnitudes.

The performance of the proposed controller is validated experimentally in Chapter 11. It is shown that this controller can regulate the experimental prototype developed in Part I. Algorithms that implement the controller within the PowerPC microcontroller are described.

The key results of Part II are summarized in Chapter 12.

Part I
Basic Converter Operation and Design

2 Multilevel Matrix Converters

This chapter describes an overview of the configuration and operation of the multilevel matrix converter. The basic configuration of the converter, in which nine switch cells are employed in the switch network, is used to demonstrate the concept. An approach to generate valid switching-device combinations from given terminal voltages is also described. Afterward, the SVM technique, which is employed for synthesizing terminal voltages, is introduced. The multilevel matrix converter can generate, at each side, 19 combinations of three-phase line-line voltages, which correspond to 19 space vectors in the dq coordinate: six space vectors with magnitude $2V_{cap}/\sqrt{3}$, six space vectors with magnitude $2V_{cap}$, six space vectors with magnitude $4V_{cap}/\sqrt{3}$, and a null-state space vector. The null-state space vector and the six space vectors with magnitude $2V_{cap}/\sqrt{3}$ are employed in the two-level switching. The 18 non-zero space vectors are employed in the three-level switching.

2.1 Configurations of the Multilevel Matrix Converter

A basic configuration of the multilevel matrix converter is illustrated in Fig. 2.1. The multilevel matrix converter contains nine four-quadrant switches connected between each input phase and each output phase, resembling a conventional matrix converter. However, the four-quadrant switches are realized as capacitor-clamped H-bridge switch cells, as illustrated in Fig. 2.2. Each switch cell is similar to the cell

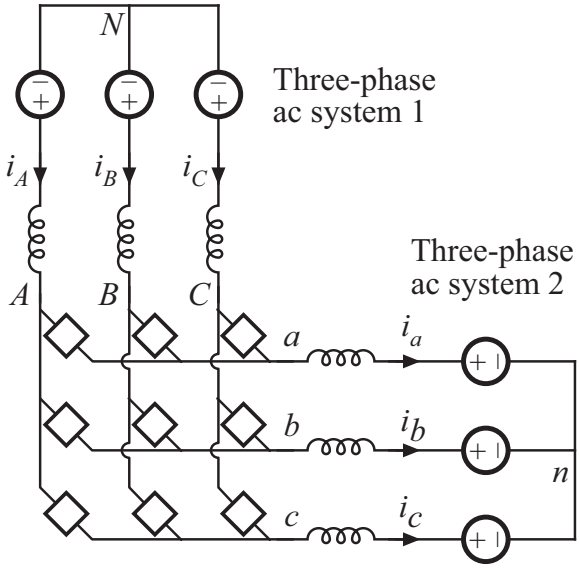


Figure 2.1: Basic configuration of a multilevel matrix converter

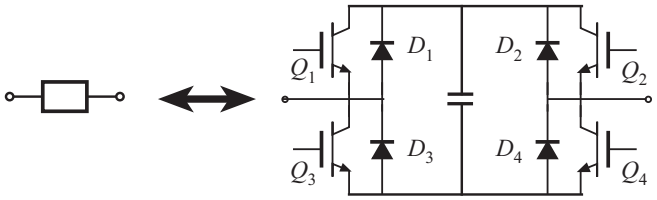


Figure 2.2: Schematic diagram of an H-bridge capacitor clamped switch cell

shown in Fig. 1.12 for the multilevel DC-link converter, except that the DC voltage sources in the H-bridge switch cells are replaced by simple DC capacitors because the use of the matrix configuration allows the converter to deliver average power without external DC voltage sources.

The multilevel matrix converter synthesizes AC line-line voltages at both sides from PWM of the switch-cell capacitor voltages. This operation differs from that of the conventional matrix converter in which voltages are synthesized on one side and currents on the other side. As a result, inductors are employed as filter elements at both sides of the multilevel matrix converter. These inductors may be physically discrete elements, or they may be inductances of other system elements, such as machine-winding inductances and transformer-leakage inductances. With the symmetry structure of the multilevel matrix converter, both step-up and step-down of voltage magnitudes are possible.

With the inductors connected to each input and output phase of the multilevel matrix converter, the operation of the switch cells in the converter must not interrupt the inductor currents. In addition, the operation of the switch cells must not create a closed-loop inside the switch network. Consequently, the multilevel matrix converter requires exactly five H-bridge switch cells conducting currents at any given instant.

The use of switch cells based on the H-bridge circuits leads to a simple bus-bar structure: simple modular construction. The voltages across transistors and diodes within each switch cell are locally clamped to the DC capacitor voltage, which can be regulated via feedback. Furthermore, with proper control of the current stresses to evenly spread over all four devices in the switch cell, the average current through the switch cell can be doubled in the conventional matrix converter, compared to a four-quadrant switch, which uses two transistors and two diodes,.

The H-bridge switch-cell configuration also allows the application of a simple switching transition procedure to avoid cross-conduction and shoot-through currents, which can occur during transitions of semiconductor devices in each switch cell. One method for coordinating the switching transition is “break before make” operation, which is to first turn off all transistors that are to be switched off and, after a short delay, turn on the transistors that are to be switched on. Turning off the transistors of five or more switch cells does not cause a calamity because the anti-parallel diodes inside the switch cells can provide paths for the inductor currents to flow continuously. Energy stored in the filter inductors, as well as the parasitic inductance in the winding of the switch-cell interconnections, is then transferred to the switch-cell capacitors.

In the basic configuration of the multilevel matrix converter, the converter operation can be divided into two operational modes. The first operational mode is where the converter generates terminal voltages with two-level switching at both sides. The converter operates in this mode when the voltage magnitudes of both sides are about the same and the capacitor voltages are regulated to be slightly greater than the line-line voltage magnitudes of both sides. Note that the number of voltage levels is conventionally referred to as the number of voltage levels in the line-neutral voltage; generally there are more voltage levels happening at the line-line voltages. With two-level switching, the line-line voltages of the converter are switched at three voltage-levels: $+V_{cap}$, 0, and $-V_{cap}$, where V_{cap} is the capacitor voltage. In the second operational mode, the multilevel matrix converter generates voltages with two-level switching at one side and voltages with three-level switching at the other side. The converter can operate in this mode only when the voltage magnitudes at both sides are significantly different. The line-line voltages of the converter at the side with three-level switching have voltage-levels of $-2V_{cap}$, $-V_{cap}$, 0, $+V_{cap}$, and $+2V_{cap}$.

The number of voltage levels can be further increased by connecting more H-bridge switch cells in series. For example, the configuration of the multilevel matrix converter (Fig. 2.3) contains two series-connected H-bridge switch cells in each branch of the matrix connection. This converter is capable of operating with three-level switching at the full-rated operating point when voltage magnitudes at both sides of the converter are close to each other and with four-level switching when the voltage magnitudes at both sides are significantly different. This approach allows the direct increase of the terminal voltage magnitudes without changing the voltage ratings of the semiconductor devices.

In this research, the proposed control algorithms are based on the multilevel matrix converter with the basic configuration in which one switch cell is used for each branch of the switch network. They can be adapted for the multilevel matrix converter that has more than one switch cell per branch of the switch network; however, additional control algorithms for controlling and regulating additional switching devices and capacitors are required.

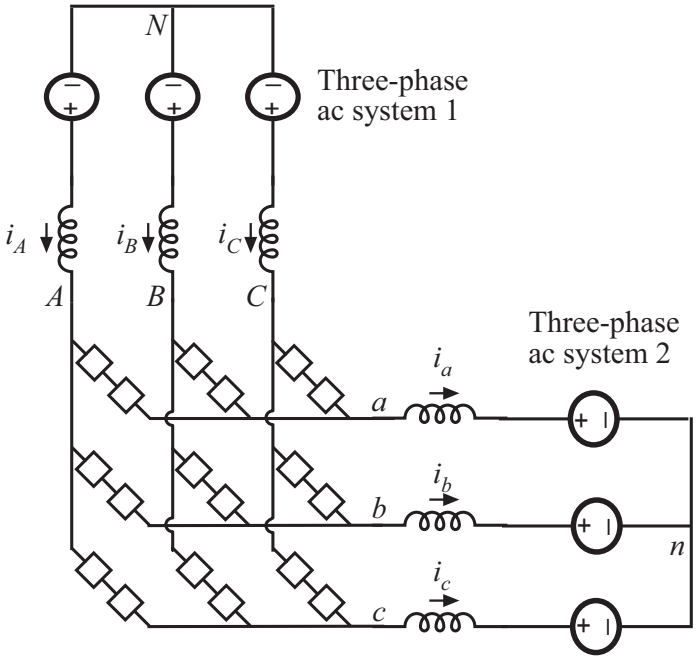
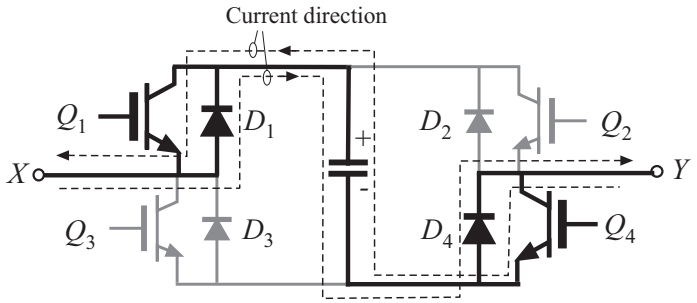


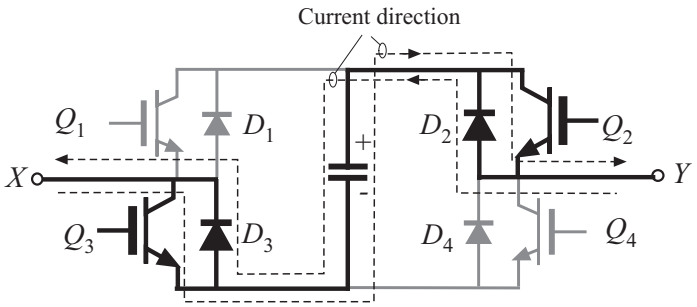
Figure 2.3: A multilevel matrix converter containing two of the switch cells in each branch to increase voltage-levels

2.1.1 States of Switch Cell

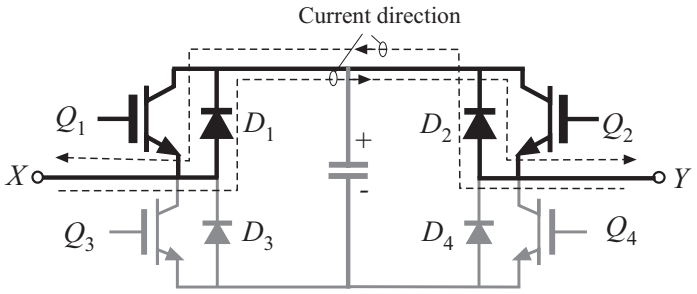
Each H-bridge switch cell can provide three different voltage levels when it conducts current and is able to block voltage magnitudes less than the DC capacitor voltage: $+V_{cap}$, 0, and $-V_{cap}$. The voltage between terminals of each switch cell can be controlled by states of the switching devices, independent of the current direction through the switch cell. Operations of the H-bridge switch cell when the devices conduct current are illustrated in Fig. 2.4. Node X and node Y are assumed to be an input phase and an output phase of the converter terminals, respectively.



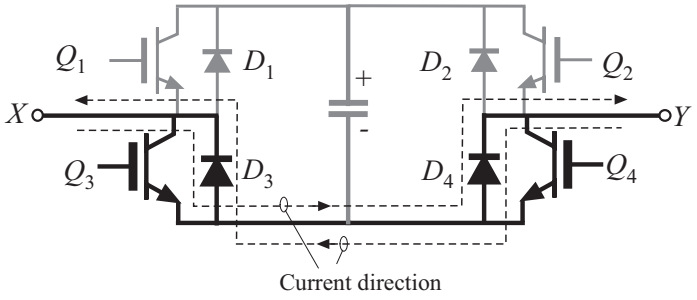
(a) State 1



(b) State 2



or



(c) State 3

Figure 2.4: Three states of the H-bridge switch cell when devices conduct current

State 1: The positive polarity of the capacitor is connected to node X and the negative polarity of the capacitor is connected to node Y (Fig. 2.4[a]). Transistors Q_1 and Q_4 are turned on. When the current flows from node X to node Y, diodes D_1 and D_4 conduct the current, and then the capacitor is charged. When the current flows from node Y to node X, transistors Q_1 and Q_4 conduct the current, and then the capacitor is discharged.

State 2: The positive polarity of the capacitor is connected to node Y, and the negative polarity of the capacitor is connected to node X (Fig. 2.4[b]). Transistors Q_2 and Q_3 are turned on. When the current flows from node X to node Y, transistors Q_2 and Q_3 conduct the current, and then the capacitor is discharged. When the current flows from node Y to node X, diodes D_2 and D_3 conduct the current, and then the capacitor is charged.

State 3: Node X and node Y are shorted together (Fig. 2.4[c]). This can be accomplished by turning on either the upper transistors, Q_1 and Q_2, or the lower transistors, Q_3 and Q_4, of the H-bridge switch cell. In either case, only one transistor and one diode conduct the current. It is advantageous to alternate the conducting devices, so that the conduction losses are distributed over the devices.

State 4: The switch cell is open-circuited. All switching devices are turned off. The terminal voltage magnitude between node X and node Y must be less than the DC capacitor voltage; otherwise, the diodes in the switch cell will forward bias and change the state of the switch cell into state 1 or state 2.

2.1.2 Branch Connections

Similar to the conventional matrix converter, the operation of multilevel matrix converter has constraints from the passive elements inside the converter. First, because of the inductors at both input and output phases, currents must flow continuously through the inductors. Therefore, the operation of the multilevel matrix converter must never result in open circuit of each input and output phase. Second, the branches in the switch network must never conduct in a way that forms a closed loop within the switch matrix. The term *branch* refers to a connection between an input phase and an output phase using one or more switch cells.

For a three-phase input and three-phase output system (nine branches in the switch network), the above constraints imply that the converter must operate with exactly five branches in the switch matrix conducting at any given instant. Although in some special cases, it is possible to allow more than five branches to conduct. There exist 81 cases of branch connections that satisfy the above constraints, which are included in Appendix A.

The followings are the summarized rules for branch connections in the multilevel matrix converter [49]:

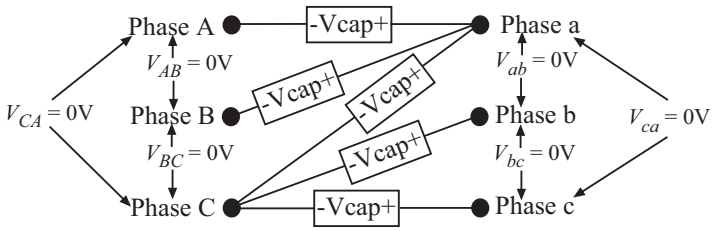
1. There is exactly one and only one conducting path between any two phases.
2. If any phase on one side (input side or output side) has two conducting branches (is connected to two phases from the other side), then there must be exactly one other phase from the same side having two conducting branches. The third phase must have only one conducting branch.
3. If any phase on one side (input side or output side) has three conducting branches (is connected to all phases from the other side), then the other two phases from the same side have one and only one conducting branch.

2.2 Switching-Device Combinations

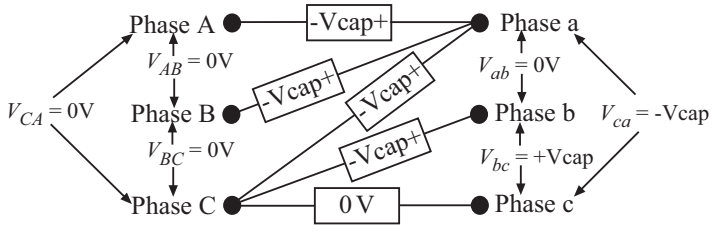
2.2.1 Constraints for Switching-Device Combinations

With five switch cells conducting currents at any given instant and each conducting switch cell having a potential of three different states, there are $3^5 = 243$ possible combinations of switch states for a given branch connection. As previously stated, there are 81 valid branch connections for the multilevel matrix converter. This leads to $243 \times 81 = 19{,}683$ combinations of the switch states and branch connections, referred to as "switching-device combinations," for the converter. Nevertheless, several switching-device combinations are not practical, and most of them can be generated by rotation of the input or output phase of previously generated combinations.

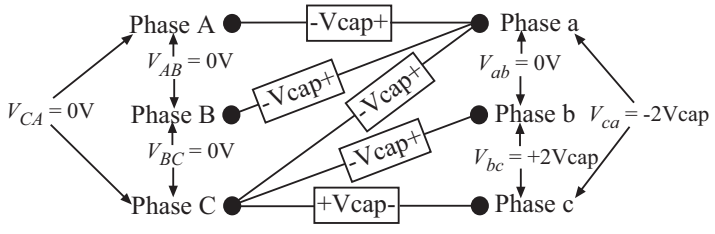
Figure 2.5 illustrates examples of different switching-device combinations for the choice of branch connection having branches *Aa*, *Ba*, *Ca*, *Cb*, and *Cc* connected and branches *Ab*, *Ac*, *Bb*, and *Bc* disconnected. Branch *Aa* uses switch cell S_{Aa}, branch *Ba* uses switch cell S_{Ba}, etc. These configurations show that it is possible to obtain five different voltage levels at line-line voltages from the multilevel matrix converter with the basic configuration, having one switch cell per branch. The configuration in Fig. 2.5(a) generates zero line-line voltages at both sides of the converter from the DC capacitor voltages,



(a)



(b)



(c)

Figure 2.5: Examples of different switching-device combinations in the multilevel matrix converter

V_{cap}. This is done by operating all switch cells of the connected branches in State 2. The same result can also be obtained by operating all switch cells in State 1 or State 3. Figure 2.5(b) illustrates what happens when the switch cell S_{Cc} is changed to State 3. The converter then produces three different voltage magnitudes ($-V_{cap}$, 0, and $+V_{cap}$) at the output line-line voltages. Figure 2.5(c) illustrates the result of changing the switch cell S_{Cc} to State 1. Consequently, the output line-line output voltages are $-2V_{cap}$, 0, and $+2V_{cap}$. By alternating among the three switching-device combinations in Fig. 2.5, the multilevel matrix converter can produce five-level line-line voltages with voltage levels of $-2V_{cap}$, $-V_{cap}$, 0, $+2V_{cap}$, and $+2V_{cap}$ at one side of the converter.

As mentioned previously, the H-bridge switch cell can block voltages with magnitudes less than the DC capacitor voltage of the switch cell, when all devices in the switch cell are turned off (State 4). With the basic configuration, when the multilevel matrix converter generates the line-line voltages with a magnitude of twice the capacitor voltage from two series-connected switch-cell capacitors, all phases on the other side of the converter must have voltage potentials equal to the voltage potential at the midpoint of the two series-connected capacitors. This avoids applying voltage exceeding capacitor voltage across open-circuited switch cells. As a result, when the multilevel matrix converter generates line-line voltages with twice the capacitor voltage on one side, all line-line voltages on the other side of the converter must remain at zero. For instance, in the switching-device combination shown in Fig. 2.5(c), all line-line voltages on the left-hand side of the converter are equal to zero, while the line-line voltages V_{bc} and V_{ca} on the right-hand side have a magnitude of twice the capacitor voltage. It can be verified that all switch cells of the open-circuited branches S_{Ab}, S_{Ac}, S_{Bb}, and S_{Bc}, block voltages with magnitudes equal to V_{cap}.

An example of invalid switching-device combination is demonstrated in Fig. 2.6. In this example, the line-line voltages V_{bc} and V_{ca} on the right-hand side of the converter have a magnitude of twice the capacitor voltage, whereas the line-line voltages V_{BC} and V_{CA} on the left-hand side of the converter have magnitudes of the capacitor voltage. Phase C has voltage potential different from the voltage potential at the midpoint of the two series-connected capacitors. Consequently, the switch cell S_{Cc} has to block a voltage with magnitude $2V_{cap}$. In practice, this kind of configuration could not happen because diodes in those switch cells would be forward-biased, changing the states of the switch cells into conduction states, State 1 or 2. As a result, a closed-loop circuit inside the switch network can be formed, and it then changes the terminal voltages.

As a result of the constraint described above, the maximum instantaneous line-line voltage magnitude of the multilevel matrix converter with the basic configuration is limited to twice the capacitor voltage. In other words, for the multilevel matrix converter with N series-connected switch cells in each branch of the switch network, the possible voltage levels of the terminal line-line voltages can vary from $-2NV_{cap}$ to $+2NV_{cap}$.

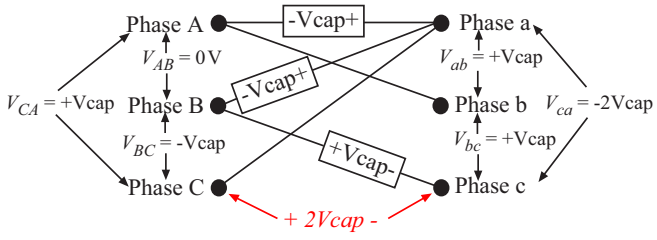


Figure 2.6: An example of invalid switching-device combination having $2V_{cap}$ across the non-conducting switch cells

In PWM, the above constraint implies that the multilevel matrix converter with basic configuration can operate with the instantaneous line-line voltages exceeding the capacitor voltage only when the voltage magnitudes at both sides of the converter are significantly different. The side that has line-line voltage magnitudes exceeding the capacitor voltage operates with three-level switching, while the other side operates with two-level switching.

2.2.2 Generating Valid Switching-Device Combinations

To generate a valid switching-device combination, all line-line voltages are used to determine voltages across all nine switch cells. Those switch cells that have the same voltage potential at both terminals are switched to the short-circuited state (State 3), while those switch cells that have $\pm V_{cap}$ across their terminals are operated with their capacitors connected according the voltages between their terminals. After states of all nine switch cells are determined, five of nine branches that satisfy the constraints of the branch connection described in Section 2.1.2 can be chosen to form a valid switching-device combination. The processes to generate valid switching-device combinations can be divided into three cases depending on the voltage levels generated by the converter.

2.2.2.1 Case 1

For the case when the line-line voltages of the multilevel matrix converter have magnitudes of $+V_{cap}$, 0, and $-V_{cap}$ (two-level switching) at both sides, the polarities of capacitors at the input and the output phases can be determined directly. Zero line-line voltage leads to the two phases connected to the same polarity of capacitors. Then, the states of all nine switch cells can be determined by the voltage difference between the two phases that they are connected to. For example, suppose that the terminal voltages of the converter are $V_{AB} = -V_{cap}$, $V_{BC} = 0$ V, $V_{CA} = +V_{cap}$, $V_{ab} = +V_{cap}$, $V_{bc} = 0$ V, and $V_{ca} = -V_{cap}$ (Fig. 2.7). Then, the voltage $V_{AB} = -V_{cap}$ determines that the input phase A must be connected to the negative polarity of the switch-cell capacitors, and the input phase B must be connected to the positive polarity of the capacitors. The voltage $V_{BC} = 0$ V indicates that the input phase C must be connected to the positive polarity of the capacitors as well. Likewise, the output phase a must be connected to the positive polarity of the switch-cell capacitors, while the output phases b and c must be connected to the negative polarity of the capacitors. Because the input phases B and C and the output phase a have the same voltage potential (at the negative capacitor polarity), the switch cells connected between those phases, S_{Ba} and S_{Ca}, are operated in State 3 (short-circuited state). Similarly, the input phase A and the output phases b and c also have the same voltage potential (at the positive capacitor polarity); therefore, S_{Ab} and S_{Ac} are operated in State 3 as well. The remaining switch cells are operated such that they provide correct voltages between the two phases to which they are connected . For instance, the voltage difference between the input phase A and the output phase a is $+V_{cap}$; therefore, the switch cell S_{Aa} is operated in State 2. Analogously, the switch cells S_{Bb}, S_{Bc}, S_{Cb}, and S_{Cc} are operated in State 1.

More caution is necessary when the multilevel matrix converter has all zero line-line voltages at one side. Every phase on the side that has all zero line-line voltages can have voltage potential at either positive or negative capacitor polarity. As a result, more valid switching combinations can be generated.

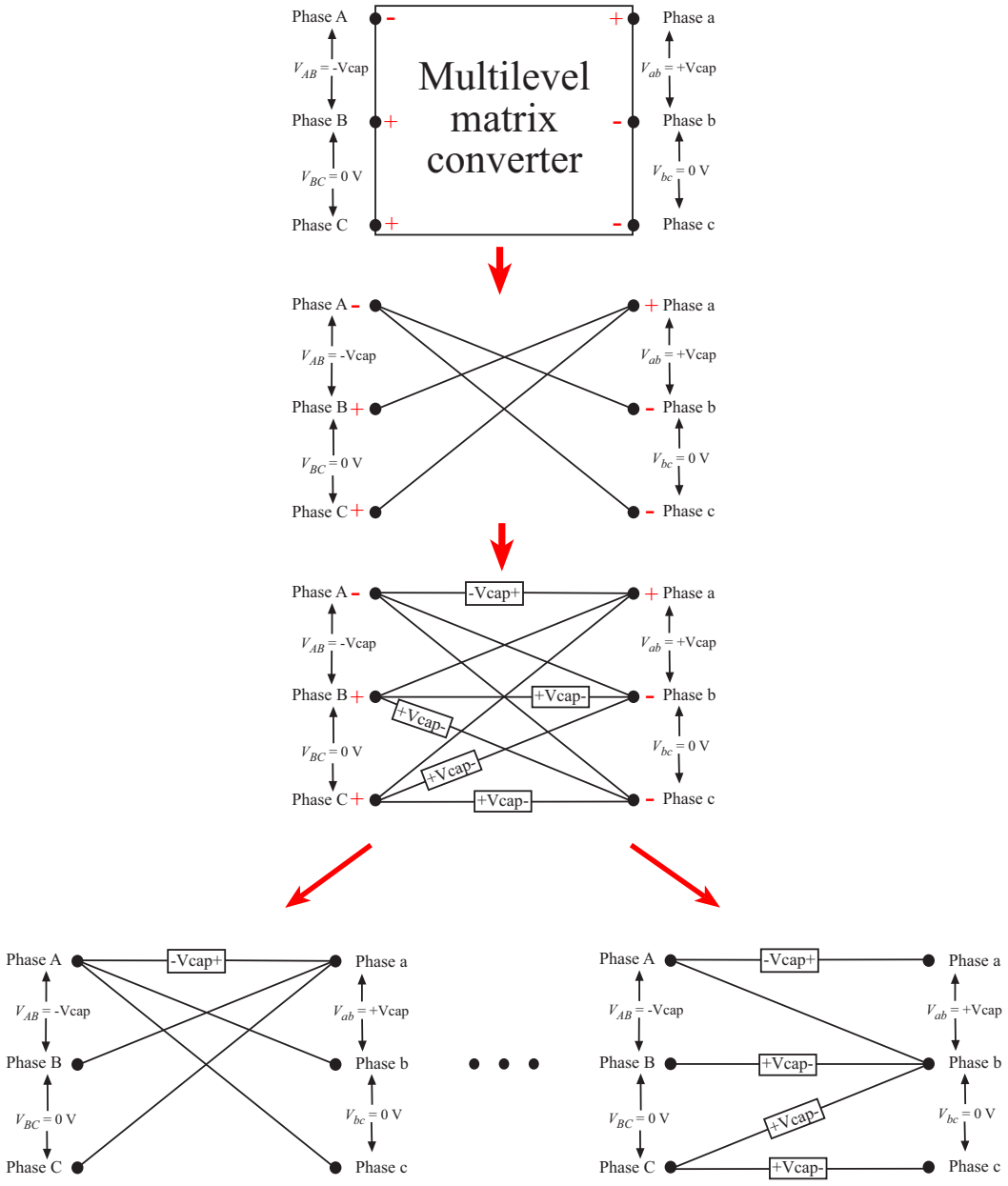


Figure 2.7: Generating valid switching combinations: Case 1

2.2.2.2 Case 2

In this case, when only one of the converter line-line voltages has a magnitude of twice the capacitor voltage, two capacitors are series-connected between those two lines. The midpoint of the two series-connected capacitors can be at any phase on the other side of the converter because they all have the same voltage potential to avoid excess voltages across open-circuited switch cells. The remaining phase on the same side also has voltage potential at the mid-point voltage and, therefore, can be directly connected to any phase on the other side of the converter. Then, the states of the remaining switch cells can be determined by the voltage difference between two phases that they are connected to.

For instance, assume that line-line voltages of the converter are $V_{AB} = V_{BC} = V_{CA} = 0$ V, $V_{ab} = +2V_{cap}$, $V_{bc} = -V_{cap}$, and $V_{ca} = -V_{cap}$ (Fig. 2.8). The output phase *a* is connected to the most positive point of two series-connected capacitors, whereas the output phase *b* is connected to the most negative point. The voltage potential at the output phase *c* is equal to the midpoint voltage to provide $V_{bc} = -V_{cap}$ and $V_{ca} = -V_{cap}$. This means that the input phases *A*, *B*, *C* and the output phase *c* have the same voltage potential. Therefore, the switch cells S_{Ac}, S_{Bc}, and S_{Cc} are operated in short-circuited state. With voltage $-V_{cap}$ between each input phase and the output phase *a*, the switch cells S_{Aa}, S_{Ba}, and S_{Cb} are operated in State 2. Likewise, there are voltages with magnitude $+V_{cap}$ between each input phase and the output

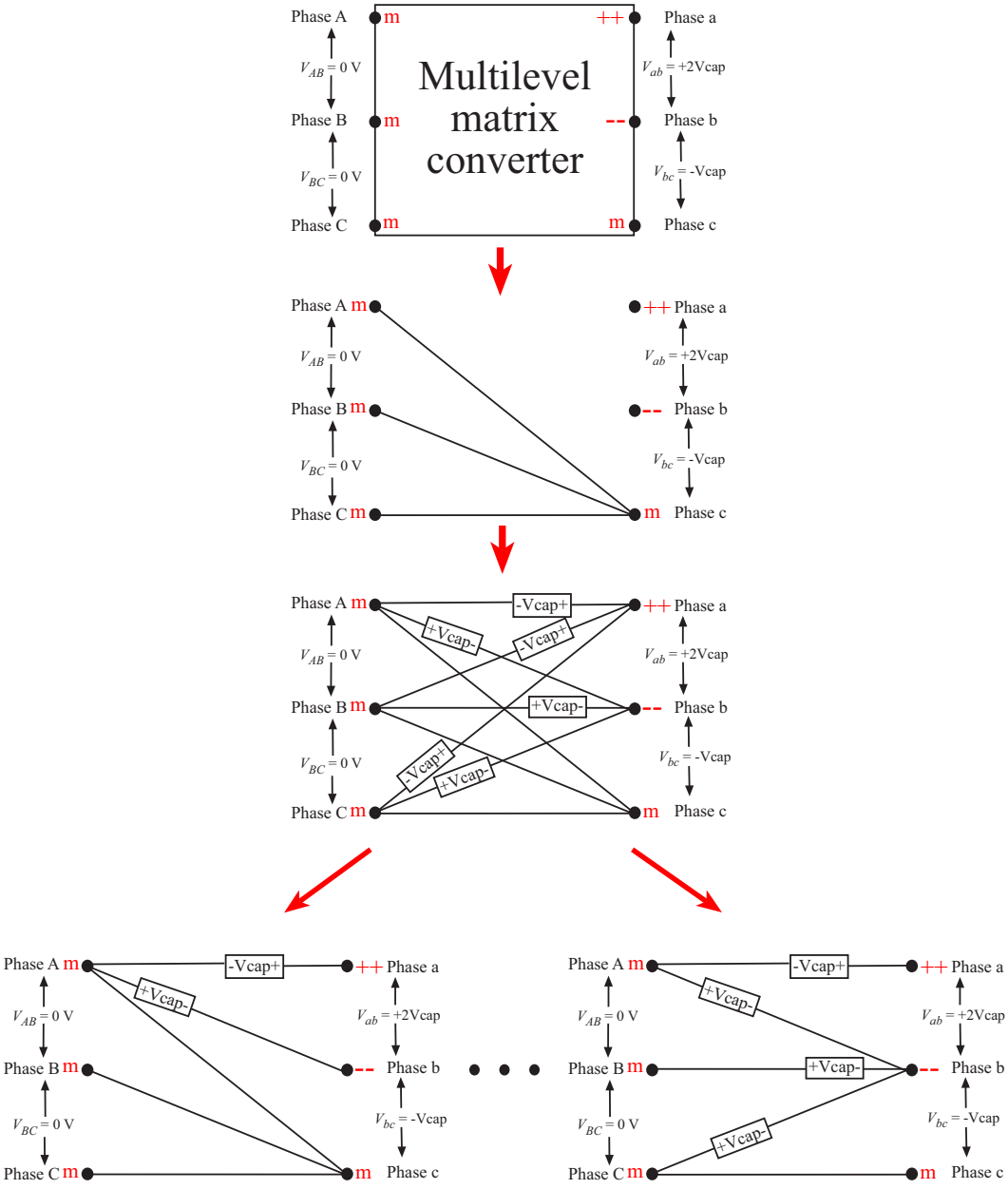


Figure 2.8: Generating valid switching combination: Case 2

phase *b*, the switch cells S_{Ab}, S_{Bb}, and S_{Cb}, therefore, are operated in State 1. The operations of all nine switch cells for this example are illustrated in Fig. 2.8.

2.2.2.3 Case 3

To generate switching-device combinations for the multilevel matrix converter having line-line voltage magnitudes of $+2V_{cap}$, 0 V, and $-2V_{cap}$, the concepts from the pervious cases are adapted. The line-line voltage with a magnitude of twice the capacitor voltage can be obtained by the series-connection of two capacitors. Zero line-line voltage means that the two lines have the same voltage potential, which can be achieved by series-connecting two switch-cell capacitors in opposite directions. In this case, only phases on the other side of the converter have voltage potential at the midpoint voltage of the two series-connected capacitors. As a result, no switch cell is operated in short-circuited state (State 3).

An example for this case is shown in Fig. 2.9, where the line-line voltages of the converter are $V_{AB} = V_{BC} = V_{CA} = 0$ V, $V_{ab} = +2V_{cap}$, $V_{bc} = 0$ V, and $V_{ca} = -2V_{cap}$. The voltage $V_{ab} = +2V_{cap}$ indicates that the output phase *a* is connected to the most positive point of the two series-connected capacitors, whereas the output phase *b* is connected to the most negative point of the two series-connected capacitors. The $V_{bc} = 0$ V voltage makes the voltage potentials at the output phases *b* and *c* to be the same. All input phases have voltage potentials equal to the voltage potential at the mid-point of the series-connected

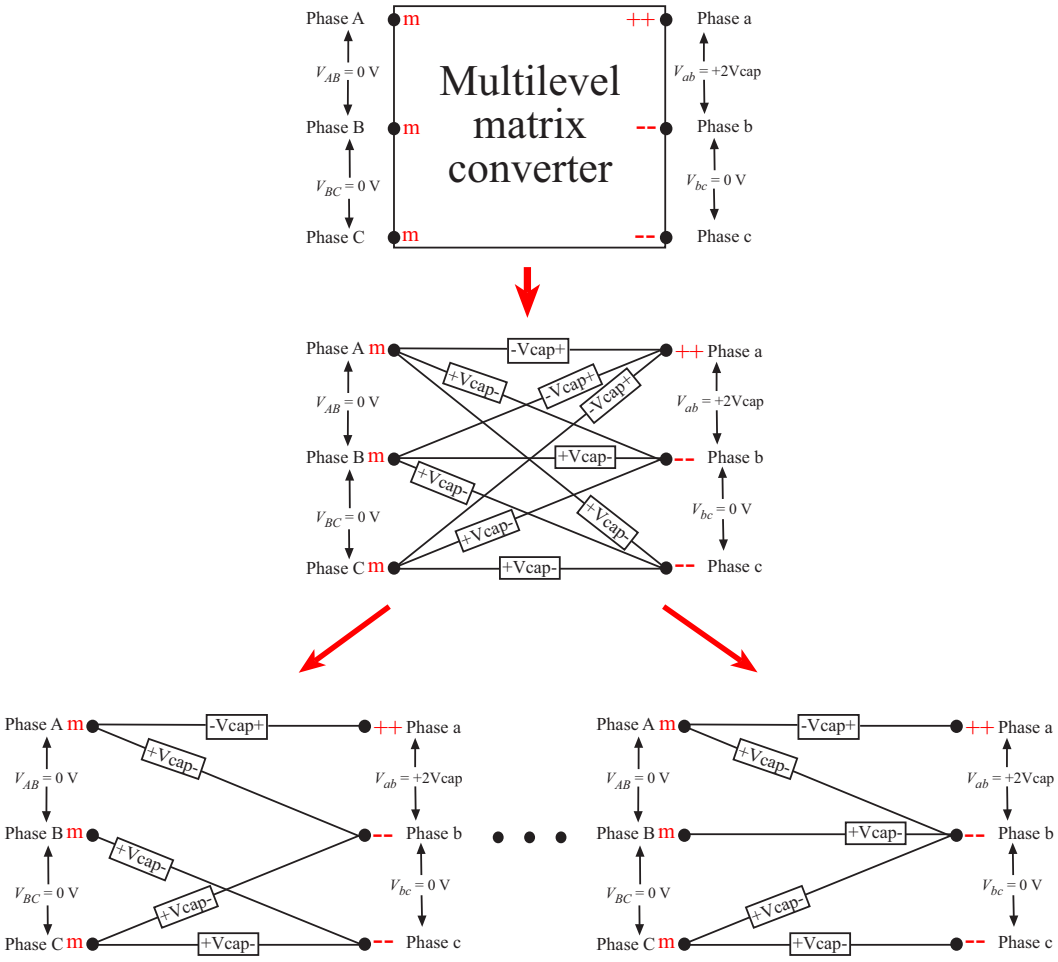


Figure 2.9: Generating valid switching combination: Case 3

capacitors. With voltage $-V_{cap}$ between each input phase and the output phase *a*, the switch cells S_{Aa}, S_{Ba}, and S_{Ca} are operated in State 2. Likewise, with voltages $+V_{cap}$ between each input phase and the output phase *b* and the output phase *c*, the switch cells S_{Ab}, S_{Bb}, S_{Cb}, S_{Ac}, S_{Bc}, and S_{Cc} are operated in State 1.

2.2.3 Redundant Switching Combinations

In the previous section, a valid switching-device combination is constructed from selecting five of nine branches in the switch network that satisfy the constraints of branch connection. Regardless of the combinations of five branches, all combinations generate identical line-line voltages of the multilevel matrix converter. For switching-device combinations that generate identical converter voltages, they can be considered as "redundant switching combinations." The redundant switching combinations in the multilevel matrix converter are analogous to those in the multilevel DC-link converter. They are generally used for regulating capacitor voltages because different converter configurations can be employed to generate the same terminal voltages, but those terminal voltages will have different currents through switch-cell capacitors.

For instance, Fig. 2.10 illustrates four different switching-device combinations that provide identical line-

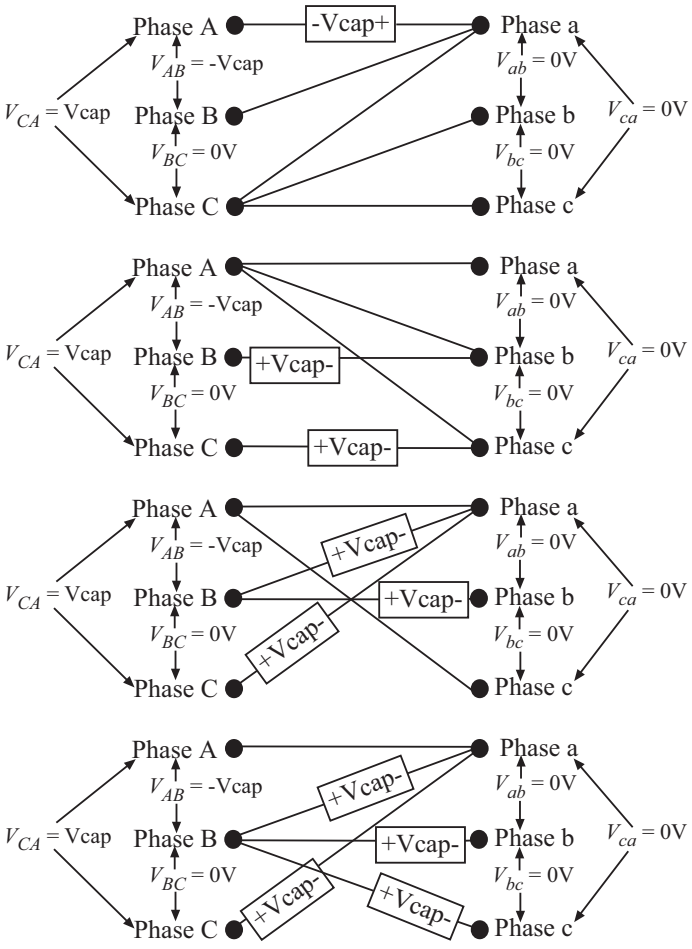


Figure 2.10: Examples of redundant switch combinations

line voltages ($V_{AB} = -V_{cap}$, $V_{BC} = 0$ V, $V_{CA} = +V_{cap}$, and $V_{ab} = V_{bc} = V_{ca} = 0$ V). However, the switching-device combinations involve different branch connections and switch-cell capacitors. As a result, different currents flow through the switch-cell capacitors. For example, in the first switching-device combination, the input current I_A flows through the switch-cell capacitor C_{Aa}, while in the second switching-device combination, the input current I_B and the input current I_C flow through the switch-cell capacitors C_{Bb} and C_{Cc}, respectively. Note that the net charges (currents) through all switch-cell capacitors in redundant-switch combinations are also the same; the net charges depend on the terminal voltages.

All valid switching-device combinations are included in Appendix B. The switching-device combinations are grouped into a table as redundant switching combinations that generate the given combination of the input and the output voltages. Currents through the capacitors involved in each switching device combinations are also included.

During operation, a switching-device combination must be chosen from the redundant switching combinations to synthesize the terminal AC voltages. A switching-device combination might be chosen such that more than one switch-cell capacitor can be regulated simultaneously. However, to search a suitable switching-device combination for regulating capacitor voltages from a large number of the redundant switching combinations is difficult for a real-time control. A simple control scheme that can determine a suitable switching-device combination from a given terminal voltage and capacitor combination is proposed and described in the next chapter. The control scheme is valid within a range of voltage-gain ratios, with arbitrary power factors at both converter terminals.

2.3 Space-Vector Control

Space-vector control is adapted for the multilevel matrix converter as a technique to synthesize the terminal voltages of the converter. This control technique is based on a transformation of three-phase variables into a simpler two-coordinate variable without loss of information, generally called *dq* coordinate. The space-vector control technique has been proven possible to considerably simplify the complexity of the mathematical model [5]. In addition, the SVM can perform a better harmonic rejection capability than does the sinusoidal PWM [28].

2.3.1 *d-q* Transformation

An analysis of three-phase systems can be simplified by transforming the three-phase variables into equivalent two-phase *dq* variables using the following *dq* transformation:

$$v(t) = \begin{bmatrix} v_d(t) \\ v_q(t) \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos(0) & \cos(\frac{2\pi}{3}) & \cos(\frac{4\pi}{3}) \\ \sin(0) & \sin(\frac{2\pi}{3}) & \sin(\frac{4\pi}{3}) \end{bmatrix} \begin{bmatrix} v_x(t) \\ v_y(t) \\ v_z(t) \end{bmatrix} \tag{2.1}$$

where $v_x(t)$, $v_y(t)$, and $v_z(t)$ are voltages in a three-phase system.

The transformation can also be expressed in a complex-variable form as follows:

$$\vec{v}(t) = v_d(t) + jv_q(t) = \frac{2}{3}(v_x(t) + v_y(t)e^{\frac{2\pi}{3}} + v_z(t)e^{\frac{4\pi}{3}}) \tag{2.2}$$

The steady-state quantities of $v_d(t)$ and $v_q(t)$ from the transformation of Eqs. (2.1) or (2.2) are sinusoids. In practice, the second transformation

Table 2.1: Combinations of Line-Line Voltages and the Corresponding Space Vectors Attained from the Multilevel Matrix Converter with the Basic Configuration

Three-phase variables			DQ variables	
V_{ab}	V_{bc}	V_{ca}	V_d	V_q
0	0	0	0	0
V_{cap}	0	$-V_{cap}$	V_{cap}	$V_{cap}/\sqrt{3}$
0	V_{cap}	$-V_{cap}$	0	$2V_{cap}/\sqrt{3}$
$-V_{cap}$	V_{cap}	0	$-V_{cap}$	$V_{cap}/\sqrt{3}$
$-V_{cap}$	0	V_{cap}	$-V_{cap}$	$-V_{cap}/\sqrt{3}$
0	$-V_{cap}$	V_{cap}	0	$-2V_{cap}/\sqrt{3}$
V_{cap}	$-V_{cap}$	0	V_{cap}	$-V_{cap}/\sqrt{3}$
$2V_{cap}$	$-V_{cap}$	$-V_{cap}$	$2V_{cap}$	0
V_{cap}	V_{cap}	$-2V_{cap}$	V_{cap}	$\sqrt{3}V_{cap}$
$-V_{cap}$	$2V_{cap}$	$-V_{cap}$	$-V_{cap}$	$\sqrt{3}V_{cap}$
$-2V_{cap}$	V_{cap}	V_{cap}	$-2V_{cap}$	0
$-V_{cap}$	$-V_{cap}$	$2V_{cap}$	$-V_{cap}$	$-\sqrt{3}V_{cap}$
V_{cap}	$-2V_{cap}$	V_{cap}	V_{cap}	$-\sqrt{3}V_{cap}$
$2V_{cap}$	0	$-2V_{cap}$	$2V_{cap}$	$2V_{cap}/\sqrt{3}$
0	$2V_{cap}$	$-2V_{cap}$	0	$4V_{cap}/\sqrt{3}$
$-2V_{cap}$	$2V_{cap}$	0	$-2V_{cap}$	$2V_{cap}/\sqrt{3}$
$-2V_{cap}$	0	$2V_{cap}$	$-2V_{cap}$	$-2V_{cap}/\sqrt{3}$
0	$-2V_{cap}$	$2V_{cap}$	0	$-4V_{cap}/\sqrt{3}$
$2V_{cap}$	$-2V_{cap}$	0	$2V_{cap}$	$-2V_{cap}/\sqrt{3}$

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \begin{bmatrix} \cos(\omega t) & \sin(\omega t) \\ -\sin(\omega t) & \cos(\omega t) \end{bmatrix} \begin{bmatrix} v_d(t) \\ v_q(t) \end{bmatrix} \tag{2.3}$$

is employed to convert the rotate waveforms of $v_d(t)$ and $v_q(t)$ into a frame of reference that is stationary with respect to time.

The transformation of Eq. (2.3) is useful for control of three-phase line currents, but is not directly used in SVM. It should be noted that this second transformation is not included in Eq. (2.1).

2.3.1.1 Reference Voltage in the *dq*-Coordinate

For the three-phase converter applications, balanced three-phase sinusoidal voltages are usually desired. In the space-vector control technique, this corresponds to producing a space vector of constant amplitude, which rotates at the desired frequency. Suppose that the desired line-line voltages are expressed as

$$
\begin{aligned}
v_{ab}(t) &= V_m \cos(\omega t) \\
v_{bc}(t) &= V_m \cos(\omega t - 120^\circ) \\
v_{ca}(t) &= V_m \cos(\omega t - 240^\circ)
\end{aligned}
\tag{2.4}
$$

where V_m denotes the magnitude of the line-line voltages. By substituting Eq. (2.4) into Eq. (2.1), the corresponding space vector can be obtained as

$$
\begin{aligned}
\begin{bmatrix} v_d(t) \\ v_q(t) \end{bmatrix} &= \frac{2}{3} \begin{bmatrix} \cos(0) & \cos(120^\circ) & \cos(240^\circ) \\ \sin(0) & \sin(120^\circ) & \sin(240^\circ) \end{bmatrix} \begin{bmatrix} V_m \cos(\omega t) \\ V_m \cos(\omega t - 120^\circ) \\ V_m \cos(\omega t - 240^\circ) \end{bmatrix} \\
&= \begin{bmatrix} V_m \cos(\omega t) \\ V_m \sin(\omega t) \end{bmatrix}
\end{aligned}
\tag{2.5}
$$

As illustrated in Eq. (2.5), the balanced three-phase voltages with line-line magnitude V_m and frequency ω correspond to a space vector with magnitude V_m, rotating with frequency ω.

2.3.1.2 Space Vectors Attainable from the Multilevel Matrix Converter

As described previously in this chapter, the multilevel matrix converter with the basic configuration can generate line-line voltages with voltage-levels of $+2V_{cap}$, $+V_{cap}$, 0, $-V_{cap}$, or $-2V_{cap}$. This leads to 19 combinations of three-phase line-line voltages in terms of capacitor voltage V_{cap} as listed in Table 2.1. All 19 combinations of line-line voltages are transformed into space vectors by Eqs. (2.1) or (2.2).

Figure 2.11 shows all 19 space vectors in the *dq* coordinate. These 19 space vectors have four different magnitudes: 0, $2V_{cap}/\sqrt{3}$, $2V_{cap}$, and $4V_{cap}/\sqrt{3}$. The null-state space vector corresponds to the converter having all zero line-line voltages. There are six space vectors with magnitude $2V_{cap}/\sqrt{3}$. These six space vectors correspond to the converter having line-line voltages with magnitudes $+V_{cap}$, 0, and $-V_{cap}$. The other six space vectors with magnitude $2V_{cap}$ correspond to the converter having one of line-line voltages with magnitudes of twice the capacitor voltage and the remaining two line-line voltages with magnitudes of one capacitor voltage. The remaining six space vectors with magnitude $4V_{cap}/\sqrt{3}$ correspond to the converter having line-line voltages with magnitudes of $+2V_{cap}$, 0, and $-2V_{cap}$.

The six space vectors with magnitude $2V_{cap}/\sqrt{3}$ (the second group in Table 2.1) and the null-state space vector are employed for two-level switching. For the three-level switching, the SVM employs 18 space vectors, except the null-state space vector. In the basic converter configuration, three-level switching is restricted to when the voltage magnitudes at both sides are significantly different. This occurs because generations of space vectors with magnitudes greater than $2V_{cap}/\sqrt{3}$ on one side of the converter force the other side to have all zero line-line voltages, as described previously. Additional converter space

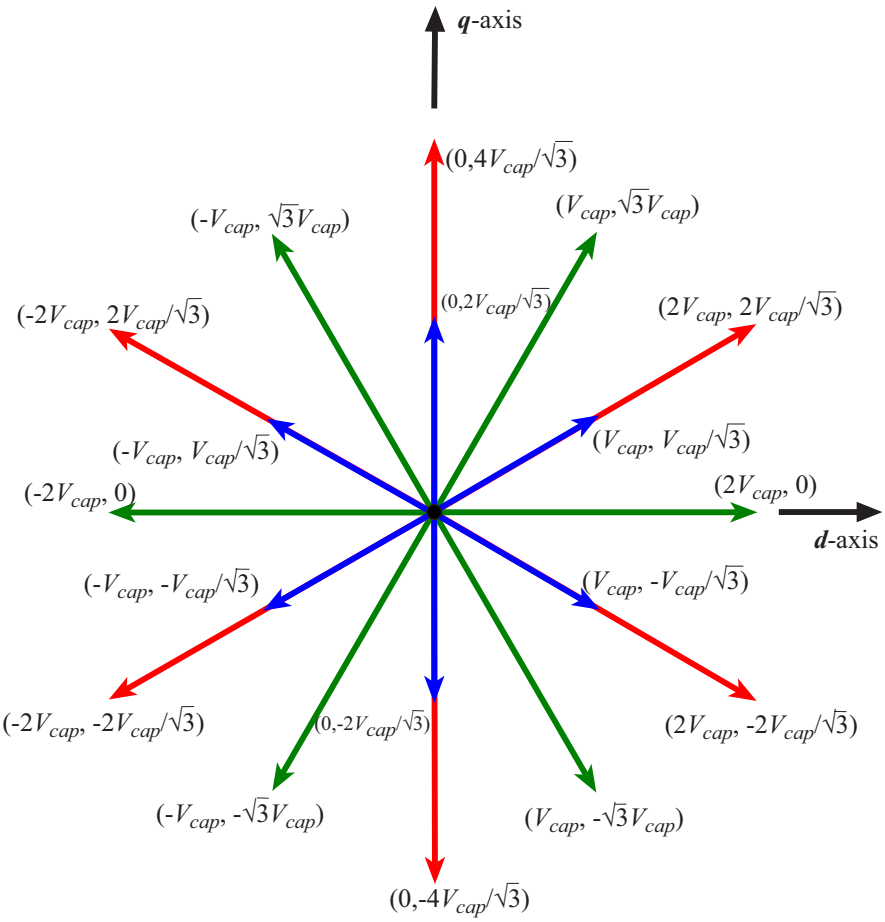


Figure 2.11: The 19 space vectors attainable from the multilevel matrix converter

vectors are possible when multiple modules are placed in each branch of the switch network.

2.3.2 Space-Vector Pulse Width Modulation

The basic concepts of the space-vector PWM technique are different from those of the conventional PWM technique. In the conventional PWM technique, each semiconductor device can be controlled independently; then each terminal voltage is also generated independently. In contrast, the space-vector PWM technique treats the converter as a single unit. All devices in the converter must be changed together to generate the terminal voltage. Modulation is accomplished by switching among switching-device combinations of the converter.

In the SVM, the desired reference space vector can be expressed as a linear combination of three adjacent space vectors. Suppose that the desired reference space vector $\boldsymbol{V_{ref}}(t)$ lies among the space vectors $\boldsymbol{V_a}$, $\boldsymbol{V_b}$, and $\boldsymbol{V_c}$; given this, the reference space vector $\boldsymbol{V_{ref}}(t)$ can be expressed as

$$\begin{aligned} \boldsymbol{V_{ref}}(t) &= d_a \boldsymbol{V_a} + d_b \boldsymbol{V_b} + d_c \boldsymbol{V_c} \\ \text{or} \qquad \boldsymbol{V_{ref}}(t) &= \frac{T_a}{T_s}\boldsymbol{V_a} + \frac{T_b}{T_s}\boldsymbol{V_b} + \frac{T_c}{T_s}\boldsymbol{V_c} \end{aligned} \tag{2.6}$$

where d_a, d_b, and d_c are the duty cycles of the space vectors V_a, V_b, and V_c, respectively. T_s is the switching period of the converter, and

$$d_a + d_b + d_c = 1$$
$$\text{or} \qquad T_a + T_b + Tc = T_s \tag{2.7}$$

Equation (2.6) suggests a way to use PWM to generate a three-phase voltage of which the average value follows a given three-phase reference by switching among the space vectors V_a, V_b, and V_c with duty cycles d_a, d_b, and d_c, respectively. In other words, the converter is changed to a configuration that generates line-line voltages corresponding to the space vector V_a for a duration of time T_a, then it is changed to another configuration having line-line voltages corresponding to the space vector V_b for a duration of time T_b, and so forth. The average values of the three-phase voltages will then follow V_{ref}.

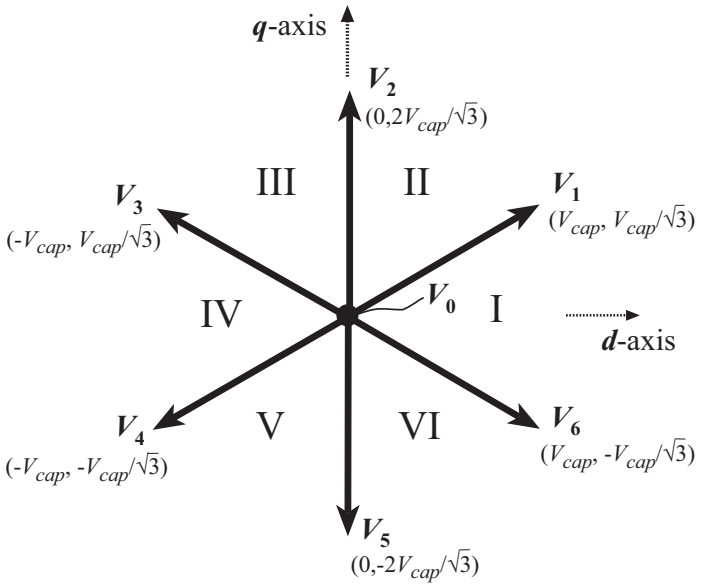
2.4 Summary of Key Points

The multilevel matrix converter with the basic configuration consists of nine capacitor-clamped H-bridge switch cells connected from each input phase to each output phase. The terminal voltages of the converter are synthesized from the PWM of the switch-cell capacitor voltages. As a result, inductors are used as filter elements at both sides of the converter. With the symmetrical structure, the converter is able to both step-up and step-down the voltage magnitudes. The operations and limitations of the multilevel matrix converter have been explained in this chapter. From the understanding of the converter constraints, an approach to generate valid switching-device combinations from given terminal voltages has been developed.

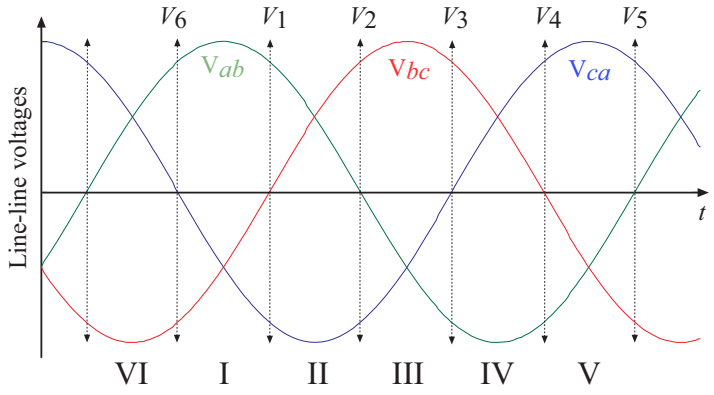
The SVM technique is employed as a technique to synthesize the terminal voltages of the converter. The modulation is performed in the *dq* coordinate; hence, the three-phase variables are transformed into two-phase *dq* variables. The SVMs for both sides of the converter are independent from each other. The multilevel matrix converter with the basic configuration can generate 19 combinations of three-phase line-line voltages at each side, which correspond to 19 space vectors in the *dq* coordinate: one null-state space vector, six space vectors with magnitude $2V_{cap}/\sqrt{3}$, six space vectors with magnitude $2V_{cap}$, and six space vectors with magnitude $4V_{cap}/\sqrt{3}$. The null-state space vector and the six space vectors with magnitude $2V_{cap}/\sqrt{3}$ are used for the two-level switching, whereas the 18 non-zero space vectors are used for the three-level switching.

3 Control Schemes for Two-Level Operation

To synthesize terminal voltages with two-level switching, the SVM employs the null-state space vector and six space vectors with magnitude $2V_{cap}/\sqrt{3}$. This chapter provides more details of the SVM



(a)



(b)

Figure 3.1: Six 60° sectors generated from the six space vectors with magnitude $2V_{cap}/\sqrt{3}$ and one null-state space vector: (a) in *dq* coordinate, (b) in time domain

technique for two-level switching. The proposed control schemes, the eight-capacitor control scheme and the single-capacitor control scheme, for the multilevel matrix converter operating in the two-level switching mode are also explained in this chapter. With the eight-capacitor control scheme, switch-cell

capacitors are connected in parallel to generate terminal voltages. Sets of parallel-connected capacitors disclose all possible capacitors that can be used for given terminal voltages. The single-capacitor control scheme was proposed to reduce the complexity of the converter by involving only one switch-cell capacitor at a time. The single-capacitor control scheme allows the multilevel matrix converter to be modeled as a two-level DC-link converter. Besides, the single-capacitor control scheme can theoretically stabilize capacitor voltages in the converter. Experimental results from the prototype operated with both control schemes are also included.

3.1 SVM for Two-Level Switching

When operating with two-level switching, the multilevel matrix converter can generate terminal line-line voltages with voltage levels of $+V_{cap}$, 0, and $-V_{cap}$. The SVM technique for this operational mode involves six space vectors with magnitude $2V_{cap}/\sqrt{3}$ and one null-state space vector generated from the multilevel matrix converter (Section 2.3.1.2). These seven space vectors form a hexagon diagram, which can be divided into six 60° sectors (Fig. 3.1[a]). The corresponding positions of the space vectors and sectors in time domain are illustrated in Fig. 3.1(b). The period of three-phase sinusoidal waveforms is also divided into six 60° sectors where none of the waveforms change their signs. Note that there are separate *dq* diagrams of each side of the converter.

The desired reference space vector for each side of the converter, at any given time, lies within one of the six 60° sectors. The SVM employs two adjacent space vectors and the null-state space vector to synthesize the desired reference space vector. Assume that the desired reference space vector $\boldsymbol{v}_{ref}(t)$ lies within one of six 60° sectors, between the space vectors $\boldsymbol{V}_k$ and $\boldsymbol{V}_l$ (Fig. 3.2). The desired reference space vector $\boldsymbol{v}_{ref}(t)$ can therefore be expressed by a linear combination of the two adjacent space vectors ($\boldsymbol{V}_k$ and $\boldsymbol{V}_l$), and the null-state space vector $\boldsymbol{V}_0$ as

$$\boldsymbol{v}_{ref} = d_k \boldsymbol{V}_k + d_l \boldsymbol{V}_l + d_0 \boldsymbol{V}_0 \tag{3.1}$$

where d_0, dk, and dl are the duty cycles of the space vectors V0, Vk, and Vl, respectively, and

$$d_k + d_l + d_0 = 1 \tag{3.2}$$

The solution of the duty cycles from the vector diagram in Fig. 3.2 using Eqs. (3.1) and (3.2) and simplifications yield the following:

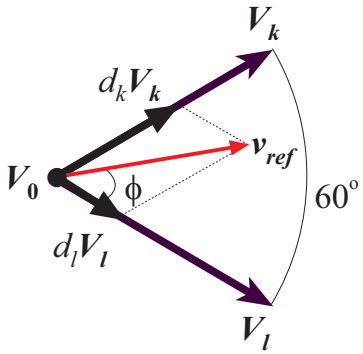


Figure 3.2: Diagram of SVM

$$
\begin{aligned}
d_k &= \frac{2}{\sqrt{3}} \frac{\|\boldsymbol{v_{ref}}\|}{\|\boldsymbol{V_k}\|} \sin\phi \\
&= \frac{\|\boldsymbol{v_{ref}}\|}{V_{cap}} \sin\phi \\
&= M \sin\phi \qquad \text{where } M = \frac{\|\boldsymbol{v_{ref}}\|}{V_{cap}} \\
d_l &= \frac{2}{\sqrt{3}} \frac{\|\boldsymbol{v_{ref}}\|}{\|\boldsymbol{V_l}\|} \sin(60^\circ - \phi) \\
&= \frac{\|\boldsymbol{v_{ref}}\|}{V_{cap}} \sin(60^\circ - \phi) \\
&= M \sin(60^\circ - \phi) \\
d_0 &= 1 - d_k - d_l \\
&= 1 - M \sin(60^\circ + \phi)
\end{aligned}
\tag{3.3}
$$

The SVMs for both sides of the multilevel matrix converter can be performed independently. However, the switching periods for the input and output sides must be synchronized. Assume that the desired input-side reference space vector has two adjacent space vectors, $\boldsymbol{V_k}$ and $\boldsymbol{V_l}$, while the desired output-side reference space vector has two adjacent space vectors, $\boldsymbol{V_m}$ and $\boldsymbol{V_n}$. The duty cycle of each space vector is computed using Eq. (3.3). In one switching period, the input and the output sides of the converter are driven with their respective space vectors and duty cycles (Fig. 3.3). Typically, because the input- and the output-side reference space vectors have different magnitudes and frequencies, the space vectors at both sides have different duty cycles; the switching of the input- and the output-side space vectors occurs at different times. As a result, each switching period can have a maximum of five distinct subintervals, which have different combinations of the input-side space vector and the output-side space vector. Note that the order of the space vectors in each switching period is arbitrary.

In each subinterval of any switching period, the configuration of the multilevel matrix converter must be changed to generate different terminal voltages according to the input and output space vectors. In fact, this can be done using only one configuration of branch connection and changing the states of the switch cells, which can provide only 243 choices of switching-device combinations to be employed throughout each switching period. However, such operation does not guarantee stability of the DC capacitor voltages.

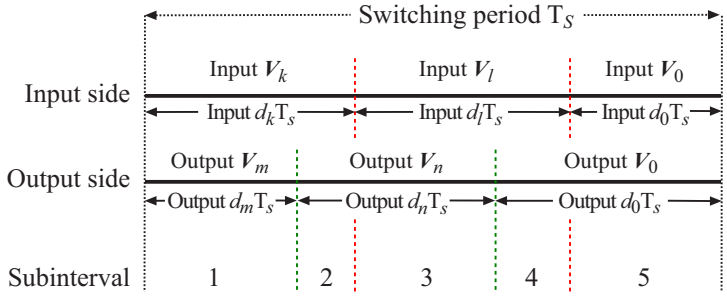
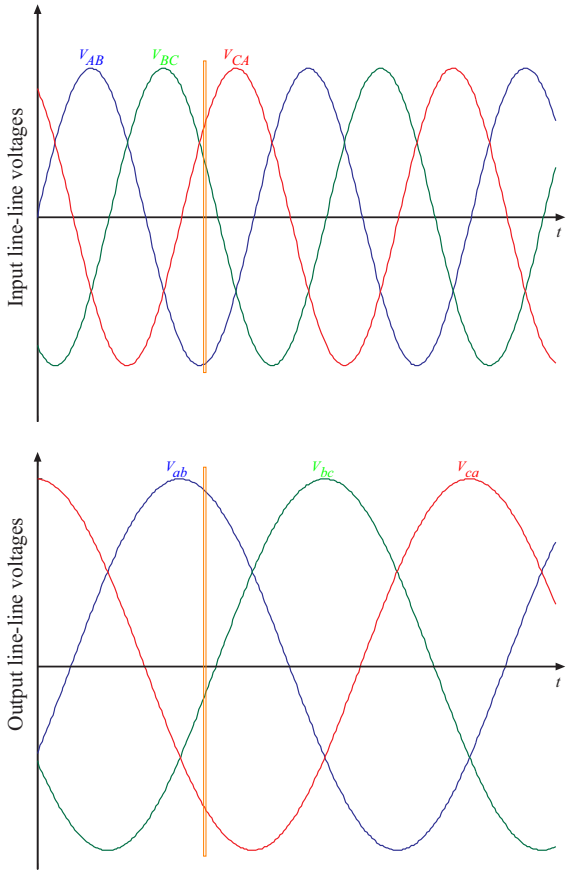
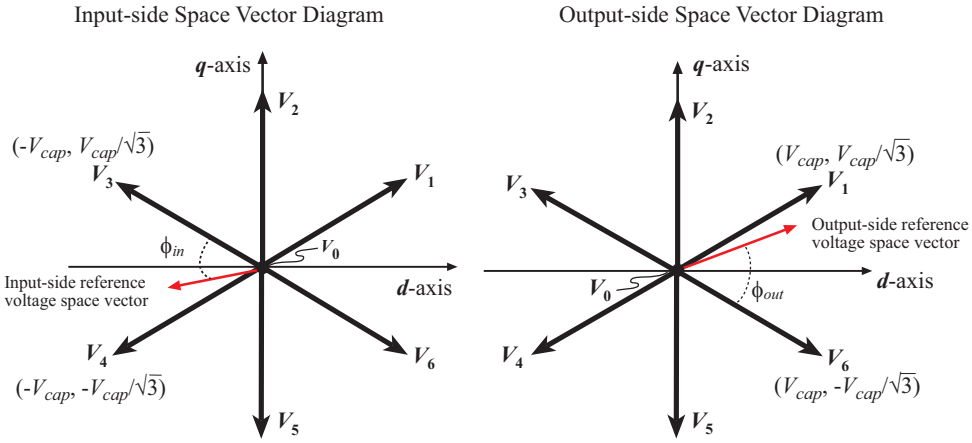


Figure 3.3: SVM of both input and output sides, dividing the switching period into five subintervals

Two control schemes are proposed for the multilevel matrix converter when the converter is operated with two-level switching on the input and output sides: the eight-capacitor control scheme and the single-capacitor control scheme [54]. With the eight-capacitor control scheme, a converter configuration for each subinterval is generated by the approach described in Section 2.2.2. All nine switch cells conduct currents at any given instant. In addition, the capacitors are connected in parallel. In each switching period, a total of eight capacitors are involved in synthesizing terminal voltages. This increases the effective capacitance for transferring the energy through the converter. On the other hand, with the single-capacitor control scheme, a switching-device combination for each subinterval is chosen from redundant switching combinations such that only one capacitor is employed to synthesize terminal voltages throughout a switching period. This approach can minimize circulating currents among the capacitors. Consequently, the stability of capacitor voltages and the efficiency of converter are improved.



(a) Time domain



(b) *dq* coordinate

Figure 3.4: An example of SVM

3.2 Eight-Capacitor Control Scheme

3.2.1 Control Scheme

The eight-capacitor control scheme is a simplified control scheme for the multilevel matrix converter. For a given set of converter line-line voltages (input-side and output-side space vectors) there is only one switching-device combination. The switching-device combination can be generated from known terminal voltages by the approach described in Section 2.2.2. For different input-side and output-side space vectors, different sets of capacitors are involved in the switching-device combinations. Throughout a complete switching period, a total of eight capacitors are involved in transferring the energy.

With the eight-capacitor control scheme, all nine switch cells conduct currents at any given instant and switch-cell capacitors are allowed to be connected in parallel. As a result, the converter configurations violate the constraints of branch connection described in Section 2.1.2.

Consider an example in which the multilevel matrix converter generates the input-side and the output-side voltages (Fig. 3.4[a]). At a switching period marked by the vertical bars, the corresponding input-side reference space vector lies between the space vectors V_{3_in} and V_{4_in}, whereas the corresponding output-side reference space vector lies between the space vectors V_{1_out} and V_{6_out} (Fig. 3.4[b]). The duty cycle for each space vector can be computed using Eq. (3.3). The SVM technique involves the modulation among input-side space vectors V_{3_in}, V_{4_in}, and V_{0_in}, with duty cycles of d_{3_in}, d_{4_in}, and d_{0_in}, respectively. Likewise, the output-side involves the modulation among the space vectors V_{1_out}, V_{6_out} , and V_{0_out} with duty cycles of d_{1_out}, d_{6_out}, and d_{0_out}, respectively. A possible pattern of the input- and the output-side space vectors in one switching period is shown in Fig. 3.5. The switching period is divided into five subintervals where the converter generates different input- and output-side space vectors; in consequence, the terminal line-line voltages differ.

With the space-vector pattern shown in Fig. 3.5, the line-line voltages of the converter can be determined from the input-side space vector and the output-side space vector (Fig. 3.6). These line-line voltages can be employed to determine the converter configuration by the approach described in Section 2.2.2. The switching-device combinations for each subinterval are illustrated in Fig. 3.7. The converter involves a different set of switch-cell capacitors for each subinterval.

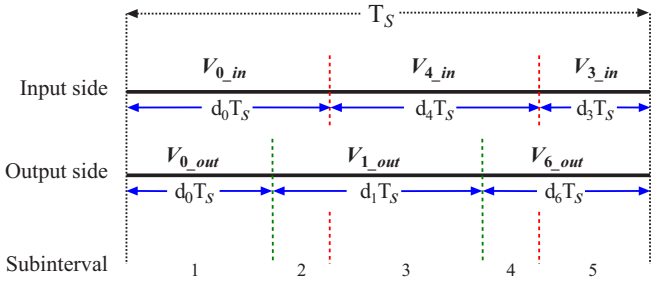


Figure 3.5: Possible switching pattern of the input and the output space vectors in one switching period for the example

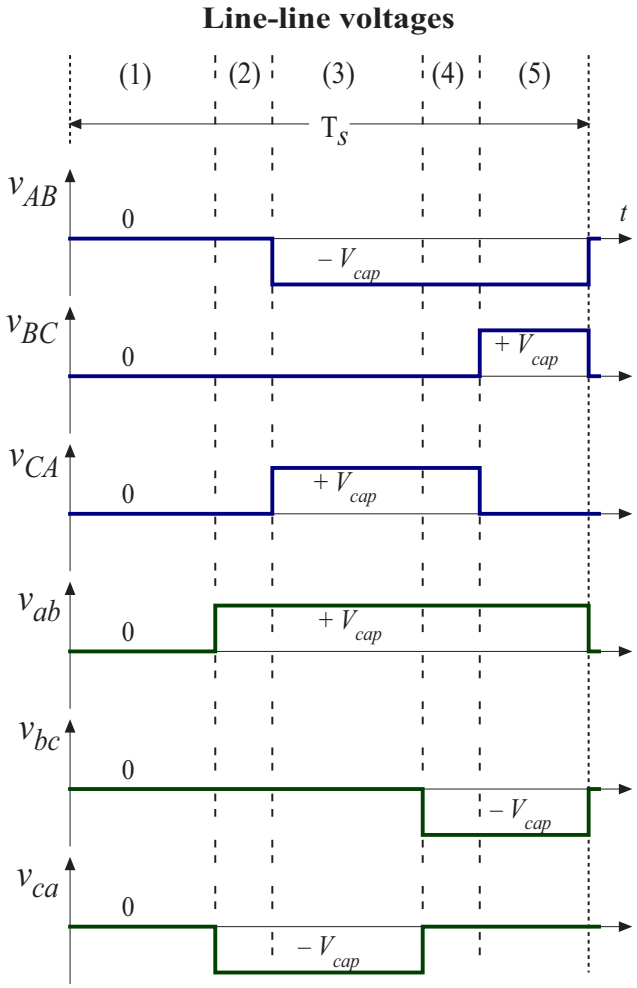
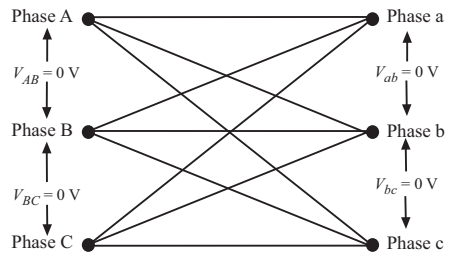
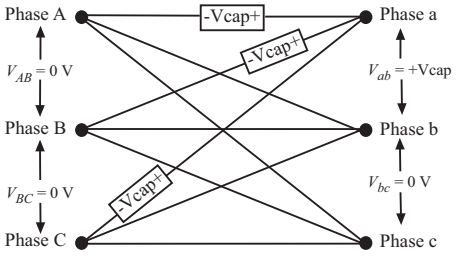


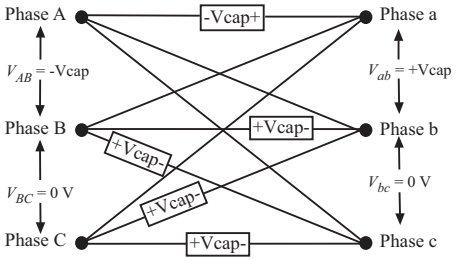
Figure 3.6: PWM line-line voltages in the given switching period for the example



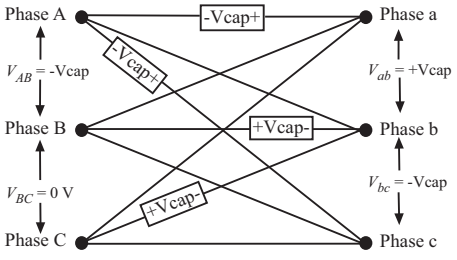
subinterval 1



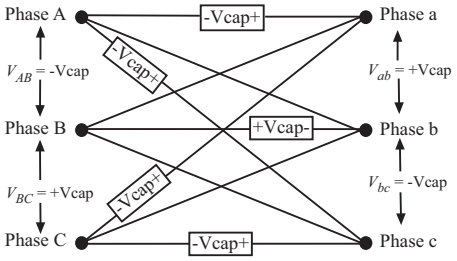
subinterval 2



subinterval 3



subinterval 4



subinterval 5

Figure 3.7: Converter configurations for each subinterval in the given switch period for the example

Close examination of Fig. 3.7 reveals that the capacitor of the switch cell in branch *Ab* is never employed in the given switch period. With this modulation approach, eight of the nine capacitors participate in synthesizing the terminal voltages during each complete switching period. Note that if the order of the input- and output-side space vectors is changed, different combinations of input- and output-side space vectors for each subinterval are obtained, as well as the duration of each subinterval. This also results in different sets of converter configurations and capacitors. In addition, in some cases all nine capacitor can participate in synthesizing terminal voltages during each switching period.

This control scheme has no limitation on the conversion ratio of the input and the output voltage magnitudes. In fact, if the voltage magnitudes of both input and output sides are significantly different, with the same order of the input and output space vectors, all nine switch-cell capacitors can be involved in one switching period.

This control scheme has one advantage – the effective capacitance for transferring the energy is increased and, hence, capacitor voltage ripple is reduced. The disadvantage of this control scheme is that high peak currents occur during the transition of the subintervals. Because the control scheme employs different sets of capacitors for subintervals in each switching period, charge balance of the switch-cell capacitors cannot be achieved. This leads to a problem of the stability in the capacitor voltages as the operating voltage of the converter increases.

3.2.2 Experimental Results from the Eight-Capacitor Control Scheme

The following experimental results illustrate the performances of the multilevel matrix converter with the eight-capacitor control scheme. The 60-Hz input voltages were converted into 30-Hz voltages with the following modulation indices:

$$\begin{aligned} M_{in} &= \frac{\|\boldsymbol{v_{ref-in}}\|}{V_{cap}} = 0.90 \\ M_{out} &= \frac{\|\boldsymbol{v_{ref-out}}\|}{V_{cap}} = 0.75 \end{aligned} \tag{3.4}$$

The multilevel matrix converter operated at a switching frequency of 50 kHz. More details about the laboratory prototype are described in Chapter 6.

The input and the output PWM line-line voltage waveforms and current waveforms are shown in Fig. 3.8. The trajectories of the input and the output voltages in the *dq* coordinate are illustrated in Fig. 3.9, while the trajectories of the input and the output currents are illustrated in Fig. 3.10. Figure 3.11 shows the output PWM line-line voltage waveform along with the filtered output line-line voltage waveform. The variation of the DC capacitor voltage along the output line period is shown in Fig. 3.12. Afterward, Fig. 3.13 shows a comparison of two capacitor voltage waveforms.

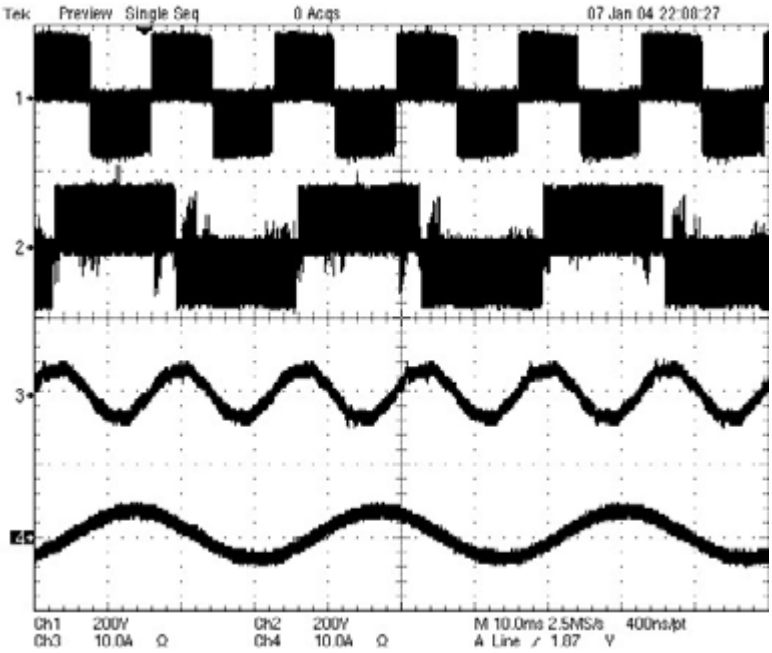


Figure 3.8: Voltage and current waveforms:
Trace 1: input PWM line-line voltage waveform at 200 V/div
Trace 2: output PWM line-line voltage waveform at 200 V/div
Trace 3: input phase current at 10 A/div
Trace 4: output phase current at 10 A/div
Horizontal scale: 10 ms/div

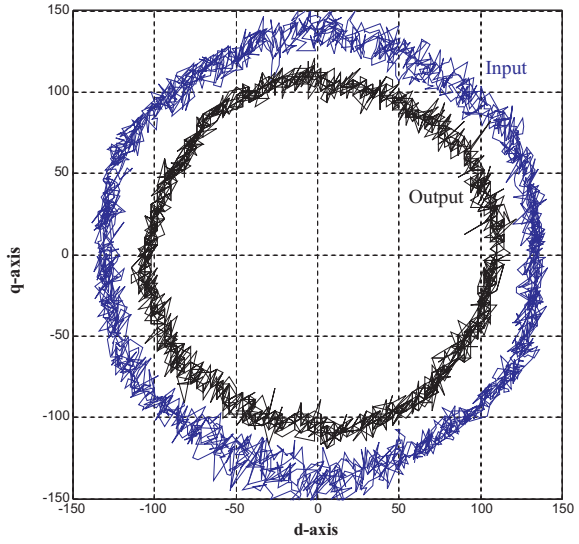


Figure 3.9: Trajectories of input- and output-voltages in dq coordinate

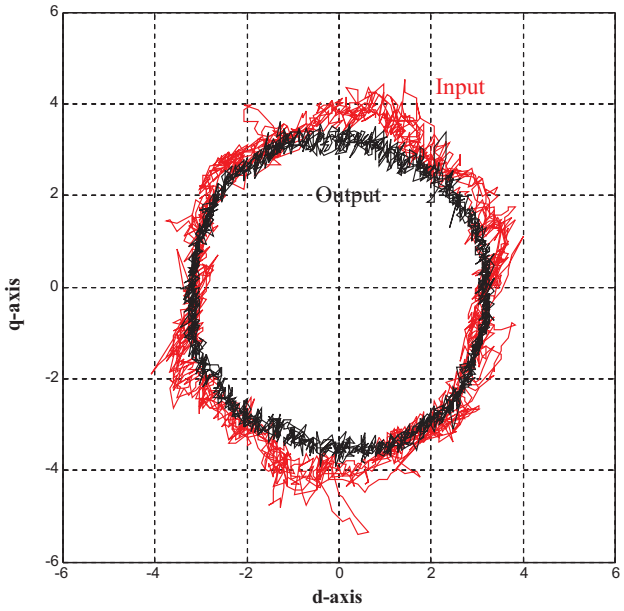


Figure 3.10: Trajectories of input and output currents in dq coordinate

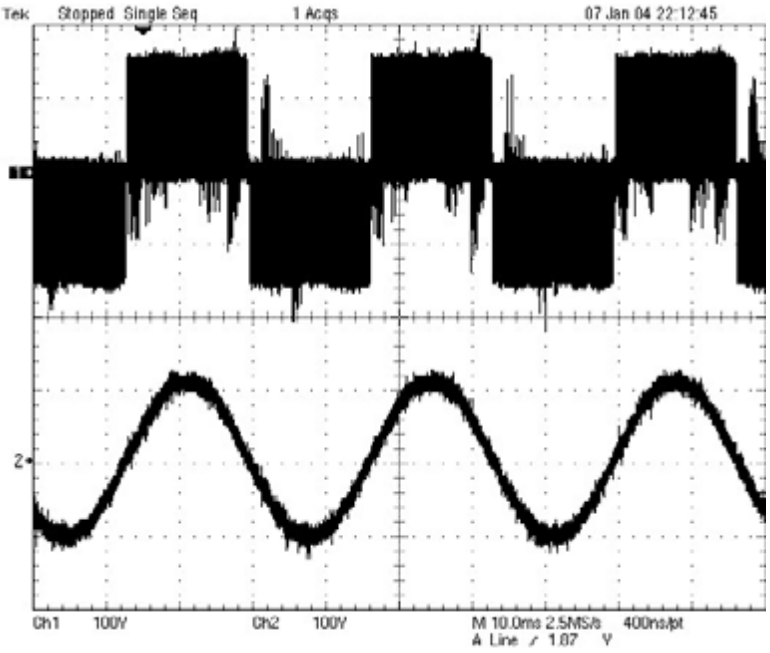


Figure 3.11: The 30-Hz line-line voltage waveforms
Trace 1: PWM voltage waveform at the output of the switch network
Trace 2: filtered load voltage waveform, after filtered by an LC low-pass network

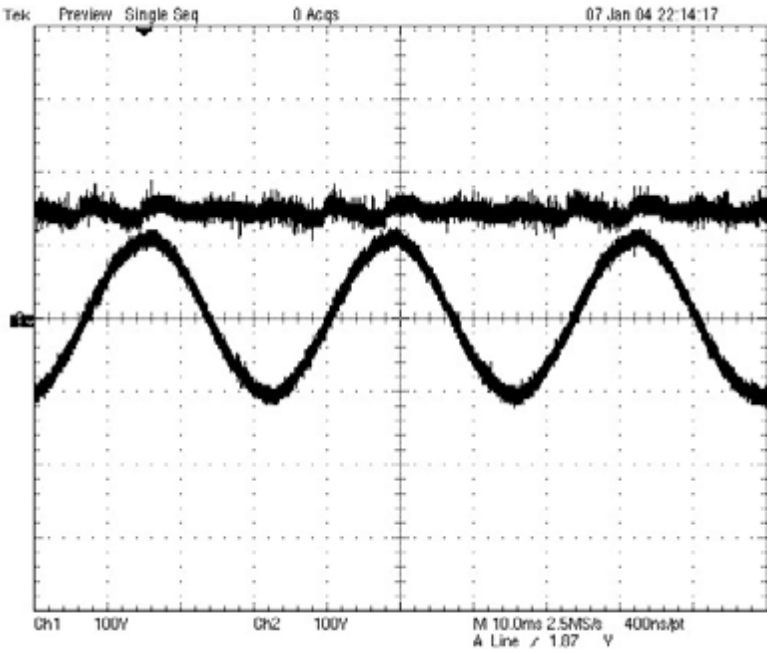


Figure 3.12: Variation of DC capacitor voltage, without active control
Trace 1: DC capacitor voltage waveform
Trace 2: filtered-load voltage waveform
Both traces have scale of 100 V/div

Even though the multilevel matrix converter operating with this control scheme exhibited practicability in the prototype testing, the capacitor voltage imbalance q and the current spikes in the converter tended to be more severe at the higher operating power. These problems restrained the converter from operating at higher voltage levels.

3.3 Single-Capacitor Control Scheme

3.3.1 Control Scheme

When the multilevel matrix converter synthesizes the input- and the output-side voltages with two-level switching, the terminal line-line voltages have voltage-levels of $+V_{cap}$, 0, and $-V_{cap}$. Hence, only one switch-cell capacitor is sufficient to be employed for synthesizing the terminal voltages in each subinterval. It is also possible to employ the same capacitor for all five subintervals in each switching period. When only one capacitor is used to transfer energy between both sides of the converter, charge balance on this single capacitor can be achieved in one complete switching period. By avoiding the parallel connection of the capacitors, circulations of currents among multiple capacitors are minimized. Therefore, the converter should exhibit high efficiency. This concept allows the multilevel matrix converter to be modeled as a two-level DC-link converter, which significantly reduces the complexity of the converter operations.

Control of the multilevel matrix converter with this concept can be accomplished through a variety of approaches; however, the proposed approach is relatively simple and easy to be implemented for a real-time control. To guarantee that the switch-cell capacitor to be employed throughout a switching period exists, the pattern of space vectors as demonstrated in Fig. 3.14 is required. In one switching period, each side of the converter synthesizes terminal voltages using three space vectors: one null-state space vector and two space vectors with magnitude $2V_{cap}/\sqrt{3}$. For both input and output sides, the pattern starts with the null-state space vector, then follows with the space vector having the greater duty cycle, and then ends with the space vector having the lesser duty cycle.

Consider the example used in the previous section. For the input side, the modulation angle is greater than 30°; hence, the duty cycle of the space vector $\boldsymbol{V}_{4\_in}$ is greater than the duty cycle of the space vector $\boldsymbol{V}_{3\_in}$. For the output side, the modulation angle is also greater than 30°; hence, the duty cycle of the space vector $\boldsymbol{V}_{1\_out}$ is greater than the duty cycle of the space vector $\boldsymbol{V}_{6\_out}$. The pattern of input-side and output-side space vectors in one switching period is shown in Fig. 3.15, as well as sets of capacitors that can be employed for each subinterval. In this case, the order of the input- and output-side space vectors is identical to the one shown in Fig. 3.5. The set of switch-cell capacitors for each subinterval is the same as those employed in the eight-capacitor control scheme. Notice that capacitor C_{Aa}, from the switch cell that is connected between the input phase A and the output phase a, can be employed throughout the switching period. Then the switching-device combination for each subinterval can be chosen from redundant switch combinations that involve the capacitor from switch cell S_{Aa} and any four more switch cells that operate in State 3 (short-circuited state) in the switch network. Figure 3.16(a) shows an example of possible switching-device combinations for each subinterval.

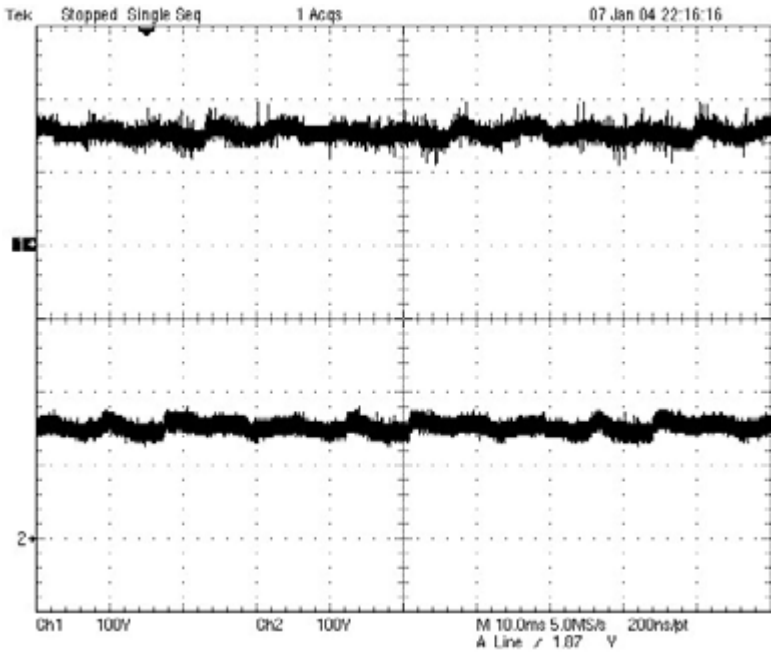


Figure 3.13: The DC capacitor voltage waveforms of two different switch cells; Trace 1 and Trace 2 are both set to scale of 100 V/div at different ground reference level

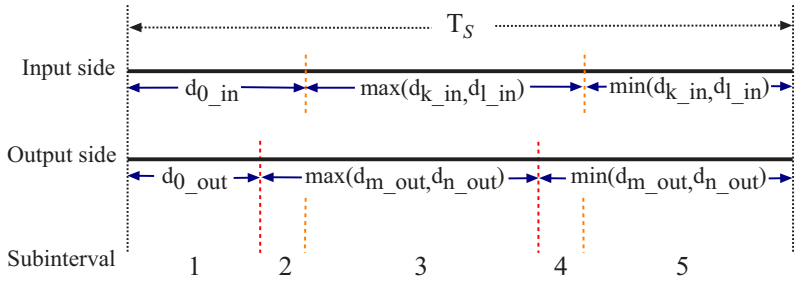


Figure 3.14: The pattern of input-side and output-side space vectors for the single-capacitor control scheme

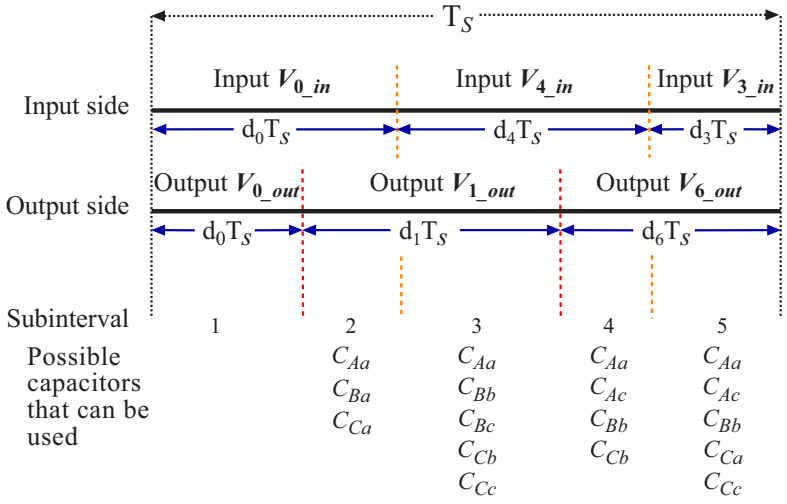


Figure 3.15: Pattern of input-side and output-side space vectors for the example with sets of capacitors that can be used in each subinterval

Figure 3.16(b) illustrates the connections in an equivalent DC-link converter that generates identical space vectors. The DC-link capacitor is equivalent to the capacitor C_{Aa}. The waveforms of the input and output line-line voltages in the switch period are identical to those illustrated in Fig. 3.6. Note that the order of subintervals can be further rearranged arbitrarily and it may be advantageous to sequence the subintervals differently to improve some specific qualities such as the total harmonic distortion or the switching loss.

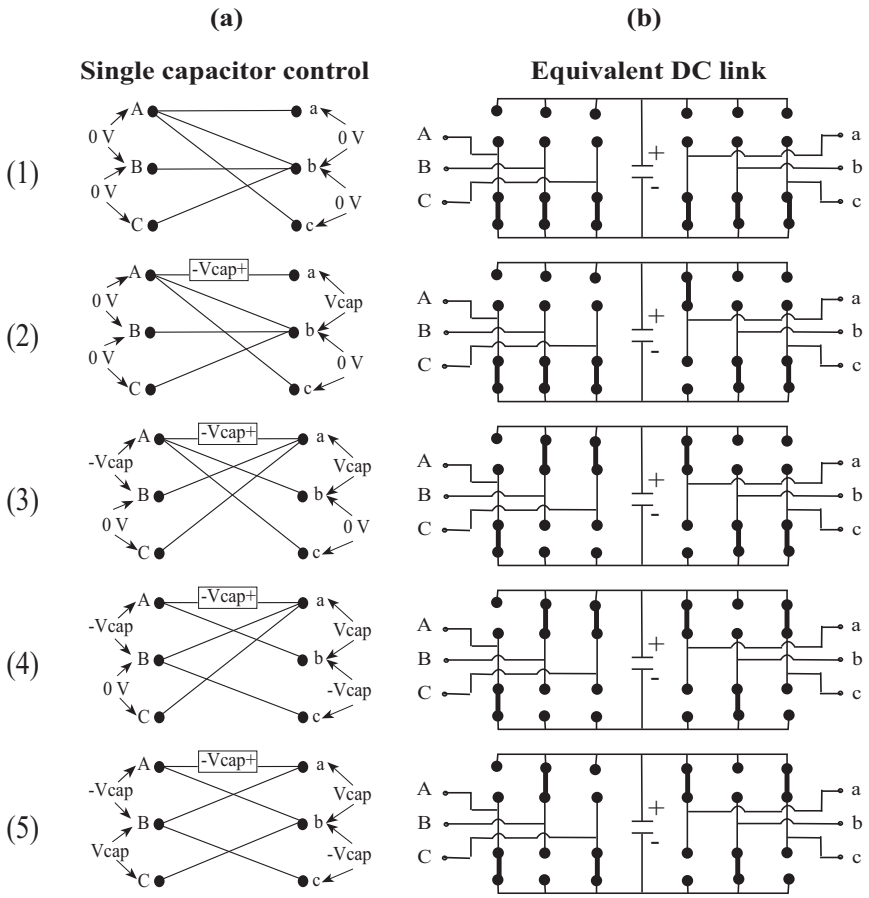


Figure 3.16: Converter configuration with the single-capacitor control technique: (a) switching-device combinations of each subinterval, (b) equivalent DC-link circuits

Throughout the input- and the output-line cycle, the converter employs all nine switch-cell capacitors to synthesize terminal voltages. The single switch-cell capacitor to be employed during a given switching period can be determined depending on two conditions: the positions of the input- and the output-side reference space vectors and the relative values of the duty cycles for the input- and the output-side null space vectors. Figures 3.17 and 3.18 summarize the results of the single-capacitor selection from the single-capacitor control scheme in the *dq* diagrams. For the case of $d_{0\_out} < d_{0\_in}$((Fig. 3.17), a different switch-cell capacitor is selected for every 60° of the output-side line cycle and for every 120° of the input-side line cycle. The situation is reversed for the case of $d_{0\_out} > d_{0\_i}$ (Fig. 3.18), where the input and the output sides are interchanged.

For example, in the case of $d_{0\_out} < d_{0\_in}$, if the output-side reference space vector has angle of 10° (within the area of ±30° of the output-side space vector $\boldsymbol{V}_1$) and the input-side reference space vector has angle of 280°, the capacitor C_{Ba} from the switch cell connected between the input phase *B* and the output phase *a* can be employed. However, for the same positions of both reference space vectors but in the case of $d_{0\_out} > d_{0\_in}$, the capacitor C_{Cb} from the switch cell connected between the input phase *C* and the output phase *b* must be employed.

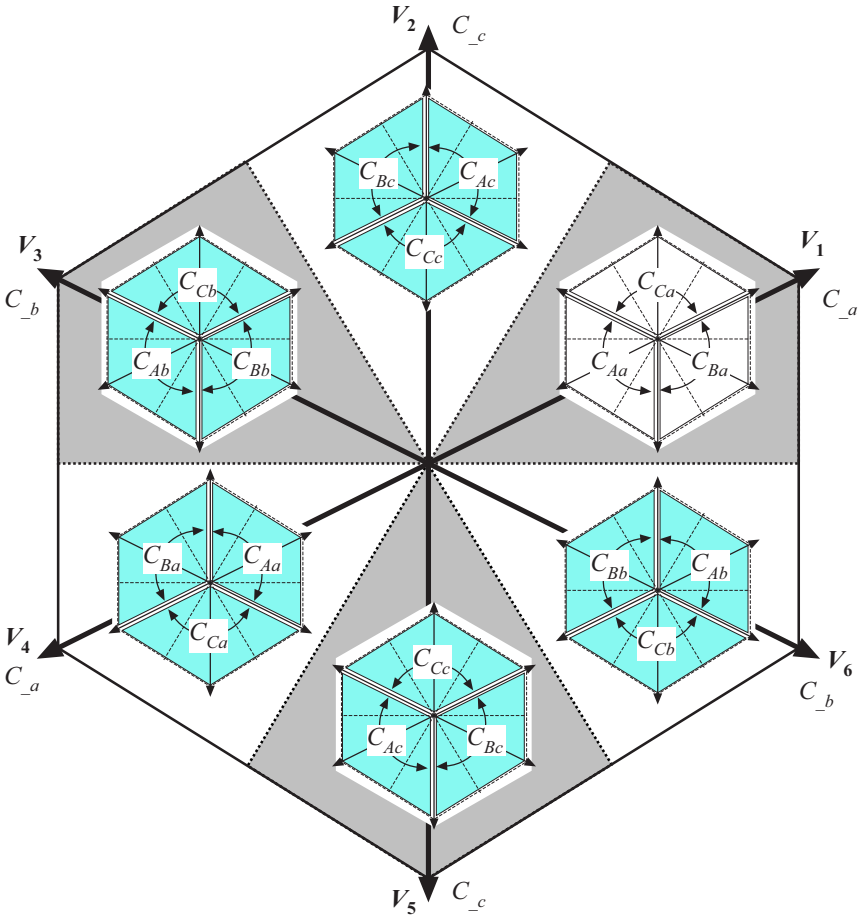


Figure 3.17: Summary of switch-cell capacitor choice with the single-capacitor control scheme for the case of $d_{0\_out} < d_{0\_in}$

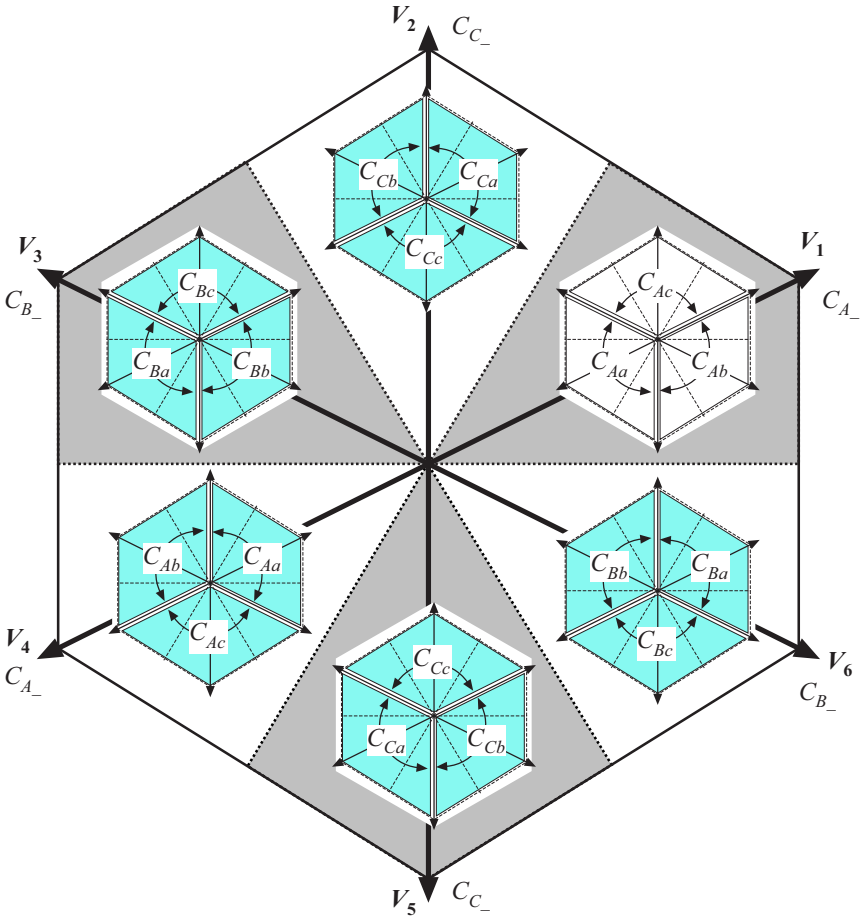


Figure 3.18: Summary of switch-cell capacitor choice with the single-capacitor control scheme for the case of $d_{0\_out} > d_{0\_in}$

It should be noted that when the reference vector coincides with one of the space vectors $\boldsymbol{V}_1$, $\boldsymbol{V}_2$, …, $\boldsymbol{V}_6$, then the corresponding line-neutral voltages v_{an}, $-v_{cn}$, v_{bn}, $-v_{an}$, v_{cn}, v_{bn} attain their peak values. Thus, the single-capacitor selection in the single-capacitor control scheme can be summarized in another way: the converter employs the capacitor from the switch cell connected between the input phase and the output phase that has the largest opposite polarity line-neutral voltage. The side of the converter in which the null-state space vector has less duty cycle must be considered first. For example, suppose that d_{0_out} is less than d_{0_in}. If $v_{ref\text{-}out}(t)$ lies within ±30° of the space vector $\boldsymbol{V}_3$, then the output-side line-neutral voltage $v_{bn}(t)$ lies within ±30° of its peak positive value for the output AC line cycle. Therefore, one of the three capacitors from the switch cells connected to the output phase b (either C_{Ab}, C_{Bb}, or C_{Cb}) can be chosen. Next, the input side is examined. To narrow the choice to a single capacitor, the capacitor that is connected to the phase having the largest negative value, of opposite polarity to the output side, is selected. Three of the six space vectors lead to negative-polarity input space vectors: $\boldsymbol{V}_2$, $\boldsymbol{V}_4$, and $\boldsymbol{V}_6$ corresponding to negative v_{CN}, v_{AN}, and v_{BN}, respectively. The space vector that lies closest to (within ±60°) the input reference space vector is selected. For instance, if the input-side reference space vector lies between the space vectors $\boldsymbol{V}_4$ and $\boldsymbol{V}_5$, then it is closest to the negative space vector $\boldsymbol{V}_4$, so input phase A exhibits the most negative line-neutral voltage. Therefore, capacitor C_{Ab} is employed.

For the single-capacitor control scheme to be valid, the conversion voltage gain ratio is limited to the following:

$$\sqrt{3} \geq \frac{\|V_{ref-in}\|}{\|V_{ref-out}\|} \geq \frac{1}{\sqrt{3}} \tag{3.5}$$

his condition comes from a constraint in the combinations of the null-state space vector and the space vectors with magnitude $2V_{cap}/\sqrt{3}$. The combinations of the null-state space vector and two adjacent space vectors on the other side always result in different sets of allowed switch-cell capacitors (Appendix B). For example, the combination of the input-side null-state space vector $\boldsymbol{V}_{\boldsymbol{0\text{-}in}}$ and the output-side space vector $\boldsymbol{V}_{\boldsymbol{1\text{-}out}}$ allows the converter to employ switch-cell capacitors C_{Aa}, C_{Ba}, or C_{Ca} as a single capacitor in the switching-device combination. However, the combination of the input-side null-state space vector $\boldsymbol{V}_{\boldsymbol{0\text{-}in}}$ and the output-side space vector $\boldsymbol{V}_{\boldsymbol{6\text{-}out}}$ allows the converter to employ switch-cell capacitor C_{Ab}, C_{Bb}, or C_{Cb}. Therefore, to guarantee that a capacitor exists that can be employed throughout a complete switching period, each switching period must contain only one subinterval having a combination of the null-state space vector and a space vector with magnitude $2V_{cap}/\sqrt{3}$. The pattern shown in Fig. 3.14 means that the duty cycle of the input null-state space vector has to be greater than the sum of the duty cycle of the output null-state space vector and the maximum duty cycle between the two output space vectors. This condition implies the limited voltage ratio as shown in Eq. (3.5). Because the converter is symmetrical, it can work with the input and output interchange. This condition is also reflected in Eq. (3.5).

3.3.2 Experimental Results from the Single-Capacitor Control Scheme

3.3.2.1 Case 1

The converter was programmed to convert 60-Hz input voltages into 30-Hz output voltages, with the following modulation indices:

$$M_{in} = \frac{\|\boldsymbol{v_{ref-in}}\|}{V_{cap}} = 0.94$$
$$M_{out} = \frac{\|\boldsymbol{v_{ref-out}}\|}{V_{cap}} = 0.84 \tag{3.6}$$

The prototype was operated with a switching frequency of 50 kHz. Details of the hardware prototype are described in Chapter 6.

Voltage and current waveforms are illustrated in Fig. 3.19. At this operating point, the capacitor voltages were approximately 150 V. The top trace, Trace 1, is the line-line voltage waveform that appeared at the input (60-Hz) side of the switch matrix. The PWM voltage waveform switched among 0, $+V_{cap}$, and $-V_{cap}$. Trace 2 is the PWM line-line voltage waveform that appeared at the output (30-Hz) side of the switch matrix. Traces 3 and 4 are the resulting current waveforms that appeared in the input-side and the output-side inductors, respectively.

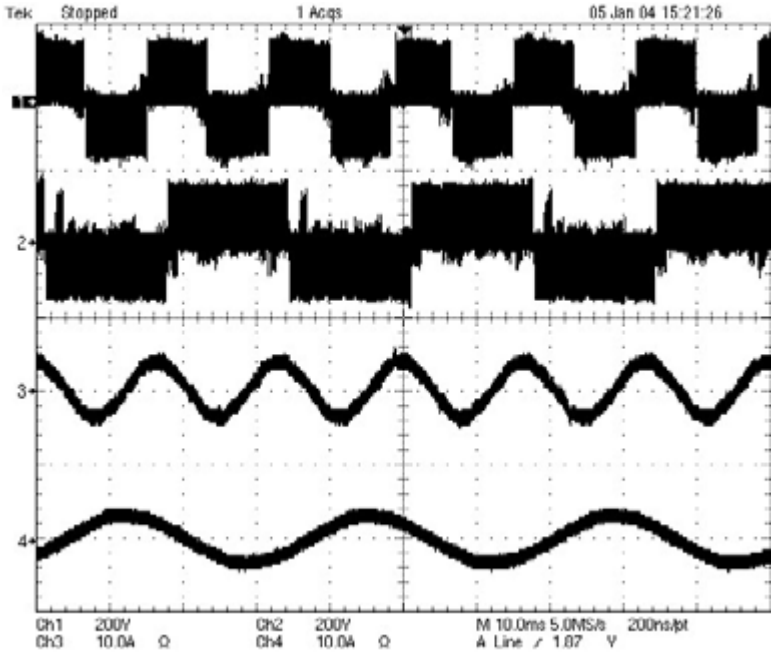


Figure 3.19: Voltage and current waveforms. Case 1
Trace 1: input PWM line-line voltage waveform at 200 V/div
Trace 2: output PWM line-line voltage waveform at 200 V/div
Trace 3: input phase current at 10 A/div
Trace 4: output phase current at 10 A/div
Horizontal scale: 10 ms/div

The trajectories of the input and output voltages in the *dq* coordinate are illustrated in Fig. 3.20, whereas the trajectories of the input and output currents in the *dq* coordinate are illustrated in Fig. 3.21.

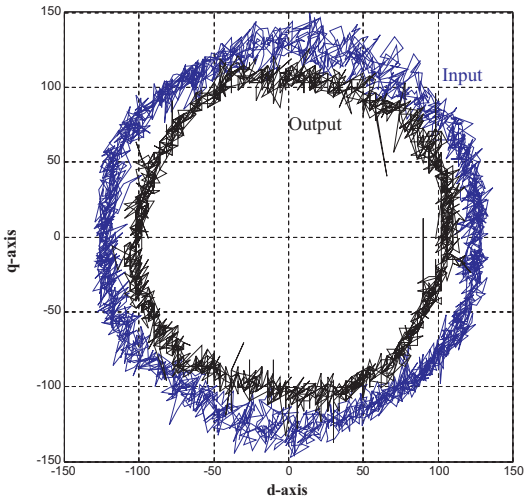


Figure 3.20: Trajectories of input- and output-voltages in *dq* coordinate

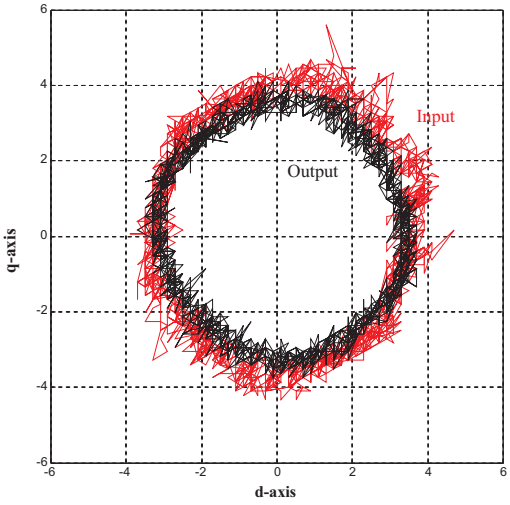


Figure 3.21: Trajectories of input- and output-currents in *dq* coordinate

Figure 3.22 illustrates the output voltage waveforms produced at this operating point. Trace 1 is the PWM line-line voltage waveform that appeared at the output of the switch network which is similar to Trace 2 in Fig. 3.19. Trace 2 is the waveform of the filtered output line-line voltage.

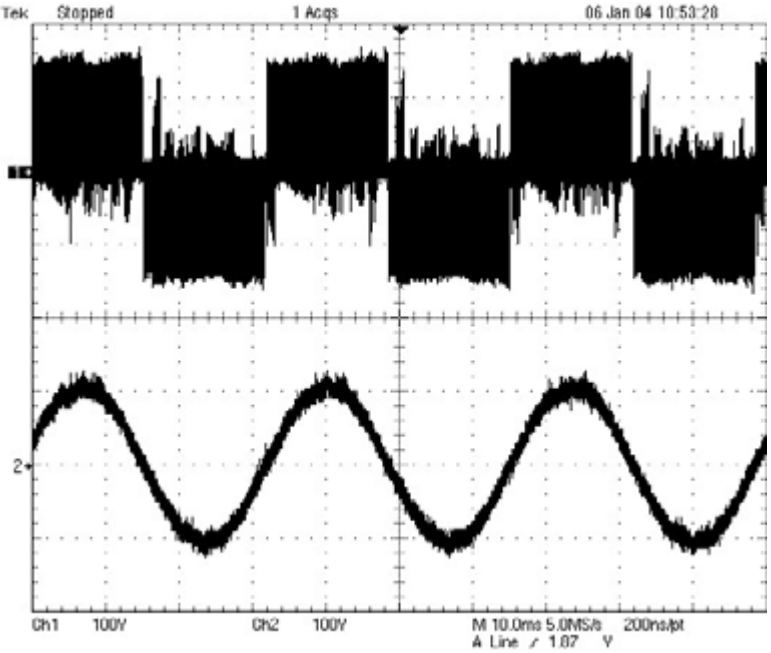


Figure 3.22: The 30-Hz output line-line voltage waveforms for Case 1
Trace 1: PWM voltage waveform at the output of the switch network
Trace 2: load voltage waveform after filtered by LC output low-pass network

Figure 3.23 illustrates the variation of capacitor voltage over output line cycles. Trace 1 is the capacitor voltage waveform at approximately 150 V. Trace 2 is the filtered 30-Hz AC output voltage waveform; it is similar to waveform of Trace 2 in Fig. 3.22.

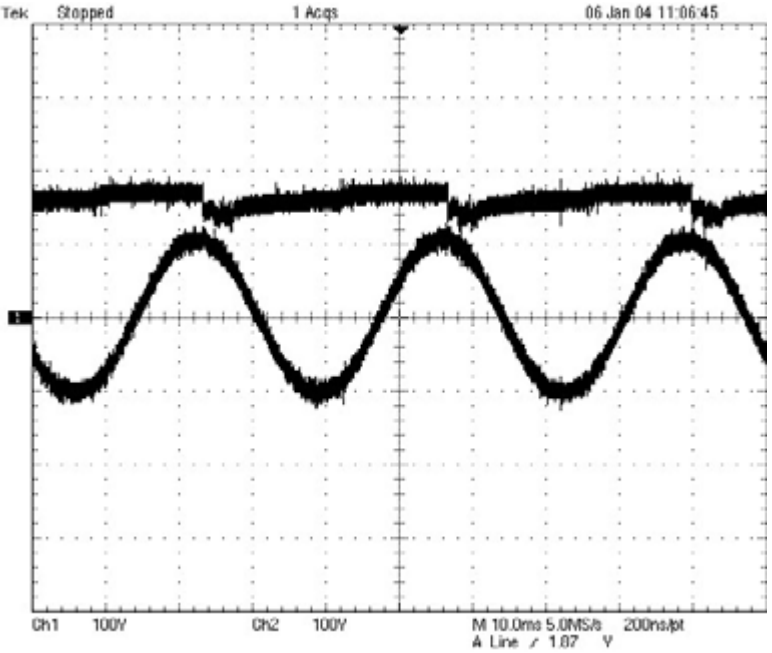


Figure 3.23: Variation of DC capacitor voltages, without any active control
Trace 1: DC capacitor voltage waveform
Trace 2: filtered load voltage
Both traces have scale of 100 V/div

Figure 3.24 illustrates the variation of the capacitor voltages in two different switch cells. The top half of the screen shows the two DC capacitor voltage waveforms, whereas the lower half of the screen shows the same waveforms with an expanded time scale. It shows the period that the charge distributed between the two switch-cell capacitors. During this period, a high-magnitude current spike is induced in the converter. To achieve higher operating voltage, a capacitor voltage regulation is required.

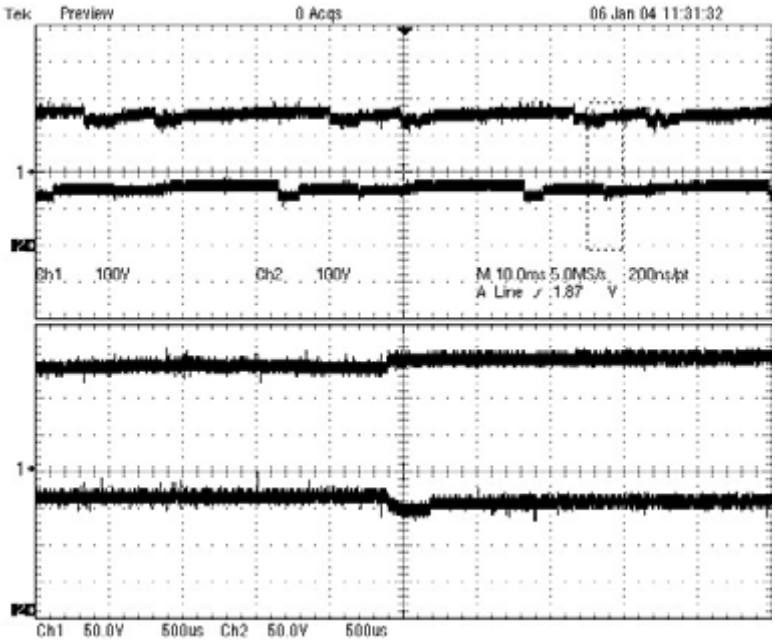


Figure 3.24: The DC capacitor voltage waveforms of two different switch cells. The upper half of the screen illustrates the measured waveforms at 10 ms/div. Trace 1 and Trace 2 are both set to scale of 100 V/div at different ground reference levels. The lower half of the screen shows the same waveforms magnified from the outlined area.

3.3.2.2 Case 2

Case 2 illustrates that the multilevel matrix converter with the single-capacitor control scheme can operate at an arbitrary line frequency. The converter was programmed to convert 60-Hz input voltages into 100-Hz output voltages with the modulation indices of $M_{in} = 0.94$ and $M_{out} = 0.65$.

The input and output PWM line-line voltage waveforms and line current waveforms are illustrated in Fig. 3.25. The trajectories of the input and output voltages in the *dq* coordinate are shown in Fig. 3.26. The trajectories of the input and output currents in the *dq* coordinate are shown in Fig. 3.27. The output PWM line-line voltage waveform is illustrated in Fig. 3.28, along with the filtered output line-line voltage waveform. The variation of capacitor voltage along the output line period is shown in Fig. 3.29.

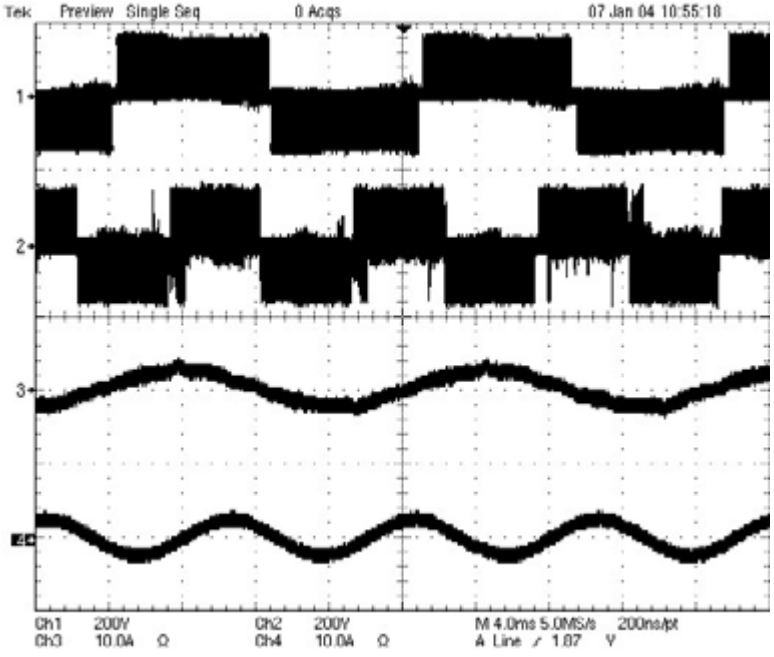


Figure 3.25: Voltage and current waveforms, Case 2
Trace 1: input line-line PWM voltage waveform at 200 V/div
Trace 2: output line-line PWM voltage waveform at 200 V/div
Trace 3: input phase current at 10 A/div
Trace 4: output phase current at 10 A/div. Horizontal scale: 4 ms/div

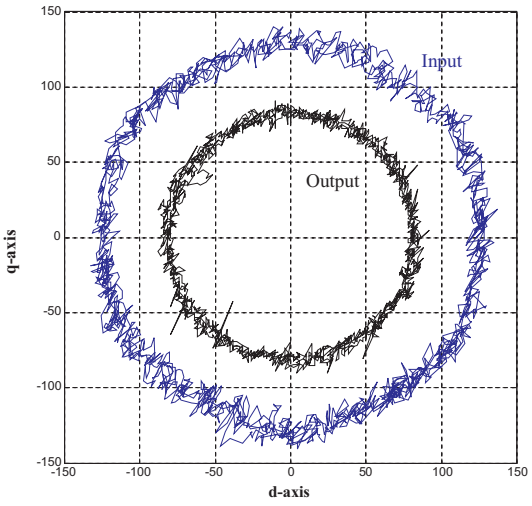


Figure 3.26: Trajectories of input- and output-voltages in *dq* coordinate

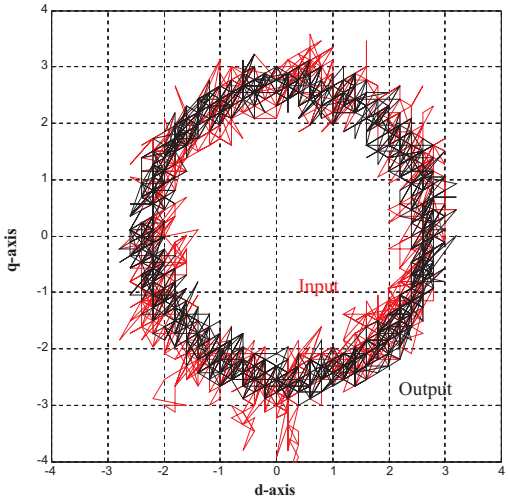


Figure 3.27: Trajectories of input- and output-currents in *dq* coordinate

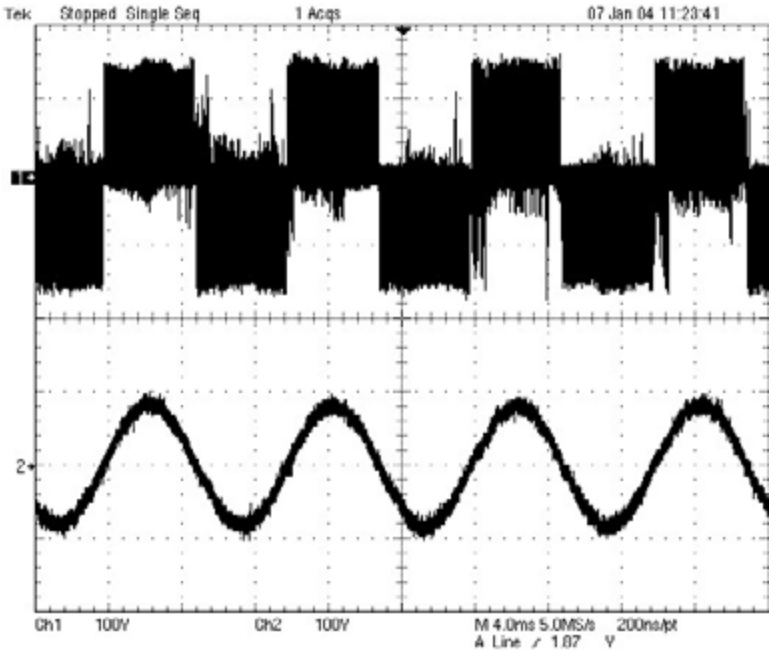


Figure 3.28: The 100-Hz output line-line voltage waveforms for Case 2
Trace 1: PWM voltage waveform at the output of the switch network
Trace 2: load voltage waveform after filtered by LC output low-pass network

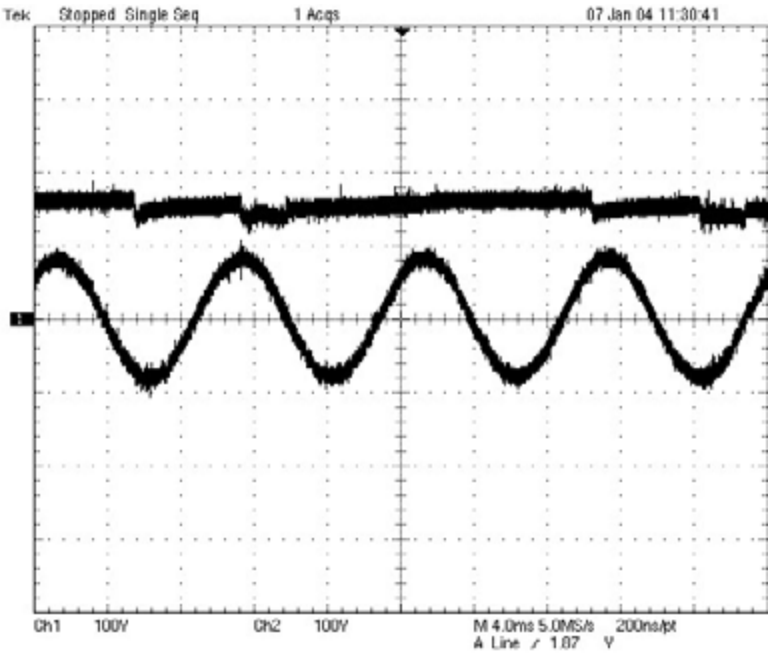


Figure 3.29: Variation of DC capacitor voltage, without active control
Trace 1: DC capacitor voltage waveform
Trace 2: filtered load voltage waveform
Both traces have scale of 100 V/div

3.3.2.3 Case 3

Case 3 illustrates the boosting voltage magnitude capacity of the multilevel matrix converter with the single-capacitor control scheme. The 60-Hz input voltages were converted into 30-Hz output voltages with the modulation indices of M_{in} = 0.7 and M_{out} = 0.9. The DC-capacitor voltages must be greater than both input and output line-line voltage magnitudes.

The input and the output PWM line-line voltage waveforms and current waveforms are shown in Fig. 3.30. The trajectories of the input and output voltages in the *dq* coordinate are shown in Fig. 3.31. The trajectories of the input and output currents in the *dq* coordinate are shown in Fig. 3.32. Figure 3.33 shows a waveform of the output PWM line-line voltage along with a waveform of the filtered output line-line voltage. The variation of capacitor voltage along the output line period is shown in Fig. 3.34.

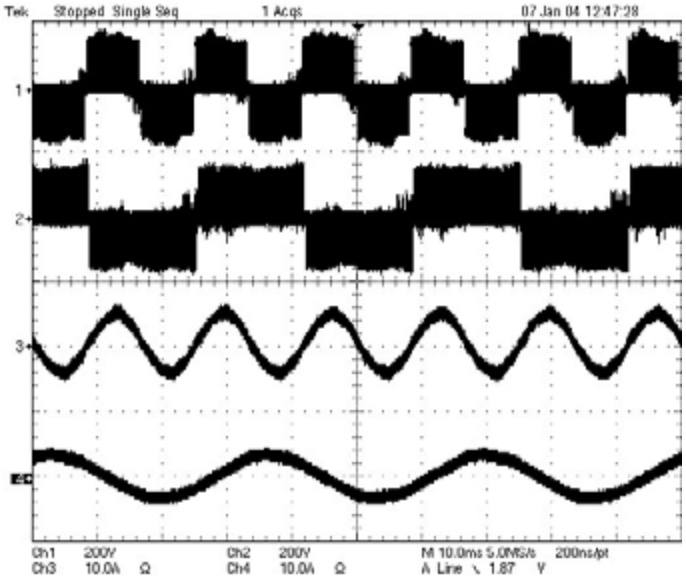


Figure 3.30: Voltage and current waveforms, Case 3
Trace 1: input line-line PWM voltage waveform at 200 V/div
Trace 2: output-side line-line PWM voltage waveform at 200 V/div
Trace 3: input phase current at 10 A/div
Trace 4: output phase current at 10 A/div
Horizontal scale: 10 ms/div

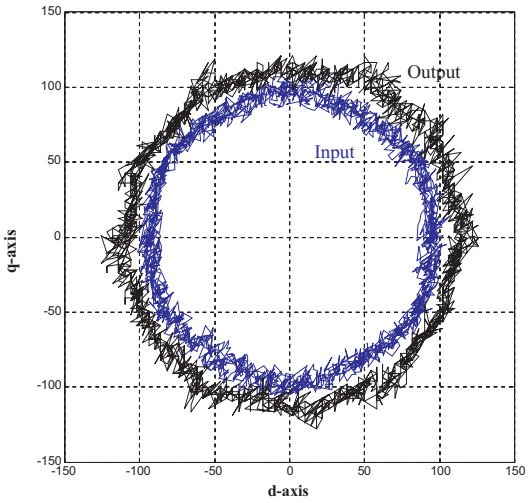


Figure 3.31: Trajectories of input- and output-voltages in *dq* coordinate

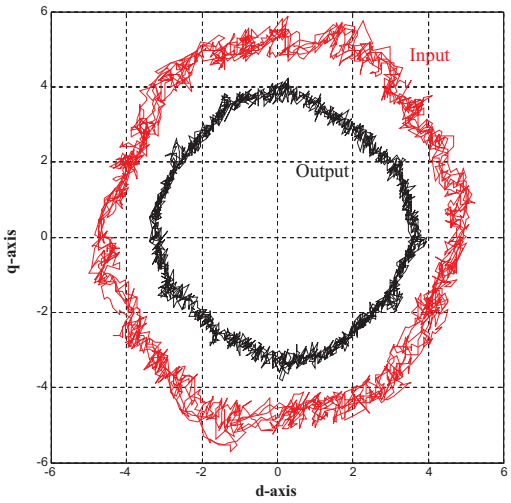


Figure 3.32: Trajectories of input- and output-currents in *dq* coordinate

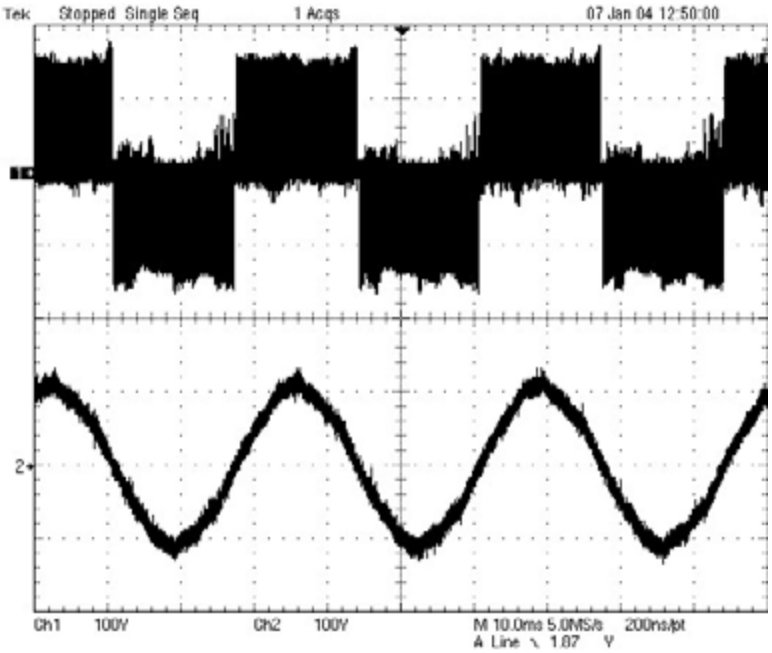


Figure 3.33: The 30-Hz output line-line voltage waveforms for Case 3
Trace 1: PWM voltage waveform at the output of the switch network
Trace 2: load voltage waveform after filtered by LC output low-pass network

3.4 Summary of Key Points

In this chapter, two control schemes for the multilevel matrix converter with basic converter configuration operated with two-level switching were described. The control schemes are the extension of the SVM technique, which is employed to synthesize the terminal ac voltages. The SVM involves the null-state space vector and the six space vectors with magnitude $2V_{cap}/\sqrt{3}$ for the two-level switching.

In the eight-capacitor control scheme, the switch-cell capacitors are connected in parallel. In addition, all nine switch cells conduct currents at any given instant. The switch-cell capacitors employed in each subinterval of a switching period show all possible capacitors that can be used. With this control scheme, the converter configuration depends only on the input- and output-side space vectors. The parallel connection of capacitors increases the effective capacitance for transferring energy of the converter. In each subinterval of a switching period, the converter employs a different set of switch-cell capacitors to synthesize terminal voltages. As a result, charge balances of the capacitors cannot be achieved.

In the single-capacitor control scheme, only one switch-cell capacitor is employed to synthesize terminal voltages during each switching period; all nine switch-cell capacitors are employed throughout the input- and output-side line periods. The control scheme determines the single capacitor to be employed in each switching period from two conditions: the positions of the input-side and the output-side reference space vectors and the relative values of the duty cycles of the input-side and the output-side null-state space vectors. This control scheme is optimized in a sense of minimizing circulating currents among the capacitors. In addition, the charge balance of the capacitors can be achieved in one switching cycle. This control scheme allows the converter to be modeled as a DC-link converter, simplifying the complexity of the multilevel matrix converter. To guarantee that there is one valid switch-cell capacitor for every subinterval throughout each switching period, a specific pattern of space vectors is required; hence, the single-capacitor control scheme can operate within a range of voltage-gain ratios.

The single-capacitor control scheme can theoretically stabilize the capacitor voltages in the multilevel matrix converter by keeping the charge balance on the single capacitor employed in each switching period. However, the experimental results also indicated that there were deviations in the capacitor voltages. The disturbances in the capacitor voltages arise from parasitic inductances inside the converter. These capacitor voltage disturbances lead to current spikes circulating inside the converter and, therefore, restrain the multilevel matrix converter from operating at higher voltages. Consequently, well-regulated capacitor voltages are required. A capacitor voltage-balancing scheme, which is based on the modification of the SVM, is described in the next chapter.

4 Capacitor Voltage Balancing Control

This chapter describes the capacitor voltage balancing control, which was proposed to regulate capacitor voltages of the multilevel matrix converter. The control scheme is based on the modification of the SVM so that two additional capacitors can be charged and discharged in each switching period. By using two additional space vectors ─having the same magnitude but opposite directions─to partially replace the null-state space vector in each switching period, the proposed capacitor voltage balancing control has minimum effect on the average terminal voltages. A Lyapunov's approach is used to prove the stability of the control scheme.

4.1 Disturbances in the Capacitor Voltages

In the multilevel matrix converter, the primary source of disturbance to the capacitor voltages arises from the energy stored in the stray inductances of the wiring interconnecting switch cells. During the dead-time interval of the on-to-off-state transitions of each switch cell, the energy from the stray-wiring inductance is transferred into the switch-cell capacitor through the anti-parallel diodes. The capacitor voltage is gradually charged up when the capacitor is not employed to generate terminal voltages. This continues until the first switching period, when the capacitor is used in the converter, then it is quickly discharged. As a result, a high-magnitude current spike is induced inside the converter. This behavior in the capacitor voltages restrains the converter from being operated at higher voltages. The effect of the stray inductances on capacitor voltages is dependent on the load current and the switching frequency of the converter.

Figure 4.1 and 4.2 show experimental waveforms of the capacitor voltages when the multilevel matrix converter operated at switching frequencies of 50 kHz and 25 kHz, respectively. It can be observed from the experimental results that the capacitor was charged more slowly at lower switching frequency (the slope of the capacitor voltage is flatter at lower switching frequency). As a result, the deviation in the capacitor voltage is decreased from 35 % to 20 % when the switching frequency of the converter is reduced from 50 kHz to 25 kHz.

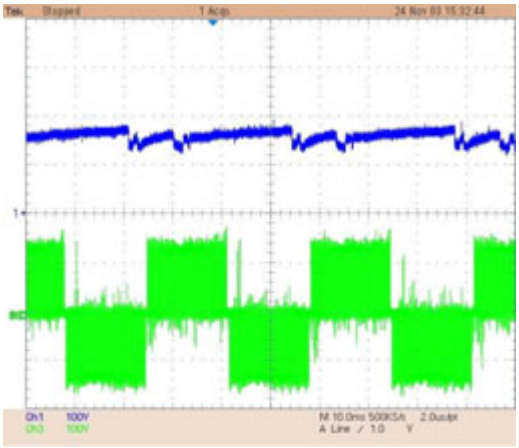


Figure 4.1: Capacitor voltage and output PWM line-line voltage waveforms when the converter operated at the switching frequency of 50 kHz

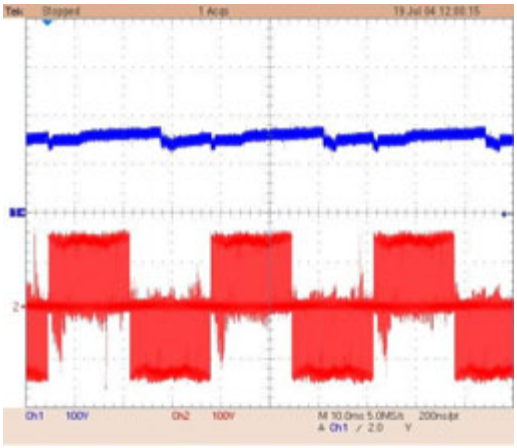


Figure 4.2 Capacitor voltage and output PWM line-line voltage waveforms when with the converter operated at the switching frequency of 25 kHz

Similar to other converters that employ multi-level switching and multiple capacitors, capacitor voltage balancing is a considerably complex problem. A general cause of the problem is that different currents flow through capacitors during converter operation. Many capacitor voltage balancing schemes have been proposed for the multilevel DC-link converter by using additional control schemes [23, 38, 44, 55] or auxiliary circuits [56]. However, with singularities in the structure and operation, those control schemes cannot be directly applied to the multilevel matrix converter.

To regulate capacitor voltages with minimum effect on the average terminal voltages, a capacitor voltage balancing control is proposed based on the modification of the SVM. The proposed control scheme uses two additional space vectors having the same magnitude but opposite directions to partially replace the null-state space vector. The use of opposite space vectors allows two additional capacitors to be charged and discharged in each switching period. In addition, the opposite space vectors with the same magnitude provide line-line voltages with the average of zero, similar to the null-state space vector. The control scheme is orthogonal to the average terminal-voltage synthesizing; therefore, it can be applied with the single-capacitor control scheme.

4.2 Capacitor Voltage Balancing Control

The single-capacitor control scheme described in the previous chapter can theoretically stabilize all nine capacitor voltages. However, with the limitation that only one capacitor is allowed in each switching period and the single capacitor is chosen independently from the capacitor voltage, the control scheme alone is not able to regulate all nine capacitor voltages in the multilevel matrix converter.
One possible approach for regulating capacitor voltages in the multilevel matrix converter can be achieved by reallocating the space vectors. In each switching period, an additional subinterval is generated such that change in the charge of the single capacitor employed during the subinterval can be determined. Figure 4.3 illustrates the space-vector patterns for regulating capacitor voltages.

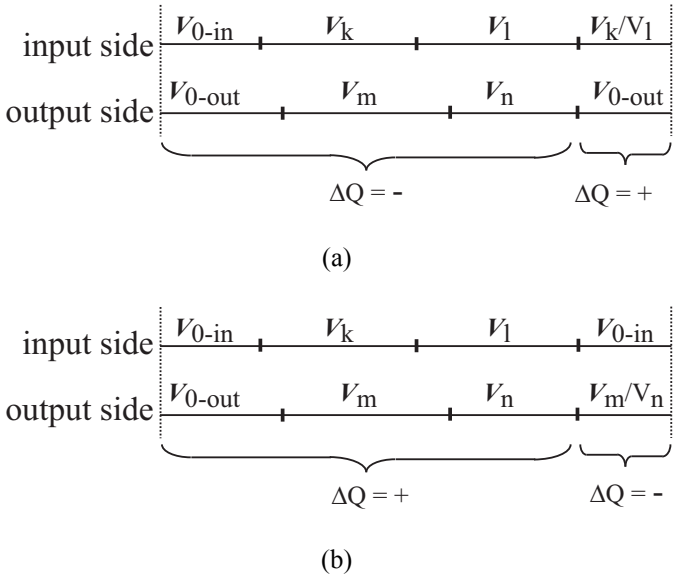


Figure 4.3: Space-vector pattern for regulating capacitor voltages: (a) for charging capacitor, (b) for discharging capacitor

The terminal voltages at the input side of the converter are modulated among the space vectors V_k, V_l, and $V_{0\text{-}in}$. The space vectors V_k and V_l are the two adjacent space vectors of the input-side reference space vector, and the space vector $V_{0\text{-}in}$ is the input-side null-state space vector. Similarly, the terminal voltages at the output side of the converter are modulated among the space vectors V_m, V_n, and $V_{0\text{-}out}$. The space vectors V_m and V_n are the two adjacent space vectors of the output-side reference space vector, and the space vector $V_{0\text{-}out}$ is the output-side null-state space vector.

To charge a capacitor, an additional subinterval having a non-zero space vector at the input side and the null-state space vector at the output (Fig. 4.3[a]) is employed. Assume that the power is transferred from the input side to the output side of the converter and only one switch-cell capacitor is used in the converter during each subinterval. There is no output energy while input energy exists in the additional subinterval (the last subinterval); therefore, the input energy is stored and charges the capacitor employed in that subinterval. Likewise, an additional subinterval having the null-state space vector at the input side and a non-zero state space vector at the output (Fig. 4.3[b]) is applied to discharge a capacitor. With no input energy, the output energy is supplied only from the capacitor employed in the additional subinterval.

With the concept described above, the choice of which capacitor to use in the additional subinterval is limited. The combination of the null-state space vector at one side of the converter and the space vector with magnitude $2V_{cap}/\sqrt{3}$ at the other side allows only three switch-cell capacitors to be chosen. Because either one of the two adjacent space vectors can be used in the additional subinterval, a total of six of nine switching-cell capacitors can be chosen for regulation. In addition, the charge on the capacitor employed in the remaining subintervals is also affected by the additional subinterval.

To involve any given capacitor in each switching period with minimum effect on the terminal voltages and charge on the other capacitors, a capacitor voltage balancing approach is proposed based on the modified SVM. Note that when the multilevel matrix converter operates in the two-level switching mode, the SVM involves the null-state space vector and the six space vectors with magnitude $2V_{cap}/\sqrt{3}$ (Fig. 4.4). The space vectors can be used to determine the current flowing through the single capacitor employed to generate terminal voltages.

In the multilevel matrix converter, the current flowing through any single capacitor in each switching-device combination depends solely on the input-side and the output-side space vectors and not on the other details of the specific switch state of the converter. In other words, for redundant switch combinations that generate identical terminal voltages, the current flowing through a capacitor employed in each redundant switch combination is also the same. An example of redundant switch combinations that generate terminal voltages $V_{AB} = -V_{cap}$, $V_{BC} = 0$ V, $V_{CA} = +V_{cap}$, and $V_{ab} = V_{bc} = V_{ca} = 0$ V is shown in Fig. 4.5. In the first switching-device combination, the input current I_A flows through the capacitor C_{Aa}, which is the capacitor in the switch cell connected between the input phase A and the output phase a. Capacitors C_{Ab} and C_{Ac} also have current I_A flow-through in the second and the third switching-device combination, respectively.

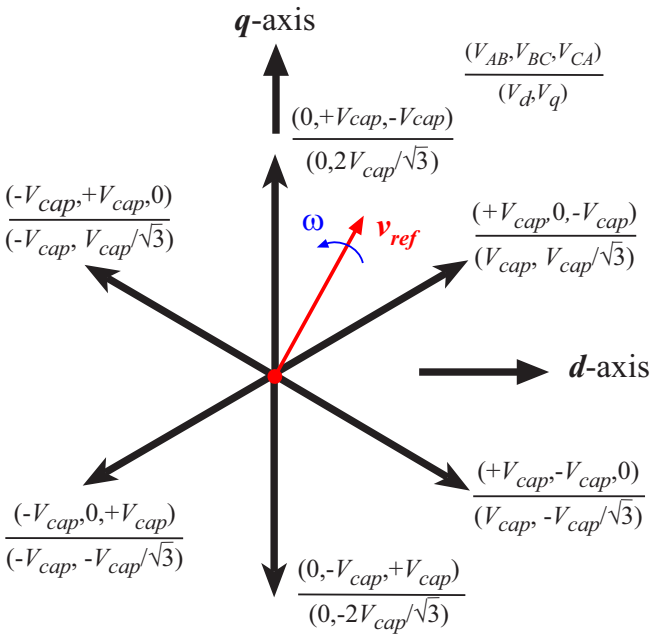


Figure 4.4: Seven space vectors employed in the two-level switching

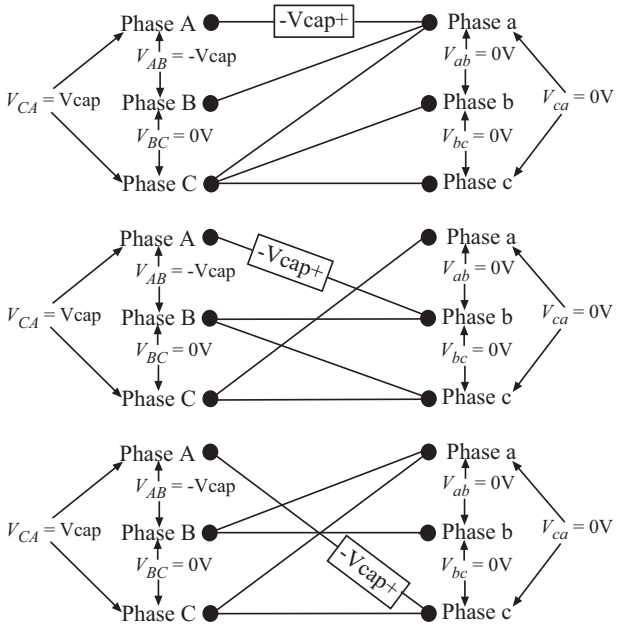


Figure 4.5: An example of redundant switching combinations having the input current I_A through switchcell capacitors

Tables 4.1 and 4.2 summarize the corresponding currents flowing through the single capacitor employed to generate the input-side space vectors and the output-side space vectors, respectively. The reference direction of the input currents is assumed to flow into the converter, whereas the reference direction of the output currents is assumed to flow out of the converter. It can be seen from the tables that, for any opposite space vectors, the currents through the capacitors also flow in opposite directions, independent of the specific choice of the capacitors.

Table 4.1: Input Currents Through a Capacitor for Each Input-Side Space Vector

Input-side space vector (V_d, V_q)	Current
$(V_{cap}, V_{cap}/\sqrt{3})$	I_A
$(0, 2V_{cap}/\sqrt{3})$	$-I_C$
$(-V_{cap}, V_{cap}/\sqrt{3})$	I_B
$(-V_{cap}, -V_{cap}/\sqrt{3})$	$-I_A$
$(0, -2V_{cap}/\sqrt{3})$	I_C
$(V_{cap}, -V_{cap}/\sqrt{3})$	$-I_B$

Table 4.2: Output Currents Through a Capacitor for Each Output-Side Space Vector

Output-side space vector (V_d, V_q)	Current
$(V_{cap}, V_{cap}/\sqrt{3})$	$-I_a$
$(0, 2V_{cap}/\sqrt{3})$	I_c
$(-V_{cap}, V_{cap}/\sqrt{3})$	$-I_b$
$(-V_{cap}, -V_{cap}/\sqrt{3})$	I_a
$(0, -2V_{cap}/\sqrt{3})$	$-I_c$
$(V_{cap}, -V_{cap}/\sqrt{3})$	I_b

4.2.1 Modified SVM

To minimize the effect on the synthesizing terminal voltages, two additional space vectors having the same magnitude but opposite directions are used to partially replace the null-state space vector. Two opposite space vectors with the same magnitude also contribute to the average of zero voltage for all line-line voltages, similar to the null-state space vectors. The two opposite space vectors allow two additional capacitors to be charged and discharged in each switching period.

With the modified approach for the capacitor voltage balancing scheme, the SVM for two-level switching at each side of the converter can involve the maximum of five space vectors in each switching period: a null-state space vector, two adjacent space vectors (similar to the conventional SVM), and two opposite space vectors. Figure 4.6 shows the diagram of the modified SVM technique. Space vector V_0 is the null-state space vector. Space vectors V_k and V_l are two adjacent space vectors of the reference space vector, V_{ref}. Space vectors V_x and V_y are any two opposite space vectors. The reference space vector V_{ref} can be expressed as

$$\boldsymbol{V_{ref}} = d_k\boldsymbol{V_k} + d_l\boldsymbol{V_l} + d_0\boldsymbol{V_0} + d'\boldsymbol{V_x} + d'\boldsymbol{V_y} \qquad \text{with} \quad d_0 = 1 - d_k - d_l - 2d' \tag{4.1}$$

where d_k and d_l are the duty cycles of the space vectors V_k and V_l, respectively, which can be obtained from Eq. (3.3). The variable d' is the duty cycle of the opposite space vectors. The two opposite space vectors and the null-state space vector contribute to the average of zero voltage for all line-line voltages.

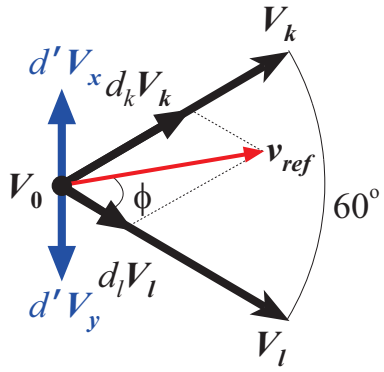


Figure 4.6: Modified SVM

Consider the case when the modified SVM is employed to synthesize terminal voltages at the output-side of the converter. The pattern of the space vectors in one switching period is illustrated in Fig. 4.7. The terminal voltages at the input side are modulated among the two adjacent space vectors of the input-side reference space vector (V_k and V_l) and the input-side null-state space vector ($V_{0\text{-}in}$). The terminal voltages at the output side are modulated among the two adjacent space vectors of the output-side reference space vector (V_m and V_n), the output-side null-state space vector ($V_{0\text{-}out}$), and the two opposite space vectors (V_x and V_y). As a result, with the modified SVM, each switching period can have the maximum of seven subintervals that have different combinations of the input-side and output-side space vectors. With the conventional SVM technique, each switching period can have the maximum of five subintervals. By

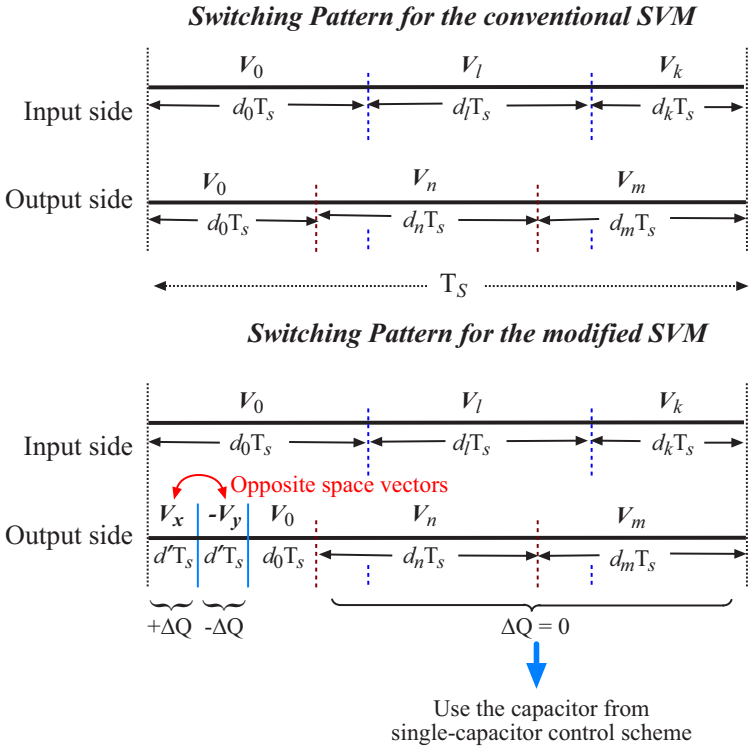


Figure 4.7: Space vector patterns with the opposite space vectors at the output side

using two opposite space vectors with the same duty cycle to partially replace the null-state space vector obtained from the conventional SVM technique, the modified SVM can generate the same reference space vector as the conventional SVM.

With the modified SVM, the multilevel matrix converter can involve a maximum of three capacitors in each switching period. In the first two subintervals, where the opposite space vectors are employed at the output side, two capacitors can be charged and discharged because the currents flowing through the two capacitors employed in these two subintervals are also in the opposite directions. The currents flowing through the capacitors can be determined from the output space vector (Table 4.2). Capacitor charges are transferred between these two capacitors during the first two subintervals. As a result, the other capacitor employed in the remaining subinterval, which can be selected using the single-capacitor control scheme, experiences no net change in charge.

When the modified SVM is applied at either the input or output side, the choices of switch-cell capacitors to be regulated is limited. In addition, only one choice of current is available for regulating the capacitors . This makes the capacitor voltage balancing control saturated when the control tries to regulate the capacitors with a low-magnitude (near the zero-crossing) current.

To regulate any two of nine capacitors in each switching period, the modified SVMs must be applied at

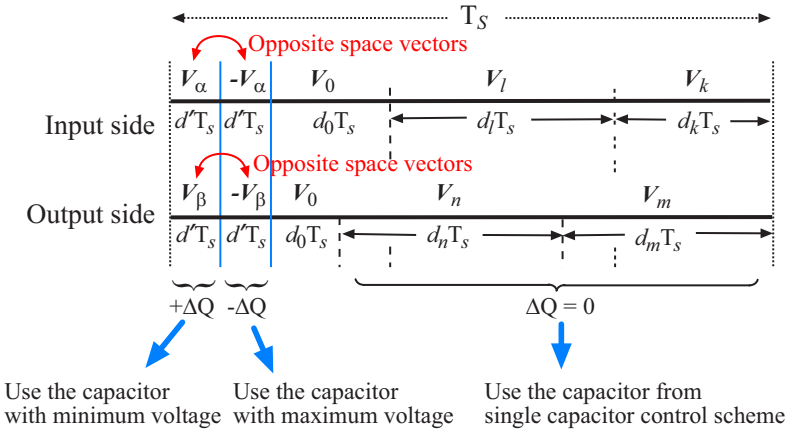


Figure 4.8: Space-vector patterns in each switching period having opposite space vectors at the input and output sides

both sides of the converter. This also allows more choices of currents to regulate the capacitors. For simplicity of control, the duty cycles are equal for the opposite space vectors applied to the SVMs at both sides of the converter.. Note that the opposite space vectors at the input-side and the output-side are independent of each other. Consequently, each switching period still consists of the maximum of seven subintervals. Two additional subintervals are generated from opposite space vectors at both input- and output-sides (Fig. 4.8).

Knowing the input-side and output-side space vectors in the additional subintervals, the currents through the capacitors employed in those subintervals can be determined regardless of the capacitors. The currents flowing through the capacitors in these two additional subintervals are the combinations of the input- and output-phase currents, which can be determined using Tables 4.1 and 4.2. Because the opposite space vectors are employed in two additional subintervals, the currents through the capacitors during those

subintervals also flow in the opposite direction. The control scheme must be able to employ the capacitor according to the current in each additional subinterval.

Note that for a given combination of the input- and output-side space vectors, some capacitors cannot be employed. To ensure that the control scheme can regulate any two of the nine switch-cell capacitors, the two capacitors that need to be regulated are used to determine the opposite space vectors.

4.2.2 Determination of Two Opposite Space Vectors

The purpose of the capacitor voltage-balancing scheme is to drive all capacitor voltages to the same value, which is the average of all nine capacitor voltages. Therefore, each capacitor voltage is defined as

$$V_{cap} = V_{cap\_avg} + \hat{v}_{cap} \tag{4.2}$$

where V_{cap_avg} is the average of all nine capacitor voltages and $\hat{v}_{cap}$ is the error of the capacitor voltage from the average value.

Using two opposite space vectors, two capacitors can be regulated during a switching period. The two capacitors having the maximum positive and maximum negative error voltages are selected to be discharged and charged, respectively. The remaining capacitor error voltages are unchanged and bounded by these two voltages. For any given combination of the two capacitors, a set of two opposite space vectors can be found that allows the desired capacitors to be charged and discharged.

The selection of any two from the nine switch-cell capacitors to be regulated during each switching period provides 36 possible combinations. In addition, four or five sets of opposite space vectors exist for each combination of two capacitors. Table 4.3 lists the sets of input- and output-side space vectors that can be generated by using both of two switch-cell capacitors. The sets of input-side and output-side space vectors that have the opposite directions are further grouped together. The notation of the space vectors can be referred in Fig. 4.4. A set of opposite space vectors is selected from the combination that provides the largest current magnitude through the capacitor and, hence, the highest gain. This avoids the saturation of the control scheme by regulating a capacitor with a low-magnitude (near-zero) current.

Table 4.3: Sets of Opposite Space Vectors for Each Combination of Two-Cell Capacitors

Combination of two capacitors	Sets of opposite space vectors ($\boldsymbol{V_{input-side}}$,$\boldsymbol{V_{output-side}}$)
(C_{Aa}, C_{Ab})	$\langle(\boldsymbol{V_1}, \boldsymbol{V_0}), (\boldsymbol{V_4}, \boldsymbol{V_0})\rangle$ $\langle(\boldsymbol{V_1}, \boldsymbol{V_5}), (\boldsymbol{V_4}, \boldsymbol{V_2})\rangle$ $\langle(\boldsymbol{V_3}, \boldsymbol{V_2}), (\boldsymbol{V_6}, \boldsymbol{V_5})\rangle$ $\langle(\boldsymbol{V_5}, \boldsymbol{V_2}), (\boldsymbol{V_2}, \boldsymbol{V_5})\rangle$
(C_{Aa}, C_{Ac})	$\langle(\boldsymbol{V_1}, \boldsymbol{V_0}), (\boldsymbol{V_4}, \boldsymbol{V_0})\rangle$ $\langle(\boldsymbol{V_1}, \boldsymbol{V_3}), (\boldsymbol{V_4}, \boldsymbol{V_6})\rangle$ $\langle(\boldsymbol{V_3}, \boldsymbol{V_6}), (\boldsymbol{V_6}, \boldsymbol{V_3})\rangle$ $\langle(\boldsymbol{V_5}, \boldsymbol{V_6}), (\boldsymbol{V_2}, \boldsymbol{V_3})\rangle$
(C_{Aa}, C_{Ba})	$\langle(\boldsymbol{V_0}, \boldsymbol{V_1}), (\boldsymbol{V_0}, \boldsymbol{V_4})\rangle$ $\langle(\boldsymbol{V_5}, \boldsymbol{V_1}), (\boldsymbol{V_2}, \boldsymbol{V_4})\rangle$ $\langle(\boldsymbol{V_5}, \boldsymbol{V_2}), (\boldsymbol{V_2}, \boldsymbol{V_5})\rangle$ $\langle(\boldsymbol{V_5}, \boldsymbol{V_6}), (\boldsymbol{V_2}, \boldsymbol{V_3})\rangle$
(C_{Aa}, C_{Bb})	$\langle(\boldsymbol{V_1}, \boldsymbol{V_3}), (\boldsymbol{V_4}, \boldsymbol{V_6})\rangle$ $\langle(\boldsymbol{V_1}, \boldsymbol{V_4}), (\boldsymbol{V_4}, \boldsymbol{V_1})\rangle$ $\langle(\boldsymbol{V_5}, \boldsymbol{V_2}), (\boldsymbol{V_2}, \boldsymbol{V_5})\rangle$ $\langle(\boldsymbol{V_3}, \boldsymbol{V_1}), (\boldsymbol{V_6}, \boldsymbol{V_4})\rangle$ $\langle(\boldsymbol{V_3}, \boldsymbol{V_6}), (\boldsymbol{V_6}, \boldsymbol{V_3})\rangle$
(C_{Aa}, C_{Bc})	$\langle(\boldsymbol{V_1}, \boldsymbol{V_4}), (\boldsymbol{V_4}, \boldsymbol{V_1})\rangle$ $\langle(\boldsymbol{V_1}, \boldsymbol{V_5}), (\boldsymbol{V_4}, \boldsymbol{V_2})\rangle$ $\langle(\boldsymbol{V_3}, \boldsymbol{V_1}), (\boldsymbol{V_6}, \boldsymbol{V_4})\rangle$ $\langle(\boldsymbol{V_3}, \boldsymbol{V_2}), (\boldsymbol{V_6}, \boldsymbol{V_5})\rangle$ $\langle(\boldsymbol{V_5}, \boldsymbol{V_6}), (\boldsymbol{V_2}, \boldsymbol{V_3})\rangle$
(C_{Aa}, C_{Ca})	$\langle(\boldsymbol{V_0}, \boldsymbol{V_1}), (\boldsymbol{V_0}, \boldsymbol{V_4})\rangle$ $\langle(\boldsymbol{V_3}, \boldsymbol{V_1}), (\boldsymbol{V_6}, \boldsymbol{V_4})\rangle$ $\langle(\boldsymbol{V_3}, \boldsymbol{V_2}), (\boldsymbol{V_6}, \boldsymbol{V_5})\rangle$ $\langle(\boldsymbol{V_3}, \boldsymbol{V_6}), (\boldsymbol{V_6}, \boldsymbol{V_3})\rangle$
(C_{Aa}, C_{Cb})	$\langle(\boldsymbol{V_1}, \boldsymbol{V_3}), (\boldsymbol{V_4}, \boldsymbol{V_6})\rangle$ $\langle(\boldsymbol{V_1}, \boldsymbol{V_4}), (\boldsymbol{V_4}, \boldsymbol{V_1})\rangle$ $\langle(\boldsymbol{V_3}, \boldsymbol{V_2}), (\boldsymbol{V_6}, \boldsymbol{V_5})\rangle$ $\langle(\boldsymbol{V_5}, \boldsymbol{V_1}), (\boldsymbol{V_2}, \boldsymbol{V_4})\rangle$ $\langle(\boldsymbol{V_5}, \boldsymbol{V_6}), (\boldsymbol{V_2}, \boldsymbol{V_3})\rangle$
(C_{Aa}, C_{Cc})	$\langle(\boldsymbol{V_1}, \boldsymbol{V_4}), (\boldsymbol{V_4}, \boldsymbol{V_1})\rangle$ $\langle(\boldsymbol{V_1}, \boldsymbol{V_5}), (\boldsymbol{V_4}, \boldsymbol{V_2})\rangle$ $\langle(\boldsymbol{V_3}, \boldsymbol{V_6}), (\boldsymbol{V_6}, \boldsymbol{V_3})\rangle$ $\langle(\boldsymbol{V_5}, \boldsymbol{V_1}), (\boldsymbol{V_2}, \boldsymbol{V_4})\rangle$ $\langle(\boldsymbol{V_5}, \boldsymbol{V_2}), (\boldsymbol{V_2}, \boldsymbol{V_5})\rangle$
(C_{Ab}, C_{Ac})	$\langle(\boldsymbol{V_1}, \boldsymbol{V_0}), (\boldsymbol{V_4}, \boldsymbol{V_0})\rangle$ $\langle(\boldsymbol{V_1}, \boldsymbol{V_1}), (\boldsymbol{V_4}, \boldsymbol{V_4})\rangle$ $\langle(\boldsymbol{V_5}, \boldsymbol{V_4}), (\boldsymbol{V_2}, \boldsymbol{V_1})\rangle$ $\langle(\boldsymbol{V_3}, \boldsymbol{V_4}), (\boldsymbol{V_6}, \boldsymbol{V_1})\rangle$
(C_{Ab}, C_{Ba})	$\langle(\boldsymbol{V_1}, \boldsymbol{V_1}), (\boldsymbol{V_4}, \boldsymbol{V_4})\rangle$ $\langle(\boldsymbol{V_1}, \boldsymbol{V_6}), (\boldsymbol{V_4}, \boldsymbol{V_3})\rangle$ $\langle(\boldsymbol{V_5}, \boldsymbol{V_2}), (\boldsymbol{V_2}, \boldsymbol{V_5})\rangle$ $\langle(\boldsymbol{V_3}, \boldsymbol{V_3}), (\boldsymbol{V_6}, \boldsymbol{V_6})\rangle$ $\langle(\boldsymbol{V_3}, \boldsymbol{V_4}), (\boldsymbol{V_6}, \boldsymbol{V_1})\rangle$
(C_{Ab}, C_{Bb})	$\langle(\boldsymbol{V_0}, \boldsymbol{V_3}), (\boldsymbol{V_0}, \boldsymbol{V_6})\rangle$ $\langle(\boldsymbol{V_5}, \boldsymbol{V_2}), (\boldsymbol{V_2}, \boldsymbol{V_5})\rangle$ $\langle(\boldsymbol{V_5}, \boldsymbol{V_3}), (\boldsymbol{V_2}, \boldsymbol{V_6})\rangle$ $\langle(\boldsymbol{V_5}, \boldsymbol{V_4}), (\boldsymbol{V_2}, \boldsymbol{V_1})\rangle$
(C_{Ab}, C_{Bc})	$\langle(\boldsymbol{V_1}, \boldsymbol{V_5}), (\boldsymbol{V_4}, \boldsymbol{V_2})\rangle$ $\langle(\boldsymbol{V_1}, \boldsymbol{V_6}), (\boldsymbol{V_4}, \boldsymbol{V_3})\rangle$ $\langle(\boldsymbol{V_5}, \boldsymbol{V_4}), (\boldsymbol{V_2}, \boldsymbol{V_1})\rangle$ $\langle(\boldsymbol{V_3}, \boldsymbol{V_2}), (\boldsymbol{V_6}, \boldsymbol{V_5})\rangle$ $\langle(\boldsymbol{V_3}, \boldsymbol{V_3}), (\boldsymbol{V_6}, \boldsymbol{V_6})\rangle$
(C_{Ab}, C_{Ca})	$\langle(\boldsymbol{V_1}, \boldsymbol{V_1}), (\boldsymbol{V_4}, \boldsymbol{V_4})\rangle$ $\langle(\boldsymbol{V_1}, \boldsymbol{V_6}), (\boldsymbol{V_4}, \boldsymbol{V_3})\rangle$ $\langle(\boldsymbol{V_3}, \boldsymbol{V_2}), (\boldsymbol{V_6}, \boldsymbol{V_5})\rangle$ $\langle(\boldsymbol{V_5}, \boldsymbol{V_3}), (\boldsymbol{V_2}, \boldsymbol{V_6})\rangle$ $\langle(\boldsymbol{V_5}, \boldsymbol{V_4}), (\boldsymbol{V_2}, \boldsymbol{V_1})\rangle$
(C_{Ab}, C_{Cb})	$\langle(\boldsymbol{V_0}, \boldsymbol{V_3}), (\boldsymbol{V_0}, \boldsymbol{V_6})\rangle$ $\langle(\boldsymbol{V_3}, \boldsymbol{V_2}), (\boldsymbol{V_6}, \boldsymbol{V_5})\rangle$ $\langle(\boldsymbol{V_3}, \boldsymbol{V_3}), (\boldsymbol{V_6}, \boldsymbol{V_6})\rangle$ $\langle(\boldsymbol{V_3}, \boldsymbol{V_4}), (\boldsymbol{V_6}, \boldsymbol{V_1})\rangle$
(C_{Ab}, C_{Cc})	$\langle(\boldsymbol{V_1}, \boldsymbol{V_5}), (\boldsymbol{V_4}, \boldsymbol{V_2})\rangle$ $\langle(\boldsymbol{V_1}, \boldsymbol{V_6}), (\boldsymbol{V_4}, \boldsymbol{V_3})\rangle$ $\langle(\boldsymbol{V_3}, \boldsymbol{V_4}), (\boldsymbol{V_6}, \boldsymbol{V_1})\rangle$ $\langle(\boldsymbol{V_5}, \boldsymbol{V_2}), (\boldsymbol{V_2}, \boldsymbol{V_5})\rangle$ $\langle(\boldsymbol{V_5}, \boldsymbol{V_3}), (\boldsymbol{V_2}, \boldsymbol{V_6})\rangle$
(C_{Ac}, C_{Ba})	$\langle(\boldsymbol{V_1}, \boldsymbol{V_1}), (\boldsymbol{V_4}, \boldsymbol{V_4})\rangle$ $\langle(\boldsymbol{V_1}, \boldsymbol{V_2}), (\boldsymbol{V_4}, \boldsymbol{V_5})\rangle$ $\langle(\boldsymbol{V_3}, \boldsymbol{V_4}), (\boldsymbol{V_6}, \boldsymbol{V_1})\rangle$ $\langle(\boldsymbol{V_3}, \boldsymbol{V_5}), (\boldsymbol{V_6}, \boldsymbol{V_2})\rangle$ $\langle(\boldsymbol{V_5}, \boldsymbol{V_6}), (\boldsymbol{V_2}, \boldsymbol{V_3})\rangle$
(C_{Ac}, C_{Bb})	$\langle(\boldsymbol{V_1}, \boldsymbol{V_2}), (\boldsymbol{V_4}, \boldsymbol{V_5})\rangle$ $\langle(\boldsymbol{V_1}, \boldsymbol{V_3}), (\boldsymbol{V_4}, \boldsymbol{V_6})\rangle$ $\langle(\boldsymbol{V_3}, \boldsymbol{V_5}), (\boldsymbol{V_6}, \boldsymbol{V_2})\rangle$ $\langle(\boldsymbol{V_3}, \boldsymbol{V_6}), (\boldsymbol{V_6}, \boldsymbol{V_3})\rangle$ $\langle(\boldsymbol{V_5}, \boldsymbol{V_4}), (\boldsymbol{V_2}, \boldsymbol{V_1})\rangle$
(C_{Ac}, C_{Bc})	$\langle(\boldsymbol{V_0}, \boldsymbol{V_2}), (\boldsymbol{V_0}, \boldsymbol{V_5})\rangle$ $\langle(\boldsymbol{V_5}, \boldsymbol{V_4}), (\boldsymbol{V_2}, \boldsymbol{V_1})\rangle$ $\langle(\boldsymbol{V_5}, \boldsymbol{V_5}), (\boldsymbol{V_2}, \boldsymbol{V_2})\rangle$ $\langle(\boldsymbol{V_5}, \boldsymbol{V_6}), (\boldsymbol{V_2}, \boldsymbol{V_3})\rangle$
(C_{Ac}, C_{Ca})	$\langle(\boldsymbol{V_1}, \boldsymbol{V_1}), (\boldsymbol{V_4}, \boldsymbol{V_4})\rangle$ $\langle(\boldsymbol{V_1}, \boldsymbol{V_2}), (\boldsymbol{V_4}, \boldsymbol{V_5})\rangle$ $\langle(\boldsymbol{V_3}, \boldsymbol{V_6}), (\boldsymbol{V_6}, \boldsymbol{V_3})\rangle$ $\langle(\boldsymbol{V_5}, \boldsymbol{V_4}), (\boldsymbol{V_2}, \boldsymbol{V_1})\rangle$ $\langle(\boldsymbol{V_5}, \boldsymbol{V_5}), (\boldsymbol{V_2}, \boldsymbol{V_2})\rangle$
(C_{Ac}, C_{Cb})	$\langle(\boldsymbol{V_1}, \boldsymbol{V_2}), (\boldsymbol{V_4}, \boldsymbol{V_5})\rangle$ $\langle(\boldsymbol{V_1}, \boldsymbol{V_3}), (\boldsymbol{V_4}, \boldsymbol{V_6})\rangle$ $\langle(\boldsymbol{V_3}, \boldsymbol{V_4}), (\boldsymbol{V_6}, \boldsymbol{V_1})\rangle$ $\langle(\boldsymbol{V_5}, \boldsymbol{V_5}), (\boldsymbol{V_2}, \boldsymbol{V_2})\rangle$ $\langle(\boldsymbol{V_5}, \boldsymbol{V_6}), (\boldsymbol{V_2}, \boldsymbol{V_3})\rangle$
(C_{Ac}, C_{Cc})	$\langle(\boldsymbol{V_0}, \boldsymbol{V_2}), (\boldsymbol{V_0}, \boldsymbol{V_5})\rangle$ $\langle(\boldsymbol{V_3}, \boldsymbol{V_4}), (\boldsymbol{V_6}, \boldsymbol{V_1})\rangle$ $\langle(\boldsymbol{V_3}, \boldsymbol{V_5}), (\boldsymbol{V_6}, \boldsymbol{V_2})\rangle$ $\langle(\boldsymbol{V_3}, \boldsymbol{V_6}), (\boldsymbol{V_6}, \boldsymbol{V_3})\rangle$

Table 4.3 continued: Sets of Opposite Space Vectors for Each Combination of Two-Cell Capacitors

Combination of two capacitors	Sets of opposite space vectors ($\boldsymbol{V_{input-side}}$,$\boldsymbol{V_{output-side}}$)
(C_{Ba}, C_{Bb})	$\langle(\boldsymbol{V_1}, \boldsymbol{V_2}), (\boldsymbol{V_4}, \boldsymbol{V_5})\rangle$ $\langle(\boldsymbol{V_3}, \boldsymbol{V_0}), (\boldsymbol{V_6}, \boldsymbol{V_0})\rangle$ $\langle(\boldsymbol{V_3}, \boldsymbol{V_5}), (\boldsymbol{V_6}, \boldsymbol{V_2})\rangle$ $\langle(\boldsymbol{V_5}, \boldsymbol{V_2}), (\boldsymbol{V_2}, \boldsymbol{V_5})\rangle$
(C_{Ba}, C_{Bc})	$\langle(\boldsymbol{V_1}, \boldsymbol{V_6}), (\boldsymbol{V_4}, \boldsymbol{V_3})\rangle$ $\langle(\boldsymbol{V_3}, \boldsymbol{V_0}), (\boldsymbol{V_6}, \boldsymbol{V_0})\rangle$ $\langle(\boldsymbol{V_3}, \boldsymbol{V_3}), (\boldsymbol{V_6}, \boldsymbol{V_6})\rangle$ $\langle(\boldsymbol{V_5}, \boldsymbol{V_6}), (\boldsymbol{V_2}, \boldsymbol{V_3})\rangle$
(C_{Ba}, C_{Ca})	$\langle(\boldsymbol{V_0}, \boldsymbol{V_1}), (\boldsymbol{V_0}, \boldsymbol{V_4})\rangle$ $\langle(\boldsymbol{V_1}, \boldsymbol{V_1}), (\boldsymbol{V_4}, \boldsymbol{V_4})\rangle$ $\langle(\boldsymbol{V_1}, \boldsymbol{V_2}), (\boldsymbol{V_4}, \boldsymbol{V_5})\rangle$ $\langle(\boldsymbol{V_1}, \boldsymbol{V_6}), (\boldsymbol{V_4}, \boldsymbol{V_3})\rangle$
(C_{Ba}, C_{Cb})	$\langle(\boldsymbol{V_1}, \boldsymbol{V_2}), (\boldsymbol{V_4}, \boldsymbol{V_5})\rangle$ $\langle(\boldsymbol{V_3}, \boldsymbol{V_3}), (\boldsymbol{V_6}, \boldsymbol{V_6})\rangle$ $\langle(\boldsymbol{V_3}, \boldsymbol{V_4}), (\boldsymbol{V_6}, \boldsymbol{V_1})\rangle$ $\langle(\boldsymbol{V_5}, \boldsymbol{V_1}), (\boldsymbol{V_2}, \boldsymbol{V_4})\rangle$ $\langle(\boldsymbol{V_5}, \boldsymbol{V_6}), (\boldsymbol{V_2}, \boldsymbol{V_3})\rangle$
(C_{Ba}, C_{Cc})	$\langle(\boldsymbol{V_1}, \boldsymbol{V_6}), (\boldsymbol{V_4}, \boldsymbol{V_3})\rangle$ $\langle(\boldsymbol{V_3}, \boldsymbol{V_5}), (\boldsymbol{V_6}, \boldsymbol{V_2})\rangle$ $\langle(\boldsymbol{V_3}, \boldsymbol{V_4}), (\boldsymbol{V_6}, \boldsymbol{V_1})\rangle$ $\langle(\boldsymbol{V_5}, \boldsymbol{V_1}), (\boldsymbol{V_2}, \boldsymbol{V_4})\rangle$ $\langle(\boldsymbol{V_5}, \boldsymbol{V_2}), (\boldsymbol{V_2}, \boldsymbol{V_5})\rangle$
(C_{Bb}, C_{Bc})	$\langle(\boldsymbol{V_1}, \boldsymbol{V_4}), (\boldsymbol{V_4}, \boldsymbol{V_1})\rangle$ $\langle(\boldsymbol{V_3}, \boldsymbol{V_0}), (\boldsymbol{V_6}, \boldsymbol{V_0})\rangle$ $\langle(\boldsymbol{V_3}, \boldsymbol{V_1}), (\boldsymbol{V_6}, \boldsymbol{V_4})\rangle$ $\langle(\boldsymbol{V_5}, \boldsymbol{V_4}), (\boldsymbol{V_2}, \boldsymbol{V_1})\rangle$
(C_{Bb}, C_{Ca})	$\langle(\boldsymbol{V_1}, \boldsymbol{V_2}), (\boldsymbol{V_4}, \boldsymbol{V_5})\rangle$ $\langle(\boldsymbol{V_3}, \boldsymbol{V_1}), (\boldsymbol{V_6}, \boldsymbol{V_4})\rangle$ $\langle(\boldsymbol{V_3}, \boldsymbol{V_6}), (\boldsymbol{V_6}, \boldsymbol{V_3})\rangle$ $\langle(\boldsymbol{V_5}, \boldsymbol{V_3}), (\boldsymbol{V_2}, \boldsymbol{V_6})\rangle$ $\langle(\boldsymbol{V_5}, \boldsymbol{V_4}), (\boldsymbol{V_2}, \boldsymbol{V_1})\rangle$
(C_{Bb}, C_{Cb})	$\langle(\boldsymbol{V_0}, \boldsymbol{V_3}), (\boldsymbol{V_0}, \boldsymbol{V_6})\rangle$ $\langle(\boldsymbol{V_1}, \boldsymbol{V_2}), (\boldsymbol{V_4}, \boldsymbol{V_5})\rangle$ $\langle(\boldsymbol{V_1}, \boldsymbol{V_3}), (\boldsymbol{V_4}, \boldsymbol{V_6})\rangle$ $\langle(\boldsymbol{V_1}, \boldsymbol{V_4}), (\boldsymbol{V_4}, \boldsymbol{V_1})\rangle$
(C_{Bb}, C_{Cc})	$\langle(\boldsymbol{V_1}, \boldsymbol{V_4}), (\boldsymbol{V_4}, \boldsymbol{V_1})\rangle$ $\langle(\boldsymbol{V_2}, \boldsymbol{V_5}), (\boldsymbol{V_5}, \boldsymbol{V_2})\rangle$ $\langle(\boldsymbol{V_2}, \boldsymbol{V_6}), (\boldsymbol{V_5}, \boldsymbol{V_3})\rangle$ $\langle(\boldsymbol{V_3}, \boldsymbol{V_5}), (\boldsymbol{V_6}, \boldsymbol{V_2})\rangle$ $\langle(\boldsymbol{V_3}, \boldsymbol{V_6}), (\boldsymbol{V_6}, \boldsymbol{V_3})\rangle$
(C_{Bc}, C_{Ca})	$\langle(\boldsymbol{V_1}, \boldsymbol{V_6}), (\boldsymbol{V_4}, \boldsymbol{V_3})\rangle$ $\langle(\boldsymbol{V_3}, \boldsymbol{V_1}), (\boldsymbol{V_6}, \boldsymbol{V_4})\rangle$ $\langle(\boldsymbol{V_3}, \boldsymbol{V_2}), (\boldsymbol{V_6}, \boldsymbol{V_5})\rangle$ $\langle(\boldsymbol{V_5}, \boldsymbol{V_4}), (\boldsymbol{V_2}, \boldsymbol{V_1})\rangle$ $\langle(\boldsymbol{V_5}, \boldsymbol{V_5}), (\boldsymbol{V_2}, \boldsymbol{V_2})\rangle$
(C_{Bc}, C_{Cb})	$\langle(\boldsymbol{V_1}, \boldsymbol{V_4}), (\boldsymbol{V_4}, \boldsymbol{V_1})\rangle$ $\langle(\boldsymbol{V_3}, \boldsymbol{V_2}), (\boldsymbol{V_6}, \boldsymbol{V_5})\rangle$ $\langle(\boldsymbol{V_3}, \boldsymbol{V_3}), (\boldsymbol{V_6}, \boldsymbol{V_6})\rangle$ $\langle(\boldsymbol{V_5}, \boldsymbol{V_5}), (\boldsymbol{V_2}, \boldsymbol{V_2})\rangle$ $\langle(\boldsymbol{V_5}, \boldsymbol{V_6}), (\boldsymbol{V_2}, \boldsymbol{V_3})\rangle$
(C_{Bc}, C_{Cc})	$\langle(\boldsymbol{V_0}, \boldsymbol{V_2}), (\boldsymbol{V_0}, \boldsymbol{V_5})\rangle$ $\langle(\boldsymbol{V_1}, \boldsymbol{V_4}), (\boldsymbol{V_4}, \boldsymbol{V_1})\rangle$ $\langle(\boldsymbol{V_1}, \boldsymbol{V_5}), (\boldsymbol{V_4}, \boldsymbol{V_2})\rangle$ $\langle(\boldsymbol{V_1}, \boldsymbol{V_6}), (\boldsymbol{V_4}, \boldsymbol{V_3})\rangle$
(C_{Ca}, C_{Cb})	$\langle(\boldsymbol{V_1}, \boldsymbol{V_2}), (\boldsymbol{V_4}, \boldsymbol{V_5})\rangle$ $\langle(\boldsymbol{V_3}, \boldsymbol{V_2}), (\boldsymbol{V_6}, \boldsymbol{V_5})\rangle$ $\langle(\boldsymbol{V_5}, \boldsymbol{V_0}), (\boldsymbol{V_2}, \boldsymbol{V_0})\rangle$ $\langle(\boldsymbol{V_5}, \boldsymbol{V_5}), (\boldsymbol{V_2}, \boldsymbol{V_2})\rangle$
(C_{Ca}, C_{Cc})	$\langle(\boldsymbol{V_1}, \boldsymbol{V_6}), (\boldsymbol{V_4}, \boldsymbol{V_3})\rangle$ $\langle(\boldsymbol{V_3}, \boldsymbol{V_6}), (\boldsymbol{V_6}, \boldsymbol{V_3})\rangle$ $\langle(\boldsymbol{V_5}, \boldsymbol{V_0}), (\boldsymbol{V_2}, \boldsymbol{V_0})\rangle$ $\langle(\boldsymbol{V_5}, \boldsymbol{V_3}), (\boldsymbol{V_2}, \boldsymbol{V_6})\rangle$
(C_{Cb}, C_{Cc})	$\langle(\boldsymbol{V_1}, \boldsymbol{V_4}), (\boldsymbol{V_4}, \boldsymbol{V_1})\rangle$ $\langle(\boldsymbol{V_3}, \boldsymbol{V_4}), (\boldsymbol{V_6}, \boldsymbol{V_1})\rangle$ $\langle(\boldsymbol{V_5}, \boldsymbol{V_0}), (\boldsymbol{V_2}, \boldsymbol{V_0})\rangle$ $\langle(\boldsymbol{V_5}, \boldsymbol{V_1}), (\boldsymbol{V_2}, \boldsymbol{V_4})\rangle$

For example, assume that the capacitors C_{Aa} and C_{Cc} have the maximum negative and the maximum positive error voltages, respectively. Figure 4.9 shows switching-device combinations that involve both capacitors. The switching-device combinations in the left column involve the capacitor C_{Aa}, whereas those in the right column involve the capacitor C_{Cc}. The terminal voltages generated from the switching-device combinations in each row are opposite each other; hence, the currents through capacitors C_{Aa} and C_{Cc} are also opposite each other. The switching-device combination in the top left column generates the input-side space vector (V_{cap}, $V_{cap}/\sqrt{3}$) as well as the output-side space vector (0, $-2V_{cap}/\sqrt{3}$) with the current (I_A-I_c) flowing through the capacitor C_{Aa}. When the input-side space vector is ($-V_{cap}$, $-V_{cap}/\sqrt{3}$) and the output-side space vector is (0, $2V_{cap}/\sqrt{3}$), then the current ($-I_A$+I_c) flows through capacitor C_{Cc}. Note that the opposite terminal voltages can also be generated by connecting the capacitors in opposite directions.

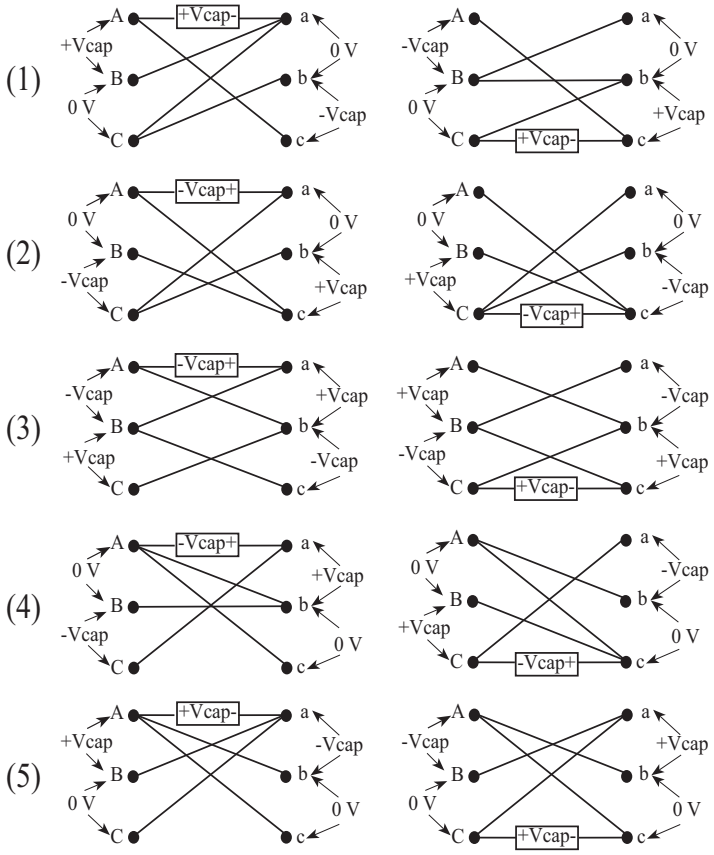


Figure 4.9: Example of switching-device combinations that involve capacitors C_{Aa} and C_{Cc}

If the current (I_A-I_c) has a positive value, then the switching-device combination on the top left column of Fig. 4.9 can be employed to charge the capacitor C_{Aa}, and the combination on the top right column can be employed to discharge the capacitor C_{Cc}. However, if the current (I_A-I_c) has a negative value, then capacitors C_{Aa} and C_{Cc} can be charged and discharged by using the same branch connections but connecting the capacitors in the opposite directions.

Knowing the capacitor error voltage ($\hat{v}$) and current (I) determined from the input- and output-side space vectors, the duty cycle d' of the opposite space vectors can be obtained from

$$d' = \frac{C}{T_s}\frac{|\hat{v}|}{|I|} \tag{4.3}$$

where C is the capacitance of the switch-cell capacitor, and T_s is the switching period of the converter. Although the maximum positive and the maximum negative error voltages, in general, have different magnitudes, either of them can be employed in Eq. (4.3).

4.2.3 Capacitor Voltage Stability

The ideal capacitor waveforms for the proposed capacitor voltage balancing scheme are illustrated in Fig. 4.10. During the first two subintervals, the capacitors having the maximum positive and negative error voltages are driven toward the average capacitor voltage; they then stay unchanged for the

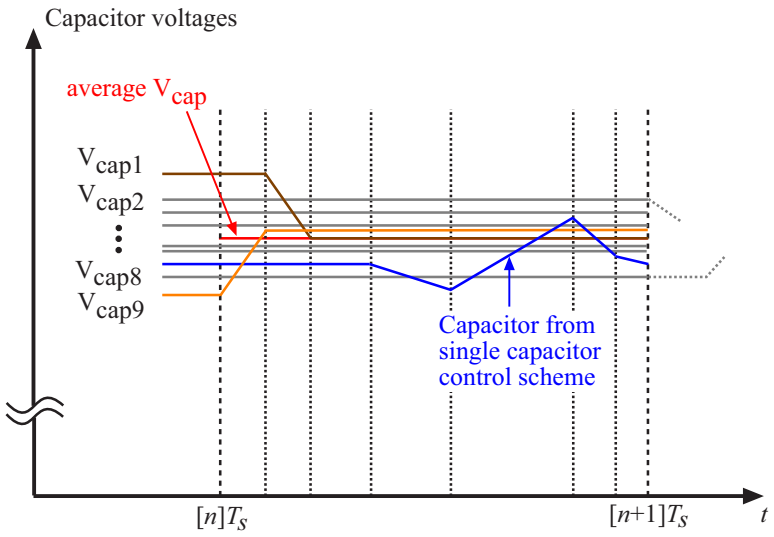


Figure 4.10: The ideal capacitor voltage waveforms for the proposed capacitor voltage-balancing scheme

remaining subintervals. The voltages of the remaining capacitors are unchanged throughout the switching period, even though the capacitors employed in the remaining subintervals of the switching period exhibit voltage ripples.

As described in the previous section, the control scheme can charge and discharge any two capacitors during each switching period. In addition, with the capacitor voltages defined in Eq. (4.2), there are always capacitors with positive and negative error voltages. The stability of the capacitor voltages can be proved by Lyapunov's approach [57]. A Lyapunov function is chosen to be

$$L = \sum_{j=1}^{9} \frac{1}{2} C \hat{v}_j^2 \geqslant 0 \tag{4.4}$$

where $\hat{v}_j$ is the error voltage of the capacitor j. With the same capacitance for all nine switch cells, Eq. (4.4) can be expressed as

$$L = \frac{1}{2} C [\hat{v}_n^2 + \hat{v}_p^2 + \cdots] \geqslant 0 \tag{4.5}$$

where $\hat{v}_p$ is the maximum positive error voltage and $\hat{v}_n$ is the maximum negative error voltage, sampled at the beginning of the switching period. The other terms are the error voltages of the remaining capacitors.

For the algorithm illustrated in Fig. 4.10, if the duty cycle d' is computed as in Eq. (4.3) using $\hat{v} = \hat{v}_p$, then the error voltage $\hat{v}_p$ is reduced to zero after one switching period, and the corresponding charge is transferred to the capacitor associated with $\hat{v}_n$. The change in L is then equal to

$$\begin{aligned}\Delta L &= \frac{1}{2}C[(\hat{v}_p + \hat{v}_n)^2 - \hat{v}_n^2] + \frac{1}{2}C[0 - \hat{v}_p^2] \\ &= C\hat{v}_p\hat{v}_n\end{aligned} \tag{4.6}$$

Because $\hat{v}_p$ is always positive and $\hat{v}_n$ is always negative, ΔL of Eq. (4.6) always has a negative value. Hence, Lyapunov's stability theorem confirms the stability of this control algorithm.

4.3 Experimental Results

The capacitor voltage balancing control associated with the single-capacitor control scheme was implemented to control the laboratory prototype. The sets of opposite space vectors were implemented in a lookup table. The detailed implementations of the control circuit are included in Chapter 6.

For comparison, Fig. 4.11 shows a capacitor voltage waveform and 30-Hz output PWM line-line voltage waveform generated without the capacitor voltage-balancing scheme. Figure 4.12 shows the same capacitor voltage and 30-Hz output PWM line-line voltage waveforms with the capacitor voltage

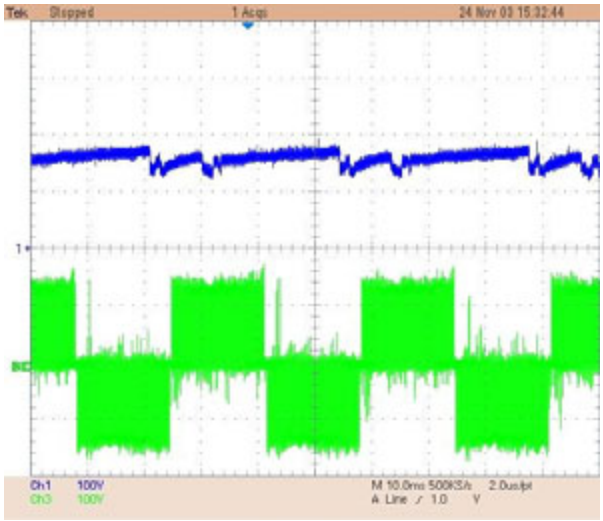


Figure 4.11: Waveforms of a capacitor voltage and an output PWM line-line voltage without capacitor voltage regulation

balancing scheme at the same operating point. Significant improvement in the capacitor voltage waveform can be observed when the capacitor voltage balancing control was applied with the single-capacitor control scheme to control the multilevel matrix converter. The effect of additional opposite space vectors can be noticed in the PWM line-line voltage waveform.

Figure 4.13 illustrates the output 30-Hz line-line voltage waveform after low-pass filtering, along with a capacitor voltage waveform. Figure 4.14 shows a comparison of two-capacitor voltage waveforms. It can be seen that the regulation of 10% is achieved.

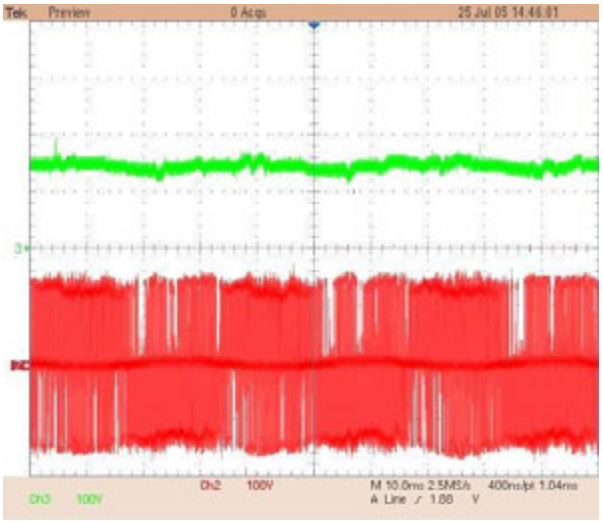


Figure 4.12: Waveforms of a capacitor voltage and an output PWM line-line voltage with capacitor voltage regulation

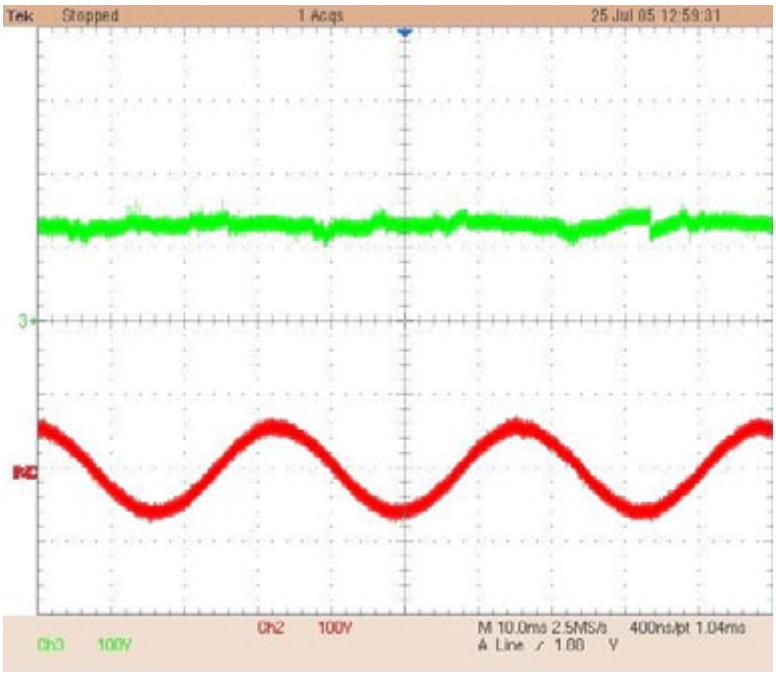


Figure 4.13: Waveforms of a capacitor voltage and a filtered output line-line voltage

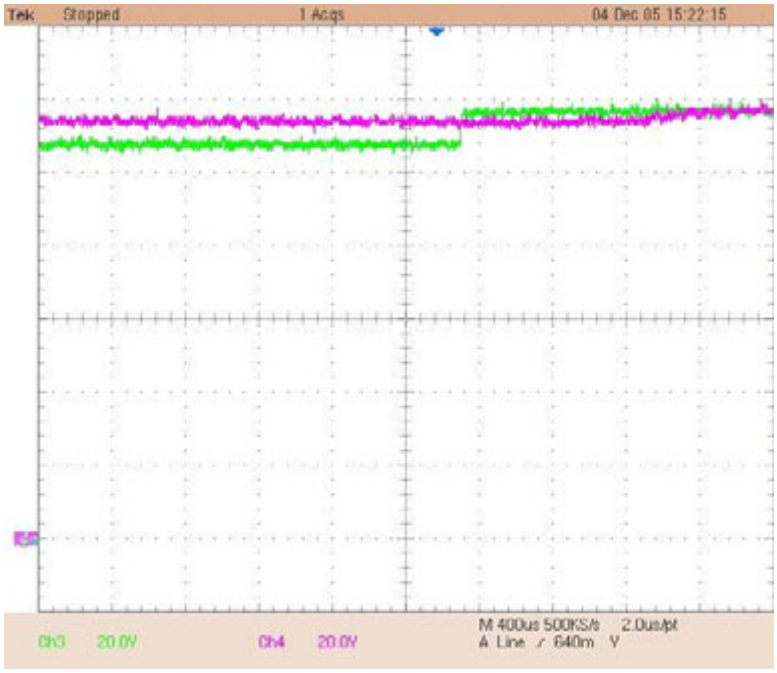


Figure 4.14: Waveforms of two capacitor voltages

Figure 4.15 shows the waveform of the average of all nine capacitor voltages, sampled at the switching frequency. The result indicates that the average capacitor voltage consists of the AC voltage at the input and output frequencies. A feedback loop for regulating the average capacitor voltage is necessary. Modeling and design of the control system for regulating the line currents and the average capacitor voltage are treated in [58].

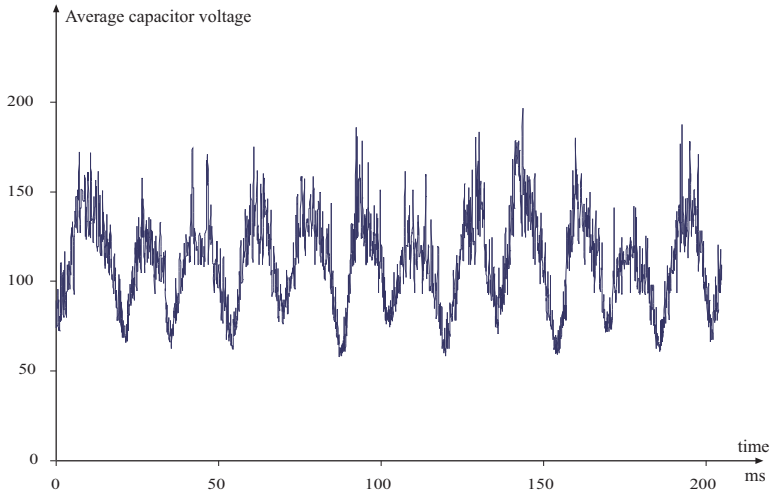


Figure 4.15: Waveform of the average of nine capacitor voltages

4.4 Summary of Key Points

The capacitor voltage balancing control was proposed to regulate the capacitor voltages in the multilevel matrix converter. The control scheme is based on the modification of the SVM using two additional space vectors having the same magnitude but opposite directions. The two opposite space vectors allow two additional capacitors to be charged and discharged in each switching period with minimum effect on synthesizing the average terminal voltages. The capacitor voltage balancing control is orthogonal to the terminal voltage synthesizing; hence, it can be employed with the single-capacitor control scheme. Two capacitors with the maximum positive and negative error voltages are regulated in each switching period. As a result, the error voltages of the remaining capacitors are bounded by the two extreme error voltages, which are driven toward zero by the control scheme. The stability of the control scheme is guaranteed by a Lyapanov's approach.

5 Three-Level Operation

In the multilevel matrix converter with the basic configuration, three-level switching can be achieved when the voltage magnitudes at both sides are sufficiently different. Two-level switching is employed at the converter side with the lower voltage magnitude, whereas three-level switching is employed at the other side. In the application where the voltage magnitude at one side of the converter is fixed (for example, the converter is connected to an infinite bus), the three-level switching allows the converter to be operated with reduced capacitor voltages.

Figure 5.1(a) summarizes the switch-cell capacitor voltage when the multilevel matrix converter interfaces between a wind generator and a utility grid. When the voltage magnitude at the generator side is greater than 0.577 of the voltage magnitude at the utility side, the converter operates with two-level switching at both sides. The capacitor voltage is fixed at slightly greater than the utility's voltage magnitude. If the voltage magnitude at the generator side drops below 0.577 of the voltage magnitude on the utility side, then the converter operates with the three-level switching mode: two-level switching at the generator side and three-level switching at the utility side. This allows the converter to be operated at

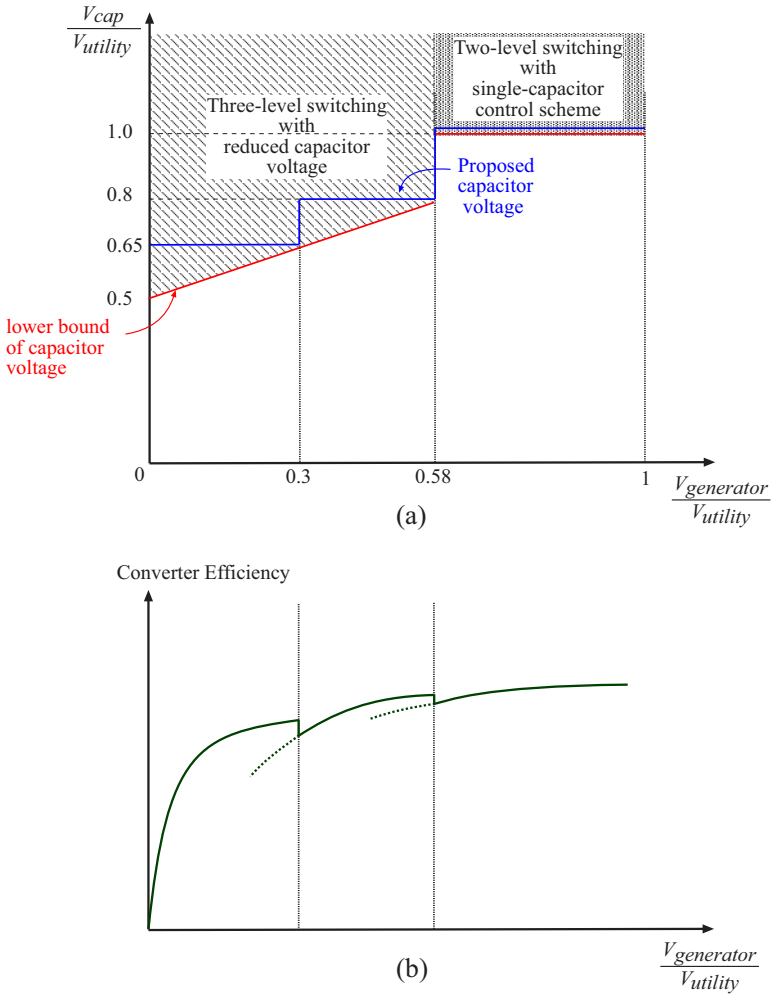


Figure 5.1: (a) Proposed capacitor voltage of the multilevel matrix converter in the wind turbine system, (b) prospective converter efficiency

lower capacitor voltages. As the capacitor voltage decreases, the switching loss of the converter is also reduced. Consequently, the efficiency of the converter is expected to be improved with the three-level switching (Fig. 5.1[b]).

5.1 Space-Vector Modulation

To perform three-level switching in the basic configuration of the multilevel matrix converter, the space-vector control involves the 18 non-zero space vectors attainable from the converter. These space vectors form the outer ring of the *dq* diagram as shown in Fig. 5.2. The SVM for three-level switching further divides each 60° sector into three cases:

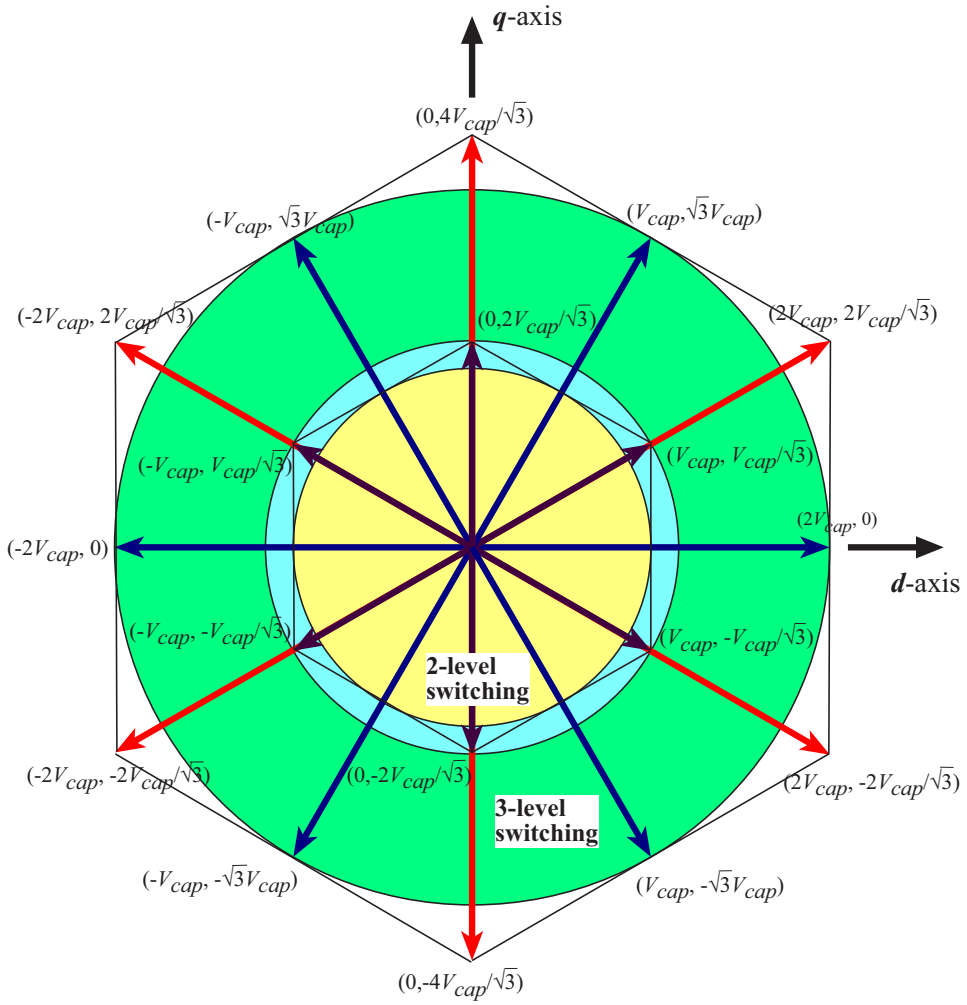


Figure 5.2: Operating regions of the multilevel matrix converter in *dq* diagram

Case 1: Modulation between two space vectors with magnitude $2V_{cap}/\sqrt{3}$ and one space vector with magnitude $2V_{cap}$. When the desired reference space vector lies in the shaded area of a 60° sector of the space-vector diagram (Fig. 5.3), three space vectors adjacent to the reference space vector V_{ref} can be assumed to be the space vectors V_{L1}, V_{L2}, and V_M. The space vectors V_{L1} and V_{L2} are two adjacent space vectors with magnitude $2V_{cap}/\sqrt{3}$, and the space vector V_M is a space vector with magnitude $2V_{cap}$.

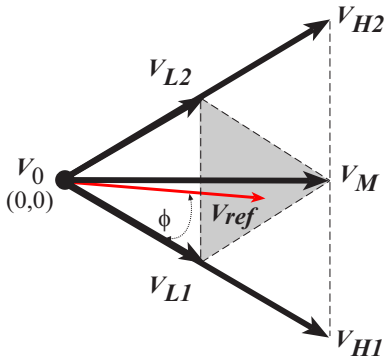


Figure 5.3: SVM for three-level switching, Case 1

The condition for modulation in this case is

$$\frac{V_{cap}}{\sin(60^\circ + \phi)} \leq \|\boldsymbol{V_{ref}}\| \leq \frac{V_{cap}}{\sin(30^\circ + |30^\circ - \phi|)} \qquad \text{where} \qquad 0 \leq \phi \leq 60^\circ \tag{5.1}$$

From Eqs. (2.6) and (2.7), the desired reference vector can be expressed as

$$\boldsymbol{V_{ref}} = d_{L1}\boldsymbol{V_{L1}} + d_{L2}\boldsymbol{V_{L2}} + d_M\boldsymbol{V_M} \qquad \text{and} \qquad d_{L1} + d_{L2} + d_M = 1 \tag{5.2}$$

The solution of the duty cycles from the vector diagram in Fig. 5.3 using Eq. (5.2) and further simplifications yields the following:

$$\begin{aligned} d_M &= -1 + \frac{\|\boldsymbol{V_{ref}}\|}{V_{cap}} \sin(60^\circ + \phi) \\ &= -1 + M \sin(60^\circ + \phi) \qquad \text{where} \quad M = \frac{\|\boldsymbol{V_{ref}}\|}{V_{cap}} \\ d_{L1} &= 1 - \frac{\|\boldsymbol{V_{ref}}\|}{V_{cap}} \sin(\phi) \\ &= 1 - M \sin(\phi) \\ d_{L2} &= 1 - \frac{\|\boldsymbol{V_{ref}}\|}{V_{cap}} \sin(60^\circ - \phi) \\ &= 1 - M \sin(60^\circ - \phi) \end{aligned} \tag{5.3}$$

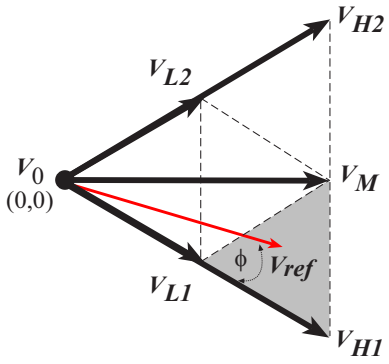


Figure 5.4: SVM for three-level switching, Case 2

Case 2: Modulation among a space vector with magnitude $2V_{cap}/\sqrt{3}$, a space vector with magnitude $2V_{cap}$, and a space vector with magnitude $4V_{cap}/\sqrt{3}$ when the modulation angle ϕ is less than 30°. Three space vectors adjacent to the reference space vector V_{ref} are the space vectors V_{L1}, V_{H1}, and V_M (Fig. 5.4). V_{L1} is a space vector with magnitude $2V_{cap}/\sqrt{3}$. V_M is a space vector with magnitude $2V_{cap}$. V_{H1} is a space vector with magnitude $4V_{cap}/\sqrt{3}$. The desired reference vector V_{ref} can be expressed as

$$\begin{aligned} \boldsymbol{V_{ref}} &= d_{L1}\boldsymbol{V_{L1}} + d_M\boldsymbol{V_{V_M}} + d_{H1}\boldsymbol{V_{H1}} \\ \text{and} \qquad d_{L1} + d_M + d_{H1} &= 1 \end{aligned} \tag{5.4}$$

The solution of the duty cycles from the vector diagram in Fig. 5.4 using Eq. (5.4) and further simplifications yields:

$$\begin{aligned} d_M &= \frac{\|\boldsymbol{V_{ref}}\|}{V_{cap}} \sin(\phi) \\ &= M\sin(\phi) \qquad \text{where} \quad M = \frac{\|\boldsymbol{V_{ref}}\|}{V_{cap}} \\ d_{L1} &= 2 - \frac{\|\boldsymbol{V_{ref}}\|}{V_{cap}} \sin(60^\circ + \phi) \\ &= 2 - M\sin(60^\circ + \phi) \\ d_{H1} &= -1 + \frac{\|\boldsymbol{V_{ref}}\|}{V_{cap}} \sin(60^\circ - \phi) \\ &= -1 + M\sin(60^\circ - \phi) \end{aligned} \tag{5.5}$$

Case 3: Modulation among a space vector with magnitude $2V_{cap}/\sqrt{3}$, a space vector with magnitude $2V_{cap}$, and a space vector with magnitude $4V_{cap}/\sqrt{3}$ when the modulation angle ϕ is greater than 30°. Three space vectors adjacent to the reference space vector V_{ref} are the space vectors V_{L2}, V_{H2}, and V_M (Fig. 5.5). V_{L2} is a space vector with magnitude $2V_{cap}/\sqrt{3}$. V_M is a space vector with magnitude $2V_{cap}$. V_{H2} is a space vector with magnitude $4V_{cap}/\sqrt{3}$. The desired reference vector V_{ref} can be expressed as follows:

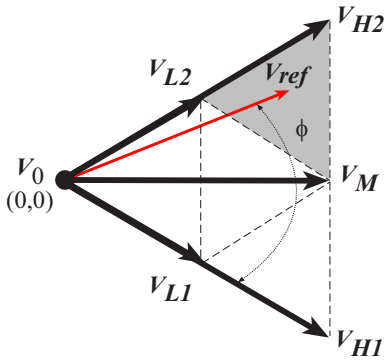


Figure 5.5: SVM for three-level switching, Case 3

$$\begin{aligned} \boldsymbol{V_{ref}} &= d_{L2}\boldsymbol{V_{L2}} + d_M\boldsymbol{V_M} + d_{H2}\boldsymbol{V_{H2}} \\ \text{and} \qquad & d_{L2} + d_M + d_{H2} = 1 \end{aligned} \tag{5.6}$$

The modulation in Case 3 is symmetrical to the modulation in Case 2; hence, ϕ in Eq. (5.5) can be replaced by (60-ϕ), which yields

$$\begin{aligned} d_M &= \frac{\|\boldsymbol{V_{ref}}\|}{V_{cap}} \sin(60^\circ - \phi) \\ &= M \sin(60^\circ - \phi) \qquad \text{where} \quad M = \frac{\|\boldsymbol{V_{ref}}\|}{V_{cap}} \\ d_{L2} &= 2 - \frac{\|\boldsymbol{V_{ref}}\|}{V_{cap}} \sin(60^\circ + \phi) \\ &= 2 - M \sin(60^\circ + \phi) \\ d_{H2} &= -1 + \frac{\|\boldsymbol{V_{ref}}\|}{V_{cap}} \sin(\phi) \\ &= -1 + M \sin(\phi) \end{aligned} \tag{5.7}$$

The conditions for modulations in Case 2 and Case 3 are as follows:

$$\begin{aligned} \frac{V_{cap}}{\sin(30^\circ + |30^\circ - \phi|)} \le \|\boldsymbol{V_{ref}}\| \le \frac{2V_{cap}}{\sin(60^\circ + \phi)} \\ \text{where} \qquad 0 \le \phi \le 60^\circ \end{aligned} \tag{5.8}$$

When the space-vector control commands the multilevel matrix converter using the space vectors with magnitudes greater than $2V_{cap}/\sqrt{3}$, the corresponding line-line voltages of the converter have magnitudes of twice the capacitor voltage. The line-line voltage with a magnitude of twice the capacitor voltage is generated from two series-connected capacitors, as described in Section 2.2.2. To avoid applying exceeding voltages across open-circuited switch cells, it is required that the voltage potentials of all phases at the other side must be equal to the voltage potential at the mid-point of the two series-connected capacitors; hence, all line-line voltages of this side have zero magnitude. In PWM, this constraint implies

that when the multilevel matrix converter operates with three-level switching on one side, two-level switching must be employed at the other side. Also the pattern of space vectors utilized in each switching period must be correctly coordinated.

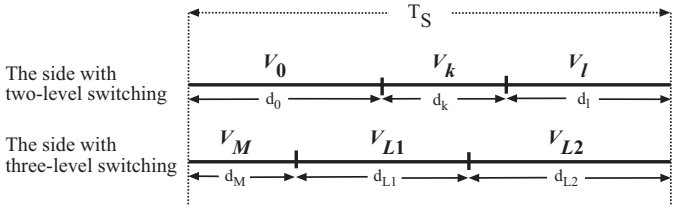
5.2 Limitations of the Three-Level Operation

With the constraint for avoiding excess voltages across open-circuited switching cell, when the multilevel matrix converter generates terminal voltages with three-level switching at one side, two-level switching must be applied to generate terminal voltages at the other side. Furthermore, the space-vector control must synchronize the space vector with a magnitude greater than $2V_{cap}/\sqrt{3}$ from the three-level switching with the null-state space vector from the two-level switching.

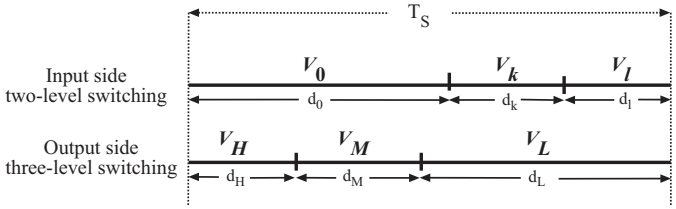
Assume that the converter generates output-side voltages with three-level switching and input-side voltages with two-level switching. A possible space-vector pattern in each switching period is illustrated in Fig. 5.6. The duty cycle of the null-state space vector, d_0, at the input side must be greater than the total duty cycles of the space vectors with magnitudes greater than $2V_{cap}/\sqrt{3}$ at the output side (the duty cycle of the space vector with magnitude $2V_{cap}$ for the modulation in Case 1 or the sum of the duty cycle of the space vector with magnitude $2V_{cap}$ and the duty cycle of the space vector with magnitude $4V_{cap}/\sqrt{3}$ for the modulation in Case 2 and Case 3). Using Eqs. (5.5) and (5.7), the sum of the duty cycle of the space vector with magnitude $2V_{cap}$ and the duty cycle of the space vector with magnitude $4V_{cap}/\sqrt{3}$ for the modulation in Case 2 and Case 3 can be expressed as:

$$d_M + d_H = -1 + \frac{\|\boldsymbol{V_{ref}}\|}{V_{cap}} \sin(60^\circ + \phi) \tag{5.9}$$

Equation (5.9) is similar to the expression for the duty cycle of the space vector with magnitude $2V_{cap}$ from the modulation in Case 1, in Eq. (5.2). Therefore, all three cases of the modulation have the same limitation either from the condition of $d_0 \geq d_M$ or from the condition of $d_0 \geq d_M + d_H$. The constraint then can be expressed in terms of input- or output-side voltage magnitudes and capacitor voltage as



(a) Modulation pattern for Case 1



(b) Modulation pattern for Case 2 and Case 3

Figure 5.6: Modulation patterns in one switching period for three-level switching

$$1 - \frac{\|\boldsymbol{V_{ref-Input}}\|}{V_{cap}} \sin(60^\circ + \phi_{Input}) \geq -1 + \frac{\|\boldsymbol{V_{ref-Output}}\|}{V_{cap}} \sin(60^\circ + \phi_{Output})$$
$$V_{cap} \geq \frac{1}{2}(\|\boldsymbol{V_{ref-Output}}\| \sin(60^\circ + \phi_{Output}) + \|\boldsymbol{V_{ref-Input}}\| \sin(60^\circ + \phi_{Input})) \tag{5.10}$$

The condition in Eq. (5.10) also depends on the modulation angles at both sides, which are time-variable parameters and independent from each other. To guarantee that this condition of the capacitor voltage is satisfied throughout the input and output line periods, the extreme condition of the right-hand side of Eq. (5.10) is considered (when both modulation angles are equal to 30°). Then the condition can be simplified as

$$V_{cap} \geq \frac{1}{2}(V_{Output} + V_{Input}) \tag{5.11}$$

where V_{Output} and V_{Input} are the line-line voltage magnitudes at the output and input sides respectively.

The condition from Eq. (5.11) sets a limitation on the minimum capacitor voltage so that three-level switching can be achieved. To cover the range of operation remaining from the single-capacitor control scheme in the two-level switching (the range where $V_{Input} < V_{Output}/\sqrt{3}$), the capacitor voltages can be reduced to 80% of the output line-line voltage magnitude. The capacitor voltages can be further reduced as the input-side voltage magnitude decreases (Fig. 5.1).

5.3 Experimental Validation

Laboratory experiments were undertaken to illustrate the capability of the multilevel matrix converter in the three-level switching mode. The converter converted 60-Hz input voltage into 30-Hz output voltage with the following modulation indices:

$$M_{in} = \frac{\|\boldsymbol{V_{ref-in}}\|}{V_{cap}} = 0.4$$
$$M_{out} = \frac{\|\boldsymbol{V_{ref-out}}\|}{V_{cap}} = 1.5 \tag{5.12}$$

The converter was operated without any capacitor voltage regulation scheme; hence, 330-μF electrolytic capacitors were added into the H-bridge switch cells to make the converter stable. More details of the hardware implementations are described in Chapter 6.

Figure 5.7 shows the input and output PWM line-line voltages at the switch network. The input side voltage waveform, Trace 1, is operated with two-level switching, while the output side voltage waveform, Trace 4, is operated with three-level switching. Figure 5.8 shows the input and output line-line voltage waveforms in one switching period.

Figure 5.9 shows a 30-Hz output PWM line-line voltage waveform alone with the corresponding voltage waveform after being filtered by the *L-C* low-pass filter circuit. Figure 5.10 shows the variation of a capacitor voltage along the output line-line voltage. The variation in the capacitor voltage consists of both the input 60-Hz and the output 30-Hz AC voltages.

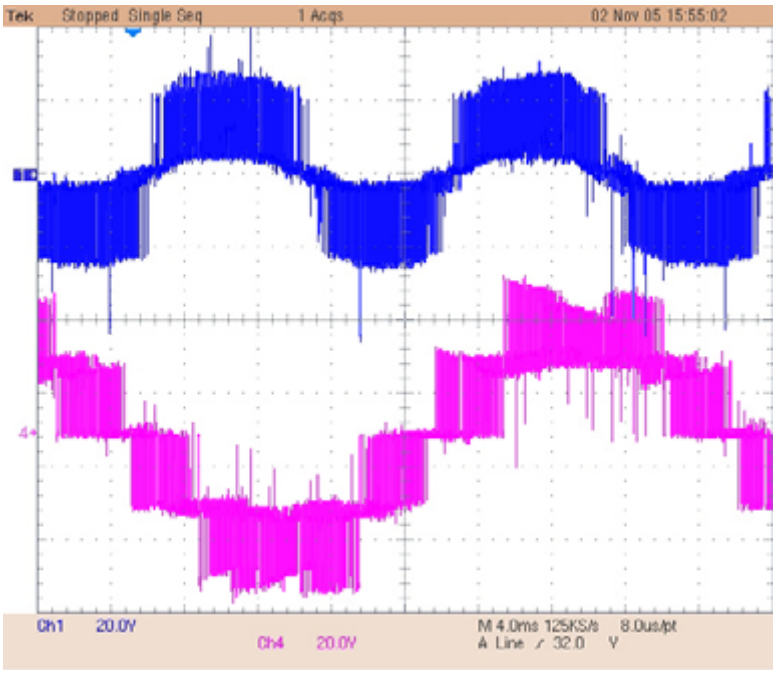


Figure 5.7: Input and output PWM line-line voltage waveforms
Trace 1: input line-line voltage with two-level switching
Trace 4: output line-line voltage with three-level switching

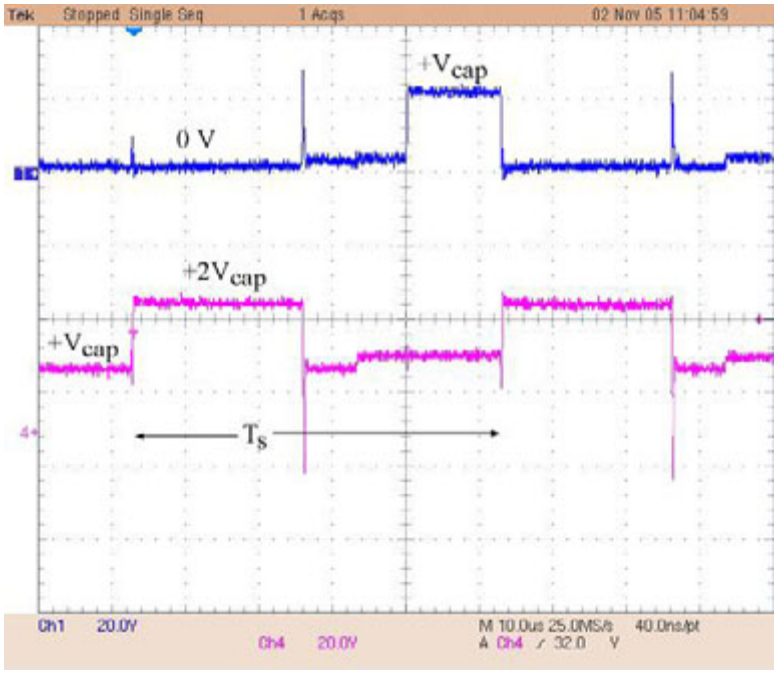


Figure 5.8: Input and output line-line voltage waveforms in one switching period
Trace 1: input line-line voltage with two-level switching
Trace 4: output line-line voltage with three-level switching

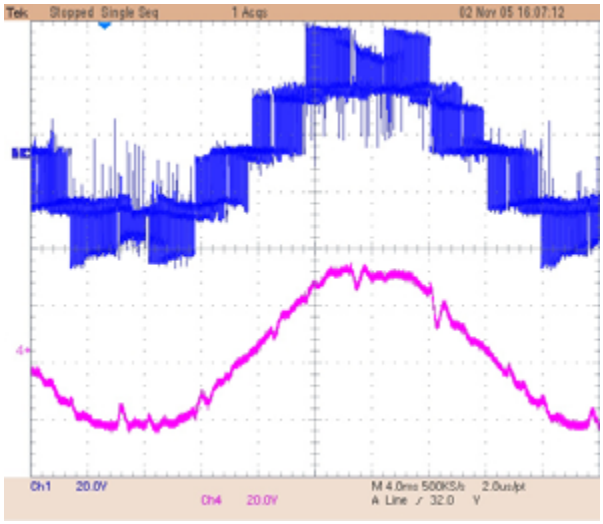


Figure 5.9: Waveforms of output PWM ine-line voltage and the filtered output line-line voltage

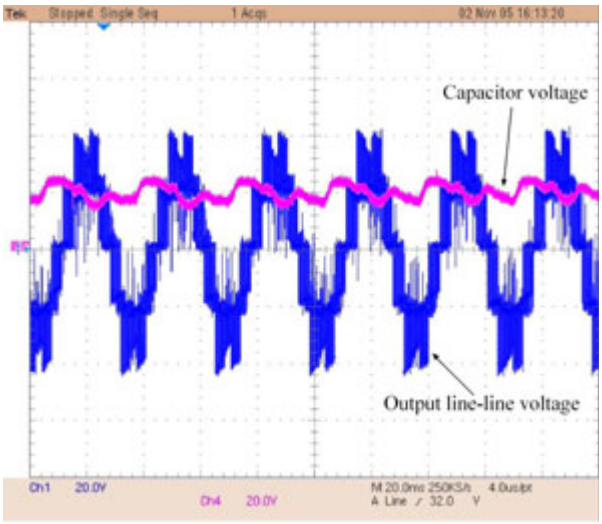
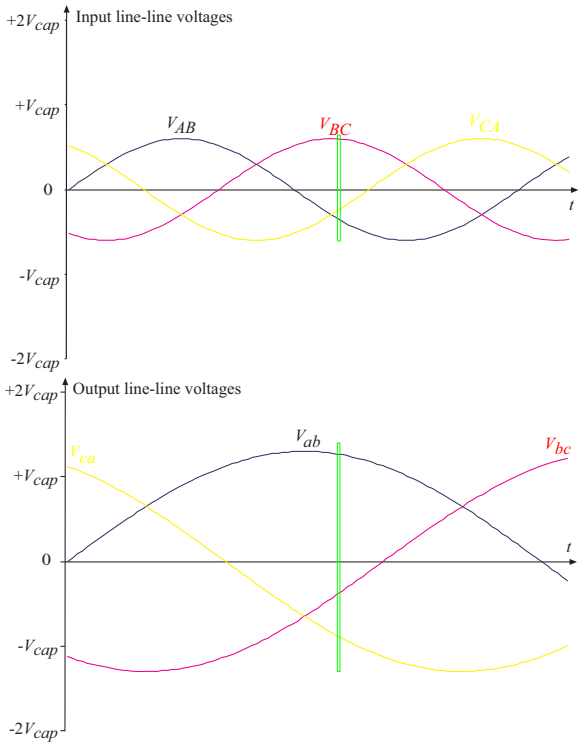


Figure 5.10: Output line-line voltage and capacitor voltage waveforms

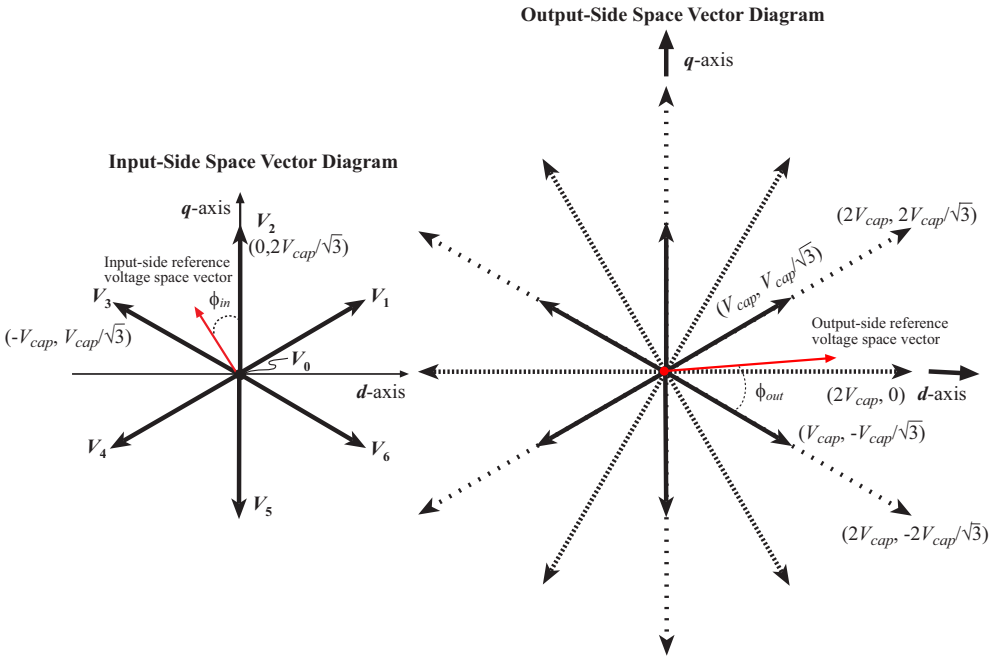
5.4 A Possible Control Scheme for Three-Level Operation

The single-capacitor control scheme, as described in Section 3.3, can be extended to the case when two switch-cell capacitors are employed during a switching period. To generate line-line voltages corresponding to the space vectors with magnitude $2V_{cap}$, the multilevel matrix converter can involve two switch-cell capacitors simultaneously in the switching-device combinations. As a result, when the multilevel matrix converter operates with three-level modulation in Case 1 of Section 5.1 (modulation among two space vectors with magnitude $2V_{cap}/\sqrt{3}$ and one space vector with magnitude $2V_{cap}$), the converter can involve two capacitors for synthesizing terminal voltages in each switching period. It is possible that, in each switching period, one additional subinterval is generated having a converter configuration to balance the charge in one capacitor. If the converter is operated at a steady state, then the charge balance on the other capacitor can also be achieved.

Consider an example in which the multilevel matrix converter generates the input and output voltages, as shown in Fig. 5.11(a). At the point marked by the vertical bars, the positions of the input-side reference space vector and the output-side reference space vector in the *dq* coordinates are illustrated in Fig. 5.11(b). The input side of the converter is modulated with two-level switching, whereas the output side is modulated with three-level switching. The duty cycle for each space vector of the input side can be computed using Eq. (3.3). The duty cycle for each space vector of the output side can be computed using Eq. (5.7). The pattern of the space vectors according to Fig. 5.6(a) is shown in Fig. 5.12, along with the sets of allowed capacitors for each subinterval in the given switching period. The corresponding line-line voltages at both input and output sides in the switching period are shown in Fig. 5.13.



(a) In time domain



(b) In *dq* coordinate

Figure 5.11: An example of SVM in three-level operation: (a) in time domain, (b) in *dq* coordinate

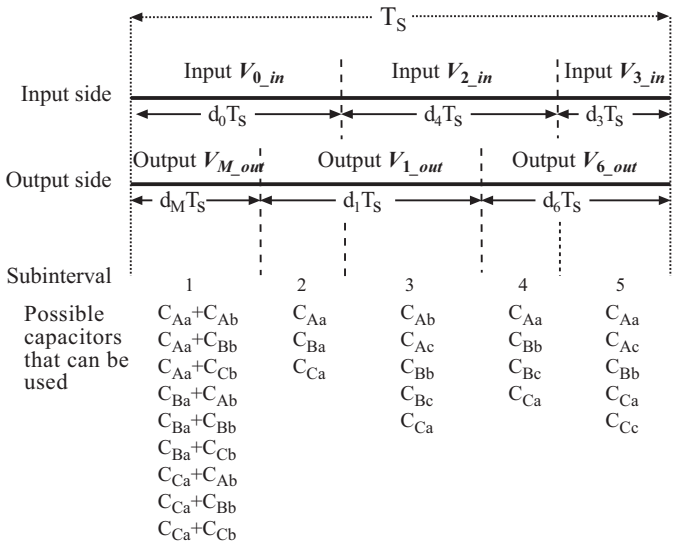


Figure 5.12: Pattern of input and output space vectors for the example with sets of capacitors that can be used in each subinterval

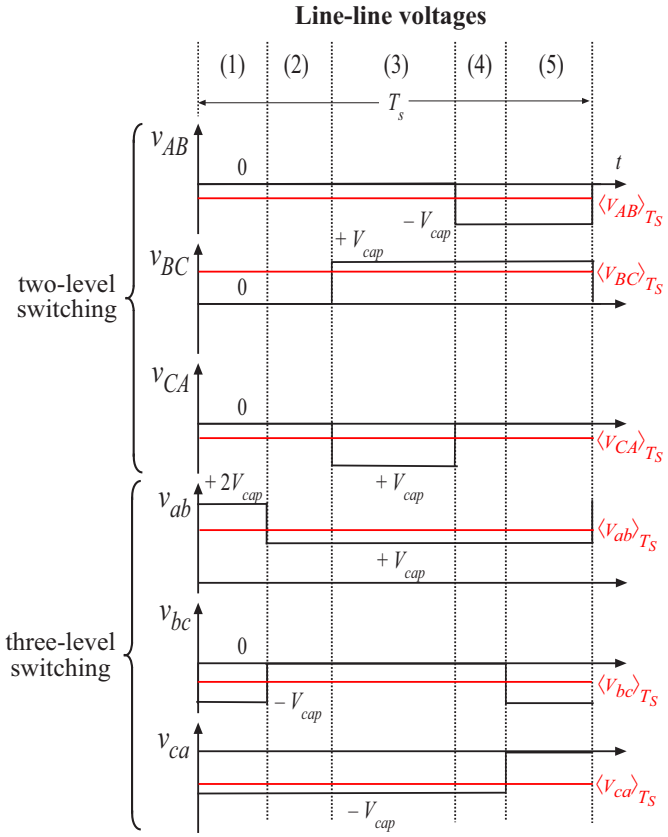


Figure 5.13: The corresponding PWM line-line voltages in the given switching period

In the first subinterval, two switch-cell capacitors must be employed simultaneously. Possible combinations of two capacitors that can be employed in this subinterval are combinations of the switch-cell capacitors connected to the output phase *a* (C_{Aa}, C_{Ba}, and C_{Ca}) and the switch-cell capacitors connected to the output phase *b* (C_{Ab}, C_{Bb}, and C_{Cb}). For any switching-device combination having only two switch-cell capacitors, the output phase current ($-I_a$) flows through the capacitor connected to the output phase *a*. At the same time, the output phase current (I_b) flows through the capacitors connected to the output phase *b*.

Notice that the capacitor C_{Ca}, from the switch cell that is connected between the input phase *C* and the output phase *a*, can be employed throughout the switching period. This capacitor can also be determined with the single-capacitor control scheme with the case of $d_{0\_out} = 0 < d_{0\_in}$. The capacitor C_{Bb} can also be employed in four of the five subintervals, except in the subinterval having a combination of the input-side null-state space vector and the output-side space vector $\boldsymbol{V}_{\mathbf{1\_out}}$. In case the capacitor C_{Bb} is employed with the capacitor C_{Ca} in the first subinterval, it is possible to generate one additional subinterval from the third subinterval (or from the forth or the fifth subinterval) having a switching-device combination to balance the charge in the capacitor C_{Bb}. Consequently, in a given switching period, the converter employs only the capacitors C_{Ca} and C_{Bb}. At the steady-state operation, with the charge balance on the capacitor C_{Bb}, the charge balance on the capacitor C_{Ca} can also be achieved.

Assume that the power factor at the output side is greater than 0.5; hence, for this example, the output phase I_b flows into the converter. As a result, the capacitor C_{Bb} is discharged with the output phase current I_b in the first subinterval. If the power factor at the input side is also greater than 0.5, then the input phase current I_B also flows into the converter. An additional subinterval with a switching-device combination having the capacitor C_{Bb} charged by the input current I_B can be employed. The duty cycle of the additional subinterval can be computed from

$$d_3' = \frac{|I_b|}{|I_B|} d_m \tag{5.13}$$

Each switching period is now divided into six subintervals. Switching-device combinations for all six subintervals are illustrated in Fig. 5.14. In the third subinterval, the converter moves the additional charge from the capacitor C_{Bb} to the capacitor C_{Ca}. In the third and the forth switching-device combinations, the converter configurations provide identical terminal voltages. The line-line voltage waveforms in the given switching period are not affected by the additional subinterval.

This switching-device combination serves to balance charge on the capacitor and is dependent on the power factors at both sides; however, there exists a valid switching-device combination for any given input- and output-side power factors. For instance, if the power factors at both sides are less than 0.5, then the switching-device combinations for the first and the third subintervals that involve capacitor $C_{Ab,}$ instead of capacitor $C_{Bb,}$ can be employed.

The concept of having an additional subinterval for each switching period to balance charge of a capacitor is feasible when the SVM is in Case 1 where the converter involves only two capacitors. However, when the SVM is in Case 2 or 3, the converter involves five capacitors simultaneously; the concept then becomes more complex. The operations of the multilevel matrix converter in these cases remain unsolved problems.

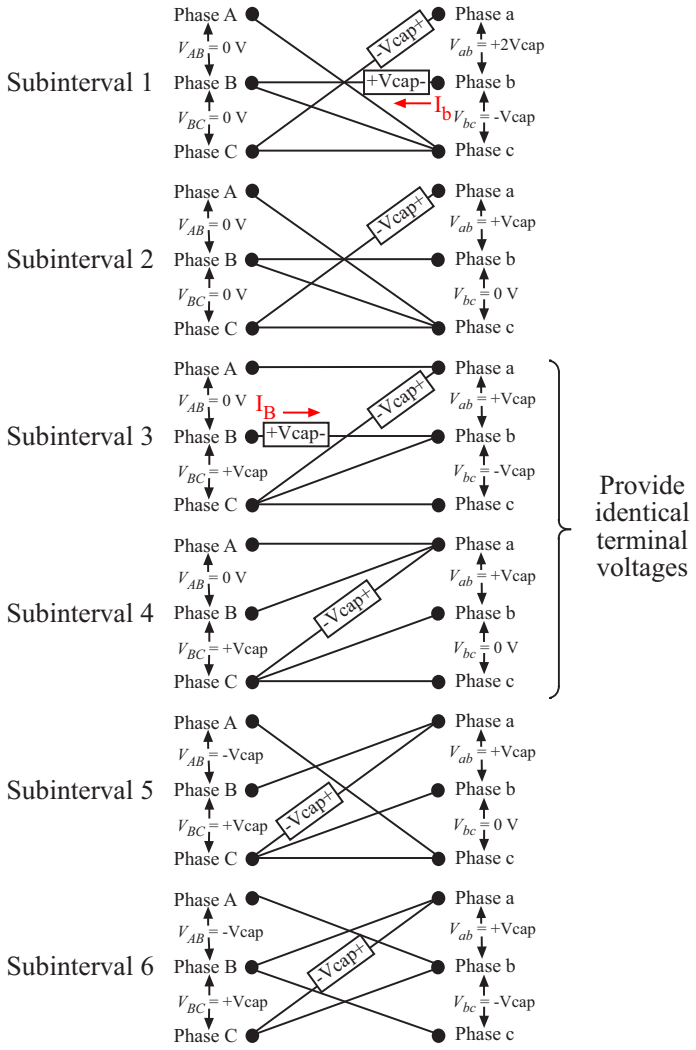


Figure 5.14: Example of switching-device combinations to balance charge of the capacitor C_{Bb}

5.5 Summary of Key Points

The three-level operation allows the multilevel matrix converter to generate terminal voltages with the maximum magnitude of twice the capacitor voltage. Compared to the two-level operation, the three-level operation allows the multilevel matrix converter to generate the same terminal voltages with lower capacitor voltage. Consequently, the switching loss of the converter is reduced and the converter efficiency is increased. With the constraint to avoid excess voltage across open-circuited switch cells, the three-level operation of the converter can be achieved only when the voltage magnitudes at both sides of the converter are significantly different. The three-level switching is applied at the side having higher voltage magnitude, whereas the two-level switching is applied at the other side. The SVM for three-level switching involves 18 non-zero space vectors. Furthermore, the space-vector pattern in each switching period must be carefully coordinated. The operations of the multilevel matrix converter in the three-level switching were proved feasible by the experimental validations.

6 Hardware Implementation

The first working laboratory prototype of the multilevel matrix converter with the basic configuration was constructed to experimentally prove the operations of the converter and to verify the proposed control schemes. The experimental results demonstrate the feasibility of controlling a complex converter containing many modules using a central controller; synthesizing terminal voltages and regulating capacitors in nine modules can be achieved using a digital control chip. The complexity of the control schemes is overcome with software programming with a lookup table.

A laboratory prototype of the multilevel matrix converter with the basic configuration was constructed to verify the proposed control algorithms. Figure 6.1 shows a block diagram of the laboratory prototype of the multilevel matrix converter. The power stage of the prototype is rated at 280 V and 50 A at both input and output terminals, which has the capability of operation at approximately 24 kVA. Each H-bridge switch cell includes an internal DC bus with the voltage of 400 V. The converter is operated at the switching frequency of 20 kHz. The digital control system was implemented using a Xilinx Virtex-II Pro XC2VP4, consisting of a PowerPC 405 microprocessor and FPGAs with flash memory chips as a lookup table.

In the experimental setup, the converter was interfaced between a three-phase variac, which provides variable 0- to 420-V 60-Hz three-phase voltage, and a three-phase resistive load. The output-side reference space vector can be programmed arbitrarily: programmable output frequency and magnitude. The laboratory setup is shown in Fig. 6.2. Five-ohm resistors were added in series with the three-phase voltage source to limit currents in case fault conditions occur. AC capacitors were also added at the input and the output terminals to filter the AC voltages. The main reason for adding these capacitors was to improve the sensing signal qualities.

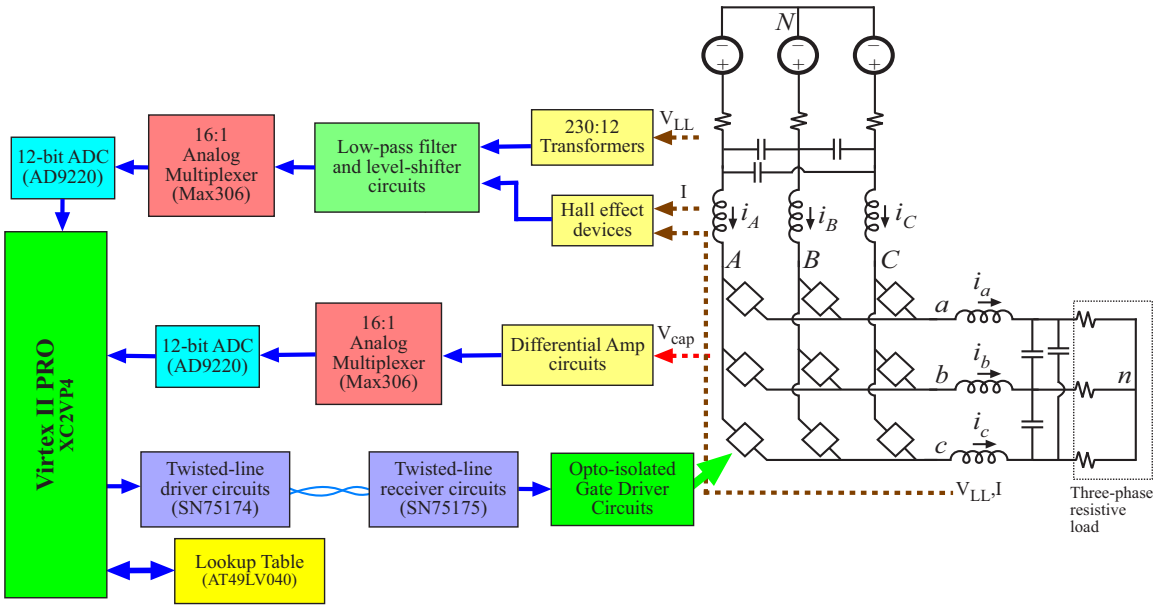


Figure 6.1: Block diagram for the laboratory prototype of multilevel matrix converter

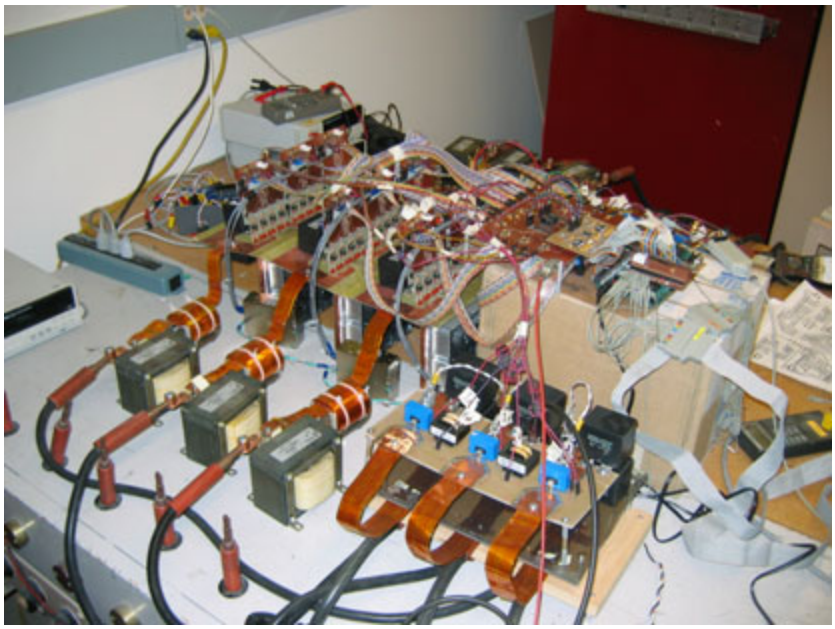


Figure 6.2: Photograph of the laboratory prototype

6.1 Power Stage

6.1.1 Switch-Cell Modules

For the switch matrix in the power stage, three H-bridge switch cells were built in each printed circuit board. The copper-clad printed circuit board (PCB) was constructed from 10-mil copper, which can conduct approximately 50 A_{rms} per inch of trace width. A photograph of the switch modules is included in Figs. 6.3, 6.4, and 6.5.

In each H-bridge switch cell, 600-V, 60-A, *n*-channel IGBTs with anti-parallel "hyper fast" diodes (Intersil part# HGTG30N60A4D) [59] are employed as switching devices. The power semiconductor devices are in TO-247 packages; they are mounted to heat sinks through copper boards as heat spreaders at the bottom side of PCBs.

The capacitors employed as the DC bus in each H-bridge switch cell are two of the 4.7-μF polypropylene capacitors (Cornell Dubilier part# SCD475K601A3Z25) [60] connected in parallel. Each capacitor has rated voltage of 600 V and current of 30 A. The capacitors were mounted at the top and bottom sides of printed circuit boards.

Each H-bridge switch cell has a separate gate-drive circuit. The gate-drive circuits are optically isolated from the digital control circuit. Power for the gate-drive circuits are supplied through the forward DC-DC converters.

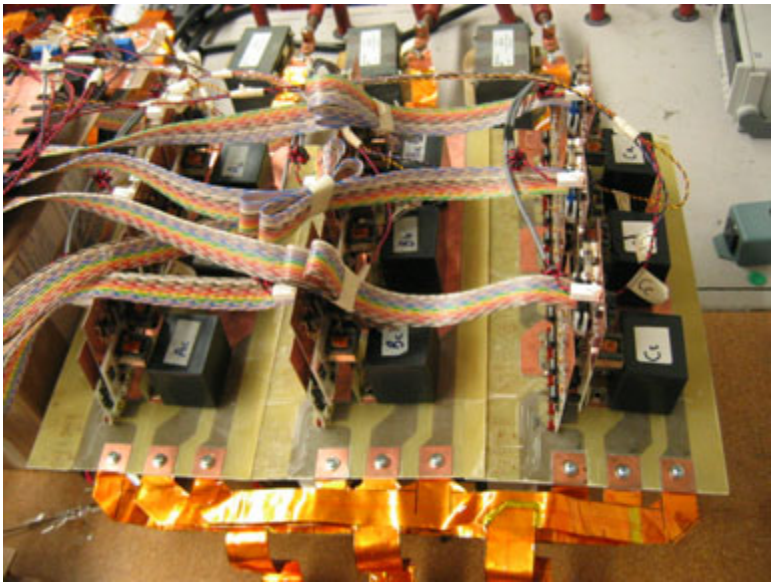


Figure 6.3: Power stage consisting of three printed circuit boards; each PCB contains three H-bridge switch cells

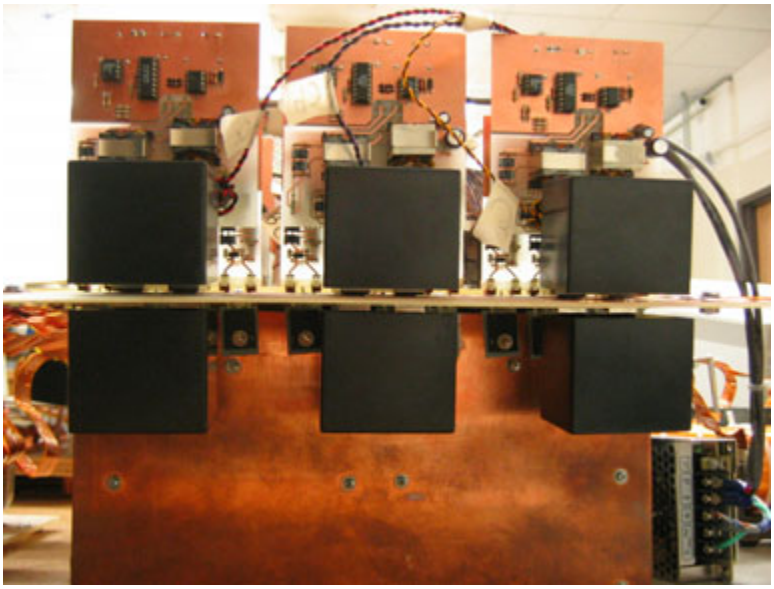


Figure 6.4: Three H-bridge switch cells per PCB

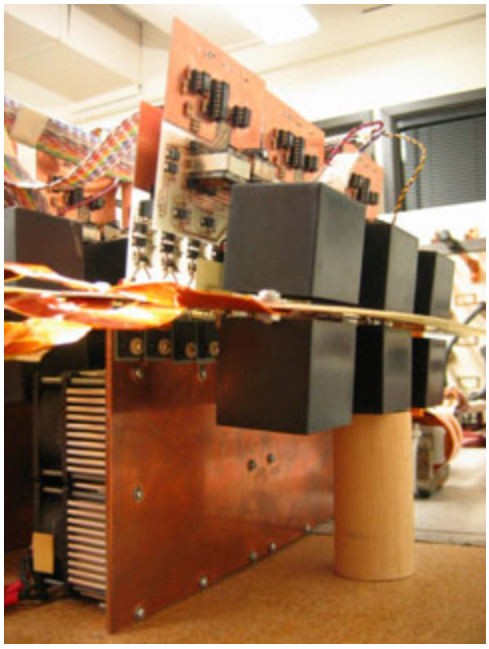


Figure 6.5: Side view of a PCB, showing the IGBTs mounted to the heat sinks through the copper heat spreader

6.1.2 Filter Inductors

Originally, the laboratory prototype of the multilevel matrix converter was designed to operate at the switching frequency of 50 kHz. Hence, the 0.2-mH inductors were employed as filter elements providing 20 % ripple at the rated rms current. As a result of the limit capability of the digital control circuit, the switching frequency of the converter was reduced to 20 kHz. The 1-mH inductors, therefore, were added and can provide 10% ripple at the rated rms currents.

The photograph of an inductor set is shown in Fig. 6.6. The 1-mH inductors are Hammond manufacturing part# 195C50, which have rated current of 50 A. The 0.2-mH inductors have the following specifications:

- Inductance: 0.2 mH
- Saturation current: 50 A
- Winding: 26 turns of 8-ounce copper foil
- Air gap: 1.64 mm
- Core material: iron-based METGLAS® amorphous cores, B_{max} = 1.4 Tesla
- Core size: AMCC63
- Core cross-sectional area: 3.9 **[Trial mode]**
- Dimensions: H = 10.2 cm, W = 5.2 cm, L = 3.0 cm

Figure 6.6: Filter inductors at one converter terminal

6.2 Digital Control System

The digital control system for the laboratory prototype was implemented using Xilinx Virtex II Pro XC2VP4 consisting of a PowerPC 405 microprocessor, FPGAs [61], and Flash memory chips. A photograph of the Virtex II Pro XC2VP4 development board is included in Fig. 6.7.

Figure 6.7: Virtex-II Pro XC2VP4 development board

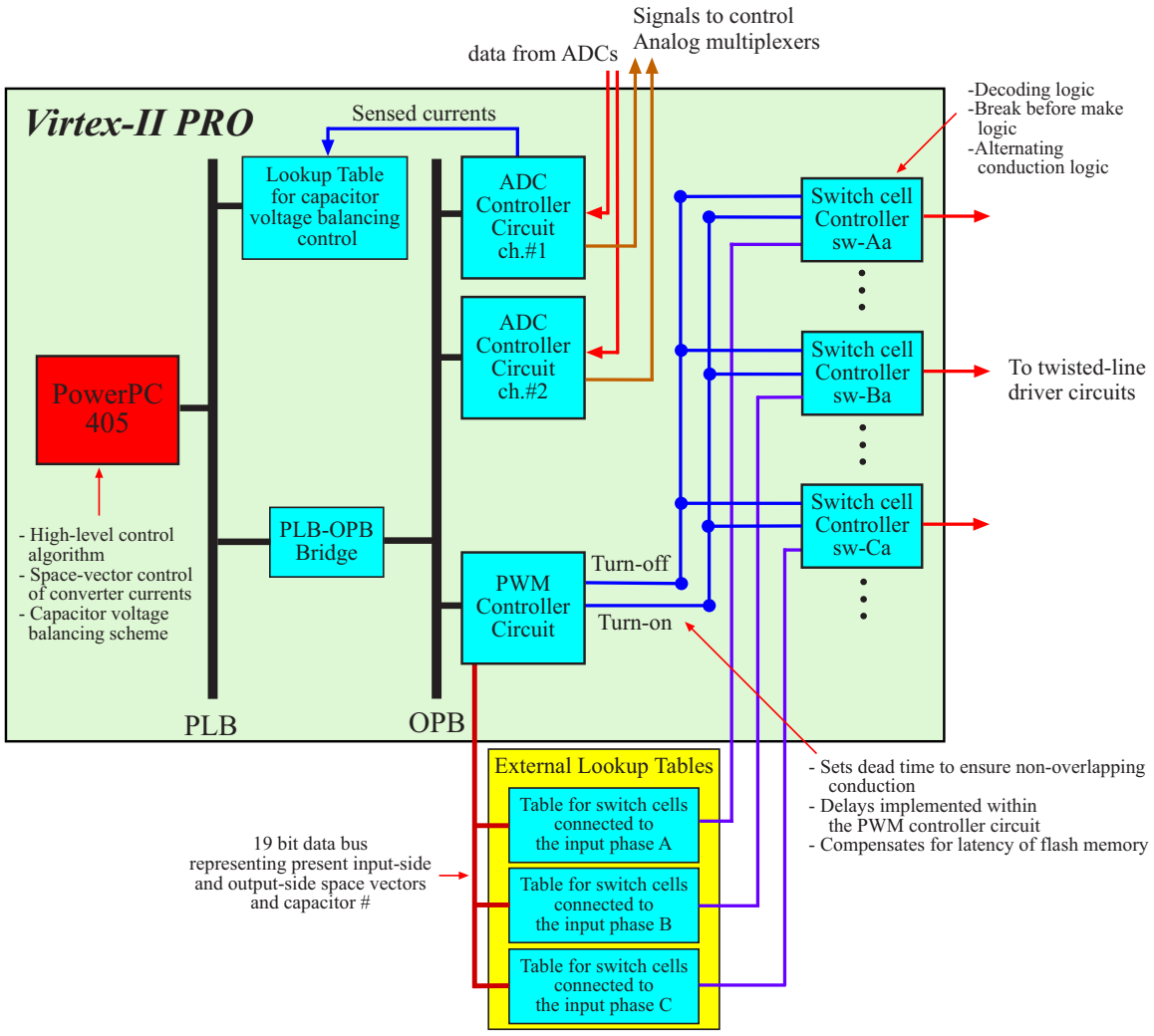


Figure 6.8: Control system block diagram

The block diagram of the digital control system is illustrated in Fig. 6.8. The digital control system is mainly divided into six parts:

1. Analog-to-digital converter (ADC) controller circuits
2. PowerPC microprocessor
3. PWM controller circuit
4. Switch-cell controller circuit
5. Lookup table for states of switch cells
6. Lookup table for capacitor voltage-balancing control.

The PowerPC microprocessor and the peripheral modules interface through a bus architecture, which consists of a processor local bus (PLB) and an on-chip peripheral bus (OPB) [62, 63, 64]. There are also

auxiliary components in the control system, such as digital clock management (DCM) modules, JTAG programming module, and Block RAM (BRAM) modules [64].

The FPGA parts of the digital control circuit were implemented using hardware description language (VHDL). The instructions for the PowerPC microprocessor were written in Assembly language. All codes for the digital control circuit are included in Appendix C.

6.2.1 ADC Controller Circuits

The ADC control circuits were implemented using the FPGA part of the Virtex-II Pro. The main functions of the ADC controller circuits are to control analog multiplexers and to latch the corresponding data from the ADCs. There are two independent control circuits for two different groups of the sensed signals.

The first group is the AC signals, such as line-line voltages and currents. The input-side line-line voltages are sensed by transformers with turn ratios of 230:12. The input, output currents, and the output-side line-line voltages are sensed by Hall Effect devices (LEM LA 55-TP/SP1 for current sensing and LEM LV 25-P for voltage sensing). Photographs of the sensing circuits are included in Figs. 6.9 and 6.10. These sensed AC signals are low-pass filtered by operational amplifier circuits, which also add DC biases into the signals and change the signals into unipolar signals. The DC biases are subtracted digitally inside the ADC controller circuit. An analog multiplexer (MAX306) is employed to select a signal to be digitized by an ADC (AD9220). This 12-bit ADC is operated at 8 MHz. The ADC controller then latches the corresponding data from the ADC.

The second group of sensed signals consists of all nine DC voltages of the switch-cell capacitors, which are sensed by differential amplifier circuits. The differential op-amp circuits also low-pass filter the signals. One of these signals is then sampled singly to be digitized by an analog multiplexer, which is also controlled by an ADC controller circuit. Then the corresponding data are read into the ADC controller circuit.

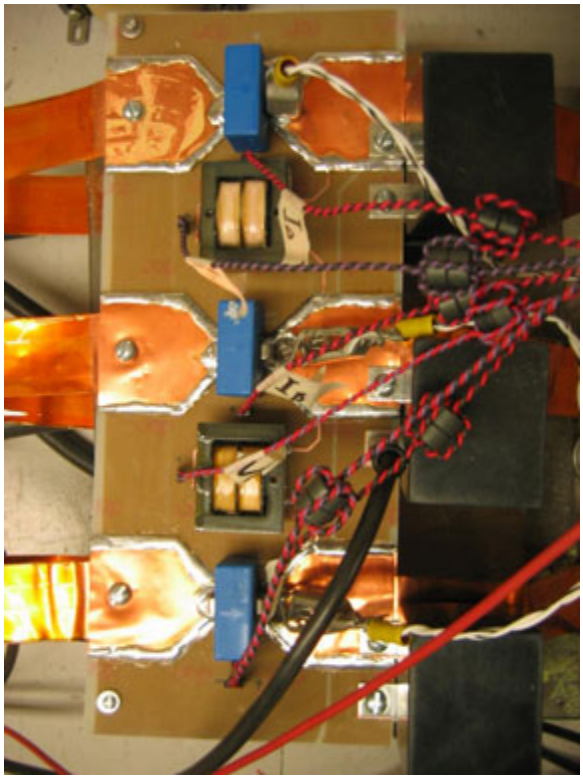


Figure 6.9: Sensor circuits at the input side consist of transformers and Hall Effect sensing devices

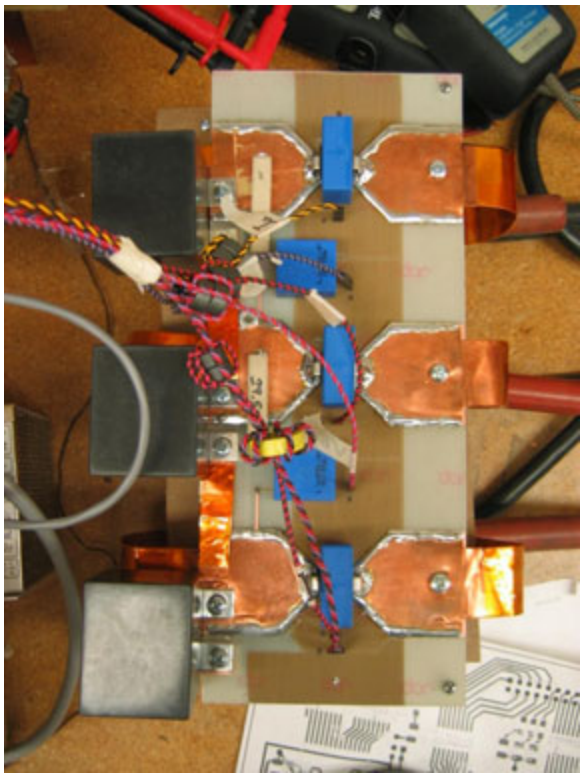


Figure 6.10: Sensor circuits at the output side consist of Hall Effect sensing devices

The op-amp circuits and ADC circuits for both groups of sensed signals were constructed on the same PCB. A photograph of the circuits is shown in Fig. 6.11.

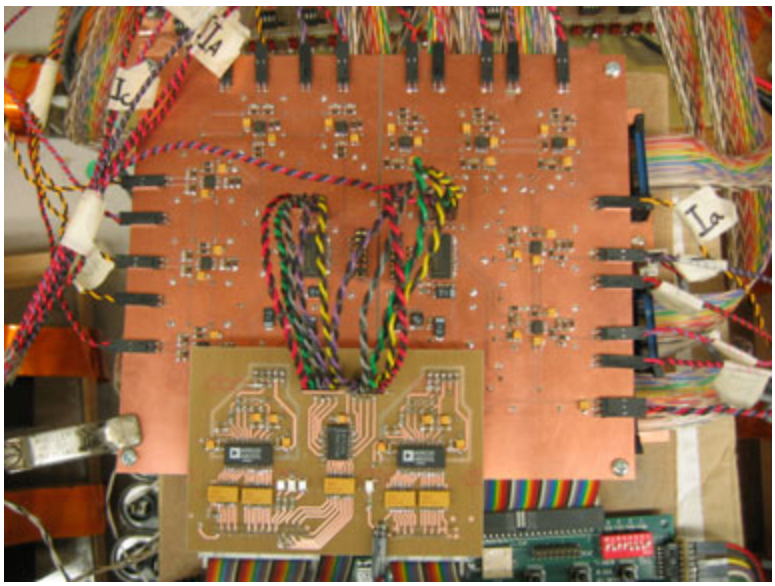


Figure 6.11: Low-pass filter and ADC circuits

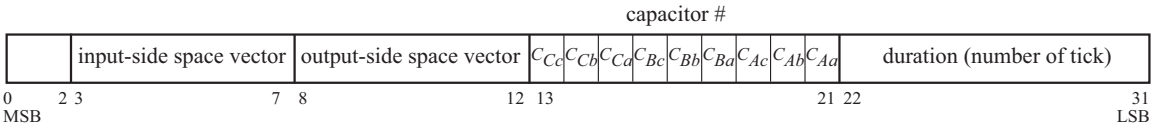
The operations of the ADC controller circuits are asynchronous to the operation of the PowerPC microprocessor. The ADC controller circuits continuously sample data from the ADCs and store the data in their buffers. To prevent the ADC controller circuits from sensing noises in the power stage during the transitions of the switching devices, the operation of the ADC controller circuits are halted .

6.2.2 PowerPC Microprocessor

The microprocessor in the Virtex-II Pro is the PowerPC 405 microprocessor [65, 66]. In the prototype, the PowerPC microprocessor operates with a clock frequency of 300 MHz. In each switching period, the PowerPC microprocessor has to perform the following tasks:

- convert all variables from the three-phase system into variables in the *dq* coordinate
- perform the SVM
- determine the capacitor to be employed in each switching period
- perform capacitor voltage-balancing scheme
- generate a data set for each subinterval in a switching period
- send all information to the PWM controller circuit.

With the maximum of seven subintervals for each switching period, the PowerPC also generates seven sets of data (one set per subinterval). Each set of data contains the input-side space vector, the output-side space vector, the capacitor, and the duration of each subinterval. The bit pattern of the resulting data for each subinterval sent to the PWM controller circuit is illustrated in Fig 6.12.



6.12: Bit pattern represents data for each subinterval of a switching period

The input- and output-side space vectors for each subinterval are represented by 5-bit words. The words can represent all 19 space vectors in the stationary *dq* reference coordinate; hence, 10 bits are needed for each subinterval.

The capacitor employed in each subinterval is represented by a 9-bit word. A high bit (digit "1") indicates that the corresponding capacitor is employed. Bit[21] refers to the capacitor of the switch cell in branch *Aa*, whereas bit[13] refers to the capacitor of the switch cell in branch *Cc*. In the two-level switching mode, the control scheme employs only one capacitor in each subinterval; hence, exactly 1 bit will be high during a given subinterval. When the converter operates in the three-level switching mode, it involves more than one capacitor simultaneously. As a result, multiple bits in this data can be asserted at a time.

The duration of each subinterval is represented by a 1-bit word corresponding to the number of clock ticks for the length of each subinterval. With a clock frequency of 20 MHz employed in the PWM controller circuit, the duration of each subinterval has a resolution of 50 ns.

6.2.3 PWM Controller Circuit

The PWM controller circuit was implemented in the FPGA part of the Virtex-II Pro. The PWM controller circuit controls the duration of each subinterval in one switching period, keeps track of the subinterval in the switching period, and also provides the data representing the converter configuration for each subinterval. A schematic diagram of the PWM controller circuit is shown in Fig. 6.13.

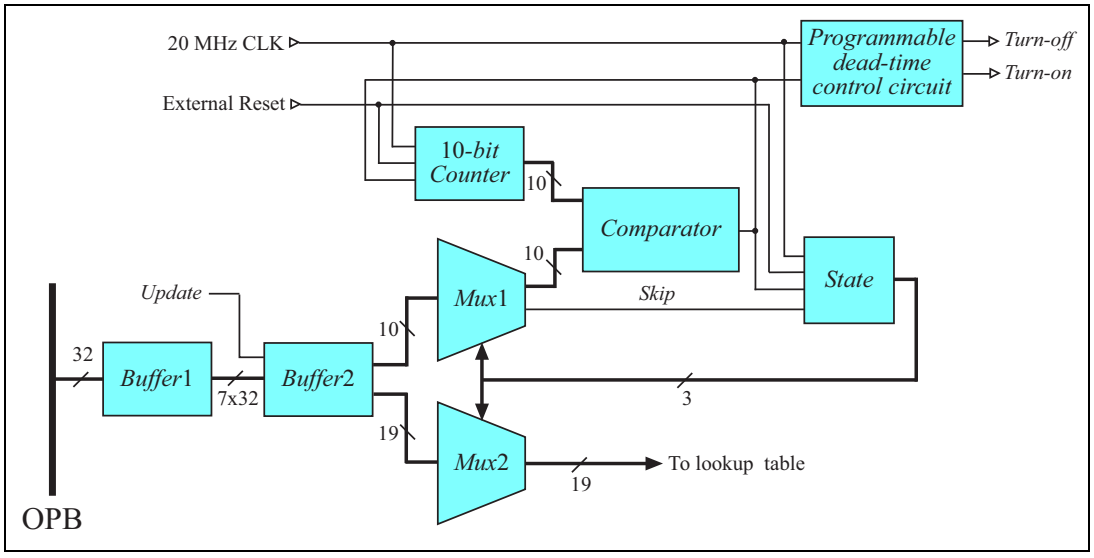


Figure 6.13: Block diagram of the PWM controller circuit

The controller circuit receives seven sets of data from the PowerPC microcontroller through the OPB. The *Buffer*1 is addressed by the PowerPC microprocessor and latches the subinterval data for the next update of these data. The second data buffer, *Buffer*2, latches the subinterval data that are currently used for the rest of the control circuit. *Buffer*2 also divides the data into two sets and feeds them to two separate multiplexers. A double-buffering scheme allows the converter switching frequency to differ from, and be asynchronous with, the microprocessor data sampling rate.

The *Update* signal controls the transfer of the data from *Buffer*1 to *Buffer*2. This signal is generated within the control circuit (not shown in the figure). It is asserted only at the beginning of the first subinterval and all new data are valid within *Buffer*1 (asserted by a signal from the microprocessor). This approach avoids glitches by ensuring that subinterval lengths are not updated in the middle of a switching period.

The two-output multiplexer, *Mux*1, driven by the state of the subinterval, provides data as the reference for an incremental counter to time the duration of the current subinterval. The multiplexer also provides the *Skip* signal, which is asserted when the length of the next subinterval is less than the programmable minimum subinterval width (1.55 μs). This minimum pulse width is needed to prevent glitches caused by gate delay and flash memory latency. The multiplexer, *Mux*2, also driven by the state of the subinterval, feeds the corresponding space vector and capacitor information for the current subinterval to the external lookup table.

The state of the subinterval in each switching period (0 to 6) is tracked by the *State* module. The next subinterval is determined from the result of the *Comparator* (asserted only when the counter value is equal to the reference data from the multiplexer, *Mux*1) and the *Skip* signal.

At the end of each subinterval, a *Turn-off* pulse is generated that commands on-to-off IGBT switching transitions to occur. After a programmable delay, a second pulse (*Turn-on* pulse) is generated, which initiates off-to-on IGBT transitions.

6.2.4 Lookup Table for States of Switch Cells

The lookup table consists of three 512-kB flash memory chips (AT49LV040). Each of these chips contains the data for the three switch cells that are connected to the same input phase. The input (address lines) of the lookup table is the 19-bit data from the PWM controller circuit, representing the input-side and output-side space vectors and capacitor for each subinterval (Bit[3] to Bit[21] in Fig. 6.12). The outputs of the lookup table are nine of 2-bit data; each 2-bit data per one switch cell, which can represent all four states of a switch cell as illustrated in Fig. 6.14.

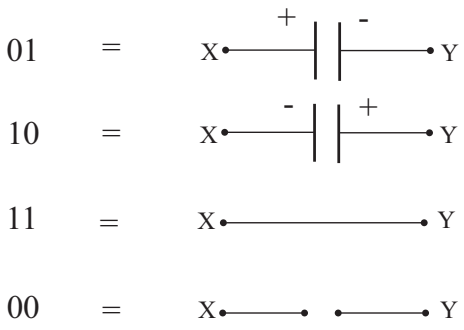


Figure 6.14: Two-bit data representing all four states of switch cell; "X" denotes an input phase and "Y" denotes an output phase

Hence, each chip produces 6 bits of the output data, and the remaining 2 bits are unused. The bit assignment for the output of each flash memory is shown in Fig. 6.15. Invalid inputs, such as illogical combination of capacitors or invalid space vectors, result in turning off all IGBTs. The data contained in the lookup table are included in Appendix D.

unused	data for switch cell connected to the output phase *c*	data for switch cell connected to the output phase *b*	data for switch cell connected to the output phase *a*

Bit 8 Bit 0

Figure 6.15: Bit pattern for the output of the lookup table per an input phase

6.2.5 Switch-Cell Controller Circuits

The digital control circuit has nine identical switch-cell controller circuits, one each for a switch cell. The block diagram of the switch-cell controller circuit is illustrated in Fig. 6.16. The switch-cell controller circuit decodes 2-bit data from the lookup table into four gate signals for the IGBTs in each switch cell. To avoid cross-conduction of the IGBTs during their switching transitions, which leads to momentary shorting of the DC bus voltages through the IGBTs, the "break before make" logics are included in the switch-cell controller circuits. The switch-cell controller circuits also accept the *Turn-on* and *Turn-off* signals from the PWM controller circuit to implement gate signals with "break before make" operation.

There are two ways to realize the short-circuit state, "11," of a switch cell: either both upper IGBTs can conduct or both lower IGBTs can conduct. To distribute the conduction losses among devices, each

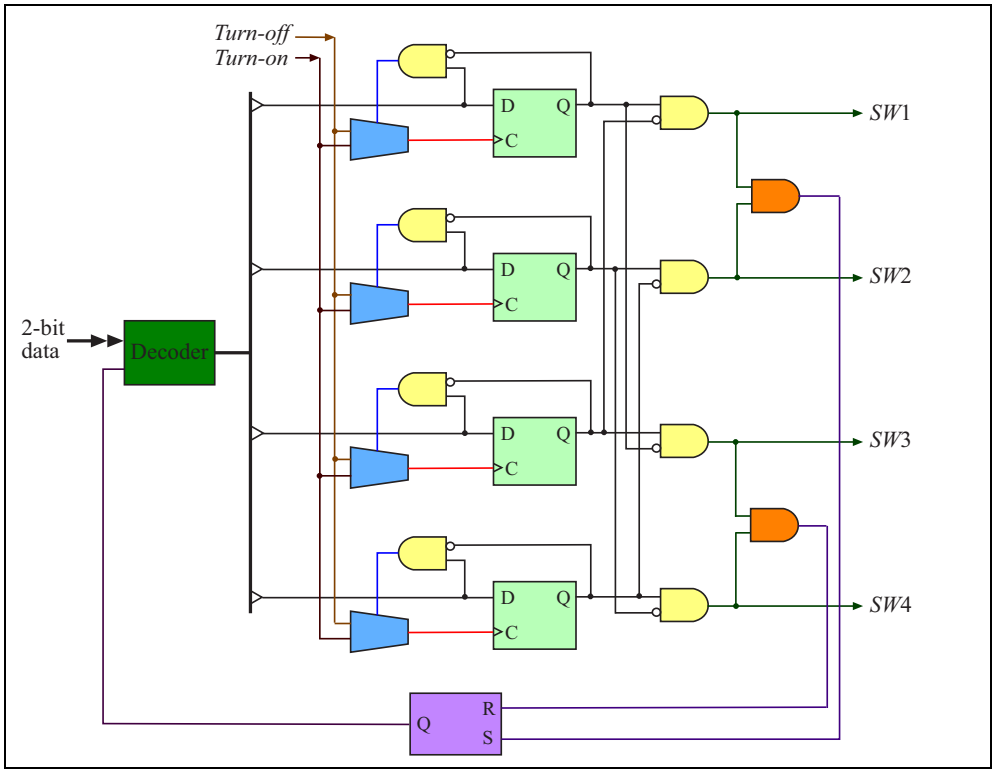


Figure 6.16: Block diagram of the switch-cell controller circuit

switch-cell controller circuit contains an R-S flip-flop that alternates the conduction path between these two choices.

The outputs of the switch-cell controller circuits are sent to opto-isolated gate-driver circuits through twisted-pair line driver and receiver-chip pairs. These twisted-pair line driver and receiver-chip pairs improve noise sustainability in the gate signals.

6.2.6 Lookup Table for Capacitor Voltage Balancing Control

This module is employed in the capacitor voltage balancing control scheme, which was described in Chapter 4. The module is connected to the PLB and can be addressed by the PowerPC microprocessor. The input of this lookup table is the data representing a combination of two capacitors and the sensed currents from the ADC controller circuit. The lookup table then provides a set of opposite space vectors, along with the current through a capacitor as outputs.

7 Conclusions: Part I

7.1 Summary of Part I

The multilevel matrix converter was proposed as a new approach to the power electronics for variable-speed wind energy systems. The purpose of this approach is to improve the energy capture of the wind energy systems by extending the high-efficiency range of the converter to low-wind operating points, where typical wind energy systems operate most of the time. The operation of the multilevel matrix converter is based on the multilevel conversion technique, which has been proved to be an approach that can meet the performance requirements. Multilevel conversion is scalable to higher power and higher voltage levels and allows the use of superior low-voltage fast-switching semiconductor devices in high-voltage, high-power applications. It can also maintain high efficiency at a fraction of its rated power, without sacrificing performance at rated power.

The multilevel matrix converter with basic converter configuration consists of nine capacitor-clamped H-bridge switch cells connected from each input phase to each output phase. Each H-bridge switch cell can generate three different voltage-levels across its terminals when devices conduct current and is capable of blocking voltages with magnitudes less than its capacitor voltage when all devices are turned off. The converter line-line voltages are synthesized from the PWM of the capacitor voltages of all nine H-bridge switch cells. Hence, inductors are used as filter elements at both sides of the converter. With the symmetrical structure, the multilevel matrix converter is able to buck or boost the voltage magnitudes.

In addition, the modular approach of the H-bridge switch cell can solve the problem of the complex bus-bar configurations in the multilevel converter. All semiconductor devices are locally clamped by the switch-cell capacitors. This approach also exhibits good semiconductor device utilization.

Two operating modes are available in the multilevel matrix converter with the basic converter configuration. First, when the voltage magnitudes at both sides are close to each other, the converter generates terminal voltages with two-level switching at both sides. Second, when the voltage magnitudes at both sides are considerably different, the converter generates terminal voltages with two-level switching at one side and terminal voltages with three-level switching at the other side.

The control scheme for the multilevel matrix converter consists of two parts that must be performed simultaneously: (1) terminal AC voltage synthesizing and (2) capacitor voltage regulating. The space-vector PWM technique is employed for synthesizing the terminal AC voltages. The single-capacitor control scheme and the capacitor voltage-balancing scheme, which are based on the SVM, are proposed for the multilevel matrix converter operating in the two-level switching mode.

The SVM is performed in the *dq* coordinate; hence, the three-phase variables are transformed into two-phase *dq* variables. The multilevel matrix converter can generate 19 combinations of the three-phase line-line voltages corresponding to 19 space vectors in the *dq* coordinate. The 19 space vectors are one null-state space vector, six space vectors with magnitude $2V_{cap}/\sqrt{3}$, six space vectors with magnitude $2V_{cap}$, and six space vectors with magnitude $4V_{cap}/\sqrt{3}$. The null-state space vector and the six space vectors with magnitude $2V_{cap}/\sqrt{3}$ are used in the two-level switching, while all 18 space vectors, except the null-state space vector, are employed in the three-level switching.

With the single-capacitor control scheme, only one switch-cell capacitor is employed to synthesize terminal voltages during each switching period; all nine switch-cell capacitors are employed throughout the input and output line periods. The single-capacitor control scheme determines the single capacitor to

be employed in each switching period from two conditions: (1) the positions of the input-side and the output-side reference space vectors(2) and the relative values of the duty cycles of the input-side and the output-side null-state space vectors. This control scheme is optimized in the sense of minimizing circulating currents among the capacitors. In addition, the control scheme also allows the multilevel matrix converter to be modeled as a DC-link converter, which significantly reduces the complexity in controlling the converter. At steady-state operation, the charge balance of the capacitor employed during a switching period can be achieved. To guarantee that there is one valid switch-cell capacitor for each switching period, a specific space-vector pattern in each switching period is required; hence, this control scheme can be operated within a range of voltage gain ratios.

The single-capacitor control scheme is theoretically able to stabilize all nine capacitor voltages in the converter. However, from the experimental results, there exists some deviation in the capacitor voltages. The disturbances in the capacitor voltages arise from the energy stored in stray inductances in the windings interconnected between switch cells. This energy is transferred to the switch-cell capacitors during the dead-time interval of on-to-off transitions of the switch cells; the anti-parallel diodes provide a path for currents to conduct. As a result, the capacitor voltages are slowly charged up when the capacitors are not employed to generate terminal voltages. In the first switching period, when the capacitor is used in the converter, it is quickly discharged causing a high-magnitude current spike in the converter. This behavior in the capacitor voltages restrains the converter from being operated at high voltages. The single-capacitor control scheme alone cannot regulate all nine capacitor voltages because the control scheme allows only one switch-cell capacitor to be employed during each switching period. Besides, the control scheme determines which capacitor is to be employed in each switching period from the terminal AC voltages, independent of the capacitor voltages.

The capacitor voltage-balancing control was proposed to regulate capacitor voltages. The control scheme is based on the modification of the SVM so that more capacitors can be employed during each switching period. By using two additional space vectors having equal magnitude but opposite directions to partially replace the null-state space vector, two more capacitors can be charged and discharged in each switching period. The opposite space vectors with the equal magnitude also contribute to the average of zero for all line-line voltages, similar to the null-state space vector. Consequently, they can partially replace the null-space space vector in the conventional SVM with minimum effect on the average terminal voltages. Associated with the single-capacitor control scheme, the control scheme can involve a maximum of three capacitors in each switching period. While the two capacitors are charged and discharged in each switching period, the other capacitor experiences no net change in charge. The capacitors having the maximum voltage and the minimum voltage are chosen to be regulated in each switching period. Therefore, the remaining capacitor voltages are bounded by these two extreme capacitor voltages. All nine capacitor voltages are driven toward the average voltage of nine capacitor voltages by the control scheme. The stability of the proposed capacitor voltage balancing scheme is guaranteed by a Lyapunov's algorithm.

The three-level switching operations in the multilevel matrix converter with the basic configuration were proved possible by the experimental validations. In the three-level switching mode, the converter involves more than one capacitor simultaneously. The currents flowing through the capacitors depend on the switching-device combinations and are dependant on the input and output currents. Hence, the control scheme for the converter operating in the three-level switching mode requires knowledge of the power factors at both sides. A possible control scheme has been discussed; however, the control scheme requires further investigation.

The laboratory prototype has been constructed to show the operation of the multilevel matrix converter and to verify the proposed control schemes. The converter prototype was built based on PCBs and operates with a switching frequency of 20 kHz. Insulated gate bipolar transistors with anti-parallel diodes

were used as switching devices. The proposed control schemes have been shown to be achievable in a real-time digital control circuit by using a microprocessor, field programmable gate arrays (FPGAs), and flash memory chips.

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Part II
Feedback Controller Design

8 Introduction to Part II

8.1 Motivation

Part II develops the fundamentals required for regulation of the average capacitor voltage and the currents of both the input and the output side of the new modular matrix converter. This is necessary for control of machine torque, power throughput, and transistor voltage stresses.

The first step is to model the converter dynamics. Several papers [14-16, 24] and books [6] discuss methods of modeling different types of converters. For example, [15-16, 24] deal with a conventional matrix converter. However, the new modular matrix converter differs in that each switch cell resembles an H-bridge converter. Hence, the modeling of the new converter requires substantial modification of the modeling approach. The differential equations derived to model the converter are nonlinear. Those equations are linearized to get a steady-state model and a small-signal linear model. The steady-state model provides information about the converter operation under nominal conditions. The linear model corresponds to the disturbances in the variables that are to be regulated (the capacitor voltages and the input and output currents). Through this model, one can investigate the stability and controllability of the converter. A controller to drive those variations to zero is then designed.

Some control techniques of conventional matrix converters are discussed in [15, 16, 24]. However, the pole placement and optimal control techniques considered in this report were never discussed with relation to matrix converters. Moreover, such techniques are simpler to realize. Both techniques yield a constant controller-gain matrix. The response of the closed-loop system is stable with minimal transients. However, the controller-gain matrix of both techniques changes as the parameters of the converter change (e.g., input voltage resulting from a change of wind speed or power demand). This led to the idea of finding relationships between the elements of the controller-gain matrix and the converter's parameters. It is found here that the controller-gain matrix designed via the pole-placement method is very sensitive to the variations in the converter's parameters. On the other hand, the optimal controller is not sensitive and can be presented as a function of the converter's parameters. The optimal control technique is applied to the converter implemented in Part I. Experimental results prove the validity of the converter model and its control.

8.2 Control of the Terminal Currents and Average Capacitor Voltage

Maximum power transfer from the input side of the new modular matrix converter, such as a variable-speed wind power generator, to the output side of the converter, such as a utility bus, requires that the currents and capacitor voltages be controlled. The transient responses resulting from a change in power demand, wind speed, or switching between capacitors must be minimized. A feedback controller can accomplish such task. Figure 8.1 shows the implementation of the controller in the whole system. The figure shows a variable-speed wind power generator connected to one side of the matrix converter, which

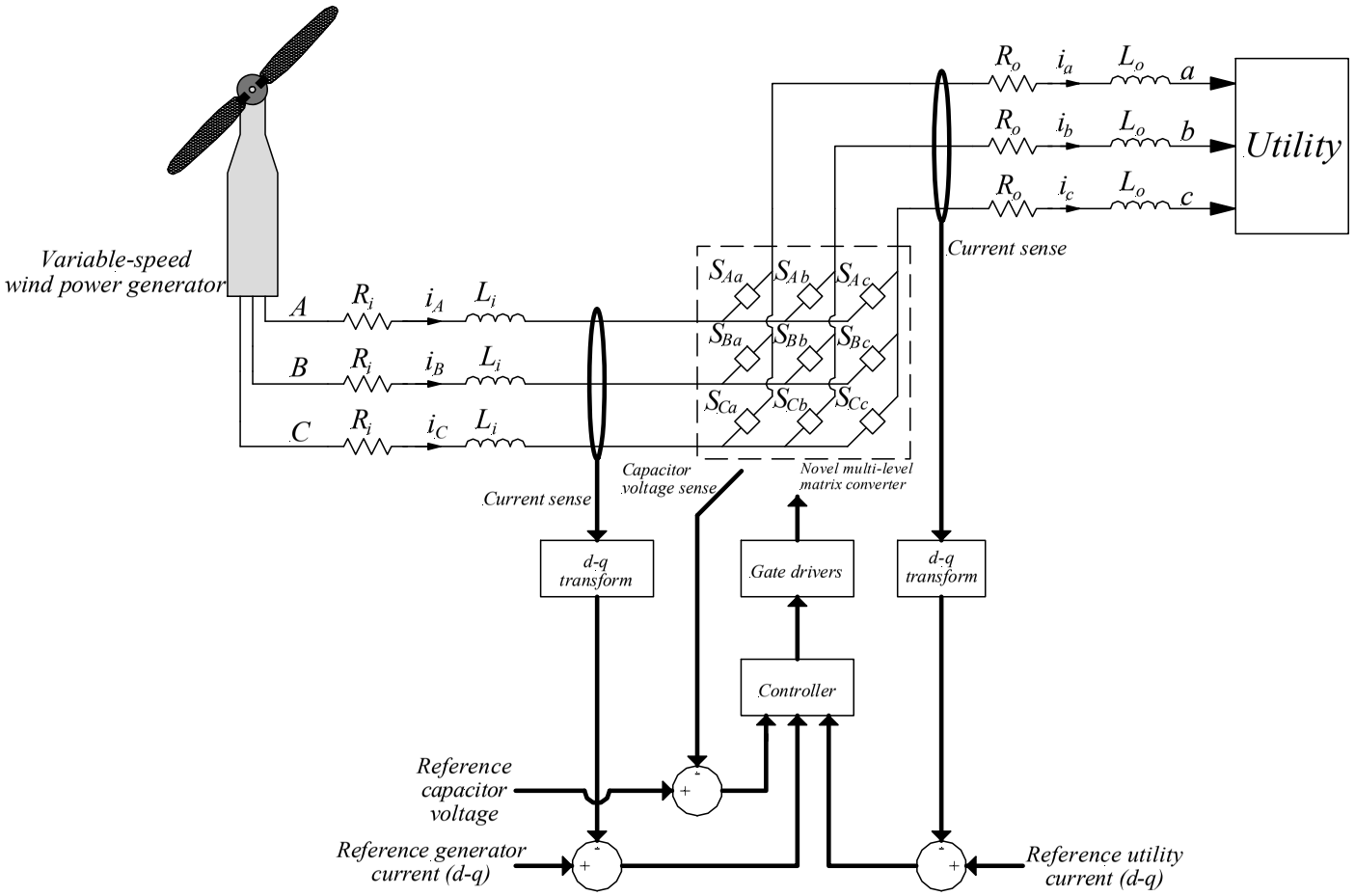


Figure 8.1 Overall system with the feedback controller implemented

is represented by nine switches (S_{Aa} , S_{Ab} ....) To provide a numerical example, it is assumed in this report that the wind power generator operates at a constant 9.6 V/Hz with a line frequency that varies from 13 Hz to 25 Hz, corresponding to an input line-to-line voltage range from 125 V to 240 V. The other side of the converter is connected to the utility grid, with a line-to-line voltage of 240 V and an output line frequency of 60 Hz. It is assumed that the utility is to draw up to 20 A current with a power factor range from 0.5 to unity. Filter inductors are connected on both sides of the converter, and the line resistances shown in the figure are the winding resistances of the inductors.

Input- and output-line currents are sensed and transformed into the *dq* frame (a transformation that represents three-phase currents or voltages as a vector). The voltage of the utilized capacitor is also sensed. The figure shows that those sensed signals are compared to reference values to get the variation signals. Those error signals are fed into the controller to get the control needed to switch the matrix converter.

To design a feedback controller for the new modular matrix converter, differential equations describing the converter are derived. The currents of the input side, as well as the output side of the matrix converter, are transformed into the *dq*0 frame; this provides the convenience of representing the three-phase currents as one vector rather than three sinusoidal variables. Those differential equations form the state-space model of the matrix converter. As it turns out, the state-space model is nonlinear with five states and four inputs and five independent outputs that coincide with the states. All five states (input and output currents and the capacitor voltage) depend on each other, as well as the input control. In this report, linear multi-input multi-output control theory is applied to this system; this requires linearization of the converter model.

The nonlinear model of the matrix converter is divided into a linear-state space (small-signal) model and the steady-state (nominal) model. The steady-state model describes how the converter operates under nominal operating conditions with no variations in its parameters. This model is a reference point to the nonlinear model of the matrix converter. The linear state space model, which is a function of the matrix converter steady-state values, represents the variations in the matrix converter's parameters about the nominal operating point. Those variations need to be minimized, if not driven to zero, with fast and acceptable transient responses. Hence, a controller has to be designed for the linear state-space model. The controller is then implemented in the nonlinear model of the matrix converter. Simulation results suggest that this approach can yield a good design. Specifically, the results show that the currents and capacitor voltages of the novel modular matrix converter can be controlled at almost any operating point to achieve maximum efficiency.

Two methods are considered in designing the controller. Both methods yield a control-gain matrix. The first method is the pole-placement technique, which involves placing the poles of the linear state space model of the matrix converter at desired locations. Upon implementation of this controller, the simulation shows acceptable results at the nominal operating point. However, as the operating conditions of the matrix converter change, the open-loop poles of the linear-state space model change and, hence, the controller has to be modified to place the poles at the desired locations. To avoid running the pole-placement routine to find a control-gain matrix every time the operating conditions change, a relationship has to be established between the elements of the control-gain matrix and the matrix converter parameters. It was found that the elements of the control-gain matrix depend strongly on the input-line frequency (and, therefore, the wind speed and the generator output voltage) and the output current. Unfortunately, no clear relationship can be found between the control-gain matrix elements and the input-line frequency and the output currents. Another control approach had to be considered.

The second method is optimal control, as explained in Chapter 10; it involves solving the *algebraic Riccati equation*. The relationships between the elements of the control-gain matrix and the input frequency and output currents, which are generated by the linear optimal-control method, are much simpler than those of the pole-placement method. By taking all possible operating points of the matrix converter into account, that relationship can be approximated by a polynomial curve-fitting method. Therefore, instead of finding a solution to the algebraic Riccati equation every switching period, the control-gain matrix can be calculated online quickly via simple math operations between the output currents and the input line frequency.

8.3 Organization of Part II

The first objective in Part II is to model the new modular matrix converter. This model provides an analytical basis for design of the "control system." The second objective is to design a controller for the modular matrix converter that operates stably at all possible operating points and guarantees good efficiency.

Chapter 9 begins with derivation of the matrix converter state space model. There, the nonlinear averaged model is developed. That model is then linearized to get the small-signal model and the steady-state model. As it will be seen, the linear-state space model is a function of the nominal (steady-state) solution of the matrix converter. This chapter ends with a discussion of the stability, controllability, and observability of the linear-state space model of the matrix converter. Tests of the model over a wide range of operating points show that the model is stable, fully controllable, and observable.

Chapter 10 covers the feedback-controller design of the new matrix converter. A simulation of the matrix converter operating under open-loop conditions illustrates the importance of the controller-design techniques of this chapter. A controller design via the pole-placement method is then presented. Simulation results of the controller implemented in the nonlinear model of the matrix converter are demonstrated. The results show that the responses of the input and output currents and the capacitor voltages of the matrix converter over a wide range of operating points settle to their nominal values after an acceptable time with small transients. An explanation is provided about how it is difficult to find a relationship between the elements of a controller-gain matrix, which is designed by the pole-placement method, and the matrix-converter parameters. As it will be seen, that relationship is not linear and is not easily approximated as a function of the converter parameters. Hence, linear optimal control is proposed instead. Fundamentals of well-known linear optimal control are briefly reviewed. An optimal controller is then designed and, as in the pole-placement method, the controller is tested with the nonlinear model. The responses of the matrix converter when the optimal controller is implemented settle faster than those when the pole-placement controller is implemented. Again, the relationships between the elements of the controller-gain matrix, which are designed by optimal control method, and the matrix-converter parameters are demonstrated. Those relationships are approximated by polynomial functions of the input-line frequency and output-current amplitude. Equations that represent the elements of the controller-gain matrix in terms of the matrix-converter parameters are derived and tested in the simulation. In Chapter 10, the simulation program is modified to implement models of all nine capacitors of the matrix converter to observe how these capacitors independently behave. Simulation results of this task are also presented. Indeed, all capacitor voltages reach their nominal values from 0 volts once each one is utilized at most one time. All simulation results are carried out using MATLAB/SIMULINK, which is a powerful tool in control design and simulation. Using SIMULINK to implement the matrix converter makes it is clear and easy to visualize its operation. Appendix D provides the SIMULINK files used for simulation of the final model of the matrix converter.

Experimental results are provided in Chapter 11. The matrix-converter prototype of Part I was connected between the utility and a resistive load. The parameters that the elements of the controller-gain matrix depend upon are different than those when the converter is connected between the utility and a wind turbine generator. The experimental results prove the validity of the modeling scheme of the matrix converter, as well as the feedback-control strategy implemented. Chapter 12 summarizes the key results of Part II.

9 State-Space Model of the Matrix Converter

9.1 Derivation of the State-Space Equations of the New Matrix Converter

This chapter provides the basis for design of a closed-loop controller for the new modular matrix converter. A mathematic model of the converter is developed, which describes the average components of the converter waveforms and which is suitable for simulation and controller design using conventional tools, including MATLAB/SIMULINK and known linear multivariable controller-design techniques.

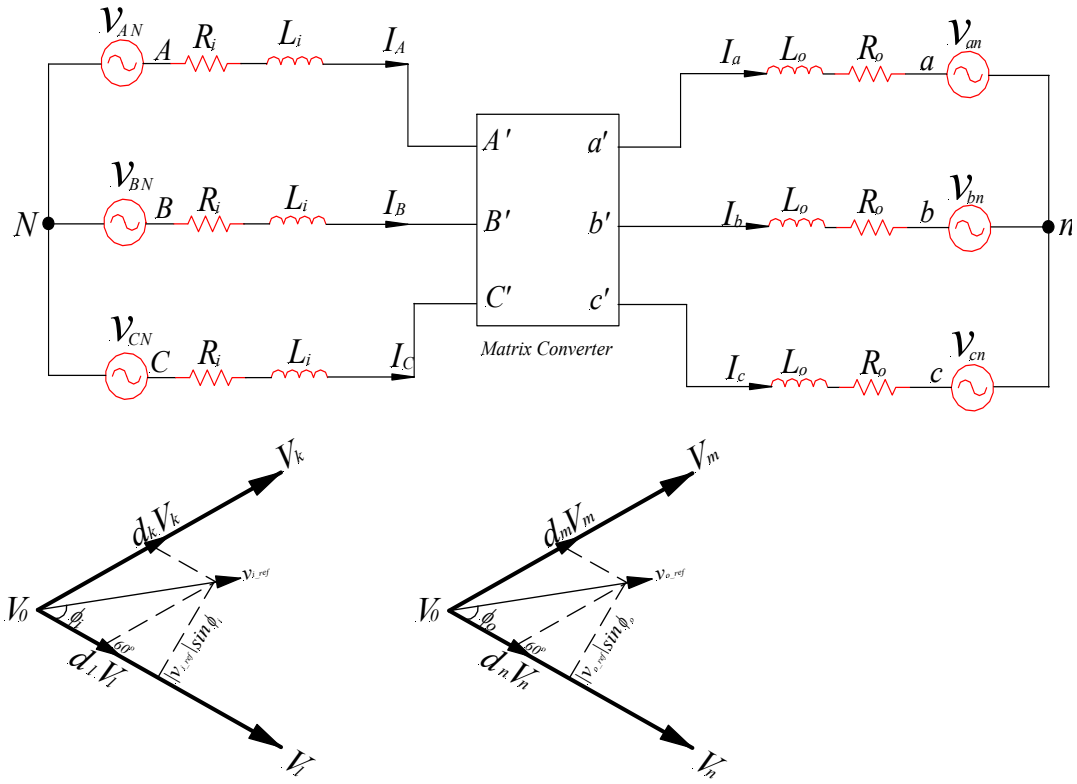
When the converter system of Part I is employed in a wind power generation system, it is desired to control the generator current magnitude and phase and, hence, also the generator torque. In addition, it is desired to control the output (utility-side) power factor and the average capacitor voltage. The control input variables are the duty cycles or their *d-q* transformed equivalents. Use of SVM and the *d-q* reference frame makes the resulting model easily employed for field-oriented control of the generator as well.

Thus, the controlled variables are chosen to be the input and output currents and the capacitor voltage. The control input will be the input and output duty ratios. In order to do so, state-space equations have to be derived for the matrix converter. Because the resulting equations are nonlinear, perturbation and linearization is required and is accomplished by assuming that the input control variables and the output variables of the state-space equations assume some nominal values (steady-state solutions) plus some small perturbations (small-signal AC model) [4, 5, 6, 14]. A controller is then designed for the small-signal AC model to drive those signals to zero. The controller is then applied to the nonlinear model.

In the following sections, the instantaneous voltages and currents of both sides of the converter are defined. A strategy is then described to transform the converter's equation to the stationary *dq*0 frame. The differentianl equations of the converter are derived for the input side, the output side, and the internal capacitors. Those equations constitute the converter's nonlinear state-space equations. The equations are then linearized. An examination of those linearized state-space equations is discussed.

9.2 The Terminal Voltages and Currents

Figure 9.1 shows the matrix converter connected to two systems: the input having capital subscripts and the output having lower case subscripts. The figure shows the direction of the current flow. Resistances have been added to take the line losses into consideration. Those resistances can be thought of as those of the filter inductors.



Input side **Output side**

Figure 9.1: Configuration of the matrix converter terminal connections and SVM to control the input and output voltages

The input-side line-to-neutral voltages are

$$\begin{bmatrix} v_{AN}(t) \\ v_{BN}(t) \\ v_{CN}(t) \end{bmatrix} = \frac{V_{im}}{\sqrt{3}} \begin{bmatrix} \cos(\omega_i t - 30^o) \\ \cos(\omega_i t - 30^o - 120^o) \\ \cos(\omega_i t - 30^o + 120^o) \end{bmatrix} \tag{9.1}$$

so that the input-side line-to-line voltages are

$$\begin{bmatrix} v_{AB}(t) \\ v_{BC}(t) \\ v_{CA}(t) \end{bmatrix} = V_{im} \begin{bmatrix} \cos(\omega_i t) \\ \cos(\omega_i t - 120^o) \\ \cos(\omega_i t + 120^o) \end{bmatrix} \tag{9.2}$$

and the input-side currents are

$$\begin{bmatrix} i_A(t) \\ i_B(t) \\ i_C(t) \end{bmatrix} = I_{im} \begin{bmatrix} \cos(\omega_i t + \theta_{pfi} - 30^o) \\ \cos(\omega_i t + \theta_{pfi} - 30^o - 120^o) \\ \cos(\omega_i t + \theta_{pfi} - 30^o + 120^o) \end{bmatrix}. \tag{9.3}$$

The voltages across the input side of the matrix converter are then

$$\begin{bmatrix} v_{A'B'}(t) \\ v_{B'C'}(t) \\ v_{C'A'}(t) \end{bmatrix} = V_{im'} \begin{bmatrix} \cos(\omega_i t + \theta_i) \\ \cos(\omega_i t + \theta_i - 120^o) \\ \cos(\omega_i t + \theta_i + 120^o) \end{bmatrix}. \tag{9.4}$$

On the output side, the line-to-neutral voltages are

$$\begin{bmatrix} v_{an}(t) \\ v_{bn}(t) \\ v_{cn}(t) \end{bmatrix} = \frac{V_{om}}{\sqrt{3}} \begin{bmatrix} \cos(\omega_o t - 30^o) \\ \cos(\omega_o t - 30^o - 120^o) \\ \cos(\omega_o t - 30^o + 120^o) \end{bmatrix} \tag{9.5}$$

and the line-to-line voltages are

$$\begin{bmatrix} v_{ab}(t) \\ v_{bc}(t) \\ v_{ca}(t) \end{bmatrix} = V_{om} \begin{bmatrix} \cos(\omega_o t) \\ \cos(\omega_o t - 120^o) \\ \cos(\omega_o t + 120^o) \end{bmatrix}. \tag{9.6}$$

The voltages across the output side of the matrix converter are

$$\begin{bmatrix} v_{a'b'}(t) \\ v_{b'c'}(t) \\ v_{c'a'}(t) \end{bmatrix} = V_{om'} \begin{bmatrix} \cos(\omega_o t + \theta_o) \\ \cos(\omega_o t + \theta_o - 120^o) \\ \cos(\omega_o t + \theta_o + 120^o) \end{bmatrix} \tag{9.7}$$

and the output currents are

$$\begin{bmatrix} i_a(t) \\ i_b(t) \\ i_c(t) \end{bmatrix} = I_{om} \begin{bmatrix} \cos(\omega_o t + \theta_{pfo} - 30^o) \\ \cos(\omega_o t + \theta_{pfo} - 30^o - 120^o) \\ \cos(\omega_o t + \theta_{pfo} - 30^o + 120^o) \end{bmatrix}. \tag{9.8}$$

Equations (9.1-9.8) are used in the derivation of the matrix-converter differential equations, as well as in finding its steady-state solution.

9.3 SVM and the Stationary *dq*0 Frame

In Part I, it was seen that each side of the converter switches three times during one switching period with duty ratios: d_l , $d_{k,}$ and d_{i_0} from the input and d_n , $d_{m,}$ and d_{o_0} from the output. Note that

$$d_l + d_k + d_{i\_0} = d_n + d_m + d_{o\_0} = 1 .$$

Figure 9.1 shows segments of the input and output space-vector diagrams. The input reference voltage space vector is found to be

$$v_{i\_ref} = d_l V_l + d_k V_k + d_{i0} V_0 \tag{9.9}$$

where

$$\begin{aligned} d_l &= m_i \sin(60^o - \phi_i) \\ d_k &= m_i \sin(\phi_i) \\ d_{i0} &= 1 - d_k - d_l \end{aligned} \tag{9.10}$$

The same concept has been applied to the output side:

$$v_{o\_ref} = d_n V_n + d_m V_m + d_{o0} V_0 \tag{9.11}$$

$$\begin{aligned} d_n &= m_o \sin(60^o - \phi_o) \\ d_m &= m_o \sin(\phi_o) \\ d_{o0} &= 1 - d_m - d_n \end{aligned} \tag{9.12}$$

Because V_k and V_l represent space vectors that tell which input phase is connected across v_{cap}, we can define a 3 x 1 vector $[V_x]$ ($x = k,l,m,n$) that consists of 1s and 0s that show which terminal is connected across the capacitor. For example, if V_k from Fig. 9.1 is V_1, then V_{AB} is connected across the capacitor, and V_{CA} is connected across the capacitor with negative polarity. Therefore, the vector $[V_k] = [1 \quad 0 \quad -1]^T$ and $[V_l] = [1 \quad -1 \quad 0]^T$. For this example, Eq. (9.9) can be rewritten as

$$v_{i\_ref} = (d_l[V_l] + d_k[V_k])v_{cap} = (d_6 \begin{bmatrix} 1 \\ 0 \\ -1 \end{bmatrix} + d_1 \begin{bmatrix} 1 \\ -1 \\ 0 \end{bmatrix})v_{cap} . \tag{9.13}$$

We can now define

$$\begin{aligned} [d_i V_i] &= d_l[V_l] + d_k[V_k] \\ [d_o V_o] &= d_n[V_n] + d_m[V_m] \end{aligned} \tag{9.14}$$

Each segment of the converter voltage space-vector diagram is 60^o in length, and ϕ_i varies from 0 to 60^o as the input reference voltage space vector v_{i_ref} rotates in the space-vector diagram. The space vector v_{i_ref} represents the rotating *dq*0 vector of the voltages across the input terminals of the converter defined in Eq. (9.4), which is transformed as follows:

$$\begin{bmatrix} v_{di'}(t) \\ v_{qi'}(t) \end{bmatrix} = \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_{A'B'}(t) \\ v_{B'C'}(t) \\ v_{C'A'}(t) \end{bmatrix} = \frac{3}{2} v_{i\_m'} \begin{bmatrix} \cos(\omega_i t + \theta_i) \\ \sin(\omega_i t + \theta_i) \end{bmatrix} \tag{9.15}$$

which is a space vector that rotates counter-clockwise, with time, at an angle $\omega_i t + \theta_i$. The angle ϕ_i can be found as a function of $\omega_i t + \theta_i$, and the segment where the reference voltage space vector is located is

$$\phi_i = (\omega_i t + \theta_i) + \frac{\pi}{6}(3 - 2s) \tag{9.16}$$

where *s* is the segment number. The same applies to the output reference voltage space vector.

For the single-capacitor control scheme, only one phase current flows into, or out of, the capacitor during each of the five subintervals. More specifically, during one cycle, exactly two different input-phase currents (from d_l and d_k subintervals) flow into the capacitor, and exactly two different output-phase currents (from d_m and d_n subintervals) flow out of the capacitor. Now, we can define a 1 x 3 vector $[I_x]$ ($x = k,l,m,n$), which consists of only one entry as –1 or 1 and two 0s that represent the current flowing into or out of the capacitor. For example, if the reference voltage space vectors of both input and output sides are in segment 1, then the current vectors are as follows:

$$[I_l] = \begin{bmatrix} 0 & -1 & 0 \end{bmatrix}$$
$$[I_k] = \begin{bmatrix} 1 & 0 & 0 \end{bmatrix}$$
$$[I_n] = \begin{bmatrix} 0 & 1 & 0 \end{bmatrix}$$
$$[I_m] = \begin{bmatrix} -1 & 0 & 0 \end{bmatrix}$$

This means that $-I_B$ flows into the capacitor (or I_B flows *out* of the capacitor) during d_l subinterval; I_A flows into the capacitor during d_k subinterval; I_b flows into the capacitor during the d_n subinterval; and $-I_A$ flows into the capacitor (or I_A flows *out* of the capacitor) during the d_m subinterval. As we've done for the voltages in Eq. (9.14), we can define

$$\begin{aligned} [d_i I_i] &= d_l[I_l] + d_k[I_k] \\ [d_o I_o] &= d_n[I_n] + d_m[I_m] \end{aligned} \tag{9.17}$$

Table 9.1 summarizes the results of the procedure previously described for the input side depending on the location of the input reference-voltage space vector. Table 9.2 summarizes the results for the output side depending on the location of the output reference-voltage space vector. Those results constitute the basis to derive the matrix converter's differential equations and transform them into the stationary *dq*0 frame.

Table 9.1: Input-Side Space Vectors

$\omega_i t+\theta_i$	s	ϕ_i	$[V_l]$	$[V_k]$	$[I_l]$	$[I_k]$	$[d_i V_i]$	$[d_i I_i]$
$[-30^o,30^o]$	1	$(\omega_i t+\theta_i)+30^o$	$\begin{bmatrix}1\\-1\\0\end{bmatrix}$	$\begin{bmatrix}1\\0\\-1\end{bmatrix}$	$\begin{bmatrix}0 & -1 & 0\end{bmatrix}$	$\begin{bmatrix}1 & 0 & 0\end{bmatrix}$	$\begin{bmatrix}d_l+d_k\\-d_l\\-d_k\end{bmatrix}$	$\begin{bmatrix}d_k & -d_l & 0\end{bmatrix}$
$[30^o,90^o]$	2	$(\omega_i t+\theta_i)-30^o$	$\begin{bmatrix}1\\0\\-1\end{bmatrix}$	$\begin{bmatrix}0\\1\\-1\end{bmatrix}$	$\begin{bmatrix}1 & 0 & 0\end{bmatrix}$	$\begin{bmatrix}0 & 0 & -1\end{bmatrix}$	$\begin{bmatrix}d_l\\d_k\\-(d_l+d_k)\end{bmatrix}$	$\begin{bmatrix}d_l & 0 & -d_k\end{bmatrix}$
$[90^o,150^o]$	3	$(\omega_i t+\theta_i)-90^o$	$\begin{bmatrix}0\\1\\-1\end{bmatrix}$	$\begin{bmatrix}-1\\1\\0\end{bmatrix}$	$\begin{bmatrix}0 & 0 & -1\end{bmatrix}$	$\begin{bmatrix}0 & 1 & 0\end{bmatrix}$	$\begin{bmatrix}-d_k\\d_l+d_k\\-d_l\end{bmatrix}$	$\begin{bmatrix}0 & d_k & -d_l\end{bmatrix}$
$[150^o,210^o]$	4	$(\omega_i t+\theta_i)-150^o$	$\begin{bmatrix}-1\\1\\0\end{bmatrix}$	$\begin{bmatrix}-1\\0\\1\end{bmatrix}$	$\begin{bmatrix}0 & 1 & 0\end{bmatrix}$	$\begin{bmatrix}-1 & 0 & 0\end{bmatrix}$	$\begin{bmatrix}-(d_l+d_k)\\d_l\\d_k\end{bmatrix}$	$\begin{bmatrix}-d_k & d_l & 0\end{bmatrix}$
$[210^o,270^o]$	5	$(\omega_i t+\theta_i)-210^o$	$\begin{bmatrix}-1\\0\\1\end{bmatrix}$	$\begin{bmatrix}0\\-1\\1\end{bmatrix}$	$\begin{bmatrix}-1 & 0 & 0\end{bmatrix}$	$\begin{bmatrix}0 & 0 & 1\end{bmatrix}$	$\begin{bmatrix}-d_l\\-d_k\\d_l+d_k\end{bmatrix}$	$\begin{bmatrix}-d_l & 0 & d_k\end{bmatrix}$
$[270^o,330^o]$	6	$(\omega_i t+\theta_i)-270^o$	$\begin{bmatrix}0\\-1\\1\end{bmatrix}$	$\begin{bmatrix}1\\-1\\0\end{bmatrix}$	$\begin{bmatrix}0 & 0 & 1\end{bmatrix}$	$\begin{bmatrix}0 & -1 & 0\end{bmatrix}$	$\begin{bmatrix}d_k\\-(d_l+d_k)\\d_l\end{bmatrix}$	$\begin{bmatrix}0 & -d_k & d_l\end{bmatrix}$

Table 9.2: Output-Side Space Vectors

$\omega_o t+\theta_o$	s	ϕ_o	$[V_n]$	$[V_m]$	$[I_n]$	$[I_m]$	$[d_o V_o]$	$[d_o I_o]$
$[-30^o,30^o]$	1	$(\omega_o t+\theta_o)+30^o$	$\begin{bmatrix}1\\-1\\0\end{bmatrix}$	$\begin{bmatrix}1\\0\\-1\end{bmatrix}$	$\begin{bmatrix}0 & 1 & 0\end{bmatrix}$	$\begin{bmatrix}-1 & 0 & 0\end{bmatrix}$	$\begin{bmatrix}d_n+d_m\\-d_n\\-d_m\end{bmatrix}$	$\begin{bmatrix}-d_m & d_n & 0\end{bmatrix}$
$[30^o,90^o]$	2	$(\omega_o t+\theta_o)-30^o$	$\begin{bmatrix}1\\0\\-1\end{bmatrix}$	$\begin{bmatrix}0\\1\\-1\end{bmatrix}$	$\begin{bmatrix}-1 & 0 & 0\end{bmatrix}$	$\begin{bmatrix}0 & 0 & 1\end{bmatrix}$	$\begin{bmatrix}d_n\\d_m\\-(d_n+d_m)\end{bmatrix}$	$\begin{bmatrix}-d_n & 0 & d_m\end{bmatrix}$
$[90^o,150^o]$	3	$(\omega_o t+\theta_o)-90^o$	$\begin{bmatrix}0\\1\\-1\end{bmatrix}$	$\begin{bmatrix}-1\\1\\0\end{bmatrix}$	$\begin{bmatrix}0 & 0 & 1\end{bmatrix}$	$\begin{bmatrix}0 & -1 & 0\end{bmatrix}$	$\begin{bmatrix}-d_m\\d_n+d_m\\-d_n\end{bmatrix}$	$\begin{bmatrix}0 & -d_m & d_n\end{bmatrix}$
$[150^o,210^o]$	4	$(\omega_o t+\theta_o)-150^o$	$\begin{bmatrix}-1\\1\\0\end{bmatrix}$	$\begin{bmatrix}-1\\0\\1\end{bmatrix}$	$\begin{bmatrix}0 & -1 & 0\end{bmatrix}$	$\begin{bmatrix}1 & 0 & 0\end{bmatrix}$	$\begin{bmatrix}-(d_n+d_m)\\d_n\\d_m\end{bmatrix}$	$\begin{bmatrix}d_m & -d_n & 0\end{bmatrix}$
$[210^o,270^o]$	5	$(\omega_o t+\theta_o)-210^o$	$\begin{bmatrix}-1\\0\\1\end{bmatrix}$	$\begin{bmatrix}0\\-1\\1\end{bmatrix}$	$\begin{bmatrix}1 & 0 & 0\end{bmatrix}$	$\begin{bmatrix}0 & 0 & -1\end{bmatrix}$	$\begin{bmatrix}-d_n\\-d_m\\d_n+d_m\end{bmatrix}$	$\begin{bmatrix}d_n & 0 & -d_m\end{bmatrix}$
$[270^o,330^o]$	6	$(\omega_o t+\theta_o)-270^o$	$\begin{bmatrix}0\\-1\\1\end{bmatrix}$	$\begin{bmatrix}1\\-1\\0\end{bmatrix}$	$\begin{bmatrix}0 & 0 & -1\end{bmatrix}$	$\begin{bmatrix}0 & 1 & 0\end{bmatrix}$	$\begin{bmatrix}d_m\\-(d_n+d_m)\\d_n\end{bmatrix}$	$\begin{bmatrix}0 & d_m & -d_n\end{bmatrix}$

9.4 Derivation of the Matrix Converter Differential Equations

In the following subsections, differential equations of the matrix converter are derived to get a state-space model. The subsections are divided into three parts: derivation of the differential equations of the input side, derivation of the differential equations of the output side, and derivation of the differential equation inside the converter.

9.4.1 Input Side

With reference to Fig. 9.1, Kirchhoff's voltage law around the input side of the terminal shows that

$$\begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \left(L_i \frac{d}{dt} \begin{bmatrix} i_A(t) \\ i_B(t) \\ i_C(t) \end{bmatrix} + R_i \begin{bmatrix} i_A(t) \\ i_B(t) \\ i_C(t) \end{bmatrix} \right) = \begin{bmatrix} v_{AB}(t) \\ v_{BC}(t) \\ v_{CA}(t) \end{bmatrix} - v_{cap}(t)[d_i V_i(t)] . \tag{9.18}$$

Note that

$$\left\langle v_{cap}(t)[d_i V_i(t)] \right\rangle = \begin{vmatrix} v_{A'B'}(t) \\ v_{B'C'}(t) \\ v_{C'A'}(t) \end{vmatrix} = \text{Equation (9.4)}$$

Rewriting Eq. (9.18) in the *stationary dq*0 frame leads to the following:

$$\begin{aligned} &[g](L_i(\frac{d}{dt}[T_{2ABC}]) \begin{bmatrix} i_{di}(t) \\ i_{qi}(t) \\ i_{0i}(t) \end{bmatrix} + L_i[T_{2ABC}] \frac{d}{dt} \begin{bmatrix} i_{di}(t) \\ i_{qi}(t) \\ i_{0i}(t) \end{bmatrix} + R_i[T_{2ABC}] \begin{bmatrix} i_{di}(t) \\ i_{qi}(t) \\ i_{0i}(t) \end{bmatrix}) \\ &= [T_{2ABC}](\begin{bmatrix} V_{di} \\ V_{qi} \\ V_{oi} \end{bmatrix} - v_{cap}(t) \begin{bmatrix} d_{di}(t) \\ d_{qi}(t) \\ d_{0i}(t) \end{bmatrix}) \end{aligned} \tag{9.19}$$

where

$$[g] = \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \tag{9.20}$$

$$\begin{bmatrix} V_{di} \\ V_{qi} \\ V_{oi} \end{bmatrix} = [T_{2dqi}] \begin{bmatrix} v_{AB}(t) \\ v_{BC}(t) \\ v_{CA}(t) \end{bmatrix} = \frac{3}{2} V_{im} \begin{bmatrix} 1 \\ 0 \\ 0 \end{bmatrix} \tag{9.21}$$

$$\begin{bmatrix} d_{di}(t) \\ d_{qi}(t) \\ d_{0i}(t) \end{bmatrix} = [T_{2dqi}][d_i V_i(t)]. \tag{9.22}$$

From Table 9.1, multiplication of $[T_{2dqi}]$ by the six possible $[d_i V_i]$ gives the same result:

$$\begin{bmatrix} d_{di}(t) \\ d_{qi}(t) \\ d_{0i}(t) \end{bmatrix} = [T_{2dqi}][d_i V_i] = \frac{3}{2} m_i \begin{bmatrix} \cos(\theta_i(t)) \\ \sin(\theta_i(t)) \\ 0 \end{bmatrix} \tag{9.23}$$

$$[T_{2dqi}] = \begin{bmatrix} \cos(\omega_i t) & \cos(\omega_i t - \frac{2\pi}{3}) & \cos(\omega_i t - \frac{4\pi}{3}) \\ -\sin(\omega_i t) & -\sin(\omega_i t - \frac{2\pi}{3}) & -\sin(\omega_i t - \frac{4\pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \tag{9.24}$$

$$[T_{2ABC}] = \frac{2}{3} \begin{bmatrix} \cos(\omega_i t) & -\sin(\omega_i t) & 1 \\ \cos(\omega_i t - \frac{2\pi}{3}) & -\sin(\omega_i t - \frac{2\pi}{3}) & 1 \\ \cos(\omega_i t - \frac{4\pi}{3}) & -\sin(\omega_i t - \frac{4\pi}{3}) & 1 \end{bmatrix} \tag{9.25}$$

$$[T_{2ABC}] \times [T_{2dqi}] = [T_{2dqi}] \times [T_{2ABC}] = [I] \tag{9.26}$$

$$\frac{d}{dt}[T_{2ABC}] = \frac{2}{3} \omega_i \begin{bmatrix} -\sin(\omega_i t) & -\cos(\omega_i t) & 0 \\ -\sin(\omega_i t - \frac{2\pi}{3}) & -\cos(\omega_i t - \frac{2\pi}{3}) & 0 \\ -\sin(\omega_i t - \frac{4\pi}{3}) & -\cos(\omega_i t - \frac{4\pi}{3}) & 0 \end{bmatrix}. \tag{9.27}$$

Multiplying both sides of Eq. (9.19) by $[T_{2dqi}]$ leads to

$$\begin{aligned}
&\frac{\sqrt{3}}{2}L_i\left(\begin{bmatrix} -\omega_i & -\sqrt{3}\omega_i & 0 \\ \sqrt{3}\omega_i & -\omega_i & 0 \\ 0 & 0 & 0 \end{bmatrix}\begin{bmatrix} i_{di}(t) \\ i_{qi}(t) \\ i_{0i}(t) \end{bmatrix} + \begin{bmatrix} \sqrt{3} & -1 & 0 \\ 1 & \sqrt{3} & 0 \\ 0 & 0 & 0 \end{bmatrix}\frac{d}{dt}\begin{bmatrix} i_{di}(t) \\ i_{qi}(t) \\ i_{0i}(t) \end{bmatrix}\right) \\
&= -\frac{\sqrt{3}}{2}R_i\begin{bmatrix} \sqrt{3} & -1 & 0 \\ 1 & \sqrt{3} & 0 \\ 0 & 0 & 0 \end{bmatrix}\begin{bmatrix} i_{di}(t) \\ i_{qi}(t) \\ i_{0i}(t) \end{bmatrix} + \left(\begin{bmatrix} \frac{3}{2}V_{im} \\ 0 \\ 0 \end{bmatrix} - \frac{3}{2}m_i(t)v_{cap}(t)\begin{bmatrix} \cos(\theta_i(t)) \\ \sin(\theta_i(t)) \\ 0 \end{bmatrix}\right)
\end{aligned} \tag{9.28}$$

The zero-sequence terms are all zero, hence can be ignored. Upon collecting like terms, we obtain the following:

$$\begin{aligned}
&\frac{\sqrt{3}}{2}L_i\begin{bmatrix} \sqrt{3} & -1 \\ 1 & \sqrt{3} \end{bmatrix}\frac{d}{dt}\begin{bmatrix} i_{di}(t) \\ i_{qi}(t) \end{bmatrix} \\
&= \left(-\frac{\sqrt{3}}{2}R_i\begin{bmatrix} \sqrt{3} & -1 \\ 1 & \sqrt{3} \end{bmatrix} + \frac{\sqrt{3}}{2}L_i\omega_i\begin{bmatrix} 1 & \sqrt{3} \\ -\sqrt{3} & 1 \end{bmatrix}\right)\begin{bmatrix} i_{di}(t) \\ i_{qi}(t) \end{bmatrix} \\
&+ \left(\begin{bmatrix} \frac{3}{2}V_{im} \\ 0 \end{bmatrix} - \frac{3}{2}m_i(t)v_{cap}(t)\begin{bmatrix} \cos(\theta_i(t)) \\ \sin(\theta_i(t)) \end{bmatrix}\right)
\end{aligned} \tag{9.29}$$

We now solve for $L_i\frac{d}{dt}\begin{bmatrix} i_{di}(t) \\ i_{qi}(t) \end{bmatrix}$:

$$\begin{aligned}
&L_i\frac{d}{dt}\begin{bmatrix} i_{di}(t) \\ i_{qi}(t) \end{bmatrix} \\
&= \begin{bmatrix} -R_i & L_i\omega_i \\ -L_i\omega_i & -R_i \end{bmatrix}\begin{bmatrix} i_{di}(t) \\ i_{qi}(t) \end{bmatrix} \\
&+ \begin{bmatrix} \frac{1}{2} & \frac{1}{2\sqrt{3}} \\ -\frac{1}{2\sqrt{3}} & \frac{1}{2} \end{bmatrix}\left(\begin{bmatrix} \frac{3}{2}V_{im} \\ 0 \end{bmatrix} - \frac{3}{2}m_i(t)v_{cap}(t)\begin{bmatrix} \cos(\theta_i(t)) \\ \sin(\theta_i(t)) \end{bmatrix}\right)
\end{aligned} \tag{9.30}$$

Define a *dq* input control $\begin{bmatrix} \gamma_{di}(t) \\ \gamma_{qi}(t) \end{bmatrix}$ such that

$$\begin{bmatrix} \gamma_{di}(t) \\ \gamma_{qi}(t) \end{bmatrix} = \frac{3}{2} m_i(t) \begin{bmatrix} \cos(\theta_i(t) - \frac{\pi}{6}) \\ \sin(\theta_i(t) - \frac{\pi}{6}) \end{bmatrix} \tag{9.31}$$

Equation (9.30) can finally be written as

$$L_i \frac{d}{dt} \begin{bmatrix} i_{di}(t) \\ i_{qi}(t) \end{bmatrix} = \begin{bmatrix} -R_i & L_i\omega_i \\ -L_i\omega_i & -R_i \end{bmatrix} \begin{bmatrix} i_{di}(t) \\ i_{qi}(t) \end{bmatrix} + V_{im} \begin{bmatrix} \frac{3}{4} \\ -\frac{\sqrt{3}}{4} \end{bmatrix} - \frac{v_{cap}(t)}{\sqrt{3}} \begin{bmatrix} \gamma_{di}(t) \\ \gamma_{qi}(t) \end{bmatrix} \tag{9.32}$$

Equation (9.32) consists of two differential equations that describe the input side of the matrix converter.

9.4.2 Output Side

Analysis similar to the above can be applied to the output side. Specifically,

$$[g](L_o \frac{d}{dt}\begin{bmatrix} i_a(t) \\ i_b(t) \\ i_c(t) \end{bmatrix} + R_o \begin{bmatrix} i_a(t) \\ i_b(t) \\ i_c(t) \end{bmatrix}) = v_{cap}(t)[d_o V_o(t)] - \begin{bmatrix} v_{ab}(t) \\ v_{bc}(t) \\ v_{ca}(t) \end{bmatrix} \tag{9.33}$$

Note that

$$\left\langle v_{cap}[d_o V_o(t)] \right\rangle = \begin{vmatrix} v_{a'b'}(t) \\ v_{b'c'}(t) \\ v_{c'a'}(t) \end{vmatrix} = \text{Equation (9.7)}$$

which are the voltages across the output terminals of the converter. Transferring Eq. (9.33) into the *stationary dq*0 frame yields

$$\begin{aligned} &[g](L_o(\frac{d}{dt}[T_{2abc}])\begin{bmatrix} i_{do}(t) \\ i_{qo}(t) \\ i_{0o}(t) \end{bmatrix} + L_o[T_{2abc}]\frac{d}{dt}\begin{bmatrix} i_{do}(t) \\ i_{qo}(t) \\ i_{0o}(t) \end{bmatrix} + R_o[T_{2abc}]\begin{bmatrix} i_{do}(t) \\ i_{qo}(t) \\ i_{0o}(t) \end{bmatrix}) \\ &= [T_{2abc}](v_{cap}\begin{bmatrix} d_{do}(t) \\ d_{qo}(t) \\ d_{0o}(t) \end{bmatrix} - \begin{bmatrix} V_{do} \\ V_{qo} \\ V_{0o} \end{bmatrix}) \end{aligned} \tag{9.34}$$

where

$$\begin{bmatrix} V_{do} \\ V_{qo} \\ V_{0o} \end{bmatrix} = [T_{2dqo}]\begin{bmatrix} v_{ab}(t) \\ v_{bc}(t) \\ v_{ca}(t) \end{bmatrix} = \frac{3}{2}V_{om}\begin{bmatrix} 1 \\ 0 \\ 0 \end{bmatrix} \tag{9.35}$$

$$\begin{bmatrix} d_{do}(t) \\ d_{qo}(t) \\ d_{0o}(t) \end{bmatrix} = [T_{2dqo}][d_o V_o(t)] \tag{9.36}$$

From Table 9.2, multiplying $[T_{2dqo}]$ by the six possible $[d_o V_o(t)]$ gives the same result:

$$[T_{2dqo}][d_o V_o(t)] = \frac{3}{2}m_o(t)\begin{bmatrix} \cos(\theta_o(t)) \\ \sin(\theta_o(t)) \\ 0 \end{bmatrix} \tag{9.37}$$

$$[T_{2dqo}] = \begin{bmatrix} \cos(\omega_o t) & \cos(\omega_o t + \frac{2\pi}{3}) & \cos(\omega_o t + \frac{4\pi}{3}) \\ -\sin(\omega_o t) & -\sin(\omega_o t + \frac{2\pi}{3}) & -\sin(\omega_o t + \frac{4\pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \tag{9.38}$$

$$[T_{2abc}] = \frac{2}{3}\begin{bmatrix} \cos(\omega_o t) & -\sin(\omega_o t) & 1 \\ \cos(\omega_o t + \frac{2\pi}{3}) & -\sin(\omega_o t + \frac{2\pi}{3}) & 1 \\ \cos(\omega_o t + \frac{4\pi}{3}) & -\sin(\omega_o t + \frac{4\pi}{3}) & 1 \end{bmatrix} \tag{9.39}$$

$$[T_{2\,abc}] \times [T_{2\,dqo}] = [T_{2\,dqo}] \times [T_{2\,abc}] = [I] \tag{9.40}$$

$$\frac{d}{dt}[T_{2abc}] = \frac{2}{3}\omega_o \begin{bmatrix} -\sin(\omega_o t) & -\cos(\omega_o t) & 0 \\ -\sin(\omega_o t - \frac{2\pi}{3}) & -\cos(\omega_o t - \frac{2\pi}{3}) & 0 \\ -\sin(\omega_o t - \frac{4\pi}{3}) & -\cos(\omega_o t - \frac{4\pi}{3}) & 0 \end{bmatrix} \tag{9.41}$$

Now, multiply Eq. (9.34) by $[T_{2dqo}]$ to obtain

$$\begin{aligned} &\frac{\sqrt{3}}{2}L_o\left(\begin{bmatrix} -\omega_o & -\sqrt{3}\omega_o & 0 \\ \sqrt{3}\omega_o & -\omega_o & 0 \\ 0 & 0 & 0 \end{bmatrix}\begin{bmatrix} i_{do}(t) \\ i_{qo}(t) \\ i_{0o}(t) \end{bmatrix} + \begin{bmatrix} \sqrt{3} & -1 & 0 \\ 1 & \sqrt{3} & 0 \\ 0 & 0 & 0 \end{bmatrix}\frac{d}{dt}\begin{bmatrix} i_{do}(t) \\ i_{qo}(t) \\ i_{0o}(t) \end{bmatrix}\right) \\ &= -\frac{\sqrt{3}}{2}R_o\begin{bmatrix} \sqrt{3} & -1 & 0 \\ 1 & \sqrt{3} & 0 \\ 0 & 0 & 0 \end{bmatrix}\begin{bmatrix} i_{do}(t) \\ i_{qo}(t) \\ i_{0o}(t) \end{bmatrix} + \left(\frac{3}{2}m_o(t)v_{cap}(t)\begin{bmatrix} \cos(\theta_o(t)) \\ \sin(\theta_o(t)) \\ 0 \end{bmatrix} - \begin{bmatrix} \frac{3}{2}V_{om} \\ 0 \\ 0 \end{bmatrix}\right) \end{aligned} \tag{9.42}$$

After the zero-sequence terms are neglected, Eq. (9.42) becomes

$$\begin{aligned}
&\frac{\sqrt{3}}{2}L_o\begin{bmatrix}\sqrt{3} & -1\\ 1 & \sqrt{3}\end{bmatrix}\frac{d}{dt}\begin{bmatrix}i_{do}(t)\\ i_{qo}(t)\end{bmatrix}\\
&=\left(-\frac{\sqrt{3}}{2}R_o\begin{bmatrix}\sqrt{3} & -1\\ 1 & \sqrt{3}\end{bmatrix}+\frac{\sqrt{3}}{2}L_o\omega_o\begin{bmatrix}1 & \sqrt{3}\\ -\sqrt{3} & 1\end{bmatrix}\right)\begin{bmatrix}i_{do}(t)\\ i_{qo}(t)\end{bmatrix}\\
&+\left(\frac{3}{2}m_o(t)v_{cap}(t)\begin{bmatrix}\cos(\theta_o(t))\\ \sin(\theta_o(t))\end{bmatrix}-\begin{bmatrix}\frac{3}{2}V_{om}\\ 0\end{bmatrix}\right)
\end{aligned} \tag{9.43}$$

Solving for $L_o\frac{d}{dt}\begin{bmatrix}i_{do}(t)\\ i_{qo}(t)\end{bmatrix}$ yields

$$\begin{aligned}
&L_o\frac{d}{dt}\begin{bmatrix}i_{do}(t)\\ i_{qo}(t)\end{bmatrix}\\
&=\begin{bmatrix}-R_o & L_o\omega_o\\ -L_o\omega_o & -R_o\end{bmatrix}\begin{bmatrix}i_{do}(t)\\ i_{qo}(t)\end{bmatrix}\\
&+\begin{bmatrix}\frac{1}{2} & \frac{1}{2\sqrt{3}}\\ -\frac{1}{2\sqrt{3}} & \frac{1}{2}\end{bmatrix}\left(\frac{3}{2}m_o(t)v_{cap}(t)\begin{bmatrix}\cos(\theta_o(t))\\ \sin(\theta_o(t))\end{bmatrix}-\begin{bmatrix}\frac{3}{2}V_{om}\\ 0\end{bmatrix}\right)
\end{aligned} \tag{9.44}$$

Now, define a *dq* control for the output, $\begin{bmatrix}\gamma_{do}(t)\\ \gamma_{qo}(t)\end{bmatrix}$, such that

$$\begin{bmatrix}\gamma_{do}(t)\\ \gamma_{qo}(t)\end{bmatrix}=\frac{3}{2}m_o(t)\begin{bmatrix}\cos(\theta_o(t)-\frac{\pi}{6})\\ \sin(\theta_o(t)-\frac{\pi}{6})\end{bmatrix} \tag{9.45}$$

Equation (9.44) can finally be written as

$$L_o\frac{d}{dt}\begin{bmatrix}i_{do}(t)\\ i_{qo}(t)\end{bmatrix}=\begin{bmatrix}-R_o & L_o\omega_o\\ -L_o\omega_o & -R_o\end{bmatrix}\begin{bmatrix}i_{do}(t)\\ i_{qo}(t)\end{bmatrix}+V_{om}\begin{bmatrix}-\frac{3}{4}\\ \frac{\sqrt{3}}{4}\end{bmatrix}+\frac{v_{cap}(t)}{\sqrt{3}}\begin{bmatrix}\gamma_{do}(t)\\ \gamma_{qo}(t)\end{bmatrix} \tag{9.46}$$

Equation (9.46) contains the two differential equations that describe the output side of the matrix converter.

9.4.3 Internal Capacitor Equations

By using *Kirchhoff's current law* and noting that currents flow from the input side through the converter to the output side, we can show that the current flowing into the capacitor is as follows:

$$C\frac{d}{dt}v_{cap}(t) = [d_i I_i(t)]\begin{bmatrix} i_A(t) \\ i_B(t) \\ i_C(t) \end{bmatrix} + [d_o I_o(t)]\begin{bmatrix} i_a(t) \\ i_b(t) \\ i_c(t) \end{bmatrix} \tag{9.47}$$

where $[d_i I_i(t)]$ and $[d_o I_o(t)]$ are defined in Eq. (9.17) and the input and output currents are defined in Eqs. (9.3) and (9.8), respectively. Multiplying the six possible $[d_i I_i(t)]$ values from Table 9.1 by Eq. (9.3) gives the same result:

$$[d_i I_i(t)]\begin{bmatrix} i_A(t) \\ i_B(t) \\ i_C(t) \end{bmatrix} = \frac{\sqrt{3}}{2} i_{im}(t) m_i(t) \cos(\theta_i(t) - \theta_{pfi}(t)) . \tag{9.48}$$

The same applies for the output side. That is, multiplying the six possible $[d_o I_o(t)]$ values from Table 9.2 by Eq. (9.8) gives

$$[d_o I_o(t)]\begin{bmatrix} i_a(t) \\ i_b(t) \\ i_c(t) \end{bmatrix} = -\frac{\sqrt{3}}{2} i_{om}(t) m_o(t) \cos(\theta_o(t) - \theta_{pfo}(t)) . \tag{9.49}$$

Equation (9.47) then becomes

$$C\frac{d}{dt}v_{cap}(t) = \frac{\sqrt{3}}{2} i_{im}(t) m_i(t) \cos(\theta_i(t) - \theta_{pfi}(t)) - \frac{\sqrt{3}}{2} i_{om}(t) m_o(t) \cos(\theta_o(t) - \theta_{pfo}(t)) . \tag{9.50}$$

By using the following trigonometric identity

$$\cos(x \pm y) = \cos(x)\cos(y) \mp \sin(x)\sin(y) = \begin{bmatrix} \cos(x) & \sin(x) \end{bmatrix}\begin{bmatrix} \cos(y) \\ \sin(y) \end{bmatrix} \tag{9.51}$$

we have the following:

$$\cos(\theta_i(t) - \theta_{pfi}(t)) = \begin{bmatrix} \cos(\theta_i(t)) & \sin(\theta_i(t)) \end{bmatrix}\begin{bmatrix} \cos(\theta_{pfi}(t)) \\ \sin(\theta_{pfi}(t)) \end{bmatrix} \tag{9.52}$$

for the input side and

$$\cos(\theta_o(t)-\theta_{pfo}(t))=\begin{bmatrix}\cos(\theta_o(t)) & \sin(\theta_o(t))\end{bmatrix}\begin{bmatrix}\cos(\theta_{pfo}(t))\\ \sin(\theta_{pfo}(t))\end{bmatrix} \tag{9.53}$$

for the output side. Now, the input currents in the $dq0$ frame are, by use of $[T_{2dqi}]$ of Eq. (9.24) and

$\begin{bmatrix} i_A(t)\\ i_B(t)\\ i_C(t)\end{bmatrix}$ of Eq. (9.3)

$$\begin{bmatrix} i_{di}(t)\\ i_{qi}(t)\\ i_{0i}(t)\end{bmatrix}=[T_{2dqi}]\begin{bmatrix} i_A(t)\\ i_B(t)\\ i_C(t)\end{bmatrix}$$

$$=i_{im}(t)\begin{bmatrix}\cos(\omega_i t) & \cos(\omega_i t-\frac{2\pi}{3}) & \cos(\omega_i t-\frac{4\pi}{3})\\ -\sin(\omega_i t) & -\sin(\omega_i t-\frac{2\pi}{3}) & -\sin(\omega_i t-\frac{4\pi}{3})\\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2}\end{bmatrix}\times\begin{bmatrix}\cos(\omega_i t+\theta_{pfi}(t)-30^o)\\ \cos(\omega_i t+\theta_{pfi}(t)-30^o-120^o)\\ \cos(\omega_i t+\theta_{pfi}(t)-30^o+120^o)\end{bmatrix}$$

$$\begin{bmatrix} i_{di}(t)\\ i_{qi}(t)\\ i_{0i}(t)\end{bmatrix}=\frac{3}{2}i_{im}(t)\begin{bmatrix}\cos(\theta_{pfi}(t)-\frac{\pi}{6})\\ \sin(\theta_{pfi}(t)-\frac{\pi}{6})\\ 0\end{bmatrix} \tag{9.54}$$

By using $[T_{2dqo}]$ of Eq. (9.38) and $\begin{bmatrix} i_a(t)\\ i_b(t)\\ i_c(t)\end{bmatrix}$ of Eq. (9.8), the output currents in the $dq0$ frame are as follows:

$$\begin{bmatrix} i_{do}(t) \\ i_{qo}(t) \\ i_{0o}(t) \end{bmatrix} = [T_{2dqo}] \begin{bmatrix} i_a(t) \\ i_b(t) \\ i_c(t) \end{bmatrix}$$

$$= i_{om}(t) \begin{bmatrix} \cos(\omega_o t) & \cos(\omega_o t - \frac{2\pi}{3}) & \cos(\omega_o t - \frac{4\pi}{3}) \\ -\sin(\omega_o t) & -\sin(\omega_o t - \frac{2\pi}{3}) & -\sin(\omega_o t - \frac{4\pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \times \begin{bmatrix} \cos(\omega_o t + \theta_{pfo}(t) - 30^o) \\ \cos(\omega_o t + \theta_{pfo}(t) - 30^o - 120^o) \\ \cos(\omega_o t + \theta_{pfo}(t) - 30^o + 120^o) \end{bmatrix}$$

$$\begin{bmatrix} i_{do}(t) \\ i_{qo}(t) \\ i_{0o}(t) \end{bmatrix} = \frac{3}{2} i_{om}(t) \begin{bmatrix} \cos(\theta_{pfo}(t) - \frac{\pi}{6}) \\ \sin(\theta_{pfo}(t) - \frac{\pi}{6}) \\ 0 \end{bmatrix} \tag{9.55}$$

Now consider Eq. (9.52). Take only the $\theta_{pfi}(t)$ vector of that equation:

$$\begin{bmatrix} \cos(\theta_{pfi}(t)) \\ \sin(\theta_{pfi}(t)) \end{bmatrix} = \begin{bmatrix} \cos(\theta_{pfi}(t) - \frac{\pi}{6} + \frac{\pi}{6}) \\ \sin(\theta_{pfi}(t) - \frac{\pi}{6} + \frac{\pi}{6}) \end{bmatrix}. \tag{9.56}$$

By using the trigonometric identity of Eq. (9.51) and the following trigonometric identity, we obtain

$$\sin(x \pm y) = \cos(y)\sin(x) \pm \sin(y)\cos(x) = \begin{bmatrix} \sin(y) & \cos(y) \end{bmatrix} \begin{bmatrix} \cos(x) \\ \sin(x) \end{bmatrix} \tag{9.57}$$

in Eq. (9.56), with $(x = \theta_{pfi}(t) - \frac{\pi}{6})$ and $(y = \frac{\pi}{6})$. Eq. (9.56) becomes:

$$\begin{bmatrix} \cos((\theta_{pfi}(t) - \frac{\pi}{6}) + \frac{\pi}{6}) \\ \sin((\theta_{pfi}(t) - \frac{\pi}{6}) + \frac{\pi}{6}) \end{bmatrix} = \begin{bmatrix} \cos(\theta_{pfi}(t) - \frac{\pi}{6})\cos(\frac{\pi}{6}) - \sin(\theta_{pfi}(t) - \frac{\pi}{6})\sin(\frac{\pi}{6}) \\ \cos(\theta_{pfi}(t) - \frac{\pi}{6})\sin(\frac{\pi}{6}) + \sin(\theta_{pfi}(t) - \frac{\pi}{6})\cos(\frac{\pi}{6}) \end{bmatrix}$$

$$= \begin{bmatrix} \cos(\frac{\pi}{6}) & -\sin(\frac{\pi}{6}) \\ \sin(\frac{\pi}{6}) & \cos(\frac{\pi}{6}) \end{bmatrix} \begin{bmatrix} \cos(\theta_{pfi}(t) - \frac{\pi}{6}) \\ \sin(\theta_{pfi}(t) - \frac{\pi}{6}) \end{bmatrix} \tag{9.58}$$

Substitute the results of Eq. (9.58) into Eq. (9.52) to obtain the following:

$$\cos(\theta_i(t)-\theta_{pfi}(t))=\begin{bmatrix}\cos(\theta_i(t)) & \sin(\theta_i(t))\end{bmatrix}\begin{bmatrix}\cos(\frac{\pi}{6}) & -\sin(\frac{\pi}{6})\\ \sin(\frac{\pi}{6}) & \cos(\frac{\pi}{6})\end{bmatrix}\begin{bmatrix}\cos(\theta_{pfi}(t)-\frac{\pi}{6})\\ \sin(\theta_{pfi}(t)-\frac{\pi}{6})\end{bmatrix} \tag{9.59}$$

Now, consider the first vector and matrix in Eq. (9.59). Using the same trigonometric identities of Eqs. (9.51) and (9.57) leads to

$$\begin{aligned}&\begin{bmatrix}\cos(\theta_i(t)) & \sin(\theta_i(t))\end{bmatrix}\begin{bmatrix}\cos(\frac{\pi}{6}) & -\sin(\frac{\pi}{6})\\ \sin(\frac{\pi}{6}) & \cos(\frac{\pi}{6})\end{bmatrix}\\ &=\begin{bmatrix}\cos(\theta_i(t))\cos(\frac{\pi}{6})+\sin(\theta_i(t))\sin(\frac{\pi}{6})\\ -\cos(\theta_i(t))\sin(\frac{\pi}{6})+\sin(\theta_i(t))\cos(\frac{\pi}{6})\end{bmatrix}^T\\ &=\begin{bmatrix}\cos(\theta_i(t)-\frac{\pi}{6}) & \sin(\theta_i(t)-\frac{\pi}{6})\end{bmatrix}\end{aligned} \tag{9.60}$$

Now, Eq. (9.52) can be written as

$$\cos(\theta_i(t)-\theta_{pfi}(t))=\begin{bmatrix}\cos(\theta_i(t)-\frac{\pi}{6}) & \sin(\theta_i(t)-\frac{\pi}{6})\end{bmatrix}\begin{bmatrix}\cos(\theta_{pfi}(t)-\frac{\pi}{6})\\ \sin(\theta_{pfi}(t)-\frac{\pi}{6})\end{bmatrix}. \tag{9.61}$$

The same analysis applies to the output side. Equation (9.53) becomes

$$\cos(\theta_o(t)-\theta_{pfo}(t))=\begin{bmatrix}\cos(\theta_o(t)-\frac{\pi}{6}) & \sin(\theta_o(t)-\frac{\pi}{6})\end{bmatrix}\begin{bmatrix}\cos(\theta_{pfo}(t)-\frac{\pi}{6})\\ \sin(\theta_{pfo}(t)-\frac{\pi}{6})\end{bmatrix}. \tag{9.62}$$

Substitution of Eqs. (9.61) and (9.62) into Eq. (9.50) causes the capacitor current equation to become

$$\begin{aligned}&C\frac{d}{dt}v_{cap}(t)\\ &=\frac{2}{3\sqrt{3}}\begin{bmatrix}\frac{3}{2}m_i(t)\cos(\theta_i(t)-\frac{\pi}{6}) & \frac{3}{2}m_i(t)\sin(\theta_i(t)-\frac{\pi}{6})\end{bmatrix}\begin{bmatrix}\frac{3}{2}i_{im}(t)\cos(\theta_{pfi}(t)-\frac{\pi}{6})\\ \frac{3}{2}i_{im}(t)\sin(\theta_{pfi}(t)-\frac{\pi}{6})\end{bmatrix}\\ &-\frac{2}{3\sqrt{3}}\begin{bmatrix}\frac{3}{2}m_o(t)\cos(\theta_o(t)-\frac{\pi}{6}) & \frac{3}{2}m_o(t)\sin(\theta_o(t)-\frac{\pi}{6})\end{bmatrix}\begin{bmatrix}\frac{3}{2}i_{om}(t)\cos(\theta_{pfo}(t)-\frac{\pi}{6})\\ \frac{3}{2}i_{om}(t)\sin(\theta_{pfo}(t)-\frac{\pi}{6})\end{bmatrix}\end{aligned} \tag{9.63}$$

Using the definition of the input control $\begin{bmatrix}\gamma_{di}(t)\\ \gamma_{qi}(t)\end{bmatrix}$ of Eq. (9.31) and the output control $\begin{bmatrix}\gamma_{do}(t)\\ \gamma_{qo}(t)\end{bmatrix}$ of Eq. (9.45) and using the input and output $dq0$ currents of Eqs. (9.54) and (9.55), respectively, causes Eq. (9.63) to become

$$C\frac{d}{dt}v_{cap}(t)=\frac{2}{3\sqrt{3}}\left(\begin{bmatrix}\gamma_{di}(t) & \gamma_{qi}(t)\end{bmatrix}\begin{bmatrix}i_{di}(t)\\ i_{qi}(t)\end{bmatrix}-\begin{bmatrix}\gamma_{do}(t) & \gamma_{qo}(t)\end{bmatrix}\begin{bmatrix}i_{do}(t)\\ i_{qo}(t)\end{bmatrix}\right). \tag{9.64}$$

Equation (9.64) describes the capacitor voltage dynamics. This is a differential equation that links the input side of the matrix converter to its output side.

9.5 The Nonlinear Differential Equations of the Matrix Converter

Equations (9.32), (9.46), and (9.64) can be combined into the following form:

$$[P]\frac{d}{dt}[x(t)]=[f(t)][x(t)]+[M][n] \tag{9.65}$$

where

$$[P]=\begin{bmatrix}C & 0 & 0 & 0 & 0\\ 0 & L_i & 0 & 0 & 0\\ 0 & 0 & L_i & 0 & 0\\ 0 & 0 & 0 & L_o & 0\\ 0 & 0 & 0 & 0 & L_o\end{bmatrix} \tag{9.66}$$

$$[x(t)]=\begin{bmatrix}v_{cap}(t)\\ i_{di}(t)\\ i_{qi}(t)\\ i_{do}(t)\\ i_{qo}(t)\end{bmatrix} \tag{9.67}$$

$$[f(t)]=\begin{bmatrix}0 & \frac{2}{3\sqrt{3}}\gamma_{di}(t) & \frac{2}{3\sqrt{3}}\gamma_{qi}(t) & \frac{-2}{2\sqrt{3}}\gamma_{do}(t) & \frac{-2}{3\sqrt{3}}\gamma_{qo}(t)\\ \frac{-1}{\sqrt{3}}\gamma_{di}(t) & -R_i & L_i\omega_i & 0 & 0\\ \frac{-1}{\sqrt{3}}\gamma_{qi}(t) & -L_i\omega_i & -R_i & 0 & 0\\ \frac{1}{\sqrt{3}}\gamma_{do}(t) & 0 & 0 & -R_o & L_o\omega_o\\ \frac{1}{\sqrt{3}}\gamma_{qo}(t) & 0 & 0 & -L_o\omega_o & -R_o\end{bmatrix} \tag{9.68}$$

$$[M]=\begin{bmatrix} 0 & 0 \\ \frac{3}{4} & 0 \\ -\frac{\sqrt{3}}{4} & 0 \\ 0 & -\frac{3}{4} \\ 0 & \frac{\sqrt{3}}{4} \end{bmatrix} \tag{9.69}$$

$$[n]=\begin{bmatrix} V_{im} \\ V_{om} \end{bmatrix}. \tag{9.70}$$

This is the nonlinear state space model of the new modular matrix converter. It involves multiplication of time varying variables, which is a nonlinear operation. It is desirable to design a controller to minimize the variations of the converter's parameters. Those variation quantities are embedded in the nonlinear model. To extract them, a technique called *linearization* will be used. Linearizing a nonlinear differential equation will divide it into a nominal part, a 1st-order linear part, and a 2nd-order nonlinear part.

9.5.1 Linearization of the Matrix-Converter Nonlinear Differential Equations

Equation (9.65) is a set of five nonlinear differential equations derived as a first step to design a feedback controller for the novel modular matrix converter. To facilitate design of the controller, those equations will be linearized. That is, we shall assume that each of the five controlled output variables, [*x(t)*], are divided into two parts: nominal values and small perturbation, as follows:

$$[x(t)]=[X]+[\hat{x}(t)]=\begin{bmatrix} V_{cap} \\ I_{di} \\ I_{qi} \\ I_{do} \\ I_{qo} \end{bmatrix}+\begin{bmatrix} \hat{v}_{cap}(t) \\ \hat{i}_{di}(t) \\ \hat{i}_{qi}(t) \\ \hat{i}_{do}(t) \\ \hat{i}_{qo}(t) \end{bmatrix} \tag{9.71}$$

and the same for the control variables:

$$\begin{aligned} \begin{bmatrix} \gamma_{dx}(t) \\ \gamma_{qx}(t) \end{bmatrix} &= \begin{bmatrix} \Gamma_{dx} \\ \Gamma_{qx} \end{bmatrix}+\begin{bmatrix} \hat{\gamma}_{dx}(t) \\ \hat{\gamma}_{qx}(t) \end{bmatrix} \\ &= \frac{3}{2}(M_x+\hat{m}_x(t))\begin{bmatrix} \cos((\Theta_x+\hat{\theta}_x(t))-\frac{\pi}{6}) \\ \sin((\Theta_x+\hat{\theta}_x(t))-\frac{\pi}{6}) \end{bmatrix} \qquad (x=i,o) \end{aligned} \tag{9.72}$$

By using the trigonometric identities (Eqs. [9.51] and [9.57]) on the trigonometric terms in Eq. (9.72), with $x = (\Theta_x - \frac{\pi}{6})$ and $y = (\hat{\theta}_x(t))$, we obtain the following:

$$\begin{bmatrix} \cos((\Theta_x + \hat{\theta}_x(t)) - \frac{\pi}{6}) \\ \sin((\Theta_x + \hat{\theta}_x(t)) - \frac{\pi}{6}) \end{bmatrix} = \begin{bmatrix} \cos(\Theta_x - \frac{\pi}{6})\cos(\hat{\theta}_x(t)) - \sin(\Theta_x - \frac{\pi}{6})\sin(\hat{\theta}_x(t)) \\ \cos(\Theta_x - \frac{\pi}{6})\sin(\hat{\theta}_x(t)) + \sin(\Theta_x - \frac{\pi}{6})\cos(\hat{\theta}_x(t)) \end{bmatrix} \tag{9.73}$$

Now, the trigonometric functions cos(*x*) and sin(*x*) can be written in power series (about $x_0 = 0$) as follows:

$$\begin{aligned} \cos(x) &= 1 - \frac{x^2}{2} + \frac{x^4}{24} - \frac{x^6}{720} + ... \\ \sin(x) &= x - \frac{x^3}{6} + \frac{x^5}{120} - ..... \end{aligned} \tag{9.74}$$

By substituting $x = (\hat{\theta}_x(t))$ in Eq. (9.74), taking only the linear terms (i.e., the first term of each series), and substituting the results into Eq. (9.73), we obtain

$$\begin{bmatrix} \cos((\Theta_x + \hat{\theta}_x(t)) - \frac{\pi}{6}) \\ \sin((\Theta_x + \hat{\theta}_x(t)) - \frac{\pi}{6}) \end{bmatrix} = \begin{bmatrix} \cos(\Theta_x - \frac{\pi}{6}) - \sin(\Theta_x - \frac{\pi}{6})\hat{\theta}_x(t) \\ \cos(\Theta_x - \frac{\pi}{6})\hat{\theta}_x(t) + \sin(\Theta_x - \frac{\pi}{6}) \end{bmatrix} \tag{9.75}$$

Now substitute Eq. (9.75) into Eq. (9.72):

$$\begin{bmatrix} \gamma_{dx}(t) \\ \gamma_{qx}(t) \end{bmatrix} = \frac{3}{2}(M_x + \hat{m}_x(t)) \begin{bmatrix} \cos(\Theta_x - \frac{\pi}{6}) - \sin(\Theta_x - \frac{\pi}{6})\hat{\theta}_x(t) \\ \cos(\Theta_x - \frac{\pi}{6})\hat{\theta}_x(t) + \sin(\Theta_x - \frac{\pi}{6}) \end{bmatrix} \quad (x = i, o) \cdot \tag{9.76}$$

Multiply the terms

$$\begin{bmatrix} \gamma_{dx}(t) \\ \gamma_{qx}(t) \end{bmatrix} = \left(\frac{3}{2} M_x \begin{bmatrix} \cos(\Theta_x - \frac{\pi}{6}) \\ \sin(\Theta_x - \frac{\pi}{6}) \end{bmatrix} \right) + \left(\frac{3}{2} M_x \begin{bmatrix} -\sin(\Theta_x - \frac{\pi}{6}) \\ \cos(\Theta_x - \frac{\pi}{6}) \end{bmatrix} \hat{\theta}_x(t) + \frac{3}{2} \begin{bmatrix} \cos(\Theta_x - \frac{\pi}{6}) \\ \sin(\Theta_x - \frac{\pi}{6}) \end{bmatrix} \hat{m}_x(t) \right) + \left(\frac{3}{2} \begin{bmatrix} -\sin(\Theta_x - \frac{\pi}{6}) \\ \cos(\Theta_x - \frac{\pi}{6}) \end{bmatrix} \hat{m}_x(t) \hat{\theta}_x(t) \right) \tag{9.77}$$

The third term is the 2nd-order nonlinear term and will be neglected in this study. The first term is the *steady-state* control:

$$\begin{bmatrix} \Gamma_{dx} \\ \Gamma_{qx} \end{bmatrix} = \frac{3}{2} M_x \begin{bmatrix} \cos(\Theta_x - \frac{\pi}{6}) \\ \sin(\Theta_x - \frac{\pi}{6}) \end{bmatrix} \qquad (x = i, o) \tag{9.78}$$

The second term is the 1st-order linear term and can be simplified to

$$\begin{bmatrix} \hat{\gamma}_{dx}(t) \\ \hat{\gamma}_{qx}(t) \end{bmatrix} = \begin{bmatrix} -\Gamma_{qx} \\ \Gamma_{dx} \end{bmatrix} \hat{\theta}_x(t) + \begin{bmatrix} \frac{\Gamma_{dx}}{M_x} \\ \frac{\Gamma_{qx}}{M_x} \end{bmatrix} \hat{m}_x(t) \qquad (x = i, o). \tag{9.79}$$

Equation (9.68) can now be written as:

$$[f(t)] = [F] + [\hat{f}(t)] \tag{9.80}$$

where

$$[F]=\begin{bmatrix} 0 & \frac{2}{2\sqrt{3}}\Gamma_{di} & \frac{2}{2\sqrt{3}}\Gamma_{qi} & \frac{-2}{2\sqrt{3}}\Gamma_{do} & \frac{-2}{2\sqrt{3}}\Gamma_{qo} \\ \frac{-1}{\sqrt{3}}\Gamma_{di} & -R_i & L_i\omega_i & 0 & 0 \\ \frac{-1}{\sqrt{3}}\Gamma_{qi} & -L_i\omega_i & -R_i & 0 & 0 \\ \frac{1}{\sqrt{3}}\Gamma_{do} & 0 & 0 & -R_o & L_o\omega_o \\ \frac{1}{\sqrt{3}}\Gamma_{qo} & 0 & 0 & -L_o\omega_o & -R_o \end{bmatrix} \tag{9.81}$$

$$[\hat{f}(t)]=\begin{bmatrix} 0 & \frac{2}{3\sqrt{3}}\hat{\gamma}_{di}(t) & \frac{2}{3\sqrt{3}}\hat{\gamma}_{qi}(t) & \frac{-2}{3\sqrt{3}}\hat{\gamma}_{do}(t) & \frac{-2}{3\sqrt{3}}\hat{\gamma}_{qo}(t) \\ \frac{-1}{\sqrt{3}}\hat{\gamma}_{di}(t) & 0 & 0 & 0 & 0 \\ \frac{-1}{\sqrt{3}}\hat{\gamma}_{qi}(t) & 0 & 0 & 0 & 0 \\ \frac{1}{\sqrt{3}}\hat{\gamma}_{do}(t) & 0 & 0 & 0 & 0 \\ \frac{1}{\sqrt{3}}\hat{\gamma}_{qo}(t) & 0 & 0 & 0 & 0 \end{bmatrix}. \tag{9.82}$$

Substitution of Eqs. (9.71) and (9.80) into Eq. (9.65) yields the converter nonlinear equations:

$$[P]\frac{d}{dt}[x(t)]=([F][X]+[M][n])+\left(\left[\hat{f}(t)\right][X]+[F]\left[\hat{x}(t)\right]\right)+\left(\left[\hat{f}(t)\right]\left[\hat{x}(t)\right]\right) \tag{9.83}$$

which is of the form [6]:

$$\begin{bmatrix}\text{Converter}\\ \text{Equations}\end{bmatrix}=\begin{bmatrix}\text{Steady-State}\\ \text{Equations}\end{bmatrix}+\begin{bmatrix}1^{\text{st}}\text{ order (linear)}\\ \text{Equations}\end{bmatrix}+\begin{bmatrix}2^{\text{nd}}\text{ order (nonlinear)}\\ \text{Equations}\end{bmatrix}.$$

The first term describes the steady-state operating point of the matrix converter. It gives an insight of how the converter behaves given certain input parameters. The second term, which will be rearranged later, represents the linear time-invariant state-space model of the matrix converter. It is a function of the first term (the steady-state model). The third term is a higher-order nonlinear model and will be neglected.

9.5.2 The Steady-State Solution of the Matrix Converter

The nominal part of Eq. (9.83) constitutes the steady-state solution of the matrix converter. After substituting Eqs. (9.71) and (9.81), the nominal part of Eq. (9.83) becomes

$$[P]\frac{d}{dt}[X]=[F][X]+[M][N]=0. \tag{9.84}$$

Equation (9.84) can be divided into three sets of equations: one equation that involves the capacitor current, two equations for the *dq* input side, and two equations for the *dq* output side, as follows:

$$C\frac{d}{dt}V_{cap}=\frac{2}{3\sqrt{3}}\left(\begin{bmatrix}\Gamma_{di} & \Gamma_{qi}\end{bmatrix}\begin{bmatrix}I_{di}\\ I_{qi}\end{bmatrix}-\begin{bmatrix}\Gamma_{do} & \Gamma_{qo}\end{bmatrix}\begin{bmatrix}I_{do}\\ I_{qo}\end{bmatrix}\right)=0 \tag{9.85}$$

$$L_i\frac{d}{dt}\begin{bmatrix}I_{di}\\ I_{qi}\end{bmatrix}=\begin{bmatrix}-R_i & L_i\omega_i\\ -L_i\omega_i & -R_i\end{bmatrix}\begin{bmatrix}I_{di}\\ I_{qi}\end{bmatrix}+\begin{bmatrix}\frac{3}{4} & \frac{-1}{\sqrt{3}}\Gamma_{di}\\ \frac{-\sqrt{3}}{4} & \frac{-1}{\sqrt{3}}\Gamma_{qi}\end{bmatrix}\begin{bmatrix}V_{im}\\ V_{cap}\end{bmatrix}=0 \tag{9.86}$$

$$L_o\frac{d}{dt}\begin{bmatrix}I_{do}\\ I_{qo}\end{bmatrix}=\begin{bmatrix}-R_o & L_o\omega_o\\ -L_o\omega_o & -R_o\end{bmatrix}\begin{bmatrix}I_{do}\\ I_{qo}\end{bmatrix}+\begin{bmatrix}\frac{-3}{4} & \frac{1}{\sqrt{3}}\Gamma_{do}\\ \frac{\sqrt{3}}{4} & \frac{1}{\sqrt{3}}\Gamma_{qo}\end{bmatrix}\begin{bmatrix}V_{om}\\ V_{cap}\end{bmatrix}=0\,. \tag{9.87}$$

Because the filter inductors of both the input and output sides are equal [1, 2, 45], we can simplify and let $L_i = L_o = L$ and $R_i = R_o = R$. Under steady-state operation, the known parameters are as follows:

Recall from Chapter 3 that the input and output modulation indexes are defined in Eq. (3.3) and expressed here as

$$M_x=\frac{2}{3}\frac{\left|v_{x\_ref}\right|}{V_{cap}}\quad (x=i,o) \tag{9.88}$$

where $\left|v_{x\_ref}\right|$ is the magnitude of the *dq*0 vector that represents the three-phase line-to-line voltages across the converter's terminals defined in Eq. (9.4) for the input side and Eq. (9.7) for the output side. Those two vectors are found by multiplying Eq. (9.4) by the transformation matrix defined in Eq. (9.24) for the input side and by multiplying Eq. (9.7) by the transformation defined in Eq. (9.38) for the output side. The answer can be put in a simplified one-vector form:

$$\begin{bmatrix}V_{Tdx}\\ V_{Tqx}\end{bmatrix}=\frac{3}{2}V_{xm'}\begin{bmatrix}\cos(\Theta_x)\\ \sin(\Theta_x)\end{bmatrix}\quad (x=i,o)\,. \tag{9.89}$$

Using Eqs. (9.88), (9.89), and (9.78) for both input and output in Eqs. (9.85-9.87), with additional simplification, leads to the following system of steady-state converter equations:

$$\left(V_{Tdi}+\frac{V_{Tqi}}{\sqrt{3}}\right)I_{di}-\left(\frac{V_{Tdi}}{\sqrt{3}}-V_{Tqi}\right)I_{qi}-\left(V_{Tdo}+\frac{V_{Tqo}}{\sqrt{3}}\right)I_{do}+\left(\frac{V_{Tdo}}{\sqrt{3}}-V_{Tqo}\right)I_{qo}=0 \tag{9.90}$$

$$\frac{3}{4}V_{im}-\frac{1}{2}V_{Tdi}-\frac{1}{2\sqrt{3}}V_{Tqi}-I_{di}R_i+I_{qi}L_i\omega_i=0 \tag{9.91}$$

$$-\frac{\sqrt{3}}{4}V_{im}+\frac{1}{2\sqrt{3}}V_{Tdi}-\frac{1}{2}V_{Tqi}-I_{di}L_i\omega_i-I_{qi}R_i=0 \tag{9.92}$$

$$-\frac{3}{4}V_{om}+\frac{1}{2}V_{Tdo}+\frac{1}{2\sqrt{3}}V_{Tqo}-I_{do}R_o+I_{qo}L_o\omega_o=0 \tag{9.93}$$

$$\frac{\sqrt{3}}{4}V_{om}-\frac{1}{2\sqrt{3}}V_{Tdo}+\frac{1}{2}V_{Tqo}-I_{do}L_o\omega_o-I_{qo}R_o=0 \tag{9.94}$$

The steady-state input currents are transformed into the *dq*0 frame in Eqs. (9.90-9.94) by multiplying Eq. (9.3) by Eq. (9.24), as follows:

$$\begin{bmatrix} I_{di} \\ I_{qi} \\ I_{0i} \end{bmatrix} = [T_{2dqi}] \begin{bmatrix} i_A(t) \\ i_B(t) \\ i_C(t) \end{bmatrix}$$

$$= I_{im} \begin{bmatrix} \cos(\omega_i t) & \cos(\omega_i t-\frac{2\pi}{3}) & \cos(\omega_i t-\frac{4\pi}{3}) \\ -\sin(\omega_i t) & -\sin(\omega_i t-\frac{2\pi}{3}) & -\sin(\omega_i t-\frac{4\pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \times \begin{bmatrix} \cos(\omega_i t+\Theta_{pfi}-30^o) \\ \cos(\omega_i t+\Theta_{pfi}-30^o-120^o) \\ \cos(\omega_i t+\Theta_{pfi}-30^o+120^o) \end{bmatrix}$$

$$\begin{bmatrix} I_{di} \\ I_{qi} \\ I_{0i} \end{bmatrix} = \frac{3}{2} I_{im} \begin{bmatrix} \cos(\Theta_{pfi}-\frac{\pi}{6}) \\ \sin(\Theta_{pfi}-\frac{\pi}{6}) \\ 0 \end{bmatrix} \tag{9.95}$$

In a similar manner, the steady-state output currents are transformed into the *dq*0 frame by multiplying Eq. (9.8) by Eq. (9.38):

$$\begin{bmatrix} I_{do} \\ I_{qo} \\ I_{0o} \end{bmatrix} = [T_{2dqo}] \begin{bmatrix} i_a(t) \\ i_b(t) \\ i_c(t) \end{bmatrix}$$

$$= I_{om} \begin{bmatrix} \cos(\omega_o t) & \cos(\omega_o t - \frac{2\pi}{3}) & \cos(\omega_o t - \frac{4\pi}{3}) \\ -\sin(\omega_o t) & -\sin(\omega_o t - \frac{2\pi}{3}) & -\sin(\omega_o t - \frac{4\pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \times \begin{bmatrix} \cos(\omega_o t + \Theta_{pfo} - 30^o) \\ \cos(\omega_o t + \Theta_{pfo} - 30^o - 120^o) \\ \cos(\omega_o t + \Theta_{pfo} - 30^o + 120^o) \end{bmatrix}$$

$$\begin{bmatrix} I_{do} \\ I_{qo} \\ I_{0o} \end{bmatrix} = \frac{3}{2} I_{om} \begin{bmatrix} \cos(\Theta_{pfo} - \frac{\pi}{6}) \\ \sin(\Theta_{pfo} - \frac{\pi}{6}) \\ 0 \end{bmatrix} \tag{9.96}$$

By substituting Eq. (9.95) for $\begin{bmatrix} I_{di} & I_{qi} \end{bmatrix}^T$ and Eq. (9.96) for $\begin{bmatrix} I_{do} & I_{qo} \end{bmatrix}^T$ in Eqs. (9.90-9.94), we obtain the final steady-state result:

$$\sqrt{3} I_{im} \left(V_{Tdi} \cos\left(\Theta_{pfi}\right) + V_{Tqi} \sin\left(\Theta_{pfi}\right) \right) - \left(V_{Tdo} + \frac{V_{Tqo}}{\sqrt{3}} \right) I_{do} + \left(\frac{V_{Tdo}}{\sqrt{3}} - V_{Tqo} \right) I_{qo} = 0 \tag{9.97}$$

$$\frac{3}{4} V_{im} - \frac{1}{2} V_{Tdi} - \frac{1}{2\sqrt{3}} V_{Tqi} - \frac{3}{2} I_{im} \left(R_i \cos\left(\Theta_{pfi} - \frac{\pi}{6} \right) - L_i \omega_i \sin\left(\Theta_{pfi} - \frac{\pi}{6} \right) \right) = 0 \tag{9.98}$$

$$-\frac{\sqrt{3}}{4} V_{im} + \frac{1}{2\sqrt{3}} V_{Tdi} - \frac{1}{2} V_{Tqi} - \frac{3}{2} I_{im} \left(R_i \sin\left(\Theta_{pfi} - \frac{\pi}{6} \right) + L_i \omega_i \cos\left(\Theta_{pfi} - \frac{\pi}{6} \right) \right) = 0 \tag{9.99}$$

$$-\frac{3}{4} V_{om} + \frac{1}{2} V_{Tdo} + \frac{1}{2\sqrt{3}} V_{Tqo} - \frac{3}{2} I_{om} \left(R_o \cos\left(\Theta_{pfo} - \frac{\pi}{6} \right) - L_o \omega_o \sin\left(\Theta_{pfo} - \frac{\pi}{6} \right) \right) = 0 \tag{9.100}$$

$$\frac{\sqrt{3}}{4} V_{om} - \frac{1}{2\sqrt{3}} V_{Tdo} + \frac{1}{2} V_{Tqo} - \frac{3}{2} I_{om} \left(R_o \sin\left(\Theta_{pfo} - \frac{\pi}{6} \right) + L_o \omega_o \cos\left(\Theta_{pfo} - \frac{\pi}{6} \right) \right) = 0 . \tag{9.101}$$

Equations (9.97-9.101) represent five equations in five unknown variables:

I_{im} : amplitude of the input current.

V_{Tdi}, V_{Tqi} : dq representation of the voltages across the input terminals.

V_{Tdo}, V_{Tqo} : dq representation of the voltages across the output terminals.

The solution of Eqs. (9.97-9.101) for those variables is as follows, after simplifications:

$$V_{Tdo} = \frac{3}{2}\left(V_{om} + \sqrt{3} I_{om}\left(\cos\left(\Theta_{pfo}\right)R_o - \sin\left(\Theta_{pfo}\right)L_o\omega_o\right)\right) \tag{9.102}$$

$$V_{Tqo} = \frac{3\sqrt{3}}{2} I_{om}\left(\sin\left(\Theta_{pfo}\right)R_o + \cos\left(\Theta_{pfo}\right)L_o\omega_o\right) \tag{9.103}$$

$$I_{im} = \frac{V_{im}\cos\left(\Theta_{pfi}\right) - \sqrt{\left(V_{im}\cos\left(\Theta_{pfi}\right)\right)^2 - 4\sqrt{3}R_i V_{om}\cos\left(\Theta_{pfo}\right)I_{om} - 12R_i R_o I_{om}^2}}{2\sqrt{3}R_i} \tag{9.104}$$

$$V_{Tdi} = \frac{3}{2}\left(V_{im} - \sqrt{3} I_{im}\left(\cos\left(\Theta_{pfi}\right)R_i - \sin\left(\Theta_{pfi}\right)L_i\omega_i\right)\right) \tag{9.105}$$

$$V_{Tqi} = -\frac{3\sqrt{3}}{2} I_{im}\left(\sin\left(\Theta_{pfi}\right)R_i + \cos\left(\Theta_{pfi}\right)L_i\omega_i\right). \tag{9.106}$$

Note that these equations are valid provided that the capacitor voltage V_{cap} is at least as great as the maximum amplitude of the converter peak terminal voltages (i.e., $V_{cap} = \max\{V_{im'}, V_{om'}\}$).

Note that, from Eq. (9.104), for maximum current transfer from the input side to the output side of the matrix converter, the equation under the square root should be set to zero. The equation under the square root of Eq. (9.104) is a quadratic equation in the amplitude of the output current I_{om}. So, if all the other parameters in that equation are known except for the output current amplitude, then the solution of this quadratic, which yields one negative answer and one desired positive answer, is the maximum output current that can be drawn from the converter. Then, Eq. (9.104) will give the corresponding input current amplitude to get that maximum output current.

The solutions of Eqs. (9.102), (9.103), (9.105), and (9.106) are used in Eq. (9.89) to find the steady-state input and output terminal voltages of the matrix converter, as well as the input and output displacement angles. The results are used in finding the input and output modulation indices (Eq. [9.88]) and then finding the input and output dq control of Eq. (9.78).

9.5.3 The Small-Signal AC Model and the LTI State-Space Equations

The small-signal AC equations of the matrix converter come from the 1st-order (linear) portion of Eq. (9.83):

$$[P]\frac{d}{dt}[\hat{x}(t)] = [\hat{f}(t)][X] + [F][\hat{x}(t)], \tag{9.107}$$

which consists of five equations:

$$C\frac{d}{dt}\hat{v}_{cap} = \frac{2I_{di}}{3\sqrt{3}}\hat{\gamma}_{di} + \frac{2I_{qi}}{3\sqrt{3}}\hat{\gamma}_{qi} + \frac{2\Gamma_{di}}{3\sqrt{3}}\hat{i}_{di} + \frac{2\Gamma_{qi}}{3\sqrt{3}}\hat{i}_{qi} - \frac{2I_{do}}{3\sqrt{3}}\hat{\gamma}_{do} - \frac{2I_{qo}}{3\sqrt{3}}\hat{\gamma}_{qo} - \frac{2\Gamma_{do}}{3\sqrt{3}}\hat{i}_{do} - \frac{2\Gamma_{qo}}{3\sqrt{3}}\hat{i}_{qo} \tag{9.108}$$

$$L_i\frac{d}{dt}\hat{i}_{di} = -R_i\hat{i}_{di} + L_i\omega_i\hat{i}_{qi} - \frac{1}{\sqrt{3}}V_{cap}\hat{\gamma}_{di} - \frac{1}{\sqrt{3}}\Gamma_{di}\hat{v}_{cap} \tag{9.109}$$

$$L_i\frac{d}{dt}\hat{i}_{qi} = -R_i\hat{i}_{qi} - L_i\omega_i\hat{i}_{di} - \frac{1}{\sqrt{3}}V_{cap}\hat{\gamma}_{qi} - \frac{1}{\sqrt{3}}\Gamma_{qi}\hat{v}_{cap} \tag{9.110}$$

$$L_o\frac{d}{dt}\hat{i}_{do} = -R_o\hat{i}_{do} + L_o\omega_o\hat{i}_{qo} + \frac{1}{\sqrt{3}}V_{cap}\hat{\gamma}_{do} + \frac{1}{\sqrt{3}}\Gamma_{do}\hat{v}_{cap} \tag{9.111}$$

$$L_o\frac{d}{dt}\hat{i}_{qo} = -R_o\hat{i}_{qo} - L_o\omega_o\hat{i}_{do} + \frac{1}{\sqrt{3}}V_{cap}\hat{\gamma}_{qo} + \frac{1}{\sqrt{3}}\Gamma_{qo}\hat{v}_{cap}\,. \tag{9.112}$$

Equations (9.108-9.112) can be used to form the *small-signal AC model* of the matrix converter. Figure 9.2 shows that model. It consists of five networks: the input and output d and q networks, all linked to the capacitor network by a transformer with turns ratio $\frac{\Gamma_{yx}}{\sqrt{3}}$ ($x = i,o$ and $y = d,q$).

The general form of a linear time-invariant (LTI) state-space system is as follows:

$$\frac{d}{dt}[x(t)] = [A][x(t)] + [B][u(t)]$$
$$y(t) = [C][x(t)] + [D][u(t)] \tag{9.113}$$

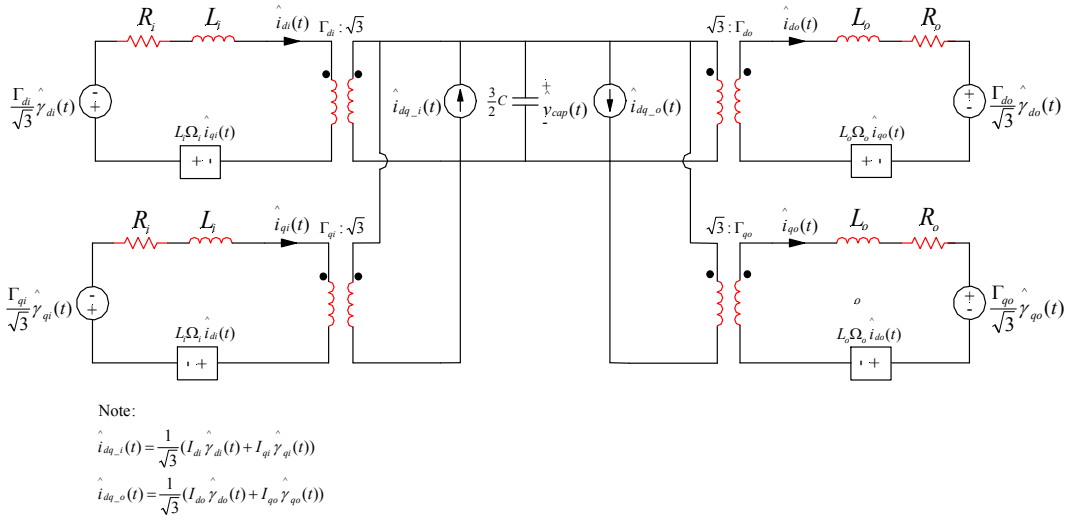


Figure 9.2: The small-signal ac model of the matrix converter

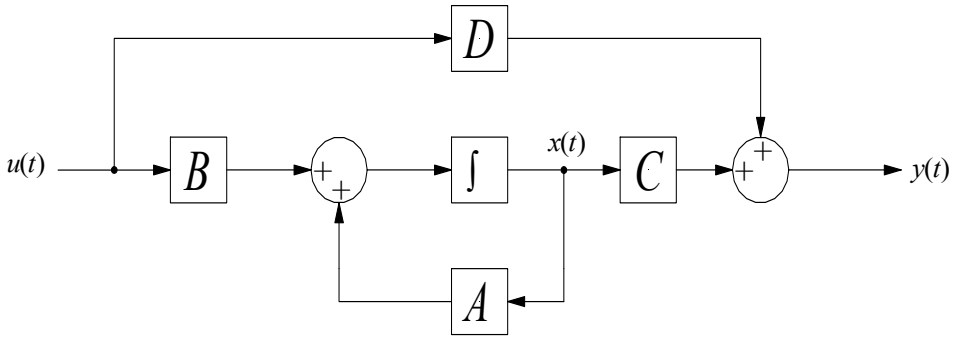


Figure 9.3: Block diagram of a general LTI state space model.

A block diagram of the system described by Eq. (9.113) is shown in Fig. 9.3. Equations (9.108-9.112) can also be combined to get the state-space equations of the linearized matrix converter. The results are

$$\begin{aligned} \frac{d}{dt}\left[\hat{x}(t)\right] &= [A]\left[\hat{x}(t)\right] + [B]\left[\hat{u}(t)\right] \\ \hat{y}(t) &= [C]\left[\hat{x}(t)\right] + [D]\left[\hat{u}(t)\right] \end{aligned} \tag{9.114}$$

where

$$\left[\hat{x}(t)\right] = \left[\hat{v}_{cap}(t) \quad \hat{i}_{di}(t) \quad \hat{i}_{qi}(t) \quad \hat{i}_{do}(t) \quad \hat{i}_{qo}(t)\right]^{\mathrm{T}} \tag{9.115}$$

$$\left[\hat{u}(t)\right] = \left[\hat{\gamma}_{di}(t) \quad \hat{\gamma}_{qi}(t) \quad \hat{\gamma}_{do}(t) \quad \hat{\gamma}_{qo}(t)\right]^{T} \tag{9.116}$$

$$[A] = \begin{bmatrix} 0 & \frac{2\Gamma_{di}}{3\sqrt{3}C} & \frac{2\Gamma_{qi}}{3\sqrt{3}C} & -\frac{2\Gamma_{do}}{3\sqrt{3}C} & -\frac{2\Gamma_{qo}}{3\sqrt{3}C} \\ -\frac{1}{\sqrt{3}L_i}\Gamma_{di} & -\frac{R_i}{L_i} & \omega_i & 0 & 0 \\ -\frac{1}{\sqrt{3}L_i}\Gamma_{qi} & -\omega_i & -\frac{R_i}{L_i} & 0 & 0 \\ \frac{1}{\sqrt{3}L_o}\Gamma_{do} & 0 & 0 & -\frac{R_o}{L_o} & \omega_o \\ \frac{1}{\sqrt{3}L_o}\Gamma_{qo} & 0 & 0 & -\omega_o & -\frac{R_o}{L_o} \end{bmatrix} \tag{9.117}$$

$$[B]=\begin{bmatrix} \frac{2I_{di}}{3\sqrt{3}C} & \frac{2I_{qi}}{3\sqrt{3}C} & -\frac{2I_{do}}{3\sqrt{3}C} & -\frac{2I_{qo}}{3\sqrt{3}C} \\ -\frac{1}{\sqrt{3}L_i}V_{cap} & 0 & 0 & 0 \\ 0 & -\frac{1}{\sqrt{3}L_i}V_{cap} & 0 & 0 \\ 0 & 0 & \frac{1}{\sqrt{3}L_o}V_{cap} & 0 \\ 0 & 0 & 0 & \frac{1}{\sqrt{3}L_o}V_{cap} \end{bmatrix} \tag{9.118}$$

$$[C]=[I]_{5\times 5} \tag{9.119}$$

$$[D]=[0]_{5\times 5}\,. \tag{9.120}$$

A block diagram of the converter state-space equations is shown in Fig. 9.4.

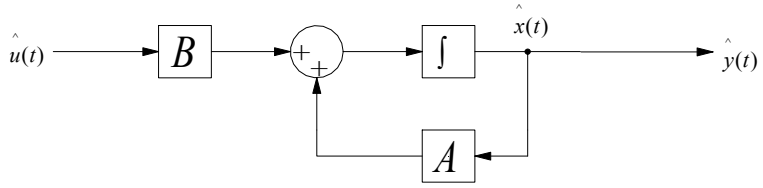


Figure 9.4: Block diagram of the linearized converter's state-space equations

9.6 Poles of the LTI State-Space Model of the Matrix Converter

The last step before designing a feedback controller is an examination of the open-loop model. An examination of the open-loop system reveals important characteristics about it, such as its stability and performance.

The stability of an open-loop linear time-invariant state-space system is determined by the location of its poles. The poles of a state-space system are defined as the eigenvalues of its ***A*** matrix, which is called the system's *state dynamics matrix* [4, 5, 35, 36, 41, 43]. Those eigenvalues can be found by solving the *characteristic polynomial* of the system, which is found to be

$$p(s)=\det\left(s[I]-[A]\right)=0\,, \tag{9.121}$$

where det denotes *determinant*. For the state-space model of the matrix converter described by Eq. (9.114), it is assumed that the filter inductances of both input and output sides are equal and, hence, their resistances ($R_x = R$ and $L_x = L$, $x = i,o$). Using that assumption, after substituting Eq. (9.117) for [*A*] in Eq. (9.121) the characteristic polynomial is

$$
\begin{aligned}
p(s) &= s^5 + 4\left(\frac{R}{L}\right)s^4 \\
&+ \left(6\left(\frac{R}{L}\right)^2 + \frac{2\left(\Gamma_{di}^2 + \Gamma_{qi}^2 + \Gamma_{do}^2 + \Gamma_{qo}^2\right)}{9LCap} + \omega_i^2 + \omega_o^2\right)s^3 \\
&+ \left(4\left(\frac{R}{L}\right)^3 + \frac{2R\left(\Gamma_{di}^2 + \Gamma_{qi}^2 + \Gamma_{do}^2 + \Gamma_{qo}^2\right)}{3L^2Cap} + 2\left(\frac{R}{L}\right)\left(\omega_i^2 + \omega_o^2\right)\right)s^2 \\
&+ \left(\begin{array}{l}\left(\frac{R}{L}\right)^4 + \frac{2\left(\left(\Gamma_{di}^2 + \Gamma_{qi}^2\right)\omega_o^2 + \left(\Gamma_{do}^2 + \Gamma_{qo}^2\right)\omega_i^2\right)}{9LCap} \\ + \frac{2R^2\left(\Gamma_{di}^2 + \Gamma_{qi}^2 + \Gamma_{do}^2 + \Gamma_{qo}^2\right)}{3L^3Cap} + \left(\frac{R}{L}\right)^2\left(\omega_i^2 + \omega_o^2\right) + \omega_i^2\omega_o^2\end{array}\right)s \\
&+ \left(\frac{2R^3\left(\Gamma_{di}^2 + \Gamma_{qi}^2 + \Gamma_{do}^2 + \Gamma_{qo}^2\right)}{9L^4Cap} + \frac{2R\left(\left(\Gamma_{di}^2 + \Gamma_{qi}^2\right)\omega_o^2 + \left(\Gamma_{do}^2 + \Gamma_{qo}^2\right)\omega_i^2\right)}{9L^2Cap}\right) \\
&= 0
\end{aligned}
\tag{9.122}
$$

Equation (9.122) can be further reduced. After substituting the values for Γ_{yx} (x = i,o and y = d,q) defined in Eq. (9.78), the characteristic polynomial becomes

$$
\begin{aligned}
p(s) &= s^5 + 4\left(\frac{R}{L}\right)s^4 + \left(6\left(\frac{R}{L}\right)^2 + \frac{M_i^2 + M_o^2}{2LCap} + \omega_i^2 + \omega_o^2\right)s^3 \\
&+ \left(4\left(\frac{R}{L}\right)^3 + \frac{3R\left(M_i^2 + M_o^2\right)}{2L^2Cap} + 2\left(\frac{R}{L}\right)\left(\omega_i^2 + \omega_o^2\right)\right)s^2 \\
&+ \left(\begin{array}{l}\left(\frac{R}{L}\right)^4 + \frac{M_i^2\omega_o^2 + M_o^2\omega_i^2}{2LCap} + \frac{3R^2\left(M_i^2 + M_o^2\right)}{2L^3Cap} \\ + \left(\frac{R}{L}\right)^2\left(\omega_i^2 + \omega_o^2\right) + \omega_i^2\omega_o^2\end{array}\right)s \\
&+ \left(\frac{R^3\left(M_i^2 + M_o^2\right)}{2L^4Cap} + \frac{R\left(M_i^2\omega_o^2 + M_o^2\omega_i^2\right)}{2L^2Cap}\right)
\end{aligned}
\tag{9.123}
$$

Equation (9.123) is a *quintic* (5th-degree polynomial) and, unfortunately, it cannot be solved by simple mathematical operations, like a quadratic, a cubic, or a quartic polynomial. Numerical solution techniques [7], such as bisection, secant, etc., will be used to solve the polynomial. Appendix (A) shows some pole values corresponding to the following matrix converter parameters:

R : input/output filter inductance resistance (approx.) = 2mΩ

L : input/output filter inductance = 0.2mH

C : matrix converter nine - switch capacitances = 10μF

f_i : input - side line frequency (variable) = 13 – 25Hz

f_o : output - side line frequency = 60Hz

V_{im} : input - side line - to - line voltage amplitude = varies according to a constant 9.6 $\frac{\text{V}}{\text{Hz}}$

V_{om} : output - side line - to - line voltage amplitude = 240V

θ_{pfi} : input power factor (variable) = 0.9 - 1

θ_{pfo} : output power factor (variable) = 0.5 - 1

The rest of the parameters of the matrix converter are found by solving the steady-state equations in Section 9.5.2. The parameters are chosen to show that the input side is some variable-speed power system with low line frequency and a power factor that's close to unity. The output side is a utility grid with a fixed line frequency and line voltage.

A system is considered *stable* if the real parts of all of its poles are negative. That is, if all poles are located to the left of the imaginary axis. From Appendix (A), it is found that the real parts of all five poles of the characteristic polynomial are negative. Therefore, for the wide range of operation points specified by the parameters listed above, the matrix converter is stable. In fact, the real parts of the poles depend mainly on the *R/L* factor. It is approximately *R/2L* for the poles P_1 and P_2 , and *R/L* for P_3 , P_4, and P_5.

9.7 Controllability and Observability of the LTI State-Space Model

A linear state-space model described by Eq. (9.114) with n states, m outputs, and r inputs is completely controllable if its $n \times rn$ controllability matrix has a full rank of n [4, 5, 35, 36, 41, 43]. The controllability matrix is defined as follows:

$$\Lambda = \left[B \mid AB \mid A^2 B \mid .... \mid A^{n-1} B \right]. \tag{9.124}$$

A full rank of controllability means that the states of the model are controllable and full-state feedback is possible; the poles of the open-loop system can be placed such that the desired response is achieved. Similarly, the linear state-space model of Eq. (9.114) is completely observable if its $n \times mn$ observability matrix has a full rank of n, where the observability matrix is defined as

$$\text{O} = \left[C^T \mid A^T C^T \mid \left(A^T\right)^2 C^T \mid .... \mid \left(A^T\right)^{n-1} C^T \right] \tag{9.125}$$

where the superscript T denotes the transpose of the matrix. Full-rank observability implies that all states are available for measurement. If that is not the case (the rank of O is less than n), an observer (state estimator) is required.

The last two columns of the table of Appendix A show the rank of controllability and observability matrices, respectively, over a range of operating points. The rank of those matrices is 5, which is the number of states. As a conclusion, the LTI state-space model of the matrix converter is fully controllable and fully observable.

9.8 Summary

In this chapter, the model of the matrix converter is developed. Differential equations representing the matrix converter were derived. Those equations were then broken down into steady state, 1^{st}-order, and 2^{nd}-order systems. The steady-state model represents the matrix converter operating under steady-state conditions. The 1^{st}-order system was then rearranged to represent the LTI state-space model of the matrix converter. The output variables, which turned out to be the states of this model, are the small perturbations of the matrix converter's variables that need to be minimized. The poles of the LTI state-space model of the matrix converter were then examined over various operating points. The system was found to be stable. Moreover, by testing the controllability and observability of the LTI state-space model, the system was found to be completely controllable and observable. Hence, based on those results, a controller-gain matrix can be designed.

Chapter nine is the main step to solving the control problem of the matrix converter. The next step is designing a feedback controller to minimize the perturbations and finding a relationship between the controller and the converter's varying parameters, which will be discussed in the next chapter.

10 Controller Design for the LTI State-Space Model of the Matrix Converter

10.1 Feedback and Controller Design of the Matrix Converter

This chapter discusses a strategy to design a controller for the matrix converter. In Chapter 9, nonlinear differential equations for the matrix converter were derived. Those equations were then linearized to get a small signal model of the matrix converter. In this chapter, two controller design methods are discussed for the linearized model. The controllers are then tested when used with the nonlinear model of the matrix converter. An attempt to find a relationship between the elements of the controller-gain matrix and the matrix converter parameters is also discussed. As it will be seen, the relationship is clearer with a linear optimal controller design.

To visualize the need to design a feedback controller to regulate the input/output currents and the switch-cells capacitor voltages, Fig. 10.1 shows an output response example of the open-loop nonlinear model of the matrix converter. The initial conditions of the states are zero (i.e., $[x(0)]=[0\ 0\ 0\ 0\ 0]^T$), and steady-state values for the input are used (that is, $[U]=\begin{bmatrix}\Gamma_{di} & \Gamma_{qi} & \Gamma_{do} & \Gamma_{qo}\end{bmatrix}^T$). This corresponds to starting the converter. The figure shows that the output signals do not settle to their constant steady-state values. Instead, they oscillate. The linearized state-space model derived in the previous chapter represents those variations. A feedback controller is to be designed to drive those variations to zero.

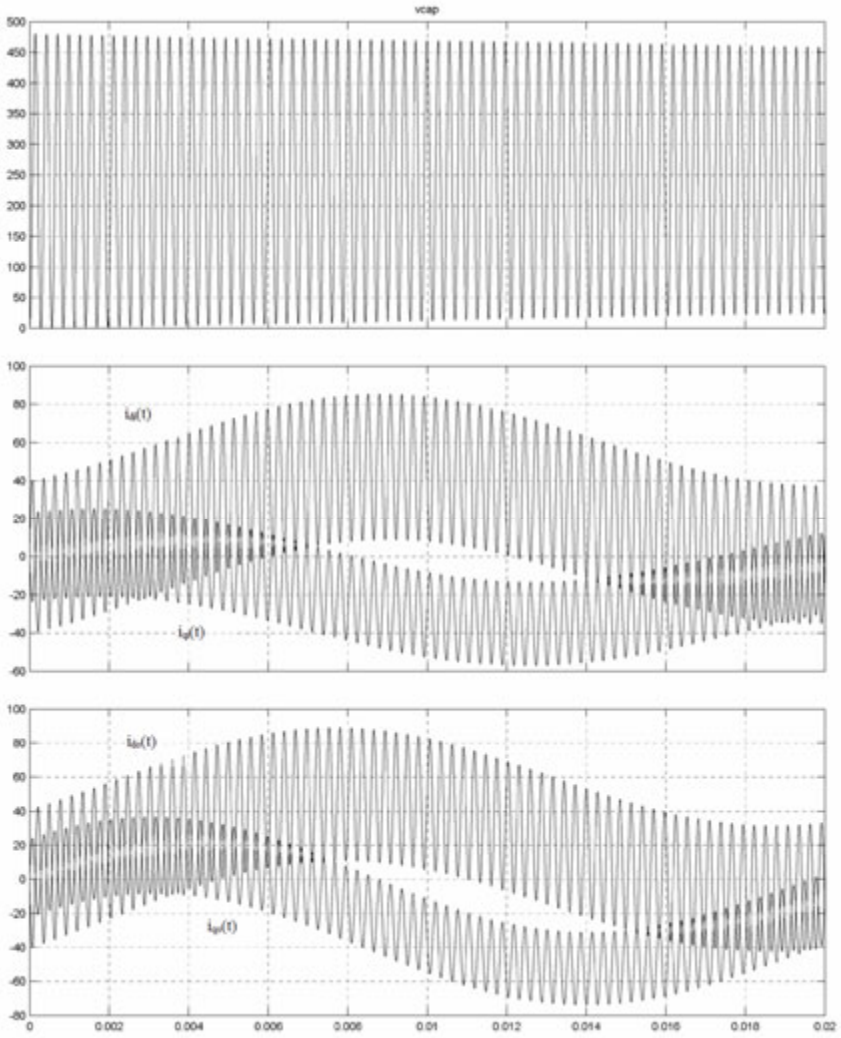


Figure 10.1: Output response example of the matrix converter nonlinear model. The parameters are
Input side: 25 Hz, unity power factor
Output side: 240 V (line-to-line), 20 A, 60 Hz, 0.95 power factor

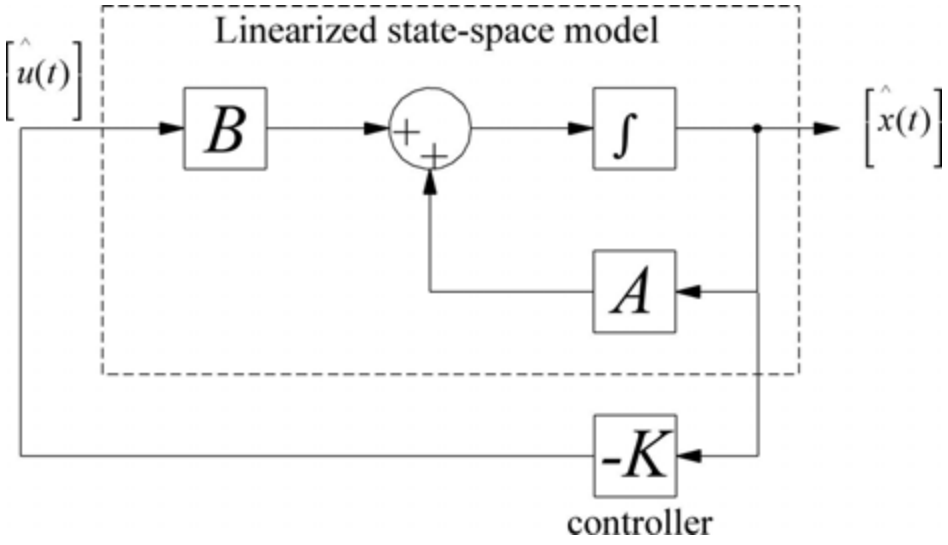


Figure 10.2: State feedback of the linearized model of the matrix converter

Two controller design techniques are considered for design of the controller. The controller produced from either method will be implemented in the LTI model as shown in Fig. 10.2. The figure shows the linearized state--space model of the converter. The outputs, which are also the states, are negatively fed back through a constant gain matrix, [*K*], to the input. The controller matrix, [*K*], is chosen such that the poles of the open-loop system (i.e., the eigenvalues of [*A*]) are *placed* in a specified location. The control input, from Fig. 4.2, is now

$$\left[\hat{u}(t)\right] = -[K]\left[\hat{x}(t)\right]. \tag{10.1}$$

The state-space equations of the linearized state-space model of the matrix converter become the following after substituting Eq. (10.1) into Eq. (9.114):

$$\begin{aligned} \frac{d}{dt}\left[\hat{x}(t)\right] &= \left([A]-[B][K]\right)\left[\hat{x}(t)\right] \\ \hat{y}(t) &= \left[\hat{x}(t)\right] \end{aligned} \tag{10.2}$$

and the new closed-loop poles are the eigenvalues of $\left([A]-[B][K]\right)$, which are the roots of the characteristic polynomial:

$$p_{cl}(s) = s[I] - \left([A]-[B][K]\right) = 0. \tag{10.3}$$

10.2 Controller Design via Pole Placement

The state feedback method via pole placement is the most common in multivariable state-space controller design [4, 5, 10, 27-28, 30-31, 33-36]. The task is finding a controller-gain matrix, *K*, such that the eigenvalues of the closed-loop system, described by the characteristic polynomial of Eq. (10.3), are chosen by the designer. Several methods for solving the problem are available. The pole assignment technique described in [31] is used and also implemented in MATLAB.

10.2.1 Simulation Results of the Linear Model

For the example of Fig. 10.1, the parameters are

Input side:

Line frequency: 25 Hz
Line-to-line voltage: (9.6)(25) = 240 V
Power factor: unity

Output side:

Line frequency: 60 Hz
Line-to-line voltage: 240 V
Line current: 20 A
Power factor: 0.95.

The filter inductances, resistances, and capacitance are, respectively: 0.2 mH, 2 mΩ, and 10 μF. Solution of the steady-state model (Eqs. [9.102-9.106])yields the following:

$$\begin{bmatrix} V_{cap} \\ I_{di} \\ I_{qi} \\ I_{do} \\ I_{qo} \end{bmatrix} = \begin{bmatrix} 240.893932\text{V} \\ 24.696001\text{A} \\ -14.258243\text{A} \\ 19.997976\text{A} \\ -22.362490\text{A} \end{bmatrix}$$

$$\begin{bmatrix} \Gamma_{di} \\ \Gamma_{qi} \\ \Gamma_{do} \\ \Gamma_{qo} \end{bmatrix} = \begin{bmatrix} 1.290642 \\ -0.752590 \\ 1.306628 \\ -0.736697 \end{bmatrix}$$

The poles of the linearized state-space model are found to be

$P_{ol1,\,2} = -5.000840 \pm j22318.155276$
$P_{ol3,\,4} = -9.999584 \pm j288.370143$

P_{ol5} = -9.999153.

The feedback-controller-gain matrix found by using the pole-placement technique depends on the location where the poles should be placed. It is found, by testing several pole locations in all possibly operating modes, that if the poles are closer to the imaginary axis, then the response oscillates. Moreover, placing the poles too far from the imaginary axis yields a high input control. Based on that, a feedback controller-gain matrix, [*K*], was chosen so that the poles of the closed-loop system are located at

P_{cl1}= -28000, P_{cl2}= -28001, P_{cl3}= -5000, P_{cl4}= -5001, P_{cl5}= -5002.

Figure 10.3 shows the simulation results. The initial conditions of each state were set to be the steady-state values:

$$\left[\hat{x}(0)\right] = \left[V_{cap} \quad I_{di} \quad I_{qi} \quad I_{do} \quad I_{qo}\right]^T, \tag{10.4}$$

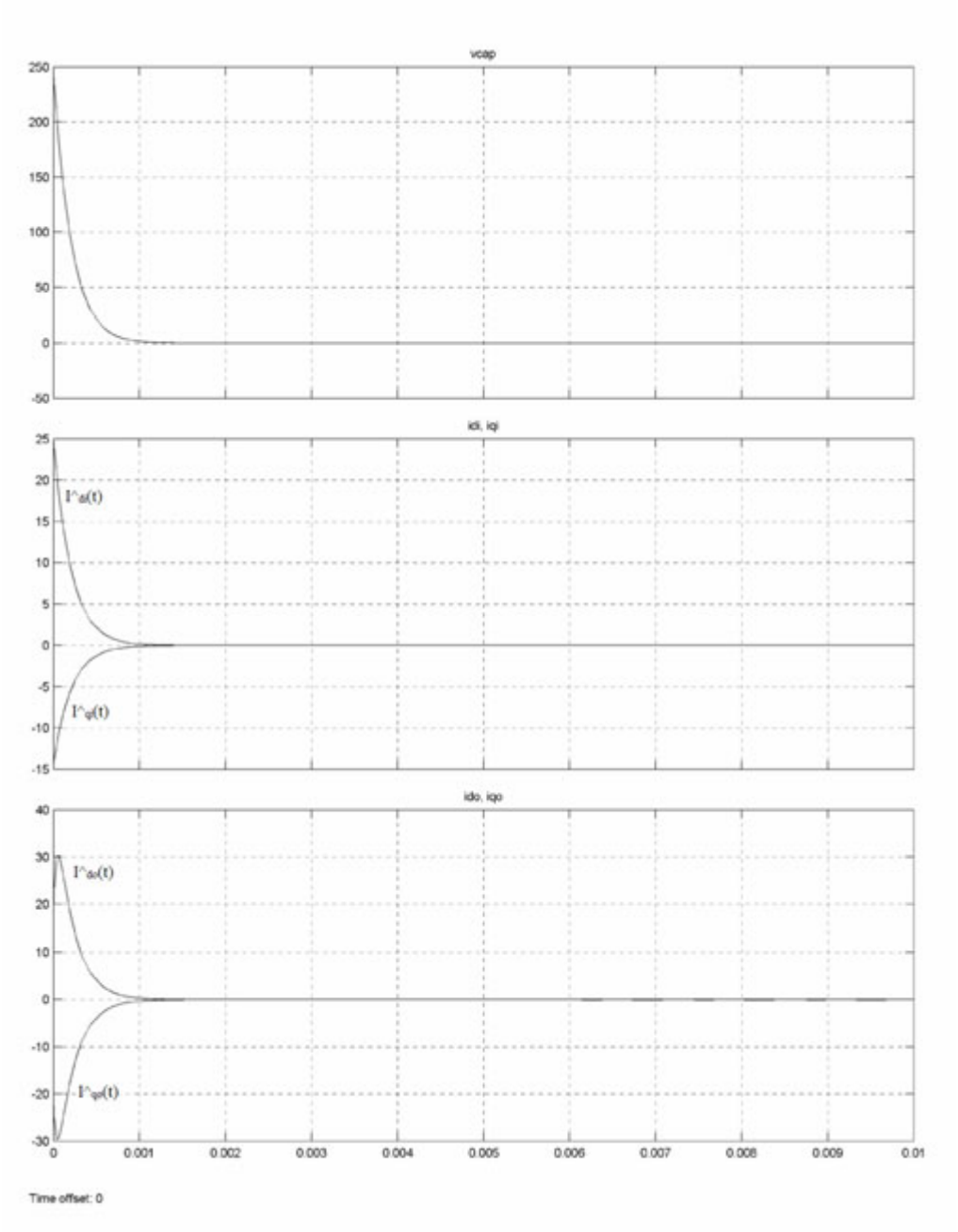


Figure 10.3: Simulation results of the closed-loop linearized state-space model of the matrix converter when a pole-placement controller is used

which correspond to starting the matrix converter. Figure 10.3 shows those variations being driven to zero in about 1.5 msec.

10.2.2 Implementation of the Controller in the Nonlinear Model

The nonlinear model of the matrix converter was derived in the previous chapter. The model was linearized by assuming that the nonlinear variables (states and input signals) are composed of nominal values and some small perturbed values (variations). In the previous section of this report, a state-space model of the perturbed variables was presented and a linear controller was designed to drive those variations to zero. In this section, the results of the previous section are implemented in the nonlinear model of the matrix converter. Figure 10.4 shows such an implementation [4, 5].

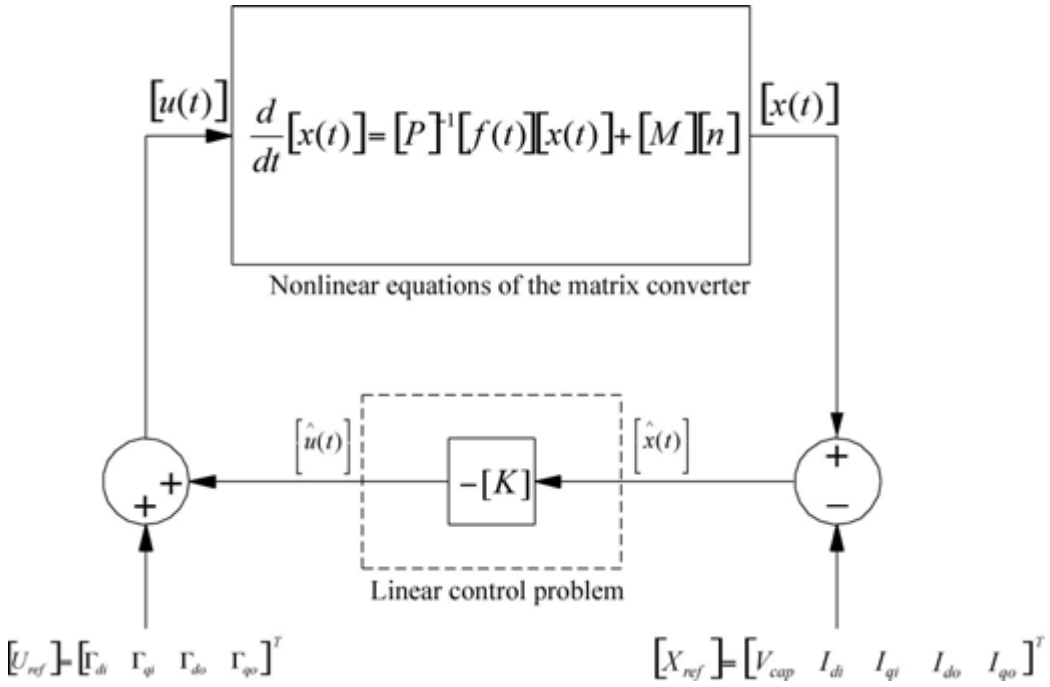


Figure 10.4: Implementation of the linear controller in the nonlinear model of the matrix converter

Figure 10.4 shows that by comparing the nonlinear output of the converter, $[x(t)]$ of Eq. (9.71), to a reference that represents the converter steady-state (nominal) values, $[X_{ref}]$, the output is simply

$$[x(t)]-[X_{ref}]=\begin{bmatrix}V_{cap}\\ I_{di}\\ I_{qi}\\ I_{do}\\ I_{qo}\end{bmatrix}+\begin{bmatrix}\hat{v}_{cap}(t)\\ \hat{i}_{di}(t)\\ \hat{i}_{qi}(t)\\ \hat{i}_{do}(t)\\ \hat{i}_{qo}(t)\end{bmatrix}-\begin{bmatrix}V_{cap}\\ I_{di}\\ I_{qi}\\ I_{do}\\ I_{qo}\end{bmatrix}=\begin{bmatrix}\hat{v}_{cap}(t)\\ \hat{i}_{di}(t)\\ \hat{i}_{qi}(t)\\ \hat{i}_{do}(t)\\ \hat{i}_{qo}(t)\end{bmatrix}=[\hat{x}(t)]. \tag{10.5}$$

The problem now is a linear problem and the controller designed in the previous section is implemented. The output of the controller represents the perturbed input signals, $[\hat{u}(t)]$. The nonlinear input signals to the nonlinear model of the converter are now equal to

$$[u(t)] = [U] + \left[\hat{u}(t)\right] = \begin{bmatrix} \Gamma_{di} \\ \Gamma_{qi} \\ \Gamma_{do} \\ \Gamma_{qo} \end{bmatrix} + \begin{bmatrix} \hat{\gamma}_{di}(t) \\ \hat{\gamma}_{qi}(t) \\ \hat{\gamma}_{do}(t) \\ \hat{\gamma}_{qo}(t) \end{bmatrix} = \begin{bmatrix} \gamma_{di}(t) \\ \gamma_{qi}(t) \\ \gamma_{do}(t) \\ \gamma_{qo}(t) \end{bmatrix}, \tag{10.6}$$

and the control problem of the nonlinear model of the converter is solved.

10.3 Simulation Results

The following simulation results show the closed-loop response of the nonlinear model of the matrix converter, with the controller designed in Section 10.2 implemented over various operating points. The simulations assume that the capacitor voltage is zero. One can think of this as the worst case. If the response is acceptable, which it is, the controller should be valid if the initial capacitor voltage does not equal zero (e.g., switching from one capacitor to another) or when shifting from one operating point to another (e.g., change in power demand or wind speed).

10.3.1 Input Side: 25 Hz, 240 V, Unity Power Factor; Output Side: 60 Hz, 240 V, 20 A, Unity Power Factor

Figure 10.5 shows the simulation results when the input side (e.g., generator) is operating at 240 V, unity power factor with an input-line frequency of 25 Hz. The output side (e.g., utility) is operating at 240 V, 60 Hz with an output demand of 20 A at unity power factor. The figure shows the transient response to the capacitor voltage, the *dq* input currents and the *dq* output current. Note how the output *dq* currents start to proceed opposite to their nominal value before changing direction. An explanation to this is that at start up, currents of both sides charge up the capacitor before output side draws current from the input side.

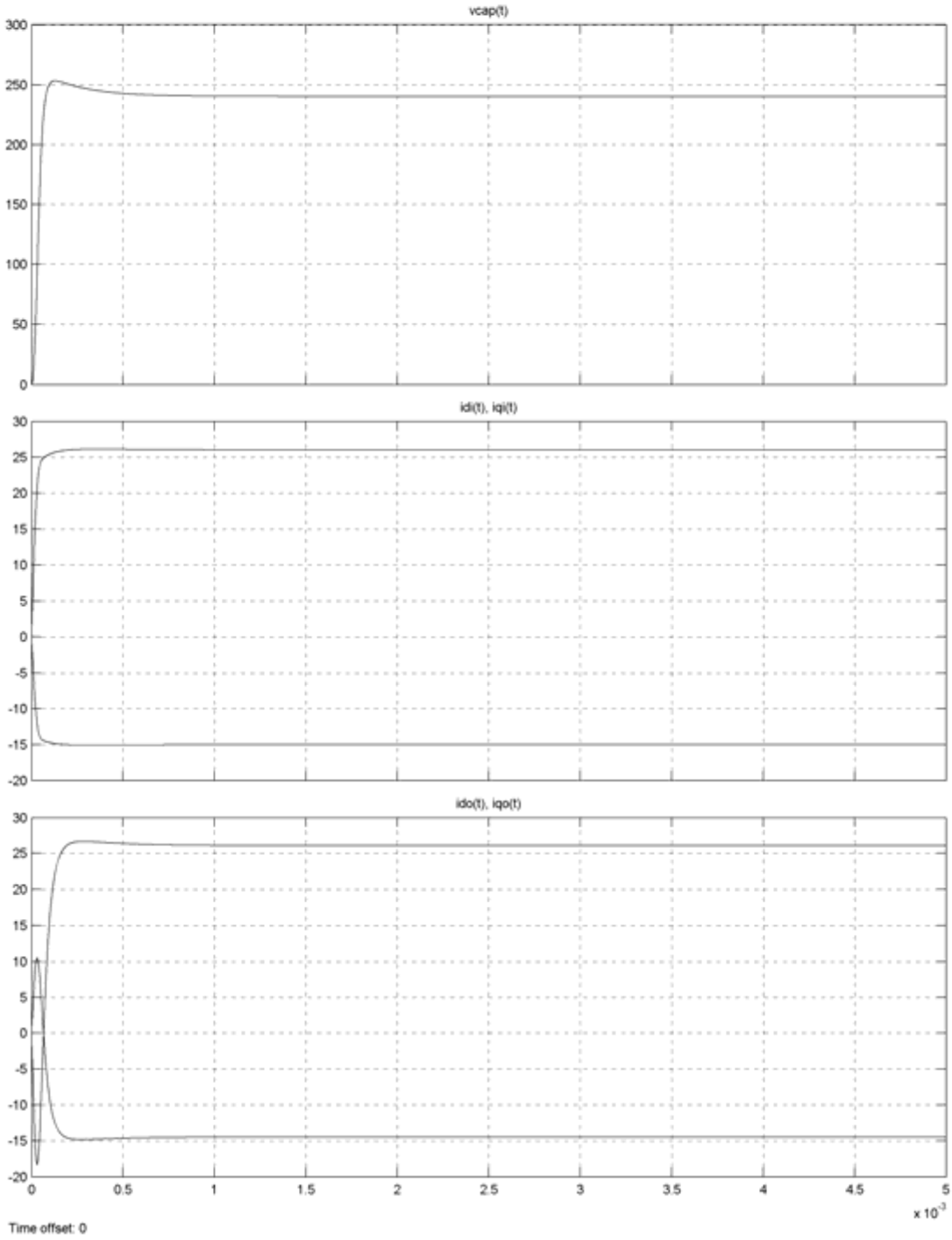


Figure 10.5: Simulation results for the following operating point:
Input side: 240 V, 25 Hz, unity power factor
Output side: 240 V, 60 Hz, 20 A, unity power factor
The first part is the capacitor voltage response, the second part is the input *dq* currents responses, and the third part is the output *dq* currents responses

10.3.2 Input Side: 25 Hz, 240 V, Unity Power Factor; Output Side: 60 Hz, 240 V, 20 A, 0.5 Power Factor

Figure 10.6 shows the simulation results when the input side (e.g., generator) is operating at 240 V, unity power factor with an input line frequency of 25 Hz. The output side (e.g., utility) is operating at 240 V, 60 Hz with an output demand of 20 A at 0.5 power factor (i.e., 50% real power transfer). The figure shows the transient response to the capacitor voltage, the *dq* input currents, and the *dq* output current. Note how the output *dq* currents start to proceed opposite to their nominal value before changing direction. An explanation to this is that at start up, currents of both sides charge up the capacitor before output side draws current from the input side. Also, note the output *d* current settles to zeros. This is because it is assumed that the line-to-line voltage is the reference voltage (i.e., zero phase angle), which means that the line currents lag by 30^o, as explained in Section 3.2. And with a 0.5 lagging-power factor (60^o angle), the nominal value of the *d*-component of the output current is zeros.

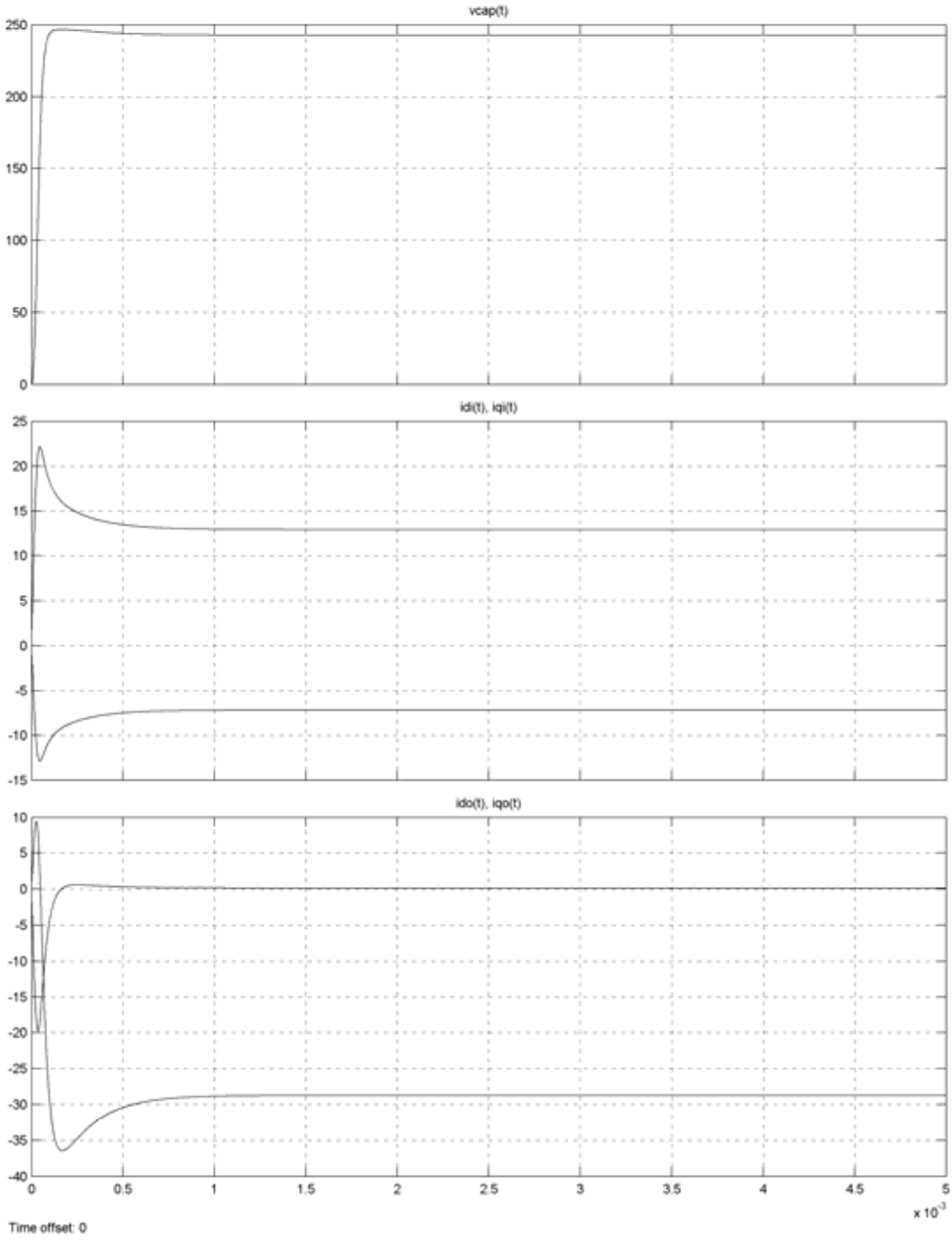


Figure 10.6: Simulation results for the following operating point:
Input side: 240 V, 25 Hz, unity power factor
Output side: 240 V, 60 Hz, 20 A, 0.5 power factor
The first part is the capacitor voltage response, the second part is the input *dq* currents responses, and the third part is the output *dq* currents responses

10.3.3 Input Side: 13 Hz, 240 V, Unity Power Factor; Output Side: 60 Hz, 240 V, 20 A, Unity Power Factor

Figure 10.7 shows the simulation results when the input side (e.g., generator) is operating at 240 V, unity power factor with an input-line frequency of 13 Hz. The output side (e.g., utility) is operating at 240 V, 60 Hz with an output demand of 20 A at unity power factor. This operating point corresponds to the lowest operating condition of the matrix converter under two-level modulation. The figure shows the transient response to the capacitor voltage, the *dq* input currents, and the *dq* output current. Note how the output *dq* currents start to proceed opposite to their nominal value before changing direction. An explanation to this is that at start up, currents of both sides charge up the capacitor before output side draws current from the input side.

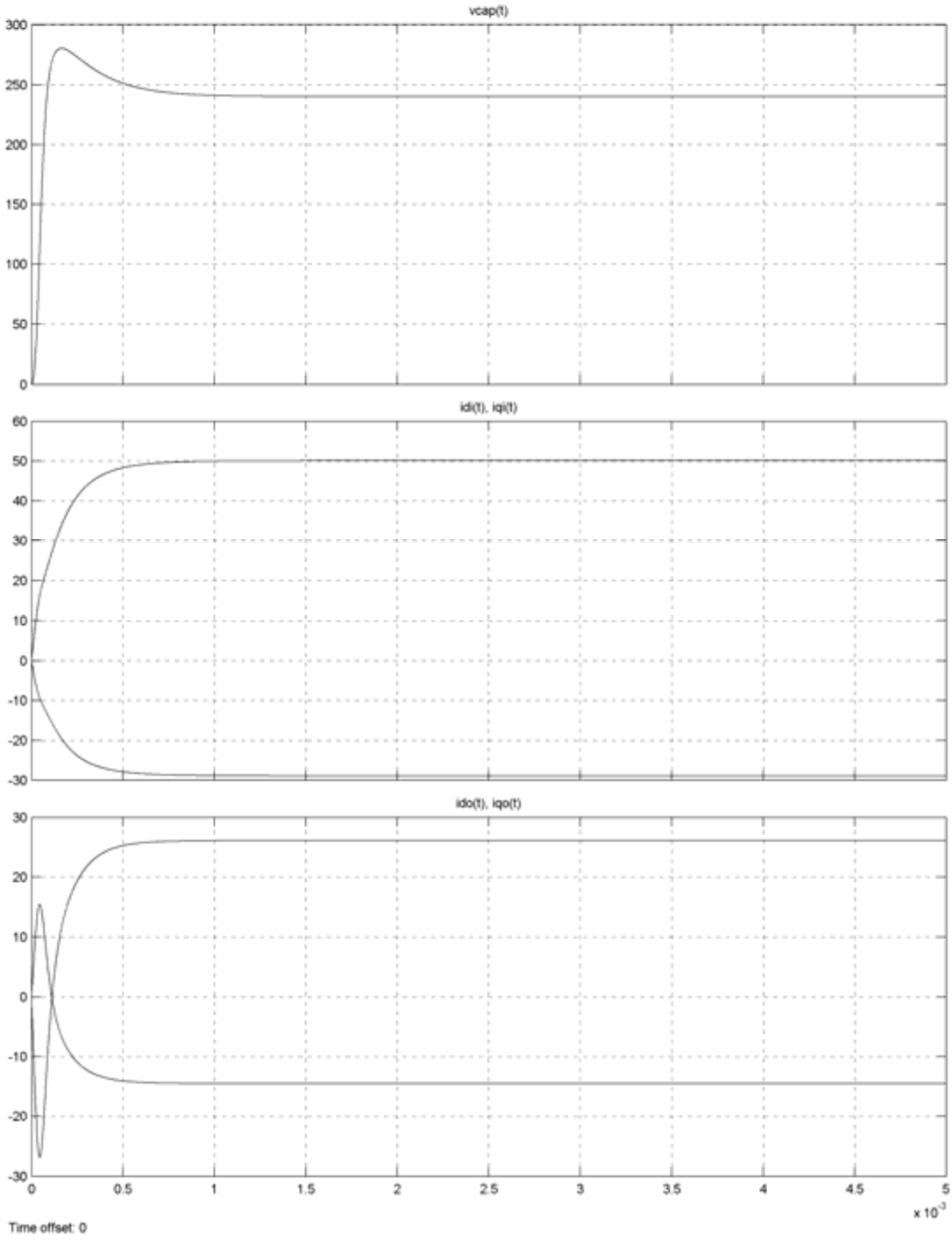


Figure 10.7: Simulation results for the following operating point:
Input side: 240 V, 13 Hz, unity power factor
Output side: 240 V, 60 Hz, 20 A, unity power factor
The first part is the capacitor voltage response, the second part is the input *dq* currents responses, and the third part is the output *dq* currents responses

10.3.4 Input Side: 13 Hz, 240 V, Unity Power Factor; Output Side: 60 Hz, 240 V, 20 A, 0.5 Power Factor

Figure 10.8 shows the simulation results when the input side (e.g., generator) is operating at 240 V, unity power factor with an input line frequency of 13 Hz. The output side (e.g., utility) is operating at 240 V, 60 Hz with an output demand of 20 A at 0.5 power factor (i.e., 50% real power transfer). This operating point is similar to that of Section 10.3.3 but with 50% real power demand. The figure shows the transient response to the capacitor voltage, the *dq* input currents, and the *dq* output current. Note how the output *dq* currents start to proceed opposite to their nominal value before changing direction. An explanation to this is that, at start up, currents of both sides charge up the capacitor before output side draws current from the input side. Also, note the output *d* current settles to zeros. This is because it is assumed that the line-to-line voltage is the reference voltage (i.e., zero phase angle), which means that the line currents lag by 30^o, as explained in Section 9.2. And with a 0.5 lagging power factor (60^o angle), the nominal value of the *d*-component of the output current is zeros.

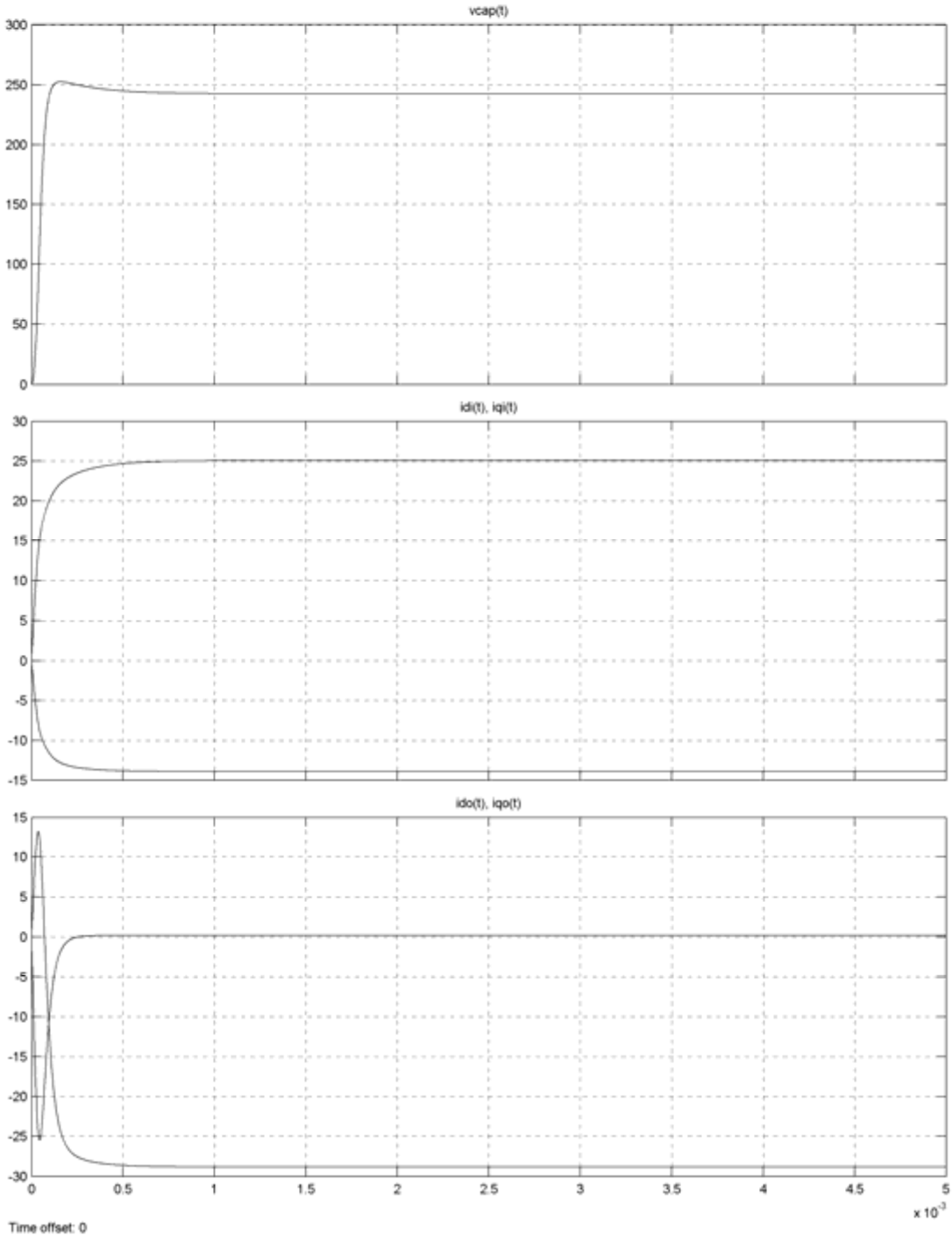


Figure 10.8: Simulation results for the following operating point:
Input side: 240 V, 13 Hz, unity power factor
Output side: 240 V, 60 Hz, 20 A, 0.5 power factor
The first part is the capacitor voltage response, the second part is the input *dq* currents responses, and the third part is the output *dq* currents responses

10.4 The Relationship Between *K* and the Matrix Converter Parameters

The performance of the controller designed by the pole-placement method was shown in the previous section to be very acceptable at a single operating point. However, whenever a reference parameter changes (e.g., output current), the controller had to be recalculated to place the poles at the desired location. Finding the controller-gain matrix online every time a parameter changes involves calculating a large time-consuming code. An easier approach is to find a relationship between the controller-gain matrix and the varying parameters. Appendix B shows a table of the elements of controller-gain matrix as the matrix converter parameters change. The table shows that those elements are dependent only on the input line frequency f_i and the amplitude of the output line current I_{om}.

A plot of the first row of K (k_{1j} , j = 1,5) as a function of the output current I_{om} is shown for several input line frequencies in Fig. 10.9. Other rows of K are shown in Appendix B. From the figure, it can be concluded that no easy relationship can be found between the elements of K, the output current, and the input line frequency. The figure also suggests that the elements are very sensitive to those variations, making it harder to physically implement the controller designed by pole placement. Although the pole-placement method discussed in [31] is fast in calculation, it is very sensitive to variations [47]. Another controller design method had to be considered.

10.5 Linear Optimal Control

Optimal control is different than pole placement in finding a controller-gain matrix. In brief, a controller-gain matrix, K, designed for a LTI state-space system (Eq. [9.114]) is defined as follows [4, 5, 35, 41-43]:

$$[K] = [R]^{-1}[B]^T[M_o] \tag{10.7}$$

where the matrix $[M_o]$ is the solution of the *algebraic Riccati equation* defined by

$$[0] = [A]^T[M_o] + [M_o][A] - [M_o][B][R]^{-1}[B]^T[M_o] + [Q]. \tag{10.8}$$

The matrix $[R]$ is called the *control cost matrix* and the matrix $[Q]$ is called the *state weighting matrix*. Both matrices should be *positive definite*. For the linear time-invariant control design problem, $[R]$ and $[Q]$ are chosen to minimize the *infinite-time objective function*:

$$J_\infty(t) = \int_t^\infty \left(\left[\hat{x}(\tau) \right]^T [Q] \left[\hat{x}(\tau) \right] + \left[\hat{u}(\tau) \right]^T [R] \left[\hat{u}(\tau) \right] \right) d\tau . \tag{10.9}$$

From Eq. (10.9), the term $\left[\hat{x}(\tau) \right]^T [Q] \left[\hat{x}(\tau) \right]$ is called the *transient energy*, and the term $\left[\hat{u}(\tau) \right]^T [R] \left[\hat{u}(\tau) \right]$ is called the *control energy*.

Unlike the pole-placement method, where the controller is calculated so that the poles are placed in a specified location, an optimal controller is calculated in such a way that minimizes Eq.(10.9), given how much control effort, [*R*], and state weight, [*Q*], should be allotted.

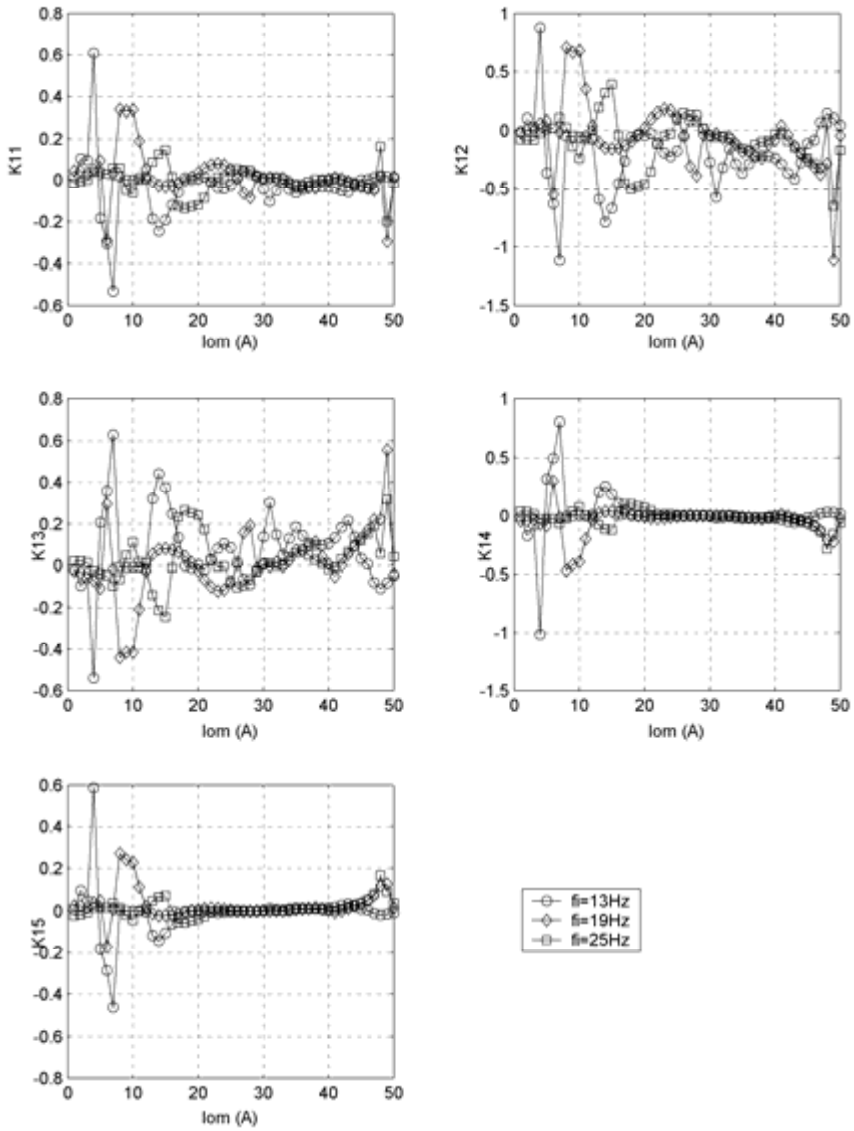


Figure 10.9: Plots of the first row of elements of the controller-gain matrix, *K*, as a function of the input current amplitude for the pole-placement technique; results are given for several input-line frequencies

For the linear state-space model of the matrix converter, several values of the matrices [R] and [Q] were tested over all possible operating modes. The values chosen to make the transient response and the error minimal were

$$[Q] = diag\{0.0001 \quad 0.01 \quad 0.01 \quad 0.01 \quad 0.01\} \tag{10.10}$$

$$[R] = diag\{3.0 \quad 3.0 \quad 3.0 \quad 3.0\}. \tag{10.11}$$

The algebraic Riccati equation (Eq. [10.8]) is then solved for [M_o], and the result is substituted in Eq. (10.7) to find the controller-gain matrix [K].

10.5.1 Simulation Results of the Linear Model

Using the same example of Section 10.2.1 but with the optimal controller implemented, Fig. 10.10 shows the simulation results for the LTI model. The output variations are driven to zero faster than when the pole-placement controller is used. It is crucial to have the capacitor voltage reach its nominal value because a capacitor is utilized for a short time before switching to another capacitor. Hence, a fast response will be better in charging the capacitor once utilized.

10.5.2 Implementation of the Optimum Controller in the Matrix Converter Nonlinear Model

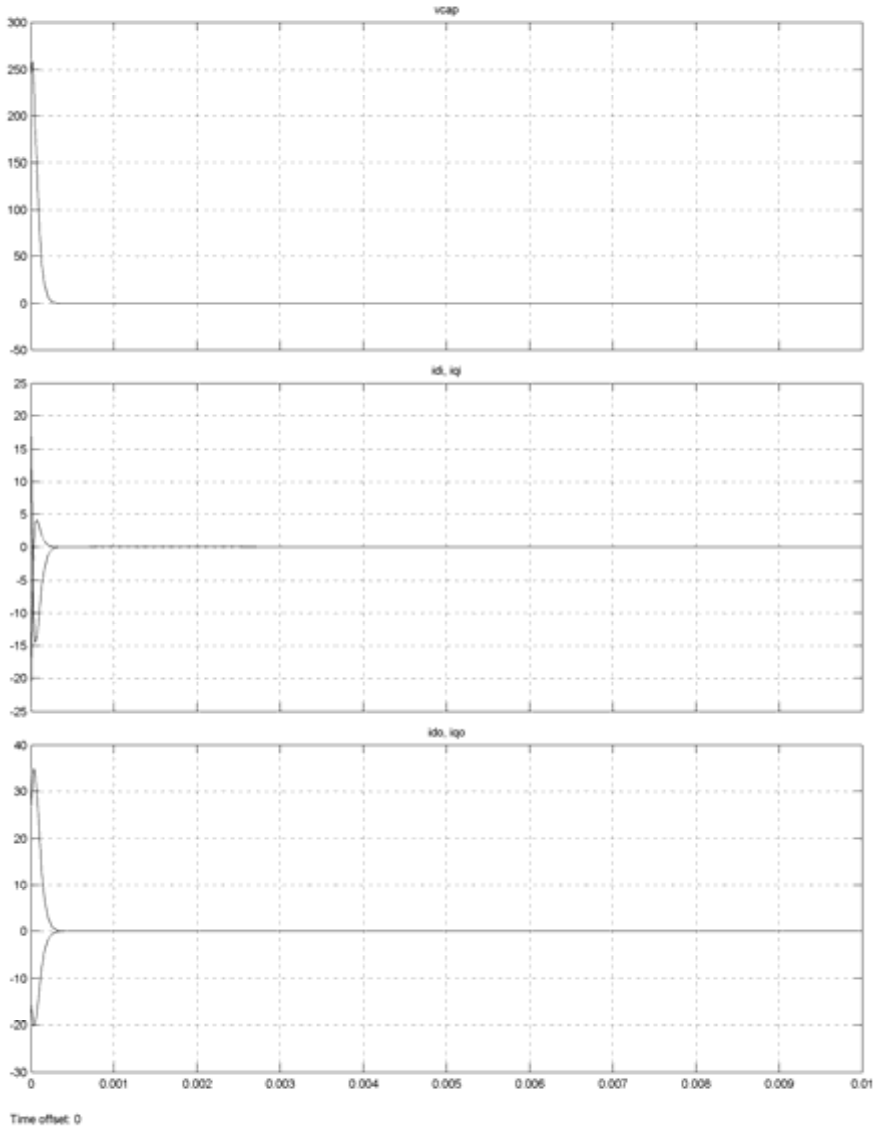


Figure 10.10: Simulation results of the closed-loop linearized state-space model of the matrix converter when an optimal controller is used

The outcome of both the controller design using pole placement and the optimal controller design was a controller-gain matrix. Hence, the implementation of the controller in the matrix converter nonlinear model, discussed in Section 10.2.2, applies here as well.

10.6 Simulation Results

The following simulation results show the closed-loop response of the nonlinear model of the matrix converter, with the linear optimal controller designed in Section 10.5 implemented over various operating points. The simulations assume that the initial value of the capacitor voltage is zero. This can be considered a worst-case response. If the response is acceptable, which it is, the controller should be valid if the initial capacitor voltage does not equal zero (e.g., switching from one capacitor to another) or when shifting from one operating point to another (e.g., change in power demand or wind speed).

10.6.1 Input Side: 25 Hz, 240 V, Unity Power Factor; Output Side: 60 Hz, 240 V, 20 A, Unity Power Factor

Figure 10.11 shows the simulation results when the input side (e.g., generator) is operating at 240 V, unity power factor with an input-,line frequency of 25 Hz. The output side (e.g., utility) is operating at 240 V, 60 Hz with an output demand of 20 A at unity power factor. The figure shows the transient response to the capacitor voltage, the *dq* input currents, and the *dq* output current. Note how the output *dq* currents start to proceed opposite to their nominal value before changing direction. An explanation to this is that at start up, currents of both sides charge up the capacitor before output side draws current from the input side. Comparing Fig. 10.11 to Fig. 10.5 shows that with the linear optimal controller, the response is faster.

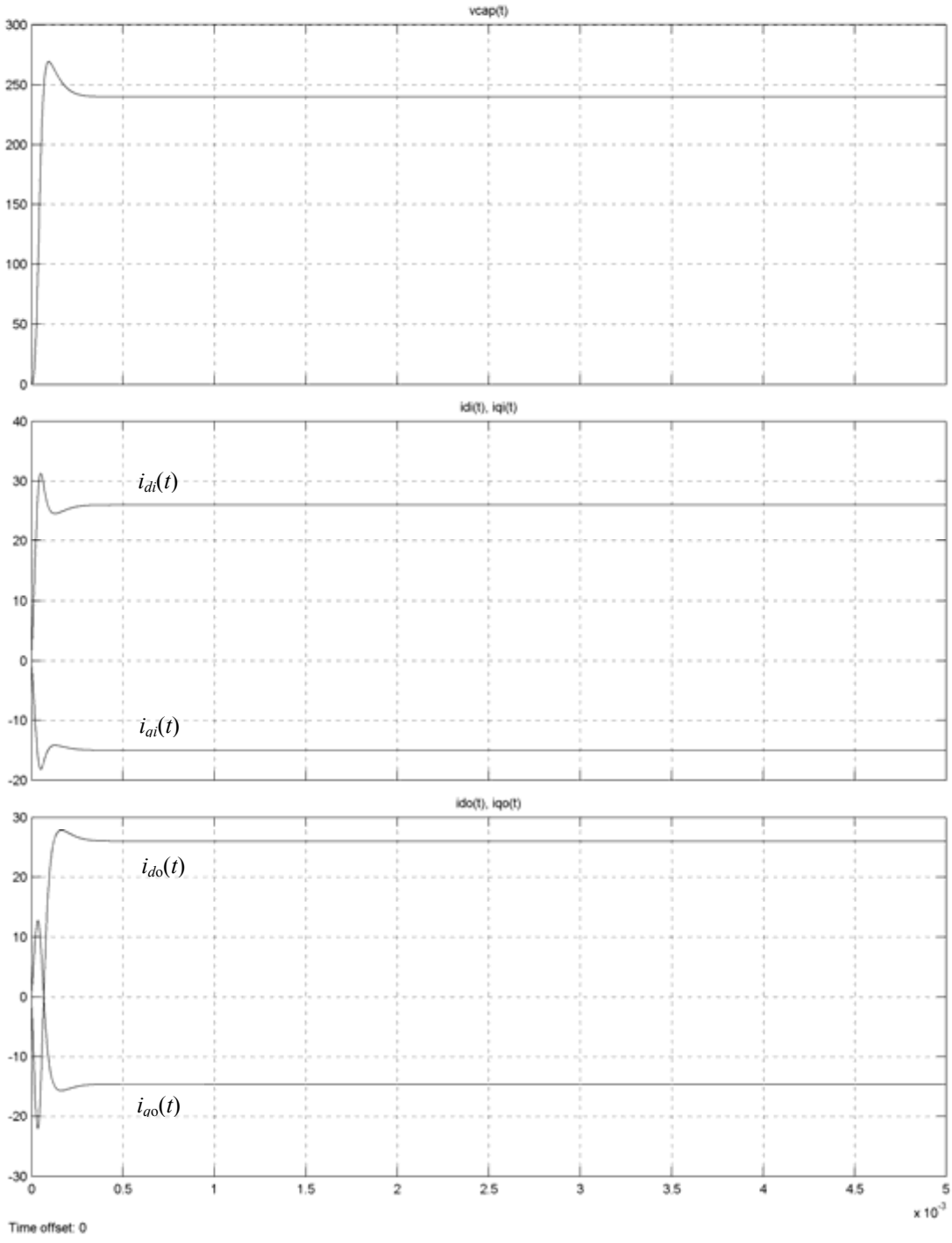


Figure 10.11: Simulation results for the following operating point:
Input side: 240 V, 25 Hz, unity power factor
Output side: 240 V, 60 Hz, 20 A, unity power factor
The first part is the capacitor voltage response, the second part is the input *dq* currents responses, and the third part is the output *dq* currents responses

10.6.2 Input Side: 25 Hz, 240 V, Unity Power Factor; Output Side: 60 Hz, 240 V, 20 A, 0.5 Power Factor

Figure 10.12 shows the simulation results when the input side (e.g., generator) is operating at 240 V, unity power factor with an input-line frequency of 25 Hz. The output side (e.g., utility) is operating at 240 V, 60 Hz with an output demand of 20 A at 0.5 power factor (i.e., 50% real power transfer). The figure shows the transient response to the capacitor voltage, the *dq* input currents, and the *dq* output current. Note how the output *dq* currents start to proceed opposite to their nominal value before changing direction. An explanation to this is that at start up, currents of both sides charge up the capacitor before output side draws current from the input side. Also, note the output direct-axis current settles to zeros. This is because it is assumed that the line-to-line voltage is the reference voltage (i.e., zero phase angle), which means that the line currents lag by 30^{o}, as explained in Section 9.2. And with a 0.5 lagging-power factor (60^{o} angle), the nominal value of the *d*-component of the output current is zeros. Comparing Fig. 10.12 to Fig. 10.6 shows that with the linear optimal controller, the response is faster.

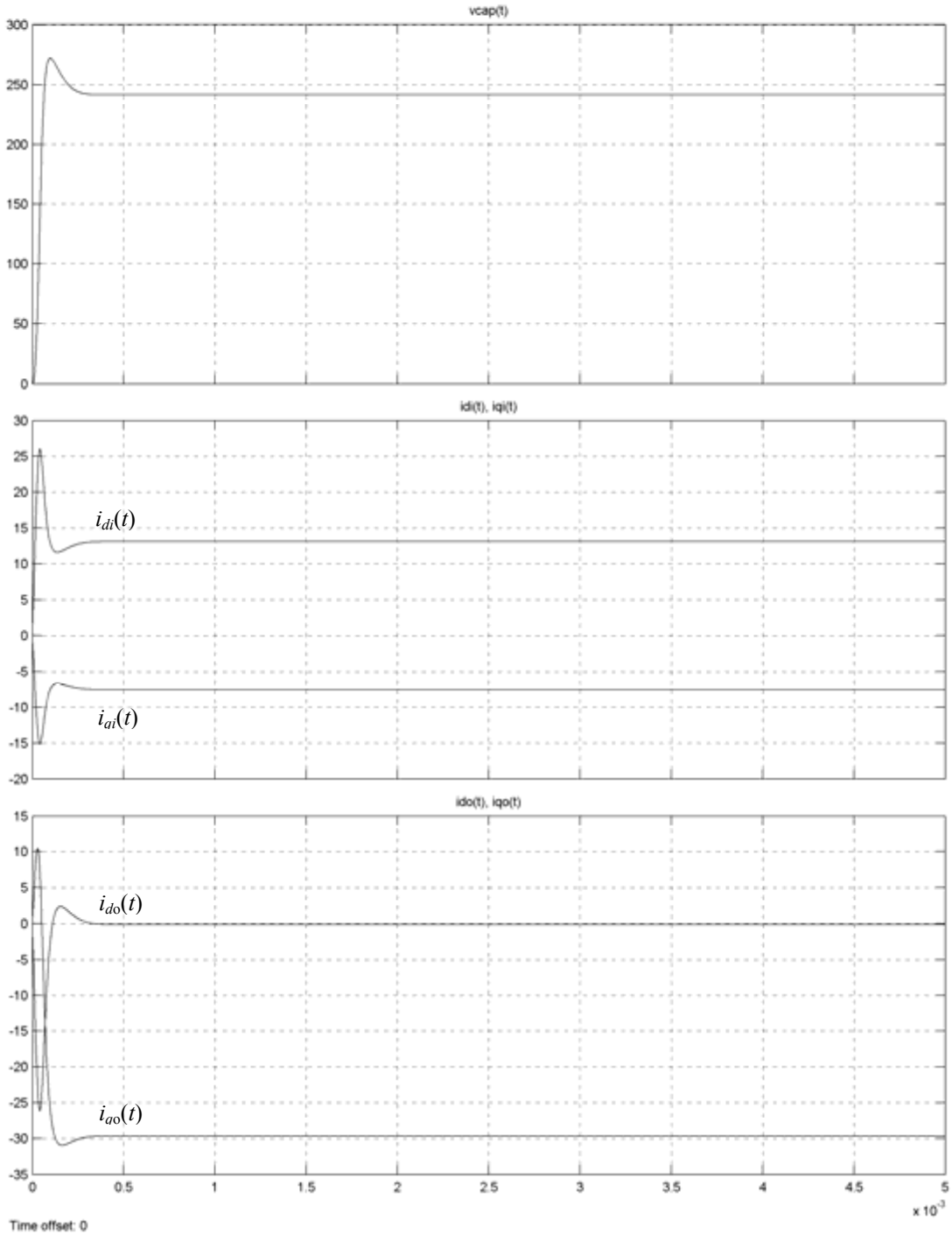


Figure 10.12: Simulation results for the following operating point:
Input side: 240 V, 25 Hz, unity power factor
Output side: 240 V, 60 Hz, 20 A, 0.5 power factor
The first part is the capacitor voltage response, the second part is the input *dq* currents responses, and the third part is the output *dq* currents responses

10.6.3 Input Side: 13 Hz, 240 V, Unity Power Factor; Output Side: 60 Hz, 240 V, 20 A, Unity Power Factor

Figure 10.13 shows the simulation results when the input side (e.g., generator) is operating at 240 V, unity power factor with an input-line frequency of 13 Hz. The output side (e.g., utility) is operating at 240 V, 60 Hz with an output demand of 20 A at unity power factor. This operating point corresponds to the lowest operating condition of the matrix converter under two-level modulation. The figure shows the transient response to the capacitor voltage, the *dq* input currents, and the *dq* output current. Note how the output *dq* currents start to proceed opposite to their nominal value before changing direction. An explanation to this is that at start up, currents of both sides charge up the capacitor before output side draws current from the input side. Comparing Fig. 10.13 to Fig. 10.7 shows that with the linear optimal controller, the response is faster.

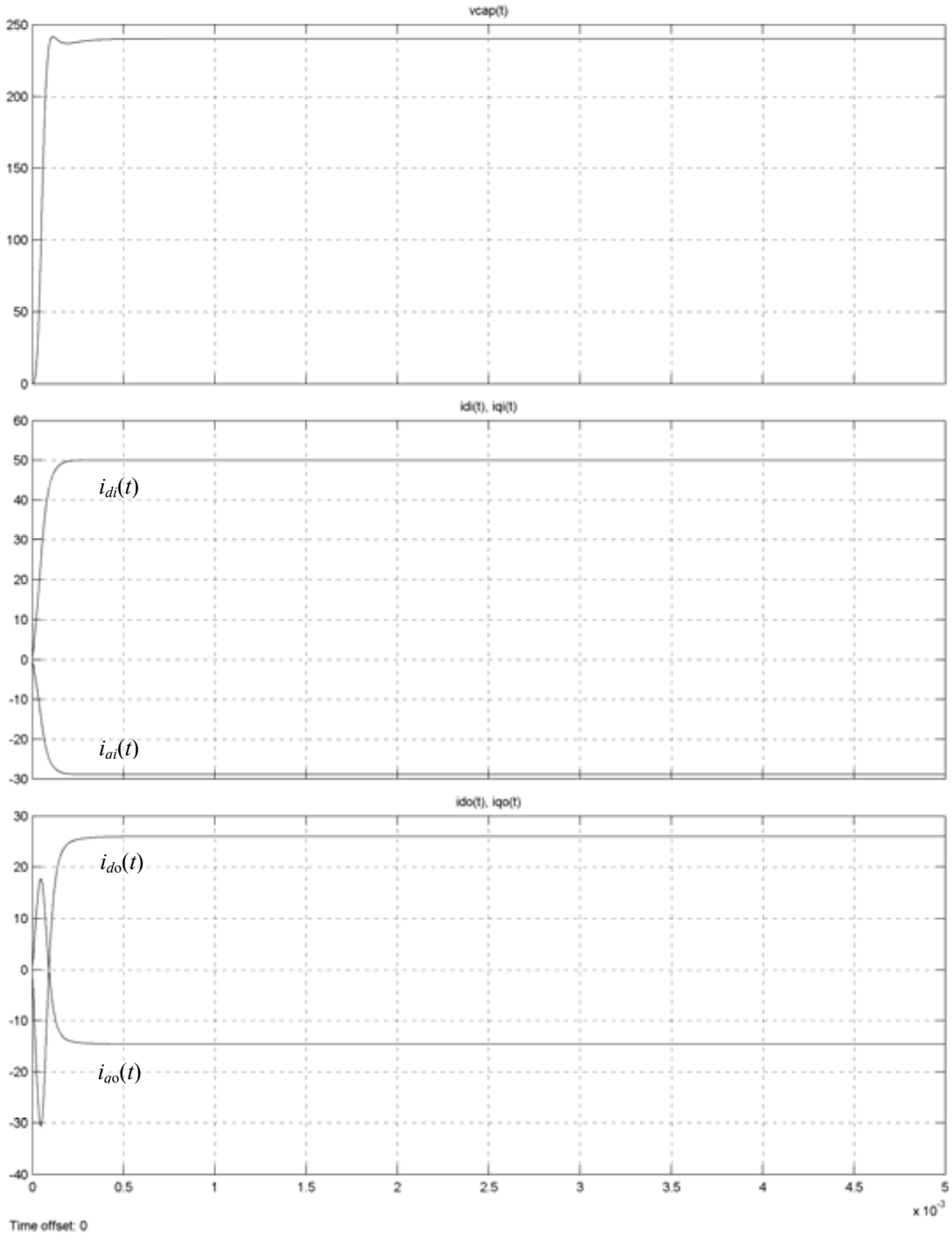


Figure 10.13: Simulation results for the following operating point:
Input side: 240 V, 13 Hz, unity power factor
Output side: 240 V, 60 Hz, 20 A, unity power factor
The first part is the capacitor voltage response, the second part is the input *dq* currents responses, and the third part is the output *dq* currents responses

10.6.4 Input Side: 13 Hz, 240 V, Unity Power Factor; Output Side: 60 Hz, 240 V, 20 A, 0.5 Power Factor

Figure 10.14 shows the simulation results when the input side (e.g., generator) is operating at 240 V, unity power factor with an input-line frequency of 13 Hz. The output side (e.g., utility) is operating at 240 V, 60 Hz with an output demand of 20 A at 0.5 power factor (i.e., 50% real power transfer). This operating point is similar to that of Section 10.6.8 but with 50% real power demand. The figure shows the transient response to the capacitor voltage, the *dq* input currents, and the *dq* output current. Note how the output *dq* currents start to proceed opposite to their nominal value before changing direction. An explanation to this is that at start up, currents of both sides charge up the capacitor before output side draws current from the input side. Also, note the output *d* current settles to zeros. This is because it is assumed that the line-to-line voltage is the reference voltage (i.e., zero phase angle), which means that the line currents lag by 30^{o}, as explained in Section 9.2. And with a 0.5 lagging-power factor (60^{o} angle), the nominal value of the *d*-component of the output current is zeros. Comparing Fig. 10.14 to Fig. 10.8 shows that with the linear optimal controller, the response settles faster.

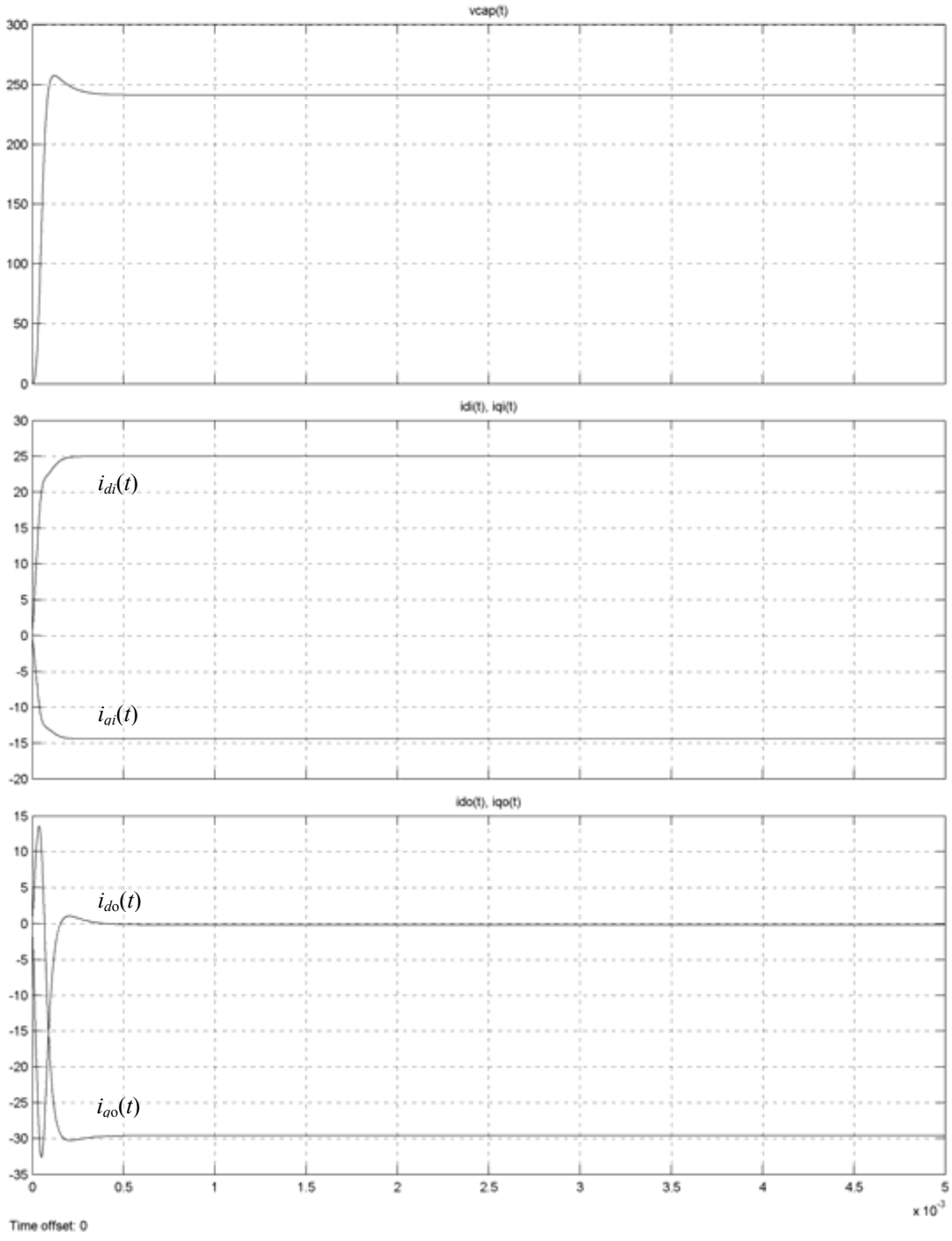


Figure 10.14: Simulation results for the following operating point:
Input side: 240 V, 13 Hz, unity power factor
Output side: 240 V, 60 Hz, 20 A, 0.5 power factor
The first part is the capacitor voltage response, the second part is the input *dq* currents responses, and the third part is the output *dq* currents responses

10.7 The Relationship between the Optimal Controller and the Matrix-Converter Parameters

As investigated in Section 10.4, a relationship between the controller and the matrix-converter parameters, if found, will save time in finding the elements of the controller-gain matrix. The controller designed via pole placement was sensitive to the matrix-converter parameter variations. Moreover, no relationship could be found between the elements of the controller-gain matrix and the matrix-converter parameters, which turned out to be the input-line frequency f_i and the output current amplitude I_{om}. We will make the same attempt to find the relationship between the optimal controller and the matrix converter by varying parameters.

Appendix C shows a table of the elements of the optimal controller-gain matrix as the matrix-converter parameters are varied. Like the pole-placement controller, the elements of the optimal controller-gain matrix depend only on the input-line frequency f_i and the output current amplitude I_{om}. Plots of the first row of the controller-gain matrix as the output current amplitude varies are shown in Figure 10.15 for several input line frequencies. Plots of other elements of the controller are shown in Appendix C. Note that the rows of the controller-gain matrix correspond to the control variation ($\hat{\gamma}_{xy}(t)$) while the columns correspond to the variation in the states ($\hat{x}(t)$). For example, the element k_{23} is the gain for the 2nd input control $\hat{\gamma}_{qi}(t)$ as a result of variation in the 3rd state $\hat{i}_{qi}(t)$. Note also from the graphs (Figs. C.1-C.4) that when an element is positive, its counterpart element is negative and vice versa. For example, k_{12} ($\hat{\gamma}_{di}(t)$ resulting from $\hat{i}_{di}(t)$) is negative, whereas k_{13} ($\hat{\gamma}_{di}(t)$ resulting from $\hat{i}_{qi}(t)$) is positive.

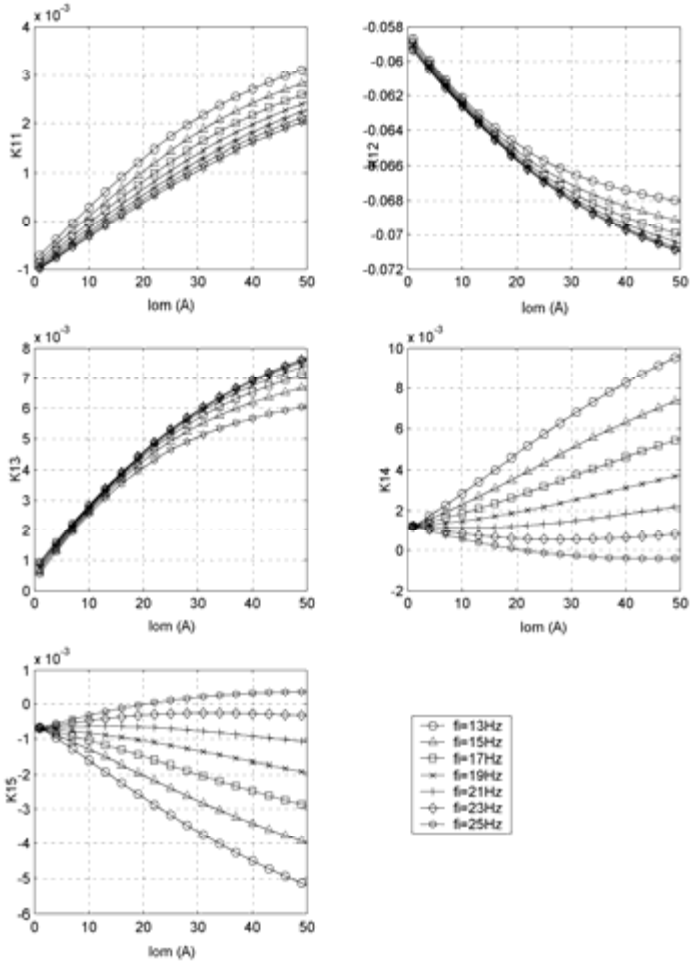


Figure 10.15: Plots of the first row of the optimal controller-gain matrix as a function of the output current amplitude, plotted for various input-line frequencies.

The graphs show that relationship between the controller-gain matrix and the

output current amplitude is smoother than that of the pole-placement controller. Because the output current amplitude was assumed to be varied from, for example, 1 to 50 A and the input-line frequency varies from 13 to 25 Hz, we can use interpolation techniques to represent k_{ij}'s of the controller-gain matrix as a function of f_i and I_{om}. First, polynomial approximations are derived for k_{ij}'s as functions of I_{om} at different input-line frequencies. For a 3rd-degree polynomial approximation, only four points along the curve are enough. The endpoints, I_{om} = 1 A and I_{om} = 50 A, and two more points along the curve are considered. For each element k_{ij}, four polynomial approximations are needed, corresponding to four different line frequencies. Again, f_i = 13Hz, f_i = 25Hz and two more input-ine frequencies are considered. Now we have four polynomials for each element as a function of the output current amplitude and corresponding to four different line frequencies:

$$(k_{ij})_{f_y} = p_{ij3y} I_{om}^3 + p_{ij2y} I_{om}^2 + p_{ij1y} I_{om} + p_{ij0y} \qquad (i = 1-4,\ j = 1-5,\ y = 1-4). \tag{10.12}$$

The term p_{ijxy} corresponds to the x^{th} coefficient of the polynomial that interpolates k_{ij} as a function of I_{om} at an input-line frequency f_y. Now, each coefficient of each polynomial has four different values corresponding to the four different input line frequencies and can be approximated by a polynomial as a function of the input-line frequency:

$$p_{ij3} = a_3 f_{in}^3 + a_2 f_{in}^2 + a_1 f_{in} + a_0 \tag{10.13}$$

$$p_{ij2} = b_3 f_{in}^3 + b_2 f_{in}^2 + b_1 f_{in} + b_0 \tag{10.14}$$

$$p_{ij1} = c_3 f_{in}^3 + c_2 f_{in}^2 + c_1 f_{in} + c_0 \tag{10.15}$$

$$p_{ij0} = d_3 f_{in}^3 + d_2 f_{in}^2 + d_1 f_{in} + d_0 . \tag{10.16}$$

Figure 10.16 shows the plot of the p_{11_x} (x = 0-3) coefficients of k_{11} as a function of the input-line frequency. The simulation results with the optimal controller implemented in Figs. 10.11 through 10.14 where executed using the controller approximation method discussed in this section. Hence, instead of finding an optimal controller online whenever the output current (i.e., load demand) or input-line frequency (i.e., wind speed) change, the new controller elements values can be calculated as follows: the a_i's, b_i's, c_i's and d_i's (i = 0-3) that are calculated offline. So, by substituting the new input-line frequency in Eqs. (10.13-10.16) and then substituting the values of p_{ij_x}'s in Eq. (10.12) along with the new value of I_{om}, the new controller elements are set up.

The method used for polynomial approximation is a basic polynomial interpolation theory, involving the *Vandermonde* matrix [37]. In brief, given n set of points (x_i , y_i) with i = *1-n*, that need to be interpolated into an n-degree polynomial of the form

$$P(x) = a_n x^n + a_{n-1} x^{n-1} + ... + a_1 x + a_0 \tag{10.17}$$

such that

$$P(x_i) = y_i . \tag{10.18}$$

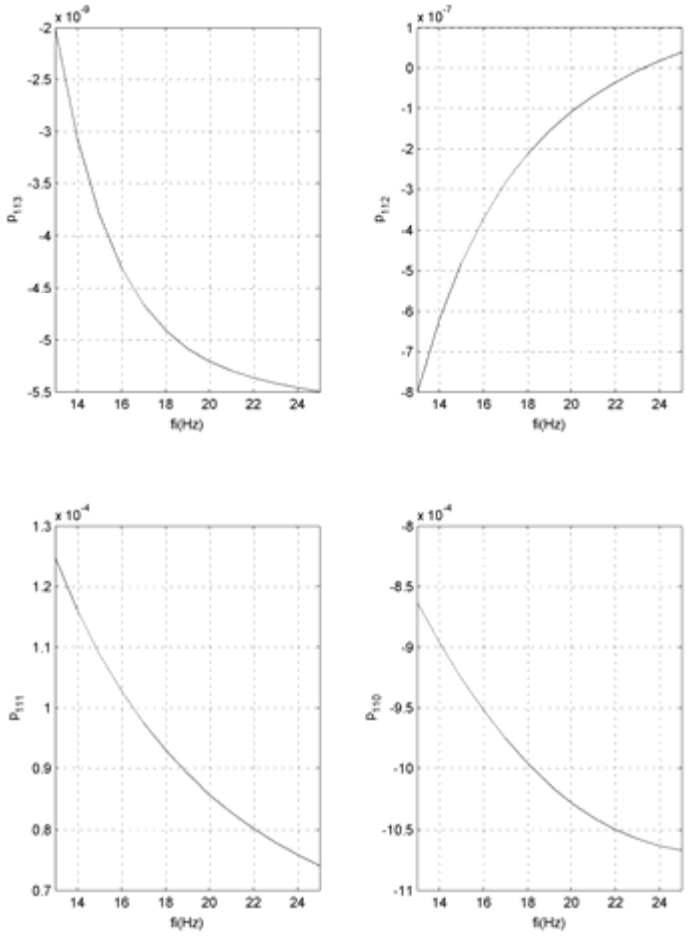


Figure 10.16: Plots of the coefficients p_{11x} (x = 0-3) as a function of the input-line frequency

By substituting Eq. (10.18) into Eq. (10.17), we obtain a system of n equations and n unknowns:

$$\begin{aligned} &a_0 + a_1 x_0 + ... + a_{n-1} x_0^{n-1} + a_n x_0^n = y_0 \\ &\qquad\qquad\qquad\qquad . \\ &\qquad\qquad\qquad\qquad . \\ &\qquad\qquad\qquad\qquad . \\ &a_0 + a_1 x_n + ... + a_{n-1} x_n^{n-1} + a_n x_n^n = y_n \end{aligned} \tag{10.19}$$

which can be put in the form

$$[X][a] = [y] \tag{10.20}$$

where

$$[X] = \left[x_{i-1}^{j-1}\right] \qquad i, j = 1,\ldots,n \tag{10.21}$$

$$[a] = [a_0 \quad . \quad . \quad a_n]^T \tag{10.22}$$

$$[y] = [y_0 \quad . \quad . \quad y_n]^T . \tag{10.23}$$

The matrix [*X*] in Eq. (10.21) is called the *Vandermonde* matrix. Equation (10.20) is a linear system of equations and can be solved by various methods, such as *Gaussian elimination* or *LU decomposition*.

10.8 Simulation Results of the Matrix Converter with all Nine Capacitors Modeled

In this chapter, two controllers have been designed using two different methods. The optimal controller design was preferred because the response of the closed-loop system settled faster than the pole-placement controller design. Also, the elements of the optimal controller-gain matrix can be expressed as functions of the parameters of the matrix converter. Simulation results were presented that demonstrated the effectiveness of the optimal controller and the controller approximation.

The state-space model of the previous chapter was derived based on the fact that only one capacitor is utilized during one switching period. It is next desired to model all nine capacitors in the simulation program, to determine the effect of capacitor switching on the controller performance. The task is done by adding the capacitor utilization scheme of Section 9.2.4 in the simulation. Instead of only one capacitor current differential equation (Eq. [9.64]), there are now nine—one for each capacitor. Whenever a capacitor is utilized, its corresponding differential equation is used on the model. The capacitor voltage initial condition equals to the last value it attained when it was last utilized, or zero at the beginning of the simulation. When another capacitor is being utilized, the capacitor voltage of the capacitor that will be turned off is held and used as capacitor voltage initial condition when utilized again.

10.8.1 Input Side: 25 Hz, 240 V, Unity Power Factor; Output Side: 60 Hz, 240 V, 20 A, Unity Power Factor

Figure 10.17 shows the simulation results when the input side (e.g., generator) is operating at 240 V, unity power factor with an input line frequency of 25 Hz. The output side (e.g., utility) is operating at 240 V, 60 Hz with an output demand of 20 A at unity power factor. The figure shows the transient response to the nine capacitor voltages, the *dq* input currents, and the *dq* output current.

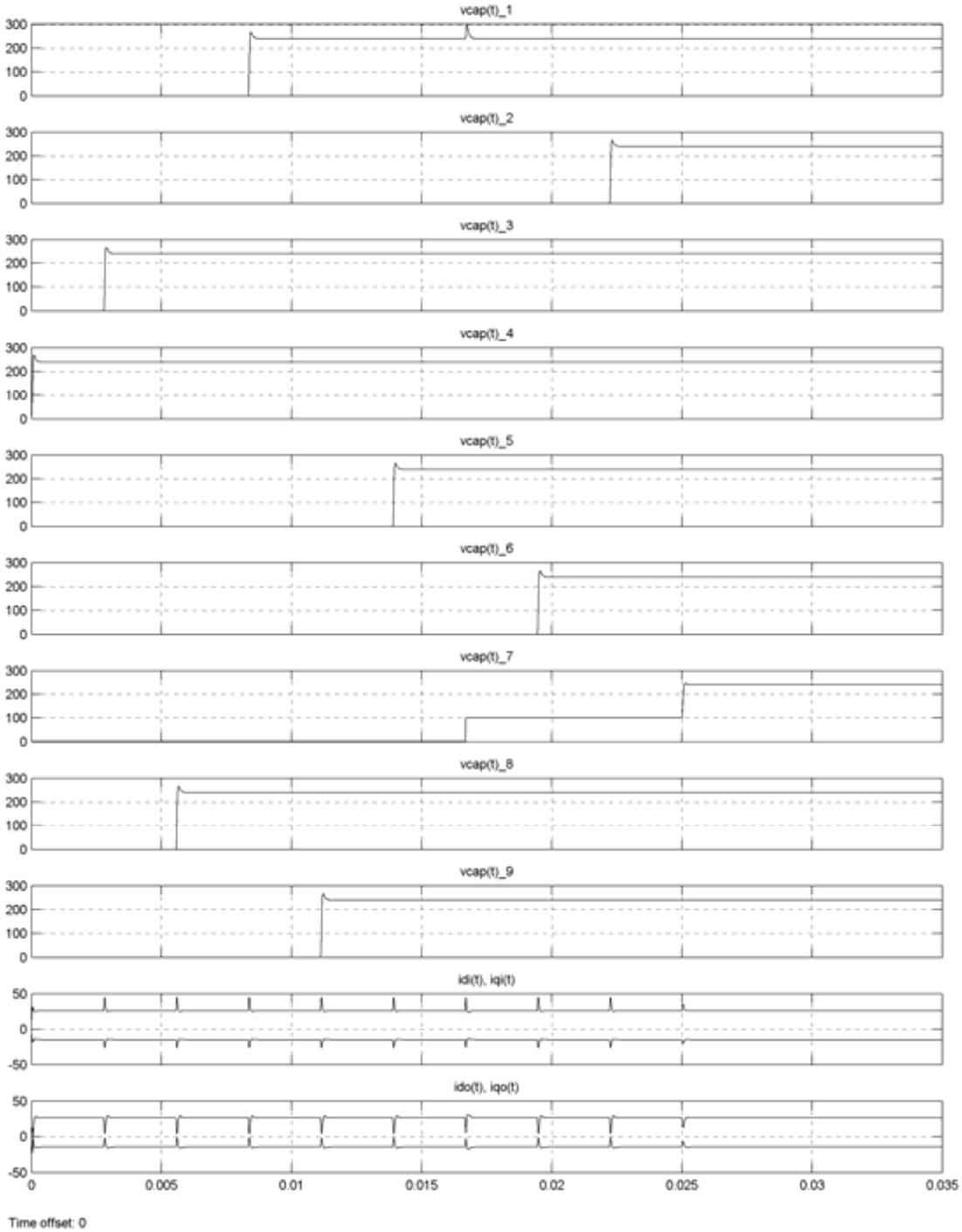


Figure 10.17: Simulation results for the following operating point:
Input side: 240 V, 25 Hz, unity power factor
Output side: 240 V, 60 Hz, 20 A, unity power factor
The first nine parts are the capacitor voltages responses, the tenth part is the input *dq* currents responses, and the last part is the output *dq* currents responses

10.8.2 Input Side: 25 Hz, 240 V, Unity Power Factor; Output Side: 60 Hz, 240 V, 20 A, 0.5 Power Factor

Figure 10.18 shows the simulation results when the input side (e.g., generator) is operating at 240 V, unity power factor with an input line frequency of 25 Hz. The output side (e.g., utility) is operating at 240 V, 60 Hz with an output demand of 20 A at 0.5 power factor (i.e., 50% real power transfer). The figure shows the transient response to the nine capacitor voltages, the *dq* input currents, and the *dq* output current.

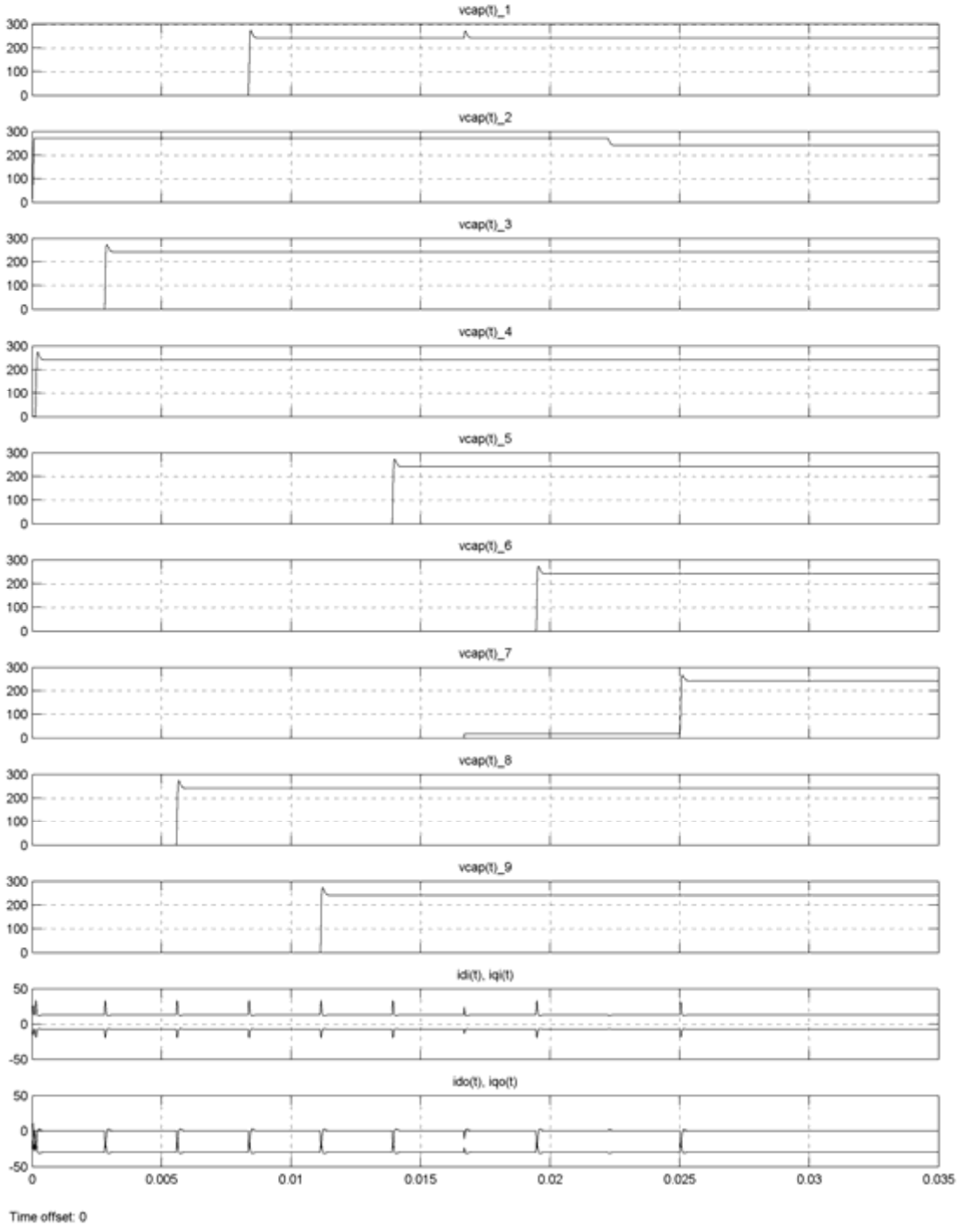


Figure 10.18: Simulation results for the following operating point:
Input side: 240 V, 25 Hz, unity power factor
Output side: 240 V, 60 Hz, 20 A, 0.5 power factor
The first nine parts are the capacitor voltages responses, the tenth part is the input *dq* currents responses, and the last part is the output *dq* currents responses

10.8.3 Input Side: 13 Hz, 240 V, Unity Power Factor; Output Side: 60 Hz, 240 V, 20 A, Unity Power Factor

Figure 10.19 shows the simulation results when the input side (e.g., generator) is operating at 240 V, unity power factor with an input line frequency of 13 Hz. The output side (e.g., utility) is operating at 240 V, 60 Hz with an output demand of 20 A at unity power factor. This operating point corresponds to the lowest operating condition of the matrix converter under two-level modulation. The figure shows the transient response to the nine capacitor voltages, the *dq* input currents, and the *dq* output current.

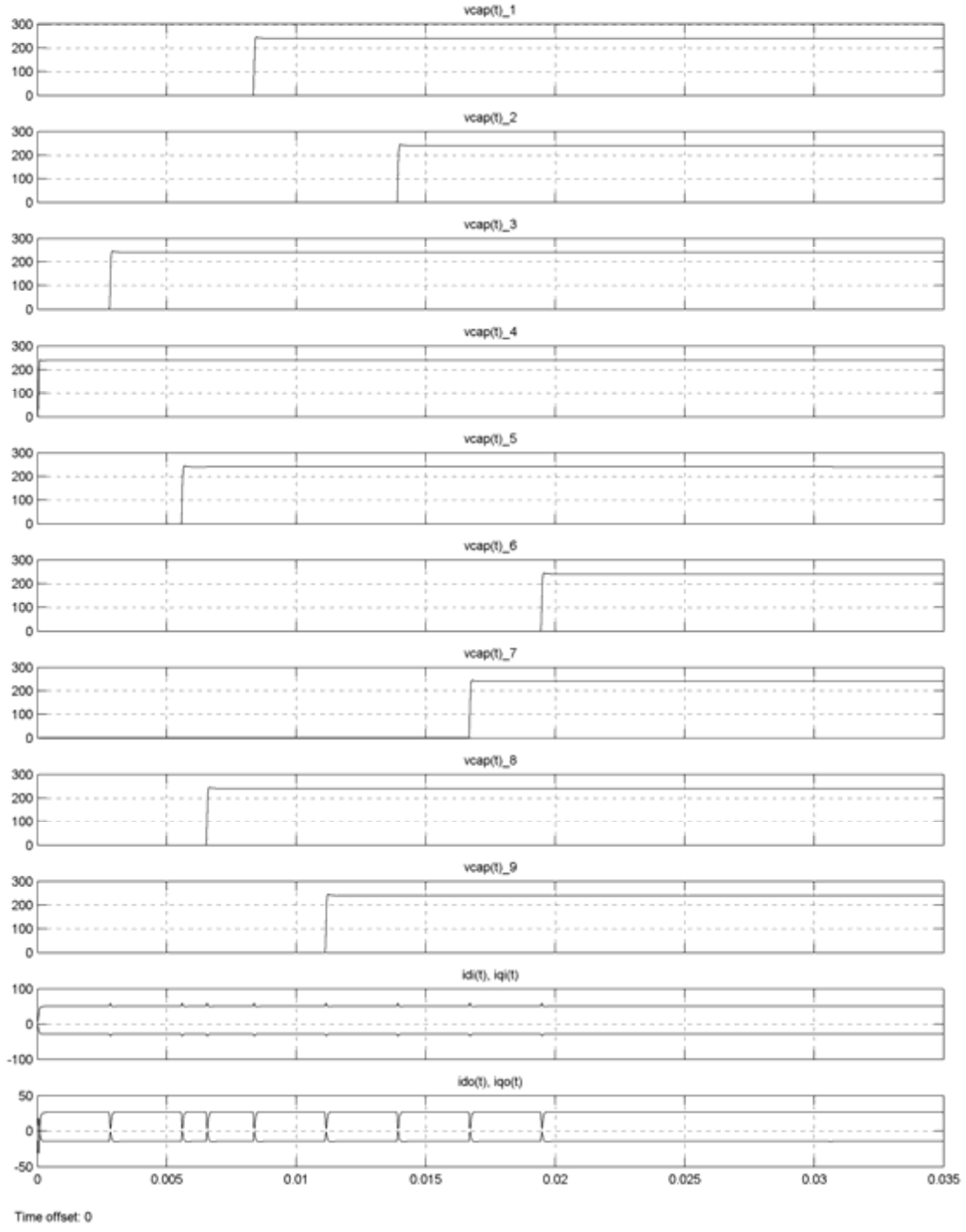


Figure 10.19: Simulation results for the following operating point:
Input side: 240 V, 13 Hz, unity power factor
Output side: 240 V, 60 Hz, 20 A, unity power factor
The first nine parts are the capacitor voltages responses, the tenth part is the input *dq* currents responses, and the last part is the output *dq* currents responses

10.8.4 Input Side: 13 Hz, 240 V, Unity Power Factor; Output Side: 60 Hz, 240 V, 20 A, 0.5 Power Factor

Figure 10.20 shows the simulation results when the input side (e.g., generator) is operating at 240 V, unity power factor with an input line frequency of 13 Hz. The output side (e.g., utility) is operating at 240 V, 60 Hz with an output demand of 20 A at 0.5 power factor (i.e., 50% real power transfer). This operating point is similar to that of Section 10.8.7 but with 50% real power demand. The figure shows the transient response to the nine capacitor voltages, the *dq* input currents, and the *dq* output current.

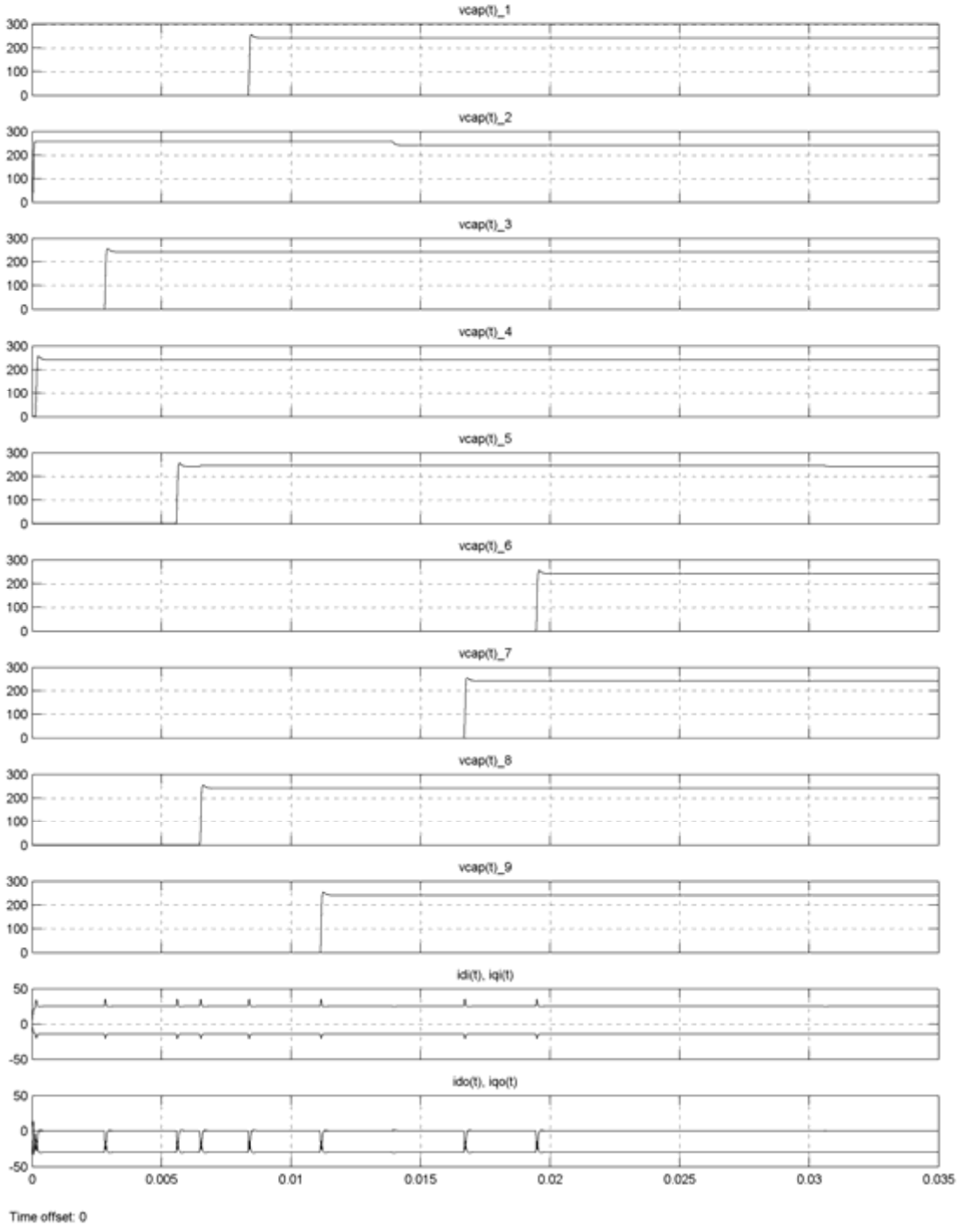


Figure 10.20: Simulation results for the following operating point:
Input side: 240 V, 13 Hz, unity power factor
Output side: 240 V, 60 Hz, 20 A, 0.5 power factor
The first nine parts are the capacitor voltages responses, the tenth part is the input *dq* currents responses, and the last part is the output *dq* currents responses

11 Experimental Results: Closed-Loop Control

In this chapter, physical tests demonstrate and prove the validity of both the mathematical modeling and feedback control of the matrix converter. Figure 11.1 shows an overall block diagram of the prototype of the matrix converter described in Part I and implemented in our laboratory at the University of Colorado [48]. The input side of the converter is fed by the utility (three-phase 240 V, 60 Hz source) that can be adjusted by a variac. The output side is a three-phase resistive load. Experimental results will be based on varying the output current, output frequency, and input voltage of the matrix converter. From the block diagram, the laboratory setup of the matrix converter can be divided into two parts, a *power stage* and a *control stage*.

11.1 Power Stage of the Matrix Converter Prototype

The power stage of the matrix converter prototype is composed of the nine H-bridge switch cells. Each cell is constructed of four IGBT devices that include anti-parallel diodes and one DC bus capacitor. Details of the converter construction are documented in Part I and will not be repeated here.

Input and output current and voltage signals are sensed by Hall-effect devices. Those signals are then digitized by feeding them to ADCs and fed into a PowerPC microcontroller embedded into the Virtex II-PRO FPGA . The voltages across the capacitors of the nine switch cells are measured by employing differential amplifier circuits; they are then digitized by feeding them to the ADCs and fed to the microcontroller. The output of the FPGA is fed into opto-isolated gate-driver circuits.

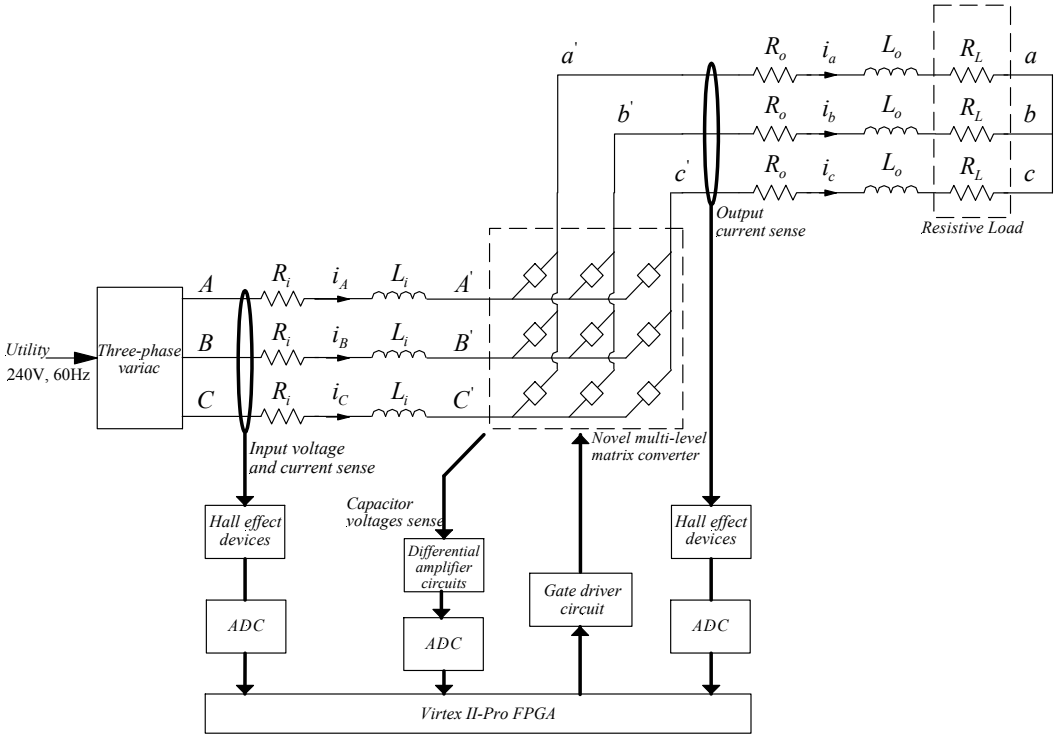


Figure 11.1: Block diagram of the prototype matrix converter

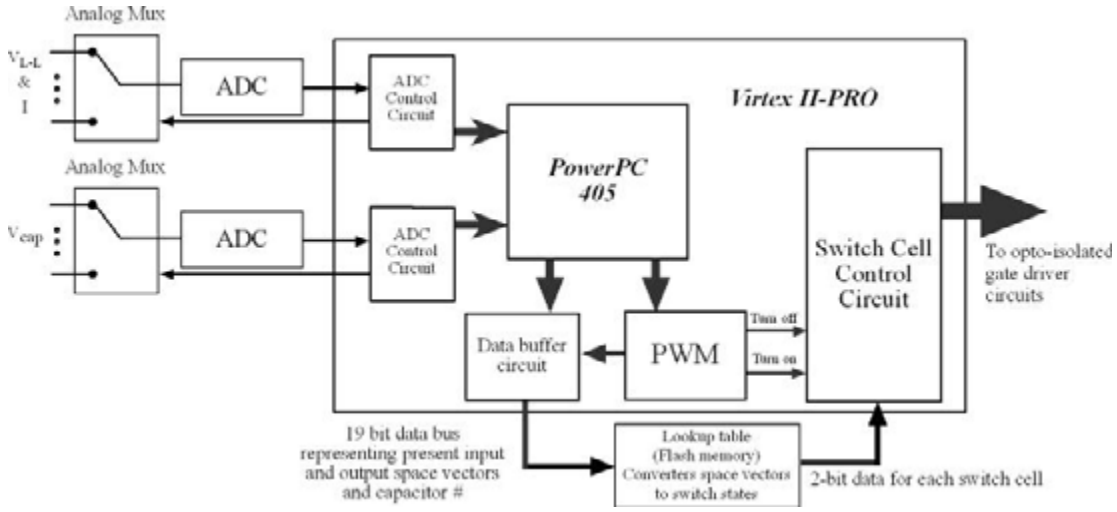


Figure 11.2: Block diagram of the VIRTEX II-PRO FPGA

The operation of the microcontroller is as follows:

1. Read input voltage and transform into rotating *dq* frame to locate the input space vector and find the magnitude of the input voltage
2. Given output frequency, current, input and output power factors, find the steady-state solution of the matrix converter
3. Generate output space vector and find its location
4. Read input and output currents, and transform them into stationary *dq* frame
5. Calculate duty cycles and determine the single capacitor
6. Read the voltage across the utilized capacitor then implement feedback control routine
7. In the feedback control routine (Fig. 10.4), the input and output *dq* currents and the utilized capacitor voltage are compared to a reference value. The results (error signals) are multiplied by the *control-gain matrix*. The output of the control matrix is the variation in the *dq* control, which is added to the steady-state control to get new modulation indices and displacement angles and, hence, new space vectors for both input and output.
8. Calculate new duty cycles and generate switching sequence
9. Send results (duty cycles, switching sequence, and utilized capacitor) to the logic control devices
10. Go to step 1 for next switching period.

The code was implemented in the microcontroller using PPC assembly language [46]. The data buffer stores the utilized capacitor number, as well as the input and output space vectors for each subinterval. The lookup table decodes input and output space vectors data for the current subinterval from the data buffer. It then provides logic signals that command each switch cell. The PWM latches five sets of data from the microcontroller that represent the number of clock ticks for the length of each subinterval. The switch-cell control circuit provides suitable logic signals to the individual gate drivers based on their inputs taken from the outputs of the lookup table.

Cross-conduction of the IGBTs during switching transitions would lead to shorting of the DC bus voltages through the IGBTs. To avoid such incidents, the switching of the IGBTs that were on previously but will be turned off takes place first. Then, after some delay (200 nsec), the turn-on transitions are triggered.

11.2 Steady-State Solution of the Matrix-Converter Prototype

The solution of the matrix-converter model in the laboratory is presented in Eqs. (9.102-9.106) with the following adjustments:

- The output line resistance R_o is that of the filter inductance resistance (3 mΩ) plus the output load (10 Ω). That resistance can be approximated to just the output load resistance because it is much larger than the resistance of the filter inductance.
- Because the output side of the matrix converter is connected to a resistive load, which is set to be the output line resistance, the output voltages (V_{an}, V_{bn}, and V_{cn} in Fig 3.1) are set to zero as shown in Fig. 11.1.

Examination of Eqs. (9.102-9.106) reveals that the changes apply to Eqs. (9.102) and (9.104). The results are

$$V_{Tdo} = \frac{3\sqrt{3}}{2} I_{om} \left(\cos\left(\Theta_{pfo}\right) R_o - \sin\left(\Theta_{pfo}\right) L_o \omega_o \right) \tag{11.2}$$

$$V_{Tqo} = \frac{3\sqrt{3}}{2} I_{om} \left(\sin\left(\Theta_{pfo}\right) R_o + \cos\left(\Theta_{pfo}\right) L_o \omega_o \right) \tag{11.3}$$

$$I_{im} = \frac{V_{im} \cos\left(\Theta_{pfi}\right) - \sqrt{\left(V_{im} \cos\left(\Theta_{pfi}\right)\right)^2 - 12 R_i R_o I_{om}^2}}{2\sqrt{3} R_i} \tag{11.4}$$

$$V_{Tdi} = \frac{3}{2} \left(V_{im} - \sqrt{3} I_{im} \left(\cos\left(\Theta_{pfi}\right) R_i - \sin\left(\Theta_{pfi}\right) L_i \omega_i \right) \right) \tag{11.5}$$

$$V_{Tqi} = -\frac{3\sqrt{3}}{2} I_{im} \left(\sin\left(\Theta_{pfi}\right) R_i + \cos\left(\Theta_{pfi}\right) L_i \omega_i \right) \tag{11.6}$$

Table 11.1 shows the steady-state solution of the prototype matrix converter for several operating points. The capacitor voltage V_{cap} is set to the maximum of the voltages across the terminals plus 5 V.

Table 11.1: Steady-State Solution for Various Operating Points

Input Voltage (V)	Input Current (A)	Input Power Factor	Capacitor Voltage (V)	Output Current (A)	Output Frequency (Hz)
240	7.218	1	244.9643	10	30
240	14.4428	0.5	243.3307	10	30
50	8.6681	1	91.6050	5	60
50	17.3833	0.5	91.6050	5	60

11.3 Poles and Feedback Control of the Linear Model

The linearized state-space model of the prototype matrix converter can be found by inserting values of its parameters in the equations of Section 9.5.3. However, the poles of the system are not quite the solution of the characteristic equations of Section 9.6 (Eqs. [9.122] and [9.123]) because of the fact that the input-line resistance and the output-line resistance are not the same (that is: $R_i \neq R_o$) and because of the resistive load. The characteristic equation is, after simplifications

$$
\begin{aligned}
p(s) = {} & s^5 + 2\left(\frac{R_i + R_o}{L}\right)s^4 + \left(\left(\frac{R_i^2 + 4R_iR_o + R_o^2}{L^2}\right) + \frac{M_i^2 + M_o^2}{2LCap} + \omega_i^2 + \omega_o^2\right)s^3 \\
& + \left(2\left(\frac{R_i^2R_o + R_o^2R_i}{L^3}\right) + \frac{R_i\left(M_i^2 + 2M_o^2\right) + R_o\left(M_o^2 + 2M_i^2\right)}{2L^2Cap} + 2\left(\frac{R_o\omega_i^2 + R_i\omega_o^2}{L}\right)\right)s^2 \\
& + \left(\left(\frac{R_iR_o}{L^2}\right)^2 + \frac{(M_oR_i)^2 + 2R_iR_o\left(M_i^2 + M_o^2\right) + (M_iR_o)^2}{2L^3Cap} \right. \\
& \left. + \frac{(R_o\omega_i)^2 + (R_i\omega_o)^2}{L^2} + \frac{(M_i\omega_o)^2 + (M_o\omega_i)^2}{2LCap} + (\omega_i\omega_o)^2\right)s \\
& + \left(\frac{R_o(M_oR_i)^2 + R_i(M_iR_o)^2}{2L^4Cap} + \frac{R_o(M_o\omega_i)^2 + R_i(M_i\omega_o)^2}{2L^2Cap}\right) \\
= {} & 0
\end{aligned}
\tag{11.7}
$$

Table E.1 in Appendix E shows a list of poles of the prototype converter at various operating points. Note that because of the resistive load, the real part of the open-loop poles are much farther from the imaginary axis than those discussed in Section 9.6. The effect of that will be discussed later.

The design of the feedback controller of the linear model is solely based on *optimal controller design* discussed in Section 10.5. In Appendix E, Table E.2 shows the elements of the controller-gain matrix as three chosen parameters (output line-current amplitude and frequency, and input line-voltage amplitude) vary. The table shows that the elements of the controller-gain matrix depend on all three parameters, unlike what was discussed in Chapter 10, where they depend on the output current and input-line frequency (and, hence, the input-line voltage). However, the dependency of those elements on the output-

line frequency is minor compared to their dependency on input-line voltage and the output-line current. Therefore, that dependency will be neglected.

The procedure of finding the relationship between the elements of the controller-gain matrix and the varying parameters is used. The only difference is that, instead of using the input-line frequency (Section 10.7), the input-line voltage is used. The results are summarized in Table E.3 of Appendix E.

11.4 Comments on Response Latency

In Chapter 10, it was shown that the closed-loop response of the non-linear model of the matrix converter has a very short time constant. That is, a high switching frequency is necessary in order to achieve this fast response. The matrix-converter model in the laboratory operates at a switching frequency of 20 kHz. Moreover, the control code, programmed in PPC assembler, was observed to exhibit a latency approaching 100 μsec so that it updates the control (sends duty cycles to CPLDs) every other switching period (10 kHz). SIMULINK simulation experiments, when the step size is set to 100 μsec, predict instability. This can also be seen from the open-loop poles (the solution of Eq. [11.7] for several operating points) in Table E.1. Because of the increase in the output-line resistance, the poles are already far from the imaginary axis (recall from Section 9.6 that the real part of the open-loop poles depends almost linearly on *R/L* factor). All modes of the closed-loop response must be sufficiently slower than the controller latency time; otherwise the optimal control technique is unable to find a stable controller.

To enable control with a 100-μsec latency time, the output filter inductors have been replaced with larger 8-mH laminated inductors. This reduced the *R/L* natural frequencies so that the open-loop poles will move closer to the imaginary axis. The response time constant would be longer that will make the settling time at least several switching periods.

Table F.1 in Appendix F shows the open-loop poles of the matrix converter model calculated for several operating points. Note how the real part of the open-loop poles is now closer to the imaginary axis. Table 11.2 shows those poles taken from both Table E.1 and Table F.1 for several operating points.

Table 11.2: Open-Loop Poles of the Matrix Converter when L_o = 0.2 mH, Compared to the Open-Loop Poles when L_o = 8mH

Operating point				Open-loop poles	
V_{im}(V)	I_{im}(A)	f_o(Hz)	I_{om}(A)	L_o = 0.2 mH (Table E.1)	L_o = 8 mH (Table F1)
35.0	0.5	20.0	1.0	-475.55 ± *j*14403 -15.685 -49081, -49983	-11.267 ± *j*14319 -15.694 -1245.9 ± *j*125.25
45.0	0.39	40.0	1.0	-304.02 ± *j*14767 -15.411 -49548, -49859	-9.857 ± *j*14710 -15.416 -1247.4 ± *j*250.89
55.0	7.96	60.0	5.0	-2527.7 ± *j*10044 -21.991 -44984, -49969	-45.971 ± *j*9730.7 -22.09 -1208 ± *j*364.11

Table F.2 shows how the elements of the controller-gain matrix vary at different operating conditions (similar to Table E.2). The coefficients that define the elements of the controller-gain matrix, as functions

of the amplitude of the output line currents and the amplitude of the input line voltages, is shown in Table F.3.

11.5 Implementation of the Control Code

The code used to implement the feedback control of the matrix converter model is shown in Appendix G. The following steps for the implementation are highlighted in the code:

1. Read the input line-to-line voltages $v_{AB}(t)$ and $v_{BC}(t)$. Transform into the rotating $\alpha\beta$ frame, find the amplitude and the location of the input space vector as follows:

$$v_\alpha = v_{AB}(t) = V_{im}\cos(\omega_i t) \tag{11.8}$$

$$v_\beta = \frac{v_{AB}(t) + 2v_{BC}(t)}{\sqrt{3}} = V_{im}\sin(\omega_i t) \tag{11.9}$$

$$V_{im} = \sqrt{v_\alpha^2 + v_\beta^2} \tag{11.10}$$

$$\omega_i t = \arctan\left(\frac{v_\beta}{v_\alpha}\right). \tag{11.11}$$

2. Find the steady-state solution: Given the output current amplitude I_{om}, output frequency f_o, output power factor pf_o, input power factor pf_i, and input voltage amplitude V_{im}, the steady-statesolution is presented by Eqs. (11.2-11.6). The amplitude of the voltages across the matrix converter terminals is (for $x = i, o$):

$$V_{xm'} = \sqrt{V_{Tdx}^2 + V_{Tqx}^2}\ . \tag{11.12}$$

The displacement angle between the input-line voltages and the matrix converter's input terminals, as well as the displacement angle between the output-line voltages and the matrix-converter's output terminals is (for $x = i, o$)

$$\Theta_x = \arctan\left(\frac{V_{Tqx}}{V_{Tdx}}\right). \tag{11.13}$$

The capacitor voltage, input/output modulation indices, the input/output dq control $\lfloor \Gamma_{dx} \quad \Gamma_{qx} \rfloor$, and the input reference vector ([X] in Eq. [10.5]) are then calculated. Finally, the location of the input-voltage space vector $v_{i\_ref}(t)$ is calculated by finding the angle ϕ_i and the sector.

3. Generate an output space vector based on the output-line frequency. The location of that vector $(\omega_o t)$ is then added to the output displacement angle Θ_o to find the angle ϕ_o and the sector where it resides.

4. Read actual input- and output-line currents and transform into stationary dq frame. The actual amplitudes and power factors are then calculated. For the input side:

$$i_\alpha = \frac{2i_A - i_B - i_C}{3} \tag{11.14}$$

$$i_\beta = \frac{i_B - i_C}{\sqrt{3}} \tag{11.15}$$

$$\begin{bmatrix} i_{di}(t) \\ i_{qi}(t) \end{bmatrix} = \begin{bmatrix} T_{dq} \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \tag{11.16}$$

$$i_{im}(t) = \sqrt{i_{di}^2(t) + i_{qi}^2(t)}\,. \tag{11.17}$$

Similar calculations are applied to the output side.

5. Calculate the duty cycles (d_l , d_k , d_{0_i} , d_m , d_n, and d_{0_o}). Based on that, determine the utilized capacitor and read its actual voltage.

6. Compare the actual values of the input/output currents and utilized capacitor voltage to their corresponding reference values. The result (error signal) is fed to the controller-gain matrix.

7. Find the output of the controller-gain matrix from multiplying the controller-gain matrix by the error signal found in step 6. The result is the variation in the *dq* control $\begin{bmatrix} \hat{\gamma}_{di}(t) & \hat{\gamma}_{qi}(t) & \hat{\gamma}_{do}(t) & \hat{\gamma}_{qo}(t) \end{bmatrix}$. That control is added to its steady-state counterpart found in step 2 to get the time-dependent control $\begin{bmatrix} \gamma_{di}(t) & \gamma_{qi}(t) & \gamma_{do}(t) & \gamma_{qo}(t) \end{bmatrix}$.

8. From the input time-dependent control, find the new input modulation index and displacement angle. Then find the new location of the input space vector by finding the angle ϕ_i and the sector where it resides. Finally, calculate the new input-side duty cycles. Check if they are valid by determining if d_0 is less than 1; if invalid, then the angle ϕ_i is kept as it is and the modulation index is varied such that d_0 is at its minimum.

9. Repeat step 8 for the output side.

10. Generate the switching sequence based on the duty cycles in step 9 and send the output to the CPLDs (Fig. 11.2)

11. Go to step 1 to compute the control for the next time step.

11.6 Measured Results

The feedback control designed for the matrix-converter prototype in the laboratory was tested with two types of variations or disturbances: output current variations and output frequency variations. The main assembly code was modified to simulate the change. For example, the converter is commanded to run for several seconds (e.g., 15 seconds) at one operating condition, e.g., 30-Hz output-line frequency. Then, the code changes that frequency to a different value (e.g., 60 Hz). After 15 seconds, the code changes the frequency back and so on.

For all results, the input line-to-line voltage was approximately 30 V RMS, the input frequency was 60 Hz, and both input and output power factors were 0.99. Moreover, the controller-gain matrix was chosen to be a constant matrix to avoid more delays in the calculations. The controller-gain matrix implemented is:

$$[K] = \frac{1}{1024}\begin{bmatrix} -1 & -20 & 1 & 0 & 0 \\ 1 & 1 & -20 & 0 & 0 \\ -1 & 0 & 0 & 1 & -1 \\ 1 & 0 & 0 & -1 & 1 \end{bmatrix}. \tag{11.18}$$

The value of the controller-gain matrix implemented [*K*] is found using the optimal controller design discussed in Sec. 10.5. It is represented in the form of Eq. (11.18) to easily implement in the PPC assembler. The zero values in Eq. (11.18) are very small compared to the other nonzero elements and can be neglected.

11.6.1 Experimental Results: Output Current Varies from 1 A to 0.5 A

Figure 11.3 shows response of the voltage across one capacitor, one output-line current, and one output

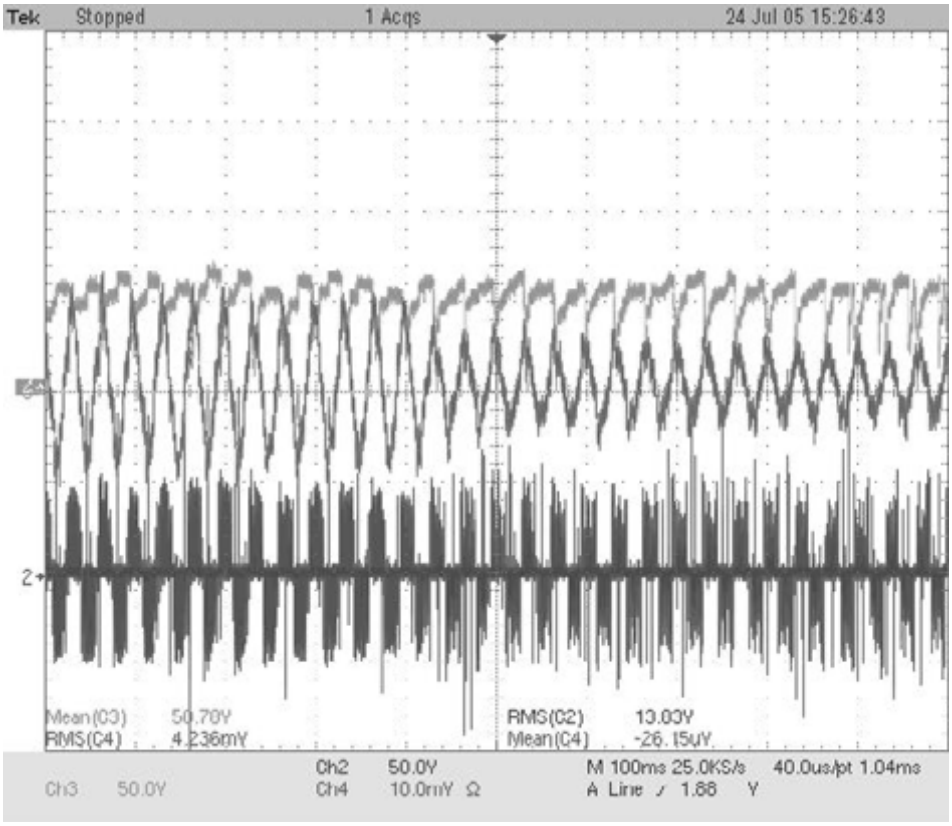


Figure 11.3: Experimental results of the matrix converter prototype when the output-line current changes from 1 A to 0.5 A amplitude:
Top trace: capacitor voltage
Middle trace: output current
Bottom trace: output line-to-line voltage

line-to-line voltage (across the converter's output terminals) of the matrix converter when the output current makes a step change from 1 A to 0.5 A amplitude. The capacitor voltage is at about 50 V, which equals to the steady-state input terminal voltage of the matrix converter plus about 5 V. The output current amplitude changes to 0.5 A without any unusual interruptions or unwanted transients.

11.6.2 Experimental Results: Output-Line Frequency Varies from 30 Hz to 60 Hz

Figure 11.4 shows the response of the voltage across one capacitor, one output-line current, and one output line-to-line voltage (across the converter's output terminals) of the matrix converter when the output-line frequency changes from 30 Hz to 60 Hz. The output current amplitude is set to about 0.75 A. The average capacitor voltage is at about 40 V, which equals to the steady-state input terminal voltage of the matrix converter. Note how the output-line frequency changes to 60 Hz without any unusual interruptions or unwanted transients in the output current and voltage responses.

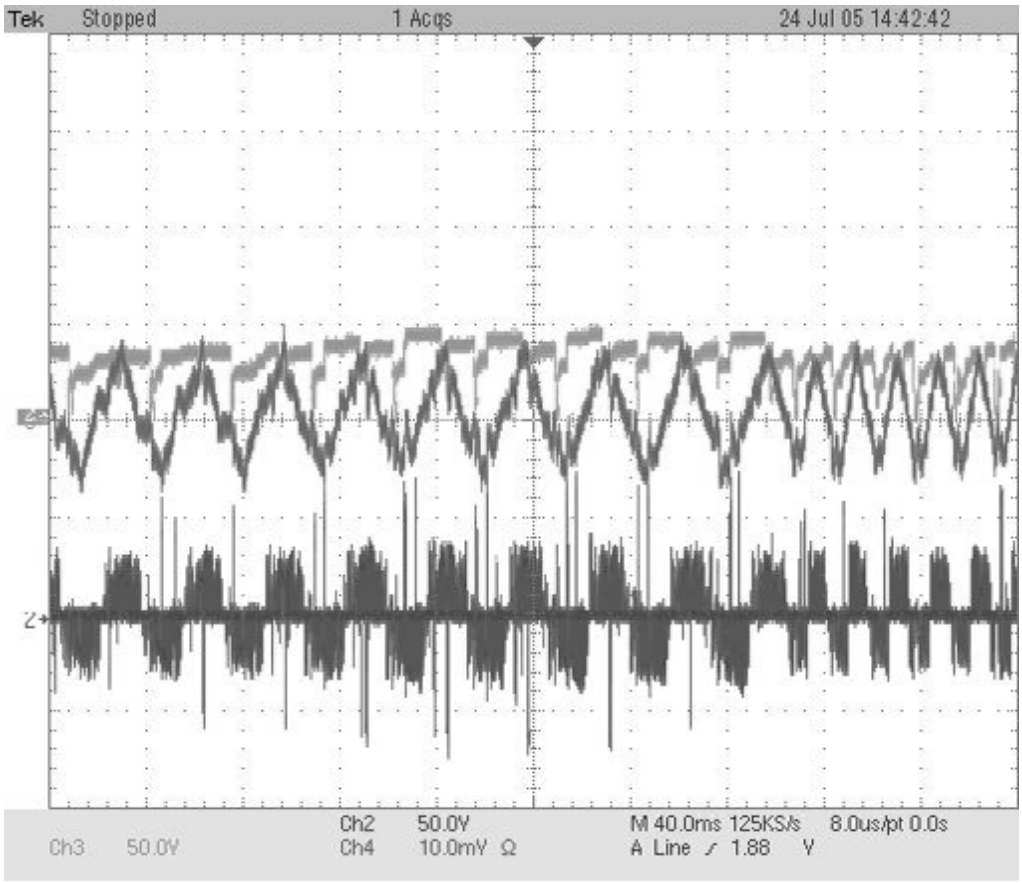


Figure 11.4: Experimental results of the matrix-converter prototype when the output-line frequency changes from 30 Hz to 60 Hz:
Top trace: capacitor voltage
Middle trace: output current
Bottom trace: output line-to-line voltage

12 Conclusions to Part II

12.1 Summary of Part II

The new modular matrix converter is a valuable tool to transfer power from a variable-speed wind power system to the utility system. With each capacitor being embedded in each switch cell, the stress on the power semi-conducting devices is lessened. Moreover, by using space-vector control, the matrix converter links the two systems to transfer power, while maintaining the capacitor voltages of the switch cells at the desired level. However, current feedback control plays a crucial part in assuring maximum power transfer at highest efficiency possible while maintaining desired capacitor voltage levels.

A strategy to model and then to control the currents and the capacitor voltages of the novel modular matrix converter is presented in this part of the report. The differential equations derived to describe the variables to be controlled (input/output currents and capacitor voltages) show how the matrix-converter parameters interact. The nonlinearity in the four-input five-output state-space model derived from those differential equations led to manipulating it and separating it into a nominal (steady-state) model and a small-signal linear model. The steady-state model describes how the converter operated under steady-state conditions, with no variations. Given the known operating conditions (input/output voltages, output current, and input/output power factors), the solution of the steady-state model shows what the input current and the utilized capacitor voltage should be at the operating point of maximum power transfer. Also, it is illustrated that the elements of the linear time-invariant state-space model are dependent on the solution of the steady-state model.

The state variables (input/output currents and capacitor voltage) in the linearized state-space model represent the variations in their corresponding state variables in the nonlinear model. The controller attempts to drive these variations to zero so that the outputs of the nonlinear model, which are the state variables, follow the desired steady-state values. Hence, design of such a feedback controller requires an investigation of the linearized state-space model. This model is developed in Chapter 9. The stability of the open-loop linearized state-space model is an essential requirement for feedback controller design. So, the model was tested for stability under all possible operating conditions. The poles of the model, which are the roots of the characteristic polynomial, were shown to be stable. In fact, the real parts of those poles, which determine the stability of the open-loop system, were dependent almost linearly on the input/output filter inductances and resistances.

The decision on which controller design method to choose was based on how the controller gains vary as the operating point of the matrix converter varies. Those variables that are most likely to vary are wind speed (i.e., the input-line voltages and frequency), output power demand (i.e., output current and power factor), and the capacitor voltages when switching between switch cells. The pole-placement method was investigated first because of its simplicity in finding a controller-gain matrix by placing the open-loop poles at a desired location. However, when checking how the elements of the controller-gain matrix change as the variables discussed change, the pole-placement controller was found to be sensitive and no simple relationship could be found, although those elements depend only on the input-line frequency and output-current amplitude. That turned the attention toward optimal control. The optimal-controller technique was found to be superior to the pole-placement controller. The settling times, when an optimal controller is implemented, were much faster. It is important that capacitor voltages exhibit short settling times. Although only one capacitor is utilized in each switching period, utilization of the nine capacitors varies as the space vectors rotate, with the period of utilization of each capacitor being dependent on the

locations of the input/output reference voltage space vectors. Therefore, if there is a difference in voltage between two capacitors when switching from one to the next, that difference has to be minimized with short settling time.

The relationships between the controller gains and the matrix-converter parameters were much clearer in the optimal controller method than that in the pole-placement method. The elements of the optimal controller-gain matrix, like those of the pole-placement controller, depend only on the input-line frequency and the output-current amplitude. However, those relationships were found to be more straightforward and could be very accurately approximated by a 3rd-degree polynomial. The simulation results of the closed-loop overall model with an optimal feedback controller implemented prove the validity of this approach.

The next step was to investigate the response of all nine capacitors. The assumption was that all capacitors are discharged (i.e., capacitor voltages are zero) and the simulation time is enough to have all nine capacitors utilized. Switching of the capacitors was implemented in the simulations. Indeed, the capacitor voltages reach their nominal values very fast while the transient responses of the currents, as a result of capacitor switching, were minimal.

The novel modular matrix converter was designed to be universal and so is this controller design strategy. That is, the matrix converter was developed to transfer power between any two systems regardless of the output power demand or the input power factor. The same applies when modeling the converter to design a state feedback controller to control its capacitor voltages and currents; the nonlinear state-space model is valid, as well as its steady-state and linearized state-space models. The optimal controller must be recalculated for various operating points, and the relationships between the controller and the operating point parameters can be approximated.

Simulation results clearly show that a feedback controller plays an important part in charging the capacitors to their nominal value, as well as transferring power from the input side to the output side. Also, the controller is important when switching from one operating condition to another; a change in wind speed and, hence, change in the input-line frequency and input-line voltages or change in output power demands expressed by the output currents and output power factor.

Experimental results verify the modeling and control of the matrix converter. Although the matrix converter prototype in the laboratory was set up differently than what was discussed in this report (input side is connected to the utility and the output side is connected to a resistive load), the modeling and control schemes are still valid. It was shown that the elements of the optimal controller-gain matrix of the prototype matrix converter depend on variables different than what was discussed in Chapter 10. Nonetheless, the strategy of designing a controller-gain matrix that varies as the matrix-converter parameters vary is still valid, and an operating controller was demonstrated.

The matrix-converter prototype in the laboratory operates with natural time constants that are comparable to the response time of the open-loop controller system. Hence, a stable controller design could not be found. That led to one of the following options: either increase the controller clock frequency or increase the converter reactive element values. The second option was used. The implementation was simply to connect larger filter inductors in one side of the matrix converter. The resulting laminated inductors are a practical and low-cost solution. Experimental results for multiple operating conditions were presented that prove the validity of the two main points of this dissertation: the validity of the matrix-converter model (i.e., differential equations derivation, linearization, … etc.) and the validity of the feedback control strategy implemented (i.e., defining controller-gain matrix whose elements vary as certain parameters of the matrix converter vary).

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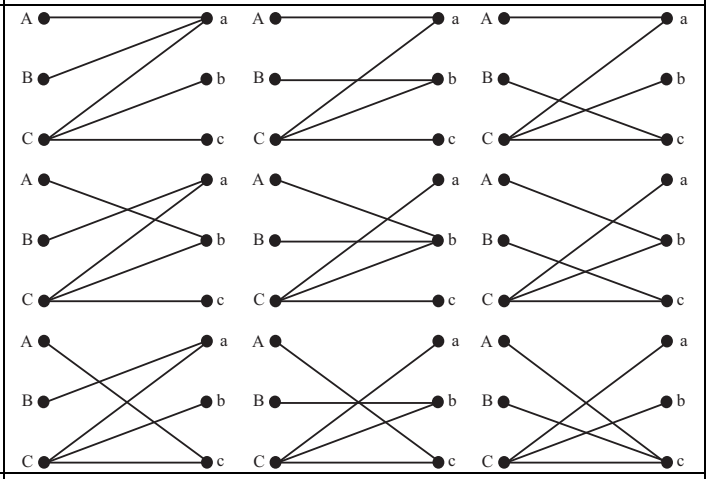
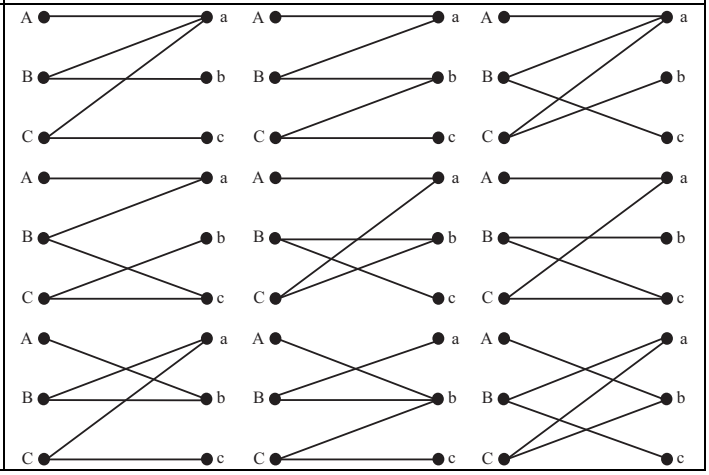
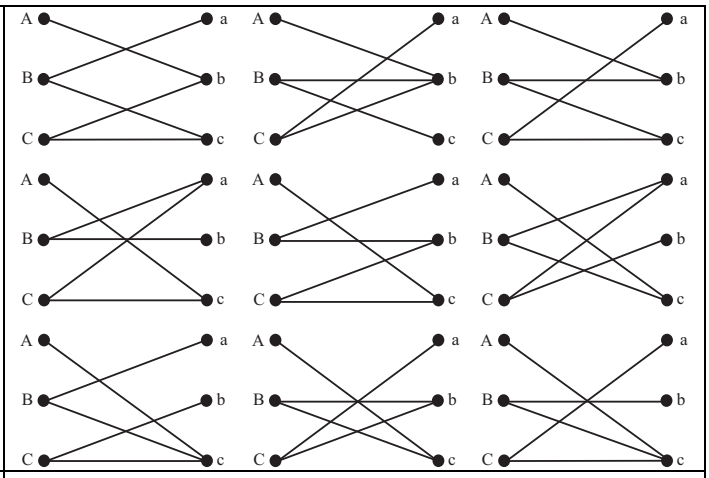
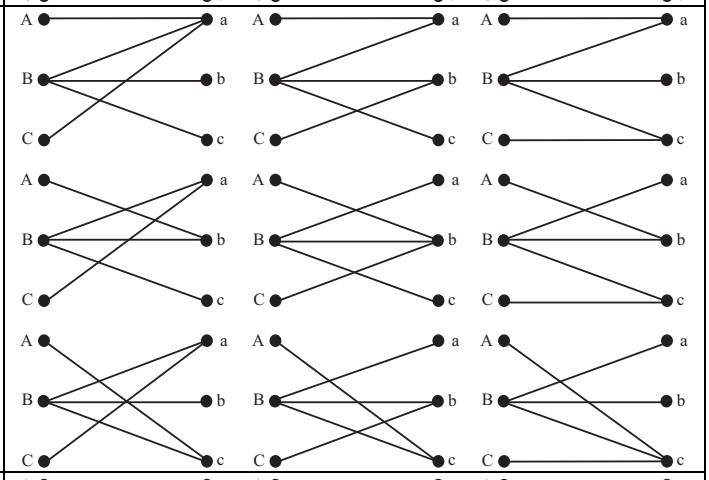
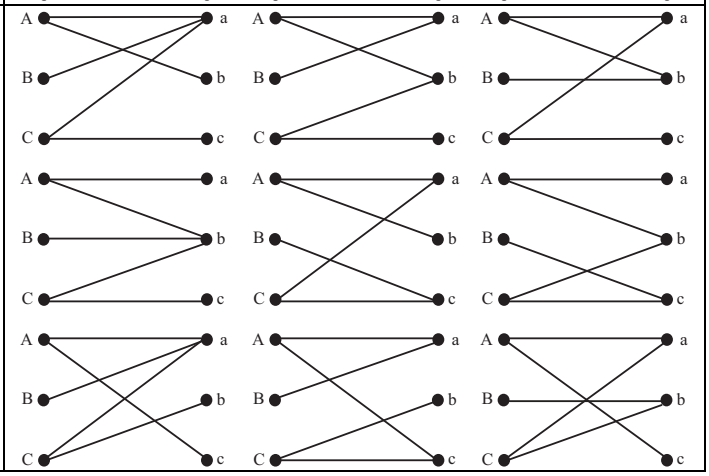
APPENDIX A

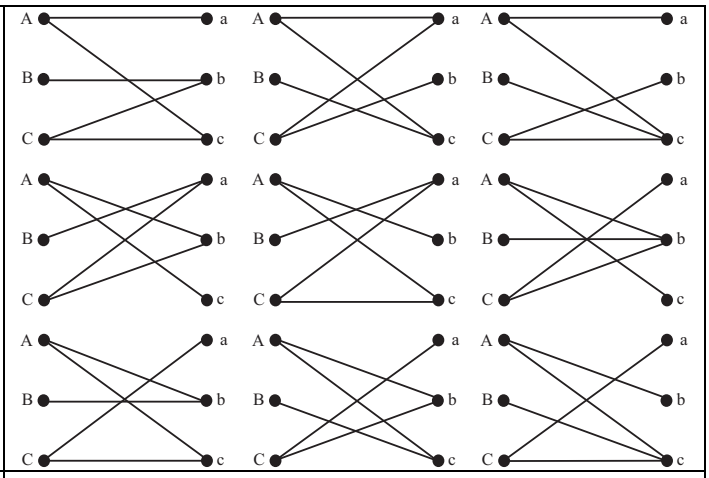
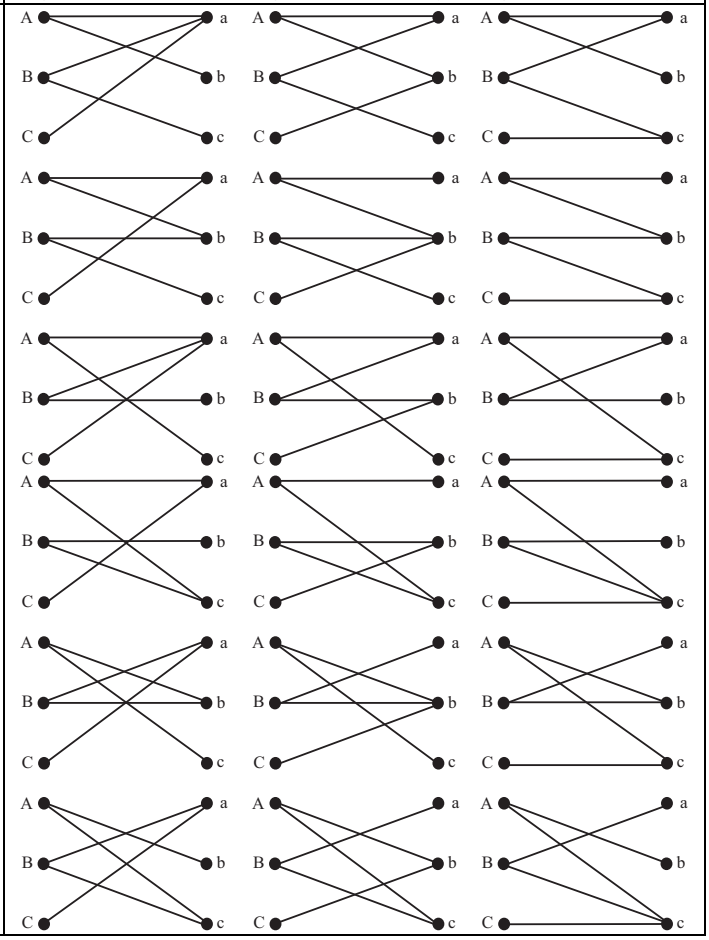
BRANCH CONNECTIONS

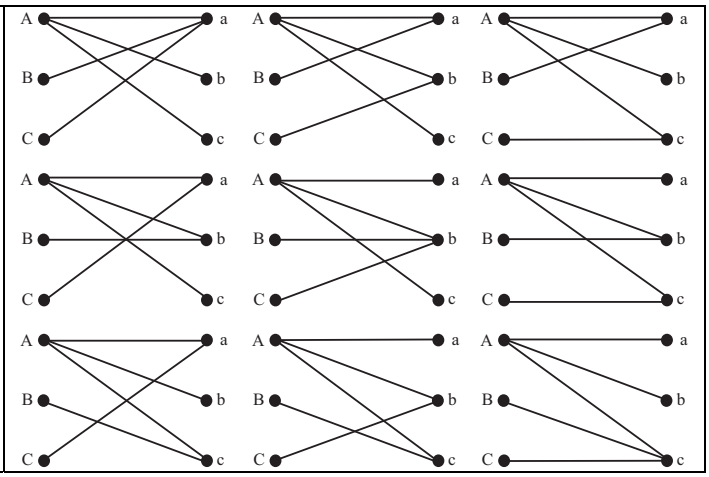
The following table lists all 81 valid branch connections that satisfy the constraints described in Section 2.1.2. The left-most columns show the numbers of possible branches that can be connected to each of the input phases. The sum of connected branches is always equal to five. The right-most column shows graphical configurations of all five connected branches.

Table A.1: 81 valid branch connections for a multilevel matrix converter

Num of branch connected to			Branch Connections
Phase A	Phase B	Phase C	
1	1	3	
1	2	2	

1	2	2	
1	3	1	
2	1	2	

			
2	2	1	

3	3	1	

APPENDIX B

BRANCH CONNECTIONS

The following tables list all valid switching device combinations of the multilevel matrix converter with the basic configuration. The switching device combinations are sorted by their corresponding space vectors at the input and output sides; each combination of the input and output vectors is grouped into a table. Each entry within a table constitutes a valid switching device combination. The corresponding switch cell states are listed in the nine columns on the left side of the tables. The states of each switch cell are denoted by 2-bit data, which can represent all four states. The 2-bit data and their corresponding switch cell states are defined as following:

"00" denotes an open-circuited state

"01" denotes a state having capacitor voltage across the switch cell terminals, with positive polarity connected to an input phase

"10" denotes a state having capacitor voltage across the switch cell terminals, with positive polarity connected to an output phase

"11" denotes a short-circuited state

The nine columns on the right side of the tables list the corresponding currents flowing through the respective capacitors of the switch cells. These currents are expressed in terms of the input- and output-phase currents. The input currents are assumed to flow into the converter, while the output currents are assumed to flow out of the converter.

In each table, the entries are further sorted by the number of capacitors that experience nonzero currents. The single-capacitor switching combinations are listed first in each table. The less-desirable multiple-capacitor combinations are listed later.

Table B.1: Switching device combinations for (V_{AB},V_{BC},V_{CA}) = (0,0,0) and (V_{ab},V_{bc},V_{ca}) = (V_{cap},0,$-V_{cap}$).

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
employ single capacitor																	
10	11	11	00	11	00	00	11	00	-Ia	0	0	0	0	0	0	0	0
10	11	11	00	11	00	00	00	11	-Ia	0	0	0	0	0	0	0	0
10	11	11	00	00	11	00	11	00	-Ia	0	0	0	0	0	0	0	0
10	11	11	00	00	11	00	00	11	-Ia	0	0	0	0	0	0	0	0
10	11	00	00	11	00	00	11	11	-Ia	0	0	0	0	0	0	0	0
10	00	11	00	11	00	00	11	11	-Ia	0	0	0	0	0	0	0	0
10	11	00	00	00	11	00	11	11	-Ia	0	0	0	0	0	0	0	0
10	00	11	00	00	11	00	11	11	-Ia	0	0	0	0	0	0	0	0
10	11	00	00	11	11	00	11	00	-Ia	0	0	0	0	0	0	0	0
10	00	11	00	11	11	00	11	00	-Ia	0	0	0	0	0	0	0	0
10	11	00	00	11	11	00	00	11	-Ia	0	0	0	0	0	0	0	0
10	00	11	00	11	11	00	00	11	-Ia	0	0	0	0	0	0	0	0
00	11	00	10	11	00	00	11	11	0	0	0	-Ia	0	0	0	0	0
00	11	00	10	00	11	00	11	11	0	0	0	-Ia	0	0	0	0	0
00	00	11	10	11	00	00	11	11	0	0	0	-Ia	0	0	0	0	0
00	00	11	10	00	11	00	11	11	0	0	0	-Ia	0	0	0	0	0
00	11	00	10	11	11	00	11	00	0	0	0	-Ia	0	0	0	0	0
00	00	11	10	11	11	00	11	00	0	0	0	-Ia	0	0	0	0	0
00	11	00	10	11	11	00	00	11	0	0	0	-Ia	0	0	0	0	0
00	00	11	10	11	11	00	00	11	0	0	0	-Ia	0	0	0	0	0
00	11	11	10	11	00	00	11	00	0	0	0	-Ia	0	0	0	0	0
00	11	11	10	00	11	00	11	00	0	0	0	-Ia	0	0	0	0	0
00	11	11	10	11	00	00	00	11	0	0	0	-Ia	0	0	0	0	0
00	11	11	10	00	11	00	00	11	0	0	0	-Ia	0	0	0	0	0
00	11	00	00	11	00	10	11	11	0	0	0	0	0	0	-Ia	0	0
00	11	00	00	00	11	10	11	11	0	0	0	0	0	0	-Ia	0	0
00	00	11	00	11	00	10	11	11	0	0	0	0	0	0	-Ia	0	0
00	00	11	00	00	11	10	11	11	0	0	0	0	0	0	-Ia	0	0
00	11	00	00	11	11	10	11	00	0	0	0	0	0	0	-Ia	0	0
00	11	00	00	11	11	10	00	11	0	0	0	0	0	0	-Ia	0	0
00	00	11	00	11	11	10	11	00	0	0	0	0	0	0	-Ia	0	0
00	00	11	00	11	11	10	00	11	0	0	0	0	0	0	-Ia	0	0
00	11	11	00	11	00	10	11	00	0	0	0	0	0	0	-Ia	0	0
00	11	11	00	11	00	10	00	11	0	0	0	0	0	0	-Ia	0	0
00	11	11	00	00	11	10	11	00	0	0	0	0	0	0	-Ia	0	0
00	11	11	00	00	11	10	00	11	0	0	0	0	0	0	-Ia	0	0
employ two capacitors																	
10	00	00	10	11	00	00	11	11	-IA	0	0	IA-Ia	0	0	0	0	0
10	00	00	10	00	11	00	11	11	-IA	0	0	IA-Ia	0	0	0	0	0
10	11	11	10	00	00	00	11	00	IB-Ia	0	0	-IB	0	0	0	0	0
10	11	11	10	00	00	00	00	11	IB-Ia	0	0	-IB	0	0	0	0	0

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
10	11	00	10	00	00	00	11	11	IB-Ia	0	0	-IB	0	0	0	0	0
10	00	11	10	00	00	00	11	11	IB-Ia	0	0	-IB	0	0	0	0	0
10	00	00	10	11	11	00	11	00	-IA	0	0	IA-Ia	0	0	0	0	0
10	00	00	10	11	11	00	00	11	-IA	0	0	IA-Ia	0	0	0	0	0
10	11	00	10	00	11	00	11	00	IB+Ib	0	0	Ic-IB	0	0	0	0	0
10	00	11	10	11	00	00	11	00	Ic-IA	0	0	IA+Ib	0	0	0	0	0
10	11	00	10	00	11	00	00	11	Ib-IA	0	0	IA+Ic	0	0	0	0	0
10	00	11	10	11	00	00	00	11	IB+Ic	0	0	Ib-IB	0	0	0	0	0
10	00	00	00	11	00	10	11	11	-IA	0	0	0	0	0	IA-Ia	0	0
10	00	00	00	00	11	10	11	11	-IA	0	0	0	0	0	IA-Ia	0	0
10	00	00	00	11	11	10	11	00	-IA	0	0	0	0	0	IA-Ia	0	0
10	00	00	00	11	11	10	00	11	-IA	0	0	0	0	0	IA-Ia	0	0
10	11	11	00	11	00	10	00	00	IC-Ia	0	0	0	0	0	-IC	0	0
10	11	11	00	00	11	10	00	00	IC-Ia	0	0	0	0	0	-IC	0	0
10	00	11	00	11	00	10	11	00	Ic-IA	0	0	0	0	0	IA+Ib	0	0
10	11	00	00	11	00	10	00	11	IC+Ib	0	0	0	0	0	Ic-IC	0	0
10	00	11	00	00	11	10	11	00	IC+Ic	0	0	0	0	0	Ib-IC	0	0
10	11	00	00	00	11	10	00	11	Ib-IA	0	0	0	0	0	IA+Ic	0	0
10	11	00	00	11	11	10	00	00	IC-Ia	0	0	0	0	0	-IC	0	0
10	00	11	00	11	11	10	00	00	IC-Ia	0	0	0	0	0	-IC	0	0
11	01	01	11	00	00	11	00	00	0	Ib	Ic	0	0	0	0	0	0
11	01	00	11	00	01	11	00	00	0	Ib	0	0	0	Ic	0	0	0
11	01	00	11	00	01	00	00	01	0	Ib	0	0	0	Ic-IC	0	0	IC
11	01	00	11	00	00	11	00	01	0	Ib	0	0	0	0	0	0	Ic
11	00	01	11	01	00	11	00	00	0	0	Ic	0	Ib	0	0	0	0
11	00	01	11	00	00	11	01	00	0	0	Ic	0	0	0	0	Ib	0
00	11	00	10	00	00	10	11	11	0	0	0	-IB	0	0	IB-Ia	0	0
00	00	11	10	00	00	10	11	11	0	0	0	-IB	0	0	IB-Ia	0	0
00	11	00	10	11	00	10	00	11	0	0	0	IC+Ib	0	0	Ic-IC	0	0
00	11	00	10	00	11	10	11	00	0	0	0	Ic-IB	0	0	IB+Ib	0	0
00	00	11	10	11	00	10	00	11	0	0	0	Ib-IB	0	0	IB+Ic	0	0
00	00	11	10	00	11	10	11	00	0	0	0	IC+Ic	0	0	Ib-IC	0	0
00	11	11	10	00	00	10	11	00	0	0	0	-IB	0	0	IB-Ia	0	0
00	11	11	10	00	00	10	00	11	0	0	0	-IB	0	0	IB-Ia	0	0
00	11	00	10	11	11	10	00	00	0	0	0	IC-Ia	0	0	-IC	0	0
00	00	11	10	11	11	10	00	00	0	0	0	IC-Ia	0	0	-IC	0	0
00	11	11	10	11	00	10	00	00	0	0	0	IC-Ia	0	0	-IC	0	0
00	11	11	10	00	11	10	00	00	0	0	0	IC-Ia	0	0	-IC	0	0
11	00	00	11	01	00	11	00	01	0	0	0	0	Ib	0	0	0	Ic
11	00	00	11	01	01	11	00	00	0	0	0	0	Ib	Ic	0	0	0
11	00	00	11	00	01	11	01	00	0	0	0	0	0	Ic	0	Ib	0
11	00	00	11	00	00	11	01	01	0	0	0	0	0	0	0	Ib	Ic
employ three capacitors																	
10	00	00	10	00	00	10	11	11	-IA	0	0	-IB	0	0	-Ia-IC	0	0
10	00	00	10	11	00	10	00	11	-IA	0	0	Ib-IB	0	0	Ic-IC	0	0

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
10	00	00	10	00	11	10	11	00	-IA	0	0	Ic-IB	0	0	Ib-IC	0	0
10	11	11	10	00	00	10	00	00	-Ia-IA	0	0	-IB	0	0	-IC	0	0
10	00	11	10	00	00	10	11	00	Ic-IA	0	0	-IB	0	0	Ib-IC	0	0
10	11	00	10	00	00	10	00	11	Ib-IA	0	0	-IB	0	0	Ic-IC	0	0
10	00	00	10	11	11	10	00	00	-IA	0	0	-Ia-IB	0	0	-IC	0	0
10	11	00	10	00	11	10	00	00	Ib-IA	0	0	Ic-IB	0	0	-IC	0	0
10	00	11	10	11	00	10	00	00	Ic-IA	0	0	Ib-IB	0	0	-IC	0	0
11	01	01	00	01	00	11	00	00	0	Ib-IB	Ic	0	IB	0	0	0	0
00	01	01	11	01	00	11	00	00	0	IA-Ic	Ic	0	-Ia-IA	0	0	0	0
11	01	01	00	00	01	11	00	00	0	Ib	Ic-IB	0	0	IB	0	0	0
00	01	01	11	00	01	11	00	00	0	Ib	IA-Ib	0	0	-Ia-IA	0	0	0
11	01	01	11	00	00	00	01	00	0	Ib-IC	Ic	0	0	0	0	IC	0
00	01	01	11	00	00	11	01	00	0	IA-Ic	Ic	0	0	0	0	-Ia-IA	0
11	01	01	11	00	00	00	00	01	0	Ib	Ic-IC	0	0	0	0	0	IC
00	01	01	11	00	00	11	00	01	0	Ib	IA-Ib	0	0	0	0	0	-Ia-IA
00	01	00	11	01	01	11	00	00	0	IA	0	0	Ib-IA	Ic	0	0	0
11	01	00	00	01	01	11	00	00	0	-Ia-IB	0	0	IB-Ic	Ic	0	0	0
00	01	00	11	01	00	11	00	01	0	IA	0	0	Ib-IA	0	0	0	Ic
11	01	00	00	01	00	11	00	01	0	Ib-IB	0	0	IB	0	0	0	Ic
00	01	00	11	00	01	11	01	00	0	IA	0	0	0	Ic	0	Ib-IA	0
11	01	00	11	00	01	00	01	00	0	Ib-IC	0	0	0	Ic	0	IC	0
11	01	00	00	00	01	11	00	01	0	Ib	0	0	0	IB	0	0	Ic-IB
00	01	00	11	00	00	11	01	01	0	IA	0	0	0	0	0	Ib-IA	Ic
11	01	00	11	00	00	00	01	01	0	-Ia-IC	0	0	0	0	0	IC-Ic	Ic
00	00	01	11	01	01	11	00	00	0	0	IA	0	Ib	Ic-IA	0	0	0
11	00	01	00	01	01	11	00	00	0	0	-Ia-IB	0	Ib	IB-Ib	0	0	0
11	00	01	00	01	00	11	01	00	0	0	Ic	0	IB	0	0	Ib-IB	0
11	00	01	11	01	00	00	01	00	0	0	Ic	0	Ib-IC	0	0	IC	0
00	00	01	11	01	00	11	00	01	0	0	IA	0	Ib	0	0	0	Ic-IA
11	00	01	11	01	00	00	00	01	0	0	Ic-IC	0	Ib	0	0	0	IC
00	00	01	11	00	01	11	01	00	0	0	IA	0	0	Ic-IA	0	Ib	0
11	00	01	00	00	01	11	01	00	0	0	Ic-IB	0	0	IB	0	Ib	0
00	00	01	11	00	00	11	01	01	0	0	IA	0	0	0	0	Ib	Ic-IA
11	00	01	11	00	00	00	01	01	0	0	-Ia-IC	0	0	0	0	Ib	IC-Ib
11	00	00	00	01	01	11	01	00	0	0	0	0	IB-Ic	Ic	0	-Ia-IB	0
11	00	00	11	01	01	00	01	00	0	0	0	0	Ib-IC	Ic	0	IC	0
11	00	00	00	01	01	11	00	01	0	0	0	0	Ib	IB-Ib	0	0	-Ia-IB
11	00	00	11	01	01	00	00	01	0	0	0	0	Ib	Ic-IC	0	0	IC
11	00	00	00	01	00	11	01	01	0	0	0	0	IB	0	0	Ib-IB	Ic
11	00	00	11	01	00	00	01	01	0	0	0	0	-Ia-IC	0	0	IC-Ic	Ic
11	00	00	00	00	01	11	01	01	0	0	0	0	0	IB	0	Ib	Ic-IB
11	00	00	11	00	01	00	01	01	0	0	0	0	0	-Ia-IC	0	Ib	IC-Ib
employ four capacitors																	
11	01	01	00	01	00	00	01	00	0	IA+Ib	Ic	0	IB	0	0	IC	0
00	01	01	00	01	00	11	01	00	0	IA-Ic	Ic	0	IB	0	0	IC-Ia	0

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
00	01	01	11	01	00	00	01	00	0	IA-Ic	Ic	0	IB-Ia	0	0	IC	0
11	01	01	00	01	00	00	00	01	0	Ib-IB	Ic-IC	0	IB	0	0	0	IC
00	01	01	00	01	00	11	00	01	0	Ib-IB	-Ib-IC	0	IB	0	0	0	IC-Ia
00	01	01	11	01	00	00	00	01	0	-Ic-IB	Ic-IC	0	IB-Ia	0	0	0	IC
11	01	01	00	00	01	00	01	00	0	Ib-IC	Ic-IB	0	0	IB	0	IC	0
00	01	01	00	00	01	11	01	00	0	-Ic-IC	Ic-IB	0	0	IB	0	IC-Ia	0
00	01	01	11	00	01	00	01	00	0	Ib-IC	-Ib-IB	0	0	IB-Ia	0	IC	0
11	01	01	00	00	01	00	00	01	0	Ib	Ic+IA	0	0	IB	0	0	IC
00	01	01	00	00	01	11	00	01	0	Ib	IA-Ib	0	0	IB	0	0	IC-Ia
00	01	01	11	00	01	00	00	01	0	Ib	IA-Ib	0	0	IB-Ia	0	0	IC
00	01	00	00	01	01	11	01	00	0	IA	0	0	IB-Ic	Ic	0	IC-Ia	0
00	01	00	11	01	01	00	01	00	0	IA	0	0	Ib+IB	Ic	0	IC	0
11	01	00	00	01	01	00	01	00	0	IA-Ia	0	0	IB-Ic	Ic	0	IC	0
00	01	00	00	01	01	11	00	01	0	IA	0	0	Ib-IA	-Ib-IC	0	0	IC-Ia
00	01	00	11	01	01	00	00	01	0	IA	0	0	Ib-IA	Ic-IC	0	0	IC
11	01	00	00	01	01	00	00	01	0	IA-Ia	0	0	-Ic-IA	Ic-IC	0	0	IC
00	01	00	00	01	00	11	01	01	0	IA	0	0	IB	0	0	Ib+IC	Ic
00	01	00	11	01	00	00	01	01	0	IA	0	0	IB-Ia	0	0	IC-Ic	Ic
11	01	00	00	01	00	00	01	01	0	IA-Ia	0	0	IB	0	0	IC-Ic	Ic
00	01	00	00	00	01	11	01	01	0	IA	0	0	0	IB	0	Ib-IA	Ic-IB
00	01	00	11	00	01	00	01	01	0	IA	0	0	0	IB-Ia	0	Ib-IA	-Ib-IB
11	01	00	00	00	01	00	01	01	0	IA-Ia	0	0	0	IB	0	-Ic-IA	Ic-IB
00	00	01	00	01	01	11	01	00	0	0	IA	0	-Ic-IC	Ic-IA	0	IC-Ia	0
11	00	01	00	01	01	00	01	00	0	0	IA-Ia	0	Ib-IC	-Ib-IA	0	IC	0
00	00	01	00	01	01	11	00	01	0	0	IA	0	Ib	IB-Ib	0	0	IC-Ia
00	00	01	11	01	01	00	01	00	0	0	IA	0	Ib-IC	Ic-IA	0	0	IC
00	00	01	11	01	01	00	00	01	0	0	IA	0	Ib	Ic+IB	0	0	IC
11	00	01	00	01	01	00	00	01	0	0	IA-Ia	0	Ib	IB-Ib	0	0	IC
00	00	01	00	01	00	11	01	01	0	0	IA	0	IB	0	0	Ib-IB	Ic-IA
00	00	01	11	01	00	00	01	01	0	0	IA	0	IB-Ia	0	0	-Ic-IB	Ic-IA
11	00	01	00	01	00	00	01	01	0	0	IA-Ia	0	IB	0	0	Ib-IB	-Ib-IA
00	00	01	00	00	01	11	01	01	0	0	IA	0	0	IB	0	Ib	Ic+IC
00	00	01	11	00	01	00	01	01	0	0	IA	0	0	IB-Ia	0	Ib	IC-Ib
11	00	01	00	00	01	00	01	01	0	0	IA-Ia	0	0	IB	0	Ib	IC-Ib

Table B.2: Switching device combinations for (V_{AB},V_{BC},V_{CA}) = (0,0,0) and (V_{ab},V_{bc},V_{ca}) = (0,V_{cap},$-V_{cap}$).

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
employ single capacitor																	
11	11	01	11	00	00	11	00	00	0	0	Ic	0	0	0	0	0	0
11	11	01	11	00	00	00	11	00	0	0	Ic	0	0	0	0	0	0
11	11	01	00	11	00	11	00	00	0	0	Ic	0	0	0	0	0	0
11	11	01	00	11	00	00	11	00	0	0	Ic	0	0	0	0	0	0
11	00	01	11	00	00	11	11	00	0	0	Ic	0	0	0	0	0	0
00	11	01	11	00	00	11	11	00	0	0	Ic	0	0	0	0	0	0
11	00	01	00	11	00	11	11	00	0	0	Ic	0	0	0	0	0	0
00	11	01	00	11	00	11	11	00	0	0	Ic	0	0	0	0	0	0
11	00	01	11	11	00	11	00	00	0	0	Ic	0	0	0	0	0	0
00	11	01	11	11	00	11	00	00	0	0	Ic	0	0	0	0	0	0
11	00	01	11	11	00	00	11	00	0	0	Ic	0	0	0	0	0	0
00	11	01	11	11	00	00	11	00	0	0	Ic	0	0	0	0	0	0
11	00	00	11	00	01	11	11	00	0	0	0	0	0	Ic	0	0	0
11	00	00	00	11	01	11	11	00	0	0	0	0	0	Ic	0	0	0
00	11	00	11	00	01	11	11	00	0	0	0	0	0	Ic	0	0	0
00	11	00	00	11	01	11	11	00	0	0	0	0	0	Ic	0	0	0
11	00	00	11	11	01	11	00	00	0	0	0	0	0	Ic	0	0	0
00	11	00	11	11	01	11	00	00	0	0	0	0	0	Ic	0	0	0
11	00	00	11	11	01	00	11	00	0	0	0	0	0	Ic	0	0	0
00	11	00	11	11	01	00	11	00	0	0	0	0	0	Ic	0	0	0
11	11	00	11	00	01	11	00	00	0	0	0	0	0	Ic	0	0	0
11	11	00	00	11	01	11	00	00	0	0	0	0	0	Ic	0	0	0
11	11	00	11	00	01	00	11	00	0	0	0	0	0	Ic	0	0	0
11	11	00	00	11	01	00	11	00	0	0	0	0	0	Ic	0	0	0
11	00	00	11	00	00	11	11	01	0	0	0	0	0	0	0	0	Ic
11	00	00	00	11	00	11	11	01	0	0	0	0	0	0	0	0	Ic
00	11	00	11	00	00	11	11	01	0	0	0	0	0	0	0	0	Ic
00	11	00	00	11	00	11	11	01	0	0	0	0	0	0	0	0	Ic
11	00	00	11	11	00	11	00	01	0	0	0	0	0	0	0	0	Ic
11	00	00	11	11	00	00	11	01	0	0	0	0	0	0	0	0	Ic
00	11	00	11	11	00	11	00	01	0	0	0	0	0	0	0	0	Ic
00	11	00	11	11	00	00	11	01	0	0	0	0	0	0	0	0	Ic
11	11	00	11	00	00	11	00	01	0	0	0	0	0	0	0	0	Ic
11	11	00	11	00	00	00	11	01	0	0	0	0	0	0	0	0	Ic
11	11	00	00	11	00	11	00	01	0	0	0	0	0	0	0	0	Ic
11	11	00	00	11	00	00	11	01	0	0	0	0	0	0	0	0	Ic
employ two capacitors																	
10	10	11	00	00	11	00	00	11	-Ia	-Ib	0	0	0	0	0	0	0
10	00	11	00	10	11	00	00	11	-Ia	0	0	0	-Ib	0	0	0	0
10	00	11	00	00	11	00	10	11	-Ia	0	0	0	0	0	0	-Ib	0
00	10	11	10	00	11	00	00	11	0	-Ib	0	-Ia	0	0	0	0	0

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
00	10	11	00	00	11	10	00	11	0	-Ib	0	0	0	0	-Ia	0	0
00	00	01	11	00	01	11	11	00	0	0	IA	0	0	Ic-IA	0	0	0
00	00	01	00	11	01	11	11	00	0	0	IA	0	0	Ic-IA	0	0	0
11	11	01	00	00	01	11	00	00	0	0	Ic-IB	0	0	IB	0	0	0
11	11	01	00	00	01	00	11	00	0	0	Ic-IB	0	0	IB	0	0	0
11	00	01	00	00	01	11	11	00	0	0	Ic-IB	0	0	IB	0	0	0
00	11	01	00	00	01	11	11	00	0	0	Ic-IB	0	0	IB	0	0	0
00	00	01	11	11	01	11	00	00	0	0	IA	0	0	Ic-IA	0	0	0
00	00	01	11	11	01	00	11	00	0	0	IA	0	0	Ic-IA	0	0	0
11	00	01	00	11	01	11	00	00	0	0	-Ia-IB	0	0	IB-Ib	0	0	0
00	11	01	11	00	01	11	00	00	0	0	IA-Ib	0	0	-Ia-IA	0	0	0
11	00	01	00	11	01	00	11	00	0	0	IA-Ia	0	0	-Ib-IA	0	0	0
00	11	01	11	00	01	00	11	00	0	0	-Ib-IB	0	0	IB-Ia	0	0	0
00	00	01	11	00	00	11	11	01	0	0	IA	0	0	0	0	0	Ic-IA
00	00	01	00	11	00	11	11	01	0	0	IA	0	0	0	0	0	Ic-IA
00	00	01	11	11	00	11	00	01	0	0	IA	0	0	0	0	0	Ic-IA
00	00	01	11	11	00	00	11	01	0	0	IA	0	0	0	0	0	Ic-IA
11	11	01	11	00	00	00	00	01	0	0	Ic-IC	0	0	0	0	0	IC
11	11	01	00	11	00	00	00	01	0	0	Ic-IC	0	0	0	0	0	IC
00	11	01	11	00	00	11	00	01	0	0	IA-Ib	0	0	0	0	0	-Ia-IA
11	00	01	11	00	00	00	11	01	0	0	-Ia-IC	0	0	0	0	0	IC-Ib
00	11	01	00	11	00	11	00	01	0	0	-Ib-IC	0	0	0	0	0	IC-Ia
11	00	01	00	11	00	00	11	01	0	0	IA-Ia	0	0	0	0	0	-Ib-IA
11	00	01	11	11	00	00	00	01	0	0	Ic-IC	0	0	0	0	0	IC
00	11	01	11	11	00	00	00	01	0	0	Ic-IC	0	0	0	0	0	IC
00	00	11	10	10	11	00	00	11	0	0	0	-Ia	-Ib	0	0	0	0
00	00	11	10	00	11	00	10	11	0	0	0	-Ia	0	0	0	-Ib	0
00	00	11	00	10	11	10	00	11	0	0	0	0	-Ib	0	-Ia	0	0
11	00	00	00	00	01	11	11	01	0	0	0	0	0	IB	0	0	Ic-IB
00	11	00	00	00	01	11	11	01	0	0	0	0	0	IB	0	0	Ic-IB
11	00	00	11	00	01	00	11	01	0	0	0	0	0	-Ia-IC	0	0	IC-Ib
11	00	00	00	11	01	11	00	01	0	0	0	0	0	IB-Ib	0	0	-Ia-IB
00	11	00	11	00	01	00	11	01	0	0	0	0	0	IB-Ia	0	0	-Ib-IB
00	11	00	00	11	01	11	00	01	0	0	0	0	0	-Ib-IC	0	0	IC-Ia
11	11	00	00	00	01	11	00	01	0	0	0	0	0	IB	0	0	Ic-IB
11	11	00	00	00	01	00	11	01	0	0	0	0	0	IB	0	0	Ic-IB
11	00	00	11	11	01	00	00	01	0	0	0	0	0	Ic-IC	0	0	IC
00	11	00	11	11	01	00	00	01	0	0	0	0	0	Ic-IC	0	0	IC
11	11	00	11	00	01	00	00	01	0	0	0	0	0	Ic-IC	0	0	IC
11	11	00	00	11	01	00	00	01	0	0	0	0	0	Ic-IC	0	0	IC
00	00	11	00	00	11	10	10	11	0	0	0	0	0	0	-Ia	-Ib	0
employ three capacitors																	
10	10	11	10	00	00	00	00	11	IB-Ia	-Ib	0	-IB	0	0	0	0	0
10	10	00	10	00	11	00	00	11	Ib-IA	-Ib	0	Ic+IA	0	0	0	0	0
10	10	11	00	10	00	00	00	11	-Ia	IB-Ib	0	0	-IB	0	0	0	0

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
10	10	00	00	10	11	00	00	11	-Ia	Ia-IA	0	0	Ic+IA	0	0	0	0
10	10	11	00	00	11	10	00	00	IC-Ia	-Ib	0	0	0	0	-IC	0	0
10	10	00	00	00	11	10	00	11	Ib-IA	-Ib	0	0	0	0	Ic+IA	0	0
10	10	11	00	00	11	00	10	00	-Ia	IC-Ib	0	0	0	0	0	-IC	0
10	10	00	00	00	11	00	10	11	-Ia	Ia-IA	0	0	0	0	0	Ic+IA	0
10	00	00	10	10	11	00	00	11	-IA	0	0	IA-Ia	-Ib	0	0	0	0
10	00	11	10	10	00	00	00	11	Ic+IB	0	0	Ib-IB	-Ib	0	0	0	0
10	00	00	10	00	11	00	10	11	-IA	0	0	IA-Ia	0	0	0	-Ib	0
10	00	11	10	00	00	00	10	11	IB-Ia	0	0	-IB	0	0	0	-Ib	0
10	00	00	00	10	11	10	00	11	-IA	0	0	0	-Ib	0	IA-Ia	0	0
10	00	11	00	10	11	10	00	00	IC-Ia	0	0	0	-Ib	0	-IC	0	0
10	00	11	00	10	00	00	10	11	-Ia	0	0	0	-IB	0	0	IB-Ib	0
10	00	11	00	10	11	00	10	00	-Ia	0	0	0	IC-Ib	0	0	-IC	0
10	00	00	00	00	11	10	10	11	-IA	0	0	0	0	0	IA-Ia	-Ib	0
10	00	11	00	00	11	10	10	00	Ic+IC	0	0	0	0	0	Ib-IC	-Ib	0
00	10	00	10	10	11	00	00	11	0	-IA	0	-Ia	IA-Ib	0	0	0	0
00	10	11	10	10	00	00	00	11	0	Ic+IB	0	-Ia	Ia-IB	0	0	0	0
00	10	11	10	00	00	10	00	11	0	-Ib	0	-IB	0	0	IB-Ia	0	0
00	10	11	10	00	11	10	00	00	0	-Ib	0	IC-Ia	0	0	-IC	0	0
00	10	00	10	00	11	00	10	11	0	-IA	0	-Ia	0	0	0	IA-Ib	0
00	10	11	10	00	11	00	10	00	0	IC-Ib	0	-Ia	0	0	0	-IC	0
00	10	00	00	10	11	10	00	11	0	-IA	0	0	IA-Ib	0	-Ia	0	0
00	10	11	00	10	00	10	00	11	0	IB-Ib	0	0	-IB	0	-Ia	0	0
00	10	00	00	00	11	10	10	11	0	-IA	0	0	0	0	-Ia	IA-Ib	0
00	10	11	00	00	11	10	10	00	0	Ic+IC	0	0	0	0	-Ia	Ia-IC	0
00	00	01	00	00	01	11	11	01	0	0	IA	0	0	IB	0	0	Ic+IC
00	00	01	11	00	01	00	11	01	0	0	IA	0	0	IB-Ia	0	0	IC-Ib
00	00	01	00	11	01	11	00	01	0	0	IA	0	0	IB-Ib	0	0	IC-Ia
11	11	01	00	00	01	00	00	01	0	0	Ic+IA	0	0	IB	0	0	IC
00	11	01	00	00	01	11	00	01	0	0	IA-Ib	0	0	IB	0	0	IC-Ia
11	00	01	00	00	01	00	11	01	0	0	IA-Ia	0	0	IB	0	0	IC-Ib
00	00	01	11	11	01	00	00	01	0	0	IA	0	0	Ic+IB	0	0	IC
11	00	01	00	11	01	00	00	01	0	0	IA-Ia	0	0	IB-Ib	0	0	IC
00	11	01	11	00	01	00	00	01	0	0	IA-Ib	0	0	IB-Ia	0	0	IC
00	00	11	10	10	00	10	00	11	0	0	0	Ib-IB	-Ib	0	Ic+IB	0	0
00	00	11	10	10	11	10	00	00	0	0	0	IC-Ia	-Ib	0	-IC	0	0
00	00	11	10	10	00	00	10	11	0	0	0	-Ia	Ia-IB	0	0	Ic+IB	0
00	00	11	10	10	11	00	10	00	0	0	0	-Ia	IC-Ib	0	0	-IC	0
00	00	11	10	00	00	10	10	11	0	0	0	-IB	0	0	IB-Ia	-Ib	0
00	00	11	10	00	11	10	10	00	0	0	0	Ic+IC	0	0	Ib-IC	-Ib	0
00	00	11	00	10	00	10	10	11	0	0	0	0	-IB	0	-Ia	IB-Ib	0
00	00	11	00	10	11	10	10	00	0	0	0	0	Ic+IC	0	-Ia	Ia-IC	0
employ four capacitors																	
10	10	11	10	00	00	10	00	00	-Ia-IA	-Ib	0	-IB	0	0	-IC	0	0
10	10	11	10	00	00	00	10	00	IB-Ia	IC-Ib	0	-IB	0	0	-IC	0	0

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
10	10	00	10	00	00	10	00	11	Ib-IA	-Ib	0	-IB	0	0	Ic-IC	0	0
10	10	00	10	00	11	10	00	00	Ib-IA	-Ib	0	Ic-IB	0	0	-IC	0	0
10	10	00	10	00	00	00	10	11	IB-Ia	Ia+IC	0	-IB	0	0	0	Ic-IC	0
10	10	00	10	00	11	00	10	00	Ib+IB	IC-Ib	0	Ic-IB	0	0	0	-IC	0
10	10	11	00	10	00	10	00	00	IC-Ia	IB-Ib	0	0	-IB	0	-IC	0	0
10	10	00	00	10	00	10	00	11	Ib+IC	IB-Ib	0	0	-IB	0	Ic-IC	0	0
10	10	00	00	10	11	10	00	00	IC-Ia	Ia+IB	0	0	Ic-IB	0	-IC	0	0
10	10	11	00	10	00	00	10	00	-Ia	-Ib-IA	0	0	-IB	0	0	-IC	0
10	10	00	00	10	00	00	10	11	-Ia	Ia-IA	0	0	-IB	0	0	Ic-IC	0
10	10	00	00	10	11	00	10	00	-Ia	Ia-IA	0	0	Ic-IB	0	0	-IC	0
10	00	00	10	10	00	10	00	11	-IA	0	0	Ib-IB	-Ib	0	Ic-IC	0	0
10	00	00	10	10	11	10	00	00	-IA	0	0	-IB-Ia	-Ib	0	-IC	0	0
10	00	11	10	10	00	10	00	00	Ic-IA	0	0	Ib-IB	-Ib	0	-IC	0	0
10	00	00	10	10	00	00	10	11	-IA	0	0	IA-Ia	Ia+IC	0	0	Ic-IC	0
10	00	00	10	10	11	00	10	00	-IA	0	0	IA-Ia	IC-Ib	0	0	-IC	0
10	00	11	10	10	00	00	10	00	Ic-IA	0	0	IA+Ib	IC-Ib	0	0	-IC	0
10	00	00	10	00	00	10	10	11	-IA	0	0	-IB	0	0	-Ia-IC	-Ib	0
10	00	00	10	00	11	10	10	00	-IA	0	0	Ic-IB	0	0	Ib-IC	-Ib	0
10	00	11	10	00	00	10	10	00	Ic-IA	0	0	-IB	0	0	Ib-IC	-Ib	0
10	00	00	00	10	00	10	10	11	-IA	0	0	0	-IB	0	IA-Ia	IB-Ib	0
10	00	00	00	10	11	10	10	00	-IA	0	0	0	Ic-IB	0	IA-Ia	Ia+IB	0
10	00	11	00	10	00	10	10	00	Ic-IA	0	0	0	-IB	0	Ib+IA	IB-Ib	0
00	10	00	10	10	00	10	00	11	0	-IA	0	Ib+IC	IA-Ib	0	Ic-IC	0	0
00	10	00	10	10	11	10	00	00	0	-IA	0	IC-Ia	IA-Ib	0	-IC	0	0
00	10	11	10	10	00	10	00	00	0	Ic-IA	0	IC-Ia	Ia+IA	0	-IC	0	0
00	10	00	10	10	00	00	10	11	0	-IA	0	-Ia	Ia-IB	0	0	Ic-IC	0
00	10	00	10	10	11	00	10	00	0	-IA	0	-Ia	-Ib-IB	0	0	-IC	0
00	10	11	10	10	00	00	10	00	0	Ic-IA	0	-Ia	Ia-IB	0	0	-IC	0
00	10	00	10	00	00	10	10	11	0	-IA	0	-IB	0	0	IB-Ia	IA-Ib	0
00	10	00	10	00	11	10	10	00	0	-IA	0	Ic-IB	0	0	Ib+IB	IA-Ib	0
00	10	11	10	00	00	10	10	00	0	Ic-IA	0	-IB	0	0	IB-Ia	Ia+IA	0
00	10	00	00	10	00	10	10	11	0	-IA	0	0	-IB	0	-Ia	-Ib-IC	0
00	10	00	00	10	11	10	10	00	0	-IA	0	0	Ic-IB	0	-Ia	Ia-IC	0
00	10	11	00	10	00	10	10	00	0	Ic-IA	0	0	-IB	0	-Ia	Ia-IC	0

Table B.3: Switching device combinations for (V_{AB},V_{BC},V_{CA}) = (0,0,0) and (V_{ab},V_{bc},V_{ca}) = ($-V_{cap}$,V_{cap},0).

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
employ single capacitor																	
11	10	11	11	00	00	11	00	00	0	-Ib	0	0	0	0	0	0	0
11	10	11	11	00	00	00	00	11	0	-Ib	0	0	0	0	0	0	0
11	10	11	00	00	11	11	00	00	0	-Ib	0	0	0	0	0	0	0
11	10	11	00	00	11	00	00	11	0	-Ib	0	0	0	0	0	0	0
11	10	00	11	00	00	11	00	11	0	-Ib	0	0	0	0	0	0	0
00	10	11	11	00	00	11	00	11	0	-Ib	0	0	0	0	0	0	0
11	10	00	00	00	11	11	00	11	0	-Ib	0	0	0	0	0	0	0
00	10	11	00	00	11	11	00	11	0	-Ib	0	0	0	0	0	0	0
11	10	00	11	00	11	11	00	00	0	-Ib	0	0	0	0	0	0	0
00	10	11	11	00	11	11	00	00	0	-Ib	0	0	0	0	0	0	0
11	10	00	11	00	11	00	00	11	0	-Ib	0	0	0	0	0	0	0
00	10	11	11	00	11	00	00	11	0	-Ib	0	0	0	0	0	0	0
11	00	00	11	10	00	11	00	11	0	0	0	0	-Ib	0	0	0	0
11	00	00	00	10	11	11	00	11	0	0	0	0	-Ib	0	0	0	0
00	00	11	11	10	00	11	00	11	0	0	0	0	-Ib	0	0	0	0
00	00	11	00	10	11	11	00	11	0	0	0	0	-Ib	0	0	0	0
11	00	00	11	10	11	11	00	00	0	0	0	0	-Ib	0	0	0	0
00	00	11	11	10	11	11	00	00	0	0	0	0	-Ib	0	0	0	0
11	00	00	11	10	11	00	00	11	0	0	0	0	-Ib	0	0	0	0
00	00	11	11	10	11	00	00	11	0	0	0	0	-Ib	0	0	0	0
11	00	11	11	10	00	11	00	00	0	0	0	0	-Ib	0	0	0	0
11	00	11	00	10	11	11	00	00	0	0	0	0	-Ib	0	0	0	0
11	00	11	11	10	00	00	00	11	0	0	0	0	-Ib	0	0	0	0
11	00	11	00	10	11	00	00	11	0	0	0	0	-Ib	0	0	0	0
11	00	00	11	00	00	11	10	11	0	0	0	0	0	0	0	-Ib	0
11	00	00	00	00	11	11	10	11	0	0	0	0	0	0	0	-Ib	0
00	00	11	11	00	00	11	10	11	0	0	0	0	0	0	0	-Ib	0
00	00	11	00	00	11	11	10	11	0	0	0	0	0	0	0	-Ib	0
11	00	00	11	00	11	11	10	00	0	0	0	0	0	0	0	-Ib	0
11	00	00	11	00	11	00	10	11	0	0	0	0	0	0	0	-Ib	0
00	00	11	11	00	11	11	10	00	0	0	0	0	0	0	0	-Ib	0
00	00	11	11	00	11	00	10	11	0	0	0	0	0	0	0	-Ib	0
11	00	11	11	00	00	11	10	00	0	0	0	0	0	0	0	-Ib	0
11	00	11	11	00	00	00	10	11	0	0	0	0	0	0	0	-Ib	0
11	00	11	00	00	11	11	10	00	0	0	0	0	0	0	0	-Ib	0
11	00	11	00	00	11	00	10	11	0	0	0	0	0	0	0	-Ib	0
employ two capacitors																	
01	11	01	00	11	00	00	11	00	Ia	0	Ic	0	0	0	0	0	0
01	11	00	00	11	01	00	11	00	Ia	0	0	0	0	Ic	0	0	0
01	11	00	00	11	00	00	11	01	Ia	0	0	0	0	0	0	0	Ic
00	10	00	11	10	00	11	00	11	0	-IA	0	0	IA-Ib	0	0	0	0

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
00	10	00	00	10	11	11	00	11	0	-IA	0	0	IA-Ib	0	0	0	0
11	10	11	00	10	00	11	00	00	0	IB-Ib	0	0	-IB	0	0	0	0
11	10	11	00	10	00	00	00	11	0	IB-Ib	0	0	-IB	0	0	0	0
11	10	00	00	10	00	11	00	11	0	IB-Ib	0	0	-IB	0	0	0	0
00	10	11	00	10	00	11	00	11	0	IB-Ib	0	0	-IB	0	0	0	0
00	10	00	11	10	11	11	00	00	0	-IA	0	0	IA-Ib	0	0	0	0
00	10	00	11	10	11	00	00	11	0	-IA	0	0	IA-Ib	0	0	0	0
11	10	00	00	10	11	11	00	00	0	IB+Ia	0	0	Ic-IB	0	0	0	0
00	10	11	11	10	00	11	00	00	0	Ic-IA	0	0	Ia+IA	0	0	0	0
11	10	00	00	10	11	00	00	11	0	Ia-A	0	0	Ic+IA	0	0	0	0
00	10	11	11	10	00	00	00	11	0	Ic+IB	0	0	Ia-IB	0	0	0	0
00	10	00	11	00	00	11	10	11	0	-IA	0	0	0	0	0	IA-Ib	0
00	10	00	00	00	11	11	10	11	0	-IA	0	0	0	0	0	IA-Ib	0
00	10	00	11	00	11	11	10	00	0	-IA	0	0	0	0	0	IA-Ib	0
00	10	00	11	00	11	00	10	11	0	-IA	0	0	0	0	0	IA-Ib	0
11	10	11	11	00	00	00	10	00	0	IC-Ib	0	0	0	0	0	-IC	0
11	10	11	00	00	11	00	10	00	0	IC-Ib	0	0	0	0	0	-IC	0
00	10	11	11	00	00	11	10	00	0	Ic-IA	0	0	0	0	0	Ia+IA	0
11	10	00	11	00	00	00	10	11	0	IC+Ia	0	0	0	0	0	Ic-IC	0
00	10	11	00	00	11	11	10	00	0	Ic+IC	0	0	0	0	0	Ia-IC	0
11	10	00	00	00	11	00	10	11	0	Ia-IA	0	0	0	0	0	Ic+IA	0
11	10	00	11	00	11	00	10	00	0	IC-Ib	0	0	0	0	0	-IC	0
00	10	11	11	00	11	00	10	00	0	IC-Ib	0	0	0	0	0	-IC	0
00	11	01	01	11	00	00	11	00	0	0	Ic	Ia	0	0	0	0	0
00	11	01	00	11	00	01	11	00	0	0	Ic	0	0	0	Ia	0	0
00	11	00	01	11	01	00	11	00	0	0	0	Ia	0	Ic	0	0	0
00	11	00	01	11	00	00	11	01	0	0	0	Ia	0	0	0	0	Ic
11	00	00	00	10	00	11	10	11	0	0	0	0	-IB	0	0	IB-Ib	0
00	00	11	00	10	00	11	10	11	0	0	0	0	-IB	0	0	IB-Ib	0
11	00	00	11	10	00	00	10	11	0	0	0	0	IC+Ia	0	0	Ic-IC	0
11	00	00	00	10	11	11	10	00	0	0	0	0	Ic-IB	0	0	IB+Ia	0
00	00	11	11	10	00	00	10	11	0	0	0	0	Ia-IB	0	0	Ic+IB	0
00	00	11	00	10	11	11	10	00	0	0	0	0	Ic+IC	0	0	Ia-IC	0
11	00	11	00	10	00	11	10	00	0	0	0	0	-IB	0	0	IB-Ib	0
11	00	11	00	10	00	00	10	11	0	0	0	0	-IB	0	0	IB-Ib	0
11	00	00	11	10	11	00	10	00	0	0	0	0	IC-Ib	0	0	-IC	0
00	00	11	11	10	11	00	10	00	0	0	0	0	IC-Ib	0	0	-IC	0
11	00	11	11	10	00	00	10	00	0	0	0	0	IC-Ib	0	0	-IC	0
11	00	11	00	10	11	00	10	00	0	0	0	0	IC-Ib	0	0	-IC	0
00	11	00	00	11	01	01	11	00	0	0	0	0	0	Ic	Ia	0	0
00	11	00	00	11	00	01	11	01	0	0	0	0	0	0	Ia	0	Ic
employ three capacitors																	
01	11	01	01	00	00	00	11	00	Ia-IB	0	Ic	IB	0	0	0	0	0
01	00	01	01	11	00	00	11	00	IA-Ic	0	Ic	-Ib-IA	0	0	0	0	0
01	00	01	00	11	01	00	11	00	Ia	0	IA-Ia	0	0	-Ib-IA	0	0	0

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
01	11	01	00	00	01	00	11	00	Ia	0	Ic-IB	0	0	IB	0	0	0
01	11	01	00	11	00	01	00	00	Ia-IC	0	Ic	0	0	0	IC	0	0
01	00	01	00	11	00	01	11	00	IA-Ic	0	Ic	0	0	0	-Ib-IA	0	0
01	11	01	00	11	00	00	00	01	Ia	0	Ic-IC	0	0	0	0	0	IC
01	00	01	00	11	00	00	11	01	Ia	0	IA-Ia	0	0	0	0	0	-Ib-IA
01	00	00	01	11	01	00	11	00	IA	0	0	Ia-IA	0	Ic	0	0	0
01	11	00	01	00	01	00	11	00	-Ib-IB	0	0	IB-Ic	0	Ic	0	0	0
01	00	00	01	11	00	00	11	01	IA	0	0	Ia-IA	0	0	0	0	Ic
01	11	00	01	00	00	00	11	01	Ia-IB	0	0	IB	0	0	0	0	Ic
01	00	00	00	11	01	01	11	00	IA	0	0	0	0	Ic	Ia-IA	0	0
01	11	00	00	11	01	01	00	00	Ia-IC	0	0	0	0	Ic	IC	0	0
01	11	00	00	00	01	00	11	01	Ia	0	0	0	0	IB	0	0	Ic-IB
01	11	00	00	11	01	00	00	01	Ia	0	0	0	0	Ic-IC	0	0	IC
01	00	00	00	11	00	01	11	01	IA	0	0	0	0	0	Ia-IA	0	Ic
01	11	00	00	11	00	01	00	01	-Ib-IC	0	0	0	0	0	IC-Ic	0	Ic
00	10	00	00	10	00	11	10	11	0	-IA	0	0	-IB	0	0	-Ib-IC	0
00	10	00	11	10	00	00	10	11	0	-IA	0	0	Ia-IB	0	0	Ic-IC	0
00	10	00	00	10	11	11	10	00	0	-IA	0	0	Ic-IB	0	0	Ia-IC	0
11	10	11	00	10	00	00	10	00	0	-Ib-IA	0	0	-IB	0	0	-IC	0
00	10	11	00	10	00	11	10	00	0	Ic-IA	0	0	-IB	0	0	Ia-IC	0
11	10	00	00	10	00	00	10	11	0	Ia-IA	0	0	-IB	0	0	Ic-IC	0
00	10	00	11	10	11	00	10	00	0	-IA	0	0	-Ib-IB	0	0	-IC	0
11	10	00	00	10	11	00	10	00	0	Ia-IA	0	0	Ic-IB	0	0	-IC	0
00	10	11	11	10	00	00	10	00	0	Ic-IA	0	0	Ia-IB	0	0	-IC	0
00	00	01	01	11	01	00	11	00	0	0	IA	Ia	0	Ic-IA	0	0	0
00	11	01	01	00	01	00	11	00	0	0	-Ib-IB	Ia	0	IB-Ia	0	0	0
00	11	01	01	00	00	01	11	00	0	0	Ic	IB	0	0	Ia-IB	0	0
00	11	01	01	11	00	01	00	00	0	0	Ic	Ia-IC	0	0	IC	0	0
00	00	01	01	11	00	00	11	01	0	0	IA	Ia	0	0	0	0	Ic-IA
00	11	01	01	11	00	00	00	01	0	0	Ic-IC	Ia	0	0	0	0	IC
00	00	01	00	11	01	01	11	00	0	0	IA	0	0	Ic-IA	Ia	0	0
00	11	01	00	00	01	01	11	00	0	0	Ic-IB	0	0	IB	Ia	0	0
00	00	01	00	11	00	01	11	01	0	0	IA	0	0	0	Ia	0	Ic-IA
00	11	01	00	11	00	01	00	01	0	0	-Ib-IC	0	0	0	Ia	0	IC-Ia
00	11	00	01	00	01	01	11	00	0	0	0	IB-Ic	0	Ic	-Ib-IB	0	0
00	11	00	01	11	01	01	00	00	0	0	0	Ia-IC	0	Ic	IC	0	0
00	11	00	01	00	01	00	11	01	0	0	0	Ia	0	IB-Ia	0	0	-Ib-IB
00	11	00	01	11	01	00	00	01	0	0	0	Ia	0	Ic-IC	0	0	IC
00	11	00	01	00	00	01	11	01	0	0	0	IB	0	0	Ia-IB	0	Ic
00	11	00	01	11	00	01	00	01	0	0	0	-Ib-IC	0	0	IC-Ic	0	Ic
00	11	00	00	00	01	01	11	01	0	0	0	0	0	IB	Ia	0	Ic-IB
00	11	00	00	11	01	01	00	01	0	0	0	0	0	-Ib-IC	Ia	0	IC-Ia
employ four capacitors																	
01	11	01	01	00	00	01	00	00	Ia+IA	0	Ic	IB	0	0	IC	0	0
01	00	01	01	00	00	01	11	00	IA-Ic	0	Ic	IB	0	0	IC-Ib	0	0

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
01	00	01	01	11	00	01	00	00	IA-Ic	0	Ic	IB-Ib	0	0	IC	0	0
01	11	01	01	00	00	00	00	01	Ia-IB	0	Ic-IC	IB	0	0	0	0	IC
01	00	01	01	00	00	00	11	01	Ia-IB	0	-Ia-IC	IB	0	0	0	0	IC-Ib
01	00	01	01	11	00	00	00	01	-Ic-IB	0	Ic-IC	IB-Ib	0	0	0	0	IC
01	11	01	00	00	01	01	00	00	Ia-IC	0	Ic-IB	0	0	IB	IC	0	0
01	00	01	00	00	01	01	11	00	-Ic-IC	0	Ic-IB	0	0	IB	IC-Ib	0	0
01	00	01	00	11	01	01	00	00	Ia-IC	0	-Ia-IB	0	0	IB-Ib	IC	0	0
01	00	01	00	00	01	00	11	01	Ia	0	IA-Ia	0	0	IB	0	0	IC-Ib
01	11	01	00	00	01	00	00	01	Ia	0	Ic+IA	0	0	IB	0	0	IC
01	00	01	00	11	01	00	00	01	Ia	0	IA-Ia	0	0	IB-Ib	0	0	IC
01	00	00	01	00	01	01	11	00	IA	0	0	IB-Ic	0	Ic	IC-Ib	0	0
01	00	00	01	11	01	01	00	00	IA	0	0	IB+Ia	0	Ic	IC	0	0
01	11	00	01	00	01	01	00	00	IA-Ib	0	0	IB-Ic	0	Ic	IC	0	0
01	00	00	01	00	01	00	11	01	IA	0	0	Ia-IA	0	-Ia-IC	0	0	IC-Ib
01	00	00	01	11	01	00	00	01	IA	0	0	Ia-IA	0	Ic-IC	0	0	IC
01	11	00	01	00	01	00	00	01	IA-Ib	0	0	-Ic-IA	0	Ic-IC	0	0	IC
01	00	00	01	00	00	01	11	01	IA	0	0	IB	0	0	IC+Ia	0	Ic
01	00	00	01	11	00	01	00	01	IA	0	0	IB-Ib	0	0	IC-Ic	0	Ic
01	11	00	01	00	00	01	00	01	IA-Ib	0	0	IB	0	0	IC-Ic	0	Ic
01	00	00	00	00	01	01	11	01	IA	0	0	0	0	IB	Ia-IA	0	Ic-IB
01	00	00	00	11	01	01	00	01	IA	0	0	0	0	IB-Ib	Ia-IA	0	-Ia-IB
01	11	00	00	00	01	01	00	01	IA-Ib	0	0	0	0	IB	-Ic-IA	0	Ic-IB
00	00	01	01	00	01	01	11	00	0	0	IA	-Ic-IC	0	Ic-IA	IC-Ib	0	0
00	00	01	01	11	01	01	00	00	0	0	IA	Ia-IC	0	Ic-IA	IC	0	0
00	11	01	01	00	01	01	00	00	0	0	IA-Ib	Ia-IC	0	-Ia-IA	IC	0	0
00	00	01	01	00	01	00	11	01	0	0	IA	Ia	0	IB-Ia	0	0	IC-Ib
00	00	01	01	11	01	00	00	01	0	0	IA	Ia	0	Ic+IB	0	0	IC
00	11	01	01	00	01	00	00	01	0	0	IA-Ib	Ia	0	IB-Ia	0	0	IC
00	00	01	01	00	00	01	11	01	0	0	IA	IB	0	0	Ia-IB	0	Ic-IA
00	00	01	01	11	00	01	00	01	0	0	IA	IB-Ib	0	0	-Ic-IB	0	Ic-IA
00	11	01	01	00	00	01	00	01	0	0	IA-Ib	IB	0	0	Ia-IB	0	-Ia-IA
00	00	01	00	00	01	01	11	01	0	0	IA	0	0	IB	Ia	0	Ic+IC
00	00	01	00	11	01	01	00	01	0	0	IA	0	0	IB-Ib	Ia	0	IC-Ia
00	11	01	00	00	01	01	00	01	0	0	IA-Ib	0	0	IB	Ia	0	IC-Ia

Table B.4: Switching device combinations for (V_{AB},V_{BC},V_{CA}) = (0,0,0) and (V_{ab},V_{bc},V_{ca}) = ($-V_{cap}$,0,V_{cap}).

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
employ single capacitor																	
01	11	11	00	11	00	00	11	00	Ia	0	0	0	0	0	0	0	0
01	11	11	00	11	00	00	00	11	Ia	0	0	0	0	0	0	0	0
01	11	11	00	00	11	00	11	00	Ia	0	0	0	0	0	0	0	0
01	11	11	00	00	11	00	00	11	Ia	0	0	0	0	0	0	0	0
01	11	00	00	11	00	00	11	11	Ia	0	0	0	0	0	0	0	0
01	00	11	00	11	00	00	11	11	Ia	0	0	0	0	0	0	0	0
01	11	00	00	00	11	00	11	11	Ia	0	0	0	0	0	0	0	0
01	00	11	00	00	11	00	11	11	Ia	0	0	0	0	0	0	0	0
01	11	00	00	11	11	00	11	00	Ia	0	0	0	0	0	0	0	0
01	00	11	00	11	11	00	11	00	Ia	0	0	0	0	0	0	0	0
01	11	00	00	11	11	00	00	11	Ia	0	0	0	0	0	0	0	0
01	00	11	00	11	11	00	00	11	Ia	0	0	0	0	0	0	0	0
00	11	00	01	11	00	00	11	11	0	0	0	Ia	0	0	0	0	0
00	11	00	01	00	11	00	11	11	0	0	0	Ia	0	0	0	0	0
00	00	11	01	11	00	00	11	11	0	0	0	Ia	0	0	0	0	0
00	00	11	01	00	11	00	11	11	0	0	0	Ia	0	0	0	0	0
00	11	00	01	11	11	00	11	00	0	0	0	Ia	0	0	0	0	0
00	00	11	01	11	11	00	11	00	0	0	0	Ia	0	0	0	0	0
00	11	00	01	11	11	00	00	11	0	0	0	Ia	0	0	0	0	0
00	00	11	01	11	11	00	00	11	0	0	0	Ia	0	0	0	0	0
00	11	11	01	11	00	00	11	00	0	0	0	Ia	0	0	0	0	0
00	11	11	01	00	11	00	11	00	0	0	0	Ia	0	0	0	0	0
00	11	11	01	11	00	00	00	11	0	0	0	Ia	0	0	0	0	0
00	11	11	01	00	11	00	00	11	0	0	0	Ia	0	0	0	0	0
00	11	00	00	11	00	01	11	11	0	0	0	0	0	0	Ia	0	0
00	11	00	00	00	11	01	11	11	0	0	0	0	0	0	Ia	0	0
00	00	11	00	11	00	01	11	11	0	0	0	0	0	0	Ia	0	0
00	00	11	00	00	11	01	11	11	0	0	0	0	0	0	Ia	0	0
00	11	00	00	11	11	01	11	00	0	0	0	0	0	0	Ia	0	0
00	11	00	00	11	11	01	00	11	0	0	0	0	0	0	Ia	0	0
00	00	11	00	11	11	01	11	00	0	0	0	0	0	0	Ia	0	0
00	00	11	00	11	11	01	00	11	0	0	0	0	0	0	Ia	0	0
00	11	11	00	11	00	01	11	00	0	0	0	0	0	0	Ia	0	0
00	11	11	00	11	00	01	00	11	0	0	0	0	0	0	Ia	0	0
00	11	11	00	00	11	01	11	00	0	0	0	0	0	0	Ia	0	0
00	11	11	00	00	11	01	00	11	0	0	0	0	0	0	Ia	0	0
employ two capacitors																	
01	00	00	01	11	00	00	11	11	IA	0	0	Ia-IA	0	0	0	0	0
01	00	00	01	00	11	00	11	11	IA	0	0	Ia-IA	0	0	0	0	0
01	11	11	01	00	00	00	11	00	Ia-IB	0	0	IB	0	0	0	0	0
01	11	11	01	00	00	00	00	11	Ia-IB	0	0	IB	0	0	0	0	0

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
01	11	00	01	00	00	00	11	11	Ia-IB	0	0	IB	0	0	0	0	0
01	00	11	01	00	00	00	11	11	Ia-IB	0	0	IB	0	0	0	0	0
01	00	00	01	11	11	00	11	00	IA	0	0	Ia-IA	0	0	0	0	0
01	00	00	01	11	11	00	00	11	IA	0	0	Ia-IA	0	0	0	0	0
01	11	00	01	00	11	00	11	00	-Ib-IB	0	0	IB-Ic	0	0	0	0	0
01	00	11	01	11	00	00	11	00	IA-Ic	0	0	-Ib-IA	0	0	0	0	0
01	11	00	01	00	11	00	00	11	IA-Ib	0	0	-Ic-IA	0	0	0	0	0
01	00	11	01	11	00	00	00	11	-Ic-IB	0	0	IB-Ib	0	0	0	0	0
01	00	00	00	11	00	01	11	11	IA	0	0	0	0	0	Ia-IA	0	0
01	00	00	00	00	11	01	11	11	IA	0	0	0	0	0	Ia-IA	0	0
01	00	00	00	11	11	01	11	00	IA	0	0	0	0	0	Ia-IA	0	0
01	00	00	00	11	11	01	00	11	IA	0	0	0	0	0	Ia-IA	0	0
01	11	11	00	11	00	01	00	00	Ia-IC	0	0	0	0	0	IC	0	0
01	11	11	00	00	11	01	00	00	Ia-IC	0	0	0	0	0	IC	0	0
01	00	11	00	11	00	01	11	00	IA-Ic	0	0	0	0	0	-Ib-IA	0	0
01	11	00	00	11	00	01	00	11	-Ib-IC	0	0	0	0	0	IC-Ic	0	0
01	00	11	00	00	11	01	11	00	-Ic-IC	0	0	0	0	0	IC-Ib	0	0
01	11	00	00	00	11	01	00	11	IA-Ib	0	0	0	0	0	-Ic-IA	0	0
01	11	00	00	11	11	01	00	00	Ia-IC	0	0	0	0	0	IC	0	0
01	00	11	00	11	11	01	00	00	Ia-IC	0	0	0	0	0	IC	0	0
11	10	10	11	00	00	11	00	00	0	-Ib	-Ic	0	0	0	0	0	0
11	10	00	11	00	10	11	00	00	0	-Ib	0	0	0	-Ic	0	0	0
11	10	00	11	00	00	11	00	10	0	-Ib	0	0	0	0	0	0	-Ic
11	00	10	11	10	00	11	00	00	0	0	-Ic	0	-Ib	0	0	0	0
11	00	10	11	00	00	11	10	00	0	0	-Ic	0	0	0	0	-Ib	0
00	11	00	01	00	00	01	11	11	0	0	0	IB	0	0	Ia-IB	0	0
00	00	11	01	00	00	01	11	11	0	0	0	IB	0	0	Ia-IB	0	0
00	11	00	01	11	00	01	00	11	0	0	0	-Ib-IC	0	0	IC-Ic	0	0
00	11	00	01	00	11	01	11	00	0	0	0	IB-Ic	0	0	-Ib-IB	0	0
00	00	11	01	11	00	01	00	11	0	0	0	IB-Ib	0	0	-Ic-IB	0	0
00	00	11	01	00	11	01	11	00	0	0	0	-Ic-IC	0	0	IC-Ib	0	0
00	11	11	01	00	00	01	11	00	0	0	0	IB	0	0	Ia-IB	0	0
00	11	11	01	00	00	01	00	11	0	0	0	IB	0	0	Ia-IB	0	0
00	11	00	01	11	11	01	00	00	0	0	0	Ia-IC	0	0	IC	0	0
00	00	11	01	11	11	01	00	00	0	0	0	Ia-IC	0	0	IC	0	0
00	11	11	01	11	00	01	00	00	0	0	0	Ia-IC	0	0	IC	0	0
00	11	11	01	00	11	01	00	00	0	0	0	Ia-IC	0	0	IC	0	0
11	00	00	11	10	10	11	00	00	0	0	0	0	-Ib	-Ic	0	0	0
11	00	00	11	10	00	11	00	10	0	0	0	0	-Ib	0	0	0	-Ic
11	00	00	11	00	10	11	10	00	0	0	0	0	0	-Ic	0	-Ib	0
11	00	00	11	00	00	11	10	10	0	0	0	0	0	0	0	-Ib	-Ic
employ three capacitors																	
01	00	00	01	00	00	01	11	11	IA	0	0	IB	0	0	IC+Ia	0	0
01	00	00	01	11	00	01	00	11	IA	0	0	IB-Ib	0	0	IC-Ic	0	0
01	00	00	01	00	11	01	11	00	IA	0	0	IB-Ic	0	0	IC-Ib	0	0

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
01	11	11	01	00	00	01	00	00	Ia+IA	0	0	IB	0	0	IC	0	0
01	00	11	01	00	00	01	11	00	IA-Ic	0	0	IB	0	0	IC-Ib	0	0
01	11	00	01	00	00	01	00	11	IA-Ib	0	0	IB	0	0	IC-Ic	0	0
01	00	00	01	11	11	01	00	00	IA	0	0	Ia+IB	0	0	IC	0	0
01	11	00	01	00	11	01	00	00	IA-Ib	0	0	IB-Ic	0	0	IC	0	0
01	00	11	01	11	00	01	00	00	IA-Ic	0	0	IB-Ib	0	0	IC	0	0
11	10	10	00	10	00	11	00	00	0	IB-Ib	-Ic	0	-IB	0	0	0	0
00	10	10	11	10	00	11	00	00	0	Ic-IA	-Ic	0	Ia+IA	0	0	0	0
11	10	10	00	00	10	11	00	00	0	-Ib	IB-Ic	0	0	-IB	0	0	0
00	10	10	11	00	10	11	00	00	0	-Ib	Ib-IA	0	0	Ia+IA	0	0	0
11	10	10	11	00	00	00	10	00	0	IC-Ib	-Ic	0	0	0	0	-IC	0
00	10	10	11	00	00	11	01	00	0	Ic-IA	-Ic	0	0	0	0	Ia+IA	0
11	10	10	11	00	00	00	00	10	0	-Ib	IC-Ic	0	0	0	0	0	-IC
00	10	10	11	00	00	11	00	10	0	-Ib	Ib-IA	0	0	0	0	0	Ia+IA
00	10	00	11	10	10	11	00	00	0	-IA	0	0	IA-Ib	-Ic	0	0	0
11	10	00	00	10	10	11	00	00	0	IB+Ia	0	0	Ic-IB	-Ic	0	0	0
00	10	00	11	10	00	11	00	10	0	-IA	0	0	IA-Ib	0	0	0	-Ic
11	10	00	00	10	00	11	00	10	0	IB-Ib	0	0	-IB	0	0	0	-Ic
00	10	00	11	00	10	11	10	00	0	-IA	0	0	0	-Ic	0	IA-Ib	0
11	10	00	11	00	10	00	10	00	0	IC-Ib	0	0	0	-Ic	0	-IC	0
11	10	00	00	00	10	11	00	10	0	-Ib	0	0	0	-IB	0	0	IB-Ic
11	10	00	11	00	10	00	00	10	0	-Ib	0	0	0	IC-Ic	0	0	-IC
00	10	00	11	00	00	11	10	10	0	-IA	0	0	0	0	0	IA-Ib	-Ic
11	10	00	11	00	00	00	10	10	0	IC+Ia	0	0	0	0	0	Ic-IC	-Ic
00	00	10	11	10	10	11	00	00	0	0	-IA	0	-Ib	IA-Ic	0	0	0
11	00	10	00	10	10	11	00	00	0	0	IB+Ia	0	-Ib	Ib-IB	0	0	0
11	00	10	00	10	00	11	10	00	0	0	-Ic	0	-IB	0	0	IB-Ib	0
11	00	10	11	10	00	00	10	00	0	0	-Ic	0	IC-Ib	0	0	-IC	0
00	00	10	11	10	00	11	00	10	0	0	-IA	0	-Ib	0	0	0	IA-Ic
11	00	10	11	10	00	00	00	10	0	0	IC-Ic	0	-Ib	0	0	0	-IC
00	00	10	11	00	10	11	10	00	0	0	-IA	0	0	IA-Ic	0	-Ib	0
11	00	10	00	00	10	11	10	00	0	0	IB-Ic	0	0	-IB	0	-Ib	0
00	00	10	11	00	00	11	10	10	0	0	-IA	0	0	0	0	-Ib	IA-Ic
11	00	10	11	00	00	00	10	10	0	0	IC+Ia	0	0	0	0	-Ib	Ib-IC
11	00	00	00	10	10	11	10	00	0	0	0	0	Ic-IB	-Ic	0	IB+Ia	0
11	00	00	11	10	10	00	10	00	0	0	0	0	IC-Ib	-Ic	0	-IC	0
11	00	00	00	10	10	11	00	10	0	0	0	0	-Ib	Ib-IB	0	0	IB+Ia
11	00	00	11	10	10	00	00	10	0	0	0	0	-Ib	IC-Ic	0	0	IC
11	00	00	00	10	00	11	10	10	0	0	0	0	-IB	0	0	IB-Ib	-Ic
11	00	00	11	10	00	00	10	10	0	0	0	0	IC+Ia	0	0	Ic-IC	-Ic
11	00	00	00	00	10	11	10	10	0	0	0	0	0	-IB	0	-Ib	IB-Ic
11	00	00	11	00	10	00	10	10	0	0	0	0	0	IC+Ia	0	-Ib	Ib-IC
employ four capacitors																	
11	10	10	00	10	00	00	10	00	0	-Ib-IA	-Ic	0	-IB	0	0	-IC	0
00	10	10	00	10	00	11	10	00	0	Ic-IA	-Ic	0	-IB	0	0	Ia-IC	0

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
00	10	10	11	10	00	00	10	00	0	Ic-IA	-Ic	0	Ia-IB	0	0	-IC	0
11	10	10	00	10	00	00	00	10	0	IB-Ib	IC-Ic	0	-IB	0	0	0	-IC
00	10	10	00	10	00	11	00	10	0	IB-Ib	Ib+IC	0	-IB	0	0	0	Ia-IC
00	10	10	11	10	00	00	00	10	0	Ic+IB	IC-Ic	0	Ia-IB	0	0	0	-IC
11	10	10	00	00	10	00	10	00	0	IC-Ib	IB-Ic	0	0	-IB	0	-IC	0
00	10	10	00	00	10	11	10	00	0	Ic+IC	IB-Ic	0	0	-IB	0	Ia-IC	0
00	10	10	11	00	10	00	10	00	0	IC-Ib	Ib+IB	0	0	Ia-IB	0	-IC	0
11	10	10	00	00	10	00	00	10	0	-Ib	-Ic-IA	0	0	-IB	0	0	-IC
00	10	10	00	00	10	11	00	10	0	-Ib	Ib-IA	0	0	-IB	0	0	Ia-IC
00	10	10	11	00	10	00	00	10	0	-Ib	Ib-IA	0	0	Ia-IB	0	0	-IC
00	10	00	00	10	10	11	10	00	0	-IA	0	0	Ic-IB	-Ic	0	Ia-IC	0
00	10	00	11	10	10	00	10	00	0	-IA	0	0	-Ib-IB	-Ic	0	-IC	0
11	10	00	00	10	10	00	10	00	0	Ia-IA	0	0	Ic-IB	-Ic	0	-IC	0
00	10	00	00	10	10	11	00	10	0	-IA	0	0	IA-Ib	Ib+IC	0	0	Ia-IC
00	10	00	11	10	10	00	00	10	0	-IA	0	0	IA-Ib	IC-Ic	0	0	-IC
11	10	00	00	10	10	00	00	10	0	Ia-IA	0	0	Ic+IA	IC-Ic	0	0	-IC
00	10	00	00	10	00	11	10	10	0	-IA	0	0	-IB	0	0	-Ib-IC	-Ic
00	10	00	11	10	00	00	10	10	0	-IA	0	0	Ia-IB	0	0	Ic-IC	-Ic
00	10	00	11	00	10	00	10	10	0	-IA	0	0	Ia-IB	0	0	IA-Ib	Ib+IB
11	10	00	00	10	00	00	10	10	0	Ia-IA	0	0	-IB	0	0	Ic-IC	-Ic
00	10	00	00	00	10	11	10	10	0	-IA	0	0	0	-IB	0	IA-Ib	IB-Ic
11	10	00	00	00	10	00	10	10	0	Ia-IA	0	0	0	-IB	0	Ic+IA	IB-Ic
00	00	10	00	10	10	11	10	00	0	0	-IA	0	Ic+IC	IA-Ic	0	Ia-IC	0
00	00	10	11	10	10	00	10	00	0	0	-IA	0	IC-Ib	IA-Ic	0	-IC	0
11	00	10	00	10	10	00	10	00	0	0	Ia-IA	0	IC-Ib	Ib+IA	0	-IC	0
00	00	10	00	10	10	11	00	10	0	0	-IA	0	-Ib	Ib-IB	0	0	Ia-IC
00	00	10	11	10	10	00	00	10	0	0	-IA	0	-Ib	-Ic-IB	0	0	-IC
11	00	10	00	10	10	00	00	10	0	0	Ia-IA	0	-Ib	Ib-IB	0	0	-IC
00	00	10	00	10	00	11	10	10	0	0	-IA	0	-IB	0	0	IB-Ib	IA-Ic
00	00	10	11	10	00	00	10	10	0	0	-IA	0	Ia-IB	0	0	Ic+IB	IA-Ic
11	00	10	00	10	00	00	10	10	0	0	Ia-IA	0	-IB	0	0	IB-Ib	Ib+IA
00	00	10	00	00	10	11	10	10	0	0	-IA	0	0	-IB	0	-Ib	-Ic-IC
00	00	10	11	00	10	00	10	10	0	0	-IA	0	0	Ia-IB	0	-Ib	Ib-IC
11	00	10	00	00	10	00	10	10	0	0	Ia-IA	0	0	-IB	0	-Ib	Ib-IC

Table B.5: Switching device combinations for (V_{AB},V_{BC},V_{CA}) = (0,0,0) and (V_{ab},V_{bc},V_{ca}) = (0,$-V_{cap}$,V_{cap}).

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
employ single capacitor																	
11	11	10	11	00	00	11	00	00	0	0	-Ic	0	0	0	0	0	0
11	11	10	11	00	00	00	11	00	0	0	-Ic	0	0	0	0	0	0
11	11	10	00	11	00	11	00	00	0	0	-Ic	0	0	0	0	0	0
11	11	10	00	11	00	00	11	00	0	0	-Ic	0	0	0	0	0	0
11	00	10	11	00	00	11	11	00	0	0	-Ic	0	0	0	0	0	0
00	11	10	11	00	00	11	11	00	0	0	-Ic	0	0	0	0	0	0
11	00	10	00	11	00	11	11	00	0	0	-Ic	0	0	0	0	0	0
00	11	10	00	11	00	11	11	00	0	0	-Ic	0	0	0	0	0	0
11	00	10	11	11	00	11	00	00	0	0	-Ic	0	0	0	0	0	0
00	11	10	11	11	00	11	00	00	0	0	-Ic	0	0	0	0	0	0
11	00	10	11	11	00	00	11	00	0	0	-Ic	0	0	0	0	0	0
00	11	10	11	11	00	00	11	00	0	0	-Ic	0	0	0	0	0	0
11	00	00	11	00	10	11	11	00	0	0	0	0	0	-Ic	0	0	0
11	00	00	00	11	10	11	11	00	0	0	0	0	0	-Ic	0	0	0
00	11	00	11	00	10	11	11	00	0	0	0	0	0	-Ic	0	0	0
00	11	00	00	11	10	11	11	00	0	0	0	0	0	-Ic	0	0	0
11	00	00	11	11	10	11	00	00	0	0	0	0	0	-Ic	0	0	0
00	11	00	11	11	10	11	00	00	0	0	0	0	0	-Ic	0	0	0
11	00	00	11	11	10	00	11	00	0	0	0	0	0	-Ic	0	0	0
00	11	00	11	11	10	00	11	00	0	0	0	0	0	-Ic	0	0	0
11	11	00	11	00	10	11	00	00	0	0	0	0	0	-Ic	0	0	0
11	11	00	00	11	10	11	00	00	0	0	0	0	0	-Ic	0	0	0
11	11	00	11	00	10	00	11	00	0	0	0	0	0	-Ic	0	0	0
11	11	00	00	11	10	00	11	00	0	0	0	0	0	-Ic	0	0	0
11	00	00	11	00	00	11	11	10	0	0	0	0	0	0	0	0	-Ic
11	00	00	00	11	00	11	11	10	0	0	0	0	0	0	0	0	-Ic
00	11	00	11	00	00	11	11	10	0	0	0	0	0	0	0	0	-Ic
00	11	00	00	11	00	11	11	10	0	0	0	0	0	0	0	0	-Ic
11	00	00	11	11	00	11	00	10	0	0	0	0	0	0	0	0	-Ic
11	00	00	11	11	00	00	11	10	0	0	0	0	0	0	0	0	-Ic
00	11	00	11	11	00	11	00	10	0	0	0	0	0	0	0	0	-Ic
00	11	00	11	11	00	00	11	10	0	0	0	0	0	0	0	0	-Ic
11	11	00	11	00	00	11	00	10	0	0	0	0	0	0	0	0	-Ic
11	11	00	11	00	00	00	11	10	0	0	0	0	0	0	0	0	-Ic
11	11	00	00	11	00	11	00	10	0	0	0	0	0	0	0	0	-Ic
11	11	00	00	11	00	00	11	10	0	0	0	0	0	0	0	0	-Ic
employ two capacitors																	
01	01	11	00	00	11	00	00	11	Ia	Ib	0	0	0	0	0	0	0
01	00	11	00	01	11	00	00	11	Ia	0	0	0	Ib	0	0	0	0
01	00	11	00	00	11	00	01	11	Ia	0	0	0	0	0	0	Ib	0
00	01	11	01	00	11	00	00	11	0	Ib	0	Ia	0	0	0	0	0

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
00	01	11	00	00	11	01	00	11	0	Ib	0	0	0	0	Ia	0	0
00	00	10	11	00	10	11	11	00	0	0	-IA	0	0	IA-Ic	0	0	0
00	00	10	00	11	10	11	11	00	0	0	-IA	0	0	IA-Ic	0	0	0
11	11	10	00	00	10	11	00	00	0	0	IB-Ic	0	0	-IB	0	0	0
11	11	10	00	00	10	00	11	00	0	0	IB-Ic	0	0	-IB	0	0	0
11	00	10	00	00	10	11	11	00	0	0	IB-Ic	0	0	-IB	0	0	0
00	11	10	00	00	10	11	11	00	0	0	IB-Ic	0	0	-IB	0	0	0
00	00	10	11	11	10	11	00	00	0	0	-IA	0	0	IA-Ic	0	0	0
00	00	10	11	11	10	00	11	00	0	0	-IA	0	0	IA-Ic	0	0	0
11	00	10	00	11	10	11	00	00	0	0	IB+Ia	0	0	Ib-IB	0	0	0
00	11	10	11	00	10	11	00	00	0	0	Ib-IA	0	0	Ia+IA	0	0	0
11	00	10	00	11	10	00	11	00	0	0	Ia-IA	0	0	IA+Ib	0	0	0
00	11	10	11	00	10	00	11	00	0	0	Ib+IB	0	0	Ia-IB	0	0	0
00	00	10	11	00	00	11	11	10	0	0	-IA	0	0	0	0	0	IA-Ic
00	00	10	00	11	00	11	11	10	0	0	-IA	0	0	0	0	0	IA-Ic
00	00	10	11	11	00	11	00	10	0	0	-IA	0	0	0	0	0	IA-Ic
00	00	10	11	11	00	00	11	10	0	0	-IA	0	0	0	0	0	IA-Ic
11	11	10	11	00	00	00	00	10	0	0	IC-Ic	0	0	0	0	0	-IC
11	11	10	00	11	00	00	00	10	0	0	IC-Ic	0	0	0	0	0	-IC
00	11	10	11	00	00	11	00	10	0	0	Ib-IA	0	0	0	0	0	Ia+IA
11	00	10	11	00	00	00	11	10	0	0	IC+Ia	0	0	0	0	0	Ib-IC
00	11	10	00	11	00	11	00	10	0	0	IC+Ib	0	0	0	0	0	Ia-IC
11	00	10	00	11	00	00	11	10	0	0	Ia-IA	0	0	0	0	0	IA+Ib
11	00	10	11	11	00	00	00	10	0	0	IC-Ic	0	0	0	0	0	-IC
00	11	10	11	11	00	00	00	10	0	0	IC-Ic	0	0	0	0	0	-IC
00	00	11	01	01	11	00	00	11	0	0	0	Ia	Ib	0	0	0	0
00	00	11	01	00	11	00	01	11	0	0	0	Ia	0	0	0	Ib	0
00	00	11	00	01	11	01	00	11	0	0	0	0	Ib	0	Ia	0	0
11	00	00	00	00	10	11	11	10	0	0	0	0	0	-IB	0	0	IB-Ic
00	11	00	00	00	10	11	11	10	0	0	0	0	0	-IB	0	0	IB-Ic
11	00	00	11	00	10	00	11	10	0	0	0	0	0	IC+Ia	0	0	Ib-IC
11	00	00	00	11	10	11	00	10	0	0	0	0	0	Ib-IB	0	0	IB+Ia
00	11	00	11	00	10	00	11	10	0	0	0	0	0	Ia-IB	0	0	Ib+IB
00	11	00	00	11	10	11	00	10	0	0	0	0	0	IC+Ib	0	0	Ia-IC
11	11	00	00	00	10	11	00	10	0	0	0	0	0	-IB	0	0	IB-Ic
11	11	00	00	00	10	00	11	10	0	0	0	0	0	-IB	0	0	IB-Ic
11	00	00	11	11	10	00	00	10	0	0	0	0	0	IC-Ic	0	0	-IC
00	11	00	11	11	10	00	00	10	0	0	0	0	0	IC-Ic	0	0	-IC
11	11	00	11	00	10	00	00	10	0	0	0	0	0	IC-Ic	0	0	-IC
11	11	00	00	11	10	00	00	10	0	0	0	0	0	IC-Ic	0	0	-IC
00	00	11	00	00	11	01	01	11	0	0	0	0	0	0	Ia	Ib	0
employ three capacitors																	
01	01	11	01	00	00	00	00	11	Ia-IB	Ib	0	IB	0	0	0	0	0
01	01	00	01	00	11	00	00	11	IA-Ib	Ib	0	-Ic-IA	0	0	0	0	0
01	01	11	00	01	00	00	00	11	Ia	Ib-IB	0	0	IB	0	0	0	0

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
01	01	00	00	01	11	00	00	11	Ia	IA-Ia	0	0	-Ic-IA	0	0	0	0
01	01	11	00	00	11	01	00	00	Ia-IC	Ib	0	0	0	0	IC	0	0
01	01	00	00	00	11	01	00	11	IA-Ib	Ib	0	0	0	0	-Ic-IA	0	0
01	01	11	00	00	11	00	01	00	Ia	Ib-IC	0	0	0	0	0	IC	0
01	01	00	00	00	11	00	01	11	Ia	IA-Ia	0	0	0	0	0	-Ic-IA	0
01	00	00	01	01	11	00	00	11	IA	0	0	Ia-IA	Ib	0	0	0	0
01	00	11	01	01	00	00	00	11	-Ic-IB	0	0	IB-Ib	Ib	0	0	0	0
01	00	00	01	00	11	00	01	11	IA	0	0	Ia-IA	0	0	0	Ib	0
01	00	11	01	00	00	00	01	11	Ia-IB	0	0	IB	0	0	0	Ib	0
01	00	00	00	01	11	01	00	11	IA	0	0	0	Ib	0	Ia-IA	0	0
01	00	11	00	01	11	01	00	00	Ia-IC	0	0	0	Ib	0	IC	0	0
01	00	11	00	01	00	00	01	11	Ia	0	0	0	IB	0	0	Ib-IB	0
01	00	11	00	01	11	00	01	00	Ia	0	0	0	Ib-IC	0	0	IC	0
01	00	00	00	00	11	01	01	11	IA	0	0	0	0	0	Ia-IA	Ib	0
01	00	11	00	00	11	01	01	00	-Ic-IC	0	0	0	0	0	IC-Ib	Ib	0
00	01	00	01	01	11	00	00	11	0	IA	0	Ia	Ib-IA	0	0	0	0
00	01	11	01	01	00	00	00	11	0	-Ic-IB	0	Ia	IB-Ia	0	0	0	0
00	01	11	01	00	00	01	00	11	0	Ib	0	IB	0	0	Ia-IB	0	0
00	01	11	01	00	11	01	00	00	0	Ib	0	Ia-IC	0	0	IC	0	0
00	01	00	01	00	11	00	01	11	0	IA	0	Ia	0	0	0	Ib-IA	0
00	01	11	01	00	11	00	01	00	0	Ib-IC	0	Ia	0	0	0	IC	0
00	01	00	00	01	11	01	00	11	0	IA	0	0	Ib-IA	0	Ia	0	0
00	01	11	00	01	00	01	00	11	0	Ib-IB	0	0	IB	0	Ia	0	0
00	01	00	00	00	11	01	01	11	0	IA	0	0	0	0	Ia	Ib-IA	0
00	01	11	00	00	11	01	01	00	0	-Ic-IC	0	0	0	0	Ia	IC-Ia	0
11	11	10	00	00	10	00	00	10	0	0	-Ic-IA	0	-IB	0	0	0	-IC
00	00	10	00	00	10	11	11	10	0	0	-IA	0	0	-IB	0	0	-Ic-IC
00	00	10	11	00	10	00	11	10	0	0	-IA	0	0	Ia-IB	0	0	Ib-IC
00	00	10	00	11	10	11	00	10	0	0	-IA	0	0	Ib-IB	0	0	Ia-IC
00	11	10	00	00	10	11	00	10	0	0	Ib-IA	0	0	-IB	0	0	Ia-IC
11	00	10	00	00	10	00	11	10	0	0	Ia-IA	0	0	-IB	0	0	Ib-IC
00	00	10	11	11	10	00	00	10	0	0	-IA	0	0	-Ic-IB	0	0	-IC
11	00	10	00	11	10	00	00	10	0	0	Ia-IA	0	0	Ib-IB	0	0	-IC
00	11	10	11	00	10	00	00	10	0	0	Ib-IA	0	0	Ia-IB	0	0	-IC
00	00	11	01	01	00	01	00	11	0	0	0	IB-Ib	Ib	0	-Ic-IB	0	0
00	00	11	01	01	11	01	00	00	0	0	0	Ia-IC	Ib	0	IC	0	0
00	00	11	01	01	00	00	01	11	0	0	0	Ia	IB-Ia	0	0	-Ic-IB	0
00	00	11	01	01	11	00	01	00	0	0	0	Ia	Ib-IC	0	0	IC	0
00	00	11	01	00	00	01	01	11	0	0	0	IB	0	0	Ia-IB	Ib	0
00	00	11	01	00	11	01	01	00	0	0	0	-Ic-IC	0	0	IC-Ib	Ib	0
00	00	11	00	01	00	01	01	11	0	0	0	0	IB	0	Ia	Ib-IB	0
00	00	11	00	01	11	01	01	00	0	0	0	0	-Ic-IC	0	Ia	IC-Ia	0
employ four capacitors																	
01	01	11	01	00	00	01	00	00	Ia+IA	Ib	0	IB	0	0	IC	0	0
01	01	00	01	00	00	01	00	11	IA-Ib	Ib	0	IB	0	0	IC-Ic	0	0

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
01	01	00	01	00	11	01	00	00	IA-Ib	Ib	0	IB-Ic	0	0	IC	0	0
01	01	11	01	00	00	00	01	00	Ia-IB	Ib-IC	0	IB	0	0	0	IC	0
01	01	00	01	00	00	00	01	11	Ia-IB	-Ia-IC	0	IB	0	0	0	IC-Ic	0
01	01	00	01	00	11	00	01	00	-Ib-IB	Ib-IC	0	IB-Ic	0	0	0	IC	0
01	01	11	00	01	00	01	00	00	Ia-IC	Ib-IB	0	0	IB	0	IC	0	0
01	01	00	00	01	00	01	00	11	-Ib-IC	Ib-IB	0	0	IB	0	IC-Ic	0	0
01	01	00	00	01	11	01	00	00	Ia-IC	-Ia-IB	0	0	IB-Ic	0	IC	0	0
01	01	11	00	01	00	00	01	00	Ia	IA+Ib	0	0	IB	0	0	IC	0
01	01	00	00	01	00	00	01	11	Ia	IA-Ia	0	0	IB	0	0	IC-Ic	0
01	01	00	00	01	11	00	01	00	Ia	IA-Ia	0	0	IB-Ic	0	0	IC	0
01	00	00	01	01	00	01	00	11	IA	0	0	IB-Ib	Ib	0	IC-Ic	0	0
01	00	00	01	01	11	01	00	00	IA	0	0	Ia+IB	Ib	0	IC	0	0
01	00	11	01	01	00	01	00	00	IA-Ic	0	0	IB-Ib	Ib	0	IC	0	0
01	00	00	01	01	00	00	01	11	IA	0	0	Ia-IA	-Ia-IC	0	0	IC-Ic	0
01	00	00	01	01	11	00	01	00	IA	0	0	Ia-IA	Ib-IC	0	0	IC	0
01	00	11	01	01	00	00	01	00	IA-Ic	0	0	-Ib-IA	Ib-IC	0	0	IC	0
01	00	00	01	00	00	01	01	11	IA	0	0	IB	0	0	Ia+IC	Ib	0
01	00	00	01	00	11	01	01	00	IA	0	0	IB-Ic	0	0	IC-Ib	Ib	0
01	00	11	01	00	00	01	01	00	IA-Ic	0	0	IB	0	0	IC-Ib	Ib	0
01	00	00	00	01	00	01	01	11	IA	0	0	0	IB	0	Ia-IA	Ib-IB	0
01	00	00	00	01	11	01	01	00	IA	0	0	0	IB-Ic	0	Ia-IA	-Ia-IB	0
01	00	11	00	01	00	01	01	00	IA-Ic	0	0	0	IB	0	-Ib-IA	Ib-IB	0
00	01	00	01	01	00	01	00	11	0	IA	0	-Ib-IC	Ib-IA	0	IC-Ic	0	0
00	01	00	01	01	11	01	00	00	0	IA	0	Ia-IC	Ib-IA	0	IC	0	0
00	01	11	01	01	00	01	00	00	0	IA-Ic	0	Ia-IC	-Ia-IA	0	IC	0	0
00	01	00	01	01	00	00	01	11	0	IA	0	Ia	IB-Ia	0	0	IC-Ic	0
00	01	00	01	01	11	00	01	00	0	IA	0	Ia	Ib+IB	0	0	IC	0
00	01	11	01	01	00	00	01	00	0	IA-Ic	0	Ia	IB-Ia	0	0	IC	0
00	01	00	01	00	00	01	01	11	0	IA	0	IB	0	0	Ia-IB	Ib-IA	0
00	01	00	01	00	11	01	01	00	0	IA	0	IB-Ic	0	0	-Ib-IB	Ib-IA	0
00	01	11	01	00	00	01	01	00	0	IA-Ic	0	IB	0	0	Ia-IB	-Ia-IA	0
00	01	00	00	01	00	01	01	11	0	IA	0	0	IB	0	Ia	IC+Ib	0
00	01	00	00	01	11	01	01	00	0	IA	0	0	IB-Ic	0	Ia	IC-Ia	0
00	01	11	00	01	00	01	01	00	0	IA-Ic	0	0	IB	0	Ia	IC-Ia	0

Table B.6: Switching device combinations for (V_{AB},V_{BC},V_{CA}) = (0,0,0) and (V_{ab},V_{bc},V_{ca}) = (V_{cap},$-V_{cap}$,0).

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
employ single capacitor																	
11	01	11	11	00	00	11	00	00	0	Ib	0	0	0	0	0	0	0
11	01	11	11	00	00	00	00	11	0	Ib	0	0	0	0	0	0	0
11	01	11	00	00	11	11	00	00	0	Ib	0	0	0	0	0	0	0
11	01	11	00	00	11	00	00	11	0	Ib	0	0	0	0	0	0	0
11	01	00	11	00	00	11	00	11	0	Ib	0	0	0	0	0	0	0
00	01	11	11	00	00	11	00	11	0	Ib	0	0	0	0	0	0	0
11	01	00	00	00	11	11	00	11	0	Ib	0	0	0	0	0	0	0
00	01	11	00	00	11	11	00	11	0	Ib	0	0	0	0	0	0	0
11	01	00	11	00	11	11	00	00	0	Ib	0	0	0	0	0	0	0
00	01	11	11	00	11	11	00	00	0	Ib	0	0	0	0	0	0	0
11	01	00	11	00	11	00	00	11	0	Ib	0	0	0	0	0	0	0
00	01	11	11	00	11	00	00	11	0	Ib	0	0	0	0	0	0	0
11	00	00	11	01	00	11	00	11	0	0	0	0	Ib	0	0	0	0
11	00	00	00	01	11	11	00	11	0	0	0	0	Ib	0	0	0	0
00	00	11	11	01	00	11	00	11	0	0	0	0	Ib	0	0	0	0
00	00	11	00	01	11	11	00	11	0	0	0	0	Ib	0	0	0	0
11	00	00	11	01	11	11	00	00	0	0	0	0	Ib	0	0	0	0
00	00	11	11	01	11	11	00	00	0	0	0	0	Ib	0	0	0	0
11	00	00	11	01	11	00	00	11	0	0	0	0	Ib	0	0	0	0
00	00	11	11	01	11	00	00	11	0	0	0	0	Ib	0	0	0	0
11	00	11	11	01	00	11	00	00	0	0	0	0	Ib	0	0	0	0
11	00	11	00	01	11	11	00	00	0	0	0	0	Ib	0	0	0	0
11	00	11	11	01	00	00	00	11	0	0	0	0	Ib	0	0	0	0
11	00	11	00	01	11	00	00	11	0	0	0	0	Ib	0	0	0	0
11	00	00	11	00	00	11	01	11	0	0	0	0	0	0	0	Ib	0
11	00	00	00	00	11	11	01	11	0	0	0	0	0	0	0	Ib	0
00	00	11	11	00	00	11	01	11	0	0	0	0	0	0	0	Ib	0
00	00	11	00	00	11	11	01	11	0	0	0	0	0	0	0	Ib	0
11	00	00	11	00	11	11	01	00	0	0	0	0	0	0	0	Ib	0
11	00	00	11	00	11	00	01	11	0	0	0	0	0	0	0	Ib	0
00	00	11	11	00	11	11	01	00	0	0	0	0	0	0	0	Ib	0
00	00	11	11	00	11	00	01	11	0	0	0	0	0	0	0	Ib	0
11	00	11	11	00	00	11	01	00	0	0	0	0	0	0	0	Ib	0
11	00	11	11	00	00	00	01	11	0	0	0	0	0	0	0	Ib	0
11	00	11	00	00	11	11	01	00	0	0	0	0	0	0	0	Ib	0
11	00	11	00	00	11	00	01	11	0	0	0	0	0	0	0	Ib	0
employ two capacitors																	
10	11	10	00	11	00	00	11	00	-Ia	0	-Ic	0	0	0	0	0	0
10	11	00	00	11	10	00	11	00	-Ia	0	0	0	0	-Ic	0	0	0
10	11	00	00	11	00	00	11	10	-Ia	0	0	0	0	0	0	0	-Ic
00	01	00	11	01	00	11	00	11	0	IA	0	0	Ib-IA	0	0	0	0

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
00	01	00	00	01	11	11	00	11	0	IA	0	0	Ib-IA	0	0	0	0
11	01	11	00	01	00	11	00	00	0	Ib-IB	0	0	IB	0	0	0	0
11	01	11	00	01	00	00	00	11	0	Ib-IB	0	0	IB	0	0	0	0
11	01	00	00	01	00	11	00	11	0	Ib-IB	0	0	IB	0	0	0	0
00	01	11	00	01	00	11	00	11	0	Ib-IB	0	0	IB	0	0	0	0
00	01	00	11	01	11	11	00	00	0	IA	0	0	Ib-IA	0	0	0	0
00	01	00	11	01	11	00	00	11	0	IA	0	0	Ib-IA	0	0	0	0
11	01	00	00	01	11	11	00	00	0	-Ia-IB	0	0	IB-Ic	0	0	0	0
00	01	11	11	01	00	11	00	00	0	IA-Ic	0	0	-Ia-IA	0	0	0	0
11	01	00	00	01	11	00	00	11	0	IA-Ia	0	0	-Ic-IA	0	0	0	0
00	01	11	11	01	00	00	00	11	0	-Ic-IB	0	0	IB-Ia	0	0	0	0
00	01	00	11	00	00	11	01	11	0	IA	0	0	0	0	0	Ib-IA	0
00	01	00	00	00	11	11	01	11	0	IA	0	0	0	0	0	Ib-IA	0
00	01	00	11	00	11	11	01	00	0	IA	0	0	0	0	0	Ib-IA	0
00	01	00	11	00	11	00	01	11	0	IA	0	0	0	0	0	Ib-IA	0
11	01	11	11	00	00	00	01	00	0	Ib-IC	0	0	0	0	0	IC	0
11	01	11	00	00	11	00	01	00	0	Ib-IC	0	0	0	0	0	IC	0
00	01	11	11	00	00	11	01	00	0	IA-Ic	0	0	0	0	0	-Ia-IA	0
11	01	00	11	00	00	00	01	11	0	-Ia-IC	0	0	0	0	0	IC-Ic	0
00	01	11	00	00	11	11	01	00	0	-Ic-IC	0	0	0	0	0	IC-Ia	0
11	01	00	00	00	11	00	01	11	0	IA-Ia	0	0	0	0	0	-Ic-IA	0
11	01	00	11	00	11	00	01	00	0	Ib-IC	0	0	0	0	0	IC	0
00	01	11	11	00	11	00	01	00	0	Ib-IC	0	0	0	0	0	IC	0
00	11	10	10	11	00	00	11	00	0	0	-Ic	-Ia	0	0	0	0	0
00	11	10	00	11	00	10	11	00	0	0	-Ic	0	0	0	-Ia	0	0
00	11	00	10	11	10	00	11	00	0	0	0	-Ia	0	-Ic	0	0	0
00	11	00	10	11	00	00	11	10	0	0	0	-Ia	0	0	0	0	-Ic
11	00	00	00	01	00	11	01	11	0	0	0	0	IB	0	0	Ib-IB	0
00	00	11	00	01	00	11	01	11	0	0	0	0	IB	0	0	Ib-IB	0
11	00	00	11	01	00	00	01	11	0	0	0	0	-Ia-IC	0	0	IC-Ic	0
11	00	00	00	01	11	11	01	00	0	0	0	0	IB-Ic	0	0	-Ia-IB	0
00	00	11	11	01	00	00	01	11	0	0	0	0	IB-Ia	0	0	-Ic-IB	0
00	00	11	00	01	11	11	01	00	0	0	0	0	-Ic-IC	0	0	IC-Ia	0
11	00	11	00	01	00	11	01	00	0	0	0	0	IB	0	0	Ib-IB	0
11	00	11	00	01	00	00	01	11	0	0	0	0	IB	0	0	Ib-IB	0
11	00	00	11	01	11	00	01	00	0	0	0	0	Ib-IC	0	0	IC	0
00	00	11	11	01	11	00	01	00	0	0	0	0	Ib-IC	0	0	IC	0
11	00	11	11	01	00	00	01	00	0	0	0	0	Ib-IC	0	0	IC	0
11	00	11	00	01	11	00	01	00	0	0	0	0	Ib-IC	0	0	IC	0
00	11	00	00	11	10	10	11	00	0	0	0	0	0	-Ic	-Ia	0	0
00	11	00	00	11	00	10	11	10	0	0	0	0	0	0	-Ia	0	-Ic
employ three capacitors																	
10	11	10	10	00	00	00	11	00	IB-Ia	0	-Ic	-IB	0	0	0	0	0
10	00	10	10	11	00	00	11	00	Ic-IA	0	-Ic	IA+Ib	0	0	0	0	0
10	11	10	00	00	10	00	11	00	-Ia	0	IB-Ic	0	0	-IB	0	0	0

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
10	00	10	00	11	10	00	11	00	-Ia	0	Ia-IA	0	0	IA+Ib	0	0	0
10	11	10	00	11	00	10	00	00	IC-Ia	0	-Ic	0	0	0	-IC	0	0
10	00	10	00	11	00	10	11	00	Ic-IA	0	-Ic	0	0	0	IA+Ib	0	0
10	11	10	00	11	00	00	00	10	-Ia	0	IC-Ic	0	0	0	0	0	-IC
10	00	10	00	11	00	00	11	10	-Ia	0	Ia-IA	0	0	0	0	0	IA+Ib
10	00	00	10	11	10	00	11	00	-IA	0	0	IA-Ia	0	-Ic	0	0	0
10	11	00	10	00	10	00	11	00	Ib+IB	0	0	Ic-IB	0	-Ic	0	0	0
10	00	00	10	11	00	00	11	10	-IA	0	0	IA-Ia	0	0	0	0	-Ic
10	11	00	10	00	00	00	11	10	IB-Ia	0	0	-IB	0	0	0	0	-Ic
10	00	00	00	11	10	10	11	00	-IA	0	0	0	0	-Ic	IA-Ia	0	0
10	11	00	00	11	10	10	00	00	IC-Ia	0	0	0	0	-Ic	-IC	0	0
10	11	00	00	00	10	00	11	10	-Ia	0	0	0	0	-IB	0	0	IB-Ic
10	11	00	00	11	10	00	00	10	-Ia	0	0	0	0	IC-Ic	0	0	-IC
10	00	00	00	11	00	10	11	10	-IA	0	0	0	0	0	IA-Ia	0	-Ic
10	11	00	00	11	00	10	00	10	IC+Ib	0	0	0	0	0	Ic-IC	0	-Ic
00	01	00	00	01	00	11	01	11	0	IA	0	0	IB	0	0	IC+Ib	0
00	01	00	11	01	00	00	01	11	0	IA	0	0	IB-Ia	0	0	IC-Ic	0
00	01	00	00	01	11	11	01	00	0	IA	0	0	IB-Ic	0	0	IC-Ia	0
11	01	11	00	01	00	00	01	00	0	Ib+IA	0	0	IB	0	0	IC	0
00	01	11	00	01	00	11	01	00	0	IA-Ic	0	0	IB	0	0	IC-Ia	0
11	01	00	00	01	00	00	01	11	0	IA-Ia	0	0	IB	0	0	IC-Ic	0
00	01	00	11	01	11	00	01	00	0	IA	0	0	Ib+IB	0	0	IC	0
11	01	00	00	01	11	00	01	00	0	IA-Ia	0	0	IB-Ic	0	0	IC	0
00	01	11	11	01	00	00	01	00	0	IA-Ic	0	0	IB-Ia	0	0	IC	0
00	00	10	10	11	10	00	11	00	0	0	-IA	-Ia	0	IA-Ic	0	0	0
00	11	10	10	00	10	00	11	00	0	0	Ib+IB	-Ia	0	Ia-IB	0	0	0
00	11	10	10	00	00	10	11	00	0	0	-Ic	-IB	0	0	IB-Ia	0	0
00	11	10	10	11	00	10	00	00	0	0	-Ic	IC-Ia	0	0	-IC	0	0
00	00	10	10	11	00	00	11	10	0	0	-IA	-Ia	0	0	0	0	IA-Ic
00	11	10	10	11	00	00	00	10	0	0	IC-Ic	-Ia	0	0	0	0	-IC
00	00	10	00	11	10	10	11	00	0	0	-IA	0	0	IA-Ic	-Ia	0	0
00	11	10	00	00	10	10	11	00	0	0	IB-Ic	0	0	-IB	-Ia	0	0
00	00	10	00	11	00	10	11	10	0	0	-IA	0	0	0	-Ia	0	IA-Ic
00	11	10	00	11	00	10	00	10	0	0	IC+Ib	0	0	0	-Ia	0	Ia-IC
00	11	00	10	00	10	10	11	00	0	0	0	Ic-IB	0	-Ic	Ib+IB	0	0
00	11	00	10	11	10	10	00	00	0	0	0	IC-Ia	0	-Ic	-IC	0	0
00	11	00	10	00	10	00	11	10	0	0	0	-Ia	0	Ia-IB	0	0	Ib+IB
00	11	00	10	11	10	00	00	10	0	0	0	-Ia	0	IC-Ic	0	0	-IC
00	11	00	10	00	00	10	11	10	0	0	0	-IB	0	0	IB-Ia	0	-Ic
00	11	00	10	11	00	10	00	10	0	0	0	IC+Ib	0	0	Ic-IC	0	-Ic
00	11	00	00	00	10	10	11	10	0	0	0	0	0	-IB	-Ia	0	IB-Ic
00	11	00	00	11	10	10	00	10	0	0	0	0	0	IC+Ib	-Ia	0	Ia-IC
employ four capacitors																	
10	11	10	10	00	00	10	00	00	-Ia-IA	0	-Ic	-IB	0	0	-IC	0	0
10	00	10	10	00	00	10	11	00	Ic-IA	0	-Ic	-IB	0	0	Ib-IC	0	0

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
10	00	10	10	11	00	10	00	00	Ic-IA	0	-Ic	Ib-IB	0	0	-IC	0	0
10	11	10	10	00	00	00	00	10	IB-Ia	0	IC-Ic	-IB	0	0	0	0	-IC
10	00	10	10	00	00	00	11	10	IB-Ia	0	Ia+IC	-IB	0	0	0	0	Ib-IC
10	00	10	10	11	00	00	00	10	Ic+IB	0	IC-Ic	Ib-IB	0	0	0	0	-IC
10	11	10	00	00	10	10	00	00	IC-Ia	0	IB-Ic	0	0	-IB	-IC	0	0
10	00	10	00	00	10	10	11	00	Ic+IC	0	IB-Ic	0	0	-IB	Ib-IC	0	0
10	00	10	00	11	10	10	00	00	IC-Ia	0	Ia+IB	0	0	Ib-IB	-IC	0	0
10	11	10	00	00	10	00	00	10	-Ia	0	-Ic-IA	0	0	-IB	0	0	-IC
10	00	10	00	00	10	00	11	10	-Ia	0	Ia-IA	0	0	-IB	0	0	Ib-IC
10	00	10	00	11	10	00	00	10	-Ia	0	Ia-IA	0	0	Ib-IB	0	0	-IC
10	00	00	10	00	10	10	11	00	-IA	0	0	Ic-IB	0	-Ic	Ib-IC	0	0
10	00	00	10	11	10	10	00	00	-IA	0	0	-Ia-IB	0	-Ic	-IC	0	0
10	11	00	10	00	10	10	00	00	Ib-IA	0	0	Ic-IB	0	-Ic	-IC	0	0
10	00	00	10	00	10	00	11	10	-IA	0	0	IA-Ia	0	Ia+IC	0	0	Ib-IC
10	00	00	10	11	10	00	00	10	-IA	0	0	IA-Ia	0	IC-Ic	0	0	-IC
10	11	00	10	00	10	00	00	10	Ib-IA	0	0	Ic+IA	0	IC-Ic	0	0	-IC
10	00	00	10	00	00	10	11	10	-IA	0	0	-IB	0	0	-Ia-IC	0	-Ic
10	00	00	10	11	00	10	00	10	-IA	0	0	Ib-IB	0	0	Ic-IC	0	-Ic
10	11	00	10	00	00	10	00	10	Ib-IA	0	0	-IB	0	0	Ic-IC	0	-Ic
10	00	00	00	00	10	10	11	10	-IA	0	0	0	0	-IB	IA-Ia	0	IB-Ic
10	00	00	00	11	10	10	00	10	-IA	0	0	0	0	Ib-IB	IA-Ia	0	Ia+IB
10	11	00	00	00	10	10	00	10	Ib-IA	0	0	0	0	-IB	Ic+IA	0	IB-Ic
00	00	10	10	00	10	10	11	00	0	0	-IA	Ic+IC	0	IA-Ic	Ib-IC	0	0
00	00	10	10	11	10	10	00	00	0	0	-IA	IC-Ia	0	IA-Ic	-IC	0	0
00	11	10	10	00	10	10	00	00	0	0	Ib-IA	IC-Ia	0	Ia+IA	-IC	0	0
00	00	10	10	00	10	00	11	10	0	0	-IA	-Ia	0	Ia-IB	0	0	Ib-IC
00	00	10	10	11	10	00	00	10	0	0	-IA	-Ia	0	-Ic-IB	0	0	-IC
00	11	10	10	00	10	00	00	10	0	0	Ib-IA	-Ia	0	Ia-IB	0	0	-IC
00	00	10	10	00	00	10	11	10	0	0	-IA	-IB	0	0	IB-Ia	0	IA-Ic
00	00	10	10	11	00	10	00	10	0	0	-IA	Ib-IB	0	0	Ic+IB	0	IA-Ic
00	11	10	10	00	00	10	00	10	0	0	Ib-IA	-IB	0	0	IB-Ia	0	Ia+IA
00	00	10	00	00	10	10	11	10	0	0	-IA	0	0	-IB	-Ia	0	-Ic-IC
00	00	10	00	11	10	10	00	10	0	0	-IA	0	0	Ib-IB	-Ia	0	Ia-IC
00	11	10	00	00	10	10	00	10	0	0	Ib-IA	0	0	-IB	-Ia	0	Ia-IC

Table B.7: Switching device combinations for (V_{AB},V_{BC},V_{CA}) = ($+V_{cap}$,0,$-V_{cap}$) and (V_{ab},V_{bc},V_{ca}) = (0,0,0).

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
employ single capacitor																	
01	00	00	11	00	00	11	11	11	IA	0	0	0	0	0	0	0	0
01	00	00	00	11	00	11	11	11	IA	0	0	0	0	0	0	0	0
01	00	00	00	00	11	11	11	11	IA	0	0	0	0	0	0	0	0
01	00	00	11	11	00	11	00	11	IA	0	0	0	0	0	0	0	0
01	00	00	11	11	00	00	11	11	IA	0	0	0	0	0	0	0	0
01	00	00	11	00	11	11	11	00	IA	0	0	0	0	0	0	0	0
01	00	00	11	00	11	00	11	11	IA	0	0	0	0	0	0	0	0
01	00	00	00	11	11	11	11	00	IA	0	0	0	0	0	0	0	0
01	00	00	00	11	11	11	00	11	IA	0	0	0	0	0	0	0	0
01	00	00	11	11	11	11	00	00	IA	0	0	0	0	0	0	0	0
01	00	00	11	11	11	00	11	00	IA	0	0	0	0	0	0	0	0
01	00	00	11	11	11	00	00	11	IA	0	0	0	0	0	0	0	0
00	01	00	11	00	00	11	11	11	0	IA	0	0	0	0	0	0	0
00	01	00	00	11	00	11	11	11	0	IA	0	0	0	0	0	0	0
00	01	00	00	00	11	11	11	11	0	IA	0	0	0	0	0	0	0
00	01	00	11	11	00	11	00	11	0	IA	0	0	0	0	0	0	0
00	01	00	11	11	00	00	11	11	0	IA	0	0	0	0	0	0	0
00	01	00	11	00	11	11	11	00	0	IA	0	0	0	0	0	0	0
00	01	00	11	00	11	00	11	11	0	IA	0	0	0	0	0	0	0
00	01	00	00	11	11	11	11	00	0	IA	0	0	0	0	0	0	0
00	01	00	00	11	11	11	00	11	0	IA	0	0	0	0	0	0	0
00	01	00	11	11	11	11	00	00	0	IA	0	0	0	0	0	0	0
00	01	00	11	11	11	00	11	00	0	IA	0	0	0	0	0	0	0
00	01	00	11	11	11	00	00	11	0	IA	0	0	0	0	0	0	0
00	00	01	11	00	00	11	11	11	0	0	IA	0	0	0	0	0	0
00	00	01	00	11	00	11	11	11	0	0	IA	0	0	0	0	0	0
00	00	01	00	00	11	11	11	11	0	0	IA	0	0	0	0	0	0
00	00	01	11	11	00	11	00	11	0	0	IA	0	0	0	0	0	0
00	00	01	11	11	00	00	11	11	0	0	IA	0	0	0	0	0	0
00	00	01	11	00	11	11	11	00	0	0	IA	0	0	0	0	0	0
00	00	01	11	00	11	00	11	11	0	0	IA	0	0	0	0	0	0
00	00	01	00	11	11	11	11	00	0	0	IA	0	0	0	0	0	0
00	00	01	00	11	11	11	00	11	0	0	IA	0	0	0	0	0	0
00	00	01	11	11	11	11	00	00	0	0	IA	0	0	0	0	0	0
00	00	01	11	11	11	00	11	00	0	0	IA	0	0	0	0	0	0
00	00	01	11	11	11	00	00	11	0	0	IA	0	0	0	0	0	0
employ two capacitors																	
01	01	00	11	00	00	11	00	11	IA-Ib	Ib	0	0	0	0	0	0	0
01	01	00	11	00	00	00	11	11	Ia-IB	-Ia-IC	0	0	0	0	0	0	0
01	01	00	00	11	00	11	00	11	-Ib-IC	Ib-IB	0	0	0	0	0	0	0
01	01	00	00	11	00	00	11	11	Ia	IA-Ia	0	0	0	0	0	0	0

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
01	01	00	00	00	11	11	00	11	IA-Ib	Ib	0	0	0	0	0	0	0
01	01	00	00	00	11	00	11	11	Ia	IA-Ia	0	0	0	0	0	0	0
01	01	00	11	00	11	11	00	00	IA-Ib	Ib	0	0	0	0	0	0	0
01	01	00	00	11	11	11	00	00	Ia-IC	-Ia-IB	0	0	0	0	0	0	0
01	01	00	11	00	11	00	11	00	-Ib-IB	Ib-IC	0	0	0	0	0	0	0
01	01	00	00	11	11	00	11	00	Ia	IA-Ia	0	0	0	0	0	0	0
01	01	00	11	00	11	00	00	11	IA-Ib	Ib	0	0	0	0	0	0	0
01	01	00	00	11	11	00	00	11	Ia	IA-Ia	0	0	0	0	0	0	0
01	00	01	11	00	00	11	11	00	IA-Ic	0	Ic	0	0	0	0	0	0
01	00	01	11	00	00	00	11	11	Ia-IB	0	-Ia-IC	0	0	0	0	0	0
01	00	01	00	11	00	11	11	00	IA-Ic	0	Ic	0	0	0	0	0	0
01	00	01	00	11	00	00	11	11	Ia	0	IA-Ia	0	0	0	0	0	0
01	00	01	00	00	11	11	11	00	-Ic-IC	0	Ic-IB	0	0	0	0	0	0
01	00	01	00	00	11	00	11	11	Ia	0	IA-Ia	0	0	0	0	0	0
01	00	01	11	11	00	11	00	00	IA-Ic	0	Ic	0	0	0	0	0	0
01	00	01	00	11	11	11	00	00	Ia-IC	0	-Ia-IB	0	0	0	0	0	0
01	00	01	11	11	00	00	11	00	IA-Ic	0	Ic	0	0	0	0	0	0
01	00	01	00	11	11	00	11	00	Ia	0	IA-Ia	0	0	0	0	0	0
01	00	01	11	11	00	00	00	11	-Ic-IB	0	Ic-IC	0	0	0	0	0	0
01	00	01	00	11	11	00	00	11	Ia	0	IA-Ia	0	0	0	0	0	0
00	01	01	11	00	00	11	11	00	0	IA-Ic	Ic	0	0	0	0	0	0
00	01	01	11	00	00	11	00	11	0	Ib	IA-Ib	0	0	0	0	0	0
00	01	01	00	11	00	11	11	00	0	IA-Ic	Ic	0	0	0	0	0	0
00	01	01	00	11	00	11	00	11	0	Ib-IB	-Ib-IC	0	0	0	0	0	0
00	01	01	00	00	11	11	11	00	0	-Ic-IC	Ic-IB	0	0	0	0	0	0
00	01	01	00	00	11	11	00	11	0	Ib	IA-Ib	0	0	0	0	0	0
00	01	01	11	11	00	11	00	00	0	IA-Ic	Ic	0	0	0	0	0	0
00	01	01	11	00	11	11	00	00	0	Ib	IA-Ib	0	0	0	0	0	0
00	01	01	11	11	00	00	11	00	0	IA-Ic	Ic	0	0	0	0	0	0
00	01	01	11	00	11	00	11	00	0	Ib-IC	-Ib-IB	0	0	0	0	0	0
00	01	01	11	11	00	00	00	11	0	-Ic-IB	Ic-IC	0	0	0	0	0	0
00	01	01	11	00	11	00	00	11	0	Ib	IA-Ib	0	0	0	0	0	0
11	11	11	10	00	00	10	00	00	0	0	0	-IB	0	0	-IC	0	0
11	11	11	10	00	00	00	10	00	0	0	0	-IB	0	0	0	-IC	0
11	11	11	10	00	00	00	00	10	0	0	0	-IB	0	0	0	0	-IC
11	11	11	00	10	00	10	00	00	0	0	0	0	-IB	0	-IC	0	0
11	11	11	00	10	00	00	10	00	0	0	0	0	-IB	0	0	-IC	0
11	11	11	00	10	00	00	00	10	0	0	0	0	-IB	0	0	0	-IC
11	11	11	00	00	10	10	00	00	0	0	0	0	0	-IB	-IC	0	0
11	11	11	00	00	10	00	10	00	0	0	0	0	0	-IB	0	-IC	0
11	11	11	00	00	10	00	00	10	0	0	0	0	0	-IB	0	0	-IC
employ three capacitors																	
01	01	01	11	00	00	11	00	00	IA+Ia	Ib	Ic	0	0	0	0	0	0
01	01	01	11	00	00	00	11	00	Ia-IB	Ib-IC	Ic	0	0	0	0	0	0
01	01	01	11	00	00	00	00	11	Ia-IB	Ib	Ic-IC	0	0	0	0	0	0

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
01	01	01	00	11	00	11	00	00	Ia-IC	Ib-IB	Ic	0	0	0	0	0	0
01	01	01	00	11	00	00	11	00	Ia	IA+Ib	Ic	0	0	0	0	0	0
01	01	01	00	11	00	00	00	11	Ia	Ib-IB	Ic-IC	0	0	0	0	0	0
01	01	01	00	00	11	11	00	00	Ia-IC	Ib	Ic-IB	0	0	0	0	0	0
01	01	01	00	00	11	00	11	00	Ia	Ib-IC	Ic-IB	0	0	0	0	0	0
01	01	01	00	00	11	00	00	11	Ia	Ib	IA+Ic	0	0	0	0	0	0
11	00	11	10	10	00	10	00	00	0	0	0	Ib-IB	-Ib	0	-IC	0	0
00	11	11	10	10	00	10	00	00	0	0	0	IC-Ia	Ia+IA	0	-IC	0	0
11	00	11	10	10	00	00	10	00	0	0	0	Ib+IA	IC-Ib	0	0	-IC	0
00	11	11	10	10	00	00	10	00	0	0	0	-Ia	Ia-IB	0	0	-IC	0
11	00	11	10	10	00	00	00	10	0	0	0	Ib-IB	-Ib	0	0	0	-IC
00	11	11	10	10	00	00	00	10	0	0	0	-Ia	Ia-IB	0	0	0	-IC
11	11	00	10	00	10	10	00	00	0	0	0	Ic-IB	0	-Ic	-IC	0	0
00	11	11	10	00	10	10	00	00	0	0	0	IC-Ia	0	Ia+IA	-IC	0	0
11	11	00	10	00	10	00	10	00	0	0	0	Ic-IB	0	-Ic	0	-IC	0
00	11	11	10	00	10	00	10	00	0	0	0	-Ia	0	Ia-IB	0	-IC	0
11	11	00	10	00	10	00	00	10	0	0	0	Ic+IA	0	IC-Ic	0	0	-IC
00	11	11	10	00	10	00	00	10	0	0	0	-Ia	0	Ia-IB	0	0	-IC
11	00	11	10	00	00	10	10	00	0	0	0	-IB	0	0	Ib-IC	-Ib	0
00	11	11	10	00	00	10	10	00	0	0	0	-IB	0	0	IB-Ia	Ia+IA	0
11	11	00	10	00	00	10	00	10	0	0	0	-IB	0	0	Ic-IC	0	-Ic
00	11	11	10	00	00	10	00	10	0	0	0	-IB	0	0	IB-Ia	0	Ia+IA
11	11	00	10	00	00	00	10	10	0	0	0	-IB	0	0	0	Ic-IC	-Ic
11	00	11	10	00	00	00	10	10	0	0	0	-IB	0	0	0	-Ib	Ib-IC
11	11	00	00	10	10	10	00	00	0	0	0	0	Ic-IB	-Ic	-IC	0	0
11	00	11	00	10	10	10	00	00	0	0	0	0	-Ib	Ib-IB	-IC	0	0
11	11	00	00	10	10	00	10	00	0	0	0	0	Ic-IB	-Ic	0	-IC	0
11	00	11	00	10	10	00	10	00	0	0	0	0	IC-Ib	Ib+IA	0	-IC	0
11	11	00	00	10	10	00	00	10	0	0	0	0	Ic+IA	IC-Ic	0	0	-IC
11	00	11	00	10	10	00	00	10	0	0	0	0	-Ib	Ib-IB	0	0	-IC
11	00	11	00	10	00	10	10	00	0	0	0	0	-IB	0	Ib+IA	IB-Ib	0
00	11	11	00	10	00	10	10	00	0	0	0	0	-IB	0	-Ia	Ia-IC	0
11	11	00	00	10	00	10	00	10	0	0	0	0	-IB	0	Ic-IC	0	-Ic
00	11	11	00	10	00	10	00	10	0	0	0	0	-IB	0	-Ia	0	Ia-IC
11	11	00	00	10	00	00	10	10	0	0	0	0	-IB	0	0	Ic-IC	-Ic
11	00	11	00	10	00	00	10	10	0	0	0	0	-IB	0	0	IB-Ib	Ib+IA
11	00	11	00	00	10	10	10	00	0	0	0	0	0	-IB	Ib-IC	-Ib	0
00	11	11	00	00	10	10	10	00	0	0	0	0	0	-IB	-Ia	Ia-IC	0
11	11	00	00	00	10	10	00	10	0	0	0	0	0	-IB	Ic+IA	0	IB-Ic
00	11	11	00	00	10	10	00	10	0	0	0	0	0	-IB	-Ia	0	Ia-IC
11	11	00	00	00	10	00	10	10	0	0	0	0	0	-IB	0	Ic+IA	IB-Ic
11	00	11	00	00	10	00	10	10	0	0	0	0	0	-IB	0	-Ib	Ib-IC
employ four capacitors																	
11	00	00	10	10	10	10	00	00	0	0	0	-Ia-IB	-Ib	-Ic	-IC	0	0
00	11	00	10	10	10	10	00	00	0	0	0	IC-Ia	IA-Ib	-Ic	-IC	0	0

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
00	00	11	10	10	10	10	00	00	0	0	0	IC-Ia	-Ib	IA-Ic	-IC	0	0
11	00	00	10	10	10	00	10	00	0	0	0	IA-Ia	IC-Ib	-Ic	0	-IC	0
00	11	00	10	10	10	00	10	00	0	0	0	-Ia	-Ib-IB	-Ic	0	-IC	0
00	00	11	10	10	10	00	10	00	0	0	0	-Ia	IC-Ib	IA-Ic	0	-IC	0
11	00	00	10	10	10	00	00	10	0	0	0	IA-Ia	-Ib	IC-Ic	0	0	-IC
00	11	00	10	10	10	00	00	10	0	0	0	-Ia	IA-Ib	IC-Ic	0	0	-IC
00	00	11	10	10	10	00	00	10	0	0	0	-Ia	-Ib	-Ic-IB	0	0	-IC
11	00	00	10	10	00	10	00	10	0	0	0	Ib-IB	-Ib	0	Ic-IC	0	-Ic
00	11	00	10	10	00	10	00	10	0	0	0	Ib+IC	IA-Ib	0	Ic-IC	0	-Ic
00	00	11	10	10	00	10	00	10	0	0	0	Ib-IB	-Ib	0	IB+Ic	0	IA-Ic
11	00	00	10	10	00	00	10	10	0	0	0	IA-Ia	Ia+IC	0	0	Ic-IC	-Ic
00	11	00	10	10	00	00	10	10	0	0	0	-Ia	Ia-IB	0	0	Ic-IC	-Ic
00	00	11	10	10	00	00	10	10	0	0	0	-Ia	Ia-IB	0	0	IB+Ic	IA-Ic
11	00	00	10	00	10	10	10	00	0	0	0	Ic-IB	0	-Ic	Ib-IC	-Ib	0
00	00	11	10	00	10	10	10	00	0	0	0	Ic+IC	0	IA-Ic	Ib-IC	-Ib	0
00	11	00	10	00	10	10	10	00	0	0	0	Ic-IB	0	-Ic	IB+Ib	0	IA-Ib
11	00	00	10	00	10	00	10	10	0	0	0	IA-Ia	0	Ia+IC	0	-Ib	Ib-IC
00	11	00	10	00	10	00	10	10	0	0	0	-Ia	0	Ia-IB	0	IA-Ib	IB+Ib
00	00	11	10	00	10	00	10	10	0	0	0	-Ia	0	Ia-IB	0	-Ib	Ib-IC
11	00	00	10	00	00	10	10	10	0	0	0	-IB	0	0	-Ia-IC	-Ib	-Ic
00	11	00	10	00	00	10	10	10	0	0	0	-IB	0	0	IB-Ia	IA-Ib	-Ic
00	00	11	10	00	00	10	10	10	0	0	0	-IB	0	0	IB-Ia	-Ib	IA-Ic
11	00	00	00	10	10	10	10	00	0	0	0	0	Ic-IB	-Ic	IA-Ia	Ia+IB	0
00	11	00	00	10	10	10	10	00	0	0	0	0	Ic-IB	-Ic	-Ia	Ia-IC	0
00	00	11	00	10	10	10	10	00	0	0	0	0	Ic+IC	IA-Ic	-Ia	Ia-IC	0
11	00	00	00	10	10	10	00	10	0	0	0	0	-Ib	Ib-IB	IA-Ia	0	Ia+IB
00	11	00	00	10	10	10	00	10	0	0	0	0	IA-Ib	Ib+IC	-Ia	0	Ia-IC
00	00	11	00	10	10	10	00	10	0	0	0	0	-Ib	Ib-IB	-Ia	0	Ia-IC
11	00	00	00	10	00	10	10	10	0	0	0	0	-IB	0	IA-Ia	IB-Ib	-Ic
00	11	00	00	10	00	10	10	10	0	0	0	0	-IB	0	-Ia	-IC-Ib	-Ic
00	00	11	00	10	00	10	10	10	0	0	0	0	-IB	0	-Ia	IB-Ib	IA-Ic
11	00	00	00	00	10	10	10	10	0	0	0	0	0	-IB	IA-Ia	-Ib	IB-Ic
00	11	00	00	00	10	10	10	10	0	0	0	0	0	-IB	-Ia	IA-Ib	IB-Ic
00	00	11	00	00	10	10	10	10	0	0	0	0	0	-IB	-Ia	-Ib	-IC-Ic

Table B.8: Switching device combinations for (V_{AB},V_{BC},V_{CA}) = ($+V_{cap}$,0,$-V_{cap}$) and (V_{ab},V_{bc},V_{ca}) = ($+V_{cap}$,0,$-V_{cap}$).

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
employ single capacitor																	
11	01	00	00	11	00	00	11	11	0	IA-Ia	0	0	0	0	0	0	0
11	01	00	00	00	11	00	11	11	0	IA-Ia	0	0	0	0	0	0	0
11	01	00	00	11	11	00	11	00	0	IA-Ia	0	0	0	0	0	0	0
11	01	00	00	11	11	00	00	11	0	IA-Ia	0	0	0	0	0	0	0
11	00	01	00	11	00	00	11	11	0	0	IA-Ia	0	0	0	0	0	0
11	00	01	00	00	11	00	11	11	0	0	IA-Ia	0	0	0	0	0	0
11	00	01	00	11	11	00	11	00	0	0	IA-Ia	0	0	0	0	0	0
11	00	01	00	11	11	00	00	11	0	0	IA-Ia	0	0	0	0	0	0
11	00	00	10	11	00	00	11	11	0	0	0	IA-Ia	0	0	0	0	0
11	00	00	10	00	11	00	11	11	0	0	0	IA-Ia	0	0	0	0	0
11	00	00	10	11	11	00	11	00	0	0	0	IA-Ia	0	0	0	0	0
11	00	00	10	11	11	00	00	11	0	0	0	IA-Ia	0	0	0	0	0
11	00	00	00	11	00	10	11	11	0	0	0	0	0	0	IA-Ia	0	0
11	00	00	00	00	11	10	11	11	0	0	0	0	0	0	IA-Ia	0	0
11	00	00	00	11	11	10	11	00	0	0	0	0	0	0	IA-Ia	0	0
11	00	00	00	11	11	10	00	11	0	0	0	0	0	0	IA-Ia	0	0
employ two capacitors																	
11	01	01	00	11	00	00	11	00	0	Ib+IA	Ic	0	0	0	0	0	0
11	01	01	00	11	00	00	00	11	0	Ib-IB	Ic-IC	0	0	0	0	0	0
11	01	01	00	00	11	00	11	00	0	Ib-IC	Ic-IB	0	0	0	0	0	0
11	01	01	00	00	11	00	00	11	0	Ib	IA+Ic	0	0	0	0	0	0
00	01	00	10	11	00	00	11	11	0	IA	0	-Ia	0	0	0	0	0
00	01	00	10	00	11	00	11	11	0	IA	0	-Ia	0	0	0	0	0
11	01	00	10	00	00	00	11	11	0	-Ia-IC	0	-IB	0	0	0	0	0
00	01	00	10	11	11	00	11	00	0	IA	0	-Ia	0	0	0	0	0
00	01	00	10	11	11	00	00	11	0	IA	0	-Ia	0	0	0	0	0
11	01	00	10	00	11	00	11	00	0	Ib-IC	0	Ic-IB	0	0	0	0	0
11	01	00	10	00	11	00	00	11	0	Ib	0	IA+Ic	0	0	0	0	0
00	01	00	00	11	00	10	11	11	0	IA	0	0	0	0	-Ia	0	0
00	01	00	00	00	11	10	11	11	0	IA	0	0	0	0	-Ia	0	0
00	01	00	00	11	11	10	11	00	0	IA	0	0	0	0	-Ia	0	0
00	01	00	00	11	11	10	00	11	0	IA	0	0	0	0	-Ia	0	0
11	01	00	00	11	00	10	00	11	0	Ib-IB	0	0	0	0	Ic-IC	0	0
11	01	00	00	00	11	10	00	11	0	Ib	0	0	0	0	IA+Ic	0	0
11	01	00	00	11	11	10	00	00	0	-Ia-IB	0	0	0	0	-IC	0	0
00	00	01	10	11	00	00	11	11	0	0	IA	-Ia	0	0	0	0	0
00	00	01	10	00	11	00	11	11	0	0	IA	-Ia	0	0	0	0	0
11	00	01	10	00	00	00	11	11	0	0	-Ia-IC	-IB	0	0	0	0	0
00	00	01	10	11	11	00	11	00	0	0	IA	-Ia	0	0	0	0	0
00	00	01	10	11	11	00	00	11	0	0	IA	-Ia	0	0	0	0	0
11	00	01	10	11	00	00	11	00	0	0	Ic	IA+Ib	0	0	0	0	0

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
11	00	01	10	11	00	00	00	11	0	0	Ic-IC	Ib-IB	0	0	0	0	0
00	00	01	00	11	00	10	11	11	0	0	IA	0	0	0	-Ia	0	0
00	00	01	00	00	11	10	11	11	0	0	IA	0	0	0	-Ia	0	0
00	00	01	00	11	11	10	11	00	0	0	IA	0	0	0	-Ia	0	0
00	00	01	00	11	11	10	00	11	0	0	IA	0	0	0	-Ia	0	0
11	00	01	00	11	00	10	11	00	0	0	Ic	0	0	0	IA+Ib	0	0
11	00	01	00	00	11	10	11	00	0	0	Ic-IB	0	0	0	Ib-IC	0	0
11	00	01	00	11	11	10	00	00	0	0	-Ia-IB	0	0	0	-IC	0	0
11	00	00	10	00	00	10	11	11	0	0	0	-IB	0	0	-IC-Ia	0	0
11	00	00	10	11	00	10	00	11	0	0	0	Ib-IB	0	0	Ic-IC	0	0
11	00	00	10	00	11	10	11	00	0	0	0	Ic-IB	0	0	Ib-IC	0	0
11	00	00	10	11	11	10	00	00	0	0	0	-IB-Ia	0	0	-IC	0	0
employ three capacitors																	
11	01	01	10	00	00	00	11	00	0	Ib-IC	Ic	-IB	0	0	0	0	0
11	01	01	10	00	00	00	00	11	0	Ib	Ic-IC	-IB	0	0	0	0	0
00	01	01	10	11	00	00	11	00	0	IA-Ic	Ic	-Ia	0	0	0	0	0
00	01	01	10	00	11	00	11	00	0	Ib-IC	-Ib-IB	-Ia	0	0	0	0	0
00	01	01	10	11	00	00	00	11	0	-Ic-IB	Ic-IC	-Ia	0	0	0	0	0
00	01	01	10	00	11	00	00	11	0	Ib	IA-Ib	-Ia	0	0	0	0	0
11	01	01	00	11	00	10	00	00	0	Ib-IB	Ic	0	0	0	-IC	0	0
11	01	01	00	00	11	10	00	00	0	Ib	Ic-IB	0	0	0	-IC	0	0
00	01	01	00	11	00	10	11	00	0	IA-Ic	Ic	0	0	0	-Ia	0	0
00	01	01	00	11	00	10	00	11	0	Ib-IB	-Ib-IC	0	0	0	-Ia	0	0
00	01	01	00	00	11	10	11	00	0	-Ic-IC	Ic-IB	0	0	0	-Ia	0	0
00	01	01	00	00	11	10	00	11	0	Ib	IA-Ib	0	0	0	-Ia	0	0
00	01	00	10	00	00	10	11	11	0	IA	0	-IB	0	0	IB-Ia	0	0
00	01	00	10	11	00	10	00	11	0	IA	0	IC+Ib	0	0	Ic-IC	0	0
00	01	00	10	00	11	10	11	00	0	IA	0	Ic-IB	0	0	IB+Ib	0	0
11	01	00	10	00	00	10	00	11	0	Ib	0	-IB	0	0	Ic-IC	0	0
00	01	00	10	11	11	10	00	00	0	IA	0	IC-Ia	0	0	-IC	0	0
11	01	00	10	00	11	10	00	00	0	Ib	0	Ic-IB	0	0	-IC	0	0
00	00	01	10	00	00	10	11	11	0	0	IA	-IB	0	0	IB-Ia	0	0
00	00	01	10	11	00	10	00	11	0	0	IA	Ib-IB	0	0	IB+Ic	0	0
00	00	01	10	00	11	10	11	00	0	0	IA	Ic+IC	0	0	Ib-IC	0	0
11	00	01	10	00	00	10	11	00	0	0	Ic	-IB	0	0	Ib-IC	0	0
00	00	01	10	11	11	10	00	00	0	0	IA	IC-Ia	0	0	-IC	0	0
11	00	01	10	11	00	10	00	00	0	0	Ic	Ib-IB	0	0	-IC	0	0
employ four capacitors																	
11	01	01	10	00	00	10	00	00	0	Ib	Ic	-IB	0	0	-IC	0	0
00	01	01	10	00	00	10	11	00	0	IA-Ic	Ic	-IB	0	0	IB-Ia	0	0
00	01	01	10	00	00	10	00	11	0	Ib	IA-Ib	-IB	0	0	IB-Ia	0	0
00	01	01	10	11	00	10	00	00	0	IA-Ic	Ic	IC-Ia	0	0	-IC	0	0
00	01	01	10	00	11	10	00	00	0	Ib	IA-Ib	IC-Ia	0	0	-IC	0	0

Table B.9: Switching device combinations for (V_{AB},V_{BC},V_{CA}) = ($+V_{cap}$,0,$-V_{cap}$) and (V_{ab},V_{bc},V_{ca}) = (0,$+V_{cap}$,$-V_{cap}$).

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
employ single capacitor																	
11	11	01	00	00	11	00	00	11	0	0	IA+Ic	0	0	0	0	0	0
11	11	00	10	00	11	00	00	11	0	0	0	IA+Ic	0	0	0	0	0
11	11	00	00	10	11	00	00	11	0	0	0	0	IA+Ic	0	0	0	0
11	11	00	00	00	11	10	00	11	0	0	0	0	0	0	IA+Ic	0	0
11	11	00	00	00	11	00	10	11	0	0	0	0	0	0	0	IA+Ic	0
employ two capacitors																	
11	11	01	10	00	00	00	00	11	0	0	Ic-IC	-IB	0	0	0	0	0
00	11	01	10	00	11	00	00	11	0	0	IA-Ib	-Ia	0	0	0	0	0
11	11	01	00	10	00	00	00	11	0	0	Ic-IC	0	-IB	0	0	0	0
11	00	01	00	10	11	00	00	11	0	0	IA-Ia	0	-Ib	0	0	0	0
11	11	01	00	00	11	10	00	00	0	0	Ic-IB	0	0	0	-IC	0	0
00	11	01	00	00	11	10	00	11	0	0	IA-Ib	0	0	0	-Ia	0	0
11	11	01	00	00	11	00	10	00	0	0	Ic-IB	0	0	0	0	-IC	0
11	00	01	00	00	11	00	10	11	0	0	IA-Ia	0	0	0	0	-Ib	0
11	00	00	10	10	11	00	00	11	0	0	0	IA-Ia	-Ib	0	0	0	0
00	11	00	10	10	11	00	00	11	0	0	0	-Ia	IA-Ib	0	0	0	0
11	11	00	10	00	00	10	00	11	0	0	0	-IB	0	0	Ic-IC	0	0
11	11	00	10	00	11	10	00	00	0	0	0	Ic-IB	0	0	-IC	0	0
11	00	00	10	00	11	00	10	11	0	0	0	IA-Ia	0	0	0	-Ib	0
00	11	00	10	00	11	00	10	11	0	0	0	-Ia	0	0	0	IA-Ib	0
11	11	00	10	00	00	00	10	11	0	0	0	-IB	0	0	0	Ic-IC	0
11	11	00	10	00	11	00	10	00	0	0	0	Ic-IB	0	0	0	-IC	0
11	00	00	00	10	11	10	00	11	0	0	0	0	-Ib	0	IA-Ia	0	0
00	11	00	00	10	11	10	00	11	0	0	0	0	IA-Ib	0	-Ia	0	0
11	11	00	00	10	00	10	00	11	0	0	0	0	-IB	0	Ic-IC	0	0
11	11	00	00	10	11	10	00	00	0	0	0	0	Ic-IB	0	-IC	0	0
11	11	00	00	10	00	00	10	11	0	0	0	0	-IB	0	0	Ic-IC	0
11	11	00	00	10	11	00	10	00	0	0	0	0	Ic-IB	0	0	-IC	0
11	00	00	00	00	11	10	10	11	0	0	0	0	0	0	IA-Ia	-Ib	0
00	11	00	00	00	11	10	10	11	0	0	0	0	0	0	-Ia	IA-Ib	0
employ three capacitors																	
00	00	01	10	10	11	00	00	11	0	0	IA	-Ia	-Ib	0	0	0	0
11	00	01	10	10	00	00	00	11	0	0	Ic-IC	Ib-IB	-Ib	0	0	0	0
00	11	01	10	10	00	00	00	11	0	0	Ic-IC	-Ia	Ia-IB	0	0	0	0
11	11	01	10	00	00	10	00	00	0	0	Ic	-IB	0	0	-IC	0	0
00	11	01	10	00	00	10	00	11	0	0	IA-Ib	-IB	0	0	IB-Ia	0	0
00	11	01	10	00	11	10	00	00	0	0	IA-Ib	IC-Ia	0	0	-IC	0	0
00	00	01	10	00	11	00	10	11	0	0	IA	-Ia	0	0	0	-Ib	0
11	11	01	10	00	00	00	10	00	0	0	Ic	-IB	0	0	0	-IC	0
11	00	01	10	00	00	00	10	11	0	0	-IC-Ia	-IB	0	0	0	-Ib	0
00	11	01	10	00	11	00	10	00	0	0	-Ib-IB	-Ia	0	0	0	-IC	0

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
00	00	01	00	10	11	10	00	11	0	0	IA	0	-Ib	0	-Ia	0	0
11	11	01	00	10	00	10	00	00	0	0	Ic	0	-IB	0	-IC	0	0
00	11	01	00	10	00	10	00	11	0	0	-IC-Ib	0	-IB	0	-Ia	0	0
11	00	01	00	10	11	10	00	00	0	0	-Ia-IB	0	-Ib	0	-IC	0	0
11	11	01	00	10	00	00	10	00	0	0	Ic	0	-IB	0	0	-IC	0
11	00	01	00	10	00	00	10	11	0	0	IA-Ia	0	-IB	0	0	IB-Ib	0
11	00	01	00	10	11	00	10	00	0	0	IA-Ia	0	IC-Ib	0	0	-IC	0
00	00	01	00	00	11	10	10	11	0	0	IA	0	0	0	-Ia	-Ib	0
11	00	01	00	00	11	10	10	00	0	0	Ic-IB	0	0	0	Ib-IC	-Ib	0
00	11	01	00	00	11	10	10	00	0	0	Ic-IB	0	0	0	-Ia	Ia-IC	0
11	00	00	10	10	00	10	00	11	0	0	0	Ib-IB	-Ib	0	Ic-IC	0	0
00	11	00	10	10	00	10	00	11	0	0	0	Ib+IC	IA-Ib	0	Ic-IC	0	0
11	00	00	10	10	11	10	00	00	0	0	0	-IB-Ia	-Ib	0	-IC	0	0
00	11	00	10	10	11	10	00	00	0	0	0	IC-Ia	IA-Ib	0	-IC	0	0
11	00	00	10	10	00	00	10	11	0	0	0	IA-Ia	Ia+IC	0	0	Ic-IC	0
00	11	00	10	10	00	00	10	11	0	0	0	-Ia	Ia-IB	0	0	Ic-IC	0
11	00	00	10	10	11	00	10	00	0	0	0	IA-Ia	IC-Ib	0	0	-IC	0
00	11	00	10	10	11	00	10	00	0	0	0	-Ia	-IB-Ib	0	0	-IC	0
11	00	00	10	00	00	10	10	11	0	0	0	-IB	0	0	-Ia-IC	-Ib	0
00	11	00	10	00	00	10	10	11	0	0	0	-IB	0	0	IB-Ia	IA-Ib	0
11	00	00	10	00	11	10	10	00	0	0	0	Ic-IB	0	0	Ib-IC	-Ib	0
00	11	00	10	00	11	10	10	00	0	0	0	Ic-IB	0	0	IB+Ib	IA-Ib	0
11	00	00	00	10	00	10	10	11	0	0	0	0	-IB	0	IA-Ia	IB-Ib	0
00	11	00	00	10	00	10	10	11	0	0	0	0	-IB	0	-Ia	-IC-Ib	0
11	00	00	00	10	11	10	10	00	0	0	0	0	Ic-IB	0	IA-Ia	Ia+IB	0
00	11	00	00	10	11	10	10	00	0	0	0	0	Ic-IB	0	-Ia	Ia-IC	0
employ four capacitors																	
00	00	01	10	10	00	10	00	11	0	0	IA	Ib-IB	-Ib	0	IB+Ic	0	0
00	00	01	10	10	11	10	00	00	0	0	IA	IC-Ia	-Ib	0	-IC	0	0
11	00	01	10	10	00	10	00	00	0	0	Ic	Ib-IB	-Ib	0	-IC	0	0
00	11	01	10	10	00	10	00	00	0	0	Ic	IC-Ia	Ia+IA	0	-IC	0	0
00	00	01	10	10	00	00	10	11	0	0	IA	-Ia	Ia-IB	0	0	IB+Ic	0
00	00	01	10	10	11	00	10	00	0	0	IA	-Ia	IC-Ib	0	0	-IC	0
11	00	01	10	10	00	00	10	00	0	0	Ic	Ib+IA	IC-Ib	0	0	-IC	0
00	11	01	10	10	00	00	10	00	0	0	Ic	-Ia	Ia-IB	0	0	-IC	0
00	00	01	10	00	00	10	10	11	0	0	IA	-IB	0	0	IB-Ia	-Ib	0
00	00	01	10	00	11	10	10	00	0	0	IA	IC+Ic	0	0	Ib-IC	-Ib	0
11	00	01	10	00	00	10	10	00	0	0	Ic	-IB	0	0	Ib-IC	-Ib	0
00	11	01	10	00	00	10	10	00	0	0	Ic	-IB	0	0	IB-Ia	Ia+IA	0
00	00	01	00	10	00	10	10	11	0	0	IA	0	-IB	0	-Ia	IB-Ib	0
00	00	01	00	10	11	10	10	00	0	0	IA	0	IC+Ic	0	-Ia	Ia-IC	0
11	00	01	00	10	00	10	10	00	0	0	Ic	0	-IB	0	Ib+IA	IB-Ib	0
00	11	01	00	10	00	10	10	00	0	0	Ic	0	-IB	0	-Ia	Ia-IC	0

Table B.10: Switching device combinations for (V_{AB},V_{BC},V_{CA}) = ($+V_{cap}$,0,$-V_{cap}$) and (V_{ab},V_{bc},V_{ca}) = ($-V_{cap}$,$+V_{cap}$,0).

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
employ single capacitor																	
01	11	00	11	00	00	11	00	11	IA-Ib	0	0	0	0	0	0	0	0
01	11	00	00	00	11	11	00	11	IA-Ib	0	0	0	0	0	0	0	0
01	11	00	11	00	11	11	00	00	IA-Ib	0	0	0	0	0	0	0	0
01	11	00	11	00	11	00	00	11	IA-Ib	0	0	0	0	0	0	0	0
00	11	01	11	00	00	11	00	11	0	0	IA-Ib	0	0	0	0	0	0
00	11	01	00	00	11	11	00	11	0	0	IA-Ib	0	0	0	0	0	0
00	11	01	11	00	11	11	00	00	0	0	IA-Ib	0	0	0	0	0	0
00	11	01	11	00	11	00	00	11	0	0	IA-Ib	0	0	0	0	0	0
00	11	00	11	10	00	11	00	11	0	0	0	0	IA-Ib	0	0	0	0
00	11	00	00	10	11	11	00	11	0	0	0	0	IA-Ib	0	0	0	0
00	11	00	11	10	11	11	00	00	0	0	0	0	IA-Ib	0	0	0	0
00	11	00	11	10	11	00	00	11	0	0	0	0	IA-Ib	0	0	0	0
00	11	00	11	00	00	11	10	11	0	0	0	0	0	0	0	IA-Ib	0
00	11	00	00	00	11	11	10	11	0	0	0	0	0	0	0	IA-Ib	0
00	11	00	11	00	11	11	10	00	0	0	0	0	0	0	0	IA-Ib	0
00	11	00	11	00	11	00	10	11	0	0	0	0	0	0	0	IA-Ib	0
employ two capacitors																	
01	11	01	11	00	00	11	00	00	Ia+IA	0	Ic	0	0	0	0	0	0
01	11	01	11	00	00	00	00	11	Ia-IB	0	Ic-IC	0	0	0	0	0	0
01	11	01	00	00	11	11	00	00	Ia-IC	0	Ic-IB	0	0	0	0	0	0
01	11	01	00	00	11	00	00	11	Ia	0	IA+Ic	0	0	0	0	0	0
01	00	00	11	10	00	11	00	11	IA	0	0	0	-Ib	0	0	0	0
01	00	00	00	10	11	11	00	11	IA	0	0	0	-Ib	0	0	0	0
01	11	00	00	10	00	11	00	11	-Ib-IC	0	0	0	-IB	0	0	0	0
01	00	00	11	10	11	11	00	00	IA	0	0	0	-Ib	0	0	0	0
01	00	00	11	10	11	00	00	11	IA	0	0	0	-Ib	0	0	0	0
01	11	00	00	10	11	11	00	00	Ia-IC	0	0	0	Ic-IB	0	0	0	0
01	11	00	00	10	11	00	00	11	Ia	0	0	0	IA+Ic	0	0	0	0
01	00	00	11	00	00	11	10	11	IA	0	0	0	0	0	0	-Ib	0
01	00	00	00	00	11	11	10	11	IA	0	0	0	0	0	0	-Ib	0
01	00	00	11	00	11	11	10	00	IA	0	0	0	0	0	0	-Ib	0
01	00	00	11	00	11	00	10	11	IA	0	0	0	0	0	0	-Ib	0
01	11	00	11	00	00	00	10	11	Ia-IB	0	0	0	0	0	0	Ic-IC	0
01	11	00	00	00	11	00	10	11	Ia	0	0	0	0	0	0	IA+Ic	0
01	11	00	11	00	11	00	10	00	-Ib-IB	0	0	0	0	0	0	-IC	0
00	00	01	11	10	00	11	00	11	0	0	IA	0	-Ib	0	0	0	0
00	00	01	00	10	11	11	00	11	0	0	IA	0	-Ib	0	0	0	0
00	11	01	00	10	00	11	00	11	0	0	-IC-Ib	0	-IB	0	0	0	0
00	00	01	11	10	11	11	00	00	0	0	IA	0	-Ib	0	0	0	0
00	00	01	11	10	11	00	00	11	0	0	IA	0	-Ib	0	0	0	0
00	11	01	11	10	00	11	00	00	0	0	Ic	0	IA+Ia	0	0	0	0

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
00	11	01	11	10	00	00	00	11	0	0	Ic-IC	0	Ia-IB	0	0	0	0
00	00	01	11	00	00	11	10	11	0	0	IA	0	0	0	0	-Ib	0
00	00	01	00	00	11	11	10	11	0	0	IA	0	0	0	0	-Ib	0
00	00	01	11	00	11	11	10	00	0	0	IA	0	0	0	0	-Ib	0
00	00	01	11	00	11	00	10	11	0	0	IA	0	0	0	0	-Ib	0
00	11	01	11	00	00	11	10	00	0	0	Ic	0	0	0	0	IA+Ia	0
00	11	01	00	00	11	11	10	00	0	0	Ic-IB	0	0	0	0	Ia-IC	0
00	11	01	11	00	11	00	10	00	0	0	-IB-Ib	0	0	0	0	-IC	0
00	11	00	00	10	00	11	10	11	0	0	0	0	-IB	0	0	-IC-Ib	0
00	11	00	11	10	00	00	10	11	0	0	0	0	Ia-IB	0	0	Ic-IC	0
00	11	00	00	10	11	11	10	00	0	0	0	0	Ic-IB	0	0	Ia-IC	0
00	11	00	11	10	11	00	10	00	0	0	0	0	-Ib-IB	0	0	-IC	0
employ three capacitors																	
01	11	01	00	10	00	11	00	00	Ia-IC	0	Ic	0	-IB	0	0	0	0
01	11	01	00	10	00	00	00	11	Ia	0	Ic-IC	0	-IB	0	0	0	0
01	00	01	11	10	00	11	00	00	IA-Ic	0	Ic	0	-Ib	0	0	0	0
01	00	01	00	10	11	11	00	00	Ia-IC	0	-Ia-IB	0	-Ib	0	0	0	0
01	00	01	11	10	00	00	00	11	-Ic-IB	0	Ic-IC	0	-Ib	0	0	0	0
01	00	01	00	10	11	00	00	11	Ia	0	IA-Ia	0	-Ib	0	0	0	0
01	11	01	11	00	00	00	10	00	Ia-IB	0	Ic	0	0	0	0	-IC	0
01	11	01	00	00	11	00	10	00	Ia	0	Ic-IB	0	0	0	0	-IC	0
01	00	01	11	00	00	11	10	00	IA-Ic	0	Ic	0	0	0	0	-Ib	0
01	00	01	11	00	00	00	10	11	Ia-IB	0	-Ia-IC	0	0	0	0	-Ib	0
01	00	01	00	00	11	11	10	00	-Ic-IC	0	Ic-IB	0	0	0	0	-Ib	0
01	00	01	00	00	11	00	10	11	Ia	0	IA-Ia	0	0	0	0	-Ib	0
01	00	00	00	10	00	11	10	11	IA	0	0	0	-IB	0	0	IB-Ib	0
01	00	00	11	10	00	00	10	11	IA	0	0	0	IC+Ia	0	0	Ic-IC	0
01	00	00	00	10	11	11	10	00	IA	0	0	0	Ic-IB	0	0	IB+Ia	0
01	11	00	00	10	00	00	10	11	Ia	0	0	0	-IB	0	0	Ic-IC	0
01	00	00	11	10	11	00	10	00	IA	0	0	0	IC-Ib	0	0	-IC	0
01	11	00	00	10	11	00	10	00	Ia	0	0	0	Ic-IB	0	0	-IC	0
00	00	01	00	10	00	11	10	11	0	0	IA	0	-IB	0	0	IB-Ib	0
00	00	01	11	10	00	00	10	11	0	0	IA	0	Ia-IB	0	0	IB+Ic	0
00	00	01	00	10	11	11	10	00	0	0	IA	0	IC+Ic	0	0	Ia-IC	0
00	11	01	00	10	00	11	10	00	0	0	Ic	0	-IB	0	0	Ia-IC	0
00	00	01	11	10	11	00	10	00	0	0	IA	0	IC-Ib	0	0	-IC	0
00	11	01	11	10	00	00	10	00	0	0	Ic	0	Ia-IB	0	0	-IC	0
employ four capacitors																	
01	11	01	00	10	00	00	10	00	Ia	0	Ic	0	-IB	0	0	-IC	0
01	00	01	00	10	00	11	10	00	IA-Ic	0	Ic	0	-IB	0	0	IB-Ib	0
01	00	01	00	10	00	00	10	11	Ia	0	IA-Ia	0	-IB	0	0	IB-Ib	0
01	00	01	11	10	00	00	10	00	IA-Ic	0	Ic	0	IC-Ib	0	0	-IC	0
01	00	01	00	10	11	00	10	00	Ia	0	IA-Ia	0	IC-Ib	0	0	-IC	0

Table B.11: Switching device combinations for (V_{AB},V_{BC},V_{CA}) = ($+V_{cap}$,0,$-V_{cap}$) and (V_{ab},V_{bc},V_{ca}) = ($-V_{cap}$,0,$+V_{cap}$).

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
employ single capacitor																	
01	11	11	11	00	00	11	00	00	IA+Ia	0	0	0	0	0	0	0	0
00	11	11	11	10	00	11	00	00	0	0	0	0	IA+Ia	0	0	0	0
00	11	11	11	00	10	11	00	00	0	0	0	0	0	IA+Ia	0	0	0
00	11	11	11	00	00	11	10	00	0	0	0	0	0	0	0	IA+Ia	0
00	11	11	11	00	00	11	00	10	0	0	0	0	0	0	0	0	IA+Ia
employ two capacitors																	
01	11	11	00	10	00	11	00	00	Ia-IC	0	0	0	-IB	0	0	0	0
01	00	11	11	10	00	11	00	00	IA-Ic	0	0	0	-Ib	0	0	0	0
01	11	11	00	00	10	11	00	00	Ia-IC	0	0	0	0	-IB	0	0	0
01	11	00	11	00	10	11	00	00	IA-Ib	0	0	0	0	-Ic	0	0	0
01	11	11	11	00	00	00	10	00	Ia-IB	0	0	0	0	0	0	-IC	0
01	00	11	11	00	00	11	10	00	IA-Ic	0	0	0	0	0	0	-Ib	0
01	11	11	11	00	00	00	00	10	Ia-IB	0	0	0	0	0	0	0	-IC
01	11	00	11	00	00	11	00	10	IA-Ib	0	0	0	0	0	0	0	-Ic
00	11	00	11	10	10	11	00	00	0	0	0	0	IA-Ib	-Ic	0	0	0
00	00	11	11	10	10	11	00	00	0	0	0	0	-Ib	IA-Ic	0	0	0
00	11	11	00	10	00	11	10	00	0	0	0	0	-IB	0	0	Ia-IC	0
00	11	11	11	10	00	00	10	00	0	0	0	0	Ia-IB	0	0	-IC	0
00	11	00	11	10	00	11	00	10	0	0	0	0	IA-Ib	0	0	0	-Ic
00	00	11	11	10	00	11	00	10	0	0	0	0	-Ib	0	0	0	IA-Ic
00	11	11	00	10	00	11	00	10	0	0	0	0	-IB	0	0	0	Ia-IC
00	11	11	11	10	00	00	00	10	0	0	0	0	Ia-IB	0	0	0	-IC
00	11	00	11	00	10	11	10	00	0	0	0	0	0	-Ic	0	IA-Ib	0
00	00	11	11	00	10	11	10	00	0	0	0	0	0	IA-Ic	0	-Ib	0
00	11	11	00	00	10	11	10	00	0	0	0	0	0	-IB	0	Ia-IC	0
00	11	11	11	00	10	00	10	00	0	0	0	0	0	Ia-IB	0	-IC	0
00	11	11	00	00	10	11	00	10	0	0	0	0	0	-IB	0	0	Ia-IC
00	11	11	11	00	10	00	00	10	0	0	0	0	0	Ia-IB	0	0	-IC
00	11	00	11	00	00	11	10	10	0	0	0	0	0	0	0	IA-Ib	-Ic
00	00	11	11	00	00	11	10	10	0	0	0	0	0	0	0	-Ib	IA-Ic
employ three capacitors																	
01	00	00	11	10	10	11	00	00	IA	0	0	0	-Ib	-Ic	0	0	0
01	11	00	00	10	10	11	00	00	Ia-IC	0	0	0	Ic-IB	-Ic	0	0	0
01	00	11	00	10	10	11	00	00	Ia-IC	0	0	0	-Ib	Ib-IB	0	0	0
01	11	11	00	10	00	00	10	00	Ia	0	0	0	-IB	0	0	-IC	0
01	00	11	00	10	00	11	10	00	IA-Ic	0	0	0	-IB	0	0	IB-Ib	0
01	00	11	11	10	00	00	10	00	IA-Ic	0	0	0	IC-Ib	0	0	-IC	0
01	00	00	11	10	00	11	00	10	IA	0	0	0	-Ib	0	0	0	-Ic
01	11	11	00	10	00	00	00	10	Ia	0	0	0	-IB	0	0	0	-IC
01	11	00	00	10	00	11	00	10	-Ib-IC	0	0	0	-IB	0	0	0	-Ic
01	00	11	11	10	00	00	00	10	-Ic-IB	0	0	0	-Ib	0	0	0	-IC

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
01	00	00	11	00	10	11	10	00	IA	0	0	0	0	-Ic	0	-Ib	0
01	11	11	00	00	10	00	10	00	Ia	0	0	0	0	-IB	0	-IC	0
01	00	11	00	00	10	11	10	00	-Ic-IC	0	0	0	0	-IB	0	-Ib	0
01	11	00	11	00	10	00	10	00	-Ib-IB	0	0	0	0	-Ic	0	-IC	0
01	11	11	00	00	10	00	00	10	Ia	0	0	0	0	-IB	0	0	-IC
01	11	00	00	00	10	11	00	10	IA-Ib	0	0	0	0	-IB	0	0	IB-Ic
01	11	00	11	00	10	00	00	10	IA-Ib	0	0	0	0	IC-Ic	0	0	-IC
01	00	00	11	00	00	11	10	10	IA	0	0	0	0	0	0	-Ib	-Ic
01	11	00	11	00	00	00	10	10	Ia-IB	0	0	0	0	0	0	Ic-IC	-Ic
01	00	11	11	00	00	00	10	10	Ia-IB	0	0	0	0	0	0	-Ib	Ib-IC
00	11	00	00	10	10	11	10	00	0	0	0	0	Ic-IB	-Ic	0	Ia-IC	0
00	00	11	00	10	10	11	10	00	0	0	0	0	IC+Ic	IA-Ic	0	Ia-IC	0
00	11	00	11	10	10	00	10	00	0	0	0	0	-Ib-IB	-Ic	0	-IC	0
00	00	11	11	10	10	00	10	00	0	0	0	0	IC-Ib	IA-Ic	0	-IC	0
00	11	00	00	10	10	11	00	10	0	0	0	0	IA-Ib	Ib+IC	0	0	Ia-IC
00	00	11	00	10	10	11	00	10	0	0	0	0	-Ib	Ib-IB	0	0	Ia-IC
00	11	00	11	10	10	00	00	10	0	0	0	0	IA-Ib	IC-Ic	0	0	-IC
00	00	11	11	10	10	00	00	10	0	0	0	0	-Ib	-Ic-IB	0	0	-IC
00	11	00	00	10	00	11	10	10	0	0	0	0	-IB	0	0	-IC-Ib	-Ic
00	00	11	00	10	00	11	10	10	0	0	0	0	-IB	0	0	IB-Ib	IA-Ic
00	11	00	11	10	00	00	10	10	0	0	0	0	Ia-IB	0	0	Ic-IC	-Ic
00	00	11	11	10	00	00	10	10	0	0	0	0	Ia-IB	0	0	IB+Ic	IA-Ic
00	11	00	00	00	10	11	10	10	0	0	0	0	0	-IB	0	IA-Ib	IB-Ic
00	00	11	00	00	10	11	10	10	0	0	0	0	0	-IB	0	-Ib	-IC-Ic
00	11	00	11	00	10	00	10	10	0	0	0	0	0	Ia-IB	0	IA-Ib	IB+Ib
00	00	11	11	00	10	00	10	10	0	0	0	0	0	Ia-IB	0	-Ib	Ib-IC
employ four capacitors																	
01	00	00	00	10	10	11	10	00	IA	0	0	0	Ic-IB	-Ic	0	IB+Ia	0
01	00	00	11	10	10	00	10	00	IA	0	0	0	IC-Ib	-Ic	0	-IC	0
01	11	00	00	10	10	00	10	00	Ia	0	0	0	Ic-IB	-Ic	0	-IC	0
01	00	11	00	10	10	00	10	00	Ia	0	0	0	IC-Ib	Ib+IA	0	-IC	0
01	00	00	11	10	10	00	00	10	IA	0	0	0	-Ib	IC-Ic	0	0	-IC
01	00	00	00	10	10	11	00	10	IA	0	0	0	-Ib	Ib-IB	0	0	IB+Ia
01	11	00	00	10	10	00	00	10	Ia	0	0	0	Ic+IA	IC-Ic	0	0	-IC
01	00	11	00	10	10	00	00	10	Ia	0	0	0	-Ib	Ib-IB	0	0	-IC
01	00	00	00	10	00	11	10	10	IA	0	0	0	-IB	0	0	IB-Ib	-Ic
01	00	00	11	10	00	00	10	10	IA	0	0	0	IC+Ia	0	0	Ic-IC	-Ic
01	11	00	00	10	00	00	10	10	Ia	0	0	0	-IB	0	0	Ic-IC	-Ic
01	00	11	00	10	00	00	10	10	Ia	0	0	0	-IB	0	0	IB-Ib	Ib+IA
01	00	00	00	00	10	11	10	10	IA	0	0	0	0	-IB	0	-Ib	IB-Ic
01	00	00	11	00	10	00	10	10	IA	0	0	0	0	IC+Ia	0	-Ib	Ib-IC
01	11	00	00	00	10	00	10	10	Ia	0	0	0	0	-IB	0	Ic+IA	IB-Ic
01	00	11	00	00	10	00	10	10	Ia	0	0	0	0	-IB	0	-Ib	Ib-IC

Table B.12: Switching device combinations for (V_{AB},V_{BC},V_{CA}) = ($+V_{cap}$,0,$-V_{cap}$) and (V_{ab},V_{bc},V_{ca}) = (0,$-V_{cap}$,$+V_{cap}$).

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
employ single capacitor																	
01	00	11	11	00	00	11	11	00	IA-Ic	0	0	0	0	0	0	0	0
01	00	11	00	11	00	11	11	00	IA-Ic	0	0	0	0	0	0	0	0
01	00	11	11	11	00	11	00	00	IA-Ic	0	0	0	0	0	0	0	0
01	00	11	11	11	00	00	11	00	IA-Ic	0	0	0	0	0	0	0	0
00	01	11	11	00	00	11	11	00	0	IA-Ic	0	0	0	0	0	0	0
00	01	11	00	11	00	11	11	00	0	IA-Ic	0	0	0	0	0	0	0
00	01	11	11	11	00	11	00	00	0	IA-Ic	0	0	0	0	0	0	0
00	01	11	11	11	00	00	11	00	0	IA-Ic	0	0	0	0	0	0	0
00	00	11	11	00	10	11	11	00	0	0	0	0	0	IA-Ic	0	0	0
00	00	11	00	11	10	11	11	00	0	0	0	0	0	IA-Ic	0	0	0
00	00	11	11	11	10	11	00	00	0	0	0	0	0	IA-Ic	0	0	0
00	00	11	11	11	10	00	11	00	0	0	0	0	0	IA-Ic	0	0	0
00	00	11	11	00	00	11	11	10	0	0	0	0	0	0	0	0	IA-Ic
00	00	11	00	11	00	11	11	10	0	0	0	0	0	0	0	0	IA-Ic
00	00	11	11	11	00	11	00	10	0	0	0	0	0	0	0	0	IA-Ic
00	00	11	11	11	00	00	11	10	0	0	0	0	0	0	0	0	IA-Ic
employ two capacitors																	
01	01	11	11	00	00	11	00	00	IA+Ia	Ib	0	0	0	0	0	0	0
01	01	11	11	00	00	00	11	00	Ia-IB	Ib-IC	0	0	0	0	0	0	0
01	01	11	00	11	00	11	00	00	Ia-IC	Ib-IB	0	0	0	0	0	0	0
01	01	11	00	11	00	00	11	00	Ia	IA+Ib	0	0	0	0	0	0	0
01	00	00	11	00	10	11	11	00	IA	0	0	0	0	-Ic	0	0	0
01	00	00	00	11	10	11	11	00	IA	0	0	0	0	-Ic	0	0	0
01	00	11	00	00	10	11	11	00	-Ic-IC	0	0	0	0	-IB	0	0	0
01	00	00	11	11	10	11	00	00	IA	0	0	0	0	-Ic	0	0	0
01	00	00	11	11	10	00	11	00	IA	0	0	0	0	-Ic	0	0	0
01	00	11	00	11	10	11	00	00	Ia-IC	0	0	0	0	Ib-IB	0	0	0
01	00	11	00	11	10	00	11	00	Ia	0	0	0	0	IA+Ib	0	0	0
01	00	00	11	00	00	11	11	10	IA	0	0	0	0	0	0	0	-Ic
01	00	00	00	11	00	11	11	10	IA	0	0	0	0	0	0	0	-Ic
01	00	00	11	11	00	11	00	10	IA	0	0	0	0	0	0	0	-Ic
01	00	00	11	11	00	00	11	10	IA	0	0	0	0	0	0	0	-Ic
01	00	11	11	00	00	00	11	10	Ia-IB	0	0	0	0	0	0	0	Ib-IC
01	00	11	00	11	00	00	11	10	Ia	0	0	0	0	0	0	0	IA+Ib
01	00	11	11	11	00	00	00	10	-Ic-IB	0	0	0	0	0	0	0	-IC
00	01	00	11	00	10	11	11	00	0	IA	0	0	0	-Ic	0	0	0
00	01	00	00	11	10	11	11	00	0	IA	0	0	0	-Ic	0	0	0
00	01	11	00	00	10	11	11	00	0	-Ic-IC	0	0	0	-IB	0	0	0
00	01	00	11	11	10	11	00	00	0	IA	0	0	0	-Ic	0	0	0
00	01	00	11	11	10	00	11	00	0	IA	0	0	0	-Ic	0	0	0
00	01	11	11	00	10	11	00	00	0	Ib	0	0	0	IA+Ia	0	0	0

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
00	01	11	11	00	10	00	11	00	0	Ib-IC	0	0	0	Ia-IB	0	0	0
00	01	00	11	00	00	11	11	10	0	IA	0	0	0	0	0	0	-Ic
00	01	00	00	11	00	11	11	10	0	IA	0	0	0	0	0	0	-Ic
00	01	00	11	11	00	11	00	10	0	IA	0	0	0	0	0	0	-Ic
00	01	00	11	11	00	00	11	10	0	IA	0	0	0	0	0	0	-Ic
00	01	11	11	00	00	11	00	10	0	Ib	0	0	0	0	0	0	IA+Ia
00	01	11	00	11	00	11	00	10	0	Ib-IB	0	0	0	0	0	0	Ia-IC
00	01	11	11	11	00	00	00	10	0	-Ic-IB	0	0	0	0	0	0	-IC
00	00	11	00	00	10	11	11	10	0	0	0	0	0	-IB	0	0	-IC-Ic
00	00	11	11	00	10	00	11	10	0	0	0	0	0	Ia-IB	0	0	Ib-IC
00	00	11	00	11	10	11	00	10	0	0	0	0	0	Ib-IB	0	0	Ia-IC
00	00	11	11	11	10	00	00	10	0	0	0	0	0	-Ic-IB	0	0	-IC
employ three capacitors																	
01	01	11	00	00	10	11	00	00	Ia-IC	Ib	0	0	0	-IB	0	0	0
01	01	11	00	00	10	00	11	00	Ia	Ib-IC	0	0	0	-IB	0	0	0
01	01	00	11	00	10	11	00	00	IA-Ib	Ib	0	0	0	-Ic	0	0	0
01	01	00	00	11	10	11	00	00	Ia-IC	-Ia-IB	0	0	0	-Ic	0	0	0
01	01	00	11	00	10	00	11	00	-Ib-IB	Ib-IC	0	0	0	-Ic	0	0	0
01	01	00	00	11	10	00	11	00	Ia	IA-Ia	0	0	0	-Ic	0	0	0
01	01	11	11	00	00	00	00	10	Ia-IB	Ib	0	0	0	0	0	0	-IC
01	01	11	00	11	00	00	00	10	Ia	Ib-IB	0	0	0	0	0	0	-IC
01	01	00	11	00	00	11	00	10	IA-Ib	Ib	0	0	0	0	0	0	-Ic
01	01	00	11	00	00	00	11	10	Ia-IB	-Ia-IC	0	0	0	0	0	0	-Ic
01	01	00	00	11	00	11	00	10	-IC-Ib	Ib-IB	0	0	0	0	0	0	-Ic
01	01	00	00	11	00	00	11	10	Ia	IA-Ia	0	0	0	0	0	0	-Ic
01	00	00	00	00	10	11	11	10	IA	0	0	0	0	-IB	0	0	IB-Ic
01	00	00	11	00	10	00	11	10	IA	0	0	0	0	IC+Ia	0	0	Ib-IC
01	00	00	00	11	10	11	00	10	IA	0	0	0	0	Ib-IB	0	0	IB+Ia
01	00	11	00	00	10	00	11	10	Ia	0	0	0	0	-IB	0	0	Ib-IC
01	00	00	11	11	10	00	00	10	IA	0	0	0	0	IC-Ic	0	0	-IC
01	00	11	00	11	10	00	00	10	Ia	0	0	0	0	Ib-IB	0	0	-IC
00	01	00	00	00	10	11	11	10	0	IA	0	0	0	-IB	0	0	IB-Ic
00	01	00	11	00	10	00	11	10	0	IA	0	0	0	Ia-IB	0	0	IB+Ib
00	01	00	00	11	10	11	00	10	0	IA	0	0	0	IC+Ib	0	0	Ia-IC
00	01	11	00	00	10	11	00	10	0	Ib	0	0	0	-IB	0	0	Ia-IC
00	01	00	11	11	10	00	00	10	0	IA	0	0	0	IC-Ic	0	0	-IC
00	01	11	11	00	10	00	00	10	0	Ib	0	0	0	Ia-IB	0	0	-IC
employ four capacitors																	
01	01	11	00	00	10	00	00	10	Ia	Ib	0	0	0	-IB	0	0	-IC
01	01	00	00	00	10	11	00	10	IA-Ib	Ib	0	0	0	-IB	0	0	IB-Ic
01	01	00	00	00	10	00	11	10	Ia	IA-Ia	0	0	0	-IB	0	0	IB-Ic
01	01	00	11	00	10	00	00	10	IA-Ib	Ib	0	0	0	IC-Ic	0	0	-IC
01	01	00	00	11	10	00	00	10	Ia	IA-Ia	0	0	0	Ic-IC	0	0	-IC

Table B.13: Switching device combinations for (V_{AB},V_{BC},V_{CA}) = ($+V_{cap}$,0,$-V_{cap}$) and (V_{ab},V_{bc},V_{ca}) = ($+V_{cap}$,$-V_{cap}$,0).

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
employ single capacitor																	
11	01	11	00	11	00	00	11	00	0	IA+Ib	0	0	0	0	0	0	0
11	00	11	10	11	00	00	11	00	0	0	0	IA+Ib	0	0	0	0	0
11	00	11	00	11	10	00	11	00	0	0	0	0	0	IA+Ib	0	0	0
11	00	11	00	11	00	10	11	00	0	0	0	0	0	0	IA+Ib	0	0
11	00	11	00	11	00	00	11	10	0	0	0	0	0	0	0	0	IA+Ib
employ two capacitors																	
11	01	11	10	00	00	00	11	00	0	Ib-IC	0	-IB	0	0	0	0	0
00	01	11	10	11	00	00	11	00	0	IA-Ic	0	-Ia	0	0	0	0	0
11	01	11	00	00	10	00	11	00	0	Ib-IC	0	0	0	-IB	0	0	0
11	01	00	00	11	10	00	11	00	0	IA-Ia	0	0	0	-Ic	0	0	0
11	01	11	00	11	00	10	00	00	0	Ib-IB	0	0	0	0	-IC	0	0
00	01	11	00	11	00	10	11	00	0	IA-Ic	0	0	0	0	-Ia	0	0
11	01	11	00	11	00	00	00	10	0	Ib-IB	0	0	0	0	0	0	-IC
11	01	00	00	11	00	00	11	10	0	IA-Ia	0	0	0	0	0	0	-Ic
11	00	00	10	11	10	00	11	00	0	0	0	IA-Ia	0	-Ic	0	0	0
00	00	11	10	11	10	00	11	00	0	0	0	-Ia	0	IA-Ic	0	0	0
11	00	11	10	00	00	10	11	00	0	0	0	-IB	0	0	Ib-IC	0	0
11	00	11	10	11	00	10	00	00	0	0	0	Ib-IB	0	0	-IC	0	0
11	00	00	10	11	00	00	11	10	0	0	0	IA-Ia	0	0	0	0	-Ic
00	00	11	10	11	00	00	11	10	0	0	0	-Ia	0	0	0	0	IA-Ic
11	00	11	10	00	00	00	11	10	0	0	0	-IB	0	0	0	0	Ib-IC
11	00	11	10	11	00	00	00	10	0	0	0	Ib-IB	0	0	0	0	-IC
11	00	00	00	11	10	10	11	00	0	0	0	0	0	-Ic	IA-Ia	0	0
00	00	11	00	11	10	10	11	00	0	0	0	0	0	IA-Ic	-Ia	0	0
11	00	11	00	00	10	10	11	00	0	0	0	0	0	-IB	Ib-IC	0	0
11	00	11	00	11	10	10	00	00	0	0	0	0	0	Ib-IB	-IC	0	0
11	00	11	00	00	10	00	11	10	0	0	0	0	0	-IB	0	0	Ib-IC
11	00	11	00	11	10	00	00	10	0	0	0	0	0	Ib-IB	0	0	-IC
11	00	00	00	11	00	10	11	10	0	0	0	0	0	0	IA-Ia	0	-Ic
00	00	11	00	11	00	10	11	10	0	0	0	0	0	0	-Ia	0	IA-Ic
employ three capacitors																	
00	01	00	10	11	10	00	11	00	0	IA	0	-Ia	0	-Ic	0	0	0
11	01	00	10	00	10	00	11	00	0	Ib-IC	0	Ic-IB	0	-Ic	0	0	0
00	01	11	10	00	10	00	11	00	0	Ib-IC	0	-Ia	0	Ia-IB	0	0	0
11	01	11	10	00	00	10	00	00	0	Ib	0	-IB	0	0	-IC	0	0
00	01	11	10	00	00	10	11	00	0	IA-Ic	0	-IB	0	0	IB-Ia	0	0
00	01	11	10	11	00	10	00	00	0	IA-Ic	0	IC-Ia	0	0	-IC	0	0
00	01	00	10	11	00	00	11	10	0	IA	0	-Ia	0	0	0	0	-Ic
11	01	11	10	00	00	00	00	10	0	Ib	0	-IB	0	0	0	0	-IC
11	01	00	10	00	00	00	11	10	0	-IC-Ia	0	-IB	0	0	0	0	-Ic
00	01	11	10	11	00	00	00	10	0	-IB-Ic	0	-Ia	0	0	0	0	-IC

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
00	01	00	00	11	10	10	11	00	0	IA	0	0	0	-Ic	-Ia	0	0
11	01	11	00	00	10	10	00	00	0	Ib	0	0	0	-IB	-IC	0	0
00	01	11	00	00	10	10	11	00	0	-Ic-IC	0	0	0	-IB	-Ia	0	0
11	01	00	00	11	10	10	00	00	0	-IB-Ia	0	0	0	-Ic	-IC	0	0
11	01	11	00	00	10	00	00	10	0	Ib	0	0	0	-IB	0	0	-IC
11	01	00	00	00	10	00	11	10	0	IA-Ia	0	0	0	-IB	0	0	IB-Ic
11	01	00	00	11	10	00	00	10	0	IA-Ia	0	0	0	IC-Ic	0	0	-IC
00	01	00	00	11	00	10	11	10	0	IA	0	0	0	0	-Ia	0	-Ic
11	01	00	00	11	00	10	00	10	0	Ib-IB	0	0	0	0	Ic-IC	0	-Ic
00	01	11	00	11	00	10	00	10	0	Ib-IB	0	0	0	0	-Ia	0	Ia-IC
11	00	00	10	00	10	10	11	00	0	0	0	Ic-IB	0	-Ic	Ib-IC	0	0
00	00	11	10	00	10	10	11	00	0	0	0	Ic+IC	0	IA-Ic	Ib-IC	0	0
11	00	00	10	11	10	10	00	00	0	0	0	-IB-Ia	0	-Ic	-IC	0	0
00	00	11	10	11	10	10	00	00	0	0	0	IC-Ia	0	IA-Ic	-IC	0	0
11	00	00	10	00	10	00	11	10	0	0	0	IA-Ia	0	Ia+IC	0	0	Ib-IC
00	00	11	10	00	10	00	11	10	0	0	0	-Ia	0	Ia-IB	0	0	Ib-IC
11	00	00	10	11	10	00	00	10	0	0	0	IA-Ia	0	IC-Ic	0	0	-IC
00	00	11	10	11	10	00	00	10	0	0	0	-Ia	0	-Ic-IB	0	0	-IC
11	00	00	10	00	00	10	11	10	0	0	0	-IB	0	0	-Ia-IC	0	-Ic
00	00	11	10	00	00	10	11	10	0	0	0	-IB	0	0	IB-Ia	0	IA-Ic
11	00	00	10	11	00	10	00	10	0	0	0	Ib-IB	0	0	Ic-IC	0	-Ic
00	00	11	10	11	00	10	00	10	0	0	0	Ib-IB	0	0	IB+Ic	0	IA-Ic
11	00	00	00	00	10	10	11	10	0	0	0	0	0	-IB	IA-Ia	0	IB-Ic
00	00	11	00	00	10	10	11	10	0	0	0	0	0	-IB	-Ia	0	-IC-Ic
11	00	00	00	11	10	10	00	10	0	0	0	0	0	Ib-IB	IA-Ia	0	Ia+IB
00	00	11	00	11	10	10	00	10	0	0	0	0	0	Ib-IB	-Ia	0	Ia-IC
employ four capacitors																	
00	01	00	10	00	10	10	11	00	0	IA	0	Ic-IB	0	-Ic	IB+Ib	0	0
00	01	00	10	11	10	10	00	00	0	IA	0	IC-Ia	0	-Ic	-IC	0	0
11	01	00	10	00	10	10	00	00	0	Ib	0	Ic-IB	0	-Ic	-IC	0	0
00	01	11	10	00	10	10	00	00	0	Ib	0	IC-Ia	0	Ia+IA	-IC	0	0
00	01	00	10	00	10	00	11	10	0	IA	0	-Ia	0	Ia-IB	0	0	IB+Ib
00	01	00	10	11	10	00	00	10	0	IA	0	-Ia	0	IC-Ic	0	0	-IC
11	01	00	10	00	10	00	00	10	0	Ib	0	Ic+IA	0	IC-Ic	0	0	-IC
00	01	11	10	00	10	00	00	10	0	Ib	0	-Ia	0	Ia-IB	0	0	-IC
00	01	00	10	00	00	10	11	10	0	IA	0	-IB	0	0	IB-Ia	0	-Ic
00	01	00	10	11	00	10	00	10	0	IA	0	IC+Ib	0	0	Ic-IC	0	-Ic
11	01	00	10	00	00	10	00	10	0	Ib	0	-IB	0	0	Ic-IC	0	-Ic
00	01	11	10	00	00	10	00	10	0	Ib	0	-IB	0	0	IB-Ia	0	Ia+IA
00	01	00	00	00	10	10	11	10	0	IA	0	0	0	-IB	-Ia	0	IB-Ic
00	01	00	00	11	10	10	00	10	0	IA	0	0	0	IC+Ib	-Ia	0	Ia-IC
11	01	00	00	00	10	10	00	10	0	Ib	0	0	0	-IB	Ic+IA	0	IB-Ic
00	01	11	00	00	10	10	00	10	0	Ib	0	0	0	-IB	-Ia	0	Ia-IC

Table B.14: Switching device combinations for (V_{AB},V_{BC},V_{CA}) = (0,+V_{cap},−V_{cap}) and (V_{ab},V_{bc},V_{ca}) = (0,0,0).

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
employ single capacitor																	
11	11	11	11	00	00	10	00	00	0	0	0	0	0	0	-IC	0	0
11	11	11	00	11	00	10	00	00	0	0	0	0	0	0	-IC	0	0
11	11	11	00	00	11	10	00	00	0	0	0	0	0	0	-IC	0	0
11	00	00	11	11	11	10	00	00	0	0	0	0	0	0	-IC	0	0
00	11	00	11	11	11	10	00	00	0	0	0	0	0	0	-IC	0	0
00	00	11	11	11	11	10	00	00	0	0	0	0	0	0	-IC	0	0
11	11	00	11	00	11	10	00	00	0	0	0	0	0	0	-IC	0	0
11	11	00	00	11	11	10	00	00	0	0	0	0	0	0	-IC	0	0
11	00	11	11	11	00	10	00	00	0	0	0	0	0	0	-IC	0	0
11	00	11	00	11	11	10	00	00	0	0	0	0	0	0	-IC	0	0
00	11	11	11	11	00	10	00	00	0	0	0	0	0	0	-IC	0	0
00	11	11	11	00	11	10	00	00	0	0	0	0	0	0	-IC	0	0
11	11	11	11	00	00	00	10	00	0	0	0	0	0	0	0	-IC	0
11	11	11	00	11	00	00	10	00	0	0	0	0	0	0	0	-IC	0
11	11	11	00	00	11	00	10	00	0	0	0	0	0	0	0	-IC	0
11	00	00	11	11	11	00	10	00	0	0	0	0	0	0	0	-IC	0
00	11	00	11	11	11	00	10	00	0	0	0	0	0	0	0	-IC	0
00	00	11	11	11	11	00	10	00	0	0	0	0	0	0	0	-IC	0
11	11	00	11	00	11	00	10	00	0	0	0	0	0	0	0	-IC	0
11	11	00	00	11	11	00	10	00	0	0	0	0	0	0	0	-IC	0
11	00	11	11	11	00	00	10	00	0	0	0	0	0	0	0	-IC	0
11	00	11	00	11	11	00	10	00	0	0	0	0	0	0	0	-IC	0
00	11	11	11	11	00	00	10	00	0	0	0	0	0	0	0	-IC	0
00	11	11	11	00	11	00	10	00	0	0	0	0	0	0	0	-IC	0
11	11	11	11	00	00	00	00	10	0	0	0	0	0	0	0	0	-IC
11	11	11	00	11	00	00	00	10	0	0	0	0	0	0	0	0	-IC
11	11	11	00	00	11	00	00	10	0	0	0	0	0	0	0	0	-IC
11	00	00	11	11	11	00	00	10	0	0	0	0	0	0	0	0	-IC
00	11	00	11	11	11	00	00	10	0	0	0	0	0	0	0	0	-IC
00	00	11	11	11	11	00	00	10	0	0	0	0	0	0	0	0	-IC
11	11	00	11	00	11	00	00	10	0	0	0	0	0	0	0	0	-IC
11	11	00	00	11	11	00	00	10	0	0	0	0	0	0	0	0	-IC
11	00	11	11	11	00	00	00	10	0	0	0	0	0	0	0	0	-IC
11	00	11	00	11	11	00	00	10	0	0	0	0	0	0	0	0	-IC
00	11	11	11	11	00	00	00	10	0	0	0	0	0	0	0	0	-IC
00	11	11	11	00	11	00	00	10	0	0	0	0	0	0	0	0	-IC
employ two capacitors																	
01	00	00	01	00	00	11	11	11	IA	0	0	IB	0	0	0	0	0
01	00	00	00	01	00	11	11	11	IA	0	0	0	IB	0	0	0	0
01	00	00	00	00	01	11	11	11	IA	0	0	0	0	IB	0	0	0
00	01	00	01	00	00	11	11	11	0	IA	0	IB	0	0	0	0	0

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
00	01	00	00	01	00	11	11	11	0	IA	0	0	IB	0	0	0	0
00	01	00	00	00	01	11	11	11	0	IA	0	0	0	IB	0	0	0
00	00	01	01	00	00	11	11	11	0	0	IA	IB	0	0	0	0	0
00	00	01	00	01	00	11	11	11	0	0	IA	0	IB	0	0	0	0
00	00	01	00	00	01	11	11	11	0	0	IA	0	0	IB	0	0	0
11	00	00	11	00	11	10	10	00	0	0	0	0	0	0	Ib-IC	-Ib	0
11	00	00	00	11	11	10	10	00	0	0	0	0	0	0	IA-Ia	Ia+IB	0
00	11	00	11	00	11	10	10	00	0	0	0	0	0	0	Ib+IB	IA-Ib	0
00	11	00	00	11	11	10	10	00	0	0	0	0	0	0	-Ia	Ia-IC	0
00	00	11	11	00	11	10	10	00	0	0	0	0	0	0	Ib-IC	-Ib	0
00	00	11	00	11	11	10	10	00	0	0	0	0	0	0	-Ia	Ia-IC	0
11	00	11	11	00	00	10	10	00	0	0	0	0	0	0	Ib-IC	-Ib	0
00	11	11	11	00	00	10	10	00	0	0	0	0	0	0	IB-Ia	Ia+IA	0
11	00	11	00	11	00	10	10	00	0	0	0	0	0	0	Ib+IA	IB-Ib	0
00	11	11	00	11	00	10	10	00	0	0	0	0	0	0	-Ia	Ia-IC	0
11	00	11	00	00	11	10	10	00	0	0	0	0	0	0	Ib-IC	-Ib	0
00	11	11	00	00	11	10	10	00	0	0	0	0	0	0	-Ia	Ia-IC	0
11	00	00	11	11	00	10	00	10	0	0	0	0	0	0	Ic-IC	0	-Ic
11	00	00	00	11	11	10	00	10	0	0	0	0	0	0	IA-Ia	0	Ia+IB
00	11	00	11	11	00	10	00	10	0	0	0	0	0	0	Ic-IC	0	-Ic
00	11	00	00	11	11	10	00	10	0	0	0	0	0	0	-Ia	0	Ia-IC
00	00	11	11	11	00	10	00	10	0	0	0	0	0	0	Ic+IB	0	IA-Ic
00	00	11	00	11	11	10	00	10	0	0	0	0	0	0	-Ia	0	Ia-IC
11	11	00	11	00	00	10	00	10	0	0	0	0	0	0	Ic-IC	0	-Ic
00	11	11	11	00	00	10	00	’10	0	0	0	0	0	0	IB-Ia	0	Ia+IA
11	11	00	00	11	00	10	00	10	0	0	0	0	0	0	Ic-IC	0	-Ic
00	11	11	00	11	00	10	00	10	0	0	0	0	0	0	-Ia	0	Ia-IC
11	11	00	00	00	11	10	00	10	0	0	0	0	0	0	Ic+IA	0	IB-Ic
00	11	11	00	00	11	10	00	10	0	0	0	0	0	0	-Ia	0	Ia-IC
11	00	00	11	11	00	00	10	10	0	0	0	0	0	0	0	Ic-IC	-Ic
11	00	00	11	00	11	00	10	10	0	0	0	0	0	0	0	-Ib	Ib-IC
00	11	00	11	11	00	00	10	10	0	0	0	0	0	0	0	Ic-IC	-Ic
00	11	00	11	00	11	00	10	10	0	0	0	0	0	0	0	IA-Ib	Ib+IB
00	00	11	11	11	00	00	10	10	0	0	0	0	0	0	0	Ic+IB	IA-Ic
00	00	11	11	00	11	00	10	10	0	0	0	0	0	0	0	-Ib	Ib-IC
11	11	00	11	00	00	00	10	10	0	0	0	0	0	0	0	Ic-IC	-Ic
11	00	11	11	00	00	00	10	10	0	0	0	0	0	0	0	-Ib	Ib-IC
11	11	00	00	11	00	00	10	10	0	0	0	0	0	0	0	Ic-IC	-Ic
11	00	11	00	11	00	00	10	10	0	0	0	0	0	0	0	IB-Ib	Ib+IA
11	11	00	00	00	11	00	10	10	0	0	0	0	0	0	0	Ic+IA	IB-Ic
11	00	11	00	00	11	00	10	10	0	0	0	0	0	0	0	-Ib	Ib-IC
employ three capacitors																	
01	01	00	01	00	00	11	00	11	IA-Ib	Ib	0	IB	0	0	0	0	0
01	01	00	01	00	00	00	11	11	Ia-IB	-Ia-IC	0	IB	0	0	0	0	0
01	01	00	00	01	00	11	00	11	-Ib-IC	Ib-IB	0	0	IB	0	0	0	0

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
01	01	00	00	01	00	00	11	11	Ia	IA-Ia	0	0	IB	0	0	0	0
01	01	00	00	00	01	11	00	11	IA-Ib	Ib	0	0	0	IB	0	0	0
01	01	00	00	00	01	00	11	11	Ia	IA-Ia	0	0	0	IB	0	0	0
01	00	01	01	00	00	11	11	00	IA-Ic	0	Ic	IB	0	0	0	0	0
01	00	01	01	00	00	00	11	11	Ia-IB	0	-Ia-IC	IB	0	0	0	0	0
01	00	01	00	01	00	11	11	00	IA-Ic	0	Ic	0	IB	0	0	0	0
01	00	01	00	01	00	00	11	11	Ia	0	IA-Ia	0	IB	0	0	0	0
01	00	01	00	00	01	11	11	00	-Ic-IC	0	Ic-IB	0	0	IB	0	0	0
01	00	01	00	00	01	00	11	11	Ia	0	IA-Ia	0	0	IB	0	0	0
01	00	00	01	01	00	11	00	11	IA	0	0	IB-Ib	Ib	0	0	0	0
01	00	00	01	01	00	00	11	11	IA	0	0	Ia-IA	-Ia-IC	0	0	0	0
01	00	00	01	00	01	11	11	00	IA	0	0	IB-Ic	0	Ic	0	0	0
01	00	00	01	00	01	00	11	11	IA	0	0	Ia-IA	0	-Ia-IC	0	0	0
01	00	00	00	01	01	11	11	00	IA	0	0	0	IB-Ic	Ic	0	0	0
01	00	00	00	01	01	11	00	11	IA	0	0	0	Ib	IB-Ib	0	0	0
00	01	01	01	00	00	11	11	00	0	IA-Ic	Ic	IB	0	0	0	0	0
00	01	01	01	00	00	11	00	11	0	Ib	IA-Ib	IB	0	0	0	0	0
00	01	01	00	01	00	11	11	00	0	IA-Ic	Ic	0	IB	0	0	0	0
00	01	01	00	01	00	11	00	11	0	Ib-IB	-Ib-IC	0	IB	0	0	0	0
00	01	01	00	00	01	11	11	00	0	-Ic-IC	Ic-IB	0	0	IB	0	0	0
00	01	01	00	00	01	11	00	11	0	Ib	IA-Ib	0	0	IB	0	0	0
00	01	00	01	01	00	11	00	11	0	IA	0	-Ib-IC	Ib-IA	0	0	0	0
00	01	00	01	01	00	00	11	11	0	IA	0	Ia	IB-Ia	0	0	0	0
00	01	00	01	00	01	11	11	00	0	IA	0	IB-Ic	0	Ic	0	0	0
00	01	00	01	00	01	00	11	11	0	IA	0	Ia	0	IB-Ia	0	0	0
00	01	00	00	01	01	11	11	00	0	IA	0	0	IB-Ic	Ic	0	0	0
00	01	00	00	01	01	11	00	11	0	IA	0	0	Ib-IA	-Ib-IC	0	0	0
00	00	01	01	01	00	11	00	11	0	0	IA	IB-Ib	Ib	0	0	0	0
00	00	01	01	01	00	00	11	11	0	0	IA	Ia	IB-Ia	0	0	0	0
00	00	01	01	00	01	11	11	00	0	0	IA	-Ic-IC	0	Ic-IA	0	0	0
00	00	01	01	00	01	00	11	11	0	0	IA	Ia	0	IB-Ia	0	0	0
00	00	01	00	01	01	11	11	00	0	0	IA	0	-Ic-IC	Ic-IA	0	0	0
00	00	01	00	01	01	11	00	11	0	0	IA	0	Ib	IB-Ib	0	0	0
11	00	00	11	00	00	10	10	10	0	0	0	0	0	0	-Ia-IC	-Ib	-Ic
11	00	00	00	11	00	10	10	10	0	0	0	0	0	0	IA-Ia	IB-Ib	-Ic
11	00	00	00	00	11	10	10	10	0	0	0	0	0	0	IA-Ia	-Ib	IB-Ic
00	11	00	11	00	00	10	10	10	0	0	0	0	0	0	IB-Ia	IA-Ib	-Ic
00	11	00	00	11	00	10	10	10	0	0	0	0	0	0	-Ia	-Ib-IC	-Ic
00	11	00	00	00	11	10	10	10	0	0	0	0	0	0	-Ia	IA-Ib	IB-Ic
00	00	11	11	00	00	10	10	10	0	0	0	0	0	0	IB-Ia	-Ib	IA-Ic
00	00	11	00	11	00	10	10	10	0	0	0	0	0	0	-Ia	IB-Ib	IA-Ic
00	00	11	00	00	11	10	10	10	0	0	0	0	0	0	-Ia	-Ib	-Ic-IC
employ four capacitors																	
01	01	01	01	00	00	11	00	00	IA+Ia	Ib	Ic	IB	0	0	0	0	0
01	01	01	01	00	00	00	11	00	Ia-IB	Ib-IC	Ic	IB	0	0	0	0	0

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
01	01	01	01	00	00	00	00	11	Ia-IB	Ib	Ic-IC	IB	0	0	0	0	0
01	01	01	00	01	00	11	00	00	Ia-IC	Ib-IB	Ic	0	IB	0	0	0	0
01	01	01	00	01	00	00	11	00	Ia	IA+Ib	Ic	0	IB	0	0	0	0
01	01	01	00	01	00	00	00	11	Ia	Ib-IB	Ic-IC	0	IB	0	0	0	0
01	01	01	00	00	01	11	00	00	Ia-IC	Ib	Ic-IB	0	0	IB	0	0	0
01	01	01	00	00	01	00	11	00	Ia	Ib-IC	Ic-IB	0	0	IB	0	0	0
01	01	01	00	00	01	00	00	11	Ia	Ib	IA+Ic	0	0	IB	0	0	0
01	01	00	01	00	01	11	00	00	IA-Ib	Ib	0	IB-Ic	0	Ic	0	0	0
01	01	00	01	00	01	00	11	00	-IB-Ib	Ib-IC	0	IB-Ic	0	Ic	0	0	0
01	01	00	01	00	01	00	00	11	IA-Ib	Ib	0	-IA-Ic	0	Ic-IC	0	0	0
01	01	00	00	01	01	11	00	00	Ia-IC	-IB-Ia	0	0	IB-Ic	Ic	0	0	0
01	01	00	00	01	01	00	11	00	Ia	IA-Ia	0	0	IB-Ic	Ic	0	0	0
01	01	00	00	01	01	00	00	11	Ia	IA-Ia	0	0	-IA-Ic	Ic-IC	0	0	0
01	00	01	01	01	00	11	00	00	IA-Ic	0	Ic	IB-Ib	Ib	0	0	0	0
01	00	01	01	01	00	00	11	00	IA-Ic	0	Ic	-IA-Ib	Ib-IC	0	0	0	0
01	00	01	01	01	00	00	00	11	-IB-Ic	0	Ic-IC	IB-Ib	Ib	0	0	0	0
01	00	01	00	01	01	11	00	00	Ia-IC	0	-IB-Ia	0	Ib	IB-Ib	0	0	0
01	00	01	00	01	01	00	11	00	Ia	0	IA-Ia	0	Ib-IC	-IA-Ib	0	0	0
01	00	01	00	01	01	00	00	11	Ia	0	IA-Ia	0	Ib	IB-Ib	0	0	0
01	00	00	01	01	01	11	00	00	IA	0	0	IB+Ia	Ib	Ic	0	0	0
01	00	00	01	01	01	00	11	00	IA	0	0	Ia-IA	Ib-IC	Ic	0	0	0
01	00	00	01	01	01	00	00	11	IA	0	0	Ia-IA	Ib	Ic-IC	0	0	0
00	01	01	01	01	00	11	00	00	0	IA-Ic	Ic	Ia-IC	-IA-Ia	0	0	0	0
00	01	01	01	01	00	00	11	00	0	IA-Ic	Ic	Ia	IB-Ia	0	0	0	0
00	01	01	01	01	00	00	00	11	0	-IB-Ic	Ic-IC	Ia	IB-Ia	0	0	0	0
00	01	01	01	00	01	11	00	00	0	Ib	IA-Ib	Ia-IC	0	-IA-Ia	0	0	0
00	01	01	01	00	01	00	11	00	0	Ib-IC	-IB-Ib	Ia	0	IB-Ia	0	0	0
00	01	01	01	00	01	00	00	11	0	Ib	IA-Ib	Ia	0	IB-Ia	0	0	0
00	01	00	01	01	01	11	00	00	0	IA	0	Ia-IC	Ib-IA	Ic	0	0	0
00	01	00	01	01	01	00	11	00	0	IA	0	Ia	IB+Ib	Ic	0	0	0
00	01	00	01	01	01	00	00	11	0	IA	0	Ia	Ib-IA	Ic-IC	0	0	0
00	00	01	01	01	01	11	00	00	0	0	IA	Ia-IC	Ib	Ic-IA	0	0	0
00	00	01	01	01	01	00	11	00	0	0	IA	Ia	Ib-IC	Ic-IA	0	0	0
00	00	01	01	01	01	00	00	11	0	0	IA	Ia	Ib	IB+Ic	0	0	0

Table B.15: Switching device combinations for (V_{AB},V_{BC},V_{CA}) = (0,+V_{cap},−V_{cap}) and (V_{ab},V_{bc},V_{ca}) = (+V_{cap},0,−V_{cap}).

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
employ single capacitor																	
11	01	00	11	00	00	00	11	11	0	-Ia-IC	0	0	0	0	0	0	0
11	00	01	11	00	00	00	11	11	0	0	-Ia-IC	0	0	0	0	0	0
11	00	00	11	01	00	00	11	11	0	0	0	0	-Ia-IC	0	0	0	0
11	00	00	11	00	01	00	11	11	0	0	0	0	0	-Ia-IC	0	0	0
11	00	00	11	00	00	10	11	11	0	0	0	0	0	0	-Ia-IC	0	0
employ two capacitors																	
11	01	01	11	00	00	00	11	00	0	Ib-IC	Ic	0	0	0	0	0	0
11	01	01	11	00	00	00	00	11	0	Ib	Ic-IC	0	0	0	0	0	0
00	01	00	11	01	00	00	11	11	0	IA	0	0	IB-Ia	0	0	0	0
11	01	00	00	01	00	00	11	11	0	IA-Ia	0	0	IB	0	0	0	0
00	01	00	11	00	01	00	11	11	0	IA	0	0	0	IB-Ia	0	0	0
11	01	00	00	00	01	00	11	11	0	IA-Ia	0	0	0	IB	0	0	0
11	01	00	11	00	01	00	11	00	0	Ib-IC	0	0	0	Ic	0	0	0
11	01	00	11	00	01	00	00	11	0	Ib	0	0	0	Ic-IC	0	0	0
00	01	00	11	00	00	10	11	11	0	IA	0	0	0	0	IB-Ia	0	0
11	01	00	11	00	00	10	00	11	0	Ib	0	0	0	0	Ic-IC	0	0
00	00	01	11	01	00	00	11	11	0	0	IA	0	IB-Ia	0	0	0	0
11	00	01	00	01	00	00	11	11	0	0	IA-Ia	0	IB	0	0	0	0
11	00	01	11	01	00	00	11	00	0	0	Ic	0	Ib-IC	0	0	0	0
11	00	01	11	01	00	00	00	11	0	0	Ic-IC	0	Ib	0	0	0	0
00	00	01	11	00	01	00	11	11	0	0	IA	0	0	IB-Ia	0	0	0
11	00	01	00	00	01	00	11	11	0	0	IA-Ia	0	0	IB	0	0	0
00	00	01	11	00	00	10	11	11	0	0	IA	0	0	0	IB-Ia	0	0
11	00	01	11	00	00	10	11	00	0	0	Ic	0	0	0	Ib-IC	0	0
11	00	00	11	01	01	00	11	00	0	0	0	0	Ib-IC	Ic	0	0	0
11	00	00	11	01	01	00	00	11	0	0	0	0	Ib	Ic-IC	0	0	0
11	00	00	00	01	00	10	11	11	0	0	0	0	IB	0	IA-Ia	0	0
11	00	00	11	01	00	10	00	11	0	0	0	0	Ib	0	Ic-IC	0	0
11	00	00	00	00	01	10	11	11	0	0	0	0	0	IB	IA-Ia	0	0
11	00	00	11	00	01	10	11	00	0	0	0	0	0	Ic	Ib-IC	0	0
employ three capacitors																	
11	01	01	00	01	00	00	11	00	0	IA+Ib	Ic	0	IB	0	0	0	0
11	01	01	00	01	00	00	00	11	0	Ib-IB	Ic-IC	0	IB	0	0	0	0
00	01	01	11	01	00	00	11	00	0	IA-Ic	Ic	0	IB-Ia	0	0	0	0
00	01	01	11	01	00	00	00	11	0	-IB-Ic	Ic-IC	0	IB-Ia	0	0	0	0
11	01	01	00	00	01	00	11	00	0	Ib-IC	Ic-IB	0	0	IB	0	0	0
11	01	01	00	00	01	00	00	11	0	Ib	IA+Ic	0	0	IB	0	0	0
00	01	01	11	00	01	00	11	00	0	Ib-IC	-IB-Ib	0	0	IB-Ia	0	0	0
00	01	01	11	00	01	00	00	11	0	Ib	IA-Ib	0	0	IB-Ia	0	0	0
11	01	01	11	00	00	10	00	00	0	Ib	Ic	0	0	0	-IC	0	0

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
00	01	01	11	00	00	10	11	00	0	IA-Ic	Ic	0	0	0	IB-Ia	0	0
00	01	01	11	00	00	10	00	11	0	Ib	IA-Ib	0	0	0	IB-Ia	0	0
00	01	00	11	01	01	00	11	00	0	IA	0	0	Ib+IB	Ic	0	0	0
00	01	00	11	01	01	00	00	11	0	IA	0	0	Ib-IA	Ic-IC	0	0	0
11	01	00	00	01	01	00	11	00	0	IA-Ia	0	0	IB-Ic	Ic	0	0	0
11	01	00	00	01	01	00	00	11	0	IA-Ia	0	0	-IA-Ic	Ic-IC	0	0	0
00	01	00	00	01	00	10	11	11	0	IA	0	0	IB	0	-Ia	0	0
00	01	00	11	01	00	10	00	11	0	IA	0	0	Ib-IA	0	Ic-IC	0	0
11	01	00	00	01	00	10	00	11	0	Ib-IB	0	0	IB	0	Ic-IC	0	0
00	01	00	00	00	01	10	11	11	0	IA	0	0	0	IB	-Ia	0	0
00	01	00	11	00	01	10	11	00	0	IA	0	0	0	Ic	Ib+IB	0	0
11	01	00	00	00	01	10	00	11	0	Ib	0	0	0	IB	Ic+IA	0	0
11	01	00	11	00	01	10	00	00	0	Ib	0	0	0	Ic	-IC	0	0
00	00	01	11	01	01	00	11	00	0	0	IA	0	Ib-IC	Ic-IA	0	0	0
00	00	01	11	01	01	00	00	11	0	0	IA	0	Ib	IB+Ic	0	0	0
11	00	01	00	01	01	00	11	00	0	0	IA-Ia	0	Ib-IC	-IA-Ib	0	0	0
11	00	01	00	01	01	00	00	11	0	0	IA-Ia	0	Ib	IB-Ib	0	0	0
00	00	01	00	01	00	10	11	11	0	0	IA	0	IB	0	-Ia	0	0
00	00	01	11	01	00	10	00	11	0	0	IA	0	Ib	0	Ic+IB	0	0
11	00	01	00	01	00	10	11	00	0	0	Ic	0	IB	0	Ib+IA	0	0
11	00	01	11	01	00	10	00	00	0	0	Ic	0	Ib	0	-IC	0	0
00	00	01	00	00	01	10	11	11	0	0	IA	0	0	IB	-Ia	0	0
00	00	01	11	00	01	10	11	00	0	0	IA	0	0	Ic-IA	Ib-IC	0	0
11	00	01	00	00	01	10	11	00	0	0	Ic-IB	0	0	IB	Ib-IC	0	0
11	00	00	00	01	01	10	11	00	0	0	0	0	IB-Ic	Ic	IA-Ia	0	0
11	00	00	00	01	01	10	00	11	0	0	0	0	Ib	IB-Ib	IA-Ia	0	0
11	00	00	11	01	01	10	00	00	0	0	0	0	Ib	Ic	-IC	0	0
employ four capacitors																	
11	01	01	00	01	00	10	00	00	0	Ib-IB	Ic	0	IB	0	-IC	0	0
00	01	01	00	01	00	10	11	00	0	IA-Ic	Ic	0	IB	0	-Ia	0	0
00	01	01	00	01	00	10	00	11	0	Ib-IB	-Ib-IC	0	IB	0	-Ia	0	0
00	01	01	11	01	00	10	00	00	0	IA-Ic	Ic	0	-IA-Ia	0	-IC	0	0
11	01	01	00	00	01	10	00	00	0	Ib	Ic-IB	0	0	IB	-IC	0	0
00	01	01	00	00	01	10	11	00	0	-Ic-IC	Ic-IB	0	0	IB	-Ia	0	0
00	01	01	00	00	01	10	00	11	0	Ib	IA-Ib	0	0	IB	-Ia	0	0
00	01	01	11	00	01	10	00	00	0	Ib	IA-Ib	0	0	-IA-Ia	-IC	0	0
00	01	00	00	01	01	10	11	00	0	IA	0	0	IB-Ic	Ic	-Ia	0	0
00	01	00	00	01	01	10	00	11	0	IA	0	0	Ib-IA	-Ib-IC	-Ia	0	0
00	01	00	11	01	01	10	00	00	0	IA	0	0	Ib-IA	Ic	-IC	0	0
11	01	00	00	01	01	10	00	00	0	-IB-Ia	0	0	IB-Ic	Ic	-IC	0	0
00	00	01	00	01	01	10	11	00	0	0	IA	0	-Ic-IC	Ic-IA	-Ia	0	0
00	00	01	00	01	01	10	00	11	0	0	IA	0	Ib	IB-Ib	-Ia	0	0
00	00	01	11	01	01	10	00	00	0	0	IA	0	Ib	Ic-IA	-IC	0	0
11	00	01	00	01	01	10	00	00	0	0	-IB-Ia	0	Ib	IB-Ib	-IC	0	0

Table B.16: Switching device combinations for (V_{AB},V_{BC},V_{CA}) = (0,+V_{cap},−V_{cap}) and (V_{ab},V_{bc},V_{ca}) = (0,+V_{cap},−V_{cap}).

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
employ single capacitor																	
11	11	01	11	00	00	00	00	11	0	0	Ic-IC	0	0	0	0	0	0
11	11	01	00	11	00	00	00	11	0	0	Ic-IC	0	0	0	0	0	0
11	00	01	11	11	00	00	00	11	0	0	Ic-IC	0	0	0	0	0	0
00	11	01	11	11	00	00	00	11	0	0	Ic-IC	0	0	0	0	0	0
11	00	00	11	11	01	00	00	11	0	0	0	0	0	Ic-IC	0	0	0
00	11	00	11	11	01	00	00	11	0	0	0	0	0	Ic-IC	0	0	0
11	11	00	11	00	01	00	00	11	0	0	0	0	0	Ic-IC	0	0	0
11	11	00	00	11	01	00	00	11	0	0	0	0	0	Ic-IC	0	0	0
11	00	00	11	11	00	10	00	11	0	0	0	0	0	0	Ic-IC	0	0
00	11	00	11	11	00	10	00	11	0	0	0	0	0	0	Ic-IC	0	0
11	11	00	11	00	00	10	00	11	0	0	0	0	0	0	Ic-IC	0	0
11	11	00	00	11	00	10	00	11	0	0	0	0	0	0	Ic-IC	0	0
11	00	00	11	11	00	00	10	11	0	0	0	0	0	0	0	Ic-IC	0
00	11	00	11	11	00	00	10	11	0	0	0	0	0	0	0	Ic-IC	0
11	11	00	11	00	00	00	10	11	0	0	0	0	0	0	0	Ic-IC	0
11	11	00	00	11	00	00	10	11	0	0	0	0	0	0	0	Ic-IC	0
employ two capacitors																	
11	11	01	00	00	01	00	00	11	0	0	IA+Ic	0	0	IB	0	0	0
00	00	01	11	11	01	00	00	11	0	0	IA	0	0	IB+Ic	0	0	0
11	00	01	00	11	01	00	00	11	0	0	IA-Ia	0	0	IB-Ib	0	0	0
00	11	01	11	00	01	00	00	11	0	0	IA-Ib	0	0	IB-Ia	0	0	0
00	00	01	11	11	00	10	00	11	0	0	IA	0	0	0	Ic+IB	0	0
11	11	01	11	00	00	10	00	00	0	0	Ic	0	0	0	-IC	0	0
11	11	01	00	11	00	10	00	00	0	0	Ic	0	0	0	-IC	0	0
00	11	01	11	00	00	10	00	11	0	0	IA-Ib	0	0	0	IB-Ia	0	0
00	11	01	00	11	00	10	00	11	0	0	-IC-Ib	0	0	0	-Ia	0	0
11	00	01	11	11	00	10	00	00	0	0	Ic	0	0	0	-IC	0	0
00	11	01	11	11	00	10	00	00	0	0	Ic	0	0	0	-IC	0	0
00	00	01	11	11	00	00	10	11	0	0	IA	0	0	0	0	Ic+IB	0
11	11	01	11	00	00	00	10	00	0	0	Ic	0	0	0	0	-IC	0
11	11	01	00	11	00	00	10	00	0	0	Ic	0	0	0	0	-IC	0
11	00	01	11	00	00	00	10	11	0	0	-IC-Ia	0	0	0	0	-Ib	0
11	00	01	00	11	00	00	10	11	0	0	IA-Ia	0	0	0	0	IB-Ib	0
11	00	01	11	11	00	00	10	00	0	0	Ic	0	0	0	0	-IC	0
00	11	01	11	11	00	00	10	00	0	0	Ic	0	0	0	0	-IC	0
11	00	00	00	11	01	10	00	11	0	0	0	0	0	IB-Ib	IA-Ia	0	0
00	11	00	00	11	01	10	00	11	0	0	0	0	0	-Ib-IC	-Ia	0	0
11	11	00	00	00	01	10	00	11	0	0	0	0	0	IB	Ic+IA	0	0
11	00	00	11	11	01	10	00	00	0	0	0	0	0	Ic	-IC	0	0
00	11	00	11	11	01	10	00	00	0	0	0	0	0	Ic	-IC	0	0
11	11	00	11	00	01	10	00	00	0	0	0	0	0	Ic	-IC	0	0

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
11	11	00	00	11	01	10	00	00	0	0	0	0	0	Ic	-IC	0	0
11	00	00	11	00	01	00	10	11	0	0	0	0	0	-IC-Ia	0	-Ib	0
00	11	00	11	00	01	00	10	11	0	0	0	0	0	IB-Ia	0	IA-Ib	0
11	11	00	00	00	01	00	10	11	0	0	0	0	0	IB	0	Ic+IA	0
11	00	00	11	11	01	00	10	00	0	0	0	0	0	Ic	0	-IC	0
00	11	00	11	11	01	00	10	00	0	0	0	0	0	Ic	0	-IC	0
11	11	00	11	00	01	00	10	00	0	0	0	0	0	Ic	0	-IC	0
11	11	00	00	11	01	00	10	00	0	0	0	0	0	Ic	0	-IC	0
11	00	00	11	00	00	10	10	11	0	0	0	0	0	0	-Ia-IC	-Ib	0
11	00	00	00	11	00	10	10	11	0	0	0	0	0	0	IA-Ia	IB-Ib	0
00	11	00	11	00	00	10	10	11	0	0	0	0	0	0	IB-Ia	IA-Ib	0
00	11	00	00	11	00	10	10	11	0	0	0	0	0	0	-Ia	-Ib-IC	0
employ three capacitors																	
00	00	01	00	11	01	10	00	11	0	0	IA	0	0	IB-Ib	-Ia	0	0
11	11	01	00	00	01	10	00	00	0	0	Ic-IB	0	0	IB	-IC	0	0
00	11	01	00	00	01	10	00	11	0	0	IA-Ib	0	0	IB	-Ia	0	0
00	00	01	11	11	01	10	00	00	0	0	IA	0	0	Ic-IA	-IC	0	0
11	00	01	00	11	01	10	00	00	0	0	-IB-Ia	0	0	IB-Ib	-IC	0	0
00	11	01	11	00	01	10	00	00	0	0	IA-Ib	0	0	-IA-Ia	-IC	0	0
00	00	01	11	00	01	00	10	11	0	0	IA	0	0	IB-Ia	0	-Ib	0
11	11	01	00	00	01	00	10	00	0	0	Ic-IB	0	0	IB	0	-IC	0
11	00	01	00	00	01	00	10	11	0	0	IA-Ia	0	0	IB	0	-Ib	0
00	00	01	11	11	01	00	10	00	0	0	IA	0	0	Ic-IA	0	-IC	0
11	00	01	00	11	01	00	10	00	0	0	IA-Ia	0	0	-IA-Ib	0	-IC	0
00	11	01	11	00	01	00	10	00	0	0	-IB-Ib	0	0	IB-Ia	0	-IC	0
00	00	01	11	00	00	10	10	11	0	0	IA	0	0	0	IB-Ia	-Ib	0
00	00	01	00	11	00	10	10	11	0	0	IA	0	0	0	-Ia	IB-Ib	0
11	00	01	11	00	00	10	10	00	0	0	Ic	0	0	0	Ib-IC	-Ib	0
00	11	01	11	00	00	10	10	00	0	0	Ic	0	0	0	IB-Ia	Ia+IA	0
11	00	01	00	11	00	10	10	00	0	0	Ic	0	0	0	IA+Ib	IB-Ib	0
00	11	01	00	11	00	10	10	00	0	0	Ic	0	0	0	-Ia	Ia-IC	0
11	00	00	00	00	01	10	10	11	0	0	0	0	0	IB	IA-Ia	-Ib	0
00	11	00	00	00	01	10	10	11	0	0	0	0	0	IB	-Ia	IA-Ib	0
11	00	00	11	00	01	10	10	00	0	0	0	0	0	Ic	Ib-IC	-Ib	0
11	00	00	00	11	01	10	10	00	0	0	0	0	0	Ic	IA-Ia	Ia+IB	0
00	11	00	11	00	01	10	10	00	0	0	0	0	0	Ic	Ib+IB	IA-Ib	0
00	11	00	00	11	01	10	10	00	0	0	0	0	0	Ic	-Ia	Ia-IC	0
employ four capacitors																	
00	00	01	00	00	01	10	10	11	0	0	IA	0	0	IB	-Ia	-Ib	0
00	00	01	11	00	01	10	10	00	0	0	IA	0	0	Ic-IA	Ib-IC	-Ib	0
00	00	01	00	11	01	10	10	00	0	0	IA	0	0	Ic-IA	-Ia	Ia-IC	0
11	00	01	00	00	01	10	10	00	0	0	Ic-IB	0	0	IB	Ib-IC	-Ib	0
00	11	01	00	00	01	10	10	00	0	0	Ic-IB	0	0	IB	-Ia	Ia-IC	0

Table B.17: Switching device combinations for (V_{AB},V_{BC},V_{CA}) = (0,+V_{cap},−V_{cap}) and (V_{ab},V_{bc},V_{ca}) = (−V_{cap},+V_{cap},0).

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
employ single capacitor																	
01	11	00	00	11	00	11	00	11	-IC-Ib	0	0	0	0	0	0	0	0
00	11	01	00	11	00	11	00	11	0	0	-IC-Ib	0	0	0	0	0	0
00	11	00	01	11	00	11	00	11	0	0	0	-IC-Ib	0	0	0	0	0
00	11	00	00	11	01	11	00	11	0	0	0	0	0	-IC-Ib	0	0	0
00	11	00	00	11	00	11	10	11	0	0	0	0	0	0	0	-IC-Ib	0
employ two capacitors																	
01	11	01	00	11	00	11	00	00	Ia-IC	0	Ic	0	0	0	0	0	0
01	11	01	00	11	00	00	00	11	Ia	0	Ic-IC	0	0	0	0	0	0
01	00	00	01	11	00	11	00	11	IA	0	0	IB-Ib	0	0	0	0	0
01	11	00	01	00	00	11	00	11	IA-Ib	0	0	IB	0	0	0	0	0
01	00	00	00	11	01	11	00	11	IA	0	0	0	0	IB-Ib	0	0	0
01	11	00	00	00	01	11	00	11	IA-Ib	0	0	0	0	IB	0	0	0
01	11	00	00	11	01	11	00	00	Ia-IC	0	0	0	0	Ic	0	0	0
01	11	00	00	11	01	00	00	11	Ia	0	0	0	0	Ic-IC	0	0	0
01	00	00	00	11	00	11	10	11	IA	0	0	0	0	0	0	IB-Ib	0
01	11	00	00	11	00	00	10	11	Ia	0	0	0	0	0	0	Ic-IC	0
00	00	01	01	11	00	11	00	11	0	0	IA	IB-Ib	0	0	0	0	0
00	11	01	01	00	00	11	00	11	0	0	IA-Ib	IB	0	0	0	0	0
00	11	01	01	11	00	11	00	00	0	0	Ic	Ia-IC	0	0	0	0	0
00	11	01	01	11	00	00	00	11	0	0	Ic-IC	Ia	0	0	0	0	0
00	00	01	00	11	01	11	00	11	0	0	IA	0	0	IB-Ib	0	0	0
00	11	01	00	00	01	11	00	11	0	0	IA-Ib	0	0	IB	0	0	0
00	00	01	00	11	00	11	10	11	0	0	IA	0	0	0	0	IB-Ib	0
00	11	01	00	11	00	11	10	00	0	0	Ic	0	0	0	0	Ia-IC	0
00	11	00	01	11	01	11	00	00	0	0	0	Ia-IC	0	Ic	0	0	0
00	11	00	01	11	01	00	00	11	0	0	0	Ia	0	Ic-IC	0	0	0
00	11	00	01	00	00	11	10	11	0	0	0	IB	0	0	0	IA-Ib	0
00	11	00	01	11	00	00	10	11	0	0	0	Ia	0	0	0	Ic-IC	0
00	11	00	00	00	01	11	10	11	0	0	0	0	0	IB	0	IA-Ib	0
00	11	00	00	11	01	11	10	00	0	0	0	0	0	Ic	0	Ia-IC	0
employ three capacitors																	
01	11	01	01	00	00	11	00	00	IA+Ia	0	Ic	IB	0	0	0	0	0
01	11	01	01	00	00	00	00	11	Ia-IB	0	Ic-IC	IB	0	0	0	0	0
01	00	01	01	11	00	11	00	00	IA-Ic	0	Ic	IB-Ib	0	0	0	0	0
01	00	01	01	11	00	00	00	11	-IB-Ic	0	Ic-IC	IB-Ib	0	0	0	0	0
01	11	01	00	00	01	11	00	00	Ia-IC	0	Ic-IB	0	0	IB	0	0	0
01	11	01	00	00	01	00	00	11	Ia	0	IA+Ic	0	0	IB	0	0	0
01	00	01	00	11	01	11	00	00	Ia-IC	0	-IB-Ia	0	0	IB-Ib	0	0	0
01	00	01	00	11	01	00	00	11	Ia	0	IA-Ia	0	0	IB-Ib	0	0	0
01	11	01	00	11	00	00	10	00	Ia	0	Ic	0	0	0	0	-IC	0
01	00	01	00	11	00	11	10	00	IA-Ic	0	Ic	0	0	0	0	IB-Ib	0

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
01	00	01	00	11	00	00	10	11	Ia	0	IA-Ia	0	0	0	0	IB-Ib	0
01	00	00	01	11	01	11	00	00	IA	0	0	IB+Ia	0	Ic	0	0	0
01	00	00	01	11	01	00	00	11	IA	0	0	Ia-IA	0	Ic-IC	0	0	0
01	11	00	01	00	01	11	00	00	IA-Ib	0	0	IB-Ic	0	Ic	0	0	0
01	11	00	01	00	01	00	00	11	IA-Ib	0	0	-IA-Ic	0	Ic-IC	0	0	0
01	00	00	01	00	00	11	10	11	IA	0	0	IB	0	0	0	-Ib	0
01	00	00	01	11	00	00	10	11	IA	0	0	Ia-IA	0	0	0	Ic-IC	0
01	11	00	01	00	00	00	10	11	Ia-IB	0	0	IB	0	0	0	Ic-IC	0
01	00	00	00	00	01	11	10	11	IA	0	0	0	0	IB	0	-Ib	0
01	00	00	00	11	01	11	10	00	IA	0	0	0	0	Ic	0	Ia+IB	0
01	11	00	00	00	01	00	10	11	Ia	0	0	0	0	IB	0	Ic+IA	0
01	11	00	00	11	01	00	10	00	Ia	0	0	0	0	Ic	0	-IC	0
00	00	01	01	11	01	11	00	00	0	0	IA	Ia-IC	0	Ic-IA	0	0	0
00	00	01	01	11	01	00	00	11	0	0	IA	Ia	0	IB+Ic	0	0	0
00	11	01	01	00	01	11	00	00	0	0	IA-Ib	Ia-IC	0	-IA-Ia	0	0	0
00	11	01	01	00	01	00	00	11	0	0	IA-Ib	Ia	0	IB-Ia	0	0	0
00	00	01	01	00	00	11	10	11	0	0	IA	IB	0	0	0	-Ib	0
00	00	01	01	11	00	00	10	11	0	0	IA	Ia	0	0	0	Ic+IB	0
00	11	01	01	00	00	11	10	00	0	0	Ic	IB	0	0	0	Ia+IA	0
00	11	01	01	11	00	00	10	00	0	0	Ic	Ia	0	0	0	-IC	0
00	00	01	00	00	01	11	10	11	0	0	IA	0	0	IB	0	-Ib	0
00	00	01	00	11	01	11	10	00	0	0	IA	0	0	Ic-IA	0	Ia-IC	0
00	11	01	00	00	01	11	10	00	0	0	Ic-IB	0	0	IB	0	Ia-IC	0
00	11	00	01	00	01	11	10	00	0	0	0	IB-Ic	0	Ic	0	IA-Ib	0
00	11	00	01	00	01	00	10	11	0	0	0	Ia	0	IB-Ia	0	IA-Ib	0
00	11	00	01	11	01	00	10	00	0	0	0	Ia	0	Ic	0	-IC	0
employ four capacitors																	
01	11	01	01	00	00	00	10	00	Ia-IB	0	Ic	IB	0	0	0	-IC	0
01	00	01	01	00	00	11	10	00	IA-Ic	0	Ic	IB	0	0	0	-Ib	0
01	00	01	01	00	00	00	10	11	Ia-IB	0	-Ia-IC	IB	0	0	0	-Ib	0
01	00	01	01	11	00	00	10	00	IA-Ic	0	Ic	-IA-Ib	0	0	0	-IC	0
01	11	01	00	00	01	00	10	00	Ia	0	Ic-IB	0	0	IB	0	-IC	0
01	00	01	00	00	01	11	10	00	-Ic-IC	0	Ic-IB	0	0	IB	0	-Ib	0
01	00	01	00	00	01	00	10	11	Ia	0	IA-Ia	0	0	IB	0	-Ib	0
01	00	01	00	11	01	00	10	00	Ia	0	IA-Ia	0	0	-IA-Ib	0	-IC	0
01	00	00	01	00	01	11	10	00	IA	0	0	IB-Ic	0	Ic	0	-Ib	0
01	00	00	01	00	01	00	10	11	IA	0	0	Ia-IA	0	-Ia-IC	0	-Ib	0
01	00	00	01	11	01	00	10	00	IA	0	0	Ia-IA	0	Ic	0	-IC	0
01	11	00	01	00	01	00	10	00	-IB-Ib	0	0	IB-Ic	0	Ic	0	-IC	0
00	00	01	01	00	01	11	10	00	0	0	IA	-Ic-IC	0	Ic-IA	0	-Ib	0
00	00	01	01	00	01	00	10	11	0	0	IA	Ia	0	IB-Ia	0	-Ib	0
00	00	01	01	11	01	00	10	00	0	0	IA	Ia	0	Ic-IA	0	-IC	0
00	11	01	01	00	01	00	10	00	0	0	-IB-Ib	Ia	0	IB-Ia	0	-IC	0

Table B.18: Switching device combinations for (V_{AB},V_{BC},V_{CA}) = (0,+V_{cap},−V_{cap}) and (V_{ab},V_{bc},V_{ca}) = (−V_{cap},0,+V_{cap}).

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
employ single capacitor																	
01	11	11	00	11	00	11	00	00	Ia-IC	0	0	0	0	0	0	0	0
01	11	11	00	00	11	11	00	00	Ia-IC	0	0	0	0	0	0	0	0
01	11	00	00	11	11	11	00	00	Ia-IC	0	0	0	0	0	0	0	0
01	00	11	00	11	11	11	00	00	Ia-IC	0	0	0	0	0	0	0	0
00	11	00	01	11	11	11	00	00	0	0	0	Ia-IC	0	0	0	0	0
00	00	11	01	11	11	11	00	00	0	0	0	Ia-IC	0	0	0	0	0
00	11	11	01	11	00	11	00	00	0	0	0	Ia-IC	0	0	0	0	0
00	11	11	01	00	11	11	00	00	0	0	0	Ia-IC	0	0	0	0	0
00	11	00	00	11	11	11	10	00	0	0	0	0	0	0	0	Ia-IC	0
00	00	11	00	11	11	11	10	00	0	0	0	0	0	0	0	Ia-IC	0
00	11	11	00	11	00	11	10	00	0	0	0	0	0	0	0	Ia-IC	0
00	11	11	00	00	11	11	10	00	0	0	0	0	0	0	0	Ia-IC	0
00	11	00	00	11	11	11	00	10	0	0	0	0	0	0	0	0	Ia-IC
00	00	11	00	11	11	11	00	10	0	0	0	0	0	0	0	0	Ia-IC
00	11	11	00	11	00	11	00	10	0	0	0	0	0	0	0	0	Ia-IC
00	11	11	00	00	11	11	00	10	0	0	0	0	0	0	0	0	Ia-IC
employ two capacitors																	
01	11	11	01	00	00	11	00	00	IA+Ia	0	0	IB	0	0	0	0	0
01	00	00	01	11	11	11	00	00	IA	0	0	IB+Ia	0	0	0	0	0
01	11	00	01	00	11	11	00	00	IA-Ib	0	0	IB-Ic	0	0	0	0	0
01	00	11	01	11	00	11	00	00	IA-Ic	0	0	IB-Ib	0	0	0	0	0
01	00	00	00	11	11	11	10	00	IA	0	0	0	0	0	0	IB+Ia	0
01	11	11	00	11	00	00	10	00	Ia	0	0	0	0	0	0	-IC	0
01	11	11	00	00	11	00	10	00	Ia	0	0	0	0	0	0	-IC	0
01	00	11	00	11	00	11	10	00	IA-Ic	0	0	0	0	0	0	IB-Ib	0
01	00	11	00	00	11	11	10	00	-Ic-IC	0	0	0	0	0	0	-Ib	0
01	11	00	00	11	11	00	10	00	Ia	0	0	0	0	0	0	-IC	0
01	00	11	00	11	11	00	10	00	Ia	0	0	0	0	0	0	-IC	0
01	00	00	00	11	11	11	00	10	IA	0	0	0	0	0	0	0	Ia+IB
01	11	11	00	11	00	00	00	10	Ia	0	0	0	0	0	0	0	-IC
01	11	11	00	00	11	00	00	10	Ia	0	0	0	0	0	0	0	-IC
01	11	00	00	11	00	11	00	10	-Ib-IC	0	0	0	0	0	0	0	-Ic
01	11	00	00	00	11	11	00	10	IA-Ib	0	0	0	0	0	0	0	IB-Ic
01	11	00	00	11	11	00	00	10	Ia	0	0	0	0	0	0	0	-IC
01	00	11	00	11	11	00	00	10	Ia	0	0	0	0	0	0	0	-IC
00	11	00	01	00	11	11	10	00	0	0	0	IB-Ic	0	0	0	IA-Ib	0
00	00	11	01	00	11	11	10	00	0	0	0	-IC-Ic	0	0	0	-Ib	0
00	11	11	01	00	00	11	10	00	0	0	0	IB	0	0	0	Ia+IA	0
00	11	00	01	11	11	00	10	00	0	0	0	Ia	0	0	0	-IC	0
00	00	11	01	11	11	00	10	00	0	0	0	Ia	0	0	0	-IC	0
00	11	11	01	11	00	00	10	00	0	0	0	Ia	0	0	0	-IC	0

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
00	11	11	01	00	11	00	10	00	0	0	0	Ia	0	0	0	-IC	0
00	11	00	01	11	00	11	00	10	0	0	0	-IC-Ib	0	0	0	0	-Ic
00	00	11	01	11	00	11	00	10	0	0	0	IB-Ib	0	0	0	0	IA-Ic
00	11	11	01	00	00	11	00	10	0	0	0	IB	0	0	0	0	Ia+IA
00	11	00	01	11	11	00	00	10	0	0	0	Ia	0	0	0	0	-IC
00	00	11	01	11	11	00	00	10	0	0	0	Ia	0	0	0	0	-IC
00	11	11	01	11	00	00	00	10	0	0	0	Ia	0	0	0	0	-IC
00	11	11	01	00	11	00	00	10	0	0	0	Ia	0	0	0	0	-IC
00	11	00	00	11	00	11	10	10	0	0	0	0	0	0	0	-Ib-IC	-Ic
00	11	00	00	00	11	11	10	10	0	0	0	0	0	0	0	IA-Ib	IB-Ic
00	00	11	00	11	00	11	10	10	0	0	0	0	0	0	0	IB-Ib	IA-Ic
00	00	11	00	00	11	11	10	10	0	0	0	0	0	0	0	-Ib	-Ic-IC
employ three capacitors																	
01	00	00	01	00	11	11	10	00	IA	0	0	IB-Ic	0	0	0	-Ib	0
01	11	11	01	00	00	00	10	00	Ia-IB	0	0	IB	0	0	0	-IC	0
01	00	11	01	00	00	11	10	00	IA-Ic	0	0	IB	0	0	0	-Ib	0
01	00	00	01	11	11	00	10	00	IA	0	0	Ia-IA	0	0	0	-IC	0
01	11	00	01	00	11	00	10	00	-IB-Ib	0	0	IB-Ic	0	0	0	-IC	0
01	00	11	01	11	00	00	10	00	IA-Ic	0	0	-IA-Ib	0	0	0	-IC	0
01	00	00	01	11	00	11	00	10	IA	0	0	IB-Ib	0	0	0	0	-Ic
01	11	11	01	00	00	00	00	10	Ia-IB	0	0	IB	0	0	0	0	-IC
01	11	00	01	00	00	11	00	10	IA-Ib	0	0	IB	0	0	0	0	-Ic
01	00	00	01	11	11	00	00	10	IA	0	0	Ia-IA	0	0	0	0	-IC
01	11	00	01	00	11	00	00	10	IA-Ib	0	0	-IA-Ic	0	0	0	0	-IC
01	00	11	01	11	00	00	00	10	-IB-Ic	0	0	IB-Ib	0	0	0	0	-IC
01	00	00	00	11	00	11	10	10	IA	0	0	0	0	0	0	IB-Ib	-Ic
01	00	00	00	00	11	11	10	10	IA	0	0	0	0	0	0	-Ib	IB-Ic
01	11	00	00	11	00	00	10	10	Ia	0	0	0	0	0	0	Ic-IC	-Ic
01	00	11	00	11	00	00	10	10	Ia	0	0	0	0	0	0	IB-Ib	Ib+IA
01	11	00	00	00	11	00	10	10	Ia	0	0	0	0	0	0	Ic+IA	IB-Ic
01	00	11	00	00	11	00	10	10	Ia	0	0	0	0	0	0	-Ib	Ib-IC
00	11	00	01	00	00	11	10	10	0	0	0	IB	0	0	0	IA-Ib	-Ic
00	00	11	01	00	00	11	10	10	0	0	0	IB	0	0	0	-Ib	IA-Ic
00	11	00	01	11	00	00	10	10	0	0	0	Ia	0	0	0	Ic-IC	-Ic
00	11	00	01	00	11	00	10	10	0	0	0	Ia	0	0	0	IA-Ib	Ib+IB
00	00	11	01	11	00	00	10	10	0	0	0	Ia	0	0	0	Ic+IB	IA-Ic
00	00	11	01	00	11	00	10	10	0	0	0	Ia	0	0	0	-Ib	Ib-IC
employ four capacitors																	
01	00	00	01	00	00	11	10	10	IA	0	0	IB	0	0	0	-Ib	-Ic
01	00	00	01	11	00	00	10	10	IA	0	0	Ia-IA	0	0	0	Ic-IC	-Ic
01	00	00	01	00	11	00	10	10	IA	0	0	Ia-IA	0	0	0	-Ib	Ib-IC
01	11	00	01	00	00	00	10	10	Ia-IB	0	0	IB	0	0	0	Ic-IC	-Ic
01	00	11	01	00	00	00	10	10	Ia-IB	0	0	IB	0	0	0	-Ib	Ib-IC

Table B.19: Switching device combinations for (V_{AB},V_{BC},V_{CA}) = (0,+V_{cap},−V_{cap}) and (V_{ab},V_{bc},V_{ca}) = (0,−V_{cap},+V_{cap}).

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
employ single capacitor																	
01	00	11	00	00	11	11	11	00	-IC-Ic	0	0	0	0	0	0	0	0
00	01	11	00	00	11	11	11	00	0	-IC-Ic	0	0	0	0	0	0	0
00	00	11	01	00	11	11	11	00	0	0	0	-IC-Ic	0	0	0	0	0
00	00	11	00	01	11	11	11	00	0	0	0	0	-IC-Ic	0	0	0	0
00	00	11	00	00	11	11	11	10	0	0	0	0	0	0	0	0	-IC-Ic
employ two capacitors																	
01	01	11	00	00	11	11	00	00	Ia-IC	Ib	0	0	0	0	0	0	0
01	01	11	00	00	11	00	11	00	Ia	Ib-IC	0	0	0	0	0	0	0
01	00	00	01	00	11	11	11	00	IA	0	0	IB-Ic	0	0	0	0	0
01	00	11	01	00	00	11	11	00	IA-Ic	0	0	IB	0	0	0	0	0
01	00	00	00	01	11	11	11	00	IA	0	0	0	IB-Ic	0	0	0	0
01	00	11	00	01	00	11	11	00	IA-Ic	0	0	0	IB	0	0	0	0
01	00	11	00	01	11	11	00	00	Ia-IC	0	0	0	Ib	0	0	0	0
01	00	11	00	01	11	00	11	00	Ia	0	0	0	Ib-IC	0	0	0	0
01	00	00	00	00	11	11	11	10	IA	0	0	0	0	0	0	0	IB-Ic
01	00	11	00	00	11	00	11	10	Ia	0	0	0	0	0	0	0	Ib-IC
00	01	00	01	00	11	11	11	00	0	IA	0	IB-Ic	0	0	0	0	0
00	01	11	01	00	00	11	11	00	0	IA-Ic	0	IB	0	0	0	0	0
00	01	11	01	00	11	11	00	00	0	Ib	0	Ia-IC	0	0	0	0	0
00	01	11	01	00	11	00	11	00	0	Ib-IC	0	Ia	0	0	0	0	0
00	01	00	00	01	11	11	11	00	0	IA	0	0	IB-Ic	0	0	0	0
00	01	11	00	01	00	11	11	00	0	IA-Ic	0	0	IB	0	0	0	0
00	01	00	00	00	11	11	11	10	0	IA	0	0	0	0	0	0	IB-Ic
00	01	11	00	00	11	11	00	10	0	Ib	0	0	0	0	0	0	Ia-IC
00	00	11	01	01	11	11	00	00	0	0	0	Ia-IC	Ib	0	0	0	0
00	00	11	01	01	11	00	11	00	0	0	0	Ia	Ib-IC	0	0	0	0
00	00	11	01	00	00	11	11	10	0	0	0	IB	0	0	0	0	IA-Ic
00	00	11	01	00	11	00	11	10	0	0	0	Ia	0	0	0	0	Ib-IC
00	00	11	00	01	00	11	11	10	0	0	0	0	IB	0	0	0	IA-Ic
00	00	11	00	01	11	11	00	10	0	0	0	0	Ib	0	0	0	Ia-IC
employ three capacitors																	
01	01	11	01	00	00	11	00	00	IA+Ia	Ib	0	IB	0	0	0	0	0
01	01	11	01	00	00	00	11	00	Ia-IB	Ib-IC	0	IB	0	0	0	0	0
01	01	00	01	00	11	11	00	00	IA-Ib	Ib	0	IB-Ic	0	0	0	0	0
01	01	00	01	00	11	00	11	00	-IB-Ib	Ib-IC	0	IB-Ic	0	0	0	0	0
01	01	11	00	01	00	11	00	00	Ia-IC	Ib-IB	0	0	IB	0	0	0	0
01	01	11	00	01	00	00	11	00	Ia	IA+Ib	0	0	IB	0	0	0	0
01	01	00	00	01	11	11	00	00	Ia-IC	-IB-Ia	0	0	IB-Ic	0	0	0	0
01	01	00	00	01	11	00	11	00	Ia	IA-Ia	0	0	IB-Ic	0	0	0	0
01	01	11	00	00	11	00	00	10	Ia	Ib	0	0	0	0	0	0	-IC

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
01	01	00	00	00	11	11	00	10	IA-Ib	Ib	0	0	0	0	0	0	IB-Ic
01	01	00	00	00	11	00	11	10	Ia	IA-Ia	0	0	0	0	0	0	IB-Ic
01	00	00	01	01	11	11	00	00	IA	0	0	IB+Ia	Ib	0	0	0	0
01	00	00	01	01	11	00	11	00	IA	0	0	Ia-IA	Ib-IC	0	0	0	0
01	00	11	01	01	00	11	00	00	IA-Ic	0	0	IB-Ib	Ib	0	0	0	0
01	00	11	01	01	00	00	11	00	IA-Ic	0	0	-IA-Ib	Ib-IC	0	0	0	0
01	00	00	01	00	00	11	11	10	IA	0	0	IB	0	0	0	0	-Ic
01	00	00	01	00	11	00	11	10	IA	0	0	Ia-IA	0	0	0	0	Ib-IC
01	00	11	01	00	00	00	11	10	Ia-IB	0	0	IB	0	0	0	0	Ib-IC
01	00	00	00	01	00	11	11	10	IA	0	0	0	IB	0	0	0	-Ic
01	00	00	00	01	11	11	00	10	IA	0	0	0	Ib	0	0	0	Ia+IB
01	00	11	00	01	00	00	11	10	Ia	0	0	0	IB	0	0	0	Ib+IA
01	00	11	00	01	11	00	00	10	Ia	0	0	0	Ib	0	0	0	-IC
00	01	00	01	01	11	11	00	00	0	IA	0	Ia-IC	Ib-IA	0	0	0	0
00	01	00	01	01	11	00	11	00	0	IA	0	Ia	IB+Ib	0	0	0	0
00	01	11	01	01	00	11	00	00	0	IA-Ic	0	Ia-IC	-IA-Ia	0	0	0	0
00	01	11	01	01	00	00	11	00	0	IA-Ic	0	Ia	IB-Ia	0	0	0	0
00	01	00	01	00	00	11	11	10	0	IA	0	IB	0	0	0	0	-Ic
00	01	00	01	00	11	00	11	10	0	IA	0	Ia	0	0	0	0	Ib+IB
00	01	11	01	00	00	11	00	10	0	Ib	0	IB	0	0	0	0	Ia+IA
00	01	11	01	00	11	00	00	10	0	Ib	0	Ia	0	0	0	0	-IC
00	01	00	00	01	00	11	11	10	0	IA	0	0	IB	0	0	0	-Ic
00	01	00	00	01	11	11	00	10	0	IA	0	0	Ib-IA	0	0	0	Ia-IC
00	01	11	00	01	00	11	00	10	0	Ib-IB	0	0	IB	0	0	0	Ia-IC
00	00	11	01	01	00	11	00	10	0	0	0	IB-Ib	Ib	0	0	0	IA-Ic
00	00	11	01	01	00	00	11	10	0	0	0	Ia	IB-Ia	0	0	0	IA-Ic
00	00	11	01	01	11	00	00	10	0	0	0	Ia	Ib	0	0	0	-IC
employ three capacitors																	
01	01	11	01	00	00	00	00	10	Ia-IB	Ib	0	IB	0	0	0	0	-IC
01	01	00	01	00	00	11	00	10	IA-Ib	Ib	0	IB	0	0	0	0	-Ic
01	01	00	01	00	00	00	11	10	Ia-IB	-Ia-IC	0	IB	0	0	0	0	-Ic
01	01	00	01	00	11	00	00	10	IA-Ib	Ib	0	-IA-Ic	0	0	0	0	-IC
01	01	11	00	01	00	00	00	10	Ia	Ib-IB	0	0	IB	0	0	0	-IC
01	01	00	00	01	00	11	00	10	-Ib-IC	Ib-IB	0	0	IB	0	0	0	-Ic
01	01	00	00	01	00	00	11	10	Ia	IA-Ia	0	0	IB	0	0	0	-Ic
01	01	00	00	01	11	00	00	10	Ia	IA-Ia	0	0	-IA-Ic	0	0	0	-IC
01	00	00	01	01	00	11	00	10	IA	0	0	IB-Ib	Ib	0	0	0	-Ic
01	00	00	01	01	00	00	11	10	IA	0	0	Ia-IA	-Ia-IC	0	0	0	-Ic
01	00	00	01	01	11	00	00	10	IA	0	0	Ia-IA	Ib	0	0	0	-IC
01	00	11	01	01	00	00	00	10	-IB-Ic	0	0	IB-Ib	Ib	0	0	0	-IC
00	01	00	01	01	00	11	00	10	0	IA	0	-Ib-IC	Ib-IA	0	0	0	-Ic
00	01	00	01	01	00	00	11	10	0	IA	0	Ia	IB-Ia	0	0	0	-Ic
00	01	00	01	01	11	00	00	10	0	IA	0	Ia	Ib-IA	0	0	0	-IC
00	01	11	01	01	00	00	00	10	0	-IB-Ic	0	Ia	IB-Ia	0	0	0	-IC

Table B.20: Switching device combinations for (V_{AB},V_{BC},V_{CA}) = (0,+V_{cap},−V_{cap}) and (V_{ab},V_{bc},V_{ca}) = (+V_{cap},−V_{cap},0).

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
employ single capacitor																	
11	01	11	11	00	00	00	11	00	0	Ib-IC	0	0	0	0	0	0	0
11	01	11	00	00	11	00	11	00	0	Ib-IC	0	0	0	0	0	0	0
11	01	00	11	00	11	00	11	00	0	Ib-IC	0	0	0	0	0	0	0
00	01	11	11	00	11	00	11	00	0	Ib-IC	0	0	0	0	0	0	0
11	00	00	11	01	11	00	11	00	0	0	0	0	Ib-IC	0	0	0	0
00	00	11	11	01	11	00	11	00	0	0	0	0	Ib-IC	0	0	0	0
11	00	11	11	01	00	00	11	00	0	0	0	0	Ib-IC	0	0	0	0
11	00	11	00	01	11	00	11	00	0	0	0	0	Ib-IC	0	0	0	0
11	00	00	11	00	11	10	11	00	0	0	0	0	0	0	Ib-IC	0	0
00	00	11	11	00	11	10	11	00	0	0	0	0	0	0	Ib-IC	0	0
11	00	11	11	00	00	10	11	00	0	0	0	0	0	0	Ib-IC	0	0
11	00	11	00	00	11	10	11	00	0	0	0	0	0	0	Ib-IC	0	0
11	00	00	11	00	11	00	11	10	0	0	0	0	0	0	0	0	Ib-IC
00	00	11	11	00	11	00	11	10	0	0	0	0	0	0	0	0	Ib-IC
11	00	11	11	00	00	00	11	10	0	0	0	0	0	0	0	0	Ib-IC
11	00	11	00	00	11	00	11	10	0	0	0	0	0	0	0	0	Ib-IC
employ two capacitors																	
11	01	11	00	01	00	00	11	00	0	IA+Ib	0	0	IB	0	0	0	0
00	01	00	11	01	11	00	11	00	0	IA	0	0	IB+Ib	0	0	0	0
11	01	00	00	01	11	00	11	00	0	IA-Ia	0	0	IB-Ic	0	0	0	0
00	01	11	11	01	00	00	11	00	0	IA-Ic	0	0	IB-Ia	0	0	0	0
00	01	00	11	00	11	10	11	00	0	IA	0	0	0	0	Ib+IB	0	0
11	01	11	11	00	00	10	00	00	0	Ib	0	0	0	0	-IC	0	0
11	01	11	00	00	11	10	00	00	0	Ib	0	0	0	0	-IC	0	0
00	01	11	11	00	00	10	11	00	0	IA-Ic	0	0	0	0	IB-Ia	0	0
00	01	11	00	00	11	10	11	00	0	-Ic-IC	0	0	0	0	-Ia	0	0
11	01	00	11	00	11	10	00	00	0	Ib	0	0	0	0	-IC	0	0
00	01	11	11	00	11	10	00	00	0	Ib	0	0	0	0	-IC	0	0
00	01	00	11	00	11	00	11	10	0	IA	0	0	0	0	0	0	Ib+IB
11	01	11	11	00	00	00	00	10	0	Ib	0	0	0	0	0	0	-IC
11	01	11	00	00	11	00	00	10	0	Ib	0	0	0	0	0	0	-IC
11	01	00	11	00	00	00	11	10	0	-Ia-IC	0	0	0	0	0	0	-Ic
11	01	00	00	00	11	00	11	10	0	IA-Ia	0	0	0	0	0	0	IB-Ic
11	01	00	11	00	11	00	00	10	0	Ib	0	0	0	0	0	0	-IC
00	01	11	11	00	11	00	00	10	0	Ib	0	0	0	0	0	0	-IC
11	00	00	00	01	11	10	11	00	0	0	0	0	IB-Ic	0	IA-Ia	0	0
00	00	11	00	01	11	10	11	00	0	0	0	0	-Ic-IC	0	-Ia	0	0
11	00	11	00	01	00	10	11	00	0	0	0	0	IB	0	Ib+IA	0	0
11	00	00	11	01	11	10	00	00	0	0	0	0	Ib	0	-IC	0	0
00	00	11	11	01	11	10	00	00	0	0	0	0	Ib	0	-IC	0	0
11	00	11	11	01	00	10	00	00	0	0	0	0	Ib	0	-IC	0	0

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
11	00	11	00	01	11	10	00	00	0	0	0	0	Ib	0	-IC	0	0
11	00	00	11	01	00	00	11	10	0	0	0	0	-Ia-IC	0	0	0	-Ic
00	00	11	11	01	00	00	11	10	0	0	0	0	IB-Ia	0	0	0	IA-Ic
11	00	11	00	01	00	00	11	10	0	0	0	0	IB	0	0	0	Ib+IA
11	00	00	11	01	11	00	00	10	0	0	0	0	Ib	0	0	0	-IC
00	00	11	11	01	11	00	00	10	0	0	0	0	Ib	0	0	0	-IC
11	00	11	11	01	00	00	00	10	0	0	0	0	Ib	0	0	0	-IC
11	00	11	00	01	11	00	00	10	0	0	0	0	Ib	0	0	0	-IC
11	00	00	11	00	00	10	11	10	0	0	0	0	0	0	-Ia-IC	0	-Ic
11	00	00	00	00	11	10	11	10	0	0	0	0	0	0	IA-Ia	0	IB-Ic
00	00	11	11	00	00	10	11	10	0	0	0	0	0	0	IB-Ia	0	IA-Ic
00	00	11	00	00	11	10	11	10	0	0	0	0	0	0	-Ia	0	-Ic-IC
employ three capacitors																	
00	01	00	00	01	11	10	11	00	0	IA	0	0	IB-Ic	0	-Ia	0	0
11	01	11	00	01	00	10	00	00	0	Ib-IB	0	0	IB	0	-IC	0	0
00	01	11	00	01	00	10	11	00	0	IA-Ic	0	0	IB	0	-Ia	0	0
00	01	00	11	01	11	10	00	00	0	IA	0	0	Ib-IA	0	-IC	0	0
11	01	00	00	01	11	10	00	00	0	-IB-Ia	0	0	IB-Ic	0	-IC	0	0
00	01	11	11	01	00	10	00	00	0	IA-Ic	0	0	-IA-Ia	0	-IC	0	0
00	01	00	11	01	00	00	11	10	0	IA	0	0	IB-Ia	0	0	0	-Ic
11	01	11	00	01	00	00	00	10	0	Ib-IB	0	0	IB	0	0	0	-IC
11	01	00	00	01	00	00	11	10	0	IA-Ia	0	0	IB	0	0	0	-Ic
00	01	00	11	01	11	00	00	10	0	IA	0	0	Ib-IA	0	0	0	-IC
11	01	00	00	01	11	00	00	10	0	IA-Ia	0	0	-IA-Ic	0	0	0	-IC
00	01	11	11	01	00	00	00	10	0	-IB-Ic	0	0	IB-Ia	0	0	0	-IC
00	01	00	11	00	00	10	11	10	0	IA	0	0	0	0	IB-Ia	0	-Ic
00	01	00	00	00	11	10	11	10	0	IA	0	0	0	0	-Ia	0	IB-Ic
11	01	00	11	00	00	10	00	10	0	Ib	0	0	0	0	Ic-IC	0	-Ic
00	01	11	11	00	00	10	00	10	0	Ib	0	0	0	0	IB-Ia	0	Ia+IA
11	01	00	00	00	11	10	00	10	0	Ib	0	0	0	0	Ic+IA	0	IB-Ic
00	01	11	00	00	11	10	00	10	0	Ib	0	0	0	0	-Ia	0	Ia-IC
11	00	00	00	01	00	10	11	10	0	0	0	0	IB	0	IA-Ia	0	-Ic
00	00	11	00	01	00	10	11	10	0	0	0	0	IB	0	-Ia	0	IA-Ic
11	00	00	11	01	00	10	00	10	0	0	0	0	Ib	0	Ic-IC	0	-Ic
11	00	00	00	01	11	10	00	10	0	0	0	0	Ib	0	IA-Ia	0	Ia+IB
00	00	11	11	01	00	10	00	10	0	0	0	0	Ib	0	Ic+IB	0	IA-Ic
00	00	11	00	01	11	10	00	10	0	0	0	0	Ib	0	-Ia	0	Ia-IC
employ four capacitors																	
00	01	00	00	01	00	10	11	10	0	IA	0	0	IB	0	-Ia	0	-Ic
00	01	00	11	01	00	10	00	10	0	IA	0	0	Ib-IA	0	Ic-IC	0	-Ic
00	01	00	00	01	11	10	00	10	0	IA	0	0	Ib-IA	0	-Ia	0	Ia-IC
11	01	00	00	01	00	10	00	10	0	Ib-IB	0	0	IB	0	Ic-IC	0	-Ic
00	01	11	00	01	00	10	00	10	0	Ib-IB	0	0	IB	0	-Ia	0	Ia-IC

Table B.21: Switching device combinations for (V_{AB},V_{BC},V_{CA}) = ($-V_{cap}$,$+V_{cap}$,0) and (V_{ab},V_{bc},V_{ca}) = (0,0,0).

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
employ single capacitor																	
11	00	00	01	00	00	11	11	11	0	0	0	IB	0	0	0	0	0
00	11	00	01	00	00	11	11	11	0	0	0	IB	0	0	0	0	0
00	00	11	01	00	00	11	11	11	0	0	0	IB	0	0	0	0	0
11	11	11	01	00	00	11	00	00	0	0	0	IB	0	0	0	0	0
11	11	11	01	00	00	00	11	00	0	0	0	IB	0	0	0	0	0
11	11	11	01	00	00	00	00	11	0	0	0	IB	0	0	0	0	0
11	00	11	01	00	00	11	11	00	0	0	0	IB	0	0	0	0	0
00	11	11	01	00	00	11	11	00	0	0	0	IB	0	0	0	0	0
11	11	00	01	00	00	11	00	11	0	0	0	IB	0	0	0	0	0
00	11	11	01	00	00	11	00	11	0	0	0	IB	0	0	0	0	0
11	11	00	01	00	00	00	11	11	0	0	0	IB	0	0	0	0	0
11	00	11	01	00	00	00	11	11	0	0	0	IB	0	0	0	0	0
11	00	00	00	01	00	11	11	11	0	0	0	0	IB	0	0	0	0
00	11	00	00	01	00	11	11	11	0	0	0	0	IB	0	0	0	0
00	00	11	00	01	00	11	11	11	0	0	0	0	IB	0	0	0	0
11	11	11	00	01	00	11	00	00	0	0	0	0	IB	0	0	0	0
11	11	11	00	01	00	00	11	00	0	0	0	0	IB	0	0	0	0
11	11	11	00	01	00	00	00	11	0	0	0	0	IB	0	0	0	0
11	00	11	00	01	00	11	11	00	0	0	0	0	IB	0	0	0	0
00	11	11	00	01	00	11	11	00	0	0	0	0	IB	0	0	0	0
11	11	00	00	01	00	11	00	11	0	0	0	0	IB	0	0	0	0
00	11	11	00	01	00	11	00	11	0	0	0	0	IB	0	0	0	0
11	11	00	00	01	00	00	11	11	0	0	0	0	IB	0	0	0	0
11	00	11	00	01	00	00	11	11	0	0	0	0	IB	0	0	0	0
11	00	00	00	00	01	11	11	11	0	0	0	0	0	IB	0	0	0
00	11	00	00	00	01	11	11	11	0	0	0	0	0	IB	0	0	0
00	00	11	00	00	01	11	11	11	0	0	0	0	0	IB	0	0	0
11	11	11	00	00	01	11	00	00	0	0	0	0	0	IB	0	0	0
11	11	11	00	00	01	00	11	00	0	0	0	0	0	IB	0	0	0
11	11	11	00	00	01	00	00	11	0	0	0	0	0	IB	0	0	0
11	00	11	00	00	01	11	11	00	0	0	0	0	0	IB	0	0	0
00	11	11	00	00	01	11	11	00	0	0	0	0	0	IB	0	0	0
11	11	00	00	00	01	11	00	11	0	0	0	0	0	IB	0	0	0
00	11	11	00	00	01	11	00	11	0	0	0	0	0	IB	0	0	0
11	11	00	00	00	01	00	11	11	0	0	0	0	0	IB	0	0	0
11	00	11	00	00	01	00	11	11	0	0	0	0	0	IB	0	0	0
employ two capacitors																	
10	00	00	11	11	11	10	00	00	-IA	0	0	0	0	0	-IC	0	0
10	00	00	11	11	11	00	10	00	-IA	0	0	0	0	0	0	-IC	0
10	00	00	11	11	11	00	00	10	-IA	0	0	0	0	0	0	0	-IC
00	10	00	11	11	11	10	00	00	0	-IA	0	0	0	0	-IC	0	0

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
00	10	00	11	11	11	00	10	00	0	-IA	0	0	0	0	0	-IC	0
00	10	00	11	11	11	00	00	10	0	-IA	0	0	0	0	0	0	-IC
00	00	10	11	11	11	10	00	00	0	0	-IA	0	0	0	-IC	0	0
00	00	10	11	11	11	00	10	00	0	0	-IA	0	0	0	0	-IC	0
00	00	10	11	11	11	00	00	10	0	0	-IA	0	0	0	0	0	-IC
11	00	00	01	01	00	11	00	11	0	0	0	IB-Ib	Ib	0	0	0	0
11	00	00	01	01	00	00	11	11	0	0	0	Ia-IA	-IC-Ia	0	0	0	0
00	11	00	01	01	00	11	00	11	0	0	0	-IC-Ib	Ib-IA	0	0	0	0
00	11	00	01	01	00	00	11	11	0	0	0	Ia	IB-Ia	0	0	0	0
00	00	11	01	01	00	11	00	11	0	0	0	IB-Ib	Ib	0	0	0	0
00	00	11	01	01	00	00	11	11	0	0	0	Ia	IB-Ia	0	0	0	0
11	00	11	01	01	00	11	00	00	0	0	0	IB-Ib	Ib	0	0	0	0
00	11	11	01	01	00	11	00	00	0	0	0	Ia-IC	-IA-Ia	0	0	0	0
11	00	11	01	01	00	00	11	00	0	0	0	-IA-Ib	Ib-IC	0	0	0	0
00	11	11	01	01	00	00	11	00	0	0	0	Ia	IB-Ia	0	0	0	0
11	00	11	01	01	00	00	00	11	0	0	0	IB-Ib	Ib	0	0	0	0
00	11	11	01	01	00	00	00	11	0	0	0	Ia	IB-Ia	0	0	0	0
11	00	00	01	00	01	11	11	00	0	0	0	IB-Ic	0	Ic	0	0	0
11	00	00	01	00	01	00	11	11	0	0	0	Ia-IA	0	-IC-Ia	0	0	0
00	11	00	01	00	01	11	11	00	0	0	0	IB-Ic	0	Ic	0	0	0
00	11	00	01	00	01	00	11	11	0	0	0	Ia	0	IB-Ia	0	0	0
00	00	11	01	00	01	11	11	00	0	0	0	-IC-Ic	0	Ic-IA	0	0	0
00	00	11	01	00	01	00	11	11	0	0	0	Ia	0	IB-Ia	0	0	0
11	11	00	01	00	01	11	00	00	0	0	0	IB-Ic	0	Ic	0	0	0
00	11	11	01	00	01	11	00	00	0	0	0	Ia-IC	0	-IA-Ia	0	0	0
11	11	00	01	00	01	00	11	00	0	0	0	IB-Ic	0	Ic	0	0	0
00	11	11	01	00	01	00	11	00	0	0	0	Ia	0	IB-Ia	0	0	0
11	11	00	01	00	01	00	00	11	0	0	0	-IA-Ic	0	Ic-IC	0	0	0
00	11	11	01	00	01	00	00	11	0	0	0	Ia	0	IB-Ia	0	0	0
11	00	00	00	01	01	11	11	00	0	0	0	0	IB-Ic	Ic	0	0	0
11	00	00	00	01	01	11	00	11	0	0	0	0	Ib	IB-Ib	0	0	0
00	11	00	00	01	01	11	11	00	0	0	0	0	IB-Ic	Ic	0	0	0
00	11	00	00	01	01	11	00	11	0	0	0	0	Ib-IA	-IC-Ib	0	0	0
00	00	11	00	01	01	11	11	00	0	0	0	0	-IC-Ic	Ic-IA	0	0	0
00	00	11	00	01	01	11	00	11	0	0	0	0	Ib	IB-Ib	0	0	0
11	11	00	00	01	01	11	00	00	0	0	0	0	IB-Ic	Ic	0	0	0
11	00	11	00	01	01	11	00	00	0	0	0	0	Ib	IB-Ib	0	0	0
11	11	00	00	01	01	00	11	00	0	0	0	0	IB-Ic	Ic	0	0	0
11	00	11	00	01	01	00	11	00	0	0	0	0	Ib-IC	-IA-Ib	0	0	0
11	11	00	00	01	01	00	00	11	0	0	0	0	-IA-Ic	Ic-IC	0	0	0
11	00	11	00	01	01	00	00	11	0	0	0	0	Ib	IB-Ib	0	0	0
employ three capacitors																	
10	10	00	11	00	11	10	00	00	Ib-IA	-Ib	0	0	0	0	-IC	0	0
10	10	00	00	11	11	10	00	00	IC-Ia	IB+Ia	0	0	0	0	-IC	0	0
10	10	00	11	00	11	00	10	00	IB+Ib	IC-Ib	0	0	0	0	0	-IC	0

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
10	10	00	00	11	11	00	10	00	-Ia	Ia-IA	0	0	0	0	0	-IC	0
10	10	00	11	00	11	00	00	10	Ib-IA	-Ib	0	0	0	0	0	0	-IC
10	10	00	00	11	11	00	00	10	-Ia	Ia-IA	0	0	0	0	0	0	-IC
10	00	10	11	11	00	10	00	00	Ic-IA	0	-Ic	0	0	0	-IC	0	0
10	00	10	00	11	11	10	00	00	IC-Ia	0	IB+Ia	0	0	0	-IC	0	0
10	00	10	11	11	00	00	10	00	Ic-IA	0	-Ic	0	0	0	0	-IC	0
10	00	10	00	11	11	00	10	00	-Ia	0	Ia-IA	0	0	0	0	-IC	0
10	00	10	11	11	00	00	00	10	IB+Ic	0	IC-Ic	0	0	0	0	0	-IC
10	00	10	00	11	11	00	00	10	-Ia	0	Ia-IA	0	0	0	0	0	-IC
10	00	00	11	00	11	10	10	00	-IA	0	0	0	0	0	Ib-IC	-Ib	0
10	00	00	00	11	11	10	10	00	-IA	0	0	0	0	0	IA-Ia	IB+Ia	0
10	00	00	11	11	00	10	00	10	-IA	0	0	0	0	0	Ic-IC	0	-Ic
10	00	00	00	11	11	10	00	10	-IA	0	0	0	0	0	IA-Ia	0	IB+Ia
10	00	00	11	11	00	00	10	10	-IA	0	0	0	0	0	0	Ic-IC	-Ic
10	00	00	11	00	11	00	10	10	-IA	0	0	0	0	0	0	-Ib	Ib-IC
00	10	10	11	11	00	10	00	00	0	Ic-IA	-Ic	0	0	0	-IC	0	0
00	10	10	11	00	11	10	00	00	0	-Ib	Ib-IA	0	0	0	-IC	0	0
00	10	10	11	11	00	00	10	00	0	Ic-IA	-Ic	0	0	0	0	-IC	0
00	10	10	11	00	11	00	10	00	0	IC-Ib	IB+Ib	0	0	0	0	-IC	0
00	10	10	11	11	00	00	00	10	0	IB+Ic	IC-Ic	0	0	0	0	0	-IC
00	10	10	11	00	11	00	00	10	0	-Ib	Ib-IA	0	0	0	0	0	-IC
00	10	00	11	00	11	10	10	00	0	-IA	0	0	0	0	IB+Ib	IA-Ib	0
00	10	00	00	11	11	10	10	00	0	-IA	0	0	0	0	-Ia	Ia-IC	0
00	10	00	11	11	00	10	00	10	0	-IA	0	0	0	0	Ic-IC	0	-Ic
00	10	00	00	11	11	10	00	10	0	-IA	0	0	0	0	-Ia	0	Ia-IC
00	10	00	11	11	00	00	10	10	0	-IA	0	0	0	0	0	Ic-IC	-Ic
00	10	00	11	00	11	00	10	10	0	-IA	0	0	0	0	0	IA-Ib	IB+Ib
00	00	10	11	00	11	10	10	00	0	0	-IA	0	0	0	Ib-IC	-Ib	0
00	00	10	00	11	11	10	10	00	0	0	-IA	0	0	0	-Ia	Ia-IC	0
00	00	10	11	11	00	10	00	10	0	0	-IA	0	0	0	IB+Ic	0	IA-Ic
00	00	10	00	11	11	10	00	10	0	0	-IA	0	0	0	-Ia	0	Ia-IC
00	00	10	11	11	00	00	10	10	0	0	-IA	0	0	0	0	IB+Ic	IA-Ic
00	00	10	11	00	11	00	10	10	0	0	-IA	0	0	0	0	-Ib	Ib-IC
11	00	00	01	01	01	11	00	00	0	0	0	IB+Ia	Ib	Ic	0	0	0
00	11	00	01	01	01	11	00	00	0	0	0	Ia-IC	Ib-IA	Ic	0	0	0
00	00	11	01	01	01	11	00	00	0	0	0	Ia-IC	Ib	Ic-IA	0	0	0
11	00	00	01	01	01	00	11	00	0	0	0	Ia-IA	Ib-IC	Ic	0	0	0
00	11	00	01	01	01	00	11	00	0	0	0	Ia	IB+Ib	Ic	0	0	0
00	00	11	01	01	01	00	11	00	0	0	0	Ia	Ib-IC	Ic-IA	0	0	0
11	00	00	01	01	01	00	00	11	0	0	0	Ia-IA	Ib	Ic-IC	0	0	0
00	11	00	01	01	01	00	00	11	0	0	0	Ia	Ib-IA	Ic-IC	0	0	0
00	00	11	01	01	01	00	00	11	0	0	0	Ia	Ib	IB+Ic	0	0	0
employ four capacitors																	
10	10	10	11	00	00	10	00	00	-IA-Ia	-Ib	-Ic	0	0	0	-IC	0	0
10	10	10	00	11	00	10	00	00	IC-Ia	IB-Ib	-Ic	0	0	0	-IC	0	0

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
10	10	10	00	00	11	10	00	00	IC-Ia	-Ib	IB-Ic	0	0	0	-IC	0	0
10	10	10	11	00	00	00	10	00	IB-Ia	IC-Ib	-Ic	0	0	0	0	-IC	0
10	10	10	00	11	00	00	10	00	-Ia	-IA-Ib	-Ic	0	0	0	0	-IC	0
10	10	10	00	00	11	00	10	00	-Ia	IC-Ib	IB-Ic	0	0	0	0	-IC	0
10	10	10	11	00	00	00	00	10	IB-Ia	-Ib	IC-Ic	0	0	0	0	0	-IC
10	10	10	00	11	00	00	00	10	-Ia	IB-Ib	IC-Ic	0	0	0	0	0	-IC
10	10	10	00	00	11	00	00	10	-Ia	-Ib	-IA-Ic	0	0	0	0	0	-IC
10	10	00	11	00	00	10	00	10	Ib-IA	-Ib	0	0	0	0	Ic-IC	0	-Ic
10	10	00	00	11	00	10	00	10	IC+Ib	IB-Ib	0	0	0	0	Ic-IC	0	-Ic
10	10	00	00	00	11	10	00	10	-Ib	Ib-IA	0	0	0	0	IA+Ic	0	IB-Ic
10	10	00	11	00	00	00	10	10	IB-Ia	IC+Ia	0	0	0	0	0	Ic-IC	-Ic
10	10	00	00	11	00	00	10	10	-Ia	Ia-IA	0	0	0	0	0	Ic-IC	-Ic
10	10	00	00	00	11	00	10	10	-Ia	Ia-IA	0	0	0	0	0	IA+Ic	IB-Ic
10	00	10	11	00	00	10	10	00	Ic-IA	0	-Ic	0	0	0	Ib-IC	-Ib	0
10	00	10	00	11	00	10	10	00	Ic-IA	0	-Ic	0	0	0	IA+Ib	IB-Ib	0
10	00	10	00	00	11	10	10	00	IC+Ic	0	IB-Ic	0	0	0	Ib-IC	-Ib	0
10	00	10	11	00	00	00	10	10	IB-Ia	0	IC+Ia	0	0	0	0	-Ib	Ib-IC
10	00	10	00	11	00	00	10	10	-Ia	0	Ia-IA	0	0	0	0	IB-Ib	IA+Ib
10	00	10	00	00	11	00	10	10	-Ia	0	Ia-IA	0	0	0	0	-Ib	Ib-IC
10	00	00	11	00	00	10	10	10	-IA	0	0	0	0	0	-IC-Ia	-Ib	-Ic
10	00	00	00	11	00	10	10	10	-IA	0	0	0	0	0	IA-Ia	IB-Ib	-Ic
10	00	00	00	00	11	10	10	10	-IA	0	0	0	0	0	IA-Ia	-Ib	IB-Ic
00	10	10	11	00	00	10	10	00	0	Ic-IA	-Ic	0	0	0	IB-Ia	IA+Ia	0
00	10	10	00	11	00	10	10	00	0	Ic-IA	-Ic	0	0	0	-Ia	Ia-IC	0
00	10	10	00	00	11	10	10	00	0	IC+Ic	IB-Ic	0	0	0	-Ia	Ia-IC	0
00	10	10	11	00	00	10	00	10	0	-Ib	Ib-IA	0	0	0	IB-Ia	0	IA+Ia
00	10	10	00	11	00	10	00	10	0	IB-Ib	IC+Ib	0	0	0	-Ia	0	Ia-IC
00	10	10	00	00	11	10	00	10	0	-Ib	Ib-IA	0	0	0	-Ia	0	Ia-IC
00	10	00	11	00	00	10	10	10	0	-IA	0	0	0	0	IB-Ia	IA-Ib	-Ic
00	10	00	00	11	00	10	10	10	0	-IA	0	0	0	0	-Ia	-IC-Ib	-Ic
00	10	00	00	00	11	10	10	10	0	-IA	0	0	0	0	-Ia	IA-Ib	IB-Ic
00	00	10	11	00	00	10	10	10	0	0	-IA	0	0	0	IB-Ia	-Ib	IA-Ic
00	00	10	00	11	00	10	10	10	0	0	-IA	0	0	0	-Ia	IB-Ib	IA-Ic
00	00	10	00	00	11	10	10	10	0	0	-IA	0	0	0	-Ia	-Ib	-IC-Ic

Table B.22: Switching device combinations for (V_{AB},V_{BC},V_{CA}) = ($-V_{cap}$,$+V_{cap}$,0) and (V_{ab},V_{bc},V_{ca}) = ($+V_{cap}$,0,$-V_{cap}$).

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
employ single capacitor																	
10	11	11	11	00	00	00	11	00	IB-Ia	0	0	0	0	0	0	0	0
10	11	11	11	00	00	00	00	11	IB-Ia	0	0	0	0	0	0	0	0
10	11	00	11	00	00	00	11	11	IB-Ia	0	0	0	0	0	0	0	0
10	00	11	11	00	00	00	11	11	IB-Ia	0	0	0	0	0	0	0	0
00	11	00	11	01	00	00	11	11	0	0	0	0	IB-Ia	0	0	0	0
00	00	11	11	01	00	00	11	11	0	0	0	0	IB-Ia	0	0	0	0
00	11	11	11	01	00	00	11	00	0	0	0	0	IB-Ia	0	0	0	0
00	11	11	11	01	00	00	00	11	0	0	0	0	IB-Ia	0	0	0	0
00	11	00	11	00	01	00	11	11	0	0	0	0	0	IB-Ia	0	0	0
00	00	11	11	00	01	00	11	11	0	0	0	0	0	IB-Ia	0	0	0
00	11	11	11	00	01	00	11	00	0	0	0	0	0	IB-Ia	0	0	0
00	11	11	11	00	01	00	00	11	0	0	0	0	0	IB-Ia	0	0	0
00	11	00	11	00	00	10	11	11	0	0	0	0	0	0	IB-Ia	0	0
00	00	11	11	00	00	10	11	11	0	0	0	0	0	0	IB-Ia	0	0
00	11	11	11	00	00	10	11	00	0	0	0	0	0	0	IB-Ia	0	0
00	11	11	11	00	00	10	00	11	0	0	0	0	0	0	IB-Ia	0	0
employ two capacitors																	
10	00	00	11	01	00	00	11	11	-IA	0	0	0	-IC-Ia	0	0	0	0
10	11	11	00	01	00	00	11	00	-Ia	0	0	0	IB	0	0	0	0
10	11	11	00	01	00	00	00	11	-Ia	0	0	0	IB	0	0	0	0
10	11	00	00	01	00	00	11	11	-Ia	0	0	0	IB	0	0	0	0
10	00	11	00	01	00	00	11	11	-Ia	0	0	0	IB	0	0	0	0
10	00	11	11	01	00	00	11	00	Ic-IA	0	0	0	Ib-IC	0	0	0	0
10	00	11	11	01	00	00	00	11	IB+Ic	0	0	0	Ib	0	0	0	0
10	00	00	11	00	01	00	11	11	-IA	0	0	0	0	-IC-Ia	0	0	0
10	11	11	00	00	01	00	11	00	-Ia	0	0	0	0	IB	0	0	0
10	11	11	00	00	01	00	00	11	-Ia	0	0	0	0	IB	0	0	0
10	11	00	00	00	01	00	11	11	-Ia	0	0	0	0	IB	0	0	0
10	00	11	00	00	01	00	11	11	-Ia	0	0	0	0	IB	0	0	0
10	11	00	11	00	01	00	11	00	IB+Ib	0	0	0	0	Ic	0	0	0
10	11	00	11	00	01	00	00	11	Ib-IA	0	0	0	0	Ic-IC	0	0	0
10	00	00	11	00	00	10	11	11	-IA	0	0	0	0	0	-IC-Ia	0	0
10	11	11	11	00	00	10	00	00	-IA-Ia	0	0	0	0	0	-IC	0	0
10	00	11	11	00	00	10	11	00	Ic-IA	0	0	0	0	0	Ib-IC	0	0
10	11	00	11	00	00	10	00	11	Ib-IA	0	0	0	0	0	Ic-IC	0	0
00	11	00	11	01	01	00	11	00	0	0	0	0	IB+Ib	Ic	0	0	0
00	00	11	11	01	01	00	11	00	0	0	0	0	Ib-IC	Ic-IA	0	0	0
00	11	00	11	01	01	00	00	11	0	0	0	0	Ib-IA	Ic-IC	0	0	0
00	00	11	11	01	01	00	00	11	0	0	0	0	Ib	IB+Ic	0	0	0
00	11	00	00	01	00	10	11	11	0	0	0	0	IB	0	-Ia	0	0
00	00	11	00	01	00	10	11	11	0	0	0	0	IB	0	-Ia	0	0

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
00	11	00	11	01	00	10	00	11	0	0	0	0	Ib-IA	0	Ic-IC	0	0
00	00	11	11	01	00	10	00	11	0	0	0	0	Ib	0	IB+Ic	0	0
00	11	11	00	01	00	10	11	00	0	0	0	0	IB	0	-Ia	0	0
00	11	11	00	01	00	10	00	11	0	0	0	0	IB	0	-Ia	0	0
00	11	11	11	01	00	10	00	00	0	0	0	0	-IA-Ia	0	-IC	0	0
00	11	00	00	00	01	10	11	11	0	0	0	0	0	IB	-Ia	0	0
00	00	11	00	00	01	10	11	11	0	0	0	0	0	IB	-Ia	0	0
00	11	00	11	00	01	10	11	00	0	0	0	0	0	Ic	IB+Ib	0	0
00	00	11	11	00	01	10	11	00	0	0	0	0	0	Ic-IA	Ib-IC	0	0
00	11	11	00	00	01	10	11	00	0	0	0	0	0	IB	-Ia	0	0
00	11	11	00	00	01	10	00	11	0	0	0	0	0	IB	-Ia	0	0
00	11	11	11	00	01	10	00	00	0	0	0	0	0	-IA-Ia	-IC	0	0
employ three capacitors																	
10	00	00	11	01	01	00	11	00	-IA	0	0	0	Ib-IC	Ic	0	0	0
10	00	00	11	01	01	00	00	11	-IA	0	0	0	Ib	Ic-IC	0	0	0
10	11	00	00	01	01	00	11	00	-Ia	0	0	0	IB-Ic	Ic	0	0	0
10	00	11	00	01	01	00	11	00	-Ia	0	0	0	Ib-IC	-IA-Ib	0	0	0
10	11	00	00	01	01	00	00	11	-Ia	0	0	0	-IA-Ic	Ic-IC	0	0	0
10	00	11	00	01	01	00	00	11	-Ia	0	0	0	Ib	IB-Ib	0	0	0
10	00	00	00	01	00	10	11	11	-IA	0	0	0	IB	0	IA-Ia	0	0
10	00	00	11	01	00	10	00	11	-IA	0	0	0	Ib	0	Ic-IC	0	0
10	11	11	00	01	00	10	00	00	IC-Ia	0	0	0	IB	0	-IC	0	0
10	00	11	00	01	00	10	11	00	Ic-IA	0	0	0	IB	0	IA+Ib	0	0
10	11	00	00	01	00	10	00	11	IC+Ib	0	0	0	IB	0	Ic-IC	0	0
10	00	11	11	01	00	10	00	00	Ic-IA	0	0	0	Ib	0	-IC	0	0
10	00	00	00	00	01	10	11	11	-IA	0	0	0	0	IB	IA-Ia	0	0
10	00	00	11	00	01	10	11	00	-IA	0	0	0	0	Ic	Ib-IC	0	0
10	11	11	00	00	01	10	00	00	IC-Ia	0	0	0	0	IB	-IC	0	0
10	00	11	00	00	01	10	11	00	IC+Ic	0	0	0	0	IB	Ib-IC	0	0
10	11	00	00	00	01	10	00	11	Ib-IA	0	0	0	0	IB	IA+Ic	0	0
10	11	00	11	00	01	10	00	00	Ib-IA	0	0	0	0	Ic	-IC	0	0
00	11	00	00	01	01	10	11	00	0	0	0	0	IB-Ic	Ic	-Ia	0	0
00	11	00	00	01	01	10	00	11	0	0	0	0	Ib-IA	-IC-Ib	-Ia	0	0
00	00	11	00	01	01	10	11	00	0	0	0	0	-IC-Ic	Ic-IA	-Ia	0	0
00	00	11	00	01	01	10	00	11	0	0	0	0	Ib	IB-Ib	-Ia	0	0
00	11	00	11	01	01	10	00	00	0	0	0	0	Ib-IA	Ic	-IC	0	0
00	00	11	11	01	01	10	00	00	0	0	0	0	Ib	Ic-IA	-IC	0	0
employ four capacitors																	
10	00	00	00	01	01	10	11	00	-IA	0	0	0	IB-Ic	Ic	IA-Ia	0	0
10	00	00	00	01	01	10	00	11	-IA	0	0	0	Ib	IB-Ib	IA-Ia	0	0
10	00	00	11	01	01	10	00	00	-IA	0	0	0	Ib	Ic	-IC	0	0
10	11	00	00	01	01	10	00	00	IC-Ia	0	0	0	IB-Ic	Ic	-IC	0	0
10	00	11	00	01	01	10	00	00	IC-Ia	0	0	0	Ib	IB-Ib	-IC	0	0

Table B.23: Switching device combinations for (V_{AB},V_{BC},V_{CA}) = ($-V_{cap}$,$+V_{cap}$,0) and (V_{ab},V_{bc},V_{ca}) = (0,$+V_{cap}$,$-V_{cap}$).

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
employ single capacitor																	
10	00	11	11	11	00	00	00	11	IB+Ic	0	0	0	0	0	0	0	0
00	10	11	11	11	00	00	00	11	0	IB+Ic	0	0	0	0	0	0	0
00	00	11	11	11	01	00	00	11	0	0	0	0	0	IB+Ic	0	0	0
00	00	11	11	11	00	10	00	11	0	0	0	0	0	0	IB+Ic	0	0
00	00	11	11	11	00	00	10	11	0	0	0	0	0	0	0	IB+Ic	0
employ two capacitors																	
10	10	11	11	00	00	00	00	11	IB-Ia	-Ib	0	0	0	0	0	0	0
10	10	11	00	11	00	00	00	11	-Ia	IB-Ib	0	0	0	0	0	0	0
10	00	00	11	11	01	00	00	11	-IA	0	0	0	0	Ic-IC	0	0	0
10	00	11	00	11	01	00	00	11	-Ia	0	0	0	0	IB-Ib	0	0	0
10	00	00	11	11	00	10	00	11	-IA	0	0	0	0	0	Ic-IC	0	0
10	00	11	11	11	00	10	00	00	Ic-IA	0	0	0	0	0	-IC	0	0
10	00	00	11	11	00	00	10	11	-IA	0	0	0	0	0	0	Ic-IC	0
10	00	11	11	00	00	00	10	11	IB-Ia	0	0	0	0	0	0	-Ib	0
10	00	11	00	11	00	00	10	11	-Ia	0	0	0	0	0	0	IB-Ib	0
10	00	11	11	11	00	00	10	00	Ic-IA	0	0	0	0	0	0	-IC	0
00	10	00	11	11	01	00	00	11	0	-IA	0	0	0	Ic-IC	0	0	0
00	10	11	11	00	01	00	00	11	0	-Ib	0	0	0	IB-Ia	0	0	0
00	10	00	11	11	00	10	00	11	0	-IA	0	0	0	0	Ic-IC	0	0
00	10	11	11	00	00	10	00	11	0	-Ib	0	0	0	0	IB-Ia	0	0
00	10	11	00	11	00	10	00	11	0	IB-Ib	0	0	0	0	-Ia	0	0
00	10	11	11	11	00	10	00	00	0	Ic-IA	0	0	0	0	-IC	0	0
00	10	00	11	11	00	00	10	11	0	-IA	0	0	0	0	0	Ic-IC	0
00	10	11	11	11	00	00	10	00	0	Ic-IA	0	0	0	0	0	-IC	0
00	00	11	00	11	01	10	00	11	0	0	0	0	0	IB-Ib	-Ia	0	0
00	00	11	11	11	01	10	00	00	0	0	0	0	0	Ic-IA	-IC	0	0
00	00	11	11	00	01	00	10	11	0	0	0	0	0	IB-Ia	0	-Ib	0
00	00	11	11	11	01	00	10	00	0	0	0	0	0	Ic-IA	0	-IC	0
00	00	11	11	00	00	10	10	11	0	0	0	0	0	0	IB-Ia	-Ib	0
00	00	11	00	11	00	10	10	11	0	0	0	0	0	0	-Ia	IB-Ib	0
employ three capacitors																	
10	10	11	00	00	01	00	00	11	-Ia	-Ib	0	0	0	IB	0	0	0
10	10	00	11	00	01	00	00	11	Ib-IA	-Ib	0	0	0	Ic-IC	0	0	0
10	10	00	00	11	01	00	00	11	-Ia	Ia-IA	0	0	0	Ic-IC	0	0	0
10	10	11	11	00	00	10	00	00	-IA-Ia	-Ib	0	0	0	0	-IC	0	0
10	10	11	00	11	00	10	00	00	IC-Ia	IB-Ib	0	0	0	0	-IC	0	0
10	10	00	11	00	00	10	00	11	Ib-IA	-Ib	0	0	0	0	Ic-IC	0	0
10	10	00	00	11	00	10	00	11	IC+Ib	IB-Ib	0	0	0	0	Ic-IC	0	0
10	10	11	11	00	00	00	10	00	IB-Ia	IC-Ib	0	0	0	0	0	-IC	0
10	10	11	00	11	00	00	10	00	-Ia	-IA-Ib	0	0	0	0	0	-IC	0
10	10	00	11	00	00	00	10	11	IB-Ia	IC+Ia	0	0	0	0	0	Ic-IC	0

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
10	10	00	00	11	00	00	10	11	-Ia	Ia-IA	0	0	0	0	0	Ic-IC	0
10	00	00	00	11	01	10	00	11	-IA	0	0	0	0	IB-Ib	IA-Ia	0	0
10	00	00	11	11	01	10	00	00	-IA	0	0	0	0	Ic	-IC	0	0
10	00	11	00	11	01	10	00	00	IC-Ia	0	0	0	0	IB-Ib	-IC	0	0
10	00	00	11	00	01	00	10	11	-IA	0	0	0	0	-IC-Ia	0	-Ib	0
10	00	11	00	00	01	00	10	11	-Ia	0	0	0	0	IB	0	-Ib	0
10	00	00	11	11	01	00	10	00	-IA	0	0	0	0	Ic	0	-IC	0
10	00	11	00	11	01	00	10	00	-Ia	0	0	0	0	-IA-Ib	0	-IC	0
10	00	00	11	00	00	10	10	11	-IA	0	0	0	0	0	-IC-Ia	-Ib	0
10	00	00	00	11	00	10	10	11	-IA	0	0	0	0	0	IA-Ia	IB-Ib	0
10	00	11	11	00	00	10	10	00	Ic-IA	0	0	0	0	0	Ib-IC	-Ib	0
10	00	11	00	11	00	10	10	00	Ic-IA	0	0	0	0	0	IA+Ib	IB-Ib	0
00	10	00	00	11	01	10	00	11	0	-IA	0	0	0	-IC-Ib	-Ia	0	0
00	10	11	00	00	01	10	00	11	0	-Ib	0	0	0	IB	-Ia	0	0
00	10	00	11	11	01	10	00	00	0	-IA	0	0	0	Ic	-IC	0	0
00	10	11	11	00	01	10	00	00	0	-Ib	0	0	0	-IA-Ia	-IC	0	0
00	10	00	11	00	01	00	10	11	0	-IA	0	0	0	IB-Ia	0	IA-Ib	0
00	10	00	11	11	01	00	10	00	0	-IA	0	0	0	Ic	0	-IC	0
00	10	11	11	00	01	00	10	00	0	IC-Ib	0	0	0	IB-Ia	0	-IC	0
00	10	00	11	00	00	10	10	11	0	-IA	0	0	0	0	IB-Ia	IA-Ib	0
00	10	00	00	11	00	10	10	11	0	-IA	0	0	0	0	-Ia	-IC-Ib	0
00	10	11	11	00	00	10	10	00	0	Ic-IA	0	0	0	0	IB-Ia	IA+Ia	0
00	10	11	00	11	00	10	10	00	0	Ic-IA	0	0	0	0	-Ia	Ia-IC	0
00	00	11	00	00	01	10	10	11	0	0	0	0	0	IB	-Ia	-Ib	0
00	00	11	11	00	01	10	10	00	0	0	0	0	0	Ic-IA	Ib-IC	-Ib	0
00	00	11	00	11	01	10	10	00	0	0	0	0	0	Ic-IA	-Ia	Ia-IC	0
employ four capacitors																	
10	10	11	00	00	01	10	00	00	IC-Ia	-Ib	0	0	0	IB	-IC	0	0
10	10	00	00	00	01	10	00	11	Ib-IA	-Ib	0	0	0	IB	IA+Ic	0	0
10	10	00	11	00	01	10	00	00	Ib-IA	-Ib	0	0	0	Ic	-IC	0	0
10	10	00	00	11	01	10	00	00	IC-Ia	IB+Ia	0	0	0	Ic	-IC	0	0
10	10	11	00	00	01	00	01	00	-Ia	IC-Ib	0	0	0	IB	0	-IC	0
10	10	00	00	00	01	00	10	11	-Ia	Ia-IA	0	0	0	IB	0	IA+Ic	0
10	10	00	11	00	01	00	10	00	IB+Ib	IC-Ib	0	0	0	Ic	0	-IC	0
10	10	00	00	11	01	00	10	00	-Ia	Ia-IA	0	0	0	Ic	0	-IC	0
10	00	00	00	00	01	10	10	11	-IA	0	0	0	0	IB	IA-Ia	-Ib	0
10	00	00	11	00	01	10	10	00	-IA	0	0	0	0	Ic	Ib-IC	-Ib	0
10	00	00	00	11	01	10	10	00	-IA	0	0	0	0	Ic	IA-Ia	IB+Ia	0
10	00	11	00	00	01	10	10	00	IC+Ic	0	0	0	0	IB	Ib-IC	-Ib	0
00	10	00	00	00	01	10	10	11	0	-IA	0	0	0	IB	-Ia	IA-Ib	0
00	10	00	11	00	01	10	10	00	0	-IA	0	0	0	Ic	IB+Ib	IA-Ib	0
00	10	00	00	11	01	10	10	00	0	-IA	0	0	0	Ic	-Ia	Ia-IC	0
00	10	11	00	00	01	10	10	00	0	IC+Ic	0	0	0	IB	-Ia	Ia-IC	0

Table B.24: Switching device combinations for (V_{AB},V_{BC},V_{CA}) = ($-V_{cap}$,$+V_{cap}$,0) and (V_{ab},V_{bc},V_{ca}) = ($-V_{cap}$,$+V_{cap}$,0).

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
employ single capacitor																	
11	10	11	00	11	00	11	00	00	0	IB-Ib	0	0	0	0	0	0	0
11	10	11	00	11	00	00	00	11	0	IB-Ib	0	0	0	0	0	0	0
11	10	00	00	11	00	11	00	11	0	IB-Ib	0	0	0	0	0	0	0
00	10	11	00	11	00	11	00	11	0	IB-Ib	0	0	0	0	0	0	0
11	00	00	01	11	00	11	00	11	0	0	0	IB-Ib	0	0	0	0	0
00	00	11	01	11	00	11	00	11	0	0	0	IB-Ib	0	0	0	0	0
11	00	11	01	11	00	11	00	00	0	0	0	IB-Ib	0	0	0	0	0
11	00	11	01	11	00	00	00	11	0	0	0	IB-Ib	0	0	0	0	0
11	00	00	00	11	01	11	00	11	0	0	0	0	0	IB-Ib	0	0	0
00	00	11	00	11	01	11	00	11	0	0	0	0	0	IB-Ib	0	0	0
11	00	11	00	11	01	11	00	00	0	0	0	0	0	IB-Ib	0	0	0
11	00	11	00	11	01	00	00	11	0	0	0	0	0	IB-Ib	0	0	0
11	00	00	00	11	00	11	10	11	0	0	0	0	0	0	0	IB-Ib	0
00	00	11	00	11	00	11	10	11	0	0	0	0	0	0	0	IB-Ib	0
11	00	11	00	11	00	11	10	00	0	0	0	0	0	0	0	IB-Ib	0
11	00	11	00	11	00	00	10	11	0	0	0	0	0	0	0	IB-Ib	0
employ two capacitors																	
00	10	00	01	11	00	11	00	11	0	-IA	0	-IC-Ib	0	0	0	0	0
11	10	11	01	00	00	11	00	00	0	-Ib	0	IB	0	0	0	0	0
11	10	11	01	00	00	00	00	11	0	-Ib	0	IB	0	0	0	0	0
11	10	00	01	00	00	11	00	11	0	-Ib	0	IB	0	0	0	0	0
00	10	11	01	00	00	11	00	11	0	-Ib	0	IB	0	0	0	0	0
00	10	11	01	11	00	11	00	00	0	Ic-IA	0	Ia-IC	0	0	0	0	0
00	10	11	01	11	00	00	00	11	0	IB+Ic	0	Ia	0	0	0	0	0
00	10	00	00	11	01	11	00	11	0	-IA	0	0	0	-IC-Ib	0	0	0
11	10	11	00	00	01	11	00	00	0	-Ib	0	0	0	IB	0	0	0
11	10	11	00	00	01	00	00	11	0	-Ib	0	0	0	IB	0	0	0
11	10	00	00	00	01	11	00	11	0	-Ib	0	0	0	IB	0	0	0
00	10	11	00	00	01	11	00	11	0	-Ib	0	0	0	IB	0	0	0
11	10	00	00	11	01	11	00	00	0	IB+Ia	0	0	0	Ic	0	0	0
11	10	00	00	11	01	00	00	11	0	Ia-IA	0	0	0	Ic-IC	0	0	0
00	10	00	00	11	00	11	10	11	0	-IA	0	0	0	0	0	-IC-Ib	0
11	10	11	00	11	00	00	10	00	0	-IA-Ib	0	0	0	0	0	-IC	0
00	10	11	00	11	00	11	10	00	0	Ic-IA	0	0	0	0	0	Ia-IC	0
11	10	00	00	11	00	00	10	11	0	Ia-IA	0	0	0	0	0	Ic-IC	0
11	00	00	01	11	01	11	00	00	0	0	0	IB+Ia	0	Ic	0	0	0
00	00	11	01	11	01	11	00	00	0	0	0	Ia-IC	0	Ic-IA	0	0	0
11	00	00	01	11	01	00	00	11	0	0	0	Ia-IA	0	Ic-IC	0	0	0
00	00	11	01	11	01	00	00	11	0	0	0	Ia	0	IB+Ic	0	0	0
11	00	00	01	00	00	11	10	11	0	0	0	IB	0	0	0	-Ib	0
00	00	11	01	00	00	11	10	11	0	0	0	IB	0	0	0	-Ib	0

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
11	00	00	01	11	00	00	10	11	0	0	0	Ia-IA	0	0	0	Ic-IC	0
00	00	11	01	11	00	00	10	11	0	0	0	Ia	0	0	0	IB+Ic	0
11	00	11	01	00	00	11	10	00	0	0	0	IB	0	0	0	-Ib	0
11	00	11	01	00	00	00	10	11	0	0	0	IB	0	0	0	-Ib	0
11	00	11	01	11	00	00	10	00	0	0	0	-IA-Ib	0	0	0	-IC	0
11	00	00	00	00	01	11	10	11	0	0	0	0	0	IB	0	-Ib	0
00	00	11	00	00	01	11	10	11	0	0	0	0	0	IB	0	-Ib	0
11	00	00	00	11	01	11	10	00	0	0	0	0	0	Ic	0	IB+Ia	0
00	00	11	00	11	01	11	10	00	0	0	0	0	0	Ic-IA	0	Ia-IC	0
11	00	11	00	00	01	11	10	00	0	0	0	0	0	IB	0	-Ib	0
11	00	11	00	00	01	00	10	11	0	0	0	0	0	IB	0	-Ib	0
11	00	11	00	11	01	00	10	00	0	0	0	0	0	-IA-Ib	0	-IC	0
employ three capacitors																	
00	10	00	01	11	01	11	00	00	0	-IA	0	Ia-IC	0	Ic	0	0	0
00	10	00	01	11	01	00	00	11	0	-IA	0	Ia	0	Ic-IC	0	0	0
11	10	00	01	00	01	11	00	00	0	-Ib	0	IB-Ic	0	Ic	0	0	0
00	10	11	01	00	01	11	00	00	0	-Ib	0	Ia-IC	0	-IA-Ia	0	0	0
11	10	00	01	00	01	00	00	11	0	-Ib	0	-IA-Ic	0	Ic-IC	0	0	0
00	10	11	01	00	01	00	00	11	0	-Ib	0	Ia	0	IB-Ia	0	0	0
00	10	00	01	00	00	11	10	11	0	-IA	0	IB	0	0	0	IA-Ib	0
00	10	00	01	11	00	00	10	11	0	-IA	0	Ia	0	0	0	Ic-IC	0
11	10	11	01	00	00	00	10	00	0	IC-Ib	0	IB	0	0	0	-IC	0
00	10	11	01	00	00	11	10	00	0	Ic-IA	0	IB	0	0	0	IA+Ia	0
11	10	00	01	00	00	00	10	11	0	IC+Ia	0	IB	0	0	0	Ic-IC	0
00	10	11	01	11	00	00	10	00	0	Ic-IA	0	Ia	0	0	0	-IC	0
00	10	00	00	00	01	11	10	11	0	-IA	0	0	0	IB	0	IA-Ib	0
00	10	00	00	11	01	11	10	00	0	-IA	0	0	0	Ic	0	Ia-IC	0
11	10	11	00	00	01	00	10	00	0	IC-Ib	0	0	0	IB	0	-IC	0
00	10	11	00	00	01	11	10	00	0	IC+Ic	0	0	0	IB	0	Ia-IC	0
11	10	00	00	00	01	00	10	11	0	Ia-IA	0	0	0	IB	0	IA+Ic	0
11	10	00	00	11	01	00	10	00	0	Ia-IA	0	0	0	Ic	0	-IC	0
11	00	00	01	00	01	11	10	00	0	0	0	IB-Ic	0	Ic	0	-Ib	0
11	00	00	01	00	01	00	10	11	0	0	0	Ia-IA	0	-IC-Ia	0	-Ib	0
00	00	11	01	00	01	11	10	00	0	0	0	-IC-Ic	0	Ic-IA	0	-Ib	0
00	00	11	01	00	01	00	10	11	0	0	0	Ia	0	IB-Ia	0	-Ib	0
11	00	00	01	11	01	00	10	00	0	0	0	Ia-IA	0	Ic	0	-IC	0
00	00	11	01	11	01	00	10	00	0	0	0	Ia	0	Ic-IA	0	-IC	0
employ four capacitors																	
00	10	00	01	00	01	11	10	00	0	-IA	0	IB-Ic	0	Ic	0	IA-Ib	0
00	10	00	01	00	01	00	10	11	0	-IA	0	Ia	0	IB-Ia	0	IA-Ib	0
00	10	00	01	11	01	00	10	00	0	-IA	0	Ia	0	Ic	0	-IC	0
11	10	00	01	00	01	00	10	00	0	IC-Ib	0	IB-Ic	0	Ic	0	-IC	0
00	10	11	01	00	01	00	10	00	0	IC-Ib	0	Ia	0	IB-Ia	0	-IC	0

Table B.25: Switching device combinations for (V_{AB},V_{BC},V_{CA}) = ($-V_{cap}$,$+V_{cap}$,0) and (V_{ab},V_{bc},V_{ca}) = ($-V_{cap}$,0,$+V_{cap}$).

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
employ single capacitor																	
11	10	00	00	11	11	11	00	00	0	IB+Ia	0	0	0	0	0	0	0
11	00	10	00	11	11	11	00	00	0	0	IB+Ia	0	0	0	0	0	0
11	00	00	01	11	11	11	00	00	0	0	0	IB+Ia	0	0	0	0	0
11	00	00	00	11	11	11	10	00	0	0	0	0	0	0	0	IB+Ia	0
11	00	00	00	11	11	11	00	10	0	0	0	0	0	0	0	0	IB+Ia
employ two capacitors																	
11	10	10	00	11	00	11	00	00	0	IB-Ib	-Ic	0	0	0	0	0	0
11	10	10	00	00	11	11	00	00	0	-Ib	IB-Ic	0	0	0	0	0	0
00	10	00	01	11	11	11	00	00	0	-IA	0	Ia-IC	0	0	0	0	0
11	10	00	01	00	11	11	00	00	0	-Ib	0	IB-Ic	0	0	0	0	0
00	10	00	00	11	11	11	10	00	0	-IA	0	0	0	0	0	Ia-IC	0
11	10	00	00	11	11	00	10	00	0	Ia-IA	0	0	0	0	0	-IC	0
00	10	00	00	11	11	11	00	10	0	-IA	0	0	0	0	0	0	Ia-IC
11	10	00	00	11	00	11	00	10	0	IB-Ib	0	0	0	0	0	0	-Ic
11	10	00	00	00	11	11	00	10	0	-Ib	0	0	0	0	0	0	IB-Ic
11	10	00	00	11	11	00	00	10	0	Ia-IA	0	0	0	0	0	0	-IC
00	00	10	01	11	11	11	00	00	0	0	-IA	Ia-IC	0	0	0	0	0
11	00	10	01	11	00	11	00	00	0	0	-Ic	IB-Ib	0	0	0	0	0
00	00	10	00	11	11	11	10	00	0	0	-IA	0	0	0	0	Ia-IC	0
11	00	10	00	11	00	11	10	00	0	0	-Ic	0	0	0	0	IB-Ib	0
11	00	10	00	00	11	11	10	00	0	0	IB-Ic	0	0	0	0	-Ib	0
11	00	10	00	11	11	00	10	00	0	0	Ia-IA	0	0	0	0	-IC	0
00	00	10	00	11	11	11	00	10	0	0	-IA	0	0	0	0	0	Ia-IC
11	00	10	00	11	11	00	00	10	0	0	Ia-IA	0	0	0	0	0	-IC
11	00	00	01	11	00	11	00	10	0	0	0	IB-Ib	0	0	0	0	-Ic
11	00	00	01	00	11	11	10	00	0	0	0	IB-Ic	0	0	0	-Ib	0
11	00	00	01	11	11	00	10	00	0	0	0	Ia-IA	0	0	0	-IC	0
11	00	00	01	11	11	00	00	10	0	0	0	Ia-IA	0	0	0	0	-IC
11	00	00	00	11	00	11	10	10	0	0	0	0	0	0	0	IB-Ib	-Ic
11	00	00	00	00	11	11	10	10	0	0	0	0	0	0	0	-Ib	IB-Ic
employ three capacitors																	
11	10	10	01	00	00	11	00	00	0	-Ib	-Ic	IB	0	0	0	0	0
00	10	10	01	11	00	11	00	00	0	Ic-IA	-Ic	Ia-IC	0	0	0	0	0
00	10	10	01	00	11	11	00	00	0	-Ib	Ib-IA	Ia-IC	0	0	0	0	0
11	10	10	00	11	00	00	10	00	0	-IA-Ib	-Ic	0	0	0	0	-IC	0
11	10	10	00	00	11	00	10	00	0	IC-Ib	IB-Ic	0	0	0	0	-IC	0
00	10	10	00	11	00	11	10	00	0	Ic-IA	-Ic	0	0	0	0	Ia-IC	0
00	10	10	00	00	11	11	10	00	0	IC+Ic	IB-Ic	0	0	0	0	Ia-IC	0
11	10	10	00	11	00	00	00	10	0	IB-Ib	IC-Ic	0	0	0	0	0	-IC
11	10	10	00	00	11	00	00	10	0	-Ib	-IA-Ic	0	0	0	0	0	-IC
00	10	10	00	11	00	11	00	10	0	IB-Ib	IC+Ib	0	0	0	0	0	Ia-IC

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
00	10	10	00	00	11	11	00	10	0	-Ib	Ib-IA	0	0	0	0	0	Ia-IC
00	10	00	01	00	11	11	10	00	0	-IA	0	IB-Ic	0	0	0	IA-Ib	0
00	10	00	01	11	11	00	10	00	0	-IA	0	Ia	0	0	0	-IC	0
11	10	00	01	00	11	00	10	00	0	IC-Ib	0	IB-Ic	0	0	0	-IC	0
00	10	00	01	11	00	11	00	10	0	-IA	0	-IC-Ib	0	0	0	0	-Ic
11	10	00	01	00	00	11	00	10	0	-Ib	0	IB	0	0	0	0	-Ic
00	10	00	01	11	11	00	00	10	0	-IA	0	Ia	0	0	0	0	-IC
11	10	00	01	00	11	00	00	10	0	-Ib	0	-IA-Ic	0	0	0	0	-IC
00	10	00	00	11	00	11	10	10	0	-IA	0	0	0	0	0	-IC-Ib	-Ic
00	10	00	00	00	11	11	10	10	0	-IA	0	0	0	0	0	IA-Ib	IB-Ic
11	10	00	00	11	00	00	10	10	0	Ia-IA	0	0	0	0	0	Ic-IC	-Ic
11	10	00	00	00	11	00	10	10	0	Ia-IA	0	0	0	0	0	IA+Ic	IB-Ic
00	00	10	01	00	11	11	10	00	0	0	-IA	-IC-Ic	0	0	0	-Ib	0
11	00	10	01	00	00	11	10	00	0	0	-Ic	IB	0	0	0	-Ib	0
00	00	10	01	11	11	00	10	00	0	0	-IA	Ia	0	0	0	-IC	0
11	00	10	01	11	00	00	10	00	0	0	-Ic	-IA-Ib	0	0	0	-IC	0
00	00	10	01	11	00	11	00	10	0	0	-IA	IB-Ib	0	0	0	0	IA-Ic
00	00	10	01	11	11	00	00	10	0	0	-IA	Ia	0	0	0	0	-IC
11	00	10	01	11	00	00	00	10	0	0	IC-Ic	IB-Ib	0	0	0	0	-IC
00	00	10	00	11	00	11	10	10	0	0	-IA	0	0	0	0	IB-Ib	IA-Ic
00	00	10	00	00	11	11	10	10	0	0	-IA	0	0	0	0	-Ib	-IC-Ic
11	00	10	00	11	00	00	10	10	0	0	Ia-IA	0	0	0	0	IB-Ib	IA+Ib
11	00	10	00	00	11	00	10	10	0	0	Ia-IA	0	0	0	0	-Ib	Ib-IC
11	00	00	01	00	11	00	10	10	0	0	0	Ia-IA	0	0	0	-Ib	Ib-IC
11	00	00	01	00	00	11	10	10	0	0	0	IB	0	0	0	-Ib	-Ic
11	00	00	01	11	00	00	10	10	0	0	0	Ia-IA	0	0	0	Ic-IC	-Ic
employ four capacitors																	
11	10	10	01	00	00	00	10	00	0	IC-Ib	-Ic	IB	0	0	0	-IC	0
00	10	10	01	00	00	11	10	00	0	Ic-IA	-Ic	IB	0	0	0	IA+Ia	0
00	10	10	01	11	00	00	10	00	0	Ic-IA	-Ic	Ia	0	0	0	-IC	0
00	10	10	01	00	11	00	10	00	0	IC-Ib	IB+Ib	Ia	0	0	0	-IC	0
11	10	10	01	00	00	00	00	10	0	-Ib	IC-Ic	IB	0	0	0	0	-IC
00	10	10	01	00	00	11	00	10	0	-Ib	Ib-IA	IB	0	0	0	0	IA+Ia
00	10	10	01	11	00	00	00	10	0	IB+Ic	IC-Ic	Ia	0	0	0	0	-IC
00	10	10	01	00	11	00	00	10	0	-Ib	Ib-IA	Ia	0	0	0	0	-IC
00	10	00	01	00	00	11	10	10	0	-IA	0	IB	0	0	0	IA-Ib	-Ic
00	10	00	01	11	00	00	10	10	0	-IA	0	Ia	0	0	0	Ic-IC	-Ic
00	10	00	01	00	11	00	10	10	0	-IA	0	Ia	0	0	0	IA-Ib	IB+Ib
11	10	00	01	00	00	00	10	10	0	IC+Ia	0	IB	0	0	0	Ic-IC	-Ic
00	00	10	01	00	00	11	10	10	0	0	-IA	IB	0	0	0	-Ib	IA-Ic
00	00	10	01	11	00	00	10	10	0	0	-IA	Ia	0	0	0	IB+Ic	IA-Ic
00	00	10	01	00	11	00	10	10	0	0	-IA	Ia	0	0	0	-Ib	Ib-IC
11	00	10	01	00	00	00	10	10	0	0	IC+Ia	IB	0	0	0	-Ib	Ib-IC

Table B.26: Switching device combinations for (V_{AB},V_{BC},V_{CA}) = ($-V_{cap}$,$+V_{cap}$,0) and (V_{ab},V_{bc},V_{ca}) = (0,$-V_{cap}$,$+V_{cap}$).

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
employ single capacitor																	
11	11	10	00	00	11	11	00	00	0	0	IB-Ic	0	0	0	0	0	0
11	11	10	00	00	11	00	11	00	0	0	IB-Ic	0	0	0	0	0	0
11	00	10	00	00	11	11	11	00	0	0	IB-Ic	0	0	0	0	0	0
00	11	10	00	00	11	11	11	00	0	0	IB-Ic	0	0	0	0	0	0
11	00	00	01	00	11	11	11	00	0	0	0	IB-Ic	0	0	0	0	0
00	11	00	01	00	11	11	11	00	0	0	0	IB-Ic	0	0	0	0	0
11	11	00	01	00	11	11	00	00	0	0	0	IB-Ic	0	0	0	0	0
11	11	00	01	00	11	00	11	00	0	0	0	IB-Ic	0	0	0	0	0
11	00	00	00	01	11	11	11	00	0	0	0	0	IB-Ic	0	0	0	0
00	11	00	00	01	11	11	11	00	0	0	0	0	IB-Ic	0	0	0	0
11	11	00	00	01	11	11	00	00	0	0	0	0	IB-Ic	0	0	0	0
11	11	00	00	01	11	00	11	00	0	0	0	0	IB-Ic	0	0	0	0
11	00	00	00	00	11	11	11	10	0	0	0	0	0	0	0	0	IB-Ic
00	11	00	00	00	11	11	11	10	0	0	0	0	0	0	0	0	IB-Ic
11	11	00	00	00	11	11	00	10	0	0	0	0	0	0	0	0	IB-Ic
11	11	00	00	00	11	00	11	10	0	0	0	0	0	0	0	0	IB-Ic
employ two capacitors																	
00	00	10	01	00	11	11	11	00	0	0	-IA	-IC-Ic	0	0	0	0	0
11	11	10	01	00	00	11	00	00	0	0	-Ic	IB	0	0	0	0	0
11	11	10	01	00	00	00	11	00	0	0	-Ic	IB	0	0	0	0	0
11	00	10	01	00	00	11	11	00	0	0	-Ic	IB	0	0	0	0	0
00	11	10	01	00	00	11	11	00	0	0	-Ic	IB	0	0	0	0	0
00	11	10	01	00	11	11	00	00	0	0	Ib-IA	Ia-IC	0	0	0	0	0
00	11	10	01	00	11	00	11	00	0	0	IB+Ib	Ia	0	0	0	0	0
00	00	10	00	01	11	11	11	00	0	0	-IA	0	-IC-Ic	0	0	0	0
11	11	10	00	01	00	11	00	00	0	0	-Ic	0	IB	0	0	0	0
11	11	10	00	01	00	00	11	00	0	0	-Ic	0	IB	0	0	0	0
11	00	10	00	01	00	11	11	00	0	0	-Ic	0	IB	0	0	0	0
00	11	10	00	01	00	11	11	00	0	0	-Ic	0	IB	0	0	0	0
11	00	10	00	01	11	11	00	00	0	0	IB+Ia	0	Ib	0	0	0	0
11	00	10	00	01	11	00	11	00	0	0	Ia-IA	0	Ib-IC	0	0	0	0
00	00	10	00	00	11	11	11	10	0	0	-IA	0	0	0	0	0	-IC-Ic
11	11	10	00	00	11	00	00	10	0	0	-IA-Ic	0	0	0	0	0	-IC
00	11	10	00	00	11	11	00	10	0	0	Ib-IA	0	0	0	0	0	Ia-IC
11	00	10	00	00	11	00	11	10	0	0	Ia-IA	0	0	0	0	0	Ib-IC
11	00	00	01	01	11	11	00	00	0	0	0	IB+Ia	Ib	0	0	0	0
00	11	00	01	01	11	11	00	00	0	0	0	Ia-IC	Ib-IA	0	0	0	0
11	00	00	01	01	11	00	11	00	0	0	0	Ia-IA	Ib-IC	0	0	0	0
00	11	00	01	01	11	00	11	00	0	0	0	Ia	IB+Ib	0	0	0	0
11	00	00	01	00	00	11	11	10	0	0	0	IB	0	0	0	0	-Ic
00	11	00	01	00	00	11	11	10	0	0	0	IB	0	0	0	0	-Ic

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
11	00	00	01	00	11	00	11	10	0	0	0	Ia-IA	0	0	0	0	Ib-IC
00	11	00	01	00	11	00	11	10	0	0	0	Ia	0	0	0	0	IB+Ib
11	11	00	01	00	00	11	00	10	0	0	0	IB	0	0	0	0	-Ic
11	11	00	01	00	00	00	11	10	0	0	0	IB	0	0	0	0	-Ic
11	11	00	01	00	11	00	00	10	0	0	0	-IA-Ic	0	0	0	0	-IC
11	00	00	00	01	00	11	11	10	0	0	0	0	IB	0	0	0	-Ic
00	11	00	00	01	00	11	11	10	0	0	0	0	IB	0	0	0	-Ic
11	11	00	00	01	00	11	00	10	0	0	0	0	IB	0	0	0	-Ic
11	11	00	00	01	00	00	11	10	0	0	0	0	IB	0	0	0	-Ic
11	00	00	00	01	11	11	00	10	0	0	0	0	Ib	0	0	0	IB+Ia
00	11	00	00	01	11	11	00	10	0	0	0	0	Ib-IA	0	0	0	Ia-IC
11	11	00	00	01	11	00	00	10	0	0	0	0	-IA-Ic	0	0	0	-IC
employ three capacitors																	
00	00	10	01	01	11	11	00	00	0	0	-IA	Ia-IC	Ib	0	0	0	0
00	00	10	01	01	11	00	11	00	0	0	-IA	Ia	Ib-IC	0	0	0	0
11	00	10	01	01	00	11	00	00	0	0	-Ic	IB-Ib	Ib	0	0	0	0
00	11	10	01	01	00	11	00	00	0	0	-Ic	Ia-IC	-IA-Ia	0	0	0	0
11	00	10	01	01	00	00	11	00	0	0	-Ic	-IA-Ib	Ib-IC	0	0	0	0
00	11	10	01	01	00	00	11	00	0	0	-Ic	Ia	IB-Ia	0	0	0	0
00	00	10	01	00	00	11	11	10	0	0	-IA	IB	0	0	0	0	IA-Ic
00	00	10	01	00	11	00	11	10	0	0	-IA	Ia	0	0	0	0	Ib-IC
11	11	10	01	00	00	00	00	10	0	0	IC-Ic	IB	0	0	0	0	-IC
00	11	10	01	00	00	11	00	10	0	0	Ib-IA	IB	0	0	0	0	IA+Ia
11	00	10	01	00	00	00	11	10	0	0	IC+Ia	IB	0	0	0	0	Ib-IC
00	11	10	01	00	11	00	00	10	0	0	Ib-IA	Ia	0	0	0	0	-IC
00	00	10	00	01	00	11	11	10	0	0	-IA	0	IB	0	0	0	IA-Ic
00	00	10	00	01	11	11	00	10	0	0	-IA	0	Ib	0	0	0	Ia-IC
11	11	10	00	01	00	00	00	10	0	0	IC-Ic	0	IB	0	0	0	-IC
00	11	10	00	01	00	11	00	10	0	0	IC+Ib	0	IB	0	0	0	Ia-IC
11	00	10	00	01	00	00	11	10	0	0	Ia-IA	0	IB	0	0	0	IA+Ib
11	00	10	00	01	11	00	00	10	0	0	Ia-IA	0	Ib	0	0	0	-IC
11	00	00	01	01	00	11	00	10	0	0	0	IB-Ib	Ib	0	0	0	-Ic
11	00	00	01	01	00	00	11	10	0	0	0	Ia-IA	-IC-Ia	0	0	0	-Ic
00	11	00	01	01	00	11	00	10	0	0	0	-IC-Ib	Ib-IA	0	0	0	-Ic
00	11	00	01	01	00	00	11	10	0	0	0	Ia	IB-Ia	0	0	0	-Ic
11	00	00	01	01	11	00	00	10	0	0	0	Ia-IA	Ib	0	0	0	-IC
00	11	00	01	01	11	00	00	10	0	0	0	Ia	Ib-IA	0	0	0	-IC
employ four capacitors																	
00	00	10	01	01	00	11	00	10	0	0	-IA	IB-Ib	Ib	0	0	0	IA-Ic
00	00	10	01	01	00	00	11	10	0	0	-IA	Ia	IB-Ia	0	0	0	IA-Ic
00	00	10	01	01	11	00	00	10	0	0	-IA	Ia	Ib	0	0	0	-IC
11	00	10	01	01	00	00	00	10	0	0	IC-Ic	IB-Ib	Ib	0	0	0	-IC
00	11	10	01	01	00	00	00	10	0	0	IC-Ic	Ia	IB-Ia	0	0	0	-IC

Table B.27: Switching device combinations for (V_{AB},V_{BC},V_{CA}) = ($-V_{cap}$,$+V_{cap}$,0) and (V_{ab},V_{bc},V_{ca}) = ($+V_{cap}$,$-V_{cap}$,0).

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
employ single capacitor																	
10	11	00	11	00	11	00	11	00	IB+Ib	0	0	0	0	0	0	0	0
00	11	10	11	00	11	00	11	00	0	0	IB+Ib	0	0	0	0	0	0
00	11	00	11	01	11	00	11	00	0	0	0	0	IB+Ib	0	0	0	0
00	11	00	11	00	11	10	11	00	0	0	0	0	0	0	IB+Ib	0	0
00	11	00	11	00	11	00	11	10	0	0	0	0	0	0	0	0	IB+Ib
employ two capacitors																	
10	11	10	11	00	00	00	11	00	IB-Ia	0	-Ic	0	0	0	0	0	0
10	11	10	00	00	11	00	11	00	-Ia	0	IB-Ic	0	0	0	0	0	0
10	00	00	11	01	11	00	11	00	-IA	0	0	0	Ib-IC	0	0	0	0
10	11	00	00	01	11	00	11	00	-Ia	0	0	0	IB-Ic	0	0	0	0
10	00	00	11	00	11	10	11	00	-IA	0	0	0	0	0	Ib-IC	0	0
10	11	00	11	00	11	10	00	00	Ib-IA	0	0	0	0	0	-IC	0	0
10	00	00	11	00	11	00	11	10	-IA	0	0	0	0	0	0	0	Ib-IC
10	11	00	11	00	00	00	11	10	IB-Ia	0	0	0	0	0	0	0	-Ic
10	11	00	00	00	11	00	11	10	-Ia	0	0	0	0	0	0	0	IB-Ic
10	11	00	11	00	11	00	00	10	Ib-IA	0	0	0	0	0	0	0	-IC
00	00	10	11	01	11	00	11	00	0	0	-IA	0	Ib-IC	0	0	0	0
00	11	10	11	01	00	00	11	00	0	0	-Ic	0	IB-Ia	0	0	0	0
00	00	10	11	00	11	10	11	00	0	0	-IA	0	0	0	Ib-IC	0	0
00	11	10	11	00	00	10	11	00	0	0	-Ic	0	0	0	IB-Ia	0	0
00	11	10	00	00	11	10	11	00	0	0	IB-Ic	0	0	0	-Ia	0	0
00	11	10	11	00	11	10	00	00	0	0	Ib-IA	0	0	0	-IC	0	0
00	00	10	11	00	11	00	11	10	0	0	-IA	0	0	0	0	0	Ib-IC
00	11	10	11	00	11	00	00	10	0	0	Ib-IA	0	0	0	0	0	-IC
00	11	00	00	01	11	10	11	00	0	0	0	0	IB-Ic	0	-Ia	0	0
00	11	00	11	01	11	10	00	00	0	0	0	0	Ib-IA	0	-IC	0	0
00	11	00	11	01	00	00	11	10	0	0	0	0	IB-Ia	0	0	0	-Ic
00	11	00	11	01	11	00	00	10	0	0	0	0	Ib-IA	0	0	0	-IC
00	11	00	11	00	00	10	11	10	0	0	0	0	0	0	IB-Ia	0	-Ic
00	11	00	00	00	11	10	11	10	0	0	0	0	0	0	-Ia	0	IB-Ic
employ three capacitors																	
10	11	10	00	01	00	00	11	00	-Ia	0	-Ic	0	IB	0	0	0	0
10	00	10	11	01	00	00	11	00	Ic-IA	0	-Ic	0	Ib-IC	0	0	0	0
10	00	10	00	01	11	00	11	00	-Ia	0	Ia-IA	0	Ib-IC	0	0	0	0
10	11	10	11	00	00	10	00	00	-IA-Ia	0	-Ic	0	0	0	-IC	0	0
10	11	10	00	00	11	10	00	00	IC-Ia	0	IB-Ic	0	0	0	-IC	0	0
10	00	10	00	00	11	10	11	00	IC+Ic	0	IB-Ic	0	0	0	Ib-IC	0	0
10	11	10	11	00	00	00	00	10	IB-Ia	0	IC-Ic	0	0	0	0	0	-IC
10	11	10	00	00	11	00	00	10	-Ia	0	-IA-Ic	0	0	0	0	0	-IC
10	00	10	11	00	00	00	11	10	IB-Ia	0	IC+Ia	0	0	0	0	0	Ib-IC
10	00	10	00	00	11	00	11	10	-Ia	0	Ia-IA	0	0	0	0	0	Ib-IC

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
10	00	10	11	00	00	10	11	00	Ic-IA	0	-Ic	0	0	0	Ib-IC	0	0
10	00	00	00	01	11	10	11	00	-IA	0	0	0	IB-Ic	0	IA-Ia	0	0
10	00	00	11	01	11	10	00	00	-IA	0	0	0	Ib	0	-IC	0	0
10	11	00	00	01	11	10	00	00	IC-Ia	0	0	0	IB-Ic	0	-IC	0	0
10	00	00	11	01	00	00	11	10	-IA	0	0	0	-IC-Ia	0	0	0	-Ic
10	11	00	00	01	00	00	11	10	-Ia	0	0	0	IB	0	0	0	-Ic
10	00	00	11	01	11	00	00	10	-IA	0	0	0	Ib	0	0	0	-IC
10	11	00	00	01	11	00	00	10	-Ia	0	0	0	-IA-Ic	0	0	0	-IC
10	00	00	11	00	00	10	11	10	-IA	0	0	0	0	0	-IC-Ia	0	-Ic
10	00	00	00	00	11	10	11	10	-IA	0	0	0	0	0	IA-Ia	0	IB-Ic
10	11	00	11	00	00	10	00	10	Ib-IA	0	0	0	0	0	Ic-IC	0	-Ic
10	11	00	00	00	11	10	00	10	Ib-IA	0	0	0	0	0	IA+Ic	0	IB-Ic
00	00	10	00	01	11	10	11	00	0	0	-IA	0	-IC-Ic	0	-Ia	0	0
00	11	10	00	01	00	10	11	00	0	0	-Ic	0	IB	0	-Ia	0	0
00	00	10	11	01	11	10	00	00	0	0	-IA	0	Ib	0	-IC	0	0
00	11	10	11	01	00	10	00	00	0	0	-Ic	0	-IA-Ia	0	-IC	0	0
00	00	10	11	01	00	00	11	10	0	0	-IA	0	IB-Ia	0	0	0	IA-Ic
00	00	10	11	01	11	00	00	10	0	0	-IA	0	Ib	0	0	0	-IC
00	11	10	11	01	00	00	00	10	0	0	IC-Ic	0	IB-Ia	0	0	0	-IC
00	00	10	11	00	00	10	11	10	0	0	-IA	0	0	0	IB-Ia	0	IA-Ic
00	00	10	00	00	11	10	11	10	0	0	-IA	0	0	0	-Ia	0	-IC-Ic
00	11	10	11	00	00	10	00	10	0	0	Ib-IA	0	0	0	IB-Ia	0	IA+Ia
00	11	10	00	00	11	10	00	10	0	0	Ib-IA	0	0	0	-Ia	0	Ia-IC
00	11	00	00	01	00	10	11	10	0	0	0	0	IB	0	-Ia	0	-Ic
00	11	00	11	01	00	10	00	10	0	0	0	0	Ib-IA	0	Ic-IC	0	-Ic
00	11	00	00	01	11	10	00	10	0	0	0	0	Ib-IA	0	-Ia	0	Ia-IC
employ four capacitors																	
10	11	10	00	01	00	10	00	00	IC-Ia	0	-Ic	0	IB	0	-IC	0	0
10	00	10	00	01	00	10	11	00	Ic-IA	0	-Ic	0	IB	0	IA+Ib	0	0
10	00	10	11	01	00	10	00	00	Ic-IA	0	-Ic	0	Ib	0	-IC	0	0
10	00	10	00	01	11	10	00	00	IC-Ia	0	IB+Ia	0	Ib	0	-IC	0	0
10	11	10	00	01	00	00	00	10	-Ia	0	IC-Ic	0	IB	0	0	0	-IC
10	00	10	00	01	00	00	11	10	-Ia	0	Ia-IA	0	IB	0	0	0	IA+Ib
10	00	10	11	01	00	00	00	10	IB+Ic	0	IC-Ic	0	Ib	0	0	0	-IC
10	00	10	00	01	11	00	00	10	-Ia	0	Ia-IA	0	Ib	0	0	0	-IC
10	00	00	00	01	00	10	11	10	-IA	0	0	0	IB	0	IA-Ia	0	-Ic
10	00	00	11	01	00	10	00	10	-IA	0	0	0	Ib	0	Ic-IC	0	-Ic
10	00	00	00	01	11	10	00	10	-IA	0	0	0	Ib	0	IA-Ia	0	IB+Ia
10	11	00	00	01	00	10	00	10	IC+Ib	0	0	0	IB	0	Ic-IC	0	-Ic
00	00	10	00	01	00	10	11	10	0	0	-IA	0	IB	0	-Ia	0	IA-Ic
00	00	10	11	01	00	10	00	10	0	0	-IA	0	Ib	0	IB+Ic	0	IA-Ic
00	00	10	00	01	11	10	00	10	0	0	-IA	0	Ib	0	-Ia	0	Ia-IC
00	11	10	00	01	00	10	00	10	0	0	IC+Ib	0	IB	0	-Ia	0	Ia-IC

Table B.28: Switching device combinations for (V_{AB},V_{BC},V_{CA}) = ($-V_{cap}$,0,$+V_{cap}$) and (V_{ab},V_{bc},V_{ca}) = (0,0,0).

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
employ single capacitor																	
10	00	00	11	00	00	11	11	11	-IA	0	0	0	0	0	0	0	0
10	00	00	00	11	00	11	11	11	-IA	0	0	0	0	0	0	0	0
10	00	00	00	00	11	11	11	11	-IA	0	0	0	0	0	0	0	0
10	00	00	11	11	00	11	00	11	-IA	0	0	0	0	0	0	0	0
10	00	00	11	11	00	00	11	11	-IA	0	0	0	0	0	0	0	0
10	00	00	11	00	11	11	11	00	-IA	0	0	0	0	0	0	0	0
10	00	00	11	00	11	00	11	11	-IA	0	0	0	0	0	0	0	0
10	00	00	00	11	11	11	11	00	-IA	0	0	0	0	0	0	0	0
10	00	00	00	11	11	11	00	11	-IA	0	0	0	0	0	0	0	0
10	00	00	11	11	11	11	00	00	-IA	0	0	0	0	0	0	0	0
10	00	00	11	11	11	00	11	00	-IA	0	0	0	0	0	0	0	0
10	00	00	11	11	11	00	00	11	-IA	0	0	0	0	0	0	0	0
00	10	00	11	00	00	11	11	11	0	-IA	0	0	0	0	0	0	0
00	10	00	00	11	00	11	11	11	0	-IA	0	0	0	0	0	0	0
00	10	00	00	00	11	11	11	11	0	-IA	0	0	0	0	0	0	0
00	10	00	11	11	00	11	00	11	0	-IA	0	0	0	0	0	0	0
00	10	00	11	11	00	00	11	11	0	-IA	0	0	0	0	0	0	0
00	10	00	11	00	11	11	11	00	0	-IA	0	0	0	0	0	0	0
00	10	00	11	00	11	00	11	11	0	-IA	0	0	0	0	0	0	0
00	10	00	00	11	11	11	11	00	0	-IA	0	0	0	0	0	0	0
00	10	00	00	11	11	11	00	11	0	-IA	0	0	0	0	0	0	0
00	10	00	11	11	11	11	00	00	0	-IA	0	0	0	0	0	0	0
00	10	00	11	11	11	00	11	00	0	-IA	0	0	0	0	0	0	0
00	10	00	11	11	11	00	00	11	0	-IA	0	0	0	0	0	0	0
00	00	10	11	00	00	11	11	11	0	0	-IA	0	0	0	0	0	0
00	00	10	00	11	00	11	11	11	0	0	-IA	0	0	0	0	0	0
00	00	10	00	00	11	11	11	11	0	0	-IA	0	0	0	0	0	0
00	00	10	11	11	00	11	00	11	0	0	-IA	0	0	0	0	0	0
00	00	10	11	11	00	00	11	11	0	0	-IA	0	0	0	0	0	0
00	00	10	11	00	11	11	11	00	0	0	-IA	0	0	0	0	0	0
00	00	10	11	00	11	00	11	11	0	0	-IA	0	0	0	0	0	0
00	00	10	00	11	11	11	11	00	0	0	-IA	0	0	0	0	0	0
00	00	10	00	11	11	11	00	11	0	0	-IA	0	0	0	0	0	0
00	00	10	11	11	11	11	00	00	0	0	-IA	0	0	0	0	0	0
00	00	10	11	11	11	00	11	00	0	0	-IA	0	0	0	0	0	0
00	00	10	11	11	11	00	00	11	0	0	-IA	0	0	0	0	0	0
employ two capacitors																	
10	10	00	11	00	00	11	00	11	Ib-IA	-Ib	0	0	0	0	0	0	0
10	10	00	11	00	00	00	11	11	IB-Ia	IC+Ia	0	0	0	0	0	0	0
10	10	00	00	11	00	11	00	11	IC+Ib	IB-Ib	0	0	0	0	0	0	0
10	10	00	00	11	00	00	11	11	-Ia	Ia-IA	0	0	0	0	0	0	0

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
10	10	00	00	00	11	11	00	11	Ib-IA	-Ib	0	0	0	0	0	0	0
10	10	00	00	00	11	00	11	11	-Ia	Ia-IA	0	0	0	0	0	0	0
10	10	00	11	00	11	11	00	00	Ib-IA	-Ib	0	0	0	0	0	0	0
10	10	00	00	11	11	11	00	00	IC-Ia	IB+Ia	0	0	0	0	0	0	0
10	10	00	11	00	11	00	11	00	IB+Ib	IC-Ib	0	0	0	0	0	0	0
10	10	00	00	11	11	00	11	00	-Ia	Ia-IA	0	0	0	0	0	0	0
10	10	00	11	00	11	00	00	11	Ib-IA	-Ib	0	0	0	0	0	0	0
10	10	00	00	11	11	00	00	11	-Ia	Ia-IA	0	0	0	0	0	0	0
10	00	10	11	00	00	11	11	00	Ic-IA	0	-Ic	0	0	0	0	0	0
10	00	10	11	00	00	00	11	11	IB-Ia	0	IC+Ia	0	0	0	0	0	0
10	00	10	00	11	00	11	11	00	Ic-IA	0	-Ic	0	0	0	0	0	0
10	00	10	00	11	00	00	11	11	-Ia	0	Ia-IA	0	0	0	0	0	0
10	00	10	00	00	11	11	11	00	IC+Ic	0	IB-Ic	0	0	0	0	0	0
10	00	10	00	00	11	00	11	11	-Ia	0	Ia-IA	0	0	0	0	0	0
10	00	10	11	11	00	11	00	00	-Ic	0	Ic-IA	0	0	0	0	0	0
10	00	10	00	11	11	11	00	00	IC-Ia	0	IB+Ia	0	0	0	0	0	0
10	00	10	11	11	00	00	11	00	Ic-IA	0	-Ic	0	0	0	0	0	0
10	00	10	00	11	11	00	11	00	-Ia	0	Ia-IA	0	0	0	0	0	0
10	00	10	11	11	00	00	00	11	IB+Ic	0	IC-Ic	0	0	0	0	0	0
10	00	10	00	11	11	00	00	11	-Ia	0	Ia-IA	0	0	0	0	0	0
00	10	10	11	00	00	11	11	00	0	Ic-IA	-Ic	0	0	0	0	0	0
00	10	10	11	00	00	11	00	11	0	-Ib	Ib-IA	0	0	0	0	0	0
00	10	10	00	11	00	11	11	00	0	Ic-IA	-Ic	0	0	0	0	0	0
00	10	10	00	11	00	11	00	11	0	IB-Ib	IC+Ib	0	0	0	0	0	0
00	10	10	00	00	11	11	11	00	0	IC+Ic	IB-Ic	0	0	0	0	0	0
00	10	10	00	00	11	11	00	11	0	-Ib	Ib-IA	0	0	0	0	0	0
00	10	10	11	11	00	11	00	00	0	Ic-IA	-Ic	0	0	0	0	0	0
00	10	10	11	00	11	11	00	00	0	-Ib	Ib-IA	0	0	0	0	0	0
00	10	10	11	11	00	00	11	00	0	Ic-IA	-Ic	0	0	0	0	0	0
00	10	10	11	00	11	00	11	00	0	IC-Ib	IB+Ib	0	0	0	0	0	0
00	10	10	11	11	00	00	00	11	0	IB+Ic	IC-Ic	0	0	0	0	0	0
00	10	10	11	00	11	00	00	11	0	-Ib	Ib-IA	0	0	0	0	0	0
11	11	11	01	00	00	01	00	00	0	0	0	IB	0	0	IC	0	0
11	11	11	01	00	00	00	01	00	0	0	0	IB	0	0	0	IC	0
11	11	11	01	00	00	00	00	01	0	0	0	IB	0	0	0	0	IC
11	11	11	00	01	00	01	00	00	0	0	0	0	IB	0	IC	0	0
11	11	11	00	01	00	00	01	00	0	0	0	0	IB	0	0	IC	0
11	11	11	00	01	00	00	00	01	0	0	0	0	IB	0	0	0	IC
11	11	11	00	00	01	01	00	00	0	0	0	0	0	IB	IC	0	0
11	11	11	00	00	01	00	01	00	0	0	0	0	0	IB	0	IC	0
11	11	11	00	00	01	00	00	01	0	0	0	0	0	IB	0	0	IC
employ three capacitors																	
10	10	10	11	00	00	11	00	00	-IA-Ia	-Ib	-Ic	0	0	0	0	0	0
10	10	10	11	00	00	00	11	00	IB-Ia	IC-Ib	-Ic	0	0	0	0	0	0
10	10	10	11	00	00	00	00	11	IB-Ia	-Ib	IC-Ic	0	0	0	0	0	0

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
10	10	10	00	11	00	11	00	00	IC-Ia	IB-Ib	-Ic	0	0	0	0	0	0
10	10	10	00	11	00	00	11	00	-Ia	-IA-Ib	-Ic	0	0	0	0	0	0
10	10	10	00	11	00	00	00	11	-Ia	IB-Ib	IC-Ic	0	0	0	0	0	0
10	10	10	00	00	11	11	00	00	IC-Ia	-Ib	IB-Ic	0	0	0	0	0	0
10	10	10	00	00	11	00	11	00	-Ia	IC-Ib	IB-Ic	0	0	0	0	0	0
10	10	10	00	00	11	00	00	11	-Ia	-Ib	-IA-Ic	0	0	0	0	0	0
11	00	11	01	01	00	01	00	00	0	0	0	IB-Ib	Ib	0	IC	0	0
00	11	11	01	01	00	01	00	00	0	0	0	Ia-IC	-IA-Ia	0	IC	0	0
11	00	11	01	01	00	00	01	00	0	0	0	-IA-Ib	Ib-IC	0	0	IC	0
00	11	11	01	01	00	00	01	00	0	0	0	Ia	IB-Ia	0	0	IC	0
11	00	11	01	01	00	00	00	01	0	0	0	IB-Ib	Ib	0	0	0	IC
00	11	11	01	01	00	00	00	01	0	0	0	Ia	IB-Ia	0	0	0	IC
11	11	00	01	00	01	01	00	00	0	0	0	IB-Ic	0	Ic	IC	0	0
00	11	11	01	00	01	01	00	00	0	0	0	Ia-IC	0	-IA-Ia	IC	0	0
11	11	00	01	00	01	00	01	00	0	0	0	IB-Ic	0	Ic	0	IC	0
00	11	11	01	00	01	00	01	00	0	0	0	Ia	0	IB-Ia	0	IC	0
11	11	00	01	00	01	00	00	01	0	0	0	-IA-Ic	0	Ic-IC	0	0	IC
00	11	11	01	00	01	00	00	01	0	0	0	Ia	0	IB-Ia	0	0	IC
11	00	11	01	00	00	01	01	00	0	0	0	IB	0	0	IC-Ib	Ib	0
00	11	11	01	00	00	01	01	00	0	0	0	IB	0	0	Ia-IB	-IA-Ia	0
11	11	00	01	00	00	01	00	01	0	0	0	IB	0	0	IC-Ic	0	Ic
00	11	11	01	00	00	01	00	01	0	0	0	IB	0	0	Ia-IB	0	-IA-Ia
11	11	00	01	00	00	00	01	01	0	0	0	IB	0	0	0	IC-Ic	Ic
11	00	11	01	00	00	00	01	01	0	0	0	IB	0	0	0	Ib	IC-Ib
11	11	00	00	01	01	01	00	00	0	0	0	0	IB-Ic	Ic	IC	0	0
11	00	11	00	01	01	01	00	00	0	0	0	0	Ib	IB-Ib	IC	0	0
11	11	00	00	01	01	00	01	00	0	0	0	0	IB-Ic	Ic	0	IC	0
11	00	11	00	01	01	00	01	00	0	0	0	0	Ib-IC	-IA-Ib	0	IC	0
11	11	00	00	01	01	00	00	01	0	0	0	0	-IA-Ic	Ic-IC	0	0	IC
11	00	11	00	01	01	00	00	01	0	0	0	0	Ib	IB-Ib	0	0	IC
11	00	11	00	01	00	01	01	00	0	0	0	0	IB	0	-IA-Ib	Ib-IB	0
00	11	11	00	01	00	01	01	00	0	0	0	0	IB	0	Ia	IC-Ia	0
11	11	00	00	01	00	01	00	01	0	0	0	0	IB	0	IC-Ic	0	Ic
00	11	11	00	01	00	01	00	01	0	0	0	0	IB	0	Ia	0	IC-Ia
11	11	00	00	01	00	00	01	01	0	0	0	0	IB	0	0	IC-Ic	Ic
11	00	11	00	01	00	00	01	01	0	0	0	0	IB	0	0	Ib-IB	-IA-Ib
11	00	11	00	00	01	01	01	00	0	0	0	0	0	IB	IC-Ib	Ib	0
00	11	11	00	00	01	01	01	00	0	0	0	0	0	IB	Ia	IC-Ia	0
11	11	00	00	00	01	01	00	01	0	0	0	0	0	IB	-IA-Ic	0	Ic-IB
00	11	11	00	00	01	01	00	01	0	0	0	0	0	IB	Ia	0	IC-Ia
11	11	00	00	00	01	00	01	01	0	0	0	0	0	IB	0	-IA-Ic	Ic-IB
11	00	11	00	00	01	00	01	01	0	0	0	0	0	IB	0	Ib	IC-Ib
employ four capacitors																	
11	00	00	01	01	01	01	00	00	0	0	0	IB+Ia	Ib	Ic	IC	0	0
00	11	00	01	01	01	01	00	00	0	0	0	Ia-IC	Ib-IA	Ic	IC	0	0

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
00	00	11	01	01	01	01	00	00	0	0	0	Ia-IC	Ib	Ic-IA	IC	0	0
11	00	00	01	01	01	00	01	00	0	0	0	Ia-IA	Ib-IC	Ic	0	IC	0
00	11	00	01	01	01	00	01	00	0	0	0	Ia	IB+Ib	Ic	0	IC	0
00	00	11	01	01	01	00	01	00	0	0	0	Ia	Ib-IC	Ic-IA	0	IC	0
11	00	00	01	01	01	00	00	01	0	0	0	Ia-IA	Ib	Ic-IC	0	0	IC
00	11	00	01	01	01	00	00	01	0	0	0	Ia	Ib-IA	Ic-IC	0	0	IC
00	00	11	01	01	01	00	00	01	0	0	0	Ia	Ib	IB+Ic	0	0	IC
11	00	00	01	01	00	01	00	01	0	0	0	IB-Ib	Ib	0	IC-Ic	0	Ic
00	11	00	01	01	00	01	00	01	0	0	0	-IC-Ib	Ib-IA	0	IC-Ic	0	Ic
00	00	11	01	01	00	01	00	01	0	0	0	IB-Ib	Ib	0	-IB-Ic	0	Ic-IA
11	00	00	01	01	00	00	01	01	0	0	0	Ia-IA	-IC-Ia	0	0	IC-Ic	Ic
00	11	00	01	01	00	00	01	01	0	0	0	Ia	IB-Ia	0	0	IC-Ic	Ic
00	00	11	01	01	00	00	01	01	0	0	0	Ia	IB-Ia	0	0	-IB-Ic	Ic-IA
11	00	00	01	00	01	01	01	00	0	0	0	IB-Ic	0	Ic	IC-Ib	Ib	0
00	11	00	01	00	01	01	01	00	0	0	0	IB-Ic	0	Ic	-IB-Ib	Ib-IA	0
00	00	11	01	00	01	01	01	00	0	0	0	-IC-Ic	0	Ic-IA	IC-Ib	Ib	0
11	00	00	01	00	01	00	01	01	0	0	0	Ia-IA	0	-IC-Ia	0	Ib	IC-Ib
00	11	00	01	00	01	00	01	01	0	0	0	Ia	0	IB-Ia	0	Ib-IA	-IB-Ib
00	00	11	01	00	01	00	01	01	0	0	0	Ia	0	IB-Ia	0	Ib	IC-Ib
00	11	00	01	00	00	01	01	01	0	0	0	IB	0	0	Ia-IB	Ib-IA	Ic
11	00	00	01	00	00	01	01	01	0	0	0	IB	0	0	IC+Ia	Ib	Ic
00	00	11	01	00	00	01	01	01	0	0	0	IB	0	0	Ia-IB	Ib	Ic-IA
11	00	00	00	01	01	01	01	00	0	0	0	0	IB-Ic	Ic	Ia-IA	-IB-Ia	0
00	11	00	00	01	01	01	01	00	0	0	0	0	IB-Ic	Ic	Ia	IC-Ia	0
00	00	11	00	01	01	01	01	00	0	0	0	0	-IC-Ic	Ic-IA	Ia	IC-Ia	0
11	00	00	00	01	01	01	00	01	0	0	0	0	Ib	IB-Ib	Ia-IA	0	-IB-Ia
00	11	00	00	01	01	01	00	01	0	0	0	0	Ib-IA	-IC-Ib	Ia	0	IC-Ia
00	00	11	00	01	01	01	00	01	0	0	0	0	Ib	IB-Ib	Ia	0	IC-Ia
11	00	00	00	01	00	01	01	01	0	0	0	0	IB	0	Ia-IA	Ib-IB	Ic
00	11	00	00	01	00	01	01	01	0	0	0	0	IB	0	Ia	IC+Ib	Ic
00	00	11	00	01	00	01	01	01	0	0	0	0	IB	0	Ia	Ib-IB	Ic-IA
11	00	00	00	00	01	01	01	01	0	0	0	0	0	IB	Ia-IA	Ib	Ic-IB
00	11	00	00	00	01	01	01	01	0	0	0	0	0	IB	Ia	Ib-IA	Ic-IB
00	00	11	00	00	01	01	01	01	0	0	0	0	0	IB	Ia	Ib	IC+Ic

Table B.29: Switching device combinations for (V_{AB},V_{BC},V_{CA}) = ($-V_{cap}$,0,$+V_{cap}$) and (V_{ab},V_{bc},V_{ca}) = ($+V_{cap}$,0,$-V_{cap}$).

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
employ single capacitor																	
10	11	11	11	00	00	11	00	00	-IA-Ia	0	0	0	0	0	0	0	0
00	11	11	11	01	00	11	00	00	0	0	0	0	-IA-Ia	0	0	0	0
00	11	11	11	00	01	11	00	00	0	0	0	0	0	-IA-Ia	0	0	0
00	11	11	11	00	00	11	01	00	0	0	0	0	0	0	0	-IA-Ia	0
00	11	11	11	00	00	11	00	01	0	0	0	0	0	0	0	0	-IA-Ia
employ two capacitors																	
10	11	11	00	01	00	11	00	00	IC-Ia	0	0	0	IB	0	0	0	0
10	00	11	11	01	00	11	00	00	Ic-IA	0	0	0	Ib	0	0	0	0
10	11	11	00	00	01	11	00	00	IC-Ia	0	0	0	0	IB	0	0	0
10	11	00	11	00	01	11	00	00	Ib-IA	0	0	0	0	Ic	0	0	0
10	11	11	11	00	00	00	01	00	IB-Ia	0	0	0	0	0	0	IC	0
10	00	11	11	00	00	11	01	00	Ic-IA	0	0	0	0	0	0	Ib	0
10	11	11	11	00	00	00	00	01	IB-Ia	0	0	0	0	0	0	0	IC
10	11	00	11	00	00	11	00	01	Ib-IA	0	0	0	0	0	0	0	Ic
00	11	00	11	01	01	11	00	00	0	0	0	0	Ib-IA	Ic	0	0	0
00	00	11	11	01	01	11	00	00	0	0	0	0	Ib	Ic-IA	0	0	0
00	11	11	00	01	00	11	01	00	0	0	0	0	IB	0	0	IC-Ia	0
00	11	11	11	01	00	00	01	00	0	0	0	0	IB-Ia	0	0	IC	0
00	11	00	11	01	00	11	00	01	0	0	0	0	Ib-IA	0	0	0	Ic
00	00	11	11	01	00	11	00	01	0	0	0	0	Ib	0	0	0	Ic-IA
00	11	11	00	01	00	11	00	01	0	0	0	0	IB	0	0	0	IC-Ia
00	11	11	11	01	00	00	00	01	0	0	0	0	IB-Ia	0	0	0	IC
00	11	00	11	00	01	11	01	00	0	0	0	0	0	Ic	0	Ib-IA	0
00	00	11	11	00	01	11	01	00	0	0	0	0	0	Ic-IA	0	Ib	0
00	11	11	00	00	01	11	01	00	0	0	0	0	0	IB	0	IC-Ia	0
00	11	11	11	00	01	00	01	00	0	0	0	0	0	IB-Ia	0	IC	0
00	11	11	00	00	01	11	00	01	0	0	0	0	0	IB	0	0	IC-Ia
00	11	11	11	00	01	00	00	01	0	0	0	0	0	IB-Ia	0	0	IC
00	11	00	11	00	00	11	01	01	0	0	0	0	0	0	0	Ib-IA	Ic
00	00	11	11	00	00	11	01	01	0	0	0	0	0	0	0	Ib	Ic-IA
employ three capacitors																	
10	00	00	11	01	01	11	00	00	-IA	0	0	0	Ib	Ic	0	0	0
10	11	00	00	01	01	11	00	00	IC-Ia	0	0	0	IB-Ic	Ic	0	0	0
10	00	11	00	01	01	11	00	00	IC-Ia	0	0	0	Ib	IB-Ib	0	0	0
10	11	11	00	01	00	00	01	00	-Ia	0	0	0	IB	0	0	IC	0
10	00	11	00	01	00	11	01	00	Ic-IA	0	0	0	IB	0	0	Ib-IB	0
10	00	11	11	01	00	00	01	00	Ic-IA	0	0	0	Ib-IC	0	0	IC	0
10	00	00	11	01	00	11	00	01	-IA	0	0	0	Ib	0	0	0	Ic
10	11	00	00	01	00	11	00	01	IC+Ib	0	0	0	IB	0	0	0	Ic
10	11	11	00	01	00	00	00	01	-Ia	0	0	0	IB	0	0	0	IC
10	00	11	11	01	00	00	00	01	IB+Ic	0	0	0	Ib	0	0	0	IC

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
10	00	00	11	00	01	11	01	00	-IA	0	0	0	0	Ic	0	Ib	0
10	11	11	00	00	01	00	01	00	-Ia	0	0	0	0	IB	0	IC	0
10	00	11	00	00	01	11	01	00	IC+Ic	0	0	0	0	IB	0	Ib	0
10	11	00	11	00	01	00	01	00	IB+Ib	0	0	0	0	Ic	0	IC	0
10	11	11	00	00	01	00	00	01	-Ia	0	0	0	0	IB	0	0	IC
10	11	00	00	00	01	11	00	01	Ib-IA	0	0	0	0	IB	0	0	Ic-IB
10	11	00	11	00	01	00	00	01	Ib-IA	0	0	0	0	Ic-IC	0	0	IC
10	00	00	11	00	00	11	01	01	-IA	0	0	0	0	0	0	Ib	Ic
10	11	00	11	00	00	00	01	01	IB-Ia	0	0	0	0	0	0	IC-Ic	Ic
10	00	11	11	00	00	00	01	01	IB-Ia	0	0	0	0	0	0	Ib	IC-Ib
00	11	00	00	01	01	11	01	00	0	0	0	0	IB-Ic	Ic	0	IC-Ia	0
00	11	00	11	01	01	00	01	00	0	0	0	0	IB+Ib	Ic	0	IC	0
00	00	11	11	01	01	00	01	00	0	0	0	0	Ib-IC	Ic-IA	0	IC	0
00	11	00	00	01	01	11	00	01	0	0	0	0	Ib-IA	-IC-Ib	0	0	IC-Ia
00	00	11	00	01	01	11	01	00	0	0	0	0	-IC-Ic	Ic-IA	0	0	IC-Ia
00	00	11	00	01	01	11	00	01	0	0	0	0	Ib	IB-Ib	0	0	IC-Ia
00	11	00	11	01	01	00	00	01	0	0	0	0	Ib-IA	Ic-IC	0	0	IC
00	00	11	11	01	01	00	00	01	0	0	0	0	Ib	IB+Ic	0	0	IC
00	11	00	00	01	00	11	01	01	0	0	0	0	IB	0	0	IC+Ib	Ic
00	00	11	00	01	00	11	01	01	0	0	0	0	IB	0	0	Ib-IB	Ic-IA
00	11	00	11	01	00	00	01	01	0	0	0	0	IB-Ia	0	0	IC-Ic	Ic
00	00	11	11	01	00	00	01	01	0	0	0	0	IB-Ia	0	0	-IB-Ic	Ic-IA
00	11	00	00	00	01	11	01	01	0	0	0	0	0	IB	0	Ib-IA	Ic-IB
00	00	11	00	00	01	11	01	01	0	0	0	0	0	IB	0	Ib	IC+Ic
00	11	00	11	00	01	00	01	01	0	0	0	0	0	IB-Ia	0	Ib-IA	-IB-Ib
00	00	11	11	00	01	00	01	01	0	0	0	0	0	IB-Ia	0	Ib	IC-Ib
				employ four capacitors													
10	00	00	00	01	01	11	01	00	-IA	0	0	0	IB-Ic	Ic	0	-IB-Ia	0
10	00	00	11	01	01	00	01	00	-IA	0	0	0	Ib-IC	Ic	0	IC	0
10	11	00	00	01	01	00	01	00	-Ia	0	0	0	IB-Ic	Ic	0	IC	0
10	00	11	00	01	01	00	01	00	-Ia	0	0	0	Ib-IC	-IA-Ib	0	IC	0
10	00	00	00	01	01	11	00	01	-IA	0	0	0	Ib	IB-Ib	0	0	-IB-Ia
10	00	00	11	01	01	00	00	01	-IA	0	0	0	Ib	Ic-IC	0	0	IC
10	11	00	00	01	01	00	00	01	-Ia	0	0	0	-IA-Ic	Ic-IC	0	0	IC
10	00	11	00	01	01	00	00	01	-Ia	0	0	0	Ib	IB-Ib	0	0	IC
10	00	00	00	01	00	11	01	01	-IA	0	0	0	IB	0	0	Ib-IB	Ic
10	00	00	11	01	00	00	01	01	-IA	0	0	0	-IC-Ia	0	0	IC-Ic	Ic
10	11	00	00	01	00	00	01	01	-Ia	0	0	0	IB	0	0	IC-Ic	Ic
10	00	11	00	01	00	00	01	01	-Ia	0	0	0	IB	0	0	Ib-IB	-IA-Ib
10	00	00	00	00	01	11	01	01	-IA	0	0	0	0	IB	0	Ib	Ic-IB
10	00	00	11	00	01	00	01	01	-IA	0	0	0	0	-IC-Ia	0	Ib	IC-Ib
10	11	00	00	00	01	00	01	01	-Ia	0	0	0	0	IB	0	-IA-Ic	Ic-IB
10	00	11	00	00	01	00	01	01	-Ia	0	0	0	0	IB	0	Ib	IC-Ib

Table B.30: Switching device combinations for (V_{AB},V_{BC},V_{CA}) = ($-V_{cap}$,0,$+V_{cap}$) and (V_{ab},V_{bc},V_{ca}) = (0,$+V_{cap}$,$-V_{cap}$).

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
employ single capacitor																	
10	00	11	11	00	00	11	11	00	Ic-IA	0	0	0	0	0	0	0	0
10	00	11	00	11	00	11	11	00	Ic-IA	0	0	0	0	0	0	0	0
10	00	11	11	11	00	11	00	00	Ic-IA	0	0	0	0	0	0	0	0
10	00	11	11	11	00	00	11	00	Ic-IA	0	0	0	0	0	0	0	0
00	10	11	11	00	00	11	11	00	0	Ic-IA	0	0	0	0	0	0	0
00	10	11	00	11	00	11	11	00	0	Ic-IA	0	0	0	0	0	0	0
00	10	11	11	11	00	11	00	00	0	Ic-IA	0	0	0	0	0	0	0
00	10	11	11	11	00	00	11	00	0	Ic-IA	0	0	0	0	0	0	0
00	00	11	11	00	01	11	11	00	0	0	0	0	0	Ic-IA	0	0	0
00	00	11	00	11	01	11	11	00	0	0	0	0	0	Ic-IA	0	0	0
00	00	11	11	11	01	11	00	00	0	0	0	0	0	Ic-IA	0	0	0
00	00	11	11	11	01	00	11	00	0	0	0	0	0	Ic-IA	0	0	0
00	00	11	11	00	00	11	11	01	0	0	0	0	0	0	0	0	Ic-IA
00	00	11	00	11	00	11	11	01	0	0	0	0	0	0	0	0	Ic-IA
00	00	11	11	11	00	11	00	01	0	0	0	0	0	0	0	0	Ic-IA
00	00	11	11	11	00	00	11	01	0	0	0	0	0	0	0	0	Ic-IA
employ two capacitors																	
10	10	11	11	00	00	11	00	00	-IA-Ia	-Ib	0	0	0	0	0	0	0
10	10	11	11	00	00	00	11	00	IB-Ia	IC-Ib	0	0	0	0	0	0	0
10	10	11	00	11	00	11	00	00	IC-Ia	IB-Ib	0	0	0	0	0	0	0
10	10	11	00	11	00	00	11	00	-Ia	-IA-Ib	0	0	0	0	0	0	0
10	00	00	11	00	01	11	11	00	-IA	0	0	0	0	Ic	0	0	0
10	00	00	00	11	01	11	11	00	-IA	0	0	0	0	Ic	0	0	0
10	00	00	11	11	01	11	00	00	-IA	0	0	0	0	Ic	0	0	0
10	00	00	11	11	01	00	11	00	-IA	0	0	0	0	Ic	0	0	0
10	00	11	00	00	01	11	11	00	IC+Ic	0	0	0	0	IB	0	0	0
10	00	11	00	11	01	11	00	00	IC-Ia	0	0	0	0	IB-Ib	0	0	0
10	00	11	00	11	01	00	11	00	-Ia	0	0	0	0	-IA-Ib	0	0	0
10	00	00	11	00	00	11	11	01	-IA	0	0	0	0	0	0	0	Ic
10	00	00	00	11	00	11	11	01	-IA	0	0	0	0	0	0	0	Ic
10	00	00	11	11	00	11	00	01	-IA	0	0	0	0	0	0	0	Ic
10	00	00	11	11	00	00	11	01	-IA	0	0	0	0	0	0	0	Ic
10	00	11	11	00	00	00	11	01	IB-Ia	0	0	0	0	0	0	0	IC-Ib
10	00	11	00	11	00	00	11	01	-Ia	0	0	0	0	0	0	0	-IA-Ib
10	00	11	11	11	00	00	00	01	IB+Ic	0	0	0	0	0	0	0	IC
00	10	00	11	00	01	11	11	00	0	-IA	0	0	0	Ic	0	0	0
00	10	00	00	11	01	11	11	00	0	-IA	0	0	0	Ic	0	0	0
00	10	11	00	00	01	11	11	00	0	IC+Ic	0	0	0	IB	0	0	0
00	10	00	11	11	01	11	00	00	0	-IA	0	0	0	Ic	0	0	0
00	10	00	11	11	01	00	11	00	0	-IA	0	0	0	Ic	0	0	0
00	10	11	11	00	01	11	00	00	0	-Ib	0	0	0	-IA-Ia	0	0	0

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
00	10	11	11	00	01	00	11	00	0	IC-Ib	0	0	0	IB-Ia	0	0	0
00	10	00	11	00	00	11	11	01	0	-IA	0	0	0	0	0	0	Ic
00	10	00	00	11	00	11	11	01	0	-IA	0	0	0	0	0	0	Ic
00	10	00	11	11	00	11	00	01	0	-IA	0	0	0	0	0	0	Ic
00	10	00	11	11	00	00	11	01	0	-IA	0	0	0	0	0	0	Ic
00	10	11	11	00	00	11	00	01	0	-Ib	0	0	0	0	0	0	-IA-Ia
00	10	11	00	11	00	11	00	01	0	IB-Ib	0	0	0	0	0	0	IC-Ia
00	10	11	11	11	00	00	00	01	0	IB+Ic	0	0	0	0	0	0	IC
00	00	11	00	00	01	11	11	01	0	0	0	0	0	IB	0	0	IC+Ic
00	00	11	11	00	01	00	11	01	0	0	0	0	0	IB-Ia	0	0	IC-Ib
00	00	11	00	11	01	11	00	01	0	0	0	0	0	IB-Ib	0	0	IC-Ia
00	00	11	11	11	01	00	00	01	0	0	0	0	0	IB+Ic	0	0	IC
					employ three capacitors												
10	10	11	00	00	01	11	00	00	IC-Ia	-Ib	0	0	0	IB	0	0	0
10	10	11	00	00	01	00	11	00	-Ia	IC-Ib	0	0	0	IB	0	0	0
10	10	00	11	00	01	11	00	00	Ib-IA	-Ib	0	0	0	Ic	0	0	0
10	10	00	00	11	01	11	00	00	IC-Ia	IB+Ia	0	0	0	Ic	0	0	0
10	10	00	11	00	01	00	11	00	IB+Ib	IC-Ib	0	0	0	Ic	0	0	0
10	10	00	00	11	01	00	11	00	-Ia	Ia-IA	0	0	0	Ic	0	0	0
10	10	00	11	00	00	11	00	01	Ib-IA	-Ib	0	0	0	0	0	0	Ic
10	10	00	11	00	00	00	11	01	IB-Ia	IC+Ia	0	0	0	0	0	0	Ic
10	10	00	00	11	00	11	00	01	IC+Ib	IB-Ib	0	0	0	0	0	0	Ic
10	10	00	00	11	00	00	11	01	-Ia	Ia-IA	0	0	0	0	0	0	Ic
10	10	11	11	00	00	00	00	01	IB-Ia	-Ib	0	0	0	0	0	0	IC
10	10	11	00	11	00	00	00	01	-Ia	IB-Ib	0	0	0	0	0	0	IC
10	00	00	00	00	01	11	11	01	-IA	0	0	0	0	IB	0	0	Ic-IB
10	00	00	11	00	01	00	11	01	-IA	0	0	0	0	-IC-Ia	0	0	IC-Ib
10	00	00	00	11	01	11	00	01	-IA	0	0	0	0	IB-Ib	0	0	-IB-Ia
10	00	11	00	00	01	00	11	01	-Ia	0	0	0	0	IB	0	0	IC-Ib
10	00	00	11	11	01	00	00	01	-IA	0	0	0	0	Ic-IC	0	0	IC
10	00	11	00	11	01	00	00	01	-Ia	0	0	0	0	IB-Ib	0	0	IC
00	10	00	00	00	01	11	11	01	0	-IA	0	0	0	IB	0	0	Ic-IB
00	10	00	11	00	01	00	11	01	0	-IA	0	0	0	IB-Ia	0	0	-IB-Ib
00	10	00	00	11	01	11	00	01	0	-IA	0	0	0	-IC-Ib	0	0	IC-Ia
00	10	11	00	00	01	11	00	01	0	-Ib	0	0	0	IB	0	0	IC-Ia
00	10	00	11	11	01	00	00	01	0	-IA	0	0	0	Ic-IC	0	0	IC
00	10	11	11	00	01	00	00	01	0	-Ib	0	0	0	IB-Ia	0	0	IC
					employ four capacitors												
10	10	11	00	00	01	00	00	01	-Ia	-Ib	0	0	0	IB	0	0	IC
10	10	00	00	00	01	11	00	01	Ib-IA	-Ib	0	0	0	IB	0	0	Ic-IB
10	10	00	00	00	01	00	11	01	-Ia	Ia-IA	0	0	0	IB	0	0	Ic-IB
10	10	00	11	00	01	00	00	01	Ib-IA	-Ib	0	0	0	Ic-IC	0	0	IC
10	10	00	00	11	01	00	00	01	-Ia	Ia-IA	0	0	0	Ic-IC	0	0	IC

Table B.31: Switching device combinations for (V_{AB},V_{BC},V_{CA}) = ($-V_{cap}$,0,$+V_{cap}$) and (V_{ab},V_{bc},V_{ca}) = ($-V_{cap}$,$+V_{cap}$,0).

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
employ single capacitor																	
11	10	11	00	11	00	00	11	00	0	-IA-Ib	0	0	0	0	0	0	0
11	00	11	01	11	00	00	11	00	0	0	0	-IA-Ib	0	0	0	0	0
11	00	11	00	11	01	00	11	00	0	0	0	0	0	-IA-Ib	0	0	0
11	00	11	00	11	00	01	11	00	0	0	0	0	0	0	-IA-Ib	0	0
11	00	11	00	11	00	00	11	01	0	0	0	0	0	0	0	0	-IA-Ib
employ two capacitors																	
11	10	11	01	00	00	00	11	00	0	IC-Ib	0	IB	0	0	0	0	0
00	10	11	01	11	00	00	11	00	0	Ic-IA	0	Ia	0	0	0	0	0
11	10	11	00	00	01	00	11	00	0	IC-Ib	0	0	0	IB	0	0	0
11	10	00	00	11	01	00	11	00	0	Ia-IA	0	0	0	Ic	0	0	0
11	10	11	00	11	00	01	00	00	0	IB-Ib	0	0	0	0	IC	0	0
00	10	11	00	11	00	01	11	00	0	Ic-IA	0	0	0	0	Ia	0	0
11	10	11	00	11	00	00	00	01	0	IB-Ib	0	0	0	0	0	0	IC
11	10	00	00	11	00	00	11	01	0	Ia-IA	0	0	0	0	0	0	Ic
11	00	00	01	11	01	00	11	00	0	0	0	Ia-IA	0	Ic	0	0	0
00	00	11	01	11	01	00	11	00	0	0	0	Ia	0	Ic-IA	0	0	0
11	00	11	01	00	00	01	11	00	0	0	0	IB	0	0	IC-Ib	0	0
11	00	11	01	11	00	01	00	00	0	0	0	IB-Ib	0	0	IC	0	0
11	00	00	01	11	00	00	11	01	0	0	0	Ia-IA	0	0	0	0	Ic
00	00	11	01	11	00	00	11	01	0	0	0	Ia	0	0	0	0	Ic-IA
11	00	11	01	00	00	00	11	01	0	0	0	IB	0	0	0	0	IC-Ib
11	00	11	01	11	00	00	00	01	0	0	0	IB-Ib	0	0	0	0	IC
11	00	00	00	11	01	01	11	00	0	0	0	0	0	Ic	Ia-IA	0	0
00	00	11	00	11	01	01	11	00	0	0	0	0	0	Ic-IA	Ia	0	0
11	00	11	00	00	01	01	11	00	0	0	0	0	0	IB	IC-Ib	0	0
11	00	11	00	11	01	01	00	00	0	0	0	0	0	IB-Ib	IC	0	0
11	00	11	00	00	01	00	11	01	0	0	0	0	0	IB	0	0	IC-Ib
11	00	11	00	11	01	00	00	01	0	0	0	0	0	IB-Ib	0	0	IC
11	00	00	00	11	00	01	11	01	0	0	0	0	0	0	Ia-IA	0	Ic
00	00	11	00	11	00	01	11	01	0	0	0	0	0	0	Ia	0	Ic-IA
employ three capacitors																	
00	10	00	01	11	01	00	11	00	0	-IA	0	Ia	0	Ic	0	0	0
11	10	00	01	00	01	00	11	00	0	IC-Ib	0	IB-Ic	0	Ic	0	0	0
00	10	11	01	00	01	00	11	00	0	IC-Ib	0	Ia	0	IB-Ia	0	0	0
11	10	11	01	00	00	01	00	00	0	-Ib	0	IB	0	0	IC	0	0
00	10	11	01	00	00	01	11	00	0	Ic-IA	0	IB	0	0	Ia-IB	0	0
00	10	11	01	11	00	01	00	00	0	Ic-IA	0	Ia-IC	0	0	IC	0	0
00	10	00	01	11	00	00	11	01	0	-IA	0	Ia	0	0	0	0	Ic
11	10	11	01	00	00	00	00	01	0	-Ib	0	IB	0	0	0	0	IC
11	10	00	01	00	00	00	11	01	0	IC+Ia	0	IB	0	0	0	0	Ic
00	10	11	01	11	00	00	00	01	0	IB+Ic	0	Ia	0	0	0	0	IC

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
00	10	00	00	11	01	01	11	00	0	-IA	0	0	0	Ic	Ia	0	0
11	10	11	00	00	01	01	00	00	0	-Ib	0	0	0	IB	IC	0	0
00	10	11	00	00	01	01	11	00	0	IC+Ic	0	0	0	IB	Ia	0	0
11	10	00	00	11	01	01	00	00	0	IB+Ia	0	0	0	Ic	IC	0	0
11	10	11	00	00	01	00	00	01	0	-Ib	0	0	0	IB	0	0	IC
11	10	00	00	00	01	00	11	01	0	Ia-IA	0	0	0	IB	0	0	Ic-IB
11	10	00	00	11	01	00	00	01	0	Ia-IA	0	0	0	Ic-IC	0	0	IC
00	10	00	00	11	00	01	11	01	0	-IA	0	0	0	0	Ia	0	Ic
11	10	00	00	11	00	01	00	01	0	IB-Ib	0	0	0	0	IC-Ic	0	Ic
00	10	11	00	11	00	01	00	01	0	IB-Ib	0	0	0	0	Ia	0	IC-Ia
11	00	00	01	00	01	01	11	00	0	0	0	IB-Ic	0	Ic	IC-Ib	0	0
00	00	11	01	00	01	01	11	00	0	0	0	-IC-Ic	0	Ic-IA	IC-Ib	0	0
11	00	00	01	11	01	01	00	00	0	0	0	IB+Ia	0	Ic	IC	0	0
00	00	11	01	11	01	01	00	00	0	0	0	Ia-IC	0	Ic-IA	IC	0	0
11	00	00	01	00	01	00	11	01	0	0	0	Ia-IA	0	-IC-Ia	0	0	IC-Ib
00	00	11	01	00	01	00	11	01	0	0	0	Ia	0	IB-Ia	0	0	IC-Ib
11	00	00	01	11	01	00	00	01	0	0	0	Ia-IA	0	Ic-IC	0	0	IC
00	00	11	01	11	01	00	00	01	0	0	0	Ia	0	IB+Ic	0	0	IC
11	00	00	01	00	00	01	11	01	0	0	0	IB	0	0	IC+Ia	0	Ic
00	00	11	01	00	00	01	11	01	0	0	0	IB	0	0	Ia-IB	0	Ic-IA
11	00	00	01	11	00	01	00	01	0	0	0	IB-Ib	0	0	IC-Ic	0	Ic
00	00	11	01	11	00	01	00	01	0	0	0	IB-Ib	0	0	-IB-Ic	0	Ic-IA
11	00	00	00	00	01	01	11	01	0	0	0	0	0	IB	Ia-IA	0	Ic-IB
00	00	11	00	00	01	01	11	01	0	0	0	0	0	IB	Ia	0	IC+Ic
11	00	00	00	11	01	01	00	01	0	0	0	0	0	IB-Ib	Ia-IA	0	-IB-Ia
00	00	11	00	11	01	01	00	01	0	0	0	0	0	IB-Ib	Ia	0	IC-Ia
employ four capacitors																	
00	10	00	01	00	01	01	11	00	0	-IA	0	IB-Ic	0	Ic	-IB-Ib	0	0
00	10	00	01	11	01	01	00	00	0	-IA	0	Ia-IC	0	Ic	IC	0	0
11	10	00	01	00	01	01	00	00	0	-Ib	0	IB-Ic	0	Ic	IC	0	0
00	10	11	01	00	01	01	00	00	0	-Ib	0	Ia-IC	0	-IA-Ia	IC	0	0
00	10	00	01	00	01	00	11	01	0	-IA	0	Ia	0	IB-Ia	0	0	-IB-Ib
00	10	00	01	11	01	00	00	01	0	-IA	0	Ia	0	Ic-IC	0	0	IC
11	10	00	01	00	01	00	00	01	0	-Ib	0	-IA-Ic	0	Ic-IC	0	0	IC
00	10	11	01	00	01	00	00	01	0	-Ib	0	Ia	0	IB-Ia	0	0	IC
00	10	00	01	00	00	01	11	01	0	-IA	0	IB	0	0	Ia-IB	0	Ic
00	10	00	01	11	00	01	00	01	0	-IA	0	-IC-Ib	0	0	IC-Ic	0	Ic
11	10	00	01	00	00	01	00	01	0	-Ib	0	IB	0	0	IC-Ic	0	Ic
00	10	11	01	00	00	01	00	01	0	-Ib	0	IB	0	0	Ia-IB	0	-IA-Ia
00	10	00	00	00	01	01	11	01	0	-IA	0	0	0	IB	Ia	0	Ic-IB
00	10	00	00	11	01	01	00	01	0	-IA	0	0	0	-IC-Ib	Ia	0	IC-Ia
11	10	00	00	00	01	01	00	01	0	-Ib	0	0	0	IB	-IA-Ic	0	Ic-IB
00	10	11	00	00	01	01	00	01	0	-Ib	0	0	0	IB	Ia	0	IC-Ia

Table B.32: Switching device combinations for (V_{AB},V_{BC},V_{CA}) = ($-V_{cap}$,0,$+V_{cap}$) and (V_{ab},V_{bc},V_{ca}) = ($-V_{cap}$,0,$+V_{cap}$).

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
employ single capacitor																	
11	10	00	00	11	00	00	11	11	0	Ia-IA	0	0	0	0	0	0	0
11	10	00	00	00	11	00	11	11	0	Ia-IA	0	0	0	0	0	0	0
11	10	00	00	11	11	00	11	00	0	Ia-IA	0	0	0	0	0	0	0
11	10	00	00	11	11	00	00	11	0	Ia-IA	0	0	0	0	0	0	0
11	00	10	00	11	00	00	11	11	0	0	Ia-IA	0	0	0	0	0	0
11	00	10	00	00	11	00	11	11	0	0	Ia-IA	0	0	0	0	0	0
11	00	10	00	11	11	00	11	00	0	0	Ia-IA	0	0	0	0	0	0
11	00	10	00	11	11	00	00	11	0	0	Ia-IA	0	0	0	0	0	0
11	00	00	01	11	00	00	11	11	0	0	0	Ia-IA	0	0	0	0	0
11	00	00	01	00	11	00	11	11	0	0	0	Ia-IA	0	0	0	0	0
11	00	00	01	11	11	00	11	00	0	0	0	Ia-IA	0	0	0	0	0
11	00	00	01	11	11	00	00	11	0	0	0	Ia-IA	0	0	0	0	0
11	00	00	00	11	00	01	11	11	0	0	0	0	0	0	Ia-IA	0	0
11	00	00	00	00	11	01	11	11	0	0	0	0	0	0	Ia-IA	0	0
11	00	00	00	11	11	01	11	00	0	0	0	0	0	0	Ia-IA	0	0
11	00	00	00	11	11	01	00	11	0	0	0	0	0	0	Ia-IA	0	0
employ two capacitors																	
11	10	10	00	11	00	00	11	00	0	-IA-Ib	-Ic	0	0	0	0	0	0
11	10	10	00	11	00	00	00	11	0	IB-Ib	IC-Ic	0	0	0	0	0	0
11	10	10	00	00	11	00	11	00	0	IC-Ib	IB-Ic	0	0	0	0	0	0
11	10	10	00	00	11	00	00	11	0	-Ib	-IA-Ic	0	0	0	0	0	0
00	10	00	01	11	00	00	11	11	0	-IA	0	Ia	0	0	0	0	0
00	10	00	01	00	11	00	11	11	0	-IA	0	Ia	0	0	0	0	0
11	10	00	01	00	00	00	11	11	0	IC+Ia	0	IB	0	0	0	0	0
00	10	00	01	11	11	00	11	00	0	-IA	0	Ia	0	0	0	0	0
00	10	00	01	11	11	00	00	11	0	-IA	0	Ia	0	0	0	0	0
11	10	00	01	00	11	00	11	00	0	IC-Ib	0	IB-Ic	0	0	0	0	0
11	10	00	01	00	11	00	00	11	0	-Ib	0	-IA-Ic	0	0	0	0	0
00	10	00	00	11	00	01	11	11	0	-IA	0	0	0	0	Ia	0	0
00	10	00	00	00	11	01	11	11	0	-IA	0	0	0	0	Ia	0	0
00	10	00	00	11	11	01	11	00	0	-IA	0	0	0	0	Ia	0	0
00	10	00	00	11	11	01	00	11	0	-IA	0	0	0	0	Ia	0	0
11	10	00	00	11	00	01	00	11	0	IB-Ib	0	0	0	0	IC-Ic	0	0
11	10	00	00	00	11	01	00	11	0	-Ib	0	0	0	0	-IA-Ic	0	0
11	10	00	00	11	11	01	00	00	0	IB+Ia	0	0	0	0	IC	0	0
00	00	10	01	11	00	00	11	11	0	0	-IA	Ia	0	0	0	0	0
00	00	10	01	00	11	00	11	11	0	0	-IA	Ia	0	0	0	0	0
11	00	10	01	00	00	00	11	11	0	0	IC+Ia	IB	0	0	0	0	0
00	00	10	01	11	11	00	11	00	0	0	-IA	Ia	0	0	0	0	0
00	00	10	01	11	11	00	00	11	0	0	-IA	Ia	0	0	0	0	0
11	00	10	01	11	00	00	11	00	0	0	-Ic	-IA-Ib	0	0	0	0	0

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
11	00	10	01	11	00	00	00	11	0	0	IC-Ic	IB-Ib	0	0	0	0	0
00	00	10	00	11	00	01	11	11	0	0	-IA	0	0	0	Ia	0	0
00	00	10	00	00	11	01	11	11	0	0	-IA	0	0	0	Ia	0	0
00	00	10	00	11	11	01	11	00	0	0	-IA	0	0	0	Ia	0	0
00	00	10	00	11	11	01	00	11	0	0	-IA	0	0	0	Ia	0	0
11	00	10	00	11	00	01	11	00	0	0	-Ic	0	0	0	-IA-Ib	0	0
11	00	10	00	00	11	01	11	00	0	0	IB-Ic	0	0	0	IC-Ib	0	0
11	00	10	00	11	11	01	00	00	0	0	IB+Ia	0	0	0	IC	0	0
11	00	00	01	00	00	01	11	11	0	0	0	IB	0	0	IC+Ia	0	0
11	00	00	01	11	00	01	00	11	0	0	0	IB-Ib	0	0	IC-Ic	0	0
11	00	00	01	00	11	01	11	00	0	0	0	IB-Ic	0	0	IC-Ib	0	0
11	00	00	01	11	11	01	00	00	0	0	0	IB+Ia	0	0	IC	0	0
employ three capacitors																	
11	10	10	01	00	00	00	11	00	0	IC-Ib	-Ic	IB	0	0	0	0	0
11	10	10	01	00	00	00	00	11	0	-Ib	IC-Ic	IB	0	0	0	0	0
00	10	01	01	11	00	00	11	00	0	Ic-IA	Ic	Ia	0	0	0	0	0
00	10	10	01	00	11	00	11	00	0	IC-Ib	IB+Ib	Ia	0	0	0	0	0
00	10	10	01	11	00	00	00	11	0	IB+Ic	IC-Ic	Ia	0	0	0	0	0
00	10	10	01	00	11	00	00	11	0	-Ib	Ib-IA	Ia	0	0	0	0	0
11	10	10	00	11	00	01	00	00	0	IB-Ib	-Ic	0	0	0	IC	0	0
11	10	10	00	00	11	01	00	00	0	-Ib	IB-Ic	0	0	0	IC	0	0
00	10	10	00	11	00	01	11	00	0	Ic-IA	-Ic	0	0	0	Ia	0	0
00	10	10	00	11	00	01	00	11	0	IB-Ib	IC+Ib	0	0	0	Ia	0	0
00	10	10	00	00	11	01	11	00	0	IC+Ic	IB-Ic	0	0	0	Ia	0	0
00	10	10	00	00	11	01	00	11	0	-Ib	Ib-IA	0	0	0	Ia	0	0
00	10	00	01	00	00	01	11	11	0	-IA	0	IB	0	0	Ia-IB	0	0
00	10	00	01	11	00	01	00	11	0	-IA	0	-IC-Ib	0	0	IC-Ic	0	0
00	10	00	01	00	11	01	11	00	0	-IA	0	IB-Ic	0	0	-IB-Ib	0	0
11	10	00	01	00	00	01	00	11	0	-Ib	0	IB	0	0	IC-Ic	0	0
00	10	00	01	11	11	01	00	00	0	-IA	0	Ia-IC	0	0	IC	0	0
11	10	00	01	00	11	01	00	00	0	-Ib	0	IB-Ic	0	0	IC	0	0
00	00	10	01	00	00	01	11	11	0	0	-IA	IB	0	0	Ia-IB	0	0
00	00	10	01	11	00	01	00	11	0	0	-IA	IB-Ib	0	0	-IB-Ic	0	0
00	00	10	01	00	11	01	11	00	0	0	-IA	-IC-Ic	0	0	IC-Ib	0	0
11	00	10	01	00	00	01	11	00	0	0	-Ic	IB	0	0	IC-Ib	0	0
00	00	10	01	11	11	01	00	00	0	0	-IA	Ia-IC	0	0	IC	0	0
11	00	10	01	11	00	01	00	00	0	0	-Ic	IB-Ib	0	0	IC	0	0
employ four capacitors																	
11	10	10	01	00	00	01	00	00	0	-Ib	-Ic	IB	0	0	IC	0	0
00	10	10	01	00	00	01	11	00	0	Ic-IA	-Ic	IB	0	0	Ia-IB	0	0
00	10	10	01	00	00	01	00	11	0	-Ib	Ib-IA	IB	0	0	Ia-IB	0	0
00	10	10	01	11	00	01	00	00	0	Ic-IA	-Ic	Ia-IC	0	0	IC	0	0
00	10	10	01	00	11	01	00	00	0	-Ib	Ib-IA	Ia-IC	0	0	IC	0	0

Table B.33: Switching device combinations for (V_{AB},V_{BC},V_{CA}) = ($-V_{cap}$,0,$+V_{cap}$) and (V_{ab},V_{bc},V_{ca}) = (0,$-V_{cap}$,$+V_{cap}$).

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
employ single capacitor																	
11	11	10	00	00	11	00	00	11	0	0	-IA-Ic	0	0	0	0	0	0
11	11	00	01	00	11	00	00	11	0	0	0	-IA-Ic	0	0	0	0	0
11	11	00	00	01	11	00	00	11	0	0	0	0	-IA-Ic	0	0	0	0
11	11	00	00	00	11	01	00	11	0	0	0	0	0	0	-IA-Ic	0	0
11	11	00	00	00	11	00	01	11	0	0	0	0	0	0	0	-IA-Ic	0
employ two capacitors																	
11	11	10	01	00	00	00	00	11	0	0	IC-Ic	IB	0	0	0	0	0
00	11	10	01	00	11	00	00	11	0	0	Ib-IA	Ia	0	0	0	0	0
11	11	10	00	01	00	00	00	11	0	0	IC-Ic	0	IB	0	0	0	0
11	00	10	00	01	11	00	00	11	0	0	Ia-IA	0	Ib	0	0	0	0
11	11	10	00	00	11	01	00	00	0	0	IB-Ic	0	0	0	IC	0	0
00	11	10	00	00	11	01	00	11	0	0	Ib-IA	0	0	0	Ia	0	0
11	11	10	00	00	11	00	01	00	0	0	IB-Ic	0	0	0	0	IC	0
11	00	10	00	00	11	00	01	11	0	0	Ia-IA	0	0	0	0	Ib	0
11	00	00	01	01	11	00	00	11	0	0	0	Ia-IA	Ib	0	0	0	0
00	11	00	01	01	11	00	00	11	0	0	0	Ia	Ib-IA	0	0	0	0
11	11	00	01	00	00	01	00	11	0	0	0	IB	0	0	IC-Ic	0	0
11	11	00	01	00	11	01	00	00	0	0	0	IB-Ic	0	0	IC	0	0
11	00	00	01	00	11	00	01	11	0	0	0	Ia-IA	0	0	0	Ib	0
00	11	00	01	00	11	00	01	11	0	0	0	Ia	0	0	0	Ib-IA	0
11	11	00	01	00	00	00	01	11	0	0	0	IB	0	0	0	IC-Ic	0
11	11	00	01	00	11	00	01	00	0	0	0	IB-Ic	0	0	0	IC	0
11	00	00	00	01	11	01	00	11	0	0	0	0	Ib	0	Ia-IA	0	0
00	11	00	00	01	11	01	00	11	0	0	0	0	Ib-IA	0	Ia	0	0
11	11	00	00	01	00	01	00	11	0	0	0	0	IB	0	IC-Ic	0	0
11	11	00	00	01	11	01	00	00	0	0	0	0	IB-Ic	0	IC	0	0
11	11	00	00	01	00	00	01	11	0	0	0	0	IB	0	0	IC-Ic	0
11	11	00	00	01	11	00	01	00	0	0	0	0	IB-Ic	0	0	IC	0
11	00	00	00	00	11	01	01	11	0	0	0	0	0	0	Ia-IA	Ib	0
00	11	00	00	00	11	01	01	11	0	0	0	0	0	0	Ia	Ib-IA	0
employ three capacitors																	
00	00	10	01	01	11	00	00	11	0	0	-IA	Ia	Ib	0	0	0	0
11	00	10	01	01	00	00	00	11	0	0	IC-Ic	IB-Ib	Ib	0	0	0	0
00	11	10	01	01	00	00	00	11	0	0	IC-Ic	Ia	IB-Ia	0	0	0	0
11	11	10	01	00	00	01	00	00	0	0	-Ic	IB	0	0	IC	0	0
00	11	10	01	00	00	01	00	11	0	0	Ib-IA	IB	0	0	Ia-IB	0	0
00	11	10	01	00	11	01	00	00	0	0	Ib-IA	Ia-IC	0	0	IC	0	0
00	00	10	01	00	11	00	01	11	0	0	-IA	Ia	0	0	0	Ib	0
11	11	10	01	00	00	00	01	00	0	0	-Ic	IB	0	0	0	IC	0
11	00	10	01	00	00	00	01	11	0	0	IC+Ia	IB	0	0	0	Ib	0
00	11	10	01	00	11	00	01	00	0	0	IB+Ib	Ia	0	0	0	IC	0

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
00	00	10	00	01	11	01	00	11	0	0	-IA	0	Ib	0	Ia	0	0
11	11	10	00	01	00	01	00	00	0	0	-Ic	0	IB	0	IC	0	0
00	11	10	00	01	00	01	00	11	0	0	IC+Ib	0	IB	0	Ia	0	0
11	00	10	00	01	11	01	00	00	0	0	IB+Ia	0	Ib	0	IC	0	0
11	11	10	00	01	00	00	01	00	0	0	-Ic	0	IB	0	0	IC	0
11	00	10	00	01	00	00	01	11	0	0	Ia-IA	0	IB	0	0	Ib-IB	0
11	00	10	00	01	11	00	01	00	0	0	Ia-IA	0	Ib-IC	0	0	IC	0
00	00	10	00	00	11	01	01	11	0	0	-IA	0	0	0	Ia	Ib	0
11	00	10	00	00	11	01	01	00	0	0	IB-Ic	0	0	0	IC-Ib	Ib	0
00	11	10	00	00	11	01	01	00	0	0	IB-Ic	0	0	0	Ia	IC-Ia	0
11	00	00	01	01	00	01	00	11	0	0	0	IB-Ib	Ib	0	IC-Ic	0	0
00	11	00	01	01	00	01	00	11	0	0	0	-IC-Ib	Ib-IA	0	IC-Ic	0	0
11	00	00	01	01	11	01	00	00	0	0	0	IB+Ia	Ib	0	IC	0	0
00	11	00	01	01	11	01	00	00	0	0	0	Ia-IC	Ib-IA	0	IC	0	0
11	00	00	01	01	00	00	01	11	0	0	0	Ia-IA	-IC-Ia	0	0	IC-Ic	0
00	11	00	01	01	00	00	01	11	0	0	0	Ia	IB-Ia	0	0	IC-Ic	0
11	00	00	01	01	11	00	01	00	0	0	0	Ia-IA	Ib-IC	0	0	IC	0
00	11	00	01	01	11	00	01	00	0	0	0	Ia	IB+Ib	0	0	IC	0
11	00	00	01	00	00	01	01	11	0	0	0	IB	0	0	IC+Ia	Ib	0
00	11	00	01	00	00	01	01	11	0	0	0	IB	0	0	Ia-IB	Ib-IA	0
00	11	00	00	01	00	01	01	11	0	0	0	IB	0	0	Ia	IC+Ib	0
11	00	00	01	00	11	01	01	00	0	0	0	IB-Ic	0	0	IC-Ib	Ib	0
00	11	00	01	00	11	01	01	00	0	0	0	IB-Ic	0	0	-IB-Ib	Ib-IA	0
11	00	00	00	01	00	01	01	11	0	0	0	0	IB	0	Ia-IA	Ib-IB	0
11	00	00	00	01	11	01	01	00	0	0	0	0	IB-Ic	0	Ia-IA	-IB-Ia	0
00	11	00	00	01	11	01	01	00	0	0	0	0	IB-Ic	0	Ia	IC-Ia	0
employ four capacitors																	
00	00	10	01	01	00	01	00	11	0	0	-IA	IB-Ib	Ib	0	-IB-Ic	0	0
00	00	10	01	01	11	01	00	00	0	0	-IA	Ia-IC	Ib	0	IC	0	0
11	00	10	01	01	00	01	00	00	0	0	-Ic	IB-Ib	Ib	0	IC	0	0
00	11	10	01	01	00	01	00	00	0	0	-Ic	Ia-IC	-IA-Ia	0	IC	0	0
00	00	10	01	01	00	00	01	11	0	0	-IA	Ia	IB-Ia	0	0	-IB-Ic	0
00	00	10	01	01	11	00	01	00	0	0	-IA	Ia	Ib-IC	0	0	IC	0
11	00	10	01	01	00	00	01	00	0	0	-Ic	-IA-Ib	Ib-IC	0	0	IC	0
00	11	10	01	01	00	00	01	00	0	0	-Ic	Ia	IB-Ia	0	0	IC	0
00	00	10	01	00	00	01	01	11	0	0	-IA	IB	0	0	Ia-IB	Ib	0
00	00	10	01	00	11	01	01	00	0	0	-IA	-IC-Ic	0	0	IC-Ib	Ib	0
11	00	10	01	00	00	01	01	00	0	0	-Ic	IB	0	0	IC-Ib	Ib	0
00	11	10	01	00	00	01	01	00	0	0	-Ic	IB	0	0	Ia-IB	-IA-Ia	0
00	00	10	00	01	11	01	01	00	0	0	-IA	0	-IC-Ic	0	Ia	IC-Ia	0
00	00	10	00	01	00	01	01	11	0	0	-IA	0	IB	0	Ia	Ib-IB	0
11	00	10	00	01	00	01	01	00	0	0	-Ic	0	IB	0	-IA-Ib	Ib-IB	0
00	11	10	00	01	00	01	01	00	0	0	-Ic	0	IB	0	Ia	IC-Ia	0

Table B.34: Switching device combinations for (V_{AB},V_{BC},V_{CA}) = ($-V_{cap}$,0,$+V_{cap}$) and (V_{ab},V_{bc},V_{ca}) = ($+V_{cap}$,$-V_{cap}$,0).

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
employ single capacitor																	
10	11	00	11	00	00	11	00	11	Ib-IA	0	0	0	0	0	0	0	0
10	11	00	00	00	11	11	00	11	Ib-IA	0	0	0	0	0	0	0	0
10	11	00	11	00	11	11	00	00	Ib-IA	0	0	0	0	0	0	0	0
10	11	00	11	00	11	00	00	11	Ib-IA	0	0	0	0	0	0	0	0
00	11	10	11	00	00	11	00	11	0	0	Ib-IA	0	0	0	0	0	0
00	11	10	00	00	11	11	00	11	0	0	Ib-IA	0	0	0	0	0	0
00	11	10	11	00	11	11	00	00	0	0	Ib-IA	0	0	0	0	0	0
00	11	10	11	00	11	00	00	11	0	0	Ib-IA	0	0	0	0	0	0
00	11	00	00	01	11	11	00	11	0	0	0	0	Ib-IA	0	0	0	0
00	11	00	11	01	00	11	00	11	0	0	0	0	Ib-IA	0	0	0	0
00	11	00	11	01	11	11	00	00	0	0	0	0	Ib-IA	0	0	0	0
00	11	00	11	01	11	00	00	11	0	0	0	0	Ib-IA	0	0	0	0
00	11	00	11	00	00	11	01	11	0	0	0	0	0	0	0	Ib-IA	0
00	11	00	00	00	11	11	01	11	0	0	0	0	0	0	0	Ib-IA	0
00	11	00	11	00	11	11	01	00	0	0	0	0	0	0	0	Ib-IA	0
00	11	00	11	00	11	00	01	11	0	0	0	0	0	0	0	Ib-IA	0
employ two capacitors																	
10	11	10	11	00	00	11	00	00	-IA-Ia	0	-Ic	0	0	0	0	0	0
10	11	10	11	00	00	00	00	11	IB-Ia	0	IC-Ic	0	0	0	0	0	0
10	11	10	00	00	11	11	00	00	IC-Ia	0	IB-Ic	0	0	0	0	0	0
10	11	10	00	00	11	00	00	11	-Ia	0	-IA-Ic	0	0	0	0	0	0
10	00	00	11	01	00	11	00	11	-IA	0	0	0	Ib	0	0	0	0
10	00	00	00	01	11	11	00	11	-IA	0	0	0	Ib	0	0	0	0
10	11	00	00	01	00	11	00	11	IC+Ib	0	0	0	IB	0	0	0	0
10	00	00	11	01	11	11	00	00	-IA	0	0	0	Ib	0	0	0	0
10	00	00	11	01	11	00	00	11	-IA	0	0	0	Ib	0	0	0	0
10	11	00	00	01	11	11	00	00	IC-Ia	0	0	0	IB-Ic	0	0	0	0
10	11	00	00	01	11	00	00	11	-Ia	0	0	0	-IA-Ic	0	0	0	0
10	00	00	11	00	00	11	01	11	-IA	0	0	0	0	0	0	Ib	0
10	00	00	00	00	11	11	01	11	-IA	0	0	0	0	0	0	Ib	0
10	00	00	11	00	11	11	01	00	-IA	0	0	0	0	0	0	Ib	0
10	00	00	11	00	11	00	01	11	-IA	0	0	0	0	0	0	Ib	0
10	11	00	11	00	00	00	01	11	IB-Ia	0	0	0	0	0	0	IC-Ic	0
10	11	00	00	00	11	00	01	11	-Ia	0	0	0	0	0	0	-IA-Ic	0
10	11	00	11	00	11	00	01	00	IB+Ib	0	0	0	0	0	0	IC	0
00	00	10	11	01	00	11	00	11	0	0	-IA	0	Ib	0	0	0	0
00	00	10	00	01	11	11	00	11	0	0	-IA	0	Ib	0	0	0	0
00	11	10	00	01	00	11	00	11	0	0	IC+Ib	0	IB	0	0	0	0
00	00	10	11	01	11	11	00	00	0	0	-IA	0	Ib	0	0	0	0
00	00	10	11	01	11	00	00	11	0	0	-IA	0	Ib	0	0	0	0
00	11	10	11	01	00	11	00	00	0	0	-Ic	0	-IA-Ia	0	0	0	0

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
00	11	10	11	01	00	00	00	11	0	0	IC-Ic	0	IB-Ia	0	0	0	0
00	00	10	11	00	00	11	01	11	0	0	-IA	0	0	0	0	Ib	0
00	00	10	00	00	11	11	01	11	0	0	-IA	0	0	0	0	Ib	0
00	00	10	11	00	11	11	01	00	0	0	-IA	0	0	0	0	Ib	0
00	00	10	11	00	11	00	01	11	0	0	-IA	0	0	0	0	Ib	0
00	11	10	11	00	00	11	01	00	0	0	-Ic	0	0	0	0	-IA-Ia	0
00	11	10	00	00	11	11	01	00	0	0	IB-Ic	0	0	0	0	IC-Ia	0
00	11	10	11	00	11	00	01	00	0	0	IB+Ib	0	0	0	0	IC	0
00	11	00	00	01	00	11	01	11	0	0	0	0	IB	0	0	IC+Ib	0
00	11	00	11	01	00	00	01	11	0	0	0	0	IB-Ia	0	0	IC-Ic	0
00	11	00	00	01	11	11	01	00	0	0	0	0	IB-Ic	0	0	IC-Ia	0
00	11	00	11	01	11	00	01	00	0	0	0	0	IB+Ib	0	0	IC	0
employ three capacitors																	
10	00	10	00	01	00	11	00	00	IC-Ia	0	-Ic	0	IB	0	0	0	0
10	11	10	00	01	00	00	00	11	-Ia	0	IC-Ic	0	IB	0	0	0	0
10	00	10	11	01	00	11	00	00	Ic-IA	0	-Ic	0	Ib	0	0	0	0
10	00	10	00	01	11	11	00	00	IC-Ia	0	IB+Ia	0	Ib	0	0	0	0
10	00	10	11	01	00	00	00	11	IB+Ic	0	IC-Ic	0	Ib	0	0	0	0
10	00	10	00	01	11	00	00	11	-Ia	0	Ia-IA	0	Ib	0	0	0	0
10	11	10	11	00	00	00	01	00	IB-Ia	0	-Ic	0	0	0	0	IC	0
10	11	10	00	00	11	00	01	00	-Ia	0	IB-Ic	0	0	0	0	IC	0
10	00	10	11	00	00	11	01	00	Ic-IA	0	-Ic	0	0	0	0	Ib	0
10	00	10	11	00	00	00	01	11	IB-Ia	0	IC+Ia	0	0	0	0	Ib	0
10	00	10	00	00	11	11	01	00	IC+Ic	0	IB-Ic	0	0	0	0	Ib	0
10	00	10	00	00	11	00	01	11	-Ia	0	Ia-IA	0	0	0	0	Ib	0
10	00	00	00	01	00	11	01	11	-IA	0	0	0	IB	0	0	Ib-IB	0
10	00	00	11	01	00	00	01	11	-IA	0	0	0	-IC-Ia	0	0	IC-Ic	0
10	00	00	00	01	11	11	01	00	-IA	0	0	0	IB-Ic	0	0	-IB-Ia	0
10	11	00	00	01	00	00	01	11	-Ia	0	0	0	IB	0	0	IC-Ic	0
10	00	00	11	01	11	00	01	00	-IA	0	0	0	Ib-IC	0	0	IC	0
10	11	00	00	01	11	00	01	00	-Ia	0	0	0	IB-Ic	0	0	IC	0
00	00	10	00	01	00	11	01	11	0	0	-IA	0	IB	0	0	Ib-IB	0
00	00	10	11	01	00	00	01	11	0	0	-IA	0	IB-Ia	0	0	-IB-Ic	0
00	00	10	00	01	11	11	01	00	0	0	-IA	0	-IC-Ic	0	0	IC-Ia	0
00	11	10	00	01	00	11	01	00	0	0	-Ic	0	IB	0	0	IC-Ia	0
00	00	10	11	01	11	00	01	00	0	0	-IA	0	Ib-IC	0	0	IC	0
00	11	10	11	01	00	00	01	00	0	0	-Ic	0	IB-Ia	0	0	IC	0
employ four capacitors																	
10	11	10	00	01	00	00	01	00	-Ia	0	-Ic	0	IB	0	0	IC	0
10	00	10	00	01	00	11	01	00	Ic-IA	0	-Ic	0	IB	0	0	Ib-IB	0
10	00	10	00	01	00	00	01	11	-Ia	0	Ia-IA	0	IB	0	0	Ib-IB	0
10	00	10	11	01	00	00	01	00	Ic-IA	0	-Ic	0	Ib-IC	0	0	IC	0
10	00	10	00	01	11	00	01	00	-Ia	0	Ia-IA	0	Ib-IC	0	0	IC	0

Table B.35: Switching device combinations for (V_{AB},V_{BC},V_{CA}) = (0,$-V_{cap}$,$+V_{cap}$) and (V_{ab},V_{bc},V_{ca}) = (0,0,0).

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
employ single capacitor																	
11	11	11	11	00	00	01	00	00	0	0	0	0	0	0	IC	0	0
11	11	11	00	11	00	01	00	00	0	0	0	0	0	0	IC	0	0
11	11	11	00	00	11	01	00	00	0	0	0	0	0	0	IC	0	0
11	00	00	11	11	11	01	00	00	0	0	0	0	0	0	IC	0	0
00	11	00	11	11	11	01	00	00	0	0	0	0	0	0	IC	0	0
00	00	11	11	11	11	01	00	00	0	0	0	0	0	0	IC	0	0
11	11	00	11	00	11	01	00	00	0	0	0	0	0	0	IC	0	0
11	11	00	00	11	11	01	00	00	0	0	0	0	0	0	IC	0	0
11	00	11	11	11	00	01	00	00	0	0	0	0	0	0	IC	0	0
11	00	11	00	11	11	01	00	00	0	0	0	0	0	0	IC	0	0
00	11	11	11	11	00	01	00	00	0	0	0	0	0	0	IC	0	0
00	11	11	11	00	11	01	00	00	0	0	0	0	0	0	IC	0	0
11	11	11	11	00	00	00	01	00	0	0	0	0	0	0	0	IC	0
11	11	11	00	11	00	00	01	00	0	0	0	0	0	0	0	IC	0
11	11	11	00	00	11	00	01	00	0	0	0	0	0	0	0	IC	0
11	00	00	11	11	11	00	01	00	0	0	0	0	0	0	0	IC	0
00	11	00	11	11	11	00	01	00	0	0	0	0	0	0	0	IC	0
00	00	11	11	11	11	00	01	00	0	0	0	0	0	0	0	IC	0
11	11	00	11	00	11	00	01	00	0	0	0	0	0	0	0	IC	0
11	11	00	00	11	11	00	01	00	0	0	0	0	0	0	0	IC	0
11	00	11	11	11	00	00	01	00	0	0	0	0	0	0	0	IC	0
11	00	11	00	11	11	00	01	00	0	0	0	0	0	0	0	IC	0
00	11	11	11	11	00	00	01	00	0	0	0	0	0	0	0	IC	0
00	11	11	11	00	11	00	01	00	0	0	0	0	0	0	0	IC	0
11	11	11	00	00	11	00	00	01	0	0	0	0	0	0	0	0	IC
11	11	11	11	00	00	00	00	01	0	0	0	0	0	0	0	0	IC
11	11	11	00	11	00	00	00	01	0	0	0	0	0	0	0	0	IC
11	00	00	11	11	11	00	00	01	0	0	0	0	0	0	0	0	IC
00	11	00	11	11	11	00	00	01	0	0	0	0	0	0	0	0	IC
00	00	11	11	11	11	00	00	01	0	0	0	0	0	0	0	0	IC
11	11	00	11	00	11	00	00	01	0	0	0	0	0	0	0	0	IC
11	11	00	00	11	11	00	00	01	0	0	0	0	0	0	0	0	IC
11	00	11	11	11	00	00	00	01	0	0	0	0	0	0	0	0	IC
11	00	11	00	11	11	00	00	01	0	0	0	0	0	0	0	0	IC
00	11	11	11	11	00	00	00	01	0	0	0	0	0	0	0	0	IC
00	11	11	11	00	11	00	00	01	0	0	0	0	0	0	0	0	IC
employ two capacitors																	
10	00	00	10	00	00	11	11	11	-IA	0	0	-IB	0	0	0	0	0
10	00	00	00	10	00	11	11	11	-IA	0	0	0	-IB	0	0	0	0
10	00	00	00	00	10	11	11	11	-IA	0	0	0	0	-IB	0	0	0
00	10	00	10	00	00	11	11	11	0	-IA	0	-IB	0	0	0	0	0

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
00	10	00	00	10	00	11	11	11	0	-IA	0	0	-IB	0	0	0	0
00	10	00	00	00	10	11	11	11	0	-IA	0	0	0	-IB	0	0	0
00	00	10	10	00	00	11	11	11	0	0	-IA	-IB	0	0	0	0	0
00	00	10	00	10	00	11	11	11	0	0	-IA	0	-IB	0	0	0	0
00	00	10	00	00	10	11	11	11	0	0	-IA	0	0	-IB	0	0	0
11	00	00	11	00	11	01	01	00	0	0	0	0	0	0	IC-Ib	Ib	0
11	00	00	00	11	11	01	01	00	0	0	0	0	0	0	Ia-IA	-IB-Ia	0
00	11	00	11	00	11	01	01	00	0	0	0	0	0	0	-IB-Ib	Ib-IA	0
00	11	00	00	11	11	01	01	00	0	0	0	0	0	0	Ia	IC-Ia	0
00	00	11	11	00	11	01	01	00	0	0	0	0	0	0	IC-Ib	Ib	0
00	00	11	00	11	11	01	01	00	0	0	0	0	0	0	Ia	IC-Ia	0
11	00	11	11	00	00	01	01	00	0	0	0	0	0	0	IC-Ib	Ib	0
00	11	11	11	00	00	01	01	00	0	0	0	0	0	0	Ia-IB	-IA-Ia	0
11	00	11	00	11	00	01	01	00	0	0	0	0	0	0	-IA-Ib	Ib-IB	0
00	11	11	00	11	00	01	01	00	0	0	0	0	0	0	Ia	IC-Ia	0
11	00	11	00	00	11	01	01	00	0	0	0	0	0	0	IC-Ib	Ib	0
00	11	11	00	00	11	01	01	00	0	0	0	0	0	0	Ia	IC-Ia	0
11	00	00	11	11	00	01	00	01	0	0	0	0	0	0	IC-Ic	0	Ic
11	00	00	00	11	11	01	00	01	0	0	0	0	0	0	Ia-IA	0	-IB-Ia
00	11	00	11	11	00	01	00	01	0	0	0	0	0	0	IC-Ic	0	Ic
00	11	00	11	00	11	00	01	01	0	0	0	0	0	0	Ib-IA	0	-IB-Ib
00	11	00	00	11	11	01	00	01	0	0	0	0	0	0	Ia	0	IC-Ia
00	00	11	11	11	00	01	00	01	0	0	0	0	0	0	-IB-Ic	0	Ic-IA
00	00	11	00	11	11	01	00	01	0	0	0	0	0	0	Ia	0	IC-Ia
11	11	00	11	00	00	01	00	01	0	0	0	0	0	0	IC-Ic	0	Ic
00	11	11	11	00	00	01	00	01	0	0	0	0	0	0	Ia-IB	0	-IA-Ia
11	11	00	00	11	00	01	00	01	0	0	0	0	0	0	IC-Ic	0	Ic
00	11	11	00	11	00	01	00	01	0	0	0	0	0	0	Ia	0	IC-Ia
11	11	00	00	00	11	01	00	01	0	0	0	0	0	0	-IA-Ic	0	Ic-IB
00	11	11	00	00	11	01	00	01	0	0	0	0	0	0	Ia	0	IC-Ia
11	00	00	11	11	00	00	01	01	0	0	0	0	0	0	0	IC-Ic	Ic
11	00	00	11	00	11	00	01	01	0	0	0	0	0	0	0	Ib	IC-Ib
00	11	00	11	11	00	00	01	01	0	0	0	0	0	0	0	IC-Ic	Ic
00	00	11	11	11	00	00	01	01	0	0	0	0	0	0	0	-IB-Ic	Ic-IA
00	00	11	11	00	11	00	01	01	0	0	0	0	0	0	0	Ib	IC-Ib
11	11	00	11	00	00	00	01	01	0	0	0	0	0	0	0	IC-Ic	Ic
11	00	11	11	00	00	00	01	01	0	0	0	0	0	0	0	Ib	IC-Ib
11	11	00	00	11	00	00	01	01	0	0	0	0	0	0	0	IC-Ic	Ic
11	00	11	00	11	00	00	01	01	0	0	0	0	0	0	0	Ib-IB	-IA-Ib
11	11	00	00	00	11	00	01	01	0	0	0	0	0	0	0	-IA-Ic	Ic-IB
11	00	11	00	00	11	00	01	01	0	0	0	0	0	0	0	Ib	IC-Ib
employ three capacitors																	
10	10	00	10	00	00	11	00	11	Ib-IA	-Ib	0	-IB	0	0	0	0	0
10	10	00	10	00	00	00	11	11	IB-Ia	IC+Ia	0	-IB	0	0	0	0	0
10	10	00	00	10	00	11	00	11	IC+Ib	IB-Ib	0	0	-IB	0	0	0	0

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
10	10	00	00	10	00	00	11	11	-Ia	Ia-IA	0	0	-IB	0	0	0	0
10	10	00	00	00	10	11	00	11	Ib-IA	-Ib	0	0	0	-IB	0	0	0
10	10	00	00	00	10	00	11	11	-Ia	Ia-IA	0	0	0	-IB	0	0	0
10	00	10	10	00	00	11	11	00	Ic-IA	0	-Ic	-IB	0	0	0	0	0
10	00	10	10	00	00	00	11	11	IB-Ia	0	IC+Ia	-IB	0	0	0	0	0
10	00	10	00	10	00	11	11	00	Ic-IA	0	-Ic	0	-IB	0	0	0	0
10	00	10	00	10	00	00	11	11	-Ia	0	Ia-IA	0	-IB	0	0	0	0
10	00	10	00	00	10	11	11	00	IC+Ic	0	IB-Ic	0	0	-IB	0	0	0
10	00	10	00	00	10	00	11	11	-Ia	0	Ia-IA	0	0	-IB	0	0	0
10	00	00	10	10	00	11	00	11	-IA	0	0	Ib-IB	-Ib	0	0	0	0
10	00	00	10	10	00	00	11	11	-IA	0	0	IA-Ia	IC+Ia	0	0	0	0
10	00	00	10	00	10	11	11	00	-IA	0	0	Ic-IB	0	-Ic	0	0	0
10	00	00	10	00	10	00	11	11	-IA	0	0	IA-Ia	0	IC+Ia	0	0	0
10	00	00	00	10	10	11	11	00	-IA	0	0	0	Ic-IB	-Ic	0	0	0
10	00	00	00	10	10	11	00	11	-IA	0	0	0	-Ib	Ib-IB	0	0	0
00	10	10	10	00	00	11	11	00	0	Ic-IA	-Ic	-IB	0	0	0	0	0
00	10	10	10	00	00	11	00	11	0	-Ib	Ib-IA	-IB	0	0	0	0	0
00	10	10	00	10	00	11	11	00	0	Ic-IA	-Ic	0	-IB	0	0	0	0
00	10	10	00	10	00	11	00	11	0	IB-Ib	IC+Ib	0	-IB	0	0	0	0
00	10	10	00	00	10	11	11	00	0	IC+Ic	IB-Ic	0	0	-IB	0	0	0
00	10	10	00	00	10	11	00	11	0	-Ib	Ib-IA	0	0	-IB	0	0	0
00	10	00	10	10	00	11	00	11	0	-IA	0	IC+Ib	IA-Ib	0	0	0	0
00	10	00	10	10	00	00	11	11	0	-IA	0	-Ia	Ia-IB	0	0	0	0
00	10	00	10	00	10	11	11	00	0	-IA	0	Ic-IB	0	-Ic	0	0	0
00	10	00	10	00	10	00	11	11	0	-IA	0	-Ia	0	Ia-IB	0	0	0
00	10	00	00	10	10	11	11	00	0	-IA	0	0	Ic-IB	-Ic	0	0	0
00	10	00	00	10	10	11	00	11	0	-IA	0	0	IA-Ib	IC+Ib	0	0	0
00	00	10	10	10	00	11	00	11	0	0	-IA	Ib-IB	-Ib	0	0	0	0
00	00	10	10	10	00	00	11	11	0	0	-IA	-Ia	Ia-IB	0	0	0	0
00	00	10	10	00	10	11	11	00	0	0	-IA	IC+Ic	0	IA-Ic	0	0	0
00	00	10	10	00	10	00	11	11	0	0	-IA	-Ia	0	Ia-IB	0	0	0
00	00	10	00	10	10	11	11	00	0	0	-IA	0	IC+Ic	IA-Ic	0	0	0
00	00	10	00	10	10	11	00	11	0	0	-IA	0	-Ib	Ib-IB	0	0	0
11	00	00	11	00	00	01	01	01	0	0	0	0	0	0	IC+Ia	Ib	Ic
11	00	00	00	11	00	01	01	01	0	0	0	0	0	0	Ia-IA	Ib-IB	Ic
11	00	00	00	00	11	01	01	01	0	0	0	0	0	0	Ia-IA	Ib	Ic-IB
00	11	00	11	00	00	01	01	01	0	0	0	0	0	0	Ia-IB	Ib-IA	Ic
00	11	00	00	11	00	01	01	01	0	0	0	0	0	0	Ia	IC+Ib	Ic
00	11	00	00	00	11	01	01	01	0	0	0	0	0	0	Ia	Ib-IA	Ic-IB
00	00	11	11	00	00	01	01	01	0	0	0	0	0	0	Ia-IB	Ib	Ic-IA
00	00	11	00	11	00	01	01	01	0	0	0	0	0	0	Ia	Ib-IB	Ic-IA
00	00	11	00	00	11	01	01	01	0	0	0	0	0	0	Ia	Ib	IC+Ic
employ four capacitors																	
10	10	10	10	00	00	11	00	00	-IA-Ia	-Ib	-Ic	-IB	0	0	0	0	0
10	10	10	10	00	00	00	11	00	IB-Ia	IC-Ib	-Ic	-IB	0	0	0	0	0

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
10	10	10	10	00	00	00	00	11	IB-Ia	-Ib	IC-Ic	-IB	0	0	0	0	0
10	10	10	00	10	00	11	00	00	IC-Ia	IB-Ib	-Ic	0	-IB	0	0	0	0
10	10	10	00	10	00	00	11	00	-Ia	-IA-Ib	-Ic	0	-IB	0	0	0	0
10	10	10	00	10	00	00	00	11	-Ia	IB-Ib	IC-Ic	0	-IB	0	0	0	0
10	10	10	00	00	10	11	00	00	IC-Ia	-Ib	IB-Ic	0	0	-IB	0	0	0
10	10	10	00	00	10	00	11	00	-Ia	IC-Ib	IB-Ic	0	0	-IB	0	0	0
10	10	10	00	00	10	00	00	11	-Ia	-Ib	-IA-Ic	0	0	-IB	0	0	0
10	10	00	10	00	10	11	00	00	Ib-IA	-Ib	0	Ic-IB	0	-Ic	0	0	0
10	10	00	10	00	10	00	11	00	IB+Ib	IC-Ib	0	Ic-IB	0	-Ic	0	0	0
10	10	00	10	00	10	00	00	11	Ib-IA	-Ib	0	IA+Ic	0	IC-Ic	0	0	0
10	10	00	00	10	10	11	00	00	IC-Ia	IB+Ia	0	0	Ic-IB	-Ic	0	0	0
10	10	00	00	10	10	00	11	00	-Ia	Ia-IA	0	0	Ic-IB	-Ic	0	0	0
10	10	00	00	10	10	00	00	11	-Ia	Ia-IA	0	0	IA+Ic	IC-Ic	0	0	0
10	00	10	10	10	00	11	00	00	Ic-IA	0	-Ic	Ib-IB	-Ib	0	0	0	0
10	00	10	10	10	00	00	11	00	Ic-IA	0	-Ic	IA+Ib	IC-Ib	0	0	0	0
10	00	10	10	10	00	00	00	11	IB+Ic	0	IC-Ic	Ib-IB	-Ib	0	0	0	0
10	00	10	00	10	10	11	00	00	IC-Ia	0	IB+Ia	0	-Ib	Ib-IB	0	0	0
10	00	10	00	10	10	00	11	00	-Ia	0	Ia-IA	0	IC-Ib	IA+Ib	0	0	0
10	00	10	00	10	10	00	00	11	-Ia	0	Ia-IA	0	-Ib	Ib-IB	0	0	0
10	00	00	10	10	10	11	00	00	-IA	0	0	-IB-Ia	-Ib	-Ic	0	0	0
10	00	00	10	10	10	00	11	00	-IA	0	0	IA-Ia	IC-Ib	-Ic	0	0	0
10	00	00	10	10	10	00	00	11	-IA	0	0	IA-Ia	-Ib	IC-Ic	0	0	0
00	10	10	10	10	00	11	00	00	0	Ic-IA	-Ic	IC-Ia	IA+Ia	0	0	0	0
00	10	10	10	10	00	00	11	00	0	Ic-IA	-Ic	-Ia	Ia-IB	0	0	0	0
00	10	10	10	10	00	00	00	11	0	IB+Ic	IC-Ic	-Ia	Ia-IB	0	0	0	0
00	10	10	10	00	10	11	00	00	0	-Ib	Ib-IA	IC-Ia	0	IA+Ia	0	0	0
00	10	10	10	00	10	00	11	00	0	IC-Ib	IB+Ib	-Ia	0	Ia-IB	0	0	0
00	10	10	10	00	10	00	00	11	0	-Ib	Ib-IA	-Ia	0	Ia-IB	0	0	0
00	10	00	10	10	10	11	00	00	0	-IA	0	IC-Ia	IA-Ib	-Ic	0	0	0
00	10	00	10	10	10	00	11	00	0	-IA	0	-Ia	-IB-Ib	-Ic	0	0	0
00	10	00	10	10	10	00	00	11	0	-IA	0	-Ia	IA-Ib	IC-Ic	0	0	0
00	00	10	10	10	10	11	00	00	0	0	-IA	IC-Ia	-Ib	IA-Ic	0	0	0
00	00	10	10	10	10	00	11	00	0	0	-IA	-Ia	IC-Ib	IA-Ic	0	0	0
00	00	10	10	10	10	00	00	11	0	0	-IA	-Ia	-Ib	-IB-Ic	0	0	0

Table B.36: Switching device combinations for (V_{AB},V_{BC},V_{CA}) = (0,$-V_{cap}$,$+V_{cap}$) and (V_{ab},V_{bc},V_{ca}) = ($+V_{cap}$,0,$-V_{cap}$).

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
employ single capacitor																	
10	11	11	00	11	00	11	00	00	IC-Ia	0	0	0	0	0	0	0	0
10	11	11	00	00	11	11	00	00	IC-Ia	0	0	0	0	0	0	0	0
10	11	00	00	11	11	11	00	00	IC-Ia	0	0	0	0	0	0	0	0
10	00	11	00	11	11	11	00	00	IC-Ia	0	0	0	0	0	0	0	0
00	11	00	10	11	11	11	00	00	0	0	0	IC-Ia	0	0	0	0	0
00	00	11	10	11	11	11	00	00	0	0	0	IC-Ia	0	0	0	0	0
00	11	11	10	11	00	11	00	00	0	0	0	IC-Ia	0	0	0	0	0
00	11	11	10	00	11	11	00	00	0	0	0	IC-Ia	0	0	0	0	0
00	11	00	00	11	11	11	01	00	0	0	0	0	0	0	0	IC-Ia	0
00	00	11	00	11	11	11	01	00	0	0	0	0	0	0	0	IC-Ia	0
00	11	11	00	11	00	11	01	00	0	0	0	0	0	0	0	IC-Ia	0
00	11	11	00	00	11	11	01	00	0	0	0	0	0	0	0	IC-Ia	0
00	11	00	00	11	11	11	00	01	0	0	0	0	0	0	0	0	IC-Ia
00	00	11	00	11	11	11	00	01	0	0	0	0	0	0	0	0	IC-Ia
00	11	11	00	11	00	11	00	01	0	0	0	0	0	0	0	0	IC-Ia
00	11	11	00	00	11	11	00	01	0	0	0	0	0	0	0	0	IC-Ia
employ two capacitors																	
10	11	11	10	00	00	11	00	00	-IA-Ia	0	0	-IB	0	0	0	0	0
10	00	00	10	11	11	11	00	00	-IA	0	0	-IB-Ia	0	0	0	0	0
10	11	00	10	00	11	11	00	00	Ib-IA	0	0	Ic-IB	0	0	0	0	0
10	00	11	10	11	00	11	00	00	Ic-IA	0	0	Ib-IB	0	0	0	0	0
10	00	00	00	11	11	11	01	00	-IA	0	0	0	0	0	0	-IB-Ia	0
10	11	11	00	11	00	00	01	00	-Ia	0	0	0	0	0	0	IC	0
10	11	11	00	00	11	00	01	00	-Ia	0	0	0	0	0	0	IC	0
10	00	11	00	11	00	11	01	00	Ic-IA	0	0	0	0	0	0	Ib-IB	0
10	00	11	00	00	11	11	01	00	IC+Ic	0	0	0	0	0	0	Ib	0
10	11	00	00	11	11	00	01	00	-Ia	0	0	0	0	0	0	IC	0
10	00	11	00	11	11	00	01	00	-Ia	0	0	0	0	0	0	IC	0
10	00	00	00	11	11	11	00	01	-IA	0	0	0	0	0	0	0	-IB-Ia
10	11	11	00	11	00	00	00	01	-Ia	0	0	0	0	0	0	0	IC
10	11	11	00	00	11	00	00	01	-Ia	0	0	0	0	0	0	0	IC
10	11	00	00	11	00	11	00	01	IC+Ib	0	0	0	0	0	0	0	Ic
10	11	00	00	00	11	11	00	01	Ib-IA	0	0	0	0	0	0	0	Ic-IB
10	11	00	00	11	11	00	00	01	-Ia	0	0	0	0	0	0	0	IC
10	00	11	00	11	11	00	00	01	-Ia	0	0	0	0	0	0	0	IC
00	11	00	10	00	11	11	01	00	0	0	0	Ic-IB	0	0	0	Ib-IA	0
00	00	11	10	00	11	11	01	00	0	0	0	IC+Ic	0	0	0	Ib	0
00	11	11	10	00	00	11	01	00	0	0	0	-IB	0	0	0	-IA-Ia	0
00	11	00	10	11	11	00	01	00	0	0	0	-Ia	0	0	0	IC	0
00	00	11	10	11	11	00	01	00	0	0	0	-Ia	0	0	0	IC	0
00	11	11	10	11	00	00	01	00	0	0	0	-Ia	0	0	0	IC	0

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
00	11	11	10	00	11	00	01	00	0	0	0	-Ia	0	0	0	IC	0
00	11	00	10	11	00	11	00	01	0	0	0	IC+Ib	0	0	0	0	Ic
00	00	11	10	11	00	11	00	01	0	0	0	Ib-IB	0	0	0	0	Ic-IA
00	11	11	10	00	00	11	00	01	0	0	0	-IB	0	0	0	0	-IA-Ia
00	11	00	10	11	11	00	00	01	0	0	0	-Ia	0	0	0	0	IC
00	00	11	10	11	11	00	00	01	0	0	0	-Ia	0	0	0	0	IC
00	11	11	10	11	00	00	00	01	0	0	0	-Ia	0	0	0	0	IC
00	11	11	10	00	11	00	00	01	0	0	0	-Ia	0	0	0	0	IC
00	11	00	00	11	00	11	01	01	0	0	0	0	0	0	0	IC+Ib	Ic
00	11	00	00	00	11	11	01	01	0	0	0	0	0	0	0	Ib-IA	Ic-IB
00	00	11	00	11	00	11	01	01	0	0	0	0	0	0	0	Ib-IB	Ic-IA
00	00	11	00	00	11	11	01	01	0	0	0	0	0	0	0	Ib	IC+Ic
employ three capacitors																	
10	00	00	10	00	11	11	01	00	-IA	0	0	Ic-IB	0	0	0	Ib	0
10	11	11	10	00	00	00	01	00	IB-Ia	0	0	-IB	0	0	0	IC	0
10	00	11	10	00	00	11	01	00	Ic-IA	0	0	-IB	0	0	0	Ib	0
10	00	00	10	11	11	00	01	00	-IA	0	0	IA-Ia	0	0	0	IC	0
10	11	00	10	00	11	00	01	00	IB+Ib	0	0	Ic-IB	0	0	0	IC	0
10	00	11	10	11	00	00	01	00	Ic-IA	0	0	IA+Ib	0	0	0	IC	0
10	00	00	10	11	00	11	00	01	-IA	0	0	Ib-IB	0	0	0	0	Ic
10	11	11	10	00	00	00	00	01	IB-Ia	0	0	-IB	0	0	0	0	IC
10	11	00	10	00	00	11	00	01	Ib-IA	0	0	-IB	0	0	0	0	Ic
10	00	00	10	11	11	00	00	01	-IA	0	0	IA-Ia	0	0	0	0	IC
10	11	00	10	00	11	00	00	01	Ib-IA	0	0	IA+Ic	0	0	0	0	IC
10	00	11	10	11	00	00	00	01	IB+Ic	0	0	Ib-IB	0	0	0	0	IC
10	00	00	00	11	00	11	01	01	-IA	0	0	0	0	0	0	Ib-IB	Ic
10	00	00	00	00	11	11	01	01	-IA	0	0	0	0	0	0	Ib	Ic-IB
10	11	00	00	11	00	00	01	01	-Ia	0	0	0	0	0	0	IC-Ic	Ic
10	00	11	00	11	00	00	01	01	-Ia	0	0	0	0	0	0	Ib-IB	-IA-Ib
10	11	00	00	00	11	00	01	01	-Ia	0	0	0	0	0	0	-IA-Ic	Ic-IB
10	00	11	00	00	11	00	01	01	-Ia	0	0	0	0	0	0	Ib	IC-Ib
00	11	00	10	00	00	11	01	01	0	0	0	-IB	0	0	0	Ib-IA	Ic
00	00	11	10	00	00	11	01	01	0	0	0	-IB	0	0	0	Ib	Ic-IA
00	11	00	10	11	00	00	01	01	0	0	0	-Ia	0	0	0	IC-Ic	Ic
00	11	00	10	00	11	00	01	01	0	0	0	-Ia	0	0	0	Ib-IA	-IB-Ib
00	00	11	10	11	00	00	01	01	0	0	0	-Ia	0	0	0	-IB-Ic	Ic-IA
00	00	11	10	00	11	00	01	01	0	0	0	-Ia	0	0	0	Ib	IC-Ib
employ four capacitors																	
10	00	00	10	00	00	11	01	01	-IA	0	0	-IB	0	0	0	Ib	Ic
10	00	00	10	11	00	00	01	01	-IA	0	0	IA-Ia	0	0	0	IC-Ic	Ic
10	00	00	10	00	11	00	01	01	-IA	0	0	IA-Ia	0	0	0	Ib	IC-Ib
10	11	00	10	00	00	00	01	01	IB-Ia	0	0	-IB	0	0	0	IC-Ic	Ic
10	00	11	10	00	00	00	01	01	IB-Ia	0	0	-IB	0	0	0	Ib	IC-Ib

Table B.37: Switching device combinations for (V_{AB},V_{BC},V_{CA}) = (0,$-V_{cap}$,$+V_{cap}$) and (V_{ab},V_{bc},V_{ca}) = (0,$+V_{cap}$,$-V_{cap}$).

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
employ single capacitor																	
10	00	11	00	00	11	11	11	00	IC+Ic	0	0	0	0	0	0	0	0
00	10	11	00	00	11	11	11	00	0	IC+Ic	0	0	0	0	0	0	0
00	00	11	10	00	11	11	11	00	0	0	0	IC+Ic	0	0	0	0	0
00	00	11	00	10	11	11	11	00	0	0	0	0	IC+Ic	0	0	0	0
00	00	11	00	00	11	11	11	01	0	0	0	0	0	0	0	0	IC+Ic
employ two capacitors																	
10	10	11	00	00	11	11	00	00	IC-Ia	-Ib	0	0	0	0	0	0	0
10	10	11	00	00	11	00	11	00	-Ia	IC-Ib	0	0	0	0	0	0	0
10	00	00	10	00	11	11	11	00	-IA	0	0	Ic-IB	0	0	0	0	0
10	00	11	10	00	00	11	11	00	Ic-IA	0	0	-IB	0	0	0	0	0
10	00	00	00	10	11	11	11	00	-IA	0	0	0	Ic-IB	0	0	0	0
10	00	11	00	10	00	11	11	00	Ic-IA	0	0	0	-IB	0	0	0	0
10	00	11	00	10	11	11	00	00	IC-Ia	0	0	0	-Ib	0	0	0	0
10	00	11	00	10	11	00	11	00	-Ia	0	0	0	IC-Ib	0	0	0	0
10	00	00	00	00	11	11	11	01	-IA	0	0	0	0	0	0	0	Ic-IB
10	00	11	00	00	11	00	11	01	-Ia	0	0	0	0	0	0	0	IC-Ib
00	10	00	10	00	11	11	11	00	0	-IA	0	Ic-IB	0	0	0	0	0
00	10	11	10	00	00	11	11	00	0	Ic-IA	0	-IB	0	0	0	0	0
00	10	11	10	00	11	11	00	00	0	-Ib	0	IC-Ia	0	0	0	0	0
00	10	11	10	00	11	00	11	00	0	IC-Ib	0	-Ia	0	0	0	0	0
00	10	00	00	10	11	11	11	00	0	-IA	0	0	Ic-IB	0	0	0	0
00	10	11	00	10	00	11	11	00	0	Ic-IA	0	0	-IB	0	0	0	0
00	10	00	00	00	11	11	11	01	0	-IA	0	0	0	0	0	0	Ic-IB
00	10	11	00	00	11	11	00	01	0	-Ib	0	0	0	0	0	0	IC-Ia
00	00	11	10	10	11	11	00	00	0	0	0	IC-Ia	-Ib	0	0	0	0
00	00	11	10	10	11	00	11	00	0	0	0	-Ia	IC-Ib	0	0	0	0
00	00	11	10	00	00	11	11	01	0	0	0	-IB	0	0	0	0	Ic-IA
00	00	11	10	00	11	00	11	01	0	0	0	-Ia	0	0	0	0	IC-Ib
00	00	11	00	10	00	11	11	01	0	0	0	0	-IB	0	0	0	Ic-IA
00	00	11	00	10	11	11	00	01	0	0	0	0	-Ib	0	0	0	IC-Ia
employ three capacitors																	
10	10	11	10	00	00	11	00	00	-IA-Ia	-IB	0	-Ib	0	0	0	0	0
10	10	11	10	00	00	00	11	00	IB-Ia	IC-Ib	0	-IB	0	0	0	0	0
10	10	00	10	00	11	11	00	00	Ib-IA	-Ib	0	Ic-IB	0	0	0	0	0
10	10	00	10	00	11	00	11	00	IB+Ib	IC-Ib	0	Ic-IB	0	0	0	0	0
10	10	11	00	10	00	11	00	00	IC-Ia	IB-Ib	0	0	-IB	0	0	0	0
10	10	11	00	10	00	00	11	00	-Ia	-IA-Ib	0	0	-IB	0	0	0	0
10	10	00	00	10	11	11	00	00	IC-Ia	IB+Ia	0	0	Ic-IB	0	0	0	0
10	10	00	00	10	11	00	11	00	-Ia	Ia-IA	0	0	Ic-IB	0	0	0	0
10	10	11	00	00	11	00	00	01	-Ia	-Ib	0	0	0	0	0	0	IC
10	10	00	00	00	11	11	00	01	Ib-IA	-Ib	0	0	0	0	0	0	Ic-IB

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
10	10	00	00	00	11	00	11	01	-Ia	Ia-IA	0	0	0	0	0	0	Ic-IB
10	00	00	10	00	00	11	11	01	-IA	0	0	-IB	0	0	0	0	Ic
10	00	00	10	00	11	00	11	01	-IA	0	0	IA-Ia	0	0	0	0	IC-Ib
10	00	11	10	00	00	00	11	01	IB-Ia	0	0	-IB	0	0	0	0	IC-Ib
10	00	00	10	10	11	11	00	00	-IA	0	0	-IB-Ia	-Ib	0	0	0	0
10	00	00	10	10	11	00	11	00	-IA	0	0	IA-Ia	IC-Ib	0	0	0	0
10	00	11	10	10	00	11	00	00	Ic-IA	0	0	Ib-IB	-Ib	0	0	0	0
10	00	11	10	10	00	00	11	00	Ic-IA	0	0	IA+Ib	IC-Ib	0	0	0	0
10	00	00	00	10	00	11	11	01	-IA	0	0	0	-IB	0	0	0	Ic
10	00	00	00	10	11	11	00	01	-IA	0	0	0	-Ib	0	0	0	-IB-Ia
10	00	11	00	10	00	00	11	01	-Ia	0	0	0	-IB	0	0	0	-IA-Ib
10	00	11	00	10	11	00	00	01	-Ia	0	0	0	-Ib	0	0	0	IC
00	10	00	10	10	11	11	00	00	0	-IA	0	IC-Ia	IA-Ib	0	0	0	0
00	10	00	10	10	11	00	11	00	0	-IA	0	-Ia	-IB-Ib	0	0	0	0
00	10	11	10	10	00	11	00	00	0	Ic-IA	0	IC-Ia	IA+Ia	0	0	0	0
00	10	11	10	10	00	00	11	00	0	Ic-IA	0	-Ia	Ia-IB	0	0	0	0
00	10	00	10	00	00	11	11	01	0	-IA	0	-IB	0	0	0	0	Ic
00	10	00	10	00	11	00	11	01	0	-IA	0	-Ia	0	0	0	0	-IB-Ib
00	10	11	10	00	00	11	00	01	0	-Ib	0	-IB	0	0	0	0	-IA-Ia
00	10	11	10	00	11	00	00	01	0	-Ib	0	-Ia	0	0	0	0	IC
00	10	00	00	10	00	11	11	01	0	-IA	0	0	-IB	0	0	0	Ic
00	10	00	00	10	11	11	00	01	0	-IA	0	0	IA-Ib	0	0	0	IC-Ia
00	10	11	00	10	00	11	00	01	0	IB-Ib	0	0	-IB	0	0	0	IC-Ia
00	00	11	10	10	00	11	00	01	0	0	0	Ib-IB	-Ib	0	0	0	Ic-IA
00	00	11	10	10	00	00	11	01	0	0	0	-Ia	Ia-IB	0	0	0	Ic-IA
00	00	11	10	10	11	00	00	01	0	0	0	-Ia	-Ib	0	0	0	IC
employ four capacitors																	
10	10	11	10	00	00	00	00	01	IB-Ia	-Ib	0	-IB	0	0	0	0	IC
10	10	00	10	00	00	11	00	01	Ib-IA	-Ib	0	-IB	0	0	0	0	Ic
10	10	00	10	00	00	00	11	01	IB-Ia	IC+Ia	0	-IB	0	0	0	0	Ic
10	10	00	10	00	11	00	00	01	Ib-IA	-Ib	0	IA+Ic	0	0	0	0	IC
10	10	11	00	10	00	00	00	01	-Ia	IB-Ib	0	0	-IB	0	0	0	IC
10	10	00	00	10	00	11	00	01	IC+Ib	IB-Ib	0	0	-IB	0	0	0	Ic
10	10	00	00	10	00	00	11	01	-Ia	Ia-IA	0	0	-IB	0	0	0	Ic
10	10	00	00	10	11	00	00	01	-Ia	Ia-IA	0	0	IA+Ic	0	0	0	IC
10	00	00	10	10	00	11	00	01	-IA	0	0	Ib-IB	-Ib	0	0	0	Ic
10	00	00	10	10	00	00	11	01	-IA	0	0	IA-Ia	IC+Ia	0	0	0	Ic
10	00	00	10	10	11	00	00	01	-IA	0	0	IA-Ia	-Ib	0	0	0	IC
10	00	11	10	10	00	00	00	01	IB+Ic	0	0	Ib-IB	-Ib	0	0	0	IC
00	10	00	10	10	00	11	00	01	0	-IA	0	IC+Ib	IA-Ib	0	0	0	Ic
00	10	00	10	10	00	00	11	01	0	-IA	0	-Ia	Ia-IB	0	0	0	Ic
00	10	00	10	10	11	00	00	01	0	-IA	0	-Ia	IA-Ib	0	0	0	IC
00	10	11	10	10	00	00	00	01	0	IB+Ic	0	-Ia	Ia-IB	0	0	0	IC

Table B.38: Switching device combinations for (V_{AB},V_{BC},V_{CA}) = (0,$-V_{cap}$,$+V_{cap}$) and (V_{ab},V_{bc},V_{ca}) = ($-V_{cap}$,$+V_{cap}$,0).

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
employ single capacitor																	
11	10	11	11	00	00	00	11	00	0	IC-Ib	0	0	0	0	0	0	0
11	10	11	00	00	11	00	11	00	0	IC-Ib	0	0	0	0	0	0	0
11	10	00	11	00	11	00	11	00	0	IC-Ib	0	0	0	0	0	0	0
00	10	11	11	00	11	00	11	00	0	IC-Ib	0	0	0	0	0	0	0
11	00	00	11	10	11	00	11	00	0	0	0	0	IC-Ib	0	0	0	0
00	00	11	11	10	11	00	11	00	0	0	0	0	IC-Ib	0	0	0	0
11	00	11	11	10	00	00	11	00	0	0	0	0	IC-Ib	0	0	0	0
11	00	11	00	10	11	00	11	00	0	0	0	0	IC-Ib	0	0	0	0
11	00	00	11	00	11	01	11	00	0	0	0	0	0	0	IC-Ib	0	0
00	00	11	11	00	11	01	11	00	0	0	0	0	0	0	IC-Ib	0	0
11	00	11	11	00	00	01	11	00	0	0	0	0	0	0	IC-Ib	0	0
11	00	11	00	00	11	01	11	00	0	0	0	0	0	0	IC-Ib	0	0
11	00	00	11	00	11	00	11	01	0	0	0	0	0	0	0	0	IC-Ib
00	00	11	11	00	11	00	11	01	0	0	0	0	0	0	0	0	IC-Ib
11	00	11	11	00	00	00	11	01	0	0	0	0	0	0	0	0	IC-Ib
11	00	11	00	00	11	00	11	01	0	0	0	0	0	0	0	0	IC-Ib
employ two capacitors																	
11	10	11	00	10	00	00	11	00	0	-IA-Ib	0	0	-IB	0	0	0	0
00	10	00	11	10	11	00	11	00	0	-IA	0	0	-IB-Ib	0	0	0	0
11	10	00	00	10	11	00	11	00	0	Ia-IA	0	0	Ic-IB	0	0	0	0
00	10	11	11	10	00	00	11	00	0	Ic-IA	0	0	Ia-IB	0	0	0	0
00	10	00	11	00	11	01	11	00	0	-IA	0	0	0	0	-IB-Ib	0	0
11	10	11	11	00	00	01	00	00	0	-Ib	0	0	0	0	IC	0	0
11	10	11	00	00	11	01	00	00	0	-Ib	0	0	0	0	IC	0	0
00	10	11	11	00	00	01	11	00	0	Ic-IA	0	0	0	0	Ia-IB	0	0
00	10	11	00	00	11	01	11	00	0	IC+Ic	0	0	0	0	Ia	0	0
11	10	00	11	00	11	01	00	00	0	-Ib	0	0	0	0	IC	0	0
00	10	11	11	00	11	01	00	00	0	-Ib	0	0	0	0	IC	0	0
00	10	00	11	00	11	00	11	01	0	-IA	0	0	0	0	0	0	-IB-Ib
11	10	11	11	00	00	00	00	01	0	-Ib	0	0	0	0	0	0	IC
11	10	11	00	00	11	00	00	01	0	-Ib	0	0	0	0	0	0	IC
11	10	00	11	00	00	00	11	01	0	IC+Ia	0	0	0	0	0	0	Ic
11	10	00	00	00	11	00	11	01	0	Ia-IA	0	0	0	0	0	0	Ic-IB
11	10	00	11	00	11	00	00	01	0	-Ib	0	0	0	0	0	0	IC
00	10	11	11	00	11	00	00	01	0	-Ib	0	0	0	0	0	0	IC
11	00	00	00	10	11	01	11	00	0	0	0	0	Ia-IA	0	Ic-IB	0	0
00	00	11	00	10	11	01	11	00	0	0	0	0	IC+Ic	0	Ia	0	0
11	00	11	00	10	00	01	11	00	0	0	0	0	-IB	0	-IA-Ib	0	0
11	00	00	11	10	11	01	00	00	0	0	0	0	-Ib	0	IC	0	0
00	00	11	11	10	11	01	00	00	0	0	0	0	-Ib	0	IC	0	0
11	00	11	11	10	00	01	00	00	0	0	0	0	-Ib	0	IC	0	0

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
11	00	11	00	10	11	01	00	00	0	0	0	0	-Ib	0	IC	0	0
11	00	00	11	10	00	00	11	01	0	0	0	0	IC+Ia	0	0	0	Ic
00	00	11	11	10	00	00	11	01	0	0	0	0	Ia-IB	0	0	0	Ic-IA
11	00	11	00	10	00	00	11	01	0	0	0	0	-IB	0	0	0	-IA-Ib
11	00	00	11	10	11	00	00	01	0	0	0	0	-Ib	0	0	0	IC
00	00	11	11	10	11	00	00	01	0	0	0	0	-Ib	0	0	0	IC
11	00	11	11	10	00	00	00	01	0	0	0	0	-Ib	0	0	0	IC
11	00	11	00	10	11	00	00	01	0	0	0	0	-Ib	0	0	0	IC
11	00	00	11	00	00	01	11	01	0	0	0	0	0	0	IC+Ia	0	Ic
11	00	00	00	00	11	01	11	01	0	0	0	0	0	0	Ia-IA	0	Ic-IB
00	00	11	11	00	00	01	11	01	0	0	0	0	0	0	Ia-IB	0	Ic-IA
00	00	11	00	00	11	01	11	01	0	0	0	0	0	0	Ia	0	IC+Ic
employ three capacitors																	
00	10	00	00	10	11	01	11	00	0	-IA	0	0	Ic-IB	0	Ia	0	0
11	10	11	00	10	00	01	00	00	0	IB-Ib	0	0	-IB	0	IC	0	0
00	10	11	00	10	00	01	11	00	0	Ic-IA	0	0	-IB	0	Ia	0	0
00	10	00	11	10	11	01	00	00	0	-IA	0	0	IA-Ib	0	IC	0	0
11	10	00	00	10	11	01	00	00	0	IB+Ia	0	0	Ic-IB	0	IC	0	0
00	10	11	11	10	00	01	00	00	0	Ic-IA	0	0	IA+Ia	0	IC	0	0
00	10	00	11	10	00	00	11	01	0	-IA	0	0	Ia-IB	0	0	0	Ic
11	10	11	00	10	00	00	00	01	0	IB-Ib	0	0	-IB	0	0	0	IC
11	10	00	00	10	00	00	11	01	0	Ia-IA	0	0	-IB	0	0	0	Ic
00	10	00	11	10	11	00	00	01	0	-IA	0	0	IA-Ib	0	0	0	IC
11	10	00	00	10	11	00	00	01	0	Ia-IA	0	0	IA+Ic	0	0	0	IC
00	10	11	11	10	00	00	00	01	0	IB+Ic	0	0	Ia-IB	0	0	0	IC
00	10	00	11	00	00	01	11	01	0	-IA	0	0	0	0	Ia-IB	0	Ic
00	10	00	00	00	11	01	11	01	0	-IA	0	0	0	0	Ia	0	Ic-IB
11	10	00	11	00	00	01	00	01	0	-Ib	0	0	0	0	IC-Ic	0	Ic
00	10	11	11	00	00	01	00	01	0	-Ib	0	0	0	0	Ia-IB	0	-IA-Ia
11	10	00	00	00	11	01	00	01	0	-Ib	0	0	0	0	-IA-Ic	0	Ic-IB
00	10	11	00	00	11	01	00	01	0	-Ib	0	0	0	0	Ia	0	IC-Ia
11	00	00	00	10	00	01	11	01	0	0	0	0	-IB	0	Ia-IA	0	Ic
00	00	11	00	10	00	01	11	01	0	0	0	0	-IB	0	Ia	0	Ic-IA
11	00	00	11	10	00	01	00	01	0	0	0	0	-Ib	0	IC-Ic	0	Ic
11	00	00	00	10	11	01	00	01	0	0	0	0	-Ib	0	Ia-IA	0	-IB-Ia
00	00	11	11	10	00	01	00	01	0	0	0	0	-Ib	0	-IB-Ic	0	Ic-IA
00	00	11	00	10	11	01	00	01	0	0	0	0	-Ib	0	Ia	0	IC-Ia
employ four capacitors																	
00	10	00	00	10	00	01	11	01	0	-IA	0	0	-IB	0	Ia	0	Ic
00	10	00	11	10	00	01	00	01	0	-IA	0	0	IA-Ib	0	IC-Ic	0	Ic
00	10	00	00	10	11	01	00	01	0	-IA	0	0	IA-Ib	0	Ia	0	IC-Ia
11	10	00	00	10	00	01	00	01	0	IB-Ib	0	0	-IB	0	IC-Ic	0	Ic
00	10	11	00	10	00	01	00	01	0	IB-Ib	0	0	-IB	0	Ia	0	IC-Ia

Table B.39: Switching device combinations for (V_{AB},V_{BC},V_{CA}) = (0,$-V_{cap}$,$+V_{cap}$) and (V_{ab},V_{bc},V_{ca}) = ($-V_{cap}$,0,$+V_{cap}$).

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
employ single capacitor																	
11	10	00	11	00	00	00	11	11	0	IC+Ia	0	0	0	0	0	0	0
11	00	10	11	00	00	00	11	11	0	0	IC+Ia	0	0	0	0	0	0
11	00	00	11	10	00	00	11	11	0	0	0	0	IC+Ia	0	0	0	0
11	00	00	11	00	10	00	11	11	0	0	0	0	0	IC+Ia	0	0	0
11	00	00	11	00	00	01	11	11	0	0	0	0	0	0	IC+Ia	0	0
employ two capacitors																	
11	10	10	11	00	00	00	11	00	0	IC-Ib	-Ic	0	0	0	0	0	0
11	10	10	11	00	00	00	00	11	0	-Ib	IC-Ic	0	0	0	0	0	0
00	10	00	11	10	00	00	11	11	0	-IA	0	0	Ia-IB	0	0	0	0
11	10	00	00	10	00	00	11	11	0	Ia-IA	0	0	-IB	0	0	0	0
00	10	00	11	00	10	00	11	11	0	-IA	0	0	0	Ia-IB	0	0	0
11	10	00	00	00	10	00	11	11	0	Ia-IA	0	0	0	-IB	0	0	0
11	10	00	11	00	10	00	11	00	0	IC-Ib	0	0	0	-Ic	0	0	0
11	10	00	11	00	10	00	00	11	0	-Ib	0	0	0	IC-Ic	0	0	0
00	10	00	11	00	00	01	11	11	0	-IA	0	0	0	0	Ia-IB	0	0
11	10	00	11	00	00	01	00	11	0	-Ib	0	0	0	0	IC-Ic	0	0
00	00	10	11	10	00	00	11	11	0	0	-IA	0	Ia-IB	0	0	0	0
11	00	10	00	10	00	00	11	11	0	0	Ia-IA	0	-IB	0	0	0	0
11	00	10	11	10	00	00	11	00	0	0	-Ic	0	IC-Ib	0	0	0	0
11	00	10	11	10	00	00	00	11	0	0	IC-Ic	0	-Ib	0	0	0	0
00	00	10	11	00	10	00	11	11	0	0	-IA	0	0	Ia-IB	0	0	0
11	00	10	00	00	10	00	11	11	0	0	Ia-IA	0	0	-IB	0	0	0
00	00	10	11	00	00	01	11	11	0	0	-IA	0	0	0	Ia-IB	0	0
11	00	10	11	00	00	01	11	00	0	0	-Ic	0	0	0	IC-Ib	0	0
11	00	00	11	10	10	00	11	00	0	0	0	0	IC-Ib	-Ic	0	0	0
11	00	00	11	10	10	00	00	11	0	0	0	0	-Ib	IC-Ic	0	0	0
11	00	00	00	10	00	01	11	11	0	0	0	0	-IB	0	Ia-IA	0	0
11	00	00	11	10	00	01	00	11	0	0	0	0	-Ib	0	IC-Ic	0	0
11	00	00	00	00	10	01	11	11	0	0	0	0	0	-IB	Ia-IA	0	0
11	00	00	11	00	10	01	11	00	0	0	0	0	0	-Ic	IC-Ib	0	0
employ three capacitors																	
11	10	10	00	10	00	00	11	00	0	-IA-Ib	-Ic	0	-IB	0	0	0	0
11	10	10	00	10	00	00	00	11	0	IB-Ib	IC-Ic	0	-IB	0	0	0	0
00	10	10	11	10	00	00	11	00	0	Ic-IA	-Ic	0	Ia-IB	0	0	0	0
00	10	10	11	10	00	00	00	11	0	IB+Ic	IC-Ic	0	Ia-IB	0	0	0	0
11	10	10	00	00	10	00	11	00	0	IC-Ib	IB-Ic	0	0	-IB	0	0	0
11	10	10	00	00	10	00	00	11	0	-Ib	-IA-Ic	0	0	-IB	0	0	0
00	10	10	11	00	10	00	11	00	0	IC-Ib	IB+Ib	0	0	Ia-IB	0	0	0
00	10	10	11	00	10	00	00	11	0	-Ib	Ib-IA	0	0	Ia-IB	0	0	0
11	10	10	11	00	00	01	00	00	0	-Ib	-Ic	0	0	0	IC	0	0
00	10	10	11	00	00	01	11	00	0	Ic-IA	-Ic	0	0	0	Ia-IB	0	0

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
00	10	10	11	00	00	01	00	11	0	-Ib	Ib-IA	0	0	0	Ia-IB	0	0
00	10	00	11	10	10	00	11	00	0	-IA	0	0	-IB-Ib	-Ic	0	0	0
00	10	00	11	10	10	00	00	11	0	-IA	0	0	IA-Ib	IC-Ic	0	0	0
11	10	00	00	10	10	00	11	00	0	Ia-IA	0	0	Ic-IB	-Ic	0	0	0
11	10	00	00	10	10	00	00	11	0	Ia-IA	0	0	IA+Ic	IC-Ic	0	0	0
00	10	00	00	10	00	01	11	11	0	-IA	0	0	-IB	0	Ia	0	0
00	10	00	11	10	00	01	00	11	0	-IA	0	0	IA-Ib	0	IC-Ic	0	0
11	10	00	00	10	00	01	00	11	0	IB-Ib	0	0	-IB	0	IC-Ic	0	0
00	10	00	00	00	10	10	11	11	0	-IA	0	0	0	-IB	Ia	0	0
00	10	00	11	00	10	10	11	00	0	-IA	0	0	0	-Ic	-IB-Ib	0	0
11	10	00	00	00	10	01	00	11	0	-Ib	0	0	0	-IB	-IA-Ic	0	0
11	10	00	11	00	10	01	00	00	0	-Ib	0	0	0	-Ic	IC	0	0
00	00	10	11	10	10	00	11	00	0	0	-IA	0	IC-Ib	IA-Ic	0	0	0
00	00	10	11	10	10	00	00	11	0	0	-IA	0	-Ib	-IB-Ic	0	0	0
11	00	10	00	10	10	00	11	00	0	0	Ia-IA	0	IC-Ib	IA+Ib	0	0	0
11	00	10	00	10	10	00	00	11	0	0	Ia-IA	0	-Ib	Ib-IB	0	0	0
00	00	10	00	10	00	01	11	11	0	0	-IA	0	-IB	0	Ia	0	0
00	00	10	11	10	00	01	00	11	0	0	-IA	0	-Ib	0	-IB-Ic	0	0
11	00	10	00	10	00	01	11	00	0	0	-Ic	0	-IB	0	-IA-Ib	0	0
11	00	10	11	10	00	01	00	00	0	0	-Ic	0	-Ib	0	IC	0	0
00	00	10	00	00	10	01	11	11	0	0	-IA	0	0	-IB	Ia	0	0
00	00	10	11	00	10	01	11	00	0	0	-IA	0	0	IA-Ic	IC-Ib	0	0
11	00	10	00	00	10	01	11	00	0	0	IB-Ic	0	0	-IB	IC-Ib	0	0
11	00	00	00	10	10	01	11	00	0	0	0	0	Ic-IB	-Ic	Ia-IA	0	0
11	00	00	00	10	10	01	00	11	0	0	0	0	-Ib	Ib-IB	Ia-IA	0	0
11	00	00	11	10	10	01	00	00	0	0	0	0	-Ib	-Ic	IC	0	0
employ four capacitors																	
11	10	10	00	10	00	01	00	00	0	IB-Ib	-Ic	0	-IB	0	IC	0	0
00	10	10	00	10	00	01	11	00	0	Ic-IA	-Ic	0	-IB	0	Ia	0	0
00	10	10	00	10	00	01	00	11	0	IB-Ib	IC+Ib	0	-IB	0	Ia	0	0
00	10	10	11	10	00	01	00	00	0	Ic-IA	-Ic	0	IA+Ia	0	IC	0	0
11	10	10	00	00	10	01	00	00	0	-Ib	IB-Ic	0	0	-IB	IC	0	0
00	10	10	00	00	10	01	11	00	0	IC+Ic	IB-Ic	0	0	-IB	Ia	0	0
00	10	10	00	00	10	01	00	11	0	-Ib	Ib-IA	0	0	-IB	Ia	0	0
00	10	10	11	00	10	01	00	00	0	-Ib	Ib-IA	0	0	IA+Ia	IC	0	0
00	10	00	00	10	10	01	11	00	0	-IA	0	0	Ic-IB	-Ic	Ia	0	0
00	10	00	00	10	10	01	00	11	0	-IA	0	0	IA-Ib	IC+Ib	Ia	0	0
11	10	00	00	10	10	01	00	00	0	IB+Ia	0	0	Ic-IB	-Ic	IC	0	0
00	10	00	11	10	10	01	00	00	0	-IA	0	0	IA-Ib	-Ic	IC	0	0
00	00	10	00	10	10	01	11	00	0	0	-IA	0	IA-Ic	IC+Ic	Ia	0	0
00	00	10	00	10	10	01	00	11	0	0	-IA	0	-Ib	Ib-IB	Ia	0	0
00	00	10	11	10	10	01	00	00	0	0	-IA	0	-Ib	IA-Ic	IC	0	0
11	00	10	00	10	10	01	00	00	0	0	IB+Ia	0	-Ib	Ib-IB	IC	0	0

Table B.40: Switching device combinations for (V_{AB},V_{BC},V_{CA}) = (0,$-V_{cap}$,$+V_{cap}$) and (V_{ab},V_{bc},V_{ca}) = (0,$-V_{cap}$,$+V_{cap}$).

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
employ single capacitor																	
11	11	10	11	00	00	00	00	11	0	0	IC-Ic	0	0	0	0	0	0
11	11	10	00	11	00	00	00	11	0	0	IC-Ic	0	0	0	0	0	0
11	00	10	11	11	00	00	00	11	0	0	IC-Ic	0	0	0	0	0	0
00	11	10	11	11	00	00	00	11	0	0	IC-Ic	0	0	0	0	0	0
11	00	00	11	11	10	00	00	11	0	0	0	0	0	IC-Ic	0	0	0
00	11	00	11	11	10	00	00	11	0	0	0	0	0	IC-Ic	0	0	0
11	11	00	11	00	10	00	00	11	0	0	0	0	0	IC-Ic	0	0	0
11	11	00	00	11	10	00	00	11	0	0	0	0	0	IC-Ic	0	0	0
11	00	00	11	11	00	01	00	11	0	0	0	0	0	0	IC-Ic	0	0
00	11	00	11	11	00	01	00	11	0	0	0	0	0	0	IC-Ic	0	0
11	11	00	11	00	00	01	00	11	0	0	0	0	0	0	IC-Ic	0	0
11	11	00	00	11	00	01	00	11	0	0	0	0	0	0	IC-Ic	0	0
11	00	00	11	11	00	00	01	11	0	0	0	0	0	0	0	IC-Ic	0
00	11	00	11	11	00	00	01	11	0	0	0	0	0	0	0	IC-Ic	0
11	11	00	11	00	00	00	01	11	0	0	0	0	0	0	0	IC-Ic	0
11	11	00	00	11	00	00	01	11	0	0	0	0	0	0	0	IC-Ic	0
employ two capacitors																	
11	11	10	00	00	10	00	00	11	0	0	-IA-Ic	0	0	-IB	0	0	0
00	00	10	11	11	10	00	00	11	0	0	-IA	0	0	-IB-Ic	0	0	0
11	00	10	00	11	10	00	00	11	0	0	Ia-IA	0	0	Ib-IB	0	0	0
00	11	10	11	00	10	00	00	11	0	0	Ib-IA	0	0	Ia-IB	0	0	0
00	00	10	11	11	00	01	00	11	0	0	-IA	0	0	0	-IB-Ic	0	0
11	11	10	11	00	00	01	00	00	0	0	-Ic	0	0	0	IC	0	0
11	11	10	00	11	00	01	00	00	0	0	-Ic	0	0	0	IC	0	0
00	11	10	11	00	00	01	00	11	0	0	Ib-IA	0	0	0	Ia-IB	0	0
00	11	10	00	11	00	01	00	11	0	0	IC+Ib	0	0	0	Ia	0	0
11	00	10	11	11	00	01	00	00	0	0	-Ic	0	0	0	IC	0	0
00	11	10	11	11	00	01	00	00	0	0	-Ic	0	0	0	IC	0	0
00	00	10	11	11	00	00	01	11	0	0	-IA	0	0	0	0	-IB-Ic	0
11	11	10	11	00	00	00	01	00	0	0	-Ic	0	0	0	0	IC	0
11	11	10	00	11	00	00	01	00	0	0	-Ic	0	0	0	0	IC	0
11	00	10	11	00	00	00	01	11	0	0	IC+Ia	0	0	0	0	Ib	0
11	00	10	00	11	00	00	01	11	0	0	Ia-IA	0	0	0	0	Ib-IB	0
11	00	10	11	11	00	00	01	00	0	0	-Ic	0	0	0	0	IC	0
00	11	10	11	11	00	00	01	00	0	0	-Ic	0	0	0	0	IC	0
11	00	00	00	11	10	01	00	11	0	0	0	0	0	Ib-IB	Ia-IA	0	0
00	11	00	00	11	10	01	00	11	0	0	0	0	0	IC+Ib	Ia	0	0
11	11	00	00	00	10	01	00	11	0	0	0	0	0	-IB	-IA-Ic	0	0
11	00	00	11	11	10	01	00	00	0	0	0	0	0	-Ic	IC	0	0
00	11	00	11	11	10	01	00	00	0	0	0	0	0	-Ic	IC	0	0
11	11	00	11	00	10	01	00	00	0	0	0	0	0	-Ic	IC	0	0

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
11	11	00	00	11	10	01	00	00	0	0	0	0	0	-Ic	IC	0	0
11	00	00	11	00	10	00	01	11	0	0	0	0	0	IC+Ia	0	Ib	0
00	11	00	11	00	10	00	01	11	0	0	0	0	0	Ia-IB	0	Ib-IA	0
11	11	00	00	00	10	00	01	11	0	0	0	0	0	-IB	0	-IA-Ic	0
11	00	00	11	11	10	00	01	00	0	0	0	0	0	-Ic	0	IC	0
00	11	00	11	11	10	00	01	00	0	0	0	0	0	-Ic	0	IC	0
11	11	00	11	00	10	00	01	00	0	0	0	0	0	-Ic	0	IC	0
11	11	00	00	11	10	00	01	00	0	0	0	0	0	-Ic	0	IC	0
11	00	00	11	00	00	01	01	11	0	0	0	0	0	0	IC+Ia	Ib	0
11	00	00	00	11	00	01	01	11	0	0	0	0	0	0	Ia-IA	Ib-IB	0
00	11	00	11	00	00	01	01	11	0	0	0	0	0	0	Ia-IB	Ib-IA	0
00	11	00	00	11	00	01	01	11	0	0	0	0	0	0	Ia	IC+Ib	0
employ three capacitors																	
00	00	10	00	11	10	01	00	11	0	0	-IA	0	0	Ib-IB	Ia	0	0
11	11	10	00	00	10	01	00	00	0	0	IB-Ic	0	0	-IB	IC	0	0
00	11	10	00	00	10	01	00	11	0	0	Ib-IA	0	0	-IB	Ia	0	0
00	00	10	11	11	10	01	00	00	0	0	-IA	0	0	IA-Ic	IC	0	0
11	00	10	00	11	10	01	00	00	0	0	IB+Ia	0	0	Ib-IB	IC	0	0
00	11	10	11	00	10	01	00	00	0	0	Ib-IA	0	0	IA+Ia	IC	0	0
00	00	10	11	00	10	00	01	11	0	0	-IA	0	0	Ia-IB	0	Ib	0
11	11	10	00	00	10	00	01	00	0	0	IB-Ic	0	0	-IB	0	IC	0
11	00	10	00	00	10	00	01	11	0	0	Ia-IA	0	0	-IB	0	Ib	0
00	00	10	11	11	10	00	01	00	0	0	-IA	0	0	IA-Ic	0	IC	0
11	00	10	00	11	10	00	01	00	0	0	Ia-IA	0	0	IA+Ib	0	IC	0
00	11	10	11	00	10	00	01	00	0	0	IB+Ib	0	0	Ia-IB	0	IC	0
00	00	10	11	00	00	01	01	11	0	0	-IA	0	0	0	Ia-IB	Ib	0
00	00	10	00	11	00	01	01	11	0	0	-IA	0	0	0	Ia	Ib-IB	0
11	00	10	11	00	00	01	01	00	0	0	-Ic	0	0	0	IC-Ib	Ib	0
00	11	10	11	00	00	01	01	00	0	0	-Ic	0	0	0	Ia-IB	-IA-Ia	0
11	00	10	00	11	00	01	01	00	0	0	-Ic	0	0	0	-IA-Ib	Ib-IB	0
00	11	10	00	11	00	01	01	00	0	0	-Ic	0	0	0	Ia	IC-Ia	0
11	00	00	00	00	10	01	01	11	0	0	0	0	0	-IB	Ia-IA	Ib	0
00	11	00	00	00	10	01	01	11	0	0	0	0	0	-IB	Ia	Ib-IA	0
11	00	00	11	00	10	01	01	00	0	0	0	0	0	-Ic	IC-Ib	Ib	0
11	00	00	00	11	10	01	01	00	0	0	0	0	0	-Ic	Ia-IA	-IB-Ia	0
00	11	00	11	00	10	01	01	00	0	0	0	0	0	-Ic	-IB-Ib	Ib-IA	0
00	11	00	00	11	10	01	01	00	0	0	0	0	0	-Ic	Ia	IC-Ia	0
employ four capacitors																	
00	00	10	00	00	10	01	01	11	0	0	-IA	0	0	-IB	Ia	Ib	0
00	00	10	11	00	10	01	01	00	0	0	-IA	0	0	IA-Ic	IC-Ib	Ib	0
00	00	10	00	11	10	01	01	00	0	0	-IA	0	0	IA-Ic	Ia	IC-Ia	0
11	00	10	00	00	10	01	01	00	0	0	IB-Ic	0	0	-IB	IC-Ib	Ib	0
00	11	10	00	00	10	01	01	00	0	0	IB-Ic	0	0	-IB	Ia	IC-Ia	0

Table B.41: Switching device combinations for (V_{AB},V_{BC},V_{CA}) = (0,$-V_{cap}$,$+V_{cap}$) and (V_{ab},V_{bc},V_{ca}) = ($+V_{cap}$,$-V_{cap}$,0).

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
employ single capacitor																	
10	11	00	00	11	00	11	00	11	IC+Ib	0	0	0	0	0	0	0	0
00	11	10	00	11	00	11	00	11	0	0	IC+Ib	0	0	0	0	0	0
00	11	00	10	11	00	11	00	11	0	0	0	IC+Ib	0	0	0	0	0
00	11	00	00	11	10	11	00	11	0	0	0	0	0	IC+Ib	0	0	0
00	11	00	00	11	00	11	01	11	0	0	0	0	0	0	0	IC+Ib	0
employ two capacitors																	
10	11	10	00	11	00	11	00	00	IC-Ia	0	-Ic	0	0	0	0	0	0
10	11	10	00	11	00	00	00	11	-Ia	0	IC-Ic	0	0	0	0	0	0
10	00	00	10	11	00	11	00	11	-IA	0	0	Ib-IB	0	0	0	0	0
10	11	00	10	00	00	11	00	11	Ib-IA	0	0	-IB	0	0	0	0	0
10	00	00	00	11	10	11	00	11	-IA	0	0	0	0	Ib-IB	0	0	0
10	11	00	00	00	10	11	00	11	Ib-IA	0	0	0	0	-IB	0	0	0
10	11	00	00	11	10	11	00	00	IC-Ia	0	0	0	0	-Ic	0	0	0
10	11	00	00	11	10	00	00	11	-Ia	0	0	0	0	IC-Ic	0	0	0
10	00	00	00	11	00	11	01	11	-IA	0	0	0	0	0	0	Ib-IB	0
10	11	00	00	11	00	00	01	11	-Ia	0	0	0	0	0	0	IC-Ic	0
00	00	10	10	11	00	11	00	11	0	0	-IA	Ib-IB	0	0	0	0	0
00	11	10	10	00	00	11	00	11	0	0	Ib-IA	-IB	0	0	0	0	0
00	11	10	10	11	00	11	00	00	0	0	-Ic	IC-Ia	0	0	0	0	0
00	11	10	10	11	00	00	00	11	0	0	IC-Ic	-Ia	0	0	0	0	0
00	00	10	00	11	10	11	00	11	0	0	-IA	0	0	Ib-IB	0	0	0
00	11	10	00	00	10	11	00	11	0	0	Ib-IA	0	0	-IB	0	0	0
00	00	10	00	11	00	11	01	11	0	0	-IA	0	0	0	0	Ib-IB	0
00	11	10	00	11	00	11	01	00	0	0	-Ic	0	0	0	0	IC-Ia	0
00	11	00	10	11	10	11	00	00	0	0	0	IC-Ia	0	-Ic	0	0	0
00	11	00	10	11	10	00	00	11	0	0	0	-Ia	0	IC-Ic	0	0	0
00	11	00	10	00	00	11	01	11	0	0	0	-IB	0	0	0	Ib-IA	0
00	11	00	10	11	00	00	01	11	0	0	0	-Ia	0	0	0	IC-Ic	0
00	11	00	00	00	10	11	01	11	0	0	0	0	0	-IB	0	Ib-IA	0
00	11	00	00	11	10	11	01	00	0	0	0	0	0	-Ic	0	IC-Ia	0
employ three capacitors																	
10	11	10	10	00	00	11	00	00	-IA-Ia	0	-Ic	-IB	0	0	0	0	0
10	11	10	10	00	00	00	00	11	IB-Ia	0	IC-Ic	-IB	0	0	0	0	0
10	00	10	10	11	00	11	00	00	Ic-IA	0	-Ic	Ib-IB	0	0	0	0	0
10	00	10	10	11	00	00	00	11	IB+Ic	0	IC-Ic	Ib-IB	0	0	0	0	0
10	11	10	00	00	10	11	00	00	IC-Ia	0	IB-Ic	0	0	-IB	0	0	0
10	11	10	00	00	10	00	00	11	-Ia	0	-IA-Ic	0	0	-IB	0	0	0
10	00	10	00	11	10	11	00	00	IC-Ia	0	IB+Ia	0	0	Ib-IB	0	0	0
10	00	10	00	11	10	00	00	11	-Ia	0	Ia-IA	0	0	Ib-IB	0	0	0
10	11	10	00	11	00	00	01	00	-Ia	0	-Ic	0	0	0	0	IC	0
10	00	10	00	11	00	11	01	00	Ic-IA	0	-Ic	0	0	0	0	Ib-IB	0

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
10	00	10	00	11	00	00	01	11	-Ia	0	Ia-IA	0	0	0	0	Ib-IB	0
10	00	00	10	11	10	11	00	00	-IA	0	0	-IB-Ia	0	-Ic	0	0	0
10	00	00	10	11	10	00	00	11	-IA	0	0	IA-Ia	0	IC-Ic	0	0	0
10	11	00	10	00	10	11	00	00	Ib-IA	0	0	Ic-IB	0	-Ic	0	0	0
10	11	00	10	00	10	00	00	11	Ib-IA	0	0	IA+Ic	0	IC-Ic	0	0	0
10	00	00	10	00	00	11	01	11	-IA	0	0	-IB	0	0	0	Ib	0
10	00	00	10	11	00	00	01	11	-IA	0	0	IA-Ia	0	0	0	IC-Ic	0
10	11	00	10	00	00	00	01	11	IB-Ia	0	0	-IB	0	0	0	IC-Ic	0
10	00	00	00	00	10	11	01	11	-IA	0	0	0	0	-IB	0	Ib	0
10	00	00	00	11	10	11	01	00	-IA	0	0	0	0	-Ic	0	-IB-Ia	0
10	11	00	00	00	10	00	10	11	-Ia	0	0	0	0	-IB	0	-IA-Ic	0
10	11	00	00	11	10	00	01	00	-Ia	0	0	0	0	-Ic	0	IC	0
00	00	10	10	11	10	11	00	00	0	0	-IA	IC-Ia	0	IA-Ic	0	0	0
00	00	10	10	11	10	00	00	11	0	0	-IA	-Ia	0	-IB-Ic	0	0	0
00	11	10	10	00	10	11	00	00	0	0	Ib-IA	IC-Ia	0	IA+Ia	0	0	0
00	11	10	10	00	10	00	00	11	0	0	Ib-IA	-Ia	0	Ia-IB	0	0	0
00	00	10	10	00	00	11	01	11	0	0	-IA	-IB	0	0	0	Ib	0
00	00	10	10	11	00	00	01	11	0	0	-IA	-Ia	0	0	0	-IB-Ic	0
00	11	10	10	00	00	11	01	00	0	0	-Ic	-IB	0	0	0	-IA-Ia	0
00	11	10	10	11	00	00	01	00	0	0	-Ic	-Ia	0	0	0	IC	0
00	00	10	00	00	10	11	01	11	0	0	-IA	0	0	-IB	0	Ib	0
00	00	10	00	11	10	11	01	00	0	0	-IA	0	0	IA-Ic	0	IC-Ia	0
00	11	10	00	00	10	11	01	00	0	0	IB-Ic	0	0	-IB	0	IC-Ia	0
00	11	00	10	00	10	11	01	00	0	0	0	Ic-IB	0	-Ic	0	Ib-IA	0
00	11	00	10	00	10	00	01	11	0	0	0	-Ia	0	Ia-IB	0	Ib-IA	0
00	11	00	10	11	10	00	01	00	0	0	0	-Ia	0	-Ic	0	IC	0
employ four capacitors																	
10	11	10	10	00	00	00	01	00	IB-Ia	0	-Ic	-IB	0	0	0	IC	0
10	00	10	10	00	00	11	01	00	Ic-IA	0	-Ic	-IB	0	0	0	Ib	0
10	00	10	10	00	00	00	01	11	IB-Ia	0	IC+Ia	-IB	0	0	0	Ib	0
10	00	10	10	11	00	00	01	00	Ic-IA	0	-Ic	IA+Ib	0	0	0	IC	0
10	11	10	00	00	10	00	01	00	-Ia	0	IB-Ic	0	0	-IB	0	IC	0
10	00	10	00	00	10	11	01	00	IC+Ic	0	IB-Ic	0	0	-IB	0	Ib	0
10	00	10	00	00	10	00	01	11	-Ia	0	Ia-IA	0	0	-IB	0	Ib	0
10	00	10	00	11	10	00	01	00	-Ia	0	Ia-IA	0	0	IA+Ib	0	IC	0
10	00	00	10	00	10	11	01	00	-IA	0	0	Ic-IB	0	-Ic	0	Ib	0
10	00	00	10	00	10	00	01	11	-IA	0	0	IA-Ia	0	IC+Ia	0	Ib	0
10	00	00	10	11	10	00	01	00	-IA	0	0	IA-Ia	0	-Ic	0	IC	0
10	11	00	10	00	10	00	01	00	IB+Ib	0	0	Ic-IB	0	-Ic	0	IC	0
00	00	10	10	00	10	11	01	00	0	0	-IA	IC+Ic	0	IA-Ic	0	Ib	0
00	00	10	10	00	10	00	01	11	0	0	-IA	-Ia	0	Ia-IB	0	Ib	0
00	00	10	10	11	10	00	01	00	0	0	-IA	-Ia	0	IA-Ic	0	IC	0
00	11	10	10	00	10	00	10	00	0	0	IB+Ib	-Ia	0	Ia-IB	0	IC	0

Table B.42: Switching device combinations for (V_{AB},V_{BC},V_{CA}) = ($+V_{cap}$,$-V_{cap}$,0) and (V_{ab},V_{bc},V_{ca}) = (0,0,0).

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
employ single capacitor																	
11	00	00	10	00	00	11	11	11	0	0	0	-IB	0	0	0	0	0
00	11	00	10	00	00	11	11	11	0	0	0	-IB	0	0	0	0	0
00	00	11	10	00	00	11	11	11	0	0	0	-IB	0	0	0	0	0
11	11	11	10	00	00	11	00	00	0	0	0	-IB	0	0	0	0	0
11	11	11	10	00	00	00	11	00	0	0	0	-IB	0	0	0	0	0
11	11	11	10	00	00	00	00	11	0	0	0	-IB	0	0	0	0	0
11	00	11	10	00	00	11	11	00	0	0	0	-IB	0	0	0	0	0
00	11	11	10	00	00	11	11	00	0	0	0	-IB	0	0	0	0	0
11	11	00	10	00	00	11	00	11	0	0	0	-IB	0	0	0	0	0
00	11	11	10	00	00	11	00	11	0	0	0	-IB	0	0	0	0	0
11	11	00	10	00	00	00	11	11	0	0	0	-IB	0	0	0	0	0
11	00	11	10	00	00	00	11	11	0	0	0	-IB	0	0	0	0	0
11	00	00	00	10	00	11	11	11	0	0	0	0	-IB	0	0	0	0
00	11	00	00	10	00	11	11	11	0	0	0	0	-IB	0	0	0	0
00	00	11	00	10	00	11	11	11	0	0	0	0	-IB	0	0	0	0
11	11	11	00	10	00	11	00	00	0	0	0	0	-IB	0	0	0	0
11	11	11	00	10	00	00	11	00	0	0	0	0	-IB	0	0	0	0
11	11	11	00	10	00	00	00	11	0	0	0	0	-IB	0	0	0	0
11	00	11	00	10	00	11	11	00	0	0	0	0	-IB	0	0	0	0
00	11	11	00	10	00	11	11	00	0	0	0	0	-IB	0	0	0	0
11	11	00	00	10	00	11	00	11	0	0	0	0	-IB	0	0	0	0
00	11	11	00	10	00	11	00	11	0	0	0	0	-IB	0	0	0	0
11	11	00	00	10	00	00	11	11	0	0	0	0	-IB	0	0	0	0
11	00	11	00	10	00	00	11	11	0	0	0	0	-IB	0	0	0	0
11	00	00	00	00	10	11	11	11	0	0	0	0	0	-IB	0	0	0
00	11	00	00	00	10	11	11	11	0	0	0	0	0	-IB	0	0	0
00	00	11	00	00	10	11	11	11	0	0	0	0	0	-IB	0	0	0
11	11	11	00	00	10	11	00	00	0	0	0	0	0	-IB	0	0	0
11	11	11	00	00	10	00	11	00	0	0	0	0	0	-IB	0	0	0
11	11	11	00	00	10	00	00	11	0	0	0	0	0	-IB	0	0	0
11	00	11	00	00	10	11	11	00	0	0	0	0	0	-IB	0	0	0
00	11	11	00	00	10	11	11	00	0	0	0	0	0	-IB	0	0	0
11	11	00	00	00	10	11	00	11	0	0	0	0	0	-IB	0	0	0
00	11	11	00	00	10	11	00	11	0	0	0	0	0	-IB	0	0	0
11	11	00	00	00	10	00	11	11	0	0	0	0	0	-IB	0	0	0
11	00	11	00	00	10	00	11	11	0	0	0	0	0	-IB	0	0	0
employ two capacitors																	
01	00	00	11	11	11	01	00	00	IA	0	0	0	0	0	IC	0	0
01	00	00	11	11	11	00	01	00	IA	0	0	0	0	0	0	IC	0
01	00	00	11	11	11	00	00	01	IA	0	0	0	0	0	0	0	IC
00	01	00	11	11	11	01	00	00	0	IA	0	0	0	0	IC	0	0

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
00	01	00	11	11	11	00	01	00	0	IA	0	0	0	0	0	IC	0
00	01	00	11	11	11	00	00	01	0	IA	0	0	0	0	0	0	IC
00	00	01	11	11	11	01	00	00	0	0	IA	0	0	0	IC	0	0
00	00	01	11	11	11	00	01	00	0	0	IA	0	0	0	0	IC	0
00	00	01	11	11	11	00	00	01	0	0	IA	0	0	0	0	0	IC
11	00	00	10	10	00	11	00	11	0	0	0	Ib-IB	-Ib	0	0	0	0
11	00	00	10	10	00	00	11	11	0	0	0	IA-Ia	IC+Ia	0	0	0	0
00	11	00	10	10	00	11	00	11	0	0	0	IC+Ib	IA-Ib	0	0	0	0
00	11	00	10	10	00	00	11	11	0	0	0	-Ia	Ia-IB	0	0	0	0
00	00	11	10	10	00	11	00	11	0	0	0	Ib-IB	-Ib	0	0	0	0
00	00	11	10	10	00	00	11	11	0	0	0	-Ia	Ia-IB	0	0	0	0
11	00	11	10	10	00	11	00	00	0	0	0	Ib-IB	-Ib	0	0	0	0
00	11	11	10	10	00	11	00	00	0	0	0	IC-Ia	IA+Ia	0	0	0	0
11	00	11	10	10	00	00	11	00	0	0	0	IA+Ib	IC-Ib	0	0	0	0
00	11	11	10	10	00	00	11	00	0	0	0	-Ia	Ia-IB	0	0	0	0
11	00	11	10	10	00	00	00	11	0	0	0	Ib-IB	-Ib	0	0	0	0
00	11	11	10	10	00	00	00	11	0	0	0	-Ia	Ia-IB	0	0	0	0
11	00	00	10	00	10	11	11	00	0	0	0	Ic-IB	0	-Ic	0	0	0
11	00	00	10	00	10	00	11	11	0	0	0	IA-Ia	0	IC+Ia	0	0	0
00	11	00	10	00	10	11	11	00	0	0	0	Ic-IB	0	-Ic	0	0	0
00	11	00	10	00	10	00	11	11	0	0	0	-Ia	0	Ia-IB	0	0	0
00	00	11	10	00	10	11	11	00	0	0	0	IC+Ic	0	IA-Ic	0	0	0
00	00	11	10	00	10	00	11	11	0	0	0	-Ia	0	Ia-IB	0	0	0
11	11	00	10	00	10	11	00	00	0	0	0	Ic-IB	0	-Ic	0	0	0
00	11	11	10	00	10	11	00	00	0	0	0	IC-Ia	0	IA+Ia	0	0	0
11	11	00	10	00	10	00	11	00	0	0	0	Ic-IB	0	-Ic	0	0	0
00	11	11	10	00	10	00	11	00	0	0	0	-Ia	0	Ia-IB	0	0	0
11	11	00	10	00	10	00	00	11	0	0	0	IA+Ic	0	IC-Ic	0	0	0
00	11	11	10	00	10	00	00	11	0	0	0	-Ia	0	Ia-IB	0	0	0
11	00	00	00	10	10	11	11	00	0	0	0	0	Ic-IB	-Ic	0	0	0
11	00	00	00	10	10	11	00	11	0	0	0	0	-Ib	Ib-IB	0	0	0
00	11	00	00	10	10	11	11	00	0	0	0	0	Ic-IB	-Ic	0	0	0
00	11	00	00	10	10	11	00	11	0	0	0	0	IA-Ib	IC+Ib	0	0	0
00	00	11	00	10	10	11	11	00	0	0	0	0	IC+Ic	IA-Ic	0	0	0
00	00	11	00	10	10	11	00	11	0	0	0	0	-Ib	Ib-IB	0	0	0
11	11	00	00	10	10	11	00	00	0	0	0	0	Ic-IB	-Ic	0	0	0
11	00	11	00	10	10	11	00	00	0	0	0	0	-Ib	Ib-IB	0	0	0
11	11	00	00	10	10	00	11	00	0	0	0	0	Ic-IB	-Ic	0	0	0
11	00	11	00	10	10	00	11	00	0	0	0	0	IC-Ib	IA+Ib	0	0	0
11	11	00	00	10	10	00	00	11	0	0	0	0	IA+Ic	IC-Ic	0	0	0
11	00	11	00	10	10	00	00	11	0	0	0	0	-Ib	Ib-IB	0	0	0
employ three capacitors																	
01	01	00	11	00	11	01	00	00	IA-Ib	Ib	0	0	0	0	IC	0	0
01	01	00	00	11	11	01	00	00	Ia-IC	-IB-Ia	0	0	0	0	IC	0	0
01	01	00	11	00	11	00	01	00	-IB-Ib	Ib-IC	0	0	0	0	0	IC	0

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
01	01	00	00	11	11	00	01	00	Ia	IA-Ia	0	0	0	0	0	IC	0
01	01	00	11	00	11	00	00	01	IA-Ib	Ib	0	0	0	0	0	0	IC
01	01	00	00	11	11	00	00	01	Ia	IA-Ia	0	0	0	0	0	0	IC
01	00	01	11	11	00	01	00	00	IA-Ic	0	Ic	0	0	0	IC	0	0
01	00	01	00	11	11	01	00	00	Ia-IC	0	-IB-Ia	0	0	0	IC	0	0
01	00	01	11	11	00	00	01	00	IA-Ic	0	Ic	0	0	0	0	IC	0
01	00	01	00	11	11	00	01	00	Ia	0	IA-Ia	0	0	0	0	IC	0
01	00	01	11	11	00	00	00	01	-IB-Ic	0	Ic-IC	0	0	0	0	0	IC
01	00	01	00	11	11	00	00	01	Ia	0	IA-Ia	0	0	0	0	0	IC
01	00	00	11	00	11	01	01	00	IA	0	0	0	0	0	IC-Ib	Ib	0
01	00	00	00	11	11	01	01	00	IA	0	0	0	0	0	Ia-IA	-IB-Ia	0
01	00	00	11	11	00	01	00	01	IA	0	0	0	0	0	IC-Ic	0	Ic
01	00	00	00	11	11	01	00	01	IA	0	0	0	0	0	Ia-IA	0	-IB-Ia
01	00	00	11	11	00	00	01	01	IA	0	0	0	0	0	0	IC-Ic	Ic
01	00	00	11	00	11	00	01	01	IA	0	0	0	0	0	0	Ib	IC-Ib
00	01	01	11	11	00	01	00	00	0	IA-Ic	Ic	0	0	0	IC	0	0
00	01	01	11	00	11	01	00	00	0	Ib	IA-Ib	0	0	0	IC	0	0
00	01	01	11	11	00	00	01	00	0	IA-Ic	Ic	0	0	0	0	IC	0
00	01	01	11	00	11	00	01	00	0	Ib-IC	-IB-Ib	0	0	0	0	IC	0
00	01	01	11	11	00	00	00	01	0	-IB-Ic	Ic-IC	0	0	0	0	0	IC
00	01	01	11	00	11	00	00	01	0	Ib	IA-Ib	0	0	0	0	0	IC
00	01	00	11	00	11	01	01	00	0	IA	0	0	0	0	-IB-Ib	Ib-IA	0
00	01	00	00	11	11	01	01	00	0	IA	0	0	0	0	Ia	IC-Ia	0
00	01	00	11	11	00	01	00	01	0	IA	0	0	0	0	IC-Ic	0	Ic
00	01	00	00	11	11	01	00	01	0	IA	0	0	0	0	Ia	0	IC-Ia
00	01	00	11	00	11	00	01	01	0	IA	0	0	0	0	0	Ib-IA	-IB-Ib
00	01	00	11	11	00	00	01	01	0	IA	0	0	0	0	0	IC-Ic	Ic
00	00	01	11	00	11	01	01	00	0	0	IA	0	0	0	IC-Ib	Ib	0
00	00	01	00	11	11	01	01	00	0	0	IA	0	0	0	Ia	IC-Ia	0
00	00	01	11	11	00	01	00	01	0	0	IA	0	0	0	-IB-Ic	0	Ic-IA
00	00	01	00	11	11	01	00	01	0	0	IA	0	0	0	Ia	0	IC-Ia
00	00	01	11	11	00	00	01	01	0	0	IA	0	0	0	0	-IB-Ic	Ic-IA
00	00	01	11	00	11	00	01	01	0	0	IA	0	0	0	0	Ib	IC-Ib
11	00	00	10	10	10	11	00	00	0	0	0	-IB-Ia	-Ib	-Ic	0	0	0
00	11	00	10	10	10	11	00	00	0	0	0	IC-Ia	IA-Ib	-Ic	0	0	0
00	00	11	10	10	10	11	00	00	0	0	0	IC-Ia	-Ib	IA-Ic	0	0	0
11	00	00	10	10	10	00	11	00	0	0	0	IA-Ia	IC-Ib	-Ic	0	0	0
00	11	00	10	10	10	00	11	00	0	0	0	-Ia	-IB-Ib	-Ic	0	0	0
00	00	11	10	10	10	00	11	00	0	0	0	-Ia	IC-Ib	IA-Ic	0	0	0
11	00	00	10	10	10	00	00	11	0	0	0	IA-Ia	-Ib	IC-Ic	0	0	0
00	11	00	10	10	10	00	00	11	0	0	0	-Ia	IA-Ib	IC-Ic	0	0	0
00	00	11	10	10	10	00	00	11	0	0	0	-Ia	-Ib	-IB-Ic	0	0	0
employ four capacitors																	
01	01	01	11	00	00	01	00	00	IA+Ia	Ib	Ic	0	0	0	IC	0	0
01	01	01	00	11	00	01	00	00	Ia-IC	Ib-IB	Ic	0	0	0	IC	0	0

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
01	01	01	00	00	11	01	00	00	Ia-IC	Ib	Ic-IB	0	0	0	IC	0	0
01	01	01	11	00	00	00	01	00	Ia-IB	Ib-IC	Ic	0	0	0	0	IC	0
01	01	01	00	11	00	00	01	00	Ia	IA+Ib	Ic	0	0	0	0	IC	0
01	01	01	00	00	11	00	01	00	Ia	Ib-IC	Ic-IB	0	0	0	0	IC	0
01	01	01	11	00	00	00	00	01	Ia-IB	Ib	Ic-IC	0	0	0	0	0	IC
01	01	01	00	11	00	00	00	01	Ia	Ib-IB	Ic-IC	0	0	0	0	0	IC
01	01	01	00	00	11	00	00	01	Ia	Ib	IA+Ic	0	0	0	0	0	IC
01	01	00	11	00	00	01	00	01	IA-Ib	Ib	0	0	0	0	IC-Ic	0	Ic
01	01	00	00	11	00	01	00	01	-IC-Ib	Ib-IB	0	0	0	0	IC-Ic	0	Ic
01	01	00	00	00	11	01	00	01	IA-Ib	Ib	0	0	0	0	-IA-Ic	0	Ic-IB
01	01	00	11	00	00	00	01	01	Ia-IB	-IC-Ia	0	0	0	0	0	IC-Ic	Ic
01	01	00	00	11	00	00	01	01	Ia	IA-Ia	0	0	0	0	0	IC-Ic	Ic
01	01	00	00	00	11	00	01	01	Ia	IA-Ia	0	0	0	0	0	-IA-Ic	Ic-IB
01	00	01	11	00	00	01	01	00	IA-Ic	0	Ic	0	0	0	IC-Ib	Ib	0
01	00	01	00	11	00	01	01	00	IA-Ic	0	Ic	0	0	0	-IA-Ib	Ib-IB	0
01	00	01	00	00	11	01	01	00	-IC-Ic	0	Ic-IB	0	0	0	IC-Ib	Ib	0
01	00	01	11	00	00	00	01	01	Ia-IB	0	-IC-Ia	0	0	0	0	Ib	IC-Ib
01	00	01	00	11	00	00	01	01	Ia	0	IA-Ia	0	0	0	0	Ib-IB	-IA-Ib
01	00	01	00	00	11	00	01	01	Ia	0	IA-Ia	0	0	0	0	Ib	IC-Ib
01	00	00	11	00	00	01	01	01	IA	0	0	0	0	0	IC+Ia	Ib	Ic
01	00	00	00	11	00	01	01	01	IA	0	0	0	0	0	Ia-IA	Ib-IB	Ic
01	00	00	00	00	11	01	01	01	IA	0	0	0	0	0	Ia-IA	Ib	Ic-IB
00	01	01	11	00	00	01	01	00	0	IA-Ic	Ic	0	0	0	Ia-IB	-IA-Ia	0
00	01	01	00	11	00	01	01	00	0	IA-Ic	Ic	0	0	0	Ia	IC-Ia	0
00	01	01	00	00	11	01	01	00	0	-IC-Ic	Ic-IB	0	0	0	Ia	IC-Ia	0
00	01	01	11	00	00	01	00	01	0	Ib	IA-Ib	0	0	0	Ia-IB	0	-IA-Ia
00	01	01	00	11	00	01	00	01	0	Ib-IB	-IC-Ib	0	0	0	Ia	0	IC-Ia
00	01	01	00	00	11	01	00	01	0	Ib	IA-Ib	0	0	0	Ia	0	IC-Ia
00	01	00	11	00	00	01	01	01	0	IA	0	0	0	0	Ia-IB	Ib-IA	Ic
00	01	00	00	11	00	01	01	01	0	IA	0	0	0	0	Ia	IC+Ib	Ic
00	01	00	00	00	11	01	01	01	0	IA	0	0	0	0	Ia	Ib-IA	Ic-IB
00	00	01	11	00	00	01	01	01	0	0	IA	0	0	0	Ia-IB	Ib	Ic-IA
00	00	01	00	11	00	01	01	01	0	0	IA	0	0	0	Ia	Ib-IB	Ic-IA
00	00	01	00	00	11	01	01	01	0	0	IA	0	0	0	Ia	Ib	IC+Ic

Table B.43: Switching device combinations for (V_{AB},V_{BC},V_{CA}) = ($+V_{cap}$,$-V_{cap}$,0) and (V_{ab},V_{bc},V_{ca}) = ($+V_{cap}$,0,$-V_{cap}$).

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
employ single capacitor																	
11	01	00	00	11	11	11	00	00	0	-IB-Ia	0	0	0	0	0	0	0
11	00	01	00	11	11	11	00	00	0	0	-IB-Ia	0	0	0	0	0	0
11	00	00	10	11	11	11	00	00	0	0	0	-IB-Ia	0	0	0	0	0
11	00	00	00	11	11	11	01	00	0	0	0	0	0	0	0	-IB-Ia	0
11	00	00	00	11	11	11	00	01	0	0	0	0	0	0	0	0	-IB-Ia
employ two capacitors																	
11	01	01	00	11	00	11	00	00	0	Ib-IB	Ic	0	0	0	0	0	0
11	01	01	00	00	11	11	00	00	0	Ib	Ic-IB	0	0	0	0	0	0
00	01	00	10	11	11	11	00	00	0	IA	0	IC-Ia	0	0	0	0	0
11	01	00	10	00	11	11	00	00	0	Ib	0	Ic-IB	0	0	0	0	0
00	01	00	00	11	11	11	01	00	0	IA	0	0	0	0	0	IC-Ia	0
11	01	00	00	11	11	00	01	00	0	IA-Ia	0	0	0	0	0	IC	0
00	01	00	00	11	11	11	00	01	0	IA	0	0	0	0	0	0	IC-Ia
11	01	00	00	11	00	11	00	01	0	Ib-IB	0	0	0	0	0	0	Ic
11	01	00	00	00	11	11	00	01	0	Ib	0	0	0	0	0	0	Ic-IB
11	01	00	00	11	11	00	00	01	0	IA-Ia	0	0	0	0	0	0	IC
00	00	01	10	11	11	11	00	00	0	0	IA	IC-Ia	0	0	0	0	0
11	00	01	10	11	00	11	00	00	0	0	Ic	Ib-IB	0	0	0	0	0
00	00	01	00	11	11	11	01	00	0	0	IA	0	0	0	0	IC-Ia	0
11	00	01	00	11	00	11	01	00	0	0	Ic	0	0	0	0	Ib-IB	0
11	00	01	00	00	11	11	01	00	0	0	Ic-IB	0	0	0	0	Ib	0
11	00	01	00	11	11	00	01	00	0	0	IA-Ia	0	0	0	0	IC	0
00	00	01	00	11	11	11	00	01	0	0	IA	0	0	0	0	0	IC-Ia
11	00	01	00	11	11	00	00	01	0	0	IA-Ia	0	0	0	0	0	IC
11	00	00	10	00	11	11	01	00	0	0	0	Ic-IB	0	0	0	Ib	0
11	00	00	10	11	11	00	01	00	0	0	0	IA-Ia	0	0	0	IC	0
11	00	00	10	11	00	11	00	01	0	0	0	Ib-IB	0	0	0	0	Ic
11	00	00	10	11	11	00	00	01	0	0	0	IA-Ia	0	0	0	0	IC
11	00	00	00	11	00	11	01	01	0	0	0	0	0	0	0	Ib-IB	Ic
11	00	00	00	00	11	11	01	01	0	0	0	0	0	0	0	Ib	Ic-IB
employ three capacitors																	
11	01	01	10	00	00	11	00	00	0	Ib	Ic	-IB	0	0	0	0	0
00	01	01	10	11	00	11	00	00	0	IA-Ic	Ic	IC-Ia	0	0	0	0	0
00	01	01	10	00	11	11	00	00	0	Ib	IA-Ib	IC-Ia	0	0	0	0	0
11	01	01	00	11	00	00	01	00	0	IA+Ib	Ic	0	0	0	0	IC	0
11	01	01	00	00	11	00	01	00	0	Ib-IC	Ic-IB	0	0	0	0	IC	0
00	01	01	00	11	00	11	01	00	0	IA-Ic	Ic	0	0	0	0	IC-Ia	0
00	01	01	00	00	11	11	01	00	0	-IC-Ic	Ic-IB	0	0	0	0	IC-Ia	0
11	01	01	00	11	00	00	00	01	0	Ib-IB	Ic-IC	0	0	0	0	0	IC
11	01	01	00	00	11	00	00	01	0	Ib	IA+Ic	0	0	0	0	0	IC
00	01	01	00	11	00	11	00	01	0	Ib-IB	-IC-Ib	0	0	0	0	0	IC-Ia

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
00	01	01	00	00	11	11	00	01	0	Ib	IA-Ib	0	0	0	0	0	IC-Ia
00	01	00	10	00	11	11	01	00	0	IA	0	Ic-IB	0	0	0	Ib-IA	0
00	01	00	10	11	11	00	01	00	0	IA	0	-Ia	0	0	0	IC	0
11	01	00	10	00	11	00	01	00	0	Ib-IC	0	Ic-IB	0	0	0	IC	0
00	01	00	10	11	00	11	00	01	0	IA	0	IC+Ib	0	0	0	0	Ic
11	01	00	10	00	00	11	00	01	0	Ib	0	-IB	0	0	0	0	Ic
00	01	00	10	11	11	00	00	01	0	IA	0	-Ia	0	0	0	0	IC
11	01	00	10	00	11	00	00	01	0	Ib	0	IA+Ic	0	0	0	0	IC
00	01	00	00	11	00	11	01	01	0	IA	0	0	0	0	0	IC+Ib	Ic
00	01	00	00	00	11	11	01	01	0	IA	0	0	0	0	0	Ib-IA	Ic-IB
11	01	00	00	11	00	00	01	01	0	IA-Ia	0	0	0	0	0	IC-Ic	Ic
11	01	00	00	00	11	00	01	01	0	IA-Ia	0	0	0	0	0	-IA-Ic	Ic-IB
00	00	01	10	00	11	11	01	00	0	0	IA	IC+Ic	0	0	0	Ib	0
11	00	01	10	00	00	11	01	00	0	0	Ic	-IB	0	0	0	Ib	0
00	00	01	10	11	11	00	01	00	0	0	IA	-Ia	0	0	0	IC	0
11	00	01	10	11	00	00	01	00	0	0	Ic	IA+Ib	0	0	0	IC	0
00	00	01	10	11	00	11	00	01	0	0	IA	Ib-IB	0	0	0	0	Ic-IA
00	00	01	10	11	11	00	00	01	0	0	IA	-Ia	0	0	0	0	IC
11	00	01	10	11	00	00	00	01	0	0	Ic-IC	Ib-IB	0	0	0	0	IC
00	00	01	00	11	00	11	01	01	0	0	IA	0	0	0	0	Ib-IB	Ic-IA
00	00	01	00	00	11	11	01	01	0	0	IA	0	0	0	0	Ib	IC+Ic
11	00	01	00	11	00	00	01	01	0	0	IA-Ia	0	0	0	0	Ib-IB	-IA-Ib
11	00	01	00	00	11	00	01	01	0	0	IA-Ia	0	0	0	0	Ib	IC-Ib
11	00	00	10	00	00	11	01	01	0	0	0	-IB	0	0	0	Ib	Ic
11	00	00	10	11	00	00	01	01	0	0	0	IA-Ia	0	0	0	IC-Ic	Ic
11	00	00	10	00	11	00	01	01	0	0	0	IA-Ia	0	0	0	Ib	IC-Ib
employ four capacitors																	
11	01	01	10	00	00	00	01	00	0	Ib-IC	Ic	-IB	0	0	0	IC	0
00	01	01	10	00	00	11	01	00	0	IA-Ic	Ic	-IB	0	0	0	-IA-Ia	0
00	01	01	10	11	00	00	01	00	0	IA-Ic	Ic	-Ia	0	0	0	IC	0
00	01	01	10	00	11	00	01	00	0	Ib-IC	-IB-Ib	-Ia	0	0	0	IC	0
11	01	01	10	00	00	00	00	01	0	Ib	Ic-IC	-IB	0	0	0	0	IC
00	01	01	10	00	00	11	00	01	0	Ib	IA-Ib	-IB	0	0	0	0	-IA-Ia
00	01	01	10	11	00	00	00	01	0	-IB-Ic	Ic-IC	-Ia	0	0	0	0	IC
00	01	01	10	00	11	00	00	01	0	Ib	IA-Ib	-Ia	0	0	0	0	IC
00	01	00	10	00	00	11	01	01	0	IA	0	-IB	0	0	0	Ib-IA	Ic
00	01	00	10	11	00	00	01	01	0	IA	0	-Ia	0	0	0	IC-Ic	Ic
00	01	00	10	00	11	00	01	01	0	IA	0	-Ia	0	0	0	Ib-IA	-IB-Ib
11	01	00	10	00	00	00	01	01	0	-IC-Ia	0	-IB	0	0	0	IC-Ic	Ic
00	00	01	10	00	00	11	01	01	0	0	IA	-IB	0	0	0	Ib	Ic-IA
00	00	01	10	11	00	00	01	01	0	0	IA	-Ia	0	0	0	-IB-Ic	Ic-IA
00	00	01	10	00	11	00	01	01	0	0	IA	-Ia	0	0	0	Ib	IC-Ib
11	00	01	10	00	00	00	01	01	0	0	-IC-Ia	-IB	0	0	0	Ib	IC-Ib

Table B.44: Switching device combinations for (V_{AB},V_{BC},V_{CA}) = ($+V_{cap}$,$-V_{cap}$,0) and (V_{ab},V_{bc},V_{ca}) = (0,$+V_{cap}$,$-V_{cap}$).

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
employ single capacitor																	
11	11	01	00	00	11	11	00	00	0	0	Ic-IB	0	0	0	0	0	0
11	11	01	00	00	11	00	11	00	0	0	Ic-IB	0	0	0	0	0	0
11	00	01	00	00	11	11	11	00	0	0	Ic-IB	0	0	0	0	0	0
00	11	01	00	00	11	11	11	00	0	0	Ic-IB	0	0	0	0	0	0
11	00	00	10	00	11	11	11	00	0	0	0	Ic-IB	0	0	0	0	0
00	11	00	10	00	11	11	11	00	0	0	0	Ic-IB	0	0	0	0	0
11	11	00	10	00	11	11	00	00	0	0	0	Ic-IB	0	0	0	0	0
11	11	00	10	00	11	00	11	00	0	0	0	Ic-IB	0	0	0	0	0
11	00	00	00	10	11	11	11	00	0	0	0	0	Ic-IB	0	0	0	0
00	11	00	00	10	11	11	11	00	0	0	0	0	Ic-IB	0	0	0	0
11	11	00	00	10	11	11	00	00	0	0	0	0	Ic-IB	0	0	0	0
11	11	00	00	10	11	00	11	00	0	0	0	0	Ic-IB	0	0	0	0
11	00	00	00	00	11	11	11	01	0	0	0	0	0	0	0	0	Ic-IB
00	11	00	00	00	11	11	11	01	0	0	0	0	0	0	0	0	Ic-IB
11	11	00	00	00	11	11	00	01	0	0	0	0	0	0	0	0	Ic-IB
11	11	00	00	00	11	00	11	01	0	0	0	0	0	0	0	0	Ic-IB
employ two capacitors																	
11	11	01	10	00	00	11	00	00	0	0	Ic	-IB	0	0	0	0	0
11	11	01	10	00	00	00	11	00	0	0	Ic	-IB	0	0	0	0	0
11	00	01	10	00	00	11	11	00	0	0	Ic	-IB	0	0	0	0	0
00	11	01	10	00	00	11	11	00	0	0	Ic	-IB	0	0	0	0	0
00	00	01	10	00	11	11	11	00	0	0	IA	IC+Ic	0	0	0	0	0
00	11	01	10	00	11	11	00	00	0	0	IA-Ib	IC-Ia	0	0	0	0	0
00	11	01	10	00	11	00	11	00	0	0	-IB-Ib	-Ia	0	0	0	0	0
11	11	01	00	10	00	11	00	00	0	0	Ic	0	-IB	0	0	0	0
11	11	01	00	10	00	00	11	00	0	0	Ic	0	-IB	0	0	0	0
11	00	01	00	10	00	11	11	00	0	0	Ic	0	-IB	0	0	0	0
00	11	01	00	10	00	11	11	00	0	0	Ic	0	-IB	0	0	0	0
00	00	01	00	10	11	11	11	00	0	0	IA	0	IC+Ic	0	0	0	0
11	00	01	00	10	11	11	00	00	0	0	-IB-Ia	0	-Ib	0	0	0	0
11	00	01	00	10	11	00	11	00	0	0	IA-Ia	0	IC-Ib	0	0	0	0
00	00	01	00	00	11	11	11	01	0	0	IA	0	0	0	0	0	IC+Ic
11	11	01	00	00	11	00	00	01	0	0	IA+Ic	0	0	0	0	0	IC
00	11	01	00	00	11	11	00	01	0	0	IA-Ib	0	0	0	0	0	IC-Ia
11	00	01	00	00	11	00	11	01	0	0	IA-Ia	0	0	0	0	0	IC-Ib
11	00	00	10	10	11	11	00	00	0	0	0	-IB-Ia	-Ib	0	0	0	0
00	11	00	10	10	11	11	00	00	0	0	0	IC-Ia	IA-Ib	0	0	0	0
11	00	00	10	10	11	00	11	00	0	0	0	IA-Ia	IC-Ib	0	0	0	0
00	11	00	10	10	11	00	11	00	0	0	0	-Ia	-IB-Ib	0	0	0	0
11	00	00	10	00	00	11	11	01	0	0	0	-IB	0	0	0	0	Ic
00	11	00	10	00	00	11	11	01	0	0	0	-IB	0	0	0	0	Ic

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
11	11	00	10	00	00	11	00	01	0	0	0	-IB	0	0	0	0	Ic
11	11	00	10	00	00	00	11	01	0	0	0	-IB	0	0	0	0	Ic
11	00	00	10	00	11	00	11	01	0	0	0	IA-Ia	0	0	0	0	IC-Ib
00	11	00	10	00	11	00	11	01	0	0	0	-Ia	0	0	0	0	-IB-Ib
11	11	00	10	00	11	00	00	01	0	0	0	IA+Ic	0	0	0	0	IC
11	00	00	00	10	00	11	11	01	0	0	0	0	-IB	0	0	0	Ic
00	11	00	00	10	00	11	11	01	0	0	0	0	-IB	0	0	0	Ic
11	11	00	00	10	00	11	00	01	0	0	0	0	-IB	0	0	0	Ic
11	11	00	00	10	00	00	11	01	0	0	0	0	-IB	0	0	0	Ic
11	00	00	00	10	11	11	00	01	0	0	0	0	-Ib	0	0	0	-IB-Ia
00	11	00	00	10	11	11	00	01	0	0	0	0	IA-Ib	0	0	0	IC-Ia
11	11	00	00	10	11	00	00	01	0	0	0	0	IA+Ic	0	0	0	IC
employ three capacitors																	
00	00	01	10	10	11	11	00	00	0	0	IA	IC-Ia	-Ib	0	0	0	0
00	00	01	10	10	11	00	11	00	0	0	IA	-Ia	IC-Ib	0	0	0	0
11	00	01	10	10	00	11	00	00	0	0	Ic	Ib-IB	-Ib	0	0	0	0
00	11	01	10	10	00	11	00	00	0	0	Ic	IC-Ia	IA+Ia	0	0	0	0
11	00	01	10	10	00	00	11	00	0	0	Ic	IA+Ib	IC-Ib	0	0	0	0
00	11	01	10	10	00	00	11	00	0	0	Ic	-Ia	Ia-IB	0	0	0	0
00	00	01	10	00	00	11	11	01	0	0	IA	-IB	0	0	0	0	Ic-IA
00	00	01	10	00	11	00	11	01	0	0	IA	-Ia	0	0	0	0	IC-Ib
11	11	01	10	00	00	00	00	01	0	0	Ic-IC	-IB	0	0	0	0	IC
11	00	01	10	00	00	00	11	01	0	0	-IC-Ia	-IB	0	0	0	0	IC-Ib
00	11	01	10	00	00	11	00	01	0	0	IA-Ib	-IB	0	0	0	0	-IA-Ia
00	11	01	10	00	11	00	00	01	0	0	IA-Ib	-Ia	0	0	0	0	IC
00	00	01	00	10	00	11	11	01	0	0	IA	0	-IB	0	0	0	Ic-IA
00	00	01	00	10	11	11	00	01	0	0	IA	0	-Ib	0	0	0	IC-Ia
11	11	01	00	10	00	00	00	01	0	0	Ic-IC	0	-IB	0	0	0	IC
00	11	01	00	10	00	11	00	01	0	0	-IC-Ib	0	-IB	0	0	0	IC-Ia
11	00	01	00	10	00	00	11	01	0	0	IA-Ia	0	-IB	0	0	0	-IA-Ib
11	00	01	00	10	11	00	00	01	0	0	IA-Ia	0	-Ib	0	0	0	IC
11	00	00	10	10	00	11	00	01	0	0	0	Ib-IB	-Ib	0	0	0	Ic
11	00	00	10	10	00	00	11	01	0	0	0	IA-Ia	IC+Ia	0	0	0	Ic
00	11	00	10	10	00	11	00	01	0	0	0	IC+Ib	IA-Ib	0	0	0	Ic
00	11	00	10	10	00	00	11	01	0	0	0	-Ia	Ia-IB	0	0	0	Ic
11	00	00	10	10	11	00	00	01	0	0	0	IA-Ia	-Ib	0	0	0	IC
00	11	00	10	10	11	00	00	01	0	0	0	-Ia	IA-Ib	0	0	0	IC
employ four capacitors																	
00	00	01	10	10	00	11	00	01	0	0	IA	Ib-IB	-Ib	0	0	0	Ic-IA
00	00	01	10	10	00	00	11	01	0	0	IA	-Ia	Ia-IB	0	0	0	Ic-IA
00	00	01	10	10	11	00	00	01	0	0	IA	-Ia	-Ib	0	0	0	IC
11	00	01	10	10	00	00	00	01	0	0	Ic-IC	Ib-IB	-Ib	0	0	0	IC
00	11	01	10	10	00	00	00	01	0	0	Ic-IC	-Ia	Ia-IB	0	0	0	IC

Table B.45: Switching device combinations for (V_{AB},V_{BC},V_{CA}) = ($+V_{cap}$,$-V_{cap}$,0) and (V_{ab},V_{bc},V_{ca}) = ($-V_{cap}$,$+V_{cap}$,0).

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
employ single capacitor																	
01	11	00	11	00	11	00	11	00	-IB-Ib	0	0	0	0	0	0	0	0
00	11	01	11	00	11	00	11	00	0	0	-IB-Ib	0	0	0	0	0	0
00	11	00	11	10	11	00	11	00	0	0	0	0	-IB-Ib	0	0	0	0
00	11	00	11	00	11	01	11	00	0	0	0	0	0	0	-IB-Ib	0	0
00	11	00	11	00	11	00	11	01	0	0	0	0	0	0	0	0	-IB-Ib
employ two capacitors																	
01	11	01	11	00	00	00	11	00	Ia-IB	0	Ic	0	0	0	0	0	0
01	11	01	00	00	11	00	11	00	Ia	0	Ic-IB	0	0	0	0	0	0
01	00	00	11	10	11	00	11	00	IA	0	0	0	IC-Ib	0	0	0	0
01	11	00	00	10	11	00	11	00	Ia	0	0	0	Ic-IB	0	0	0	0
01	00	00	11	00	11	01	11	00	IA	0	0	0	0	0	IC-Ib	0	0
01	11	00	11	00	11	01	00	00	IA-Ib	0	0	0	0	0	IC	0	0
01	00	00	11	00	11	00	11	01	IA	0	0	0	0	0	0	0	IC-Ib
01	11	00	11	00	00	00	11	01	Ia-IB	0	0	0	0	0	0	0	Ic
01	11	00	00	00	11	00	11	01	Ia	0	0	0	0	0	0	0	Ic-IB
01	11	00	11	00	11	00	00	01	IA-Ib	0	0	0	0	0	0	0	IC
00	00	01	11	10	11	00	11	00	0	0	IA	0	IC-Ib	0	0	0	0
00	11	01	11	10	00	00	11	00	0	0	Ic	0	Ia-IB	0	0	0	0
00	00	01	11	00	11	01	11	00	0	0	IA	0	0	0	IC-Ib	0	0
00	11	01	11	00	00	01	11	00	0	0	Ic	0	0	0	Ia-IB	0	0
00	11	01	00	00	11	01	11	00	0	0	Ic-IB	0	0	0	Ia	0	0
00	11	01	11	00	11	01	00	00	0	0	IA-Ib	0	0	0	IC	0	0
00	00	01	11	00	11	00	11	01	0	0	IA	0	0	0	0	0	IC-Ib
00	11	01	11	00	11	00	00	01	0	0	IA-Ib	0	0	0	0	0	IC
00	11	00	00	10	11	01	11	00	0	0	0	0	Ic-IB	0	Ia	0	0
00	11	00	11	10	11	01	00	00	0	0	0	0	IA-Ib	0	IC	0	0
00	11	00	11	10	00	00	11	01	0	0	0	0	Ia-IB	0	0	0	Ic
00	11	00	11	10	11	00	00	01	0	0	0	0	IA-Ib	0	0	0	IC
00	11	00	11	00	00	01	11	01	0	0	0	0	0	0	Ia-IB	0	Ic
00	11	00	00	00	11	01	11	01	0	0	0	0	0	0	Ia	0	Ic-IB
employ three capacitors																	
01	11	01	00	10	00	00	11	00	Ia	0	Ic	0	-IB	0	0	0	0
01	00	01	11	10	00	00	11	00	IA-Ic	0	Ic	0	IC-Ib	0	0	0	0
01	00	01	00	10	11	00	11	00	Ia	0	IA-Ia	0	IC-Ib	0	0	0	0
01	11	01	11	00	00	01	00	00	IA+Ia	0	Ic	0	0	0	IC	0	0
01	11	01	00	00	11	01	00	00	Ia-IC	0	Ic-IB	0	0	0	IC	0	0
01	00	01	11	00	00	01	11	00	IA-Ic	0	Ic	0	0	0	IC-Ib	0	0
01	00	01	00	00	11	01	11	00	-IC-Ic	0	Ic-IB	0	0	0	IC-Ib	0	0
01	11	01	11	00	00	00	00	01	Ia-IB	0	Ic-IC	0	0	0	0	0	IC
01	11	01	00	00	11	00	00	01	Ia	0	IA+Ic	0	0	0	0	0	IC
01	00	01	11	00	00	00	11	01	Ia-IB	0	-IC-Ia	0	0	0	0	0	IC-Ib

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
01	00	01	00	00	11	00	11	01	Ia	0	IA-Ia	0	0	0	0	0	IC-Ib
01	00	00	00	10	11	01	11	00	IA	0	0	0	Ic-IB	0	Ia-IA	0	0
01	00	00	11	10	11	01	00	00	IA	0	0	0	-Ib	0	IC	0	0
01	11	00	00	10	11	01	00	00	Ia-IC	0	0	0	Ic-IB	0	IC	0	0
01	00	00	11	10	00	00	11	01	IA	0	0	0	IC+Ia	0	0	0	Ic
01	11	00	00	10	00	00	11	01	Ia	0	0	0	-IB	0	0	0	Ic
01	00	00	11	10	11	00	00	01	IA	0	0	0	-Ib	0	0	0	IC
01	11	00	00	10	11	00	00	01	Ia	0	0	0	IA+Ic	0	0	0	IC
01	00	00	11	00	00	01	11	01	IA	0	0	0	0	0	IC+Ia	0	Ic
01	00	00	00	00	11	01	11	01	IA	0	0	0	0	0	Ia-IA	0	Ic-IB
01	11	00	11	00	00	01	00	01	IA-Ib	0	0	0	0	0	IC-Ic	0	Ic
01	11	00	00	00	11	01	00	01	IA-Ib	0	0	0	0	0	-IA-Ic	0	Ic-IB
00	00	01	00	10	11	01	11	00	0	0	IA	0	IC+Ic	0	Ia	0	0
00	11	01	00	10	00	01	11	00	0	0	Ic	0	-IB	0	Ia	0	0
00	00	01	11	10	11	01	00	00	0	0	IA	0	-Ib	0	IC	0	0
00	11	01	11	10	00	01	00	00	0	0	Ic	0	IA+Ia	0	IC	0	0
00	00	01	11	10	00	00	11	01	0	0	IA	0	Ia-IB	0	0	0	Ic-IA
00	00	01	11	10	11	00	00	01	0	0	IA	0	-Ib	0	0	0	IC
00	11	01	11	10	00	00	00	01	0	0	Ic-IC	0	Ia-IB	0	0	0	IC
00	00	01	11	00	00	01	11	01	0	0	IA	0	0	0	Ia-IB	0	Ic-IA
00	00	01	00	00	11	01	11	01	0	0	IA	0	0	0	Ia	0	IC+Ic
00	11	01	11	00	00	01	00	01	0	0	IA-Ib	0	0	0	Ia-IB	0	-IA-Ia
00	11	01	00	00	11	01	00	01	0	0	IA-Ib	0	0	0	Ia	0	IC-Ia
00	11	00	00	10	00	01	11	01	0	0	0	0	-IB	0	Ia	0	Ic
00	11	00	11	10	00	01	00	01	0	0	0	0	IA-Ib	0	IC-Ic	0	Ic
00	11	00	00	10	11	01	00	01	0	0	0	0	IA-Ib	0	Ia	0	IC-Ia
employ four capacitors																	
01	11	01	00	10	00	01	00	00	Ia-IC	0	Ic	0	-IB	0	IC	0	0
01	00	01	00	10	00	01	11	00	IA-Ic	0	Ic	0	-IB	0	-IA-Ib	0	0
01	00	01	11	10	00	01	00	00	IA-Ic	0	Ic	0	-Ib	0	IC	0	0
01	00	01	00	10	11	01	00	00	Ia-IC	0	-IB-Ia	0	-Ib	0	IC	0	0
01	11	01	00	10	00	00	00	01	Ia	0	Ic-IC	0	-IB	0	0	0	IC
01	00	01	00	10	00	00	11	01	Ia	0	IA-Ia	0	-IB	0	0	0	-IA-Ib
01	00	01	11	10	00	00	00	01	-IB-Ic	0	Ic-IC	0	-Ib	0	0	0	IC
01	00	01	00	10	11	00	00	01	Ia	0	IA-Ia	0	-Ib	0	0	0	IC
01	00	00	00	10	00	01	11	01	IA	0	0	0	-IB	0	Ia-IA	0	Ic
01	00	00	11	10	00	01	00	01	IA	0	0	0	-Ib	0	IC-Ic	0	Ic
01	00	00	00	10	11	01	00	01	IA	0	0	0	-Ib	0	Ia-IA	0	-IB-Ia
01	11	00	00	10	00	01	00	01	-IC-Ib	0	0	0	-IB	0	IC-Ic	0	Ic
00	00	01	00	10	00	01	11	01	0	0	IA	0	-IB	0	Ia	0	Ic-IA
00	00	01	11	10	00	01	00	01	0	0	IA	0	-Ib	0	-IB-Ic	0	Ic-IA
00	00	01	00	10	11	01	00	01	0	0	IA	0	-Ib	0	Ia	0	IC-Ia
00	11	01	00	10	00	01	00	01	0	0	-IC-Ib	0	-IB	0	Ia	0	IC-Ia

Table B.46: Switching device combinations for (V_{AB},V_{BC},V_{CA}) = ($+V_{cap}$,$-V_{cap}$,0) and (V_{ab},V_{bc},V_{ca}) = ($-V_{cap}$,0,$+V_{cap}$).

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
employ single capacitor																	
01	11	11	11	00	00	00	11	00	Ia-IB	0	0	0	0	0	0	0	0
01	11	11	11	00	00	00	00	11	Ia-IB	0	0	0	0	0	0	0	0
01	11	00	11	00	00	00	11	11	Ia-IB	0	0	0	0	0	0	0	0
01	00	11	11	00	00	00	11	11	Ia-IB	0	0	0	0	0	0	0	0
00	11	00	11	10	00	00	11	11	0	0	0	0	Ia-IB	0	0	0	0
00	00	11	11	10	00	00	11	11	0	0	0	0	Ia-IB	0	0	0	0
00	11	11	11	10	00	00	11	00	0	0	0	0	Ia-IB	0	0	0	0
00	11	11	11	10	00	00	00	11	0	0	0	0	Ia-IB	0	0	0	0
00	11	00	11	00	10	00	11	11	0	0	0	0	0	Ia-IB	0	0	0
00	00	11	11	00	10	00	11	11	0	0	0	0	0	Ia-IB	0	0	0
00	11	11	11	00	10	00	11	00	0	0	0	0	0	Ia-IB	0	0	0
00	11	11	11	00	10	00	00	11	0	0	0	0	0	Ia-IB	0	0	0
00	11	00	11	00	00	01	11	11	0	0	0	0	0	0	Ia-IB	0	0
00	00	11	11	00	00	01	11	11	0	0	0	0	0	0	Ia-IB	0	0
00	11	11	11	00	00	01	11	00	0	0	0	0	0	0	Ia-IB	0	0
00	11	11	11	00	00	01	00	11	0	0	0	0	0	0	Ia-IB	0	0
employ two capacitors																	
01	00	00	11	10	00	00	11	11	IA	0	0	0	IC+Ia	0	0	0	0
01	11	11	00	10	00	00	11	00	Ia	0	0	0	-IB	0	0	0	0
01	11	11	00	10	00	00	00	11	Ia	0	0	0	-IB	0	0	0	0
01	11	00	00	10	00	00	11	11	Ia	0	0	0	-IB	0	0	0	0
01	00	11	00	10	00	00	11	11	Ia	0	0	0	-IB	0	0	0	0
01	00	11	11	10	00	00	11	00	IA-Ic	0	0	0	IC-Ib	0	0	0	0
01	00	11	11	10	00	00	00	11	-IB-Ic	0	0	0	-Ib	0	0	0	0
01	00	00	11	00	10	00	11	11	IA	0	0	0	0	IC+Ia	0	0	0
01	11	11	00	00	10	00	11	00	Ia	0	0	0	0	-IB	0	0	0
01	11	11	00	00	10	00	00	11	Ia	0	0	0	0	-IB	0	0	0
01	11	00	00	00	10	00	11	11	Ia	0	0	0	0	-IB	0	0	0
01	00	11	00	00	10	00	11	11	Ia	0	0	0	0	-IB	0	0	0
01	11	00	11	00	10	00	11	00	-IB-Ib	0	0	0	0	-Ic	0	0	0
01	11	00	11	00	10	00	00	11	IA-Ib	0	0	0	0	IC-Ic	0	0	0
01	00	00	11	00	00	01	11	11	IA	0	0	0	0	0	IC+Ia	0	0
01	11	11	11	00	00	01	00	00	IA+Ia	0	0	0	0	0	IC	0	0
01	00	11	11	00	00	01	11	00	IA-Ic	0	0	0	0	0	IC-Ib	0	0
01	11	00	11	00	00	01	00	11	IA-Ib	0	0	0	0	0	IC-Ic	0	0
00	11	00	11	10	10	00	11	00	0	0	0	0	-IB-Ib	-Ic	0	0	0
00	00	11	11	10	10	00	11	00	0	0	0	0	IC-Ib	IA-Ic	0	0	0
00	11	00	11	10	10	00	00	11	0	0	0	0	IA-Ib	IC-Ic	0	0	0
00	00	11	11	10	10	00	00	11	0	0	0	0	-Ib	-IB-Ic	0	0	0
00	11	00	11	10	00	01	00	11	0	0	0	0	IA-Ib	0	IC-Ic	0	0
00	11	00	00	10	00	01	11	11	0	0	0	0	-IB	0	Ia	0	0

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
00	00	11	00	10	00	01	11	11	0	0	0	0	-IB	0	Ia	0	0
00	00	11	11	10	00	01	00	11	0	0	0	0	-Ib	0	-IB-Ic	0	0
00	11	11	00	10	00	01	11	00	0	0	0	0	-IB	0	Ia	0	0
00	11	11	00	10	00	01	00	11	0	0	0	0	-IB	0	Ia	0	0
00	11	11	11	10	00	01	00	00	0	0	0	0	IA+Ia	0	IC	0	0
00	11	00	00	00	10	01	11	11	0	0	0	0	0	-IB	Ia	0	0
00	00	11	00	00	10	01	11	11	0	0	0	0	0	-IB	Ia	0	0
00	11	00	11	00	10	01	11	00	0	0	0	0	0	-Ic	-IB-Ib	0	0
00	00	11	11	00	10	01	11	00	0	0	0	0	0	IA-Ic	IC-Ib	0	0
00	11	11	00	00	10	01	11	00	0	0	0	0	0	-IB	Ia	0	0
00	11	11	00	00	10	01	00	11	0	0	0	0	0	-IB	Ia	0	0
00	11	11	11	00	10	01	00	00	0	0	0	0	0	IA+Ia	IC	0	0
employ three capacitors																	
01	00	00	00	10	00	01	11	11	IA	0	0	0	-IB	0	Ia-IA	0	0
01	00	00	11	10	00	01	00	11	IA	0	0	0	-Ib	0	IC-Ic	0	0
01	11	11	00	10	00	01	00	00	Ia-IC	0	0	0	-IB	0	IC	0	0
01	00	11	00	10	00	01	11	00	IA-Ic	0	0	0	-IB	0	-IA-Ib	0	0
01	11	00	00	10	00	01	00	11	-IC-Ib	0	0	0	-IB	0	IC-Ic	0	0
01	00	11	11	10	00	01	00	00	IA-Ic	0	0	0	-Ib	0	IC	0	0
01	00	00	11	10	10	00	11	00	IA	0	0	0	IC-Ib	-Ic	0	0	0
01	00	00	11	10	10	00	00	11	IA	0	0	0	-Ib	IC-Ic	0	0	0
01	11	00	00	10	10	00	11	00	Ia	0	0	0	Ic-IB	-Ic	0	0	0
01	00	11	00	10	10	00	11	00	Ia	0	0	0	IC-Ib	IA+Ib	0	0	0
01	11	00	00	10	10	00	00	11	Ia	0	0	0	IA+Ic	IC-Ic	0	0	0
01	00	11	00	10	10	00	00	11	Ia	0	0	0	-Ib	Ib-IB	0	0	0
01	00	00	00	00	10	01	11	11	IA	0	0	0	0	-IB	Ia-IA	0	0
01	00	00	11	00	10	01	11	00	IA	0	0	0	0	-Ic	IC-Ib	0	0
01	11	11	00	00	10	01	00	00	Ia-IC	0	0	0	0	-IB	IC	0	0
01	00	11	00	00	10	01	11	00	-IC-Ic	0	0	0	0	-IB	IC-Ib	0	0
01	11	00	00	00	10	01	00	11	IA-Ib	0	0	0	0	-IB	-IA-Ic	0	0
01	11	00	11	00	10	01	00	00	IA-Ib	0	0	0	0	-Ic	IC	0	0
00	11	00	00	10	10	01	11	00	0	0	0	0	Ic-IB	-Ic	Ia	0	0
00	11	00	00	10	10	01	00	11	0	0	0	0	IA-Ib	IC+Ib	Ia	0	0
00	00	11	00	10	10	01	11	00	0	0	0	0	IC+Ic	IA-Ic	Ia	0	0
00	00	11	00	10	10	01	00	11	0	0	0	0	-Ib	Ib-IB	Ia	0	0
00	11	00	11	10	10	01	00	00	0	0	0	0	IA-Ib	-Ic	IC	0	0
00	00	11	11	10	10	01	00	00	0	0	0	0	-Ib	IA-Ic	IC	0	0
employ four capacitors																	
01	00	00	00	10	10	01	11	00	IA	0	0	0	Ic-IB	-Ic	Ia-IA	0	0
01	00	00	00	10	10	01	00	11	IA	0	0	0	-Ib	Ib-IB	Ia-IA	0	0
01	00	00	11	10	10	01	00	00	IA	0	0	0	-Ib	-Ic	IC	0	0
01	11	00	00	10	10	01	00	00	Ia-IC	0	0	0	Ic-IB	-Ic	IC	0	0
01	00	11	00	10	10	01	00	00	Ia-IC	0	0	0	-Ib	Ib-IB	IC	0	0

Table B.47: Switching device combinations for (V_{AB},V_{BC},V_{CA}) = ($+V_{cap}$,$-V_{cap}$,0) and (V_{ab},V_{bc},V_{ca}) = (0,$-V_{cap}$,$+V_{cap}$).

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
employ single capacitor																	
01	00	11	11	11	00	00	00	11	-IB-Ic	0	0	0	0	0	0	0	0
00	01	11	11	11	00	00	00	11	0	-IB-Ic	0	0	0	0	0	0	0
00	00	11	11	11	10	00	00	11	0	0	0	0	0	-IB-Ic	0	0	0
00	00	11	11	11	00	01	00	11	0	0	0	0	0	0	-IB-Ic	0	0
00	00	11	11	11	00	00	01	11	0	0	0	0	0	0	0	-IB-Ic	0
employ two capacitors																	
01	01	11	11	00	00	00	00	11	Ia-IB	Ib	0	0	0	0	0	0	0
01	01	11	00	11	00	00	00	11	Ia	Ib-IB	0	0	0	0	0	0	0
01	00	00	11	11	10	00	00	11	IA	0	0	0	0	IC-Ic	0	0	0
01	00	11	00	11	10	00	00	11	Ia	0	0	0	0	Ib-IB	0	0	0
01	00	00	11	11	00	01	00	11	IA	0	0	0	0	0	IC-Ic	0	0
01	00	11	11	11	00	01	00	00	IA-Ic	0	0	0	0	0	IC	0	0
01	00	00	11	11	00	00	01	11	IA	0	0	0	0	0	0	IC-Ic	0
01	00	11	11	00	00	00	01	11	Ia-IB	0	0	0	0	0	0	Ib	0
01	00	11	00	11	00	00	01	11	Ia	0	0	0	0	0	0	Ib-IB	0
01	00	11	11	11	00	00	01	00	IA-Ic	0	0	0	0	0	0	IC	0
00	01	00	11	11	10	00	00	11	0	IA	0	0	0	IC-Ic	0	0	0
00	01	11	11	00	10	00	00	11	0	Ib	0	0	0	Ia-IB	0	0	0
00	01	00	11	11	00	01	00	11	0	IA	0	0	0	0	IC-Ic	0	0
00	01	11	11	00	00	01	00	11	0	Ib	0	0	0	0	Ia-IB	0	0
00	01	11	00	11	00	01	00	11	0	Ib-IB	0	0	0	0	Ia	0	0
00	01	11	11	11	00	01	00	00	0	IA-Ic	0	0	0	0	IC	0	0
00	01	00	11	11	00	00	01	11	0	IA	0	0	0	0	0	IC-Ic	0
00	01	11	11	11	00	00	01	00	0	IA-Ic	0	0	0	0	0	IC	0
00	00	11	00	11	10	01	00	11	0	0	0	0	0	Ib-IB	Ia	0	0
00	00	11	11	11	10	01	00	00	0	0	0	0	0	IA-Ic	IC	0	0
00	00	11	11	00	10	00	01	11	0	0	0	0	0	Ia-IB	0	Ib	0
00	00	11	11	11	10	00	01	00	0	0	0	0	0	IA-Ic	0	IC	0
00	00	11	11	00	00	01	01	11	0	0	0	0	0	0	Ia-IB	Ib	0
00	00	11	00	11	00	01	01	11	0	0	0	0	0	0	Ia	Ib-IB	0
employ three capacitors																	
01	01	11	00	00	10	00	00	11	Ia	Ib	0	0	0	-IB	0	0	0
01	01	00	11	00	10	00	00	11	IA-Ib	Ib	0	0	0	IC-Ic	0	0	0
01	01	00	00	11	10	00	00	11	Ia	IA-Ia	0	0	0	IC-Ic	0	0	0
01	01	11	11	00	00	01	00	00	IA+Ia	Ib	0	0	0	0	IC	0	0
01	01	11	00	11	00	01	00	00	Ia-IC	Ib-IB	0	0	0	0	IC	0	0
01	01	00	11	00	00	01	00	11	IA-Ib	Ib	0	0	0	0	IC-Ic	0	0
01	01	00	00	11	00	01	00	11	-IC-Ib	Ib-IB	0	0	0	0	IC-Ic	0	0
01	01	11	11	00	00	00	01	00	Ia-IB	Ib-IC	0	0	0	0	0	IC	0
01	01	11	00	11	00	00	01	00	Ia	IA+Ib	0	0	0	0	0	IC	0
01	01	00	11	00	00	00	01	11	Ia-IB	-IC-Ia	0	0	0	0	0	IC-Ic	0

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
01	01	00	00	11	00	00	01	11	Ia	IA-Ia	0	0	0	0	0	IC-Ic	0
01	00	00	00	11	10	01	00	11	IA	0	0	0	0	Ib-IB	Ia-IA	0	0
01	00	00	11	11	10	01	00	00	IA	0	0	0	0	-Ic	IC	0	0
01	00	11	00	11	10	01	00	00	Ia-IC	0	0	0	0	Ib-IB	IC	0	0
01	00	00	11	00	10	00	01	11	IA	0	0	0	0	IC+Ia	0	Ib	0
01	00	11	00	00	10	00	01	11	Ia	0	0	0	0	-IB	0	Ib	0
01	00	00	11	11	10	00	01	00	IA	0	0	0	0	-Ic	0	IC	0
01	00	11	00	11	10	00	01	00	Ia	0	0	0	0	IA+Ib	0	IC	0
01	00	00	11	00	00	01	01	11	IA	0	0	0	0	0	IC+Ia	Ib	0
01	00	00	00	11	00	01	01	11	IA	0	0	0	0	0	Ia-IA	Ib-IB	0
01	00	11	11	00	00	01	01	00	IA-Ic	0	0	0	0	0	IC-Ib	Ib	0
01	00	11	00	11	00	01	01	00	IA-Ic	0	0	0	0	0	-IA-Ib	Ib-IB	0
00	01	00	00	11	10	01	00	11	0	IA	0	0	0	IC+Ib	Ia	0	0
00	01	11	00	00	10	01	00	11	0	Ib	0	0	0	-IB	Ia	0	0
00	01	00	11	11	10	01	00	00	0	IA	0	0	0	-Ic	IC	0	0
00	01	11	11	00	10	01	00	00	0	Ib	0	0	0	IA+Ia	IC	0	0
00	01	00	11	00	10	00	01	11	0	IA	0	0	0	Ia-IB	0	Ib-IA	0
00	01	00	11	11	10	00	01	00	0	IA	0	0	0	-Ic	0	IC	0
00	01	11	11	00	10	00	01	00	0	Ib-IC	0	0	0	Ia-IB	0	IC	0
00	01	00	11	00	00	01	01	11	0	IA	0	0	0	0	Ia-IB	Ib-IA	0
00	01	00	00	11	00	01	01	11	0	IA	0	0	0	0	Ia	IC+Ib	0
00	01	11	11	00	00	01	01	00	0	IA-Ic	0	0	0	0	Ia-IB	-IA-Ia	0
00	01	11	00	11	00	01	01	00	0	IA-Ic	0	0	0	0	Ia	IC-Ia	0
00	00	11	00	00	10	01	01	11	0	0	0	0	0	-IB	Ia	Ib	0
00	00	11	11	00	10	01	01	00	0	0	0	0	0	IA-Ic	IC-Ib	Ib	0
00	00	11	00	11	10	01	01	00	0	0	0	0	0	IA-Ic	Ia	IC-Ia	0
employ four capacitors																	
01	01	11	00	00	10	01	00	00	Ia-IC	Ib	0	0	0	-IB	IC	0	0
01	01	00	00	00	10	01	00	11	IA-Ib	Ib	0	0	0	-IB	-IA-Ic	0	0
01	01	00	11	00	10	01	00	00	IA-Ib	Ib	0	0	0	-Ic	IC	0	0
01	01	00	00	11	10	01	00	00	Ia-IC	-IB-Ia	0	0	0	-Ic	IC	0	0
01	01	11	00	00	10	00	01	00	Ia	Ib-IC	0	0	0	-IB	0	IC	0
01	01	00	00	00	10	00	01	11	Ia	IA-Ia	0	0	0	-IB	0	-IA-Ic	0
01	01	00	11	00	10	00	01	00	-IB-Ib	Ib-IC	0	0	0	-Ic	0	IC	0
01	01	00	00	11	10	00	01	00	Ia	IA-Ia	0	0	0	-Ic	0	IC	0
01	00	00	00	00	10	01	01	11	IA	0	0	0	0	-IB	Ia-IA	Ib	0
01	00	00	11	00	10	01	01	00	IA	0	0	0	0	-Ic	IC-Ib	Ib	0
01	00	00	00	11	10	01	01	00	IA	0	0	0	0	-Ic	Ia-IA	-IB-Ia	0
01	00	11	00	00	10	01	01	00	-IC-Ic	0	0	0	0	-IB	IC-Ib	Ib	0
00	01	00	00	00	10	01	01	11	0	IA	0	0	0	-IB	Ia	Ib-IA	0
00	01	00	11	00	10	01	01	00	0	IA	0	0	0	-Ic	-IB-Ib	Ib-IA	0
00	01	00	00	11	10	01	01	00	0	IA	0	0	0	-Ic	Ia	IC-Ia	0
00	01	11	00	00	10	01	01	00	0	-IC-Ic	0	0	0	-IB	Ia	IC-Ia	0

Table B.48: Switching device combinations for (V_{AB},V_{BC},V_{CA}) = ($+V_{cap}$,$-V_{cap}$,0) and (V_{ab},V_{bc},V_{ca}) = ($+V_{cap}$,$-V_{cap}$,0).

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
employ single capacitor																	
11	01	11	00	11	00	11	00	00	0	Ib-IB	0	0	0	0	0	0	0
11	01	11	00	11	00	00	00	11	0	Ib-IB	0	0	0	0	0	0	0
11	01	00	00	11	00	11	00	11	0	Ib-IB	0	0	0	0	0	0	0
00	01	11	00	11	00	11	00	11	0	Ib-IB	0	0	0	0	0	0	0
11	00	00	10	11	00	11	00	11	0	0	0	Ib-IB	0	0	0	0	0
00	00	11	10	11	00	11	00	11	0	0	0	Ib-IB	0	0	0	0	0
11	00	11	10	11	00	11	00	00	0	0	0	Ib-IB	0	0	0	0	0
11	00	11	10	11	00	00	00	11	0	0	0	Ib-IB	0	0	0	0	0
11	00	00	00	11	10	11	00	11	0	0	0	0	0	Ib-IB	0	0	0
00	00	11	00	11	10	11	00	11	0	0	0	0	0	Ib-IB	0	0	0
11	00	11	00	11	10	11	00	00	0	0	0	0	0	Ib-IB	0	0	0
11	00	11	00	11	10	00	00	11	0	0	0	0	0	Ib-IB	0	0	0
11	00	00	00	11	00	11	01	11	0	0	0	0	0	0	0	Ib-IB	0
00	00	11	00	11	00	11	01	11	0	0	0	0	0	0	0	Ib-IB	0
11	00	11	00	11	00	11	01	00	0	0	0	0	0	0	0	Ib-IB	0
11	00	11	00	11	00	00	01	11	0	0	0	0	0	0	0	Ib-IB	0
employ two capacitors																	
11	01	11	10	00	00	11	00	00	0	Ib	0	-IB	0	0	0	0	0
11	01	11	10	00	00	00	00	11	0	Ib	0	-IB	0	0	0	0	0
11	01	00	10	00	00	11	00	11	0	Ib	0	-IB	0	0	0	0	0
00	01	11	10	00	00	11	00	11	0	Ib	0	-IB	0	0	0	0	0
00	01	00	10	11	00	11	00	11	0	IA	0	IC+Ib	0	0	0	0	0
00	01	11	10	11	00	11	00	00	0	IA-Ic	0	IC-Ia	0	0	0	0	0
00	01	11	10	11	00	00	00	11	0	-IB-Ic	0	-Ia	0	0	0	0	0
11	01	11	00	00	10	11	00	00	0	Ib	0	0	0	-IB	0	0	0
11	01	11	00	00	10	00	00	11	0	Ib	0	0	0	-IB	0	0	0
11	01	00	00	00	10	11	00	11	0	Ib	0	0	0	-IB	0	0	0
00	01	11	00	00	10	11	00	11	0	Ib	0	0	0	-IB	0	0	0
00	01	00	00	11	10	11	00	11	0	IA	0	0	0	IC+Ib	0	0	0
11	01	00	00	11	10	11	00	00	0	-IB-Ia	0	0	0	-Ic	0	0	0
11	01	00	00	11	10	00	00	11	0	IA-Ia	0	0	0	IC-Ic	0	0	0
00	01	00	00	11	00	11	01	11	0	IA	0	0	0	0	0	IC+Ib	0
11	01	11	00	11	00	00	01	00	0	IA+Ib	0	0	0	0	0	IC	0
00	01	11	00	11	00	11	01	00	0	IA-Ic	0	0	0	0	0	IC-Ia	0
11	01	00	00	11	00	00	01	11	0	IA-Ia	0	0	0	0	0	IC-Ic	0
11	00	00	10	11	10	11	00	00	0	0	0	-IB-Ia	0	-Ic	0	0	0
00	00	11	10	11	10	11	00	00	0	0	0	IC-Ia	0	IA-Ic	0	0	0
11	00	00	10	11	10	00	00	11	0	0	0	IA-Ia	0	IC-Ic	0	0	0
00	00	11	10	11	10	00	00	11	0	0	0	-Ia	0	-IB-Ic	0	0	0
11	00	00	10	00	00	11	01	11	0	0	0	-IB	0	0	0	Ib	0
00	00	11	10	00	00	11	01	11	0	0	0	-IB	0	0	0	Ib	0

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
11	00	11	10	00	00	11	01	00	0	0	0	-IB	0	0	0	Ib	0
11	00	11	10	00	00	00	01	11	0	0	0	-IB	0	0	0	Ib	0
11	00	00	10	11	00	00	01	11	0	0	0	IA-Ia	0	0	0	IC-Ic	0
00	00	11	10	11	00	00	01	11	0	0	0	-Ia	0	0	0	-IB-Ic	0
11	00	11	10	11	00	00	01	00	0	0	0	IA+Ib	0	0	0	IC	0
11	00	00	00	00	10	11	01	11	0	0	0	0	0	-IB	0	Ib	0
00	00	11	00	00	10	11	01	11	0	0	0	0	0	-IB	0	Ib	0
11	00	11	00	00	10	11	01	00	0	0	0	0	0	-IB	0	Ib	0
11	00	11	00	00	10	00	01	11	0	0	0	0	0	-IB	0	Ib	0
11	00	00	00	11	10	11	01	00	0	0	0	0	0	-Ic	0	-IB-Ia	0
00	00	11	00	11	10	11	01	00	0	0	0	0	0	IA-Ic	0	IC-Ia	0
11	00	11	00	11	10	00	01	00	0	0	0	0	0	IA+Ib	0	IC	0
employ three capacitors																	
00	01	00	10	11	10	11	00	00	0	IA	0	IC-Ia	0	-Ic	0	0	0
00	01	00	10	11	10	00	00	11	0	IA	0	-Ia	0	IC-Ic	0	0	0
11	01	00	10	00	10	11	00	00	0	Ib	0	Ic-IB	0	-Ic	0	0	0
00	01	11	10	00	10	11	00	00	0	Ib	0	IC-Ia	0	IA+Ia	0	0	0
11	01	00	10	00	10	00	00	11	0	Ib	0	IA+Ic	0	IC-Ic	0	0	0
00	01	11	10	00	10	00	00	11	0	Ib	0	-Ia	0	Ia-IB	0	0	0
00	01	00	10	00	00	11	01	11	0	IA	0	-IB	0	0	0	Ib-IA	0
00	01	00	10	11	00	00	01	11	0	IA	0	-Ia	0	0	0	IC-Ic	0
11	01	11	10	00	00	00	01	00	0	Ib-IC	0	-IB	0	0	0	IC	0
00	01	11	10	00	00	11	01	00	0	IA-Ic	0	-IB	0	0	0	-IA-Ia	0
11	01	00	10	00	00	00	01	11	0	-IC-Ia	0	-IB	0	0	0	IC-Ic	0
00	01	11	10	11	00	00	01	00	0	IA-Ic	0	-Ia	0	0	0	IC	0
00	01	00	00	00	10	11	01	11	0	IA	0	0	0	-IB	0	Ib-IA	0
00	01	00	00	11	10	11	01	00	0	IA	0	0	0	-Ic	0	IC-Ia	0
11	01	11	00	00	10	00	01	00	0	Ib-IC	0	0	0	-IB	0	IC	0
00	01	11	00	00	10	11	01	00	0	-IC-Ic	0	0	0	-IB	0	IC-Ia	0
11	01	00	00	00	10	00	01	11	0	IA-Ia	0	0	0	-IB	0	-IA-Ic	0
11	01	00	00	11	10	00	01	00	0	IA-Ia	0	0	0	-Ic	0	IC	0
11	00	00	10	00	10	11	01	00	0	0	0	Ic-IB	0	-Ic	0	Ib	0
11	00	00	10	00	10	00	01	11	0	0	0	IA-Ia	0	IC+Ia	0	Ib	0
00	00	11	10	00	10	11	01	00	0	0	0	IC+Ic	0	IA-Ic	0	Ib	0
00	00	11	10	00	10	00	01	11	0	0	0	-Ia	0	Ia-IB	0	Ib	0
11	00	00	10	11	10	00	01	00	0	0	0	IA-Ia	0	-Ic	0	IC	0
00	00	11	10	11	10	00	01	00	0	0	0	-Ia	0	IA-Ic	0	IC	0
employ four capacitors																	
00	01	00	10	00	10	11	01	00	0	IA	0	Ic-IB	0	-Ic	0	Ib-IA	0
00	01	00	10	00	10	00	01	11	0	IA	0	-Ia	0	Ia-IB	0	Ib-IA	0
00	01	00	10	11	10	00	01	00	0	IA	0	-Ia	0	-Ic	0	IC	0
11	01	00	10	00	10	00	01	00	0	Ib-IC	0	Ic-IB	0	-Ic	0	IC	0
00	01	11	10	00	10	00	01	00	0	Ib-IC	0	-Ia	0	Ia-IB	0	IC	0

Table B.49: Switching device combinations for (V_{AB},V_{BC},V_{CA}) = (0,0,0) and (V_{ab},V_{bc},V_{ca}) = ($+2V_{cap}$,$-V_{cap}$,$-V_{cap}$).

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
employ two capacitors																	
10	01	11	00	00	11	00	00	11	-Ia	Ib	0	0	0	0	0	0	0
10	00	11	00	01	11	00	00	11	-Ia	0	0	0	Ib	0	0	0	0
10	00	11	00	00	11	00	01	11	-Ia	0	0	0	0	0	0	Ib	0
00	01	11	10	00	11	00	00	11	0	Ib	0	-Ia	0	0	0	0	0
00	01	11	00	00	11	10	00	11	0	Ib	0	0	0	0	-Ia	0	0
00	00	11	10	01	11	00	00	11	0	0	0	-Ia	Ib	0	0	0	0
00	00	11	10	00	11	00	01	11	0	0	0	-Ia	0	0	0	Ib	0
00	00	11	00	01	11	10	00	11	0	0	0	0	Ib	0	-Ia	0	0
00	00	11	00	00	11	10	01	11	0	0	0	0	0	0	-Ia	Ib	0
employ three capacitors																	
10	01	00	10	00	11	00	00	11	Ib-IA	Ib	0	IA+Ic	0	0	0	0	0
10	01	11	10	00	00	00	00	11	IB-Ia	Ib	0	-IB	0	0	0	0	0
10	01	00	00	01	11	00	00	11	-Ia	IA-Ia	0	0	-IA-Ic	0	0	0	0
10	01	11	00	01	00	00	00	11	-Ia	Ib-IB	0	0	IB	0	0	0	0
10	01	00	00	00	11	10	00	11	Ib-IA	Ib	0	0	0	0	IA+Ic	0	0
10	01	11	00	00	11	10	00	00	IC-Ia	Ib	0	0	0	0	-IC	0	0
10	01	00	00	00	11	00	01	11	-Ia	IA-Ia	0	0	0	0	0	-IA-Ic	0
10	01	11	00	00	11	00	01	00	-Ia	Ib-IC	0	0	0	0	0	IC	0
10	00	00	10	01	11	00	00	11	-IA	0	0	IA-Ia	Ib	0	0	0	0
10	00	11	10	01	00	00	00	11	IB+Ic	0	0	Ib-IB	Ib	0	0	0	0
10	00	00	10	00	11	00	01	11	-IA	0	0	IA-Ia	0	0	0	Ib	0
10	00	11	10	00	00	00	01	11	IB-Ia	0	0	-IB	0	0	0	Ib	0
10	00	00	00	01	11	10	00	11	-IA	0	0	0	Ib	0	IA-Ia	0	0
10	00	11	00	01	11	10	00	00	IC-Ia	0	0	0	Ib	0	-IC	0	0
10	00	11	00	01	00	00	01	11	-Ia	0	0	0	IB	0	0	Ib-IB	0
10	00	11	00	01	11	00	01	00	-Ia	0	0	0	Ib-IC	0	0	IC	0
10	00	00	00	00	11	10	01	11	-IA	0	0	0	0	0	IA-Ia	Ib	0
10	00	11	00	00	11	10	01	00	IC+Ic	0	0	0	0	0	Ib-IC	Ib	0
00	01	00	10	01	11	00	00	11	0	IA	0	-Ia	Ib-IA	0	0	0	0
00	01	11	10	01	00	00	00	11	0	-IB-Ic	0	-Ia	IB-Ia	0	0	0	0
00	01	11	10	00	00	10	00	11	0	Ib	0	-IB	0	0	IB-Ia	0	0
00	01	11	10	00	11	10	00	00	0	Ib	0	IC-Ia	0	0	-IC	0	0
00	01	00	10	00	11	00	01	11	0	IA	0	-Ia	0	0	0	Ib-IA	0
00	01	11	10	00	11	00	01	00	0	Ib-IC	0	-Ia	0	0	0	IC	0
00	01	00	00	01	11	10	00	11	0	IA	0	0	Ib-IA	0	-Ia	0	0
00	01	11	00	01	00	10	00	11	0	Ib-IB	0	0	IB	0	-Ia	0	0
00	01	00	00	00	11	10	01	11	0	IA	0	0	0	0	-Ia	Ib-IA	0
00	01	11	00	00	11	10	01	00	0	-IC-Ic	0	0	0	0	-Ia	IC-Ia	0
00	00	11	10	01	00	10	00	11	0	0	0	Ib-IB	Ib	0	IB+Ic	0	0
00	00	11	10	01	11	10	00	00	0	0	0	IC-Ia	Ib	0	-IC	0	0
00	00	11	10	01	00	00	01	11	0	0	0	-Ia	IB-Ia	0	0	-IB-Ic	0

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
00	00	11	10	01	11	00	01	00	0	0	0	-Ia	Ib-IC	0	0	IC	0
00	00	11	10	00	00	10	01	11	0	0	0	-IB	0	0	IB-Ia	Ib	0
00	00	11	10	00	11	10	01	00	0	0	0	IC+Ic	0	0	Ib-IC	Ib	0
00	00	11	00	01	00	10	01	11	0	0	0	0	IB	0	-Ia	Ib-IB	0
00	00	11	00	01	11	10	01	00	0	0	0	0	-IC-Ic	0	-Ia	IC-Ia	0
employ four capacitors																	
10	01	00	10	00	00	10	00	11	Ib-IA	Ib	0	-IB	0	0	Ic-IC	0	0
10	01	00	10	00	11	10	00	00	Ib-IA	Ib	0	Ic-IB	0	0	-IC	0	0
10	01	11	10	00	00	10	00	00	-IA-Ia	Ib	0	-IB	0	0	-IC	0	0
10	01	00	10	00	00	00	01	11	IB-Ia	-IC-Ia	0	-IB	0	0	0	IC-Ic	0
10	01	00	10	00	11	00	01	00	IB+Ib	Ib-IC	0	Ic-IB	0	0	0	IC	0
10	01	11	10	00	00	00	01	00	IB-Ia	Ib-IC	0	-IB	0	0	0	IC	0
10	01	00	00	01	00	10	00	11	IC+Ib	Ib-IB	0	0	IB	0	Ic-IC	0	0
10	01	00	00	01	11	10	00	00	IC-Ia	-IB-Ia	0	0	IB-Ic	0	-IC	0	0
10	01	11	00	01	00	10	00	00	IC-Ia	Ib-IB	0	0	IB	0	-IC	0	0
10	01	00	00	01	00	00	01	11	-Ia	IA-Ia	0	0	IB	0	0	IC-Ic	0
10	01	00	00	01	11	00	01	00	-Ia	IA-Ia	0	0	IB-Ic	0	0	IC	0
10	01	11	00	01	00	00	01	00	-Ia	IA+Ib	0	0	IB	0	0	IC	0
10	00	00	10	01	00	10	00	11	-IA	0	0	Ib-IB	Ib	0	Ic-IC	0	0
10	00	00	10	01	11	10	00	00	-IA	0	0	-IB-Ia	Ib	0	-IC	0	0
10	00	11	10	01	00	10	00	00	Ic-IA	0	0	Ib-IB	Ib	0	-IC	0	0
10	00	00	10	01	00	00	01	11	-IA	0	0	IA-Ia	-IC-Ia	0	0	IC-Ic	0
10	00	00	10	01	11	00	01	00	-IA	0	0	IA-Ia	Ib-IC	0	0	IC	0
10	00	11	10	01	00	00	01	00	Ic-IA	0	0	IA+Ib	Ib-IC	0	0	IC	0
10	00	00	10	00	00	10	01	11	-IA	0	0	-IB	0	0	-IC-Ia	Ib	0
10	00	00	10	00	11	10	01	00	-IA	0	0	Ic-IB	0	0	Ib-IC	Ib	0
10	00	11	10	00	00	10	01	00	Ic-IA	0	0	-IB	0	0	Ib-IC	Ib	0
10	00	00	00	01	00	10	01	11	-IA	0	0	0	IB	0	IA-Ia	Ib-IB	0
10	00	00	00	01	11	10	01	00	-IA	0	0	0	IB-Ic	0	IA-Ia	-IB-Ia	0
10	00	11	00	01	00	10	01	00	Ic-IA	0	0	0	IB	0	IA+Ib	Ib-IB	0
00	01	00	10	01	00	10	00	11	0	IA	0	IC+Ib	Ib-IA	0	Ic-IC	0	0
00	01	00	10	01	11	10	00	00	0	IA	0	IC-Ia	Ib-IA	0	-IC	0	0
00	01	11	10	01	00	10	00	00	0	IA-Ic	0	IC-Ia	-IA-Ia	0	-IC	0	0
00	01	00	10	01	00	00	01	11	0	IA	0	-Ia	IB-Ia	0	0	IC-Ic	0
00	01	00	10	01	11	00	01	00	0	IA	0	-Ia	IB+Ib	0	0	IC	0
00	01	11	10	01	00	00	01	00	0	IA-Ic	0	-Ia	IB-Ia	0	0	IC	0
00	01	00	10	00	00	10	01	11	0	IA	0	-IB	0	0	IB-Ia	Ib-IA	0
00	01	00	10	00	11	10	01	00	0	IA	0	Ic-IB	0	0	IB+Ib	Ib-IA	0
00	01	11	10	00	00	10	01	00	0	IA-Ic	0	-IB	0	0	IB-Ia	-IA-Ia	0
00	01	00	00	01	00	10	01	11	0	IA	0	0	IB	0	-Ia	IC+Ib	0
00	01	00	00	01	11	10	01	00	0	IA	0	0	IB-Ic	0	-Ia	IC-Ia	0
00	01	11	00	01	00	10	01	00	0	IA-Ic	0	0	IB	0	-Ia	IC-Ia	0

Table B.50: Switching device combinations for (V_{AB},V_{BC},V_{CA}) = (0,0,0) and (V_{ab},V_{bc},V_{ca}) = ($+V_{cap}$,$+V_{cap}$,$-2V_{cap}$).

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
employ two capacitors																	
10	11	01	00	11	00	00	11	00	-Ia	0	Ic	0	0	0	0	0	0
10	11	00	00	11	01	00	11	00	-Ia	0	0	0	0	Ic	0	0	0
10	11	00	00	11	00	00	11	01	-Ia	0	0	0	0	0	0	0	Ic
00	11	01	10	11	00	00	11	00	0	0	Ic	-Ia	0	0	0	0	0
00	11	01	00	11	00	10	11	00	0	0	Ic	0	0	0	-Ia	0	0
00	11	00	10	11	01	00	11	00	0	0	0	-Ia	0	Ic	0	0	0
00	11	00	10	11	00	00	11	01	0	0	0	-Ia	0	0	0	0	Ic
00	11	00	00	11	01	10	11	00	0	0	0	0	0	Ic	-Ia	0	0
00	11	00	00	11	00	10	11	01	0	0	0	0	0	0	-Ia	0	Ic
employ three capacitors																	
10	00	01	10	11	00	00	11	00	Ic-IA	0	Ic	IA+Ib	0	0	0	0	0
10	11	01	10	00	00	00	11	00	IB-Ia	0	Ic	-IB	0	0	0	0	0
10	00	01	00	11	01	00	11	00	-Ia	0	IA-Ia	0	0	-IA-Ib	0	0	0
10	11	01	00	00	01	00	11	00	-Ia	0	Ic-IB	0	0	IB	0	0	0
10	00	01	00	11	00	10	11	00	Ic-IA	0	Ic	0	0	0	IA+Ib	0	0
10	11	01	00	11	00	10	00	00	IC-Ia	0	Ic	0	0	0	-IC	0	0
10	00	01	00	11	00	00	11	01	-Ia	0	IA-Ia	0	0	0	0	0	-IA-Ib
10	11	01	00	11	00	00	00	01	-Ia	0	Ic-IC	0	0	0	0	0	IC
10	00	00	10	11	01	00	11	00	-IA	0	0	IA-Ia	0	Ic	0	0	0
10	11	00	10	00	01	00	11	00	IB+Ib	0	0	Ic-IB	0	Ic	0	0	0
10	00	00	10	11	00	00	11	01	-IA	0	0	IA-Ia	0	0	0	0	Ic
10	11	00	10	00	00	00	11	01	IB-Ia	0	0	-IB	0	0	0	0	Ic
10	00	00	00	11	01	10	11	00	-IA	0	0	0	0	Ic	IA-Ia	0	0
10	11	00	00	11	01	10	00	00	IC-Ia	0	0	0	0	Ic	-IC	0	0
10	11	00	00	00	01	00	11	01	-Ia	0	0	0	0	IB	0	0	Ic-IB
10	11	00	00	11	01	00	00	01	-Ia	0	0	0	0	Ic-IC	0	0	IC
10	00	00	00	11	00	10	11	01	-IA	0	0	0	0	0	IA-Ia	0	Ic
10	11	00	00	11	00	10	00	01	IC+Ib	0	0	0	0	0	Ic-IC	0	Ic
00	00	01	10	11	01	00	11	00	0	0	IA	-Ia	0	Ic-IA	0	0	0
00	11	01	10	00	01	00	11	00	0	0	-IB-Ib	-Ia	0	IB-Ia	0	0	0
00	11	01	10	00	00	10	11	00	0	0	Ic	-IB	0	0	IB-Ia	0	0
00	11	01	10	11	00	10	00	00	0	0	Ic	IC-Ia	0	0	-IC	0	0
00	00	01	10	11	00	00	11	01	0	0	IA	-Ia	0	0	0	0	Ic-IA
00	11	01	10	11	00	00	00	01	0	0	Ic-IC	-Ia	0	0	0	0	IC
00	00	01	00	11	01	10	11	00	0	0	IA	0	0	Ic-IA	-Ia	0	0
00	11	01	00	00	01	10	11	00	0	0	Ic-IB	0	0	IB	-Ia	0	0
00	00	01	00	11	00	10	11	01	0	0	IA	0	0	0	-Ia	0	Ic-IA
00	11	01	00	11	00	10	00	01	0	0	-IC-Ib	0	0	0	-Ia	0	IC-Ia
00	11	00	10	00	01	10	11	00	0	0	0	Ic-IB	0	Ic	IB+Ib	0	0
00	11	00	10	11	01	10	00	00	0	0	0	IC-Ia	0	Ic	-IC	0	0
00	11	00	10	11	01	00	00	01	0	0	0	-Ia	0	Ic-IC	0	0	IC

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
00	11	00	10	00	01	00	11	01	0	0	0	-Ia	0	IB-Ia	0	0	-IB-Ib
00	11	00	10	00	00	10	11	01	0	0	0	-IB	0	0	IB-Ia	0	Ic
00	11	00	10	11	00	10	00	01	0	0	0	IC+Ib	0	0	Ic-IC	0	Ic
00	11	00	00	00	01	10	11	01	0	0	0	0	0	IB	-Ia	0	Ic-IB
00	11	00	00	11	01	10	00	01	0	0	0	0	0	-IC-Ib	-Ia	0	IC-Ia
employ four capacitors																	
10	00	01	10	00	00	10	11	00	Ic-IA	0	Ic	-IB	0	0	Ib-IC	0	0
10	00	01	10	11	00	10	00	00	Ic-IA	0	Ic	Ib-IB	0	0	-IC	0	0
10	11	01	10	00	00	10	00	00	-IA-Ia	0	Ic	-IB	0	0	-IC	0	0
10	00	01	10	00	00	00	11	01	IB-Ia	0	-IC-Ia	-IB	0	0	0	0	IC-Ib
10	00	01	10	11	00	00	00	01	IB+Ic	0	Ic-IC	Ib-IB	0	0	0	0	IC
10	11	01	10	00	00	00	00	01	IB-Ia	0	Ic-IC	-IB	0	0	0	0	IC
10	00	01	00	00	01	10	11	00	IC+Ic	0	Ic-IB	0	0	IB	Ib-IC	0	0
10	00	01	00	11	01	10	00	00	IC-Ia	0	-IB-Ia	0	0	IB-Ib	-IC	0	0
10	11	01	00	00	01	10	00	00	IC-Ia	0	Ic-IB	0	0	IB	-IC	0	0
10	00	01	00	00	01	00	11	01	-Ia	0	IA-Ia	0	0	IB	0	0	IC-Ib
10	00	01	00	11	01	00	00	01	-Ia	0	IA-Ia	0	0	IB-Ib	0	0	IC
10	11	01	00	00	01	00	00	01	-Ia	0	IA+Ic	0	0	IB	0	0	IC
10	00	00	10	00	01	10	11	00	-IA	0	0	Ic-IB	0	Ic	Ib-IC	0	0
10	00	00	10	11	01	10	00	00	-IA	0	0	-IB-Ia	0	Ic	-IC	0	0
10	11	00	10	00	01	10	00	00	Ib-IA	0	0	Ic-IB	0	Ic	-IC	0	0
10	00	00	10	00	01	00	11	01	-IA	0	0	IA-Ia	0	-IC-Ia	0	0	IC-Ib
10	00	00	10	11	01	00	00	01	-IA	0	0	IA-Ia	0	Ic-IC	0	0	IC
10	11	00	10	00	01	00	00	01	Ib-IA	0	0	IA+Ic	0	Ic-IC	0	0	IC
10	00	00	10	00	00	10	11	01	-IA	0	0	-IB	0	0	-IC-Ia	0	Ic
10	00	00	10	11	00	10	00	01	-IA	0	0	Ib-IB	0	0	Ic-IC	0	Ic
10	11	00	10	00	00	10	00	01	Ib-IA	0	0	-IB	0	0	Ic-IC	0	Ic
10	00	00	00	00	01	10	11	01	-IA	0	0	0	0	IB	IA-Ia	0	Ic-IB
10	00	00	00	11	01	10	00	01	-IA	0	0	0	0	IB-Ib	IA-Ia	0	-IB-Ia
10	11	00	00	00	01	10	00	01	Ib-IA	0	0	0	0	IB	IA+Ic	0	Ic-IB
00	00	01	10	00	01	10	11	00	0	0	IA	IC+Ic	0	Ic-IA	Ib-IC	0	0
00	00	01	10	11	01	10	00	00	0	0	IA	IC-Ia	0	Ic-IA	-IC	0	0
00	11	01	10	00	01	10	00	00	0	0	IA-Ib	IC-Ia	0	-IA-Ia	-IC	0	0
00	00	01	10	00	01	00	11	01	0	0	IA	-Ia	0	IB-Ia	0	0	IC-Ib
00	00	01	10	11	01	00	00	01	0	0	IA	-Ia	0	IB+Ic	0	0	IC
00	11	01	10	00	01	00	00	01	0	0	IA-Ib	-Ia	0	IB-Ia	0	0	IC
00	00	01	10	00	00	10	11	01	0	0	IA	-IB	0	0	IB-Ia	0	Ic-IA
00	00	01	10	11	00	10	00	01	0	0	IA	Ib-IB	0	0	IB+Ic	0	Ic-IA
00	11	01	10	00	00	10	00	01	0	0	IA-Ib	-IB	0	0	IB-Ia	0	-IA-Ia
00	00	01	00	00	01	10	11	01	0	0	IA	0	0	IB	-Ia	0	IC+Ic
00	00	01	00	11	01	10	00	01	0	0	IA	0	0	IB-Ib	-Ia	0	IC-Ia
00	11	01	00	00	01	10	00	01	0	0	IA-Ib	0	0	IB	-Ia	0	IC-Ia

Table B.51: Switching device combinations for (V_{AB},V_{BC},V_{CA}) = (0,0,0) and (V_{ab},V_{bc},V_{ca}) = ($-V_{cap}$,$+2V_{cap}$,$-Vcap$).

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
employ two capacitors																	
11	10	01	11	00	00	11	00	00	0	-Ib	Ic	0	0	0	0	0	0
11	10	00	11	00	01	11	00	00	0	-Ib	0	0	0	Ic	0	0	0
11	10	00	11	00	00	11	00	01	0	-Ib	0	0	0	0	0	0	Ic
11	00	01	11	10	00	11	00	00	0	0	Ic	0	-Ib	0	0	0	0
11	00	01	11	00	00	11	10	00	0	0	Ic	0	0	0	0	-Ib	0
11	00	00	11	10	01	11	00	00	0	0	0	0	-Ib	Ic	0	0	0
11	00	00	11	10	00	11	00	01	0	0	0	0	-Ib	0	0	0	Ic
11	00	00	11	00	01	11	10	00	0	0	0	0	0	Ic	0	-Ib	0
11	00	00	11	00	00	11	10	01	0	0	0	0	0	0	0	-Ib	Ic
employ three capacitors																	
00	10	01	11	10	00	11	00	00	0	Ic-IA	Ic	0	IA+Ia	0	0	0	0
11	10	01	00	10	00	11	00	00	0	IB-Ib	Ic	0	-IB	0	0	0	0
00	10	01	11	00	01	11	00	00	0	-Ib	IA-Ib	0	0	-IA-Ia	0	0	0
11	10	01	00	00	01	11	00	00	0	-Ib	Ic-IB	0	0	IB	0	0	0
00	10	01	11	00	00	11	10	00	0	Ic-IA	Ic	0	0	0	0	IA+Ia	0
11	10	01	11	00	00	00	10	00	0	IC-Ib	Ic	0	0	0	0	-IC	0
00	10	01	11	00	00	11	00	01	0	-Ib	IA-Ib	0	0	0	0	0	-IA-Ia
11	10	01	11	00	00	00	00	01	0	-Ib	Ic-IC	0	0	0	0	0	IC
00	10	00	11	10	01	11	00	00	0	-IA	0	0	IA-Ib	Ic	0	0	0
11	10	00	00	10	01	11	00	00	0	IB+Ia	0	0	Ic-IB	Ic	0	0	0
00	10	00	11	10	00	11	00	01	0	-IA	0	0	IA-Ib	0	0	0	Ic
11	10	00	00	10	00	11	00	01	0	IB-Ib	0	0	-IB	0	0	0	Ic
00	10	00	11	00	01	11	10	00	0	-IA	0	0	0	Ic	0	IA-Ib	0
11	10	00	11	00	01	00	10	00	0	IC-Ib	0	0	0	Ic	0	-IC	0
11	10	00	00	00	01	11	00	01	0	-Ib	0	0	0	IB	0	0	Ic-IB
11	10	00	11	00	01	00	00	01	0	-Ib	0	0	0	Ic-IC	0	0	IC
00	10	00	11	00	00	11	10	01	0	-IA	0	0	0	0	0	IA-Ib	Ic
11	10	00	11	00	00	00	10	01	0	IC+Ia	0	0	0	0	0	Ic-IC	Ic
00	00	01	11	10	01	11	00	00	0	0	IA	0	-Ib	Ic-IA	0	0	0
11	00	01	00	10	01	11	00	00	0	0	-IB-Ia	0	-Ib	IB-Ib	0	0	0
11	00	01	00	10	00	11	10	00	0	0	Ic	0	-IB	0	0	IB-Ib	0
11	00	01	11	10	00	00	10	00	0	0	Ic	0	IC-Ib	0	0	-IC	0
00	00	01	11	10	00	11	00	01	0	0	IA	0	-Ib	0	0	0	Ic-IA
11	00	01	11	10	00	00	00	01	0	0	Ic-IC	0	-Ib	0	0	0	IC
00	00	01	11	00	01	11	10	00	0	0	IA	0	0	Ic-IA	0	-Ib	0
11	00	01	00	00	01	11	10	00	0	0	Ic-IB	0	0	IB	0	-Ib	0
00	00	01	11	00	00	11	10	01	0	0	IA	0	0	0	0	-Ib	Ic-IA
11	00	01	11	00	00	00	10	01	0	0	-IC-Ia	0	0	0	0	-Ib	IC-Ib
11	00	00	00	10	01	11	10	00	0	0	0	0	Ic-IB	Ic	0	IB+Ia	0
11	00	00	11	10	01	00	10	00	0	0	0	0	IC-Ib	Ic	0	-IC	0
11	00	00	00	10	01	11	00	01	0	0	0	0	-Ib	IB-Ib	0	0	-IB-Ia

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
11	00	00	11	10	01	00	00	01	0	0	0	0	-Ib	Ic-IC	0	0	IC
11	00	00	00	10	00	11	10	01	0	0	0	0	-IB	0	0	IB-Ib	Ic
11	00	00	11	10	00	00	10	01	0	0	0	0	IC+Ia	0	0	Ic-IC	Ic
11	00	00	00	00	01	11	10	01	0	0	0	0	0	IB	0	-Ib	Ic-IB
11	00	00	11	00	01	00	10	01	0	0	0	0	0	-IC-Ia	0	-Ib	IC-Ib
employ four capacitors																	
00	10	01	00	10	00	11	10	00	0	Ic-IA	Ic	0	-IB	0	0	Ia-IC	0
00	10	01	11	10	00	00	10	00	0	Ic-IA	Ic	0	Ia-IB	0	0	-IC	0
11	10	01	00	10	00	00	10	00	0	-IA-Ib	Ic	0	-IB	0	0	-IC	0
00	10	01	00	10	00	11	00	01	0	IB-Ib	-IC-Ib	0	-IB	0	0	0	IC-Ia
00	10	01	11	10	00	00	00	01	0	IB+Ic	Ic-IC	0	Ia-IB	0	0	0	IC
11	10	01	00	10	00	00	00	01	0	IB-Ib	Ic-IC	0	-IB	0	0	0	IC
00	10	01	00	00	01	11	10	00	0	IC+Ic	Ic-IB	0	0	IB	0	Ia-IC	0
00	10	01	11	00	01	00	10	00	0	IC-Ib	-IB-Ib	0	0	IB-Ia	0	-IC	0
11	10	01	00	00	01	00	10	00	0	IC-Ib	Ic-IB	0	0	IB	0	-IC	0
00	10	01	00	00	01	11	00	01	0	-Ib	IA-Ib	0	0	IB	0	0	IC-Ia
00	10	01	11	00	01	00	00	01	0	-Ib	IA-Ib	0	0	IB-Ia	0	0	IC
11	10	01	00	00	01	00	00	01	0	-Ib	IA+Ic	0	0	IB	0	0	IC
00	10	00	00	10	01	11	10	00	0	-IA	0	0	Ic-IB	Ic	0	Ia-IC	0
00	10	00	11	10	01	00	10	00	0	-IA	0	0	-IB-Ib	Ic	0	-IC	0
11	10	00	00	10	01	00	10	00	0	Ia-IA	0	0	Ic-IB	Ic	0	-IC	0
00	10	00	00	10	01	11	00	01	0	-IA	0	0	IA-Ib	-IC-Ib	0	0	IC-Ia
00	10	00	11	10	01	00	00	01	0	-IA	0	0	IA-Ib	Ic-IC	0	0	IC
11	10	00	00	10	01	00	00	01	0	Ia-IA	0	0	IA+Ic	Ic-IC	0	0	IC
00	10	00	00	10	00	11	10	01	0	-IA	0	0	-IB	0	0	-IC-Ib	Ic
00	10	00	11	10	00	00	10	01	0	-IA	0	0	Ia-IB	0	0	Ic-IC	Ic
11	10	00	00	10	00	00	10	01	0	Ia-IA	0	0	-IB	0	0	Ic-IC	Ic
00	10	00	00	00	01	11	10	01	0	-IA	0	0	0	IB	0	IA-Ib	Ic-IB
00	10	00	11	00	01	00	10	01	0	-IA	0	0	0	IB-Ia	0	IA-Ib	-IB-Ib
11	10	00	00	00	01	00	10	01	0	Ia-IA	0	0	0	IB	0	IA+Ic	Ic-IB
00	00	01	00	10	01	11	10	00	0	0	IA	0	IC+Ic	Ic-IA	0	Ia-IC	0
00	00	01	11	10	01	00	10	00	0	0	IA	0	IC-Ib	Ic-IA	0	-IC	0
11	00	01	00	10	01	00	10	00	0	0	IA-Ia	0	IC-Ib	-IA-Ib	0	-IC	0
00	00	01	00	10	01	11	00	01	0	0	IA	0	-Ib	IB-Ib	0	0	IC-Ia
00	00	01	11	10	01	00	00	01	0	0	IA	0	-Ib	IB+Ic	0	0	IC
11	00	01	00	10	01	00	00	01	0	0	IA-Ia	0	-Ib	IB-Ib	0	0	IC
00	00	01	00	10	00	11	10	01	0	0	IA	0	-IB	0	0	IB-Ib	Ic-IA
00	00	01	11	10	00	00	10	01	0	0	IA	0	Ia-IB	0	0	IB+Ic	Ic-IA
11	00	01	00	10	00	00	10	01	0	0	IA-Ia	0	-IB	0	0	IB-Ib	-IA-Ib
00	00	01	00	00	01	11	10	01	0	0	IA	0	0	IB	0	-Ib	IC+Ic
00	00	01	11	00	01	00	10	01	0	0	IA	0	0	IB-Ia	0	-Ib	IC-Ib
11	00	01	00	00	01	00	10	01	0	0	IA-Ia	0	0	IB	0	-Ib	IC-Ib

Table B.52: Switching device combinations for (V_{AB},V_{BC},V_{CA}) = (0,0,0) and (V_{ab},V_{bc},V_{ca}) = ($-2V_{cap}$,$+V_{cap}$,$+V_{cap}$).

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
employ two capacitors																	
01	10	11	00	00	11	00	00	11	Ia	-Ib	0	0	0	0	0	0	0
01	00	11	00	10	11	00	00	11	Ia	0	0	0	-Ib	0	0	0	0
01	00	11	00	00	11	00	10	11	Ia	0	0	0	0	0	0	-Ib	0
00	10	11	01	00	11	00	00	11	0	-Ib	0	Ia	0	0	0	0	0
00	00	11	01	10	11	00	00	11	0	0	0	Ia	-Ib	0	0	0	0
00	00	11	01	00	11	00	10	11	0	0	0	Ia	0	0	0	-Ib	0
00	10	11	00	00	11	01	00	11	0	-Ib	0	0	0	0	Ia	0	0
00	00	11	00	10	11	01	00	11	0	0	0	0	-Ib	0	Ia	0	0
00	00	11	00	00	11	01	10	11	0	0	0	0	0	0	Ia	-Ib	0
employ three capacitors																	
01	10	00	01	00	11	00	00	11	IA-Ib	-Ib	0	-IA-Ic	0	0	0	0	0
01	10	11	01	00	00	00	00	11	Ia-IB	-Ib	0	IB	0	0	0	0	0
01	10	00	00	10	11	00	00	11	Ia	Ia-IA	0	0	IA+Ic	0	0	0	0
01	10	11	00	10	00	00	00	11	Ia	IB-Ib	0	0	-IB	0	0	0	0
01	10	00	00	00	11	01	00	11	IA-Ib	-Ib	0	0	0	0	-IA-Ic	0	0
01	10	11	00	00	11	01	00	00	Ia-IC	-Ib	0	0	0	0	IC	0	0
01	10	00	00	00	11	00	10	11	Ia	Ia-IA	0	0	0	0	0	IA+Ic	0
01	10	11	00	00	11	00	10	00	Ia	IC-Ib	0	0	0	0	0	-IC	0
01	00	00	01	10	11	00	00	11	IA	0	0	Ia-IA	-Ib	0	0	0	0
01	00	11	01	10	00	00	00	11	-IB-Ic	0	0	IB-Ib	-Ib	0	0	0	0
01	00	00	01	00	11	00	10	11	IA	0	0	Ia-IA	0	0	0	-Ib	0
01	00	11	01	00	00	00	10	11	Ia-IB	0	0	IB	0	0	0	-Ib	0
01	00	00	00	10	11	01	00	11	IA	0	0	0	-Ib	0	Ia-IA	0	0
01	00	11	00	10	11	01	00	00	Ia-IC	0	0	0	-Ib	0	IC	0	0
01	00	11	00	10	00	00	10	11	Ia	0	0	0	-IB	0	0	IB-Ib	0
01	00	11	00	10	11	00	10	00	Ia	0	0	0	IC-Ib	0	0	-IC	0
01	00	00	00	00	11	01	10	11	IA	0	0	0	0	0	Ia-IA	-Ib	0
01	00	11	00	00	11	01	10	00	-IC-Ic	0	0	0	0	0	IC-Ib	-Ib	0
00	10	00	01	10	11	00	00	11	0	-IA	0	Ia	IA-Ib	0	0	0	0
00	10	11	01	10	00	00	00	11	0	IB+Ic	0	Ia	Ia-IB	0	0	0	0
00	10	11	01	00	00	01	00	11	0	-Ib	0	IB	0	0	Ia-IB	0	0
00	10	11	01	00	11	01	00	00	0	-Ib	0	Ia-IC	0	0	IC	0	0
00	10	00	01	00	11	00	10	11	0	-IA	0	Ia	0	0	0	IA-Ib	0
00	10	11	01	00	11	00	10	00	0	IC-Ib	0	Ia	0	0	0	-IC	0
00	10	00	00	10	11	01	00	11	0	-IA	0	0	IA-Ib	0	Ia	0	0
00	10	11	00	10	00	01	00	11	0	IB-Ib	0	0	-IB	0	Ia	0	0
00	10	00	00	00	11	01	10	11	0	-IA	0	0	0	0	Ia	IA-Ib	0
00	00	11	01	10	00	01	00	11	0	0	0	IB-Ib	-Ib	0	-IB-Ic	0	0
00	00	11	01	10	11	01	00	00	0	0	0	Ia-IC	-Ib	0	IC	0	0
00	00	11	01	10	00	00	10	11	0	0	0	Ia	Ia-IB	0	0	IB+Ic	0
00	00	11	01	10	11	00	10	00	0	0	0	Ia	IC-Ib	0	0	-IC	0

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
00	00	11	01	00	00	01	10	11	0	0	0	IB	0	0	Ia-IB	-Ib	0
00	00	11	01	00	11	01	10	00	0	0	0	-IC-Ic	0	0	IC-Ib	-Ib	0
00	00	11	00	10	00	01	10	11	0	0	0	0	-IB	0	Ia	IB-Ib	0
00	00	11	00	10	11	01	10	00	0	0	0	0	IC+Ic	0	Ia	Ia-IC	0
employ four capacitors																	
01	10	00	01	00	00	01	00	11	IA-Ib	-Ib	0	IB	0	0	IC-Ic	0	0
01	10	00	01	00	11	01	00	00	IA-Ib	-Ib	0	IB-Ic	0	0	IC	0	0
01	10	11	01	00	00	01	00	00	IA+Ia	-Ib	0	IB	0	0	IC	0	0
01	10	00	01	00	00	00	10	11	Ia-IB	IC+Ia	0	IB	0	0	0	Ic-IC	0
01	10	00	01	00	11	00	10	00	-IB-Ib	IC-Ib	0	IB-Ic	0	0	0	-IC	0
01	10	11	01	00	00	00	10	00	Ia-IB	IC-Ib	0	IB	0	0	0	-IC	0
01	10	00	00	10	00	01	00	11	-IC-Ib	IB-Ib	0	0	-IB	0	IC-Ic	0	0
01	10	00	00	10	11	01	00	00	Ia-IC	IB+Ia	0	0	Ic-IB	0	IC	0	0
01	10	11	00	10	00	01	00	00	Ia-IC	IB-Ib	0	0	-IB	0	IC	0	0
01	10	00	00	10	00	00	10	11	Ia	Ia-IA	0	0	-IB	0	0	Ic-IC	0
01	10	00	00	10	11	00	10	00	Ia	Ia-IA	0	0	Ic-IB	0	0	-IC	0
01	10	11	00	10	00	00	10	00	Ia	-IA-Ib	0	0	-IB	0	0	-IC	0
01	00	00	01	10	00	01	00	11	IA	0	0	IB-Ib	-Ib	0	IC-Ic	0	0
01	00	00	01	10	11	01	00	00	IA	0	0	IB+Ia	-Ib	0	IC	0	0
01	00	11	01	10	00	01	00	00	IA-Ic	0	0	IB-Ib	-Ib	0	IC	0	0
01	00	00	01	10	00	00	10	11	IA	0	0	Ia-IA	IC+Ia	0	0	Ic-IC	0
01	00	00	01	10	11	00	10	00	IA	0	0	Ia-IA	IC-Ib	0	0	-IC	0
01	00	11	01	10	00	00	10	00	IA-Ic	0	0	-IA-Ib	IC-Ib	0	0	-IC	0
01	00	00	01	00	00	01	10	11	IA	0	0	IB	0	0	IC+Ia	-Ib	0
01	00	00	01	00	11	01	10	00	IA	0	0	IB-Ic	0	0	IC-Ib	-Ib	0
01	00	11	01	00	00	01	10	00	IA-Ic	0	0	IB	0	0	IC-Ib	-Ib	0
01	00	00	00	10	00	01	10	11	IA	0	0	0	-IB	0	Ia-IA	IB-Ib	0
01	00	00	00	10	11	01	10	00	IA	0	0	0	Ic-IB	0	Ia-IA	IB+Ia	0
01	00	11	00	10	00	01	10	00	IA-Ic	0	0	0	-IB	0	-IA-Ib	IB-Ib	0
00	10	00	01	10	00	01	00	11	0	-IA	0	-IC-Ib	IA-Ib	0	IC-Ic	0	0
00	10	00	01	10	11	01	00	00	0	-IA	0	Ia-IC	IA-Ib	0	IC	0	0
00	10	11	01	10	00	01	00	00	0	Ic-IA	0	Ia-IC	IA+Ia	0	IC	0	0
00	10	00	01	10	00	00	10	11	0	-IA	0	Ia	Ia-IB	0	0	Ic-IC	0
00	10	00	01	10	11	00	10	00	0	-IA	0	Ia	-IB-Ib	0	0	-IC	0
00	10	11	01	10	00	00	10	00	0	Ic-IA	0	Ia	Ia-IB	0	0	-IC	0
00	10	00	01	00	00	01	10	11	0	-IA	0	IB	0	0	Ia-IB	IA-Ib	0
00	10	00	01	00	11	01	10	00	0	-IA	0	IB-Ic	0	0	-IB-Ib	IA-Ib	0
00	10	11	01	00	00	01	10	00	0	Ic-IA	0	IB	0	0	Ia-IB	IA+Ia	0
00	10	00	00	10	00	01	10	11	0	-IA	0	0	-IB	0	Ia	-IC-Ib	0
00	10	00	00	10	11	01	10	00	0	-IA	0	0	Ic-IB	0	Ia	Ia-IC	0
00	10	11	00	10	00	01	10	00	0	Ic-IA	0	0	-IB	0	Ia	Ia-IC	0
00	10	11	00	00	11	01	10	00	0	IC+Ic	0	0	0	0	Ia	Ia-IC	0

Table B.53: Switching device combinations for (V_{AB},V_{BC},V_{CA}) = (0,0,0) and (V_{ab},V_{bc},V_{ca}) = ($-V_{cap}$,$-V_{cap}$,$+2V_{cap}$).

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
employ two capacitors																	
01	11	10	00	11	00	00	11	00	Ia	0	-Ic	0	0	0	0	0	0
01	11	00	00	11	10	00	11	00	Ia	0	0	0	0	-Ic	0	0	0
01	11	00	00	11	00	00	11	10	Ia	0	0	0	0	0	0	0	-Ic
00	11	10	01	11	00	00	11	00	0	0	-Ic	Ia	0	0	0	0	0
00	11	10	00	11	00	01	11	00	0	0	-Ic	0	0	0	Ia	0	0
00	11	00	01	11	10	00	11	00	0	0	0	Ia	0	-Ic	0	0	0
00	11	00	01	11	00	00	11	10	0	0	0	Ia	0	0	0	0	-Ic
00	11	00	00	11	10	01	11	00	0	0	0	0	0	-Ic	Ia	0	0
00	11	00	00	11	00	01	11	10	0	0	0	0	0	0	Ia	0	-Ic
employ three capacitors																	
01	00	10	01	11	00	00	11	00	IA-Ic	0	-Ic	-IA-Ib	0	0	0	0	0
01	11	10	01	00	00	00	11	00	Ia-IB	0	-Ic	IB	0	0	0	0	0
01	00	10	00	11	10	00	11	00	Ia	0	Ia-IA	0	0	IA+Ib	0	0	0
01	11	10	00	00	10	00	11	00	Ia	0	IB-Ic	0	0	-IB	0	0	0
01	00	10	00	11	00	01	11	00	IA-Ic	0	-Ic	0	0	0	-IA-Ib	0	0
01	11	10	00	11	00	01	00	00	Ia-IC	0	-Ic	0	0	0	IC	0	0
01	00	10	00	11	00	00	11	10	Ia	0	Ia-IA	0	0	0	0	0	IA+Ib
01	11	10	01	00	00	00	00	10	Ia-IB	0	IC-Ic	-IB	0	0	0	0	-IC
01	11	10	00	11	00	00	00	10	Ia	0	IC-Ic	0	0	0	0	0	-IC
01	00	00	01	11	10	00	11	00	IA	0	0	Ia-IA	0	-Ic	0	0	0
01	11	00	01	00	10	00	11	00	-IB-Ib	0	0	IB-Ic	0	-Ic	0	0	0
01	00	00	01	11	00	00	11	10	IA	0	0	Ia-IA	0	0	0	0	-Ic
01	11	00	01	00	00	00	11	10	Ia-IB	0	0	IB	0	0	0	0	-Ic
01	00	00	00	11	10	01	11	00	IA	0	0	0	0	-Ic	Ia-IA	0	0
01	11	00	00	11	10	01	00	00	Ia-IC	0	0	0	0	-Ic	IC	0	0
01	11	00	00	00	10	00	11	10	Ia	0	0	0	0	-IB	0	0	IB-Ic
01	11	00	00	11	10	00	00	10	Ia	0	0	0	0	IC-Ic	0	0	-IC
01	00	00	00	11	00	01	11	10	IA	0	0	0	0	0	Ia-IA	0	-Ic
01	11	00	00	11	00	01	00	10	-IC-Ib	0	0	0	0	0	IC-Ic	0	-Ic
00	00	10	01	11	10	00	11	00	0	0	-IA	Ia	0	IA-Ic	0	0	0
00	11	10	01	00	10	00	11	00	0	0	IB+Ib	Ia	0	Ia-IB	0	0	0
00	11	10	01	00	00	01	11	00	0	0	-Ic	IB	0	0	Ia-IB	0	0
00	11	10	01	11	00	01	00	00	0	0	-Ic	Ia-IC	0	0	IC	0	0
00	00	10	01	11	00	00	11	10	0	0	-IA	Ia	0	0	0	0	IA-Ic
00	11	10	01	11	00	00	00	10	0	0	IC-Ic	Ia	0	0	0	0	-IC
00	00	10	00	11	10	01	11	00	0	0	-IA	0	0	IA-Ic	Ia	0	0
00	11	10	00	00	10	01	11	00	0	0	IB-Ic	0	0	-IB	Ia	0	0
00	00	10	00	11	00	01	11	10	0	0	-IA	0	0	0	Ia	0	IA-Ic
00	11	10	00	11	00	01	00	10	0	0	IC+Ib	0	0	0	Ia	0	Ia-IC
00	11	00	01	00	10	01	11	00	0	0	0	IB-Ic	0	-Ic	-IB-Ib	0	0
00	11	00	01	11	10	01	00	00	0	0	0	Ia-IC	0	-Ic	IC	0	0

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
00	11	00	01	00	10	00	11	10	0	0	0	Ia	0	Ia-IB	0	0	IB+Ib
00	11	00	01	11	10	00	00	10	0	0	0	Ia	0	IC-Ic	0	0	-IC
00	11	00	01	00	00	01	11	10	0	0	0	IB	0	0	Ia-IB	0	-Ic
00	11	00	01	11	00	01	00	10	0	0	0	-IC-Ib	0	0	IC-Ic	0	-Ic
00	11	00	00	00	10	01	11	10	0	0	0	0	0	-IB	Ia	0	IB-Ic
00	11	00	00	11	10	01	00	10	0	0	0	0	0	IC+Ib	Ia	0	Ia-IC
employ four capacitors																	
01	00	10	01	00	00	01	11	00	IA-Ic	0	-Ic	IB	0	0	IC-Ib	0	0
01	00	10	01	11	00	01	00	00	IA-Ic	0	-Ic	IB-Ib	0	0	IC	0	0
01	11	10	01	00	00	01	00	00	IA+Ia	0	-Ic	IB	0	0	IC	0	0
01	00	10	01	00	00	00	11	10	Ia-IB	0	IC+Ia	IB	0	0	0	0	Ib-IC
01	00	10	01	11	00	00	00	10	-IB-Ic	0	IC-Ic	IB-Ib	0	0	0	0	-IC
01	00	10	00	00	10	01	11	00	-IC-Ic	0	IB-Ic	0	0	-IB	IC-Ib	0	0
01	00	10	00	11	10	01	00	00	Ia-IC	0	IB+Ia	0	0	Ib-IB	IC	0	0
01	11	10	00	00	10	01	00	00	Ia-IC	0	IB-Ic	0	0	-IB	IC	0	0
01	00	10	00	00	10	00	11	10	Ia	0	Ia-IA	0	0	-IB	0	0	Ib-IC
01	00	10	00	11	10	00	00	10	Ia	0	Ia-IA	0	0	Ib-IB	0	0	-IC
01	11	10	00	00	10	00	00	10	Ia	0	-IA-Ic	0	0	-IB	0	0	-IC
01	00	00	01	00	10	01	11	00	IA	0	0	IB-Ic	0	-Ic	IC-Ib	0	0
01	00	00	01	11	10	01	00	00	IA	0	0	IB+Ia	0	-Ic	IC	0	0
01	11	00	01	00	10	01	00	00	IA-Ib	0	0	IB-Ic	0	-Ic	IC	0	0
01	00	00	01	00	10	00	11	10	IA	0	0	Ia-IA	0	IC+Ia	0	0	Ib-IC
01	00	00	01	11	10	00	00	10	IA	0	0	Ia-IA	0	IC-Ic	0	0	-IC
01	11	00	01	00	10	00	00	10	IA-Ib	0	0	-IA-Ic	0	IC-Ic	0	0	-IC
01	00	00	01	00	00	01	11	10	IA	0	0	IB	0	0	IC+Ia	0	-Ic
01	00	00	01	11	00	01	00	10	IA	0	0	IB-Ib	0	0	IC-Ic	0	-Ic
01	11	00	01	00	00	01	00	10	IA-Ib	0	0	IB	0	0	IC-Ic	0	-Ic
01	00	00	00	00	10	01	11	10	IA	0	0	0	0	-IB	Ia-IA	0	IB-Ic
01	00	00	00	11	10	01	00	10	IA	0	0	0	0	Ib-IB	Ia-IA	0	IB+Ia
01	11	00	00	00	10	01	00	10	IA-Ib	0	0	0	0	-IB	-IA-Ic	0	IB-Ic
00	00	10	01	00	10	01	11	00	0	0	-IA	-IC-Ic	0	IA-Ic	IC-Ib	0	0
00	00	10	01	11	10	01	00	00	0	0	-IA	Ia-IC	0	IA-Ic	IC	0	0
00	11	10	01	00	10	01	00	00	0	0	Ib-IA	Ia-IC	0	IA+Ia	IC	0	0
00	00	10	01	00	10	00	11	10	0	0	-IA	Ia	0	Ia-IB	0	0	Ib-IC
00	00	10	01	11	10	00	00	10	0	0	-IA	Ia	0	-IB-Ic	0	0	-IC
00	11	10	01	00	10	00	00	10	0	0	Ib-IA	Ia	0	Ia-IB	0	0	-IC
00	00	10	01	00	00	01	11	10	0	0	-IA	IB	0	0	Ia-IB	0	IA-Ic
00	00	10	01	11	00	01	00	10	0	0	-IA	IB-Ib	0	0	-IB-Ic	0	IA-Ic
00	11	10	01	00	00	01	00	10	0	0	Ib-IA	IB	0	0	Ia-IB	0	IA+Ia
00	00	10	00	00	10	01	11	10	0	0	-IA	0	0	-IB	Ia	0	-IC-Ic
00	00	10	00	11	10	01	00	10	0	0	-IA	0	0	Ib-IB	Ia	0	Ia-IC
00	11	10	00	00	10	01	00	10	0	0	Ib-IA	0	0	-IB	Ia	0	Ia-IC

Table B.54: Switching device combinations for (V_{AB},V_{BC},V_{CA}) = (0,0,0) and (V_{ab},V_{bc},V_{ca}) = ($+V_{cap}$,$-2V_{cap}$,$+V_{cap}$).

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
employ two capacitors																	
11	01	10	11	00	00	11	00	00	0	Ib	-Ic	0	0	0	0	0	0
11	01	00	11	00	10	11	00	00	0	Ib	0	0	0	-Ic	0	0	0
11	01	00	11	00	00	11	00	10	0	Ib	0	0	0	0	0	0	-Ic
11	00	10	11	01	00	11	00	00	0	0	-Ic	0	Ib	0	0	0	0
11	00	10	11	00	00	11	01	00	0	0	-Ic	0	0	0	0	Ib	0
11	00	00	11	01	10	11	00	00	0	0	0	0	Ib	-Ic	0	0	0
11	00	00	11	01	00	11	00	10	0	0	0	0	Ib	0	0	0	-Ic
11	00	00	11	00	10	11	01	00	0	0	0	0	0	-Ic	0	Ib	0
11	00	00	11	00	00	11	01	10	0	0	0	0	0	0	0	Ib	-Ic
employ three capacitors																	
00	01	10	11	01	00	11	00	00	0	IA-Ic	-Ic	0	-IA-Ia	0	0	0	0
11	01	10	00	01	00	11	00	00	0	Ib-IB	-Ic	0	IB	0	0	0	0
00	01	10	11	00	10	11	00	00	0	Ib	Ib-IA	0	0	IA+Ia	0	0	0
11	01	10	00	00	10	11	00	00	0	Ib	IB-Ic	0	0	-IB	0	0	0
00	01	10	11	00	00	11	01	00	0	IA-Ic	-Ic	0	0	0	0	-IA-Ia	0
11	01	10	11	00	00	00	01	00	0	Ib-IC	-Ic	0	0	0	0	IC	0
00	01	10	11	00	00	11	00	10	0	Ib	Ib-IA	0	0	0	0	0	IA+Ia
11	01	10	11	00	00	00	00	10	0	Ib	IC-Ic	0	0	0	0	0	-IC
00	01	00	11	01	10	11	00	00	0	IA	0	0	Ib-IA	-Ic	0	0	0
11	01	00	00	01	10	11	00	00	0	-IB-Ia	0	0	IB-Ic	-Ic	0	0	0
00	01	00	11	01	00	11	00	10	0	IA	0	0	Ib-IA	0	0	0	-Ic
11	01	00	00	01	00	11	00	10	0	Ib-IB	0	0	IB	0	0	0	-Ic
00	01	00	11	00	10	11	01	00	0	IA	0	0	0	-Ic	0	Ib-IA	0
11	01	00	11	00	10	00	01	00	0	Ib-IC	0	0	0	-Ic	0	IC	0
11	01	00	00	00	10	11	00	10	0	Ib	0	0	0	-IB	0	0	IB-Ic
11	01	00	11	00	10	00	00	10	0	Ib	0	0	0	IC-Ic	0	0	-IC
00	01	00	11	00	00	11	01	10	0	IA	0	0	0	0	0	Ib-IA	-Ic
11	01	00	11	00	00	00	01	10	0	-IC-Ia	0	0	0	0	0	IC-Ic	-Ic
00	00	10	11	01	10	11	00	00	0	0	-IA	0	Ib	IA-Ic	0	0	0
11	00	10	00	01	10	11	00	00	0	0	IB+Ia	0	Ib	Ib-IB	0	0	0
11	00	10	00	01	00	11	01	00	0	0	-Ic	0	IB	0	0	Ib-IB	0
11	00	10	11	01	00	00	01	00	0	0	-Ic	0	Ib-IC	0	0	IC	0
00	00	10	11	01	00	11	00	10	0	0	-IA	0	Ib	0	0	0	IA-Ic
11	00	10	11	01	00	00	00	10	0	0	IC-Ic	0	Ib	0	0	0	-IC
00	00	10	11	00	10	11	01	00	0	0	-IA	0	0	IA-Ic	0	Ib	0
11	00	10	00	00	10	11	01	00	0	0	IB-Ic	0	0	-IB	0	Ib	0
00	00	10	11	00	00	11	01	10	0	0	-IA	0	0	0	0	Ib	IA-Ic
11	00	10	11	00	00	00	01	10	0	0	IC+Ia	0	0	0	0	Ib	Ib-IC
11	00	00	00	01	10	11	01	00	0	0	0	0	IB-Ic	-Ic	0	-IB-Ia	0
11	00	00	11	01	10	00	01	00	0	0	0	0	Ib-IC	-Ic	0	IC	0
11	00	00	00	01	10	11	00	10	0	0	0	0	Ib	Ib-IB	0	0	IB+Ia

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
11	00	00	11	01	10	00	00	10	0	0	0	0	Ib	IC-Ic	0	0	-IC
11	00	00	00	01	00	11	01	10	0	0	0	0	IB	0	0	Ib-IB	-Ic
11	00	00	11	01	00	00	01	10	0	0	0	0	-IC-Ia	0	0	IC-Ic	-Ic
11	00	00	00	00	10	11	01	10	0	0	0	0	0	-IB	0	Ib	IB-Ic
11	00	00	11	00	10	00	01	10	0	0	0	0	0	IC+Ia	0	Ib	Ib-IC
employ four capacitors																	
00	01	10	00	01	00	11	01	00	0	IA-Ic	-Ic	0	IB	0	0	IC-Ia	0
00	01	10	01	01	00	00	01	00	0	IA-Ic	-Ic	0	IB-Ia	0	0	IC	0
11	01	10	00	01	00	00	01	00	0	IA+Ib	-Ic	0	IB	0	0	IC	0
00	01	10	00	01	00	11	00	10	0	Ib-IB	IC+Ib	0	IB	0	0	0	Ia-IC
00	01	10	11	01	00	00	00	10	0	-IB-Ic	IC-Ic	0	IB-Ia	0	0	0	-IC
11	01	10	00	01	00	00	00	10	0	Ib-IB	IC-Ic	0	IB	0	0	0	-IC
00	01	10	00	00	10	11	01	00	0	-IC-Ic	IB-Ic	0	0	-IB	0	IC-Ia	0
00	01	10	11	00	10	00	01	00	0	Ib-IC	IB+Ib	0	0	Ia-IB	0	IC	0
11	01	10	00	00	10	00	01	00	0	Ib-IC	IB-Ic	0	0	-IB	0	IC	0
00	01	10	00	00	10	11	00	10	0	Ib	Ib-IA	0	0	-IB	0	0	Ia-IC
00	01	10	11	00	10	00	00	10	0	Ib	Ib-IA	0	0	Ia-IB	0	0	-IC
11	01	10	00	00	10	00	00	10	0	Ib	-IA-Ic	0	0	-IB	0	0	-IC
00	01	00	00	01	10	11	01	00	0	IA	0	0	IB-Ic	-Ic	0	IC-Ia	0
00	01	00	11	01	10	00	01	00	0	IA	0	0	IB+Ib	-Ic	0	IC	0
11	01	00	00	01	10	00	01	00	0	IA-Ia	0	0	IB-Ic	-Ic	0	IC	0
00	01	00	00	01	10	11	00	10	0	IA	0	0	Ib-IA	IC+Ib	0	0	Ia-IC
00	01	00	11	01	10	00	00	10	0	IA	0	0	Ib-IA	IC-Ic	0	0	-IC
11	01	00	00	01	10	00	00	10	0	IA-Ia	0	0	-IA-Ic	IC-Ic	0	0	-IC
00	01	00	00	01	00	11	01	10	0	IA	0	0	IB	0	0	IC+Ib	-Ic
00	01	00	11	01	00	00	01	10	0	IA	0	0	IB-Ia	0	0	IC-Ic	-Ic
11	01	00	00	01	00	00	01	10	0	IA-Ia	0	0	IB	0	0	IC-Ic	-Ic
00	01	00	00	00	10	11	01	10	0	IA	0	0	0	-IB	0	Ib-IA	IB-Ic
00	01	00	11	00	10	00	01	10	0	IA	0	0	0	Ia-IB	0	Ib-IA	IB+Ib
11	01	00	00	00	10	00	01	10	0	IA-Ia	0	0	0	-IB	0	-IA-Ic	IB-Ic
00	00	10	00	01	10	11	01	00	0	0	-IA	0	-IC-Ic	IA-Ic	0	IC-Ia	0
00	00	10	11	01	10	00	01	00	0	0	-IA	0	Ib-IC	IA-Ic	0	IC	0
11	00	10	00	01	10	00	01	00	0	0	Ia-IA	0	Ib-IC	IA+Ib	0	IC	0
00	00	10	00	01	10	11	00	10	0	0	-IA	0	Ib	Ib-IB	0	0	Ia-IC
00	00	10	11	01	10	00	00	10	0	0	-IA	0	Ib	-IB-Ic	0	0	-IC
11	00	10	00	01	10	00	00	10	0	0	Ia-IA	0	Ib	Ib-IB	0	0	-IC
00	00	10	00	01	00	11	01	10	0	0	-IA	0	IB	0	0	Ib-IB	IA-Ic
00	00	10	11	01	00	00	01	10	0	0	-IA	0	IB-Ia	0	0	-IB-Ic	IA-Ic
11	00	10	00	01	00	00	01	10	0	0	Ia-IA	0	IB	0	0	Ib-IB	IA+Ib
00	00	10	00	00	10	11	01	10	0	0	-IA	0	0	-IB	0	Ib	-IC-Ic
00	00	10	11	00	10	00	01	10	0	0	-IA	0	0	Ia-IB	0	Ib	Ib-IC
11	00	10	00	00	10	00	01	10	0	0	Ia-IA	0	0	-IB	0	Ib	Ib-IC

Table B.55: Switching device combinations for (V_{AB},V_{BC},V_{CA}) = (0,0,0) and (V_{ab},V_{bc},V_{ca}) = ($+2V_{cap}$,0,$-2V_{cap}$).

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
employ five capacitors																	
10	01	01	10	00	00	10	00	00	-IA-Ia	Ib	Ic	-IB	0	0	-IC	0	0
10	01	01	10	00	00	00	01	00	IB-Ia	Ib-IC	Ic	-IB	0	0	0	IC	0
10	01	01	10	00	00	00	00	01	IB-Ia	Ib	Ic-IC	-IB	0	0	0	0	IC
10	01	01	00	01	00	10	00	00	IC-Ia	Ib-IB	Ic	0	IB	0	-IC	0	0
10	01	01	00	01	00	00	01	00	-Ia	IA+Ib	Ic	0	IB	0	0	IC	0
10	01	01	00	01	00	00	00	01	-Ia	Ib-IB	Ic-IC	0	IB	0	0	0	IC
10	01	01	00	00	01	10	00	00	IC-Ia	Ib	Ic-IB	0	0	IB	-IC	0	0
10	01	01	00	00	01	00	01	00	-Ia	Ib-IC	Ic-IB	0	0	IB	0	IC	0
10	01	01	00	00	01	00	00	01	-Ia	Ib	IA+Ic	0	0	IB	0	0	IC
10	01	00	10	00	01	10	00	00	Ib-IA	Ib	0	Ic-IB	0	Ic	-IC	0	0
10	01	00	10	00	01	00	01	00	IB+Ib	Ib-IC	0	Ic-IB	0	Ic	0	IC	0
10	01	00	10	00	01	00	00	01	Ib-IA	Ib	0	IA+Ic	0	Ic-IC	0	0	IC
10	01	00	10	00	00	10	00	01	Ib-IA	Ib	0	-IB	0	0	Ic-IC	0	Ic
10	01	00	10	00	00	00	01	01	IB-Ia	-IC-Ia	0	-IB	0	0	0	IC-Ic	Ic
10	01	00	00	01	01	10	00	00	IC-Ia	-IB-Ia	0	0	IB-Ic	Ic	-IC	0	0
10	01	00	00	01	01	00	01	00	-Ia	IA-Ia	0	0	IB-Ic	Ic	0	IC	0
10	01	00	00	01	01	00	00	01	-Ia	IA-Ia	0	0	-IA-Ic	Ic-IC	0	0	IC
10	01	00	00	01	00	10	00	01	IC+Ib	Ib-IB	0	0	IB	0	Ic-IC	0	Ic
10	01	00	00	01	00	00	01	01	-Ia	IA-Ia	0	0	IB	0	0	IC-Ic	Ic
10	01	00	00	00	01	10	00	01	Ib-IA	Ib	0	0	0	IB	IA+Ic	0	Ic-IB
10	01	00	00	00	01	00	01	01	-Ia	IA-Ia	0	0	0	IB	0	-IA-Ic	Ic-IB
10	00	01	10	01	00	10	00	00	Ic-IA	0	Ic	Ib-IB	Ib	0	-IC	0	0
10	00	01	10	01	00	00	01	00	Ic-IA	0	Ic	IA+Ib	Ib-IC	0	0	IC	0
10	00	01	10	01	00	00	00	01	IB+Ic	0	Ic-IC	Ib-IB	Ib	0	0	0	IC
10	00	01	10	00	00	10	01	00	Ic-IA	0	Ic	-IB	0	0	Ib-IC	Ib	0
10	00	01	10	00	00	00	01	01	IB-Ia	0	-IC-Ia	-IB	0	0	0	Ib	IC-Ib
10	00	01	00	01	01	10	00	00	IC-Ia	0	-IB-Ia	0	Ib	IB-Ib	-IC	0	0
10	00	01	00	01	01	00	01	00	-Ia	0	IA-Ia	0	Ib-IC	-IA-Ib	0	IC	0
10	00	01	00	01	01	00	00	01	-Ia	0	IA-Ia	0	Ib	IB-Ib	0	0	IC
10	00	01	00	01	00	10	01	00	Ic-IA	0	Ic	0	IB	0	IA+Ib	Ib-IB	0
10	00	01	00	01	00	00	01	01	-Ia	0	IA-Ia	0	IB	0	0	Ib-IB	-IA-Ib
10	00	01	00	00	01	10	01	00	IC+Ic	0	Ic-IB	0	0	IB	Ib-IC	Ib	0
10	00	01	00	00	01	00	01	01	-Ia	0	IA-Ia	0	0	IB	0	Ib	IC-Ib
10	00	00	10	00	00	10	01	01	-IA	0	0	-IB	0	0	-IC-Ia	Ib	Ic
10	00	00	00	01	00	10	01	01	-IA	0	0	0	IB	0	IA-Ia	Ib-IB	Ic
10	00	00	00	00	01	10	01	01	-IA	0	0	0	0	IB	IA-Ia	Ib	Ic-IB
10	00	00	10	01	00	10	00	01	-IA	0	0	Ib-IB	Ib	0	Ic-IC	0	Ic
10	00	00	10	01	00	00	01	01	-IA	0	0	IA-Ia	-IC-Ia	0	0	IC-Ic	Ic
10	00	00	10	00	01	10	01	00	-IA	0	0	Ic-IB	0	Ic	Ib-IC	Ib	0
10	00	00	10	00	01	00	01	01	-IA	0	0	IA-Ia	0	-IC-Ia	0	Ib	IC-Ib
10	00	00	00	01	01	10	01	00	-IA	0	0	0	IB-Ic	Ic	IA-Ia	-IB-Ia	0

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
10	00	00	00	01	01	10	00	01	-IA	0	0	0	Ib	IB-Ib	IA-Ia	0	-IB-Ia
10	00	00	10	01	01	10	00	00	-IA	0	0	-IB-Ia	Ib	Ic	-IC	0	0
10	00	00	10	01	01	00	01	00	-IA	0	0	IA-Ia	Ib-IC	Ic	0	IC	0
10	00	00	10	01	01	00	00	01	-IA	0	0	IA-Ia	Ib	Ic-IC	0	0	IC
00	01	01	10	01	00	10	00	00	0	IA-Ic	Ic	IC-Ia	-IA-Ia	0	-IC	0	0
00	01	01	10	01	00	00	01	00	0	IA-Ic	Ic	-Ia	IB-Ia	0	0	IC	0
00	01	01	10	01	00	00	00	01	0	-IB-Ic	Ic-IC	-Ia	IB-Ia	0	0	0	IC
00	01	01	10	00	01	10	00	00	0	Ib	IA-Ib	IC-Ia	0	-IA-Ia	-IC	0	0
00	01	01	10	00	01	00	01	00	0	Ib-IC	-IB-Ib	-Ia	0	IB-Ia	0	IC	0
00	01	01	10	00	01	00	00	01	0	Ib	IA-Ib	-Ia	0	IB-Ia	0	0	IC
00	01	01	10	00	00	10	01	00	0	IA-Ic	Ic	-IB	0	0	IB-Ia	-IA-Ia	0
00	01	01	10	00	00	10	00	01	0	Ib	IA-Ib	-IB	0	0	IB-Ia	0	-IA-Ia
00	01	01	00	01	00	10	01	00	0	IA-Ic	Ic	0	IB	0	-Ia	IC-Ia	0
00	01	01	00	01	00	10	00	01	0	Ib-IB	-IC-Ib	0	IB	0	-Ia	0	IC-Ia
00	01	01	00	00	01	10	01	00	0	-IC-Ic	Ic-IB	0	0	IB	-Ia	IC-Ia	0
00	01	01	00	00	01	10	00	01	0	Ib	IA-Ib	0	0	IB	-Ia	0	IC-Ia
00	01	00	10	01	01	10	00	00	0	IA	0	IC-Ia	Ib-IA	Ic	-IC	0	0
00	01	00	10	01	01	00	01	00	0	IA	0	-Ia	IB+Ib	Ic	0	IC	0
00	01	00	10	01	01	00	00	01	0	IA	0	-Ia	Ib-IA	Ic-IC	0	0	IC
00	01	00	10	01	00	10	00	01	0	IA	0	IC+Ib	Ib-IA	0	Ic-IC	0	Ic
00	01	00	10	01	00	00	01	01	0	IA	0	-Ia	IB-Ia	0	0	IC-Ic	Ic
00	01	00	10	00	01	10	01	00	0	IA	0	Ic-IB	0	Ic	IB+Ib	Ib-IA	0
00	01	00	10	00	01	00	01	01	0	IA	0	-Ia	0	IB-Ia	0	Ib-IA	-IB-Ib
00	01	00	10	00	00	10	01	01	0	IA	0	-IB	0	0	IB-Ia	Ib-IA	Ic
00	01	00	00	01	01	10	01	00	0	IA	0	0	IB-Ic	Ic	-Ia	IC-Ia	0
00	01	00	00	01	01	10	00	01	0	IA	0	0	Ib-IA	-IC-Ib	-Ia	0	IC-Ia
00	01	00	00	01	00	10	01	01	0	IA	0	0	IB	0	-Ia	IC+Ib	Ic
00	01	00	00	00	01	10	01	01	0	IA	0	0	0	IB	-Ia	Ib-IA	Ic-IB
00	00	01	10	01	01	10	00	00	0	0	IA	IC-Ia	Ib	Ic-IA	-IC	0	0
00	00	01	10	01	01	00	01	00	0	0	IA	-Ia	Ib-IC	Ic-IA	0	IC	0
00	00	01	10	01	01	00	00	01	0	0	IA	-Ia	Ib	IB+Ic	0	0	IC
00	00	01	10	01	00	10	00	01	0	0	IA	Ib-IB	Ib	0	IB+Ic	0	Ic-IA
00	00	01	10	01	00	00	01	01	0	0	IA	-Ia	IB-Ia	0	0	-IB-Ic	Ic-IA
00	00	01	10	00	00	10	01	01	0	0	IA	-IB	0	0	IB-Ia	Ib	Ic-IA
00	00	01	10	00	01	10	01	00	0	0	IA	IC+Ic	0	Ic-IA	Ib-IC	0	Ib
00	00	01	10	00	01	00	01	01	0	0	IA	-Ia	0	IB-Ia	0	Ib	IC-Ib
00	00	01	00	01	01	10	01	00	0	0	IA	0	-IC-Ic	Ic-IA	-Ia	IC-Ia	0
00	00	01	00	01	01	10	00	01	0	0	IA	0	Ib	IB-Ib	-Ia	0	IC-Ia
00	00	01	00	01	00	10	01	01	0	0	IA	0	IB	0	-Ia	Ib-IB	Ic-IA
00	00	01	00	00	01	10	01	01	0	0	IA	0	0	IB	-Ia	Ib	IC+Ic

Table B.56: Switching device combinations for (V_{AB},V_{BC},V_{CA}) = (0,0,0) and (V_{ab},V_{bc},V_{ca}) = (0,+2V_{cap},−2V_{cap}).

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
employ five capacitors																	
10	10	01	10	00	00	10	00	00	-IA-Ia	-Ib	Ic	-IB	0	0	-IC	0	0
10	10	01	10	00	00	00	10	00	IB-Ia	IC-Ib	Ic	-IB	0	0	0	-IC	0
10	10	01	10	00	00	00	00	01	IB-Ia	-Ib	Ic-IC	-IB	0	0	0	0	IC
10	10	01	00	10	00	10	00	00	IC-Ia	IB-Ib	Ic	0	-IB	0	-IC	0	0
10	10	01	00	10	00	00	10	00	-Ia	-IA-Ib	Ic	0	-IB	0	0	-IC	0
10	10	01	00	10	00	00	00	01	-Ia	IB-Ib	Ic-IC	0	-IB	0	0	0	IC
10	10	01	00	00	01	10	00	00	IC-Ia	-Ib	Ic-IB	0	0	IB	-IC	0	0
10	10	01	00	00	01	00	10	00	-Ia	IC-Ib	Ic-IB	0	0	IB	0	-IC	0
10	10	01	00	00	01	00	00	01	-Ia	-Ib	IA+Ic	0	0	IB	0	0	IC
10	10	00	10	00	01	10	00	00	Ib-IA	-Ib	0	Ic-IB	0	Ic	-IC	0	0
10	10	00	10	00	01	00	10	00	IB+Ib	IC-Ib	0	Ic-IB	0	Ic	0	-IC	0
10	10	00	10	00	01	00	00	01	Ib-IA	-Ib	0	IA+Ic	0	Ic-IC	0	0	IC
10	10	00	10	00	00	10	00	01	Ib-IA	-Ib	0	-IB	0	0	Ic-IC	0	Ic
10	10	00	10	00	00	00	10	01	IB-Ia	IC+Ia	0	-IB	0	0	0	Ic-IC	Ic
10	10	00	00	10	01	10	00	00	IC-Ia	IB+Ia	0	0	Ic-IB	Ic	-IC	0	0
10	10	00	00	10	01	00	10	00	-Ia	Ia-IA	0	0	Ic-IB	Ic	0	-IC	0
10	10	00	00	10	01	00	00	01	-Ia	Ia-IA	0	0	IA+Ic	Ic-IC	0	0	IC
10	10	00	00	10	00	10	00	01	IC+Ib	IB-Ib	0	0	-IB	0	Ic-IC	0	Ic
10	10	00	00	10	00	00	10	01	-Ia	Ia-IA	0	0	-IB	0	0	Ic-IC	Ic
10	10	00	00	00	01	10	00	01	Ib-IA	-Ib	0	0	0	IB	IA+Ic	0	Ic-IB
10	10	00	00	00	01	00	10	01	-Ia	Ia-IA	0	0	0	IB	0	IA+Ic	Ic-IB
10	00	01	10	10	00	10	00	00	Ic-IA	0	Ic	Ib-IB	-Ib	0	-IC	0	0
10	00	01	10	10	00	00	10	00	Ic-IA	0	Ic	IA+Ib	IC-Ib	0	0	-IC	0
10	00	01	10	01	00	00	00	01	IB+Ic	0	Ic-IC	Ib-IB	-Ib	0	0	0	IC
10	00	01	10	00	00	10	10	00	Ic-IA	0	Ic	-IB	0	0	Ib-IC	-Ib	0
10	00	01	10	00	00	00	10	01	IB-Ia	0	-IC-Ia	-IB	0	0	0	-Ib	IC-Ib
10	00	01	00	10	01	10	00	00	IC-Ia	0	-IB-Ia	0	-Ib	IB-Ib	-IC	0	0
10	00	01	00	10	01	00	10	00	-Ia	0	IA-Ia	0	IC-Ib	-IA-Ib	0	-IC	0
10	00	01	00	10	01	00	00	01	-Ia	0	IA-Ia	0	-Ib	IB-Ib	0	0	IC
10	00	01	00	10	00	10	10	00	Ic-IA	0	Ic	0	-IB	0	IA+Ib	IB-Ib	0
10	00	01	00	10	00	00	10	01	-Ia	0	IA-Ia	0	-IB	0	0	IB-Ib	-IA-Ib
10	00	01	00	00	01	10	10	00	IC+Ic	0	Ic-IB	0	0	IB	Ib-IC	-Ib	0
10	00	01	00	00	01	00	10	01	-Ia	0	IA-Ia	0	0	IB	0	-Ib	IC-Ib
10	00	00	10	10	01	10	00	00	-IA	0	0	-IB-Ia	-Ib	Ic	-IC	0	0
10	00	00	10	10	01	00	10	00	-IA	0	0	IA-Ia	IC-Ib	Ic	0	-IC	0
10	00	00	10	10	01	00	00	01	-IA	0	0	IA-Ia	-Ib	Ic-IC	0	0	IC
10	00	00	10	10	00	10	00	01	-IA	0	0	Ib-IB	-Ib	0	Ic-IC	0	Ic
10	00	00	10	10	00	00	10	01	-IA	0	0	IA-Ia	IC+Ia	0	0	Ic-IC	Ic
10	00	00	10	00	01	10	10	00	-IA	0	0	Ic-IB	0	Ic	Ib-IC	-Ib	0
10	00	00	10	00	01	00	10	01	-IA	0	0	IA-Ia	0	-IC-Ia	0	-Ib	IC-Ib
10	00	00	10	00	00	10	10	01	-IA	0	0	-IB	0	0	-IC-Ia	-Ib	Ic

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
10	00	00	00	10	01	10	10	00	-IA	0	0	0	Ic-IB	Ic	IA-Ia	IB+Ia	0
10	00	00	00	10	01	10	00	01	-IA	0	0	0	-Ib	IB-Ib	IA-Ia	0	-IB-Ia
10	00	00	00	10	00	10	10	01	-IA	0	0	0	-IB	0	IA-Ia	IB-Ib	Ic
10	00	00	00	00	01	10	10	01	-IA	0	0	0	0	IB	IA-Ia	-Ib	Ic-IB
00	10	01	10	10	00	10	00	00	0	Ic-IA	Ic	IC-Ia	IA+Ia	0	-IC	0	0
00	10	01	10	10	00	00	10	00	0	Ic-IA	Ic	-Ia	Ia-IB	0	0	-IC	0
00	10	01	10	10	00	00	00	01	0	IB+Ic	Ic-IC	-Ia	Ia-IB	0	0	0	IC
00	10	01	10	00	01	10	00	00	0	-Ib	IA-Ib	IC-Ia	0	-IA-Ia	-IC	0	0
00	10	01	10	00	01	00	10	00	0	IC-Ib	-IB-Ib	-Ia	0	IB-Ia	0	-IC	0
00	10	01	10	00	01	00	00	01	0	-Ib	IA-Ib	-Ia	0	IB-Ia	0	0	IC
00	10	01	10	00	00	10	10	00	0	Ic-IA	Ic	-IB	0	0	IB-Ia	IA+Ia	0
00	10	01	10	00	00	10	00	01	0	-Ib	IA-Ib	-IB	0	0	IB-Ia	0	-IA-Ia
00	10	01	00	10	00	10	10	00	0	Ic-IA	Ic	0	-IB	0	-Ia	Ia-IC	0
00	10	01	00	10	00	10	00	01	0	IB-Ib	-IC-Ib	0	-IB	0	-Ia	0	IC-Ia
00	10	01	00	00	01	10	10	00	0	IC+Ic	Ic-IB	0	0	IB	-Ia	Ia-IC	0
00	10	01	00	00	01	10	00	01	0	-Ib	IA-Ib	0	0	IB	-Ia	0	IC-Ia
00	10	00	10	10	01	10	00	00	0	-IA	0	IC-Ia	IA-Ib	Ic	-IC	0	0
00	10	00	10	10	01	00	10	00	0	-IA	0	-Ia	-IB-Ib	Ic	0	-IC	0
00	10	00	10	10	01	00	00	01	0	-IA	0	-Ia	IA-Ib	Ic-IC	0	0	IC
00	10	00	10	10	00	10	00	01	0	-IA	0	IC+Ib	IA-Ib	0	Ic-IC	0	Ic
00	10	00	10	10	00	00	10	01	0	-IA	0	-Ia	Ia-IB	0	0	Ic-IC	Ic
00	10	00	10	00	01	10	10	00	0	-IA	0	Ic-IB	0	Ic	IB+Ib	IA-Ib	0
00	10	00	10	00	01	00	10	01	0	-IA	0	-Ia	0	IB-Ia	0	IA-Ib	-IB-Ib
00	10	00	10	00	00	10	10	01	0	-IA	0	-IB	0	0	IB-Ia	IA-Ib	Ic
00	10	00	00	10	01	10	10	00	0	-IA	0	0	Ic-IB	Ic	-Ia	Ia-IC	0
00	10	00	00	10	00	10	10	01	0	-IA	0	0	-IB	0	-Ia	-IC-Ib	Ic
00	10	00	00	10	01	10	00	01	0	-IA	0	0	IA-Ib	-IC-Ib	-Ia	0	IC-Ia
00	10	00	00	00	01	10	10	01	0	-IA	0	0	0	IB	-Ia	IA-Ib	Ic-IB
00	00	01	10	10	01	10	00	00	0	0	IA	IC-Ia	-Ib	Ic-IA	-IC	0	0
00	00	01	10	10	01	00	10	00	0	0	IA	-Ia	IC-Ib	Ic-IA	0	-IC	0
00	00	01	10	10	01	00	00	01	0	0	IA	-Ia	-Ib	IB+Ic	0	0	IC
00	00	01	10	10	00	10	00	01	0	0	IA	Ib-IB	-Ib	0	IB+Ic	0	Ic-IA
00	00	01	10	10	00	00	10	01	0	0	IA	-Ia	Ia-IB	0	0	IB+Ic	Ic-IA
00	00	01	10	00	01	10	10	00	0	0	IA	IC+Ic	0	Ic-IA	Ib-IC	-Ib	0
00	00	01	10	00	01	00	10	01	0	0	IA	-Ia	0	IB-Ia	0	-Ib	IC-Ib
00	00	01	10	00	00	10	10	01	0	0	IA	-IB	0	0	IB-Ia	-Ib	Ic-IA
00	00	10	00	10	01	10	10	00	0	0	IA	0	IC+Ic	Ic-IA	-Ia	Ia-IC	0
00	00	01	00	10	01	10	00	01	0	0	IA	0	-Ib	IB-Ib	-Ia	0	IC-Ia
00	00	01	00	10	00	10	10	01	0	0	IA	0	-IB	0	-Ia	IB-Ib	Ic-IA
00	00	01	00	00	01	10	10	01	0	0	IA	0	0	IB	-Ia	-Ib	IC+Ic

Table B.57: Switching device combinations for (V_{AB},V_{BC},V_{CA}) = (0,0,0) and (V_{ab},V_{bc},V_{ca}) = ($-2V_{cap}$,$+2V_{cap}$,0).

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
employ five capacitors																	
01	10	01	01	00	00	01	00	00	IA+Ia	-Ib	Ic	IB	0	0	IC	0	0
01	10	01	01	00	00	00	10	00	Ia-IB	IC-Ib	Ic	IB	0	0	0	-IC	0
01	10	01	01	00	00	00	00	01	Ia-IB	-Ib	Ic-IC	IB	0	0	0	0	IC
01	10	01	00	10	00	01	00	00	Ia-IC	IB-Ib	Ic	0	-IB	0	IC	0	0
01	10	01	00	10	00	00	10	00	Ia	-IA-Ib	Ic	0	-IB	0	0	-IC	0
01	10	01	00	10	00	00	00	01	Ia	IB-Ib	Ic-IC	0	-IB	0	0	0	IC
01	10	01	00	00	01	01	00	00	Ia-IC	-Ib	Ic-IB	0	0	IB	IC	0	0
01	10	01	00	00	01	00	10	00	Ia	IC-Ib	Ic-IB	0	0	IB	0	-IC	0
01	10	01	00	00	01	00	00	01	Ia	-Ib	IA+Ic	0	0	IB	0	0	IC
01	10	00	01	00	01	01	00	00	IA-Ib	-Ib	0	IB-Ic	0	Ic	IC	0	0
01	10	00	01	00	01	00	10	00	-IB-Ib	IC-Ib	0	IB-Ic	0	Ic	0	-IC	0
01	10	00	01	00	01	00	00	01	IA-Ib	-Ib	0	-IA-Ic	0	Ic-IC	0	0	IC
01	10	00	01	00	00	01	00	01	IA-Ib	-Ib	0	IB	0	0	IC-Ic	0	Ic
01	10	00	01	00	00	00	10	10	Ia-IB	IC+Ia	0	IB	0	0	0	Ic-IC	Ic
01	10	00	00	10	01	01	00	00	Ia-IC	IB+Ia	0	0	Ic-IB	Ic	IC	0	0
01	10	00	00	10	01	00	10	00	Ia	Ia-IA	0	0	Ic-IB	Ic	0	-IC	0
01	10	00	00	10	01	00	00	01	Ia	Ia-IA	0	0	IA+Ic	Ic-IC	0	0	IC
01	10	00	00	10	00	01	00	01	-IC-Ib	IB-Ib	0	0	-IB	0	IC-Ic	0	Ic
01	10	00	00	10	00	00	10	01	Ia	Ia-IA	0	0	-IB	0	0	Ic-IC	Ic
01	01	00	00	10	00	00	10	01	Ia	IA-Ia	0	0	-IB	0	0	IB-Ib	-IA-Ib
01	10	00	00	00	01	01	00	01	IA-Ib	-Ib	0	0	0	IB	-IA-Ic	0	Ic-IB
01	10	00	00	00	01	00	10	01	Ia	Ia-IA	0	0	0	IB	0	IA+Ic	Ic-IB
01	00	01	01	10	00	01	00	00	IA-Ic	0	Ic	IB-Ib	-Ib	0	IC	0	0
01	00	01	01	10	00	00	10	00	IA-Ic	0	Ic	-IA-Ib	IC-Ib	0	0	-IC	0
01	00	01	01	10	00	00	00	01	-IB-Ic	0	Ic-IC	IB-Ib	-Ib	0	0	0	IC
01	00	01	01	00	00	01	10	00	IA-Ic	0	Ic	IB	0	0	IC-Ib	-Ib	0
01	00	01	01	00	00	00	10	01	Ia-IB	0	-IC-Ia	IB	0	0	0	-Ib	IC-Ib
01	00	01	00	10	01	01	00	00	Ia-IC	0	-IB-Ia	0	-Ib	IB-Ib	IC	0	0
01	00	01	00	10	01	00	10	00	Ia	0	IA-Ia	0	IC-Ib	-IA-Ib	0	-IC	0
01	00	01	00	10	01	00	00	01	Ia	0	IA-Ia	0	-Ib	IB-Ib	0	0	IC
01	00	01	00	10	00	01	10	00	IA-Ic	0	Ic	0	-IB	0	-IA-Ib	IB-Ib	0
01	00	01	00	00	01	01	10	00	-IC-Ic	0	Ic-IB	0	0	IB	IC-Ib	-Ib	0
01	00	01	00	00	01	00	10	01	Ia	0	IA-Ia	0	0	IB	0	-Ib	IC-Ib
01	00	00	01	10	01	01	00	00	IA	0	0	IB+Ia	-Ib	Ic	IC	0	0
01	00	00	01	10	01	00	10	00	IA	0	0	Ia-IA	IC-Ib	Ic	0	-IC	0
01	00	00	01	10	01	00	00	01	IA	0	0	Ia-IA	-Ib	Ic-IC	0	0	IC
01	00	00	01	10	00	01	00	01	IA	0	0	IB-Ib	-Ib	0	IC-Ic	0	Ic
01	00	00	01	10	00	00	10	01	IA	0	0	Ia-IA	IC+Ia	0	0	Ic-IC	Ic
01	00	00	01	00	01	01	10	00	IA	0	0	IB-Ic	0	Ic	IC-Ib	-Ib	0
01	00	00	01	00	01	00	10	01	IA	0	0	Ia-IA	0	-IC-Ia	0	-Ib	IC-Ib
01	00	00	01	00	00	01	10	01	IA	0	0	IB	0	0	IC+Ia	-Ib	Ic

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
01	00	00	00	10	01	01	10	00	IA	0	0	0	Ic-IB	Ic	Ia-IA	IB+Ia	0
01	00	00	00	10	01	01	00	01	IA	0	0	0	-Ib	IB-Ib	Ia-IA	0	-IB-Ia
01	00	00	00	10	00	01	10	01	IA	0	0	0	-IB	0	Ia-IA	IB-Ib	Ic
01	00	00	00	00	01	01	10	01	IA	0	0	0	0	IB	Ia-IA	-Ib	Ic-IB
00	10	01	01	10	00	01	00	00	0	Ic-IA	Ic	Ia-IC	IA+Ia	0	IC	0	0
00	10	01	01	10	00	00	10	00	0	Ic-IA	Ic	Ia	Ia-IB	0	0	-IC	0
00	10	01	01	10	00	00	00	01	0	IB+Ic	Ic-IC	Ia	Ia-IB	0	0	0	IC
00	10	01	01	00	01	01	00	00	0	-Ib	IA-Ib	Ia-IC	0	-IA-Ia	IC	0	0
00	10	01	01	00	01	00	10	00	0	IC-Ib	-IB-Ib	Ia	0	IB-Ia	0	-IC	0
00	10	01	01	00	01	00	00	01	0	-Ib	IA-Ib	Ia	0	IB-Ia	0	0	IC
00	10	01	01	00	00	01	10	00	0	Ic-IA	Ic	IB	0	0	Ia-IB	IA+Ia	0
00	10	01	01	00	00	01	00	01	0	-Ib	IA-Ib	IB	0	0	Ia-IB	0	-IA-Ia
00	10	01	00	10	00	01	10	00	0	Ic-IA	Ic	0	-IB	0	Ia	Ia-IC	0
00	10	01	00	10	00	01	00	01	0	IB-Ib	-IC-Ib	0	-IB	0	Ia	0	IC-Ia
00	10	01	00	00	01	01	10	00	0	IC+Ic	Ic-IB	0	0	IB	Ia	Ia-IC	0
00	10	01	00	00	01	01	00	01	0	-Ib	IA-Ib	0	0	IB	Ia	0	IC-Ia
00	10	00	01	10	01	01	00	00	0	-IA	0	Ia-IC	IA-Ib	Ic	IC	0	0
00	10	00	01	10	01	00	10	00	0	-IA	0	Ia	-IB-Ib	Ic	0	-IC	0
00	10	00	01	10	01	00	00	01	0	-IA	0	Ia	IA-Ib	Ic-IC	0	0	IC
00	10	00	01	10	00	01	00	01	0	-IA	0	-IC-Ib	IA-Ib	0	IC-Ic	0	Ic
00	10	00	01	10	00	00	10	01	0	-IA	0	Ia	Ia-IB	0	0	Ic-IC	Ic
00	10	00	01	00	01	01	10	00	0	-IA	0	IB-Ic	0	Ic	-IB-Ib	IA-Ib	0
00	10	00	01	00	01	00	10	01	0	-IA	0	Ia	0	IB-Ia	0	IA-Ib	-IB-Ib
00	10	00	01	00	00	01	10	01	0	-IA	0	IB	0	0	Ia-IB	IA-Ib	Ic
00	10	00	01	00	00	01	10	01	0	-IA	0	IB	0	0	Ia-IB	IA-Ib	Ic
00	10	00	00	10	01	01	10	00	0	-IA	0	0	Ic-IB	Ic	Ia	Ia-IC	0
00	10	00	00	10	01	01	00	01	0	-IA	0	0	IA-Ib	-IC-Ib	Ia	0	IC-Ia
00	10	00	00	10	00	01	10	01	0	-IA	0	0	-IB	0	Ia	-IC-Ib	Ic
00	10	00	00	00	01	01	10	01	0	-IA	0	0	0	IB	Ia	IA-Ib	Ic-IB
00	00	01	01	10	01	01	00	00	0	0	IA	Ia-IC	-Ib	Ic-IA	IC	0	0
00	00	01	01	10	01	00	10	00	0	0	IA	Ia	IC-Ib	Ic-IA	0	-IC	0
00	00	01	01	10	01	00	00	01	0	0	IA	Ia	-Ib	IB+Ic	0	0	IC
00	00	01	01	10	00	01	00	01	0	0	IA	IB-Ib	-Ib	0	-IB-Ic	0	Ic-IA
00	00	01	01	10	00	00	10	01	0	0	IA	Ia	Ia-IB	0	0	IB+Ic	Ic-IA
00	00	01	01	00	01	01	10	00	0	0	IA	-IC-Ic	0	Ic-IA	IC-Ib	-Ib	0
00	00	01	01	00	01	00	10	01	0	0	IA	Ia	0	IB-Ia	0	-Ib	IC-Ib
00	00	01	00	10	01	01	10	00	0	0	IA	0	IC+Ic	Ic-IA	Ia	0	Ia-IC
00	00	01	00	10	01	01	00	01	0	0	IA	0	-Ib	IB-Ib	Ia	0	IC-Ia
00	00	01	00	10	00	01	10	01	0	0	IA	0	-IB	0	Ia	IB-Ib	Ic-IA
00	00	01	00	00	01	01	10	01	0	0	IA	0	0	IB	Ia	-Ib	IC+Ic

Table B.58: Switching device combinations for (V_{AB},V_{BC},V_{CA}) = (0,0,0) and (V_{ab},V_{bc},V_{ca}) = ($-2V_{cap}$,0,$+2Vcap$).

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
employ five capacitors																	
01	10	10	01	00	00	01	00	00	IA+Ia	-Ib	-Ic	IB	0	0	IC	0	0
01	10	10	01	00	00	00	10	00	Ia-IB	IC-Ib	-Ic	IB	0	0	0	-IC	0
01	10	10	01	00	00	00	00	10	Ia-IB	-Ib	IC-Ic	IB	0	0	0	0	-IC
01	10	10	00	10	00	01	00	00	Ia-IC	IB-Ib	-Ic	0	-IB	0	IC	0	0
01	10	10	00	10	00	00	10	00	Ia	-IA-Ib	-Ic	0	-IB	0	0	-IC	0
01	10	10	00	10	00	00	00	10	Ia	IB-Ib	IC-Ic	0	-IB	0	0	0	-IC
01	10	10	00	00	10	01	00	00	Ia-IC	-Ib	IB-Ic	0	0	-IB	IC	0	0
01	10	10	00	00	10	00	10	00	Ia	IC-Ib	IB-Ic	0	0	-IB	0	-IC	0
01	10	10	00	00	10	00	00	10	Ia	-Ib	-IA-Ic	0	0	-IB	0	0	-IC
01	10	00	01	00	10	01	00	00	IA-Ib	-Ib	0	IB-Ic	0	-Ic	IC	0	0
01	10	00	01	00	10	00	10	00	-IB-Ib	IC-Ib	0	IB-Ic	0	-Ic	0	-IC	0
01	10	00	01	00	10	00	00	10	IA-Ib	-Ib	0	-IA-Ic	0	IC-Ic	0	0	-IC
01	10	00	01	00	00	01	00	10	IA-Ib	-Ib	0	IB	0	0	IC-Ic	0	-Ic
01	10	00	01	00	00	00	10	10	Ia-IB	IC+Ia	0	IB	0	0	0	Ic-IC	-Ic
01	10	00	00	10	10	01	00	00	Ia-IC	IB+Ia	0	0	Ic-IB	-Ic	IC	0	0
01	10	00	00	10	10	00	10	00	Ia	Ia-IA	0	0	Ic-IB	-Ic	0	-IC	0
01	10	00	00	10	10	00	00	10	Ia	Ia-IA	0	0	IA+Ic	IC-Ic	0	0	-IC
01	10	00	00	10	00	01	00	10	-IC-Ib	IB-Ib	0	0	-IB	0	IC-Ic	0	-Ic
01	10	00	00	10	00	00	10	10	Ia	Ia-IA	0	0	-IB	0	0	Ic-IC	-Ic
01	10	00	00	00	10	01	00	10	IA-Ib	-Ib	0	0	0	-IB	-IA-Ic	0	IB-Ic
01	10	00	00	00	10	00	10	10	Ia	Ia-IA	0	0	0	-IB	0	IA+Ic	IB-Ic
01	00	10	01	10	00	01	00	00	IA-Ic	0	-Ic	IB-Ib	-Ib	0	IC	0	0
01	00	10	01	10	00	00	10	00	IA-Ic	0	-Ic	-IA-Ib	IC-Ib	0	0	-IC	0
01	00	10	01	10	00	00	00	10	-IB-Ic	0	IC-Ic	IB-Ib	-Ib	0	0	0	-IC
01	00	10	01	00	00	01	10	00	IA-Ic	0	-Ic	IB	0	0	IC-Ib	-Ib	0
01	00	10	01	00	00	00	10	10	Ia-IB	0	IC+Ia	IB	0	0	0	-Ib	Ib-IC
01	00	10	00	10	10	01	00	00	Ia-IC	0	IB+Ia	0	-Ib	Ib-IB	IC	0	0
01	00	10	00	10	10	00	10	00	Ia	0	Ia-IA	0	IC-Ib	IA+Ib	0	-IC	0
01	00	10	00	10	10	00	00	10	Ia	0	Ia-IA	0	-Ib	Ib-IB	0	0	-IC
01	00	10	00	10	00	01	10	00	IA-Ic	0	-Ic	0	-IB	0	-IA-Ib	IB-Ib	0
01	00	10	00	10	00	00	10	10	Ia	0	Ia-IA	0	-IB	0	0	IB-Ib	IA+Ib
01	00	10	00	00	10	01	10	00	-IC-Ic	0	IB-Ic	0	0	-IB	IC-Ib	-Ib	0
01	00	10	00	00	10	00	10	10	Ia	0	Ia-IA	0	0	-IB	0	-Ib	Ib-IC
01	00	00	01	10	10	01	00	00	IA	0	0	IB+Ia	-Ib	-Ic	IC	0	0
01	00	00	01	10	10	00	10	00	IA	0	0	Ia-IA	IC-Ib	-Ic	0	-IC	0
01	00	00	01	10	10	00	00	10	IA	0	0	Ia-IA	-Ib	IC-Ic	0	0	-IC
01	00	00	01	10	00	01	00	10	IA	0	0	IB-Ib	-Ib	0	IC-Ic	0	-Ic
01	00	00	01	10	00	00	10	10	IA	0	0	Ia-IA	IC+Ia	0	0	Ic-IC	-Ic
01	00	00	01	00	10	01	10	00	IA	0	0	IB-Ic	0	-Ic	IC-Ib	-Ib	0
01	00	00	01	00	10	00	10	10	IA	0	0	Ia-IA	0	IC+Ia	0	-Ib	Ib-IC
01	00	00	01	00	00	01	10	10	IA	0	0	IB	0	0	IC+Ia	-Ib	-Ic

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
01	00	00	00	10	10	01	10	00	IA	0	0	0	Ic-IB	-Ic	Ia-IA	IB+Ia	0
01	00	00	00	10	10	01	00	10	IA	0	0	0	-Ib	Ib-IB	Ia-IA	0	IB+Ia
01	00	00	00	10	00	01	10	10	IA	0	0	0	-IB	0	Ia-IA	IB-Ib	-Ic
01	00	00	00	00	10	01	10	10	IA	0	0	0	0	-IB	Ia-IA	-Ib	IB-Ic
00	10	10	01	10	00	01	00	00	0	Ic-IA	-Ic	Ia-IC	IA+Ia	0	IC	0	0
00	10	10	01	10	00	00	10	00	0	Ic-IA	-Ic	Ia	Ia-IB	0	0	-IC	0
00	10	10	01	10	00	00	00	10	0	IB+Ic	IC-Ic	Ia	Ia-IB	0	0	0	-IC
00	10	10	01	00	10	01	00	00	0	-Ib	Ib-IA	Ia-IC	0	IA+Ia	IC	0	0
00	10	10	01	00	10	00	10	00	0	IC-Ib	IB+Ib	Ia	0	Ia-IB	0	-IC	0
00	10	10	01	00	10	00	00	10	0	-Ib	Ib-IA	Ia	0	Ia-IB	0	0	-IC
00	10	10	01	00	00	01	10	00	0	Ic-IA	-Ic	IB	0	0	Ia-IB	IA+Ia	0
00	10	10	01	00	00	01	00	10	0	-Ib	Ib-IA	IB	0	0	Ia-IB	0	IA+Ia
00	10	10	00	10	00	01	10	00	0	Ic-IA	-Ic	0	-IB	0	Ia	Ia-IC	0
00	10	10	00	10	00	01	00	10	0	IB-Ib	IC+Ib	0	-IB	0	Ia	0	Ia-IC
00	10	10	00	00	10	01	10	00	0	IC+Ic	IB-Ic	0	0	-IB	Ia	Ia-IC	0
00	10	10	00	00	10	01	00	10	0	-Ib	Ib-IA	0	0	-IB	Ia	0	Ia-IC
00	10	00	01	10	10	01	00	00	0	-IA	0	Ia-IC	IA-Ib	-Ic	IC	0	0
00	10	00	01	10	10	00	10	00	0	-IA	0	Ia	-IB-Ib	-Ic	0	-IC	0
00	10	00	01	10	10	00	00	10	0	-IA	0	Ia	IA-Ib	IC-Ic	0	0	-IC
00	10	00	01	10	00	01	00	10	0	-IA	0	-IC-Ib	IA-Ib	0	IC-Ic	0	-Ic
00	10	00	01	10	00	00	10	10	0	-IA	0	Ia	Ia-IB	0	0	Ic-IC	-Ic
00	10	00	01	00	10	01	10	00	0	-IA	0	IB-Ic	0	-Ic	-IB-Ib	IA-Ib	0
00	10	00	01	00	10	00	10	10	0	-IA	0	Ia	0	Ia-IB	0	IA-Ib	IB+Ib
00	10	00	01	00	00	01	10	10	0	-IA	0	IB	0	0	Ia-IB	IA-Ib	-Ic
00	10	00	00	10	10	01	10	00	0	-IA	0	0	Ic-IB	-Ic	Ia	Ia-IC	0
00	10	00	00	10	10	01	00	10	0	-IA	0	0	IA-Ib	IC+Ib	Ia	0	Ia-IC
00	10	00	00	10	00	01	10	10	0	-IA	0	0	-IB	0	Ia	-IC-Ib	-Ic
00	10	00	00	00	10	01	10	10	0	-IA	0	0	0	-IB	Ia	IA-Ib	IB-Ic
00	00	10	01	10	10	01	00	00	0	0	-IA	Ia-IC	-Ib	IA-Ic	IC	0	0
00	00	10	01	10	10	00	10	00	0	0	-IA	Ia	IC-Ib	IA-Ic	0	-IC	0
00	00	10	01	10	10	00	00	10	0	0	-IA	Ia	-Ib	-IB-Ic	0	0	-IC
00	00	10	01	10	00	01	00	10	0	0	-IA	IB-Ib	-Ib	0	-IB-Ic	0	IA-Ic
00	00	10	01	10	00	00	10	10	0	0	-IA	Ia	Ia-IB	0	0	IB+Ic	IA-Ic
00	00	10	01	00	10	01	10	00	0	0	-IA	-IC-Ic	0	IA-Ic	IC-Ib	0	-Ib
00	00	10	01	00	10	00	10	10	0	0	-IA	Ia	0	Ia-IB	-Ib	0	Ib-IC
00	00	10	01	00	00	01	10	10	0	0	-IA	IB	0	0	Ia-IB	-Ib	IA-Ic
00	00	10	00	10	10	01	10	00	0	0	-IA	0	IC+Ic	IA-Ic	Ia	Ia-IC	0
00	00	10	00	10	10	01	00	10	0	0	-IA	0	-Ib	Ib-IB	Ia	0	Ia-IC
00	00	10	00	10	00	01	10	10	0	0	-IA	0	-IB	0	Ia	IB-Ib	IA-Ic
00	00	10	00	00	10	01	10	10	0	0	-IA	0	0	-IB	Ia	-Ib	-IC-Ic

Table B.59: Switching device combinations for (V_{AB},V_{BC},V_{CA}) = (0,0,0) and (V_{ab},V_{bc},V_{ca}) = (0,$-2V_{cap}$,$+2V_{cap}$).

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
employ two capacitors																	
01	01	10	01	00	00	01	00	00	IA+Ia	Ib	-Ic	IB	0	0	IC	0	0
01	01	10	01	00	00	00	01	00	Ia-IB	Ib-IC	-Ic	IB	0	0	0	IC	0
01	01	10	01	00	00	00	00	10	Ia-IB	Ib	IC-Ic	IB	0	0	0	0	-IC
01	01	10	00	01	00	01	00	00	Ia-IC	Ib-IB	-Ic	0	IB	0	IC	0	0
01	01	10	00	01	00	00	01	00	Ia	IA+Ib	-Ic	0	IB	0	0	IC	0
01	01	10	00	01	00	00	00	10	Ia	Ib-IB	IC-Ic	0	IB	0	0	0	-IC
01	01	10	00	00	10	01	00	00	Ia-IC	Ib	IB-Ic	0	0	-IB	IC	0	0
01	01	10	00	00	10	00	01	00	Ia	Ib-IC	IB-Ic	0	0	-IB	0	IC	0
01	01	10	00	00	10	00	00	10	Ia	Ib	-IA-Ic	0	0	-IB	0	0	-IC
01	01	00	01	00	10	01	00	00	IA-Ib	Ib	0	IB-Ic	0	-Ic	IC	0	0
01	01	00	01	00	10	00	01	00	-IB-Ib	Ib-IC	0	IB-Ic	0	-Ic	0	IC	0
01	01	00	01	00	10	00	00	10	IA-Ib	Ib	0	-IA-Ic	0	IC-Ic	0	0	-IC
01	01	00	01	00	00	01	00	10	IA-Ib	Ib	0	IB	0	0	IC-Ic	0	-Ic
01	01	00	01	00	00	00	01	10	Ia-IB	-IC-Ia	0	IB	0	0	0	IC-Ic	-Ic
01	01	00	00	01	10	01	00	00	Ia-IC	-IB-Ia	0	0	IB-Ic	-Ic	IC	0	0
01	01	00	00	01	10	00	01	00	Ia	IA-Ia	0	0	IB-Ic	-Ic	0	IC	0
01	01	00	00	01	10	00	00	10	Ia	IA-Ia	0	0	-IA-Ic	IC-Ic	0	0	-IC
01	01	00	00	01	00	01	00	10	-IC-Ib	Ib-IB	0	0	IB	0	IC-Ic	0	-Ic
01	01	00	00	01	00	00	01	10	Ia	IA-Ia	0	0	IB	0	0	IC-Ic	-Ic
01	01	00	00	00	10	01	00	10	IA-Ib	Ib	0	0	0	-IB	-IA-Ic	0	IB-Ic
01	01	00	00	00	10	00	01	10	Ia	IA-Ia	0	0	0	-IB	0	-IA-Ic	IB-Ic
01	00	10	01	01	00	01	00	00	IA-Ic	0	-Ic	IB-Ib	Ib	0	IC	0	0
01	00	10	01	01	00	00	01	00	IA-Ic	0	-Ic	-IA-Ib	Ib-IC	0	0	IC	0
01	00	10	01	01	00	00	00	10	-IB-Ic	0	IC-Ic	IB-Ib	Ib	0	0	0	-IC
01	00	10	01	00	00	01	01	00	IA-Ic	0	-Ic	IB	0	0	IC-Ib	Ib	0
01	00	10	01	00	00	00	01	10	Ia-IB	0	IC+Ia	IB	0	0	0	Ib	Ib-IC
01	00	10	00	01	10	01	00	00	Ia-IC	0	IB+Ia	0	Ib	Ib-IB	IC	0	0
01	00	10	00	01	10	00	01	00	Ia	0	Ia-IA	0	Ib-IC	IA+Ib	0	IC	0
01	00	10	00	01	10	00	00	10	Ia	0	Ia-IA	0	Ib	Ib-IB	0	0	-IC
01	00	10	00	01	00	01	01	00	IA-Ic	0	-Ic	0	IB	0	-IA-Ib	Ib-IB	0
01	00	10	00	01	00	00	01	10	Ia	0	Ia-IA	0	IB	0	0	Ib-IB	IA+Ib
01	00	10	00	00	10	01	01	00	-IC-Ic	0	IB-Ic	0	0	-IB	IC-Ib	Ib	0
01	00	10	00	00	10	00	01	10	Ia	0	Ia-IA	0	0	-IB	0	Ib	Ib-IC
01	00	00	01	01	10	01	00	00	IA	0	0	IB+Ia	Ib	-Ic	IC	0	0
01	00	00	01	01	10	00	01	00	IA	0	0	Ia-IA	Ib-IC	-Ic	0	IC	0
01	00	00	01	01	10	00	00	10	IA	0	0	Ia-IA	Ib	IC-Ic	0	0	-IC
01	00	00	01	01	00	01	00	10	IA	0	0	IB-Ib	Ib	0	IC-Ic	0	-Ic
01	00	00	01	01	00	00	01	10	IA	0	0	Ia-IA	-IC-Ia	0	0	IC-Ic	-Ic
01	00	00	01	00	10	01	01	00	IA	0	0	IB-Ic	0	-Ic	IC-Ib	Ib	0
01	00	00	01	00	10	00	01	10	IA	0	0	Ia-IA	0	IC+Ia	0	Ib	Ib-IC
01	00	00	01	00	00	01	01	10	IA	0	0	IB	0	0	IC+Ia	Ib	-Ic

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
01	00	00	00	01	10	01	01	00	IA	0	0	0	IB-Ic	-Ic	Ia-IA	-IB-Ia	0
01	00	00	00	01	10	01	00	10	IA	0	0	0	Ib	Ib-IB	Ia-IA	0	IB+Ia
01	00	00	00	01	00	01	01	10	IA	0	0	0	IB	0	Ia-IA	Ib-IB	-Ic
01	00	00	00	00	10	01	01	10	IA	0	0	0	0	-IB	Ia-IA	Ib	IB-Ic
00	01	10	01	01	00	00	00	10	0	-IB-Ic	IC-Ic	Ia	IB-Ia	0	0	0	-IC
00	01	10	01	01	00	00	01	00	0	IA-Ic	-Ic	Ia	IB-Ia	0	0	IC	0
00	01	10	01	01	00	01	00	00	0	IA-Ic	-Ic	Ia-IC	-IA-Ia	0	IC	0	0
00	01	10	01	00	10	01	00	00	0	Ib	Ib-IA	Ia-IC	0	IA+Ia	IC	0	0
00	01	10	01	00	10	00	01	00	0	Ib-IC	IB+Ib	Ia	0	Ia-IB	0	IC	0
00	01	10	01	00	10	00	00	10	0	Ib	Ib-IA	Ia	0	Ia-IB	0	0	-IC
00	01	10	01	00	00	01	01	00	0	IA-Ic	-Ic	IB	0	0	Ia-IB	-IA-Ia	0
00	01	10	01	00	00	01	00	10	0	Ib	Ib-IA	IB	0	0	Ia-IB	0	IA+Ia
00	01	10	00	01	00	01	01	00	0	IA-Ic	-Ic	0	IB	0	Ia	IC-Ia	0
00	01	10	00	01	00	01	00	10	0	Ib-IB	IC+Ib	0	IB	0	Ia	0	Ia-IC
00	01	10	00	00	10	01	01	00	0	-IC-Ic	IB-Ic	0	0	-IB	Ia	IC-Ia	0
00	01	10	00	00	10	01	00	10	0	Ib	Ib-IA	0	0	-IB	Ia	0	Ia-IC
00	01	00	01	01	10	01	00	00	0	IA	0	Ia-IC	Ib-IA	-Ic	IC	0	0
00	01	00	01	01	10	00	01	00	0	IA	0	Ia	IB+Ib	-Ic	0	IC	0
00	01	00	01	01	10	00	00	10	0	IA	0	Ia	Ib-IA	IC-Ic	0	0	-IC
00	01	00	01	01	00	01	00	10	0	IA	0	-IC-Ib	Ib-IA	0	IC-Ic	0	-Ic
00	01	00	01	01	00	00	01	10	0	IA	0	Ia	IB-Ia	0	0	IC-Ic	-Ic
00	01	00	01	00	10	01	01	00	0	IA	0	IB-Ic	0	-Ic	-IB-Ib	Ib-IA	0
00	01	00	01	00	10	00	01	10	0	IA	0	Ia	0	Ia-IB	0	Ib-IA	IB+Ib
00	01	00	01	00	00	01	01	10	0	IA	0	IB	0	0	Ia-IB	Ib-IA	-Ic
00	01	00	00	01	10	01	01	00	0	IA	0	0	IB-Ic	-Ic	Ia	IC-Ia	0
00	01	00	00	01	10	01	00	10	0	IA	0	0	Ib-IA	IC+Ib	Ia	0	Ia-IC
00	01	00	00	01	00	01	01	10	0	IA	0	0	IB	0	Ia	IC+Ib	-Ic
00	01	00	00	00	10	01	01	10	0	IA	0	0	0	-IB	Ia	Ib-IA	IB-Ic
00	00	10	01	01	10	01	00	00	0	0	-IA	Ia-IC	Ib	IA-Ic	IC	0	0
00	00	10	01	01	10	00	01	00	0	0	-IA	Ia	Ib-IC	IA-Ic	0	IC	0
00	00	10	01	01	10	00	00	10	0	0	-IA	Ia	Ib	-IB-Ic	0	0	-IC
00	00	10	01	01	00	01	00	10	0	0	-IA	IB-Ib	Ib	0	-IB-Ic	0	IA-Ic
00	00	10	01	01	00	00	01	10	0	0	-IA	Ia	IB-Ia	0	0	-IB-Ic	IA-Ic
00	00	10	01	00	10	01	01	00	0	0	-IA	-IC-Ic	0	IA-Ic	IC-Ib	Ib	0
00	00	10	01	00	10	00	01	10	0	0	-IA	Ia	0	Ia-IB	0	Ib	Ib-IC
00	00	10	01	00	00	01	01	10	0	0	-IA	IB	0	0	Ia-IB	Ib	IA-Ic
00	00	10	00	01	10	01	01	00	0	0	-IA	0	-IC-Ic	IA-Ic	Ia	IC-Ia	0
00	00	10	00	01	10	01	00	10	0	0	-IA	0	Ib	Ib-IB	Ia	0	Ia-IC
00	00	10	00	01	00	01	01	10	0	0	-IA	0	IB	0	Ia	Ib-IB	IA-Ic
00	00	10	00	00	10	01	01	10	0	0	-IA	0	0	-IB	Ia	Ib	-IC-Ic

Table B.60: Switching device combinations for (V_{AB},V_{BC},V_{CA}) = (0,0,0) and (V_{ab},V_{bc},V_{ca}) = ($+2V_{cap}$,$-2V_{cap}$,0).

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
employ two capacitors																	
10	01	10	10	00	00	10	00	00	-IA-Ia	Ib	-Ic	-IB	0	0	-IC	0	0
10	01	10	10	00	00	00	01	00	IB-Ia	Ib-IC	-Ic	-IB	0	0	0	IC	0
10	01	10	10	00	00	00	00	10	IB-Ia	Ib	IC-Ic	-IB	0	0	0	0	-IC
10	01	10	00	01	00	10	00	00	IC-Ia	Ib-IB	-Ic	0	IB	0	-IC	0	0
10	01	10	00	01	00	00	01	00	-Ia	IA+Ib	-Ic	0	IB	0	0	IC	0
10	01	10	00	01	00	00	00	10	-Ia	Ib-IB	IC-Ic	0	IB	0	0	0	-IC
10	01	10	00	00	10	10	00	00	IC-Ia	Ib	IB-Ic	0	0	-IB	-IC	0	0
10	01	10	00	00	10	00	01	00	-Ia	Ib-IC	IB-Ic	0	0	-IB	0	IC	0
10	01	10	00	00	10	00	00	10	-Ia	Ib	-IA-Ic	0	0	-IB	0	0	-IC
10	01	00	10	00	10	10	00	00	Ib-IA	Ib	0	Ic-IB	0	-Ic	-IC	0	0
10	01	00	10	00	10	00	01	00	IB+Ib	Ib-IC	0	Ic-IB	0	-Ic	0	IC	0
10	01	00	10	00	10	00	00	10	Ib-IA	Ib	0	IA+Ic	0	IC-Ic	0	0	-IC
10	01	00	10	00	00	10	00	10	Ib-IA	Ib	0	-IB	0	0	Ic-IC	0	-Ic
10	01	00	10	00	00	00	01	01	IB-Ia	-IC-Ia	0	-IB	0	0	0	IC-Ic	-Ic
10	01	00	00	01	10	10	00	00	IC-Ia	-IB-Ia	0	0	IB-Ic	-Ic	-IC	0	0
10	01	00	00	01	10	00	01	00	-Ia	IA-Ia	0	0	IB-Ic	-Ic	0	IC	0
10	01	00	00	01	10	00	00	10	-Ia	IA-Ia	0	0	-IA-Ic	IC-Ic	0	0	-IC
10	01	00	00	01	00	10	00	10	IC+Ib	Ib-IB	0	0	IB	0	Ic-IC	0	-Ic
10	01	00	00	01	00	00	01	10	-Ia	IA-Ia	0	0	IB	0	0	IC-Ic	-Ic
10	01	00	00	00	10	10	00	10	Ib-IA	Ib	0	0	0	-IB	IA+Ic	0	IB-Ic
10	01	00	00	00	10	00	01	10	-Ia	IA-Ia	0	0	0	-IB	0	-IA-Ic	IB-Ic
10	00	10	10	01	00	10	00	00	Ic-IA	0	-Ic	Ib-IB	Ib	0	-IC	0	0
10	00	10	10	01	00	00	01	00	Ic-IA	0	-Ic	IA+Ib	Ib-IC	0	0	IC	0
10	00	10	10	01	00	00	00	10	IB+Ic	0	IC-Ic	Ib-IB	Ib	0	0	0	-IC
10	00	10	10	00	00	10	01	00	Ic-IA	0	-Ic	-IB	0	0	Ib-IC	Ib	0
10	00	10	10	00	00	00	01	10	IB-Ia	0	IC+Ia	-IB	0	0	0	Ib	Ib-IC
10	00	10	00	01	10	10	00	00	IC-Ia	0	IB+Ia	0	Ib	Ib-IB	-IC	0	0
10	00	10	00	01	10	00	01	00	-Ia	0	Ia-IA	0	Ib-IC	IA+Ib	0	IC	0
10	00	10	00	01	10	00	00	10	-Ia	0	Ia-IA	0	Ib	Ib-IB	0	0	-IC
10	00	10	00	01	00	10	01	00	Ic-IA	0	-Ic	0	IB	0	IA+Ib	Ib-IB	0
10	00	10	00	01	00	00	01	10	-Ia	0	Ia-IA	0	IB	0	0	Ib-IB	IA+Ib
10	00	10	00	00	10	10	01	00	IC+Ic	0	IB-Ic	0	0	-IB	Ib-IC	Ib	0
10	00	10	00	00	10	00	01	10	-Ia	0	Ia-IA	0	0	-IB	0	Ib	Ib-IC
10	00	00	10	01	10	10	00	00	-IA	0	0	-IB-Ia	Ib	-Ic	-IC	0	0
10	00	00	10	01	10	00	01	00	-IA	0	0	IA-Ia	Ib-IC	-Ic	0	IC	0
10	00	00	10	01	10	00	00	10	-IA	0	0	IA-Ia	Ib	IC-Ic	0	0	-IC
10	00	00	10	01	00	10	00	10	-IA	0	0	Ib-IB	Ib	0	Ic-IC	0	-Ic
10	00	00	10	01	00	00	01	10	-IA	0	0	IA-Ia	-IC-Ia	0	0	IC-Ic	-Ic
10	00	00	10	00	10	10	01	00	-IA	0	0	Ic-IB	0	-Ic	Ib-IC	Ib	0
10	00	00	10	00	10	00	01	10	-IA	0	0	IA-Ia	0	IC+Ia	0	Ib	Ib-IC
10	00	00	10	00	00	10	01	10	-IA	0	0	-IB	0	0	-IC-Ia	Ib	-Ic

States of switch cell									Current through capacitor								
S_{Aa}	S_{Ab}	S_{Ac}	S_{Ba}	S_{Bb}	S_{Bc}	S_{Ca}	S_{Cb}	S_{Cc}	C_{Aa}	C_{Ab}	C_{Ac}	C_{Ba}	C_{Bb}	C_{Bc}	C_{Ca}	C_{Cb}	C_{Cc}
10	00	00	00	01	10	10	01	00	-IA	0	0	0	IB-Ic	-Ic	IA-Ia	-IB-Ia	0
10	00	00	00	01	10	10	00	10	-IA	0	0	0	Ib	Ib-IB	IA-Ia	0	IB+Ia
10	00	00	00	01	00	10	01	10	-IA	0	0	0	IB	0	IA-Ia	Ib-IB	-Ic
10	00	00	00	00	10	10	01	10	-IA	0	0	0	0	-IB	IA-Ia	Ib	IB-Ic
00	01	10	10	01	00	10	00	00	0	IA-Ic	-Ic	IC-Ia	-IA-Ia	0	-IC	0	0
00	01	10	10	01	00	00	01	00	0	IA-Ic	-Ic	-Ia	IB-Ia	0	0	IC	0
00	01	10	10	01	00	00	00	10	0	-IB-Ic	IC-Ic	-Ia	IB-Ia	0	0	0	-IC
00	01	10	10	00	10	10	00	00	0	Ib	Ib-IA	IC-Ia	0	IA+Ia	-IC	0	0
00	01	10	10	00	10	00	01	00	0	Ib-IC	IB+Ib	-Ia	0	Ia-IB	0	IC	0
00	01	10	10	00	10	00	00	10	0	Ib	Ib-IA	-Ia	0	Ia-IB	0	0	-IC
00	01	10	10	00	00	10	01	00	0	IA-Ic	-Ic	-IB	0	0	IB-Ia	-IA-Ia	0
00	01	10	10	00	00	10	00	10	0	Ib	Ib-IA	-IB	0	0	IB-Ia	0	IA+Ia
00	01	10	00	01	00	10	01	00	0	IA-Ic	-Ic	0	IB	0	-Ia	IC-Ia	0
00	01	10	00	01	00	10	00	10	0	Ib-IB	IC+Ib	0	IB	0	-Ia	0	Ia-IC
00	01	10	00	00	10	10	01	00	0	-IC-Ic	IB-Ic	0	0	-IB	-Ia	IC-Ia	0
00	01	10	00	00	10	10	00	10	0	Ib	Ib-IA	0	0	-IB	-Ia	0	Ia-IC
00	01	00	10	01	10	10	00	00	0	IA	0	IC-Ia	Ib-IA	-Ic	-IC	0	0
00	01	00	10	01	10	00	01	00	0	IA	0	-Ia	IB+Ib	-Ic	0	IC	0
00	01	00	10	01	10	00	00	10	0	IA	0	-Ia	Ib-IA	IC-Ic	0	0	-IC
00	01	00	10	01	00	10	00	10	0	IA	0	IC+Ib	Ib-IA	0	Ic-IC	0	-Ic
00	01	00	10	01	00	00	01	10	0	IA	0	-Ia	IB-Ia	0	0	IC-Ic	-Ic
00	01	00	10	00	10	10	01	00	0	IA	0	Ic-IB	0	-Ic	IB+Ib	Ib-IA	0
00	01	00	10	00	10	00	01	10	0	IA	0	-Ia	0	Ia-IB	0	Ib-IA	IB+Ib
00	01	00	10	00	00	10	01	10	0	IA	0	-IB	0	0	IB-Ia	Ib-IA	-Ic
00	01	00	00	01	10	10	01	00	0	IA	0	0	IB-Ic	-Ic	-Ia	IC-Ia	0
00	01	00	00	01	10	10	00	10	0	IA	0	0	Ib-IA	IC+Ib	-Ia	0	Ia-IC
00	01	00	00	01	00	01	01	10	0	IA	0	0	IB	0	-Ia	IC+Ib	-Ic
00	01	00	00	00	10	10	01	10	0	IA	0	0	0	-IB	-Ia	Ib-IA	IB-Ic
00	00	10	10	01	10	10	00	00	0	0	-IA	IC-Ia	Ib	IA-Ic	-IC	0	0
00	00	10	10	01	10	00	01	00	0	0	-IA	-Ia	Ib-IC	IA-Ic	0	IC	0
00	00	10	10	01	10	00	00	10	0	0	-IA	-Ia	Ib	-IB-Ic	0	0	-IC
00	00	10	10	01	00	10	00	10	0	0	-IA	Ib-IB	Ib	0	IB+Ic	0	IA-Ic
00	00	10	10	01	00	00	01	10	0	0	-IA	-Ia	IB-Ia	0	0	-IB-Ic	IA-Ic
00	00	10	10	00	10	10	01	00	0	0	-IA	IC+Ic	0	IA-Ic	Ib-IC	Ib	0
00	00	10	10	00	10	00	01	10	0	0	-IA	-Ia	0	Ia-IB	0	Ib	Ib-IC
00	00	10	10	00	00	10	01	10	0	0	-IA	-IB	0	0	IB-Ia	Ib	IA-Ic
00	00	10	00	01	10	10	01	00	0	0	-IA	0	-IC-Ic	IA-Ic	-Ia	0	IC-Ia
00	00	10	00	01	10	10	00	10	0	0	-IA	0	Ib	Ib-IB	-Ia	0	Ia-IC
00	00	10	00	01	00	10	01	10	0	0	-IA	0	IB	0	-Ia	Ib-IB	IA-Ic
00	00	10	00	00	10	10	01	10	0	0	-IA	0	0	-IB	-Ia	Ib	-IC-Ic

Appendix C

VIRTEX-II PRO PROGRAMMING

This appendix documents the detailed programming of the Xilinx Virtex-II Pro. The Virtex-II Pro was designed using the Xilinx EDK and ISE development software. The Top-level configuration of the system is defined in a Microprocessor Hardware Specification (MHS) file. This file describes the hardware components and the configuration of the system including bus architecture, peripheral, processor, address space, and connectivity of the system.

Each peripheral module is implemented using three files:

1). User logic file: This file contains detailed behaviors of the peripheral module, which was implemented using the hardware description language (VHDL).
2). HDL peripheral definition file: This file is the top-level source file of the peripheral module to instantiate the bus interfaces, ports, and parameters inside the module.
3). Microprocessor Peripheral Description (MPD) file: This files list port and default connectivity of the bus interface. Parameters and default values are also listed in this file.

C.1. TOP-LEVEL CONFIGURATION

The top-level configuration of the control system in the Virtex-II Pro is described in the MHS file.

- Codes for the MHS file

```
# Parameters
 PARAMETER VERSION = 2.1.0

# Global Ports
 PORT DCMin_clk = DCMin_clk, DIR = IN, SIGIS = CLK
 PORT system_reset = system_reset, DIR = IN
 PORT ADC1_data = ADC1_data, DIR = IN, VEC = [0:11]
 PORT ADC1_otr = ADC1_otr, DIR = IN
 PORT ADC1_clk = ADC1_clk, DIR = OUT, SIGIS = CLK
 PORT ADC1_LED1 = ADC1_LED1, DIR = OUT
 PORT ADC1_LED2 = ADC1_LED2, DIR = OUT
 PORT ADC1_mux = ADC1_mux, DIR = OUT, VEC = [0:3]
 PORT ADC2_data = ADC2_data, DIR = IN, VEC = [0:11]
 PORT ADC2_otr = ADC2_otr, DIR = IN
 PORT ADC2_clk = ADC2_clk, DIR = OUT, SIGIS = CLK
 PORT ADC2_LED1 = ADC2_LED1, DIR = OUT
 PORT ADC2_LED2 = ADC2_LED2, DIR = OUT
 PORT ADC2_mux = ADC2_mux, DIR = OUT, VEC = [0:3]
 PORT data_valid = data_valid, DIR = OUT
 PORT lut_data = lut_data, DIR = OUT, VEC = [0:18]
 PORT SAa = SAa, DIR = IN, VEC = [0:1]
 PORT SAb = SAb, DIR = IN, VEC = [0:1]
 PORT SAc = SAc, DIR = IN, VEC = [0:1]
 PORT SBa = SBa, DIR = IN, VEC = [0:1]
 PORT SBb = SBb, DIR = IN, VEC = [0:1]
 PORT SBc = SBc, DIR = IN, VEC = [0:1]
```

```
 PORT SCa = SCa, DIR = IN, VEC = [0:1]
 PORT SCb = SCb, DIR = IN, VEC = [0:1]
 PORT SCc = SCc, DIR = IN, VEC = [0:1]
 PORT SAa_out = SAa_out, DIR = OUT, VEC = [0:3]
 PORT SAb_out = SAb_out, DIR = OUT, VEC = [0:3]
 PORT SAc_out = SAc_out, DIR = OUT, VEC = [0:3]
 PORT SBa_out = SBa_out, DIR = OUT, VEC = [0:3]
 PORT SBb_out = SBb_out, DIR = OUT, VEC = [0:3]
 PORT SBc_out = SBc_out, DIR = OUT, VEC = [0:3]
 PORT SCa_out = SCa_out, DIR = OUT, VEC = [0:3]
 PORT SCb_out = SCb_out, DIR = OUT, VEC = [0:3]
 PORT SCc_out = SCc_out, DIR = OUT, VEC = [0:3]
 PORT data = data, DIR = OUT, VEC = [0:12]
 PORT ADC_temp1 = ADC_temp1, DIR = OUT

BEGIN ppc405
 PARAMETER INSTANCE = ppc405_i
 PARAMETER HW_VER = 2.00.c
 BUS_INTERFACE DPLB = plb
 BUS_INTERFACE IPLB = plb
 BUS_INTERFACE JTAGPPC = jtagppc_0_0
 PORT PLBCLK = bus_clk
 PORT C405RSTCHIPRESETREQ = C405RSTCHIPRESETREQ
 PORT C405RSTCORERESETREQ = C405RSTCORERESETREQ
 PORT C405RSTSYSRESETREQ = C405RSTSYSRESETREQ
 PORT RSTC405RESETCHIP = RSTC405RESETCHIP
 PORT RSTC405RESETCORE = RSTC405RESETCORE
 PORT RSTC405RESETSYS = RSTC405RESETSYS
 PORT BRAMISOCMCLK = bus_clk
 PORT BRAMDSOCMCLK = bus_clk
 PORT EICC405EXTINPUTIRQ = net_gnd
 PORT CPMC405CLOCK = PPC_clk
END

BEGIN jtagppc_cntlr
 PARAMETER INSTANCE = JTAG_CNTL
 PARAMETER HW_VER = 2.00.a
 BUS_INTERFACE JTAGPPC0 = jtagppc_0_0
END

BEGIN proc_sys_reset
 PARAMETER INSTANCE = reset_block
 PARAMETER HW_VER = 1.00.a
 PARAMETER C_EXT_RST_WIDTH = 20
 PARAMETER C_EXT_RESET_HIGH = 0
 PORT Slowest_sync_clk = bus_clk
 PORT Ext_Reset_In = system_reset
 PORT Chip_Reset_Req = C405RSTCHIPRESETREQ
 PORT Core_Reset_Req = C405RSTCORERESETREQ
 PORT System_Reset_Req = C405RSTSYSRESETREQ
 PORT Rstc405resetchip = RSTC405RESETCHIP
 PORT Rstc405resetcore = RSTC405RESETCORE
 PORT Rstc405resetsys = RSTC405RESETSYS
 PORT Bus_Struct_Reset = sys_bus_reset
 PORT Dcm_locked = net_vcc
END
```

```
BEGIN plb_v34
 PARAMETER INSTANCE = plb
 PARAMETER HW_VER = 1.01.a
 PARAMETER C_DCR_INTFCE = 0
 PORT PLB_Clk = bus_clk
 PORT SYS_Rst = sys_bus_reset
 PORT M_busLock = net_gnd
END

BEGIN opb_v20
 PARAMETER INSTANCE = opb
 PARAMETER HW_VER = 1.10.c
 PORT OPB_Clk = bus_clk
 PORT SYS_Rst = sys_bus_reset
END

BEGIN plb2opb_bridge
 PARAMETER INSTANCE = plb2opb
 PARAMETER HW_VER = 1.00.b
 PARAMETER C_NUM_ADDR_RNG = 1
 PARAMETER C_CLK_ASYNC = 0
 PARAMETER C_DCR_INTFCE = 0
 PARAMETER C_RNG0_BASEADDR = 0xF0000000
 PARAMETER C_RNG0_HIGHADDR = 0xF7FFFFFF
 BUS_INTERFACE SPLB = plb
 BUS_INTERFACE MOPB = opb
 PORT PLB_Clk = bus_clk
 PORT OPB_Clk = bus_clk
END

BEGIN plb_bram_if_cntlr
 PARAMETER INSTANCE = plb_bram_if_ctrlr_1
 PARAMETER HW_VER = 1.00.b
 PARAMETER c_plb_clk_period_ps = 10000
 PARAMETER C_BASEADDR = 0xFFFF8000
 PARAMETER C_HIGHADDR = 0xFFFFFFFF
 BUS_INTERFACE PORTA = porta
 BUS_INTERFACE SPLB = plb
 PORT PLB_Clk = bus_clk
END

BEGIN bram_block
 PARAMETER INSTANCE = bram
 PARAMETER HW_VER = 1.00.a
 BUS_INTERFACE PORTA = porta
END

BEGIN dcm_module
 PARAMETER INSTANCE = dcm_module_1
 PARAMETER HW_VER = 1.00.a
 PARAMETER C_CLK_FEEDback = 1X
 PARAMETER C_CLKFX_MULTIPLY = 3
 PARAMETER C_CLKFX_DIVIDE = 1
 PARAMETER C_CLKDV_DIVIDE = 2.0
 PARAMETER C_CLKIN_BUF = TRUE
 PARAMETER C_CLK0_BUF = TRUE
 PARAMETER C_CLKIN_PERIOD = 10.0
```

```
 PARAMETER C_EXT_RESET_HIGH = 1
 PORT CLKIN = DCMin_clk
 PORT CLKFX = PPC_clk
 PORT CLKDV = bus_clk
 PORT CLK0 = CLK_100MHz_1
 PORT CLKFB = CLK_100MHz_1
 PORT RST = net_gnd
END

BEGIN dcm_module
 PARAMETER INSTANCE = dcm_module_2
 PARAMETER HW_VER = 1.00.a
 PARAMETER C_CLK_FEEDback = 1X
 PARAMETER C_CLKDV_DIVIDE = 13.0
 PARAMETER C_CLKIN_BUF = TRUE
 PARAMETER C_CLK0_BUF = TRUE
 PARAMETER C_CLKIN_PERIOD = 10.0
 PARAMETER C_EXT_RESET_HIGH = 1
 PORT CLKDV = CLK_ADC
 PORT CLKIN = DCMin_clk
 PORT CLK0 = CLK_100MHz_2
 PORT CLKFB = CLK_100MHz_2
 PORT RST = net_gnd
END

BEGIN dcm_module
 PARAMETER INSTANCE = dcm_module_3
 PARAMETER HW_VER = 1.00.a
 PARAMETER C_CLK_FEEDback = 1X
 PARAMETER C_CLKDV_DIVIDE = 5.0
 PARAMETER C_CLKIN_BUF = TRUE
 PARAMETER C_CLK0_BUF = TRUE
 PARAMETER C_CLKIN_PERIOD = 10.0
 PARAMETER C_EXT_RESET_HIGH = 1
 PORT CLKDV = CLK_PWM
 PORT CLKIN = DCMin_clk
 PORT CLK0 = CLK_100MHz_3
 PORT CLKFB = CLK_100MHz_3
 PORT RST = net_gnd
END

BEGIN adc1_opb
 PARAMETER INSTANCE = adc1_opb_1
 PARAMETER HW_VER = 1.00.a
 PARAMETER C_BASEADDR = 0xF0000500
 PARAMETER C_HIGHADDR = 0xF00005FF
 BUS_INTERFACE SOPB = opb
 PORT ADC1_data = ADC1_data
 PORT ADC1_otr = ADC1_otr
 PORT ADC1_en = enable
 PORT CLK_ADC = CLK_ADC
 PORT ADC1_clk = ADC1_clk
 PORT ADC1_LED1 = ADC1_LED1
 PORT ADC1_LED2 = ADC1_LED2
 PORT ADC1_mux = ADC1_mux
 PORT ADC1_temp1 = ADC_temp1
 PORT ADC1_temp2 = data
```

```
 PORT Iin_A = Iin_A
 PORT Iin_B = Iin_B
 PORT Iin_C = Iin_C
 PORT Iout_a = Iout_a
 PORT Iout_b = Iout_b
 PORT Iout_c = Iout_c
END

BEGIN ADC2_OPB
 PARAMETER INSTANCE = ADC2_OPB_0
 PARAMETER HW_VER = 1.00.a
 PARAMETER C_BASEADDR = 0xF0000600
 PARAMETER C_HIGHADDR = 0xF00006FF
 BUS_INTERFACE SOPB = opb
 PORT ADC2_data = ADC2_data
 PORT ADC2_otr = ADC2_otr
 PORT ADC2_en = enable
 PORT CLK_ADC = CLK_ADC
 PORT ADC2_clk = ADC2_clk
 PORT ADC2_LED1 = ADC2_LED1
 PORT ADC2_LED2 = ADC2_LED2
 PORT ADC2_mux = ADC2_mux
 PORT ADC2_temp1 = ADC2_temp1
 PORT ADC2_temp2 = data2
END

BEGIN cap_reg
 PARAMETER INSTANCE = cap_reg_1
 PARAMETER C_BASEADDR = 0xF8000100
 PARAMETER C_HIGHADDR = 0xF80001FF
 BUS_INTERFACE SPLB = plb
 PORT Iin_A = Iin_A
 PORT Iin_B = Iin_B
 PORT Iin_C = Iin_C
 PORT Iout_a = Iout_a
 PORT Iout_b = Iout_b
 PORT Iout_c = Iout_c
END

BEGIN pwm
 PARAMETER INSTANCE = pwm_1
 PARAMETER C_BASEADDR = 0xF0000700
 PARAMETER C_HIGHADDR = 0xF00007FF
 BUS_INTERFACE SOPB = opb
 PORT CLK_PWM = CLK_PWM
 PORT enable = enable
 PORT data_valid = data_valid
 PORT lut_data = lut_data
 PORT switch_on = switch_on
 PORT switch_off = switch_off
END

BEGIN sw_ctrl
 PARAMETER INSTANCE = sw_ctrl_Aa
 PORT SS = SAa
 PORT switch_on = switch_on
 PORT switch_off = switch_off
```

```
 PORT S_out = SAa_out
END

BEGIN sw_ctrl
 PARAMETER INSTANCE = sw_ctrl_Ab
 PORT SS = SAb
 PORT switch_on = switch_on
 PORT switch_off = switch_off
 PORT S_out = SAb_out
END

BEGIN sw_ctrl
 PARAMETER INSTANCE = sw_ctrl_Ac
 PORT SS = SAc
 PORT switch_on = switch_on
 PORT switch_off = switch_off
 PORT S_out = SAc_out
END

BEGIN sw_ctrl
 PARAMETER INSTANCE = sw_ctrl_Ba
 PORT SS = SBa
 PORT switch_on = switch_on
 PORT switch_off = switch_off
 PORT S_out = SBa_out
END

BEGIN sw_ctrl
 PARAMETER INSTANCE = sw_ctrl_Bb
 PORT SS = SBb
 PORT switch_on = switch_on
 PORT switch_off = switch_off
 PORT S_out = SBb_out
END

BEGIN sw_ctrl
 PARAMETER INSTANCE = sw_ctrl_Bc
 PORT SS = SBc
 PORT switch_on = switch_on
 PORT switch_off = switch_off
 PORT S_out = SBc_out
END

BEGIN sw_ctrl
 PARAMETER INSTANCE = sw_ctrl_Ca
 PORT SS = SCa
 PORT switch_on = switch_on
 PORT switch_off = switch_off
 PORT S_out = SCa_out
END

BEGIN sw_ctrl
 PARAMETER INSTANCE = sw_ctrl_Cb
 PORT SS = SCb
 PORT switch_on = switch_on
 PORT switch_off = switch_off
 PORT S_out = SCb_out
```

```
END

BEGIN sw_ctrl
 PARAMETER INSTANCE = sw_ctrl_Cc
 PORT SS = SCc
 PORT switch_on = switch_on
 PORT switch_off = switch_off
 PORT S_out = SCc_out
END
```

C.2. ADC1_OPB

The ADC1_OPB module is an ADC controller circuit that samples the ac signals, line-line voltages and currents, of the multilevel matrix converter.

- Codes for the user logic file

```
------------------------------------------------------------------
-- user_logic.vhd - entity/architecture pair
------------------------------------------------------------------
-- Filename:          user_logic.vhd
-- Version:           1.00.a
-- Description:       User logic.
-- Date:              Wed Sep 21 16:43:25 2005
                        (by Create and Import Peripheral Wizard)
-- VHDL Standard:     VHDL'93
------------------------------------------------------------------
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;
use ieee.std_logic_unsigned.all;

library proc_common_v2_00_a;
use proc_common_v2_00_a.proc_common_pkg.all;

------------------------------------------------------------------
-- Entity section
------------------------------------------------------------------

entity user_logic is
  generic
    (
      ADC_DWIDTH : integer := 12;
      -- Bus protocol parameters, do not add to or delete
      C_DWIDTH : integer := 16;
      C_NUM_CE : integer := 10
    );
  port
    (
      ADC1_data  : in  std_logic_vector(0 to (ADC_DWIDTH-1));
      ADC1_otr   : in  std_logic;
      ADC1_en    : in  std_logic;
      CLK_ADC    : in  std_logic;
      ADC1_clk   : out std_logic;
```

```
      ADC1_LED1  : out std_logic;
      ADC1_LED2  : out std_logic;
      ADC1_mux   : out std_logic_vector(0 to 3);
      ADC1_temp1 : out std_logic;
      ADC1_temp2 : out std_logic_vector(0 to 12);
      Iin_A  : out std_logic_vector(0 to C_DWIDTH-1);
      Iin_B  : out std_logic_vector(0 to C_DWIDTH-1);
      Iin_C  : out std_logic_vector(0 to C_DWIDTH-1);
      Iout_a : out std_logic_vector(0 to C_DWIDTH-1);
      Iout_b : out std_logic_vector(0 to C_DWIDTH-1);
      Iout_c : out std_logic_vector(0 to C_DWIDTH-1);
      -- Bus protocol ports, do not add to or delete
      Bus2IP_Clk     : in  std_logic;
      Bus2IP_Reset   : in  std_logic;
      Bus2IP_Data    : in  std_logic_vector(0 to C_DWIDTH-1);
      Bus2IP_BE      : in  std_logic_vector(0 to C_DWIDTH/8-1);
      Bus2IP_RdCE    : in  std_logic_vector(0 to C_NUM_CE-1);
      Bus2IP_WrCE    : in  std_logic_vector(0 to C_NUM_CE-1);
      IP2Bus_Data    : out std_logic_vector(0 to C_DWIDTH-1);
      IP2Bus_Ack     : out std_logic;
      IP2Bus_Retry   : out std_logic;
      IP2Bus_Error   : out std_logic;
      IP2Bus_ToutSup : out std_logic
     );
end entity user_logic;

------------------------------------------------------------------------
-- Architecture section
------------------------------------------------------------------------

architecture IMP of user_logic is

  ---------------------------------------------
  -- Signals for user logic slave model s/w accessible register
  -- example
  ---------------------------------------------
  signal slv_reg0 : std_logic_vector(0 to C_DWIDTH-1);
  signal slv_reg1 : std_logic_vector(0 to C_DWIDTH-1);
  signal slv_reg2 : std_logic_vector(0 to C_DWIDTH-1);
  signal slv_reg3 : std_logic_vector(0 to C_DWIDTH-1);
  signal slv_reg4 : std_logic_vector(0 to C_DWIDTH-1);
  signal slv_reg5 : std_logic_vector(0 to C_DWIDTH-1);
  signal slv_reg6 : std_logic_vector(0 to C_DWIDTH-1);
  signal slv_reg7 : std_logic_vector(0 to C_DWIDTH-1);
  signal slv_reg8 : std_logic_vector(0 to C_DWIDTH-1);
  signal slv_reg9 : std_logic_vector(0 to C_DWIDTH-1);
  signal slv_reg_write_select : std_logic_vector(0 to 9);
  signal slv_reg_read_select  : std_logic_vector(0 to 9);
  signal slv_ip2bus_data : std_logic_vector(0 to C_DWIDTH-1);
  signal slv_read_ack  : std_logic;
  signal slv_write_ack : std_logic;
  signal temp1,temp2 : std_logic_vector(0 to ADC_DWIDTH-1);
  signal temp3,temp4 : std_logic_vector(0 to ADC_DWIDTH-1);
  signal temp  : std_logic_vector(0 to C_DWIDTH-1);
  signal temp5 : std_logic_vector( 0 to 13);
  signal count,next_count : integer range 0 to 16;
  signal temp_ADC1_mux,next_ADC1_mux : std_logic_vector(0 to 3);
```

```
  signal Vi_AB,Vi_BC : std_logic_vector(0 to C_DWIDTH-1);
  signal Vo_ab,Vo_bc : std_logic_vector(0 to C_DWIDTH-1);
  signal Ii_A,Ii_B,Ii_C : std_logic_vector(0 to C_DWIDTH-1);
  signal Io_a,Io_b,Io_c : std_logic_vector(0 to C_DWIDTH-1);

begin

  slv_reg_write_select <= Bus2IP_WrCE(0 to 9);
  slv_reg_read_select  <= Bus2IP_RdCE(0 to 9);
  slv_write_ack        <= Bus2IP_WrCE(0) or Bus2IP_WrCE(1) or
                          Bus2IP_WrCE(2) or Bus2IP_WrCE(3) or
                          Bus2IP_WrCE(4) or Bus2IP_WrCE(5) or
                          Bus2IP_WrCE(6) or Bus2IP_WrCE(7) or
                          Bus2IP_WrCE(8) or Bus2IP_WrCE(9);
  slv_read_ack         <= Bus2IP_RdCE(0) or Bus2IP_RdCE(1) or
                          Bus2IP_RdCE(2) or Bus2IP_RdCE(3) or
                          Bus2IP_RdCE(4) or Bus2IP_RdCE(5) or
                          Bus2IP_RdCE(6) or Bus2IP_RdCE(7) or
                          Bus2IP_RdCE(8) or Bus2IP_RdCE(9);

  SLAVE_REG_READ_PROC : process( slv_reg_read_select, slv_reg0,
                                 slv_reg1, slv_reg2, slv_reg3,
                                 slv_reg4, slv_reg5, slv_reg6,
                                 slv_reg7, slv_reg8, slv_reg9 ) is
  begin
    case slv_reg_read_select is
      when "1000000000" => slv_ip2bus_data <= slv_reg0;
      when "0100000000" => slv_ip2bus_data <= slv_reg1;
      when "0010000000" => slv_ip2bus_data <= slv_reg2;
      when "0001000000" => slv_ip2bus_data <= slv_reg3;
      when "0000100000" => slv_ip2bus_data <= slv_reg4;
      when "0000010000" => slv_ip2bus_data <= slv_reg5;
      when "0000001000" => slv_ip2bus_data <= slv_reg6;
      when "0000000100" => slv_ip2bus_data <= slv_reg7;
      when "0000000010" => slv_ip2bus_data <= slv_reg8;
      when "0000000001" => slv_ip2bus_data <= slv_reg9;
      when others => slv_ip2bus_data <= (others => '0');
    end case;

  end process SLAVE_REG_READ_PROC;

  ----------------------------------------
  -- Example code to drive IP to Bus signals
  ----------------------------------------
  IP2Bus_Data        <= slv_ip2bus_data;
  IP2Bus_Ack         <= slv_write_ack or slv_read_ack;
  IP2Bus_Error       <= '0';
  IP2Bus_Retry       <= '0';
  IP2Bus_ToutSup     <= '0';

  process(CLK_ADC,Bus2IP_Reset,ADC1_en)
  begin
    if (Bus2IP_Reset = '1' OR ADC1_en = '0') then
      count <= 0;
    elsif (CLK_ADC'event AND CLK_ADC = '1') then
      count <= next_count;
    end if;
```

```
end process;

process(count)
begin
  next_count <= 0;
  case count is
    when 0 to 15 =>
      next_count <= count + 1;
    when 16 =>
      next_count <= 0;
    when others =>
  end case;
end process;

process(CLK_ADC,Bus2IP_reset)
begin
  if (Bus2IP_Reset = '1') then
    temp_ADC1_mux <= "0000";
  elsif (CLK_ADC'event and CLK_ADC = '1') then
    if(count = 16) then
      temp_ADC1_mux <= next_ADC1_mux;
    end if;
  end if;
end process;

process(temp_ADC1_mux)
begin
  next_ADC1_mux <= "0000";
  case temp_ADC1_mux is
    when "0000" =>
      next_ADC1_mux <= "1000";
    when "1000" =>
      next_ADC1_mux <= "0001";
    when "0001" =>
      next_ADC1_mux <= "1001";
    when "1001" =>
      next_ADC1_mux <= "0101";
    when "0101" =>
      next_ADC1_mux <= "1101";
    when "1101" =>
      next_ADC1_mux <= "0011";
    when "0011" =>
      next_ADC1_mux <= "1011";
    when "1011" =>
      next_ADC1_mux <= "0111";
    when "0111" =>
      next_ADC1_mux <= "1111";
    when "1111" =>
      next_ADC1_mux <= "0000";
    when others =>
  end case;
end process;

process(CLK_ADC)
begin
  if (CLK_ADC'event and CLK_ADC = '0') then
    if (count = 10) then
```

```
        temp1 <= (ADC1_data);
      elsif (count = 11) then
        temp2 <= (ADC1_data);
      elsif (count = 12) then
        temp3 <= (ADC1_data);
      elsif (count = 13) then
        temp4 <= (ADC1_data);
      elsif (count = 15) then
        case temp_ADC1_mux is
          when "0000" => Vi_BC <= temp - x"07F7";
          when "1000" => Ii_C <= temp - x"07F4";
          when "0001" => Ii_B <= temp - x"07F2";
          when "1001" => Vi_AB <= temp - x"07F5";
          when "0101" => Ii_A <= temp - x"07F4";
          when "1101" => Io_a <= temp - x"07F2";
          when "0011" => Vo_ab <= temp - x"07F8";
          when "1011" => Io_b <= temp - x"07F2";
          when "0111" => Vo_bc <= temp - x"07F7";
          when "1111" => Io_c <= temp - x"07F4";
          when others =>
        end case;
      end if;
    end if;
end process;

-------------------------------------------------------------------
------ Calculating the average of four sampling data -----

temp5 <= (("00" & temp1) + ("00" & temp2) +
          ("00" & temp3) + ("00" & temp4));
temp <= ("0000" & temp5(0 to 11));

-------------------------------------------------------------------

process(Bus2IP_Clk)
begin
  if(Bus2IP_Clk'event and Bus2IP_Clk = '1') then
    slv_reg0 <= Vi_AB;
    slv_reg1 <= Vi_BC;
    slv_reg2 <= Vo_ab;
    slv_reg3 <= Vo_bc;
    slv_reg4 <= Ii_A;
    slv_reg5 <= Ii_B;
    slv_reg6 <= Ii_C;
    slv_reg7 <= Io_a;
    slv_reg8 <= Io_b;
    slv_reg9 <= Io_c;
    Iin_A <= Ii_A;
    Iin_B <= Ii_B;
    Iin_C <= Ii_C;
    Iout_a <= Io_a;
    Iout_b <= Io_b;
    Iout_c <= Io_c;
  end if;
end process;

ADC1_clk <= CLK_ADC;-- when ADC1_en = '1' else '0';
```

```
ADC1_LED1 <= ADC1_otr;
ADC1_LED2 <= '1';--ADC1_en;
ADC1_mux <= temp_ADC1_mux;
ADC1_temp1 <= '1' when (count = 15) else '0';
ADC1_temp2 <= (ADC1_otr & temp(4 to 15));

end IMP;
```

- Codes for the HDL peripheral definition file

```
------------------------------------------------------------------------------
-- adc1_opb.vhd - entity/architecture pair
------------------------------------------------------------------------------
-- Filename:          adc1_opb.vhd
-- Version:           1.00.a
-- Description:       Top level design,
--                      instantiates IPIF and user logic.
-- Date:              Wed Sep 21 16:43:25 2005
--                      (by Create and Import Peripheral Wizard)
-- VHDL Standard:     VHDL'93
------------------------------------------------------------------------------
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;
use ieee.std_logic_unsigned.all;

library proc_common_v2_00_a;
use proc_common_v2_00_a.proc_common_pkg.all;
use proc_common_v2_00_a.ipif_pkg.all;
library opb_ipif_v3_01_a;
use opb_ipif_v3_01_a.all;

library adc1_opb_v1_00_a;
use adc1_opb_v1_00_a.all;

------------------------------------------------------------------------------
-- Entity section
------------------------------------------------------------------------------
entity adc1_opb is
  generic
  (
     -- Bus protocol parameters, do not add to or delete
    C_BASEADDR   : std_logic_vector := X"00000000";
    C_HIGHADDR   : std_logic_vector := X"0000FFFF";
    C_OPB_AWIDTH : integer := 32;
    C_OPB_DWIDTH : integer := 32;
    C_FAMILY     : string  := "virtex2p"
  );
  port
  (
    ADC1_data  : in std_logic_vector(0 to 11);
    ADC1_otr   : in std_logic;
    ADC1_en    : in std_logic;
    CLK_ADC    : in std_logic;
    ADC1_clk   : out std_logic;
    ADC1_LED1  : out std_logic;
```

```
    ADC1_LED2  : out std_logic;
    ADC1_mux   : out std_logic_vector(0 to 3);
    ADC1_temp1 : out std_logic;
    ADC1_temp2 : out std_logic_vector(0 to 12);
    Iin_A,Iin_B,Iin_C : out std_logic_vector(0 to 15);
    Iout_a,Iout_b,Iout_c : out std_logic_vector(0 to 15);

    -- Bus protocol ports, do not add to or delete
    OPB_Clk     : in  std_logic;
    OPB_Rst     : in  std_logic;
    Sl_DBus     : out std_logic_vector(0 to C_OPB_DWIDTH-1);
    Sl_errAck   : out std_logic;
    Sl_retry    : out std_logic;
    Sl_toutSup  : out std_logic;
    Sl_xferAck  : out std_logic;
    OPB_ABus    : in  std_logic_vector(0 to C_OPB_AWIDTH-1);
    OPB_BE      : in  std_logic_vector(0 to C_OPB_DWIDTH/8-1);
    OPB_DBus    : in  std_logic_vector(0 to C_OPB_DWIDTH-1);
    OPB_RNW     : in  std_logic;
    OPB_select  : in  std_logic;
    OPB_seqAddr : in  std_logic
  );

  attribute SIGIS : string;
  attribute SIGIS of OPB_Clk : signal is "Clk";
  attribute SIGIS of OPB_Rst : signal is "Rst";

end entity adc1_opb;

------------------------------------------------------------------------
-- Architecture section
------------------------------------------------------------------------

architecture IMP of adc1_opb is

  ---------------------------------------------
  -- Constant: array of address range identifiers
  ---------------------------------------------
  constant ARD_ID_ARRAY : INTEGER_ARRAY_TYPE :=
    (
      0  => USER_00 -- user logic S/W register address space
    );

  ---------------------------------------------
  -- Constant: array of address pairs for each address range
  ---------------------------------------------
  constant ZERO_ADDR_PAD: std_logic_vector(0 to 64-C_OPB_AWIDTH-1)
                          := (others => '0');

  constant USER_BASEADDR : std_logic_vector := C_BASEADDR;
  constant USER_HIGHADDR : std_logic_vector := C_HIGHADDR;

  constant ARD_ADDR_RANGE_ARRAY : SLV64_ARRAY_TYPE  :=
    (
      ZERO_ADDR_PAD & USER_BASEADDR, -- user logic base address
      ZERO_ADDR_PAD & USER_HIGHADDR  -- user logic high address
    );
```

```
---------------------------------------
-- Constant: array of data widths for each target address range
---------------------------------------
constant USER_DWIDTH  : integer := 16;

constant ARD_DWIDTH_ARRAY : INTEGER_ARRAY_TYPE :=
  (
    0  => USER_DWIDTH -- user logic data width
  );

---------------------------------------
-- Constant: array of desired number of chip enables
--            for each address range
---------------------------------------
constant USER_NUM_CE      : integer := 10;

constant ARD_NUM_CE_ARRAY : INTEGER_ARRAY_TYPE :=
  (
    0  => pad_power2(USER_NUM_CE)  -- user logic number of CEs
  );

---------------------------------------
-- Constant: array of unique properties for each address range
---------------------------------------
constant ARD_DEPENDENT_PROPS_ARRAY:DEPENDENT_PROPS_ARRAY_TYPE :=
  (
    0  => (others => 0)
   -- user logic slave space dependent properties (none defined)
  );

---------------------------------------
constant PIPELINE_MODEL : integer := 5;

---------------------------------------
-- Constant: user core ID code
---------------------------------------
constant DEV_BLK_ID : integer := 0;

---------------------------------------
-- Constant: enable MIR/Reset register
---------------------------------------
constant DEV_MIR_ENABLE : integer := 0;

---------------------------------------
constant IP_INTR_MODE_ARRAY : INTEGER_ARRAY_TYPE   :=
  (
    0  => 0  -- not used
  );

---------------------------------------
-- Constant: enable device burst
---------------------------------------
constant DEV_BURST_ENABLE : integer := 0;

---------------------------------------
-- Constant: include address counter for burst transfers
```

```
------------------------------------------
constant INCLUDE_ADDR_CNTR : integer := 0;

------------------------------------------
-- Constant: include write buffer that decouples OPB and
--           IPIC write transactions
------------------------------------------
constant INCLUDE_WR_BUF : integer := 0;

------------------------------------------
-- Constant: index for CS/CE
------------------------------------------
constant USER00_CS_INDEX : integer :=
                           get_id_index(ARD_ID_ARRAY, USER_00);

constant USER00_CE_INDEX : integer :=
       calc_start_ce_index(ARD_NUM_CE_ARRAY, USER00_CS_INDEX);

------------------------------------------
-- IP Interconnect (IPIC) signal declarations -- do not delete
-- prefix 'i' stands for IPIF while prefix 'u' stands for user
-- logic typically user logic will be hooked up to IPIF
-- directly via i<sig> unless signal slicing and muxing are
-- needed via u<sig>
------------------------------------------
signal iBus2IP_RdCE :
       std_logic_vector(0 to calc_num_ce(ARD_NUM_CE_ARRAY)-1);
signal iBus2IP_WrCE :
       std_logic_vector(0 to calc_num_ce(ARD_NUM_CE_ARRAY)-1);
signal iBus2IP_Data : std_logic_vector(0 to C_OPB_DWIDTH-1);
signal iBus2IP_BE   : std_logic_vector(0 to C_OPB_DWIDTH/8-1);
signal iIP2Bus_Data : std_logic_vector(0 to C_OPB_DWIDTH-1)
                              := (others => '0');
signal iIP2Bus_Ack     : std_logic   := '0';
signal iIP2Bus_Error   : std_logic   := '0';
signal iIP2Bus_Retry   : std_logic   := '0';
signal iIP2Bus_ToutSup : std_logic   := '0';
signal ZERO_IP2Bus_PostedWrInh :
          std_logic_vector(0 to ARD_ID_ARRAY'length-1)
               := (others => '0');
signal ZERO_IP2RFIFO_Data : std_logic_vector(0 to
     ARD_DWIDTH_ARRAY(get_id_index_iboe(ARD_ID_ARRAY,
            IPIF_RDFIFO_DATA))-1)   := (others => '0');
signal ZERO_WFIFO2IP_Data : std_logic_vector(0 to
     ARD_DWIDTH_ARRAY(get_id_index_iboe(ARD_ID_ARRAY,
            IPIF_WRFIFO_DATA))-1)   := (others => '0');
signal ZERO_IP2Bus_IntrEvent :
          std_logic_vector(0 to IP_INTR_MODE_ARRAY'length-1)
               := (others => '0');
signal iBus2IP_Clk   : std_logic;
signal iBus2IP_Reset : std_logic;
signal uBus2IP_Data  : std_logic_vector(0 to USER_DWIDTH-1);
signal uBus2IP_BE    : std_logic_vector(0 to USER_DWIDTH/8-1);
signal uBus2IP_RdCE  : std_logic_vector(0 to USER_NUM_CE-1);
signal uBus2IP_WrCE  : std_logic_vector(0 to USER_NUM_CE-1);
signal uIP2Bus_Data  : std_logic_vector(0 to USER_DWIDTH-1);
```

```
begin

  ---------------------------------------
  -- instantiate the OPB IPIF
  ---------------------------------------
  OPB_IPIF_I : entity opb_ipif_v3_01_a.opb_ipif
    generic map
    (
      C_ARD_ID_ARRAY              => ARD_ID_ARRAY,
      C_ARD_ADDR_RANGE_ARRAY      => ARD_ADDR_RANGE_ARRAY,
      C_ARD_DWIDTH_ARRAY          => ARD_DWIDTH_ARRAY,
      C_ARD_NUM_CE_ARRAY          => ARD_NUM_CE_ARRAY,
      C_ARD_DEPENDENT_PROPS_ARRAY => ARD_DEPENDENT_PROPS_ARRAY,
      C_PIPELINE_MODEL            => PIPELINE_MODEL,
      C_DEV_BLK_ID                => DEV_BLK_ID,
      C_DEV_MIR_ENABLE            => DEV_MIR_ENABLE,
      C_OPB_AWIDTH                => C_OPB_AWIDTH,
      C_OPB_DWIDTH                => C_OPB_DWIDTH,
      C_FAMILY                    => C_FAMILY,
      C_IP_INTR_MODE_ARRAY        => IP_INTR_MODE_ARRAY,
      C_DEV_BURST_ENABLE          => DEV_BURST_ENABLE,
      C_INCLUDE_ADDR_CNTR         => INCLUDE_ADDR_CNTR,
      C_INCLUDE_WR_BUF            => INCLUDE_WR_BUF
    )
    port map
    (
      OPB_select           => OPB_select,
      OPB_DBus             => OPB_DBus,
      OPB_ABus             => OPB_ABus,
      OPB_BE               => OPB_BE,
      OPB_RNW              => OPB_RNW,
      OPB_seqAddr          => OPB_seqAddr,
      Sln_DBus             => Sl_DBus,
      Sln_xferAck          => Sl_xferAck,
      Sln_errAck           => Sl_errAck,
      Sln_retry            => Sl_retry,
      Sln_toutSup          => Sl_toutSup,
      Bus2IP_CS            => open,
      Bus2IP_CE            => open,
      Bus2IP_RdCE          => iBus2IP_RdCE,
      Bus2IP_WrCE          => iBus2IP_WrCE,
      Bus2IP_Data          => iBus2IP_Data,
      Bus2IP_Addr          => open,
      Bus2IP_AddrValid     => open,
      Bus2IP_BE            => iBus2IP_BE,
      Bus2IP_RNW           => open,
      Bus2IP_Burst         => open,
      IP2Bus_Data          => iIP2Bus_Data,
      IP2Bus_Ack           => iIP2Bus_Ack,
      IP2Bus_AddrAck       => '0',
      IP2Bus_Error         => iIP2Bus_Error,
      IP2Bus_Retry         => iIP2Bus_Retry,
      IP2Bus_ToutSup       => iIP2Bus_ToutSup,
      IP2Bus_PostedWrInh   => ZERO_IP2Bus_PostedWrInh,
      IP2RFIFO_Data        => ZERO_IP2RFIFO_Data,
      IP2RFIFO_WrMark      => '0',
      IP2RFIFO_WrRelease   => '0',
```

```
    IP2RFIFO_WrReq       => '0',
    IP2RFIFO_WrRestore   => '0',
    RFIFO2IP_AlmostFull  => open,
    RFIFO2IP_Full        => open,
    RFIFO2IP_Vacancy     => open,
    RFIFO2IP_WrAck       => open,
    IP2WFIFO_RdMark      => '0',
    IP2WFIFO_RdRelease   => '0',
    IP2WFIFO_RdReq       => '0',
    IP2WFIFO_RdRestore   => '0',
    WFIFO2IP_AlmostEmpty => open,
    WFIFO2IP_Data        => ZERO_WFIFO2IP_Data,
    WFIFO2IP_Empty       => open,
    WFIFO2IP_Occupancy   => open,
    WFIFO2IP_RdAck       => open,
    IP2Bus_IntrEvent     => ZERO_IP2Bus_IntrEvent,
    IP2INTC_Irpt         => open,
    Freeze               => '0',
    Bus2IP_Freeze        => open,
    OPB_Clk              => OPB_Clk,
    Bus2IP_Clk           => iBus2IP_Clk,
    IP2Bus_Clk           => '0',
    Reset                => OPB_Rst,
    Bus2IP_Reset         => iBus2IP_Reset
  );

------------------------------------------
-- instantiate the User Logic
------------------------------------------
USER_LOGIC_I : entity adc1_opb_v1_00_a.user_logic
  generic map
  (
    C_DWIDTH  => USER_DWIDTH,
    C_NUM_CE  => USER_NUM_CE
  )
  port map
  (
    ADC1_data         => ADC1_data,
    ADC1_otr          => ADC1_otr,
    ADC1_en           => ADC1_en,
    CLK_ADC           => CLK_ADC,
    ADC1_clk          => ADC1_clk,
    ADC1_LED1         => ADC1_LED1,
    ADC1_LED2         => ADC1_LED2,
    ADC1_mux          => ADC1_mux,
    ADC1_temp1        => ADC1_temp1,
    ADC1_temp2        => ADC1_temp2,
    Iin_A             => Iin_A,
    Iin_B             => Iin_B,
    Iin_C             => Iin_C,
    Iout_a            => Iout_a,
    Iout_b            => Iout_b,
    Iout_c            => Iout_c,
    Bus2IP_Clk        => iBus2IP_Clk,
    Bus2IP_Reset      => iBus2IP_Reset,
    Bus2IP_Data       => uBus2IP_Data,
    Bus2IP_BE         => uBus2IP_BE,
```

```
      Bus2IP_RdCE       => uBus2IP_RdCE,
      Bus2IP_WrCE       => uBus2IP_WrCE,
      IP2Bus_Data       => uIP2Bus_Data,
      IP2Bus_Ack        => iIP2Bus_Ack,
      IP2Bus_Retry      => iIP2Bus_Retry,
      IP2Bus_Error      => iIP2Bus_Error,
      IP2Bus_ToutSup    => iIP2Bus_ToutSup
    );

  ----------------------------------------
  -- hooking up signal slicing
  ----------------------------------------
  uBus2IP_BE <= iBus2IP_BE(0 to USER_DWIDTH/8-1);
  uBus2IP_Data <= iBus2IP_Data(0 to USER_DWIDTH-1);
  uBus2IP_RdCE <= iBus2IP_RdCE(USER00_CE_INDEX to
                               USER00_CE_INDEX+USER_NUM_CE-1);
  uBus2IP_WrCE <= iBus2IP_WrCE(USER00_CE_INDEX to
                               USER00_CE_INDEX+USER_NUM_CE-1);
  iIP2Bus_Data(0 to USER_DWIDTH-1) <= uIP2Bus_Data;

end IMP;
```

- Codes for the MPD file

```
##############################################################################
## Name     : adc1_opb                                                      ##
## Desc     : Microprocessor Peripheral Description                         ##
##          : Automatically generated by PsfUtility                         ##
##############################################################################

BEGIN adc1_opb

## Peripheral Options
OPTION IPTYPE = PERIPHERAL
OPTION IMP_NETLIST = TRUE
OPTION HDL = VHDL
OPTION IP_GROUP = MICROBLAZE:PPC:USER
OPTION CORE_STATE = DEVELOPMENT


## Bus Interfaces
BUS_INTERFACE BUS = SOPB, BUS_TYPE = SLAVE, BUS_STD = OPB

## Generics for VHDL or Parameters for Verilog
PARAMETER C_BASEADDR = 0xffffffff, DT = std_logic_vector, MIN_SIZE =
          0x100, BUS = SOPB, ADDRESS = BASE, PAIR = C_HIGHADDR
PARAMETER C_HIGHADDR = 0x00000000, DT = std_logic_vector, BUS = SOPB,
          ADDRESS = HIGH, PAIR = C_BASEADDR
PARAMETER C_OPB_AWIDTH = 32, DT = INTEGER, BUS = SOPB
PARAMETER C_OPB_DWIDTH = 32, DT = INTEGER, BUS = SOPB
PARAMETER C_FAMILY = virtex2p, DT = STRING

## Ports
PORT OPB_Clk = "", DIR = I, SIGIS = Clk, BUS = SOPB
PORT OPB_Rst = OPB_Rst, DIR = I, SIGIS = Rst, BUS = SOPB
```

```
PORT Sl_DBus = Sl_DBus, DIR = O, VEC = [0:(C_OPB_DWIDTH-1)],
            BUS = SOPB
PORT Sl_errAck = Sl_errAck, DIR = O, BUS = SOPB
PORT Sl_retry = Sl_retry, DIR = O, BUS = SOPB
PORT Sl_toutSup = Sl_toutSup, DIR = O, BUS = SOPB
PORT Sl_xferAck = Sl_xferAck, DIR = O, BUS = SOPB
PORT OPB_ABus = OPB_ABus, DIR = I, VEC = [0:(C_OPB_AWIDTH-1)],
            BUS = SOPB
PORT OPB_BE = OPB_BE, DIR = I, VEC = [0:((C_OPB_DWIDTH/8)-1)],
            BUS = SOPB
PORT OPB_DBus = OPB_DBus, DIR = I, VEC = [0:(C_OPB_DWIDTH-1)],
            BUS = SOPB
PORT OPB_RNW = OPB_RNW, DIR = I, BUS = SOPB
PORT OPB_select = OPB_select, DIR = I, BUS = SOPB
PORT OPB_seqAddr = OPB_seqAddr, DIR = I, BUS = SOPB

## adc_opb signals
PORT ADC1_data = "", DIR = I, VEC = [0:11]
PORT ADC1_otr = "", DIR = I
PORT ADC1_en = "", DIR = I
PORT CLK_ADC = "", DIR = I, SIGIS = CLK
PORT ADC1_clk = "", DIR = O, SIGIS = CLK
PORT ADC1_LED1 = "", DIR = O
PORT ADC1_LED2 = "", DIR = O
PORT ADC1_mux = "", DIR = O, VEC = [0:3]
PORT ADC1_temp1 = "",DIR = O
PORT ADC1_temp2 = "",DIR = O,VEC=[0:12]
PORT Iin_A = "", DIR = O, VEC = [0:15]
PORT Iin_B = "", DIR = O, VEC = [0:15]
PORT Iin_C = "", DIR = O, VEC = [0:15]
PORT Iout_a = "", DIR = O, VEC = [0:15]
PORT Iout_b = "", DIR = O, VEC = [0:15]
PORT Iout_c = "", DIR = O, VEC = [0:15]

END
```

C.3. ADC2_OPB

The ADC2_OPB module is an ADC controller circuit that samples all nine dc switch cell capacitor voltages in the multilevel matrix converter.

- Codes for the user logic file

```
------------------------------------------------------------------
-- user_logic.vhd - entity/architecture pair
------------------------------------------------------------------
-- Filename:          user_logic.vhd
-- Version:           1.00.a
-- Description:       User logic.
-- Date:              Fri Nov 18 16:08:58 2005
                      (by Create and Import Peripheral Wizard)
-- VHDL Standard:     VHDL'93
------------------------------------------------------------------
library ieee;
```

```
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;
use ieee.std_logic_unsigned.all;

library proc_common_v2_00_a;
use proc_common_v2_00_a.proc_common_pkg.all;

entity user_logic is
  generic
  (
    ADC_DWIDTH : integer := 12;
    -- Bus protocol parameters, do not add to or delete
    C_DWIDTH   : integer := 16;
    C_NUM_CE   : integer := 9
  );
  port
  (
    ADC2_data      : in std_logic_vector(0 to 11);
    ADC2_otr       : in std_logic;
    ADC2_en        : in std_logic;
    CLK_ADC        : in std_logic;
    ADC2_clk       : out std_logic;
    ADC2_LED1      : out std_logic;
    ADC2_LED2      : out std_logic;
    ADC2_mux       : out std_logic_vector(0 to 3);
    ADC2_temp1     : out std_logic;
    ADC2_temp2     : out std_logic_vector(0 to 12);

    -- Bus protocol ports, do not add to or delete
    Bus2IP_Clk     : in  std_logic;
    Bus2IP_Reset   : in  std_logic;
    Bus2IP_Data    : in  std_logic_vector(0 to C_DWIDTH-1);
    Bus2IP_BE      : in  std_logic_vector(0 to C_DWIDTH/8-1);
    Bus2IP_RdCE    : in  std_logic_vector(0 to C_NUM_CE-1);
    Bus2IP_WrCE    : in  std_logic_vector(0 to C_NUM_CE-1);
    IP2Bus_Data    : out std_logic_vector(0 to C_DWIDTH-1);
    IP2Bus_Ack     : out std_logic;
    IP2Bus_Retry   : out std_logic;
    IP2Bus_Error   : out std_logic;
    IP2Bus_ToutSup : out std_logic
  );
end entity user_logic;

------------------------------------------------------------------------
-- Architecture section
------------------------------------------------------------------------

architecture IMP of user_logic is

  ---------------------------------------
  -- Signals for user logic slave model s/w accessible
  --            register example
  ---------------------------------------
  signal slv_reg0       : std_logic_vector(0 to C_DWIDTH-1);
  signal slv_reg1       : std_logic_vector(0 to C_DWIDTH-1);
  signal slv_reg2       : std_logic_vector(0 to C_DWIDTH-1);
  signal slv_reg3       : std_logic_vector(0 to C_DWIDTH-1);
```

```
  signal slv_reg4       : std_logic_vector(0 to C_DWIDTH-1);
  signal slv_reg5       : std_logic_vector(0 to C_DWIDTH-1);
  signal slv_reg6       : std_logic_vector(0 to C_DWIDTH-1);
  signal slv_reg7       : std_logic_vector(0 to C_DWIDTH-1);
  signal slv_reg8       : std_logic_vector(0 to C_DWIDTH-1);
  signal slv_reg_write_select : std_logic_vector(0 to 8);
  signal slv_reg_read_select  : std_logic_vector(0 to 8);
  signal slv_ip2bus_data      : std_logic_vector(0 to C_DWIDTH-1);
  signal slv_read_ack         : std_logic;
  signal slv_write_ack  : std_logic;
  signal temp           : std_logic_vector (0 to (C_DWIDTH-1));
  signal temp1,temp2    : std_logic_vector (0 to (ADC_DWIDTH-1));
  signal temp3,temp4    : std_logic_vector (0 to (ADC_DWIDTH-1));
  signal temp5            : std_logic_vector(0 to 13);
  signal count,next_count : integer range 0 to 16;
  signal temp_ADC2_mux,next_ADC2_mux : std_logic_vector(0 to 3);
  signal VC_Aa,VC_Ab,VC_Ac : std_logic_vector(0 to C_DWIDTH-1);
  signal VC_Ba,VC_Bb,VC_Bc : std_logic_vector(0 to C_DWIDTH-1);
  signal VC_Ca,VC_Cb,VC_Cc : std_logic_vector(0 to C_DWIDTH-1);

begin
  slv_reg_write_select <= Bus2IP_WrCE(0 to 8);
  slv_reg_read_select  <= Bus2IP_RdCE(0 to 8);
  slv_write_ack        <= Bus2IP_WrCE(0) or Bus2IP_WrCE(1) or
                          Bus2IP_WrCE(2) or Bus2IP_WrCE(3) or
                          Bus2IP_WrCE(4) or Bus2IP_WrCE(5) or
                          Bus2IP_WrCE(6) or Bus2IP_WrCE(7) or
                          Bus2IP_WrCE(8);
  slv_read_ack         <= Bus2IP_RdCE(0) or Bus2IP_RdCE(1) or
                          Bus2IP_RdCE(2) or Bus2IP_RdCE(3) or
                          Bus2IP_RdCE(4) or Bus2IP_RdCE(5) or
                          Bus2IP_RdCE(6) or Bus2IP_RdCE(7) or
                          Bus2IP_RdCE(8);

  -- implement slave model register read mux
  SLAVE_REG_READ_PROC : process( slv_reg_read_select, slv_reg0,
                                 slv_reg1, slv_reg2, slv_reg3,
                                 slv_reg4, slv_reg5, slv_reg6,
                                 slv_reg7, slv_reg8 ) is
  begin

    case slv_reg_read_select is
      when "100000000" => slv_ip2bus_data <= slv_reg0;
      when "010000000" => slv_ip2bus_data <= slv_reg1;
      when "001000000" => slv_ip2bus_data <= slv_reg2;
      when "000100000" => slv_ip2bus_data <= slv_reg3;
      when "000010000" => slv_ip2bus_data <= slv_reg4;
      when "000001000" => slv_ip2bus_data <= slv_reg5;
      when "000000100" => slv_ip2bus_data <= slv_reg6;
      when "000000010" => slv_ip2bus_data <= slv_reg7;
      when "000000001" => slv_ip2bus_data <= slv_reg8;
      when others => slv_ip2bus_data <= (others => '0');
    end case;

  end process SLAVE_REG_READ_PROC;

  ----------------------------------------
```

```
-- Example code to drive IP to Bus signals
------------------------------------------
IP2Bus_Data        <= slv_ip2bus_data;
IP2Bus_Ack         <= slv_write_ack or slv_read_ack;
IP2Bus_Error       <= '0';
IP2Bus_Retry       <= '0';
IP2Bus_ToutSup     <= '0';

process(CLK_ADC,Bus2IP_Reset,ADC2_en)
begin
    if ((Bus2IP_Reset = '1') or (ADC2_en = '0')) then
          count <= 0;
      elsif (CLK_ADC'event AND CLK_ADC = '1') then
              count <= next_count;
      end if;
end process;

process(count)
begin
      next_count <= 0;
      case count is
        when 0 to 15 =>
          next_count <= count + 1;
        when 16 =>
          next_count <= 0;
        when others =>
      end case;
end process;

process(CLK_ADC,Bus2IP_reset)
begin
  if (Bus2IP_Reset = '1') then
    temp_ADC2_mux <= "0000";
  elsif (CLK_ADC'event and CLK_ADC = '1') then
    if(count = 16) then
      temp_ADC2_mux <= next_ADC2_mux;
    end if;
  end if;
end process;

process(temp_ADC2_mux)
begin
  next_ADC2_mux <= "1000";
  case temp_ADC2_mux is
    when "0000" => next_ADC2_mux <= "1000";
    when "1000" => next_ADC2_mux <= "0100";
    when "0100" => next_ADC2_mux <= "1100";
    when "1100" => next_ADC2_mux <= "0010";
    when "0010" => next_ADC2_mux <= "1010";
    when "1010" => next_ADC2_mux <= "0110";
    when "0110" => next_ADC2_mux <= "1110";
    when "1110" => next_ADC2_mux <= "0001";
    when "0001" => next_ADC2_mux <= "0000";
    when others =>
  end case;
end process;
```

```
  process(CLK_ADC)
  begin
    if (CLK_ADC'event and CLK_ADC = '0') then
      if (count = 10) then
        temp1 <= ADC2_data;
      elsif (count = 11) then
        temp2 <= ADC2_data;
      elsif (count = 12) then
        temp3 <= ADC2_data;
      elsif (count = 13) then
        temp4 <= ADC2_data;
      elsif (count = 15) then
        case temp_ADC2_mux is
          when "0000" => VC_Cb <= (temp);
          when "1000" => VC_Ca <= (temp);
          when "0100" => VC_Ba <= (temp);
          when "1100" => VC_Bb <= (temp);
          when "0010" => VC_Bc <= (temp);
          when "1010" => VC_Aa <= (temp);
          when "0110" => VC_Ab <= (temp);
          when "1110" => VC_Ac <= (temp);
          when "0001" => VC_Cc <= (temp);
          when others =>
        end case;
      end if;
    end if;
  end process;

-----------------------------------------------------------------
------ Calculating the average of four sampling data         -----

      temp5 <= (("00" & temp1) + ("00" & temp2) +
                  ("00" & temp3) + ("00" & temp4));
      temp <= ("0000" & temp5(0 to 11));

  process(Bus2IP_Clk)
  begin
    if (Bus2IP_Clk'event and Bus2IP_Clk = '1') then
      slv_reg0 <= (VC_Aa);
      slv_reg1 <= (VC_Ab);
      slv_reg2 <= (VC_Ac);
      slv_reg3 <= (VC_Ba);
      slv_reg4 <= (VC_Bb);
      slv_reg5 <= (VC_Bc);
      slv_reg6 <= (VC_Ca);
      slv_reg7 <= (VC_Cb);
      slv_reg8 <= (VC_Cc);
    end if;
  end process;

  ADC2_clk <= CLK_ADC;-- when ADC2_en = '1' else '0';
  ADC2_LED1 <= ADC2_otr;
  ADC2_LED2 <= '1'; --ADC2_en;
  ADC2_mux <= temp_ADC2_mux;
  ADC2_temp1 <= '1' when (count = 15) else '0';
  ADC2_temp2 <= (ADC2_otr & temp(4 to 15));
```

```
end IMP;
```

- Codes for the HDL peripheral definition file

```
------------------------------------------------------------------------------
-- ADC2_OPB.vhd - entity/architecture pair
------------------------------------------------------------------------------
-- Filename:          ADC2_OPB.vhd
-- Version:           1.00.a
-- Description:       Top level design, instantiates IPIF
--                       and user logic.
-- Date:              Fri Nov 18 16:08:58 2005
--                      (by Create and Import Peripheral Wizard)
-- VHDL Standard:     VHDL'93
------------------------------------------------------------------------------
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;
use ieee.std_logic_unsigned.all;

library proc_common_v2_00_a;
use proc_common_v2_00_a.proc_common_pkg.all;
use proc_common_v2_00_a.ipif_pkg.all;
library opb_ipif_v3_01_a;
use opb_ipif_v3_01_a.all;

library ADC2_OPB_v1_00_a;
use ADC2_OPB_v1_00_a.all;

entity ADC2_OPB is
  generic
  (
    -- Bus protocol parameters, do not add to or delete
    C_BASEADDR   : std_logic_vector := X"00000000";
    C_HIGHADDR   : std_logic_vector := X"0000FFFF";
    C_OPB_AWIDTH : integer          := 32;
    C_OPB_DWIDTH : integer          := 32;
    C_FAMILY     : string           := "virtex2p"
  );
  port
  (
    ADC2_data   : in std_logic_vector(0 to 11);
    ADC2_otr    : in std_logic;
    ADC2_en     : in std_logic;
    CLK_ADC     : in std_logic;
    ADC2_clk    : out std_logic;
    ADC2_LED1   : out std_logic;
    ADC2_LED2   : out std_logic;
    ADC2_mux    : out std_logic_vector(0 to 3);
    ADC2_temp1  : out std_logic;
    ADC2_temp2  : out std_logic_vector(0 to 12);
    -- Bus protocol ports, do not add to or delete
    OPB_Clk     : in  std_logic;
    OPB_Rst     : in  std_logic;
    Sl_DBus     : out std_logic_vector(0 to C_OPB_DWIDTH-1);
    Sl_errAck   : out std_logic;
```

```
    Sl_retry    : out std_logic;
    Sl_toutSup  : out std_logic;
    Sl_xferAck  : out std_logic;
    OPB_ABus    : in  std_logic_vector(0 to C_OPB_AWIDTH-1);
    OPB_BE      : in  std_logic_vector(0 to C_OPB_DWIDTH/8-1);
    OPB_DBus    : in  std_logic_vector(0 to C_OPB_DWIDTH-1);
    OPB_RNW     : in  std_logic;
    OPB_select  : in  std_logic;
    OPB_seqAddr : in  std_logic
  );

  attribute SIGIS : string;
  attribute SIGIS of OPB_Clk       : signal is "Clk";
  attribute SIGIS of OPB_Rst       : signal is "Rst";

end entity ADC2_OPB;

------------------------------------------------------------------------
-- Architecture section
------------------------------------------------------------------------
architecture IMP of ADC2_OPB is

  ---------------------------------------------
  -- Constant: array of address range identifiers
  ---------------------------------------------
  constant ARD_ID_ARRAY : INTEGER_ARRAY_TYPE :=
    (
      0  => USER_00  -- user logic S/W register address space
    );

  ---------------------------------------------
  -- Constant: array of address pairs for each address range
  ---------------------------------------------
  constant ZERO_ADDR_PAD : std_logic_vector(0 to 64-C_OPB_AWIDTH-1)
                           := (others => '0');

  constant USER_BASEADDR : std_logic_vector := C_BASEADDR;
  constant USER_HIGHADDR : std_logic_vector := C_HIGHADDR;

  constant ARD_ADDR_RANGE_ARRAY : SLV64_ARRAY_TYPE :=
    (
      ZERO_ADDR_PAD & USER_BASEADDR, -- user logic base address
      ZERO_ADDR_PAD & USER_HIGHADDR  -- user logic high address
    );

  ---------------------------------------------
  -- Constant: array of data widths for each target address range
  ---------------------------------------------
  constant USER_DWIDTH      : integer            := 16;

  constant ARD_DWIDTH_ARRAY : INTEGER_ARRAY_TYPE :=
    (
      0  => USER_DWIDTH  -- user logic data width
    );

  ---------------------------------------------
  -- Constant: array of desired number of chip enables for
```

```
--            each address range
------------------------------------------
constant USER_NUM_CE      : integer            := 9;

constant ARD_NUM_CE_ARRAY : INTEGER_ARRAY_TYPE :=
  (
    0  => pad_power2(USER_NUM_CE) -- user logic number of CEs
  );

------------------------------------------
-- Constant: array of unique properties for each address range
------------------------------------------
constant ARD_DEPENDENT_PROPS_ARRAY :
                                  DEPENDENT_PROPS_ARRAY_TYPE :=
  (
    0  => (others => 0)
  -- user logic slave space dependent properties (none defined)
  );

 ------------------------------------------
constant PIPELINE_MODEL : integer := 5;

------------------------------------------
-- Constant: user core ID code
------------------------------------------
constant DEV_BLK_ID     : integer := 0;

------------------------------------------
-- Constant: enable MIR/Reset register
------------------------------------------
constant DEV_MIR_ENABLE : integer := 0;

 ------------------------------------------
constant IP_INTR_MODE_ARRAY : INTEGER_ARRAY_TYPE   :=
  (
    0  => 0  -- not used
  );

------------------------------------------
-- Constant: enable device burst
------------------------------------------
constant DEV_BURST_ENABLE  : integer := 0;

------------------------------------------
-- Constant: include address counter for burst transfers
------------------------------------------
constant INCLUDE_ADDR_CNTR : integer := 0;

------------------------------------------
-- Constant: include write buffer that decouples OPB and
--            IPIC write transactions
------------------------------------------
constant INCLUDE_WR_BUF    : integer := 0;

------------------------------------------
-- Constant: index for CS/CE
------------------------------------------
```

```
  constant USER00_CS_INDEX   : integer
        := get_id_index(ARD_ID_ARRAY, USER_00);
  constant USER00_CE_INDEX   : integer
        := calc_start_ce_index(ARD_NUM_CE_ARRAY, USER00_CS_INDEX);

  ------------------------------------------
  -- IP Interconnect (IPIC) signal declarations -- do not delete
  -- prefix 'i' stands for IPIF while prefix 'u' stands for user
  -- logic typically user logic will be hooked up to IPIF
  -- directly via i<sig> unless signal slicing and muxing are
  -- needed via u<sig>
  ------------------------------------------
  signal iBus2IP_RdCE            : std_logic_vector(0 to
                 calc_num_ce(ARD_NUM_CE_ARRAY)-1);
  signal iBus2IP_WrCE            : std_logic_vector(0 to
                 calc_num_ce(ARD_NUM_CE_ARRAY)-1);
  signal iBus2IP_Data            : std_logic_vector(0 to
                 C_OPB_DWIDTH-1);
  signal iBus2IP_BE              : std_logic_vector(0 to
                 C_OPB_DWIDTH/8-1);
  signal iIP2Bus_Data            : std_logic_vector(0 to
                 C_OPB_DWIDTH-1)   := (others => '0');
  signal iIP2Bus_Ack             : std_logic   := '0';
  signal iIP2Bus_Error           : std_logic   := '0';
  signal iIP2Bus_Retry           : std_logic   := '0';
  signal iIP2Bus_ToutSup         : std_logic   := '0';
  signal ZERO_IP2Bus_PostedWrInh : std_logic_vector(0 to
                 ARD_ID_ARRAY'length-1)  := (others => '0');
  signal ZERO_IP2RFIFO_Data      : std_logic_vector(0 to
                 ARD_DWIDTH_ARRAY(get_id_index_iboe(ARD_ID_ARRAY,
                 IPIF_RDFIFO_DATA))-1)   := (others => '0');
  signal ZERO_WFIFO2IP_Data      : std_logic_vector(0 to
                 ARD_DWIDTH_ARRAY(get_id_index_iboe(ARD_ID_ARRAY,
                 IPIF_WRFIFO_DATA))-1)   := (others => '0');
  signal ZERO_IP2Bus_IntrEvent   : std_logic_vector(0 to
                 IP_INTR_MODE_ARRAY'length-1) := (others => '0');
  signal iBus2IP_Clk    : std_logic;
  signal iBus2IP_Reset  : std_logic;
  signal uBus2IP_Data   : std_logic_vector(0 to USER_DWIDTH-1);
  signal uBus2IP_BE     : std_logic_vector(0 to USER_DWIDTH/8-1);
  signal uBus2IP_RdCE   : std_logic_vector(0 to USER_NUM_CE-1);
  signal uBus2IP_WrCE   : std_logic_vector(0 to USER_NUM_CE-1);
  signal uIP2Bus_Data   : std_logic_vector(0 to USER_DWIDTH-1);

begin

  ------------------------------------------
  -- instantiate the OPB IPIF
  ------------------------------------------
  OPB_IPIF_I : entity opb_ipif_v3_01_a.opb_ipif
    generic map
    (
      C_ARD_ID_ARRAY              => ARD_ID_ARRAY,
      C_ARD_ADDR_RANGE_ARRAY      => ARD_ADDR_RANGE_ARRAY,
      C_ARD_DWIDTH_ARRAY          => ARD_DWIDTH_ARRAY,
      C_ARD_NUM_CE_ARRAY          => ARD_NUM_CE_ARRAY,
      C_ARD_DEPENDENT_PROPS_ARRAY => ARD_DEPENDENT_PROPS_ARRAY,
```

```
  C_PIPELINE_MODEL            => PIPELINE_MODEL,
  C_DEV_BLK_ID                => DEV_BLK_ID,
  C_DEV_MIR_ENABLE            => DEV_MIR_ENABLE,
  C_OPB_AWIDTH                => C_OPB_AWIDTH,
  C_OPB_DWIDTH                => C_OPB_DWIDTH,
  C_FAMILY                    => C_FAMILY,
  C_IP_INTR_MODE_ARRAY        => IP_INTR_MODE_ARRAY,
  C_DEV_BURST_ENABLE          => DEV_BURST_ENABLE,
  C_INCLUDE_ADDR_CNTR         => INCLUDE_ADDR_CNTR,
  C_INCLUDE_WR_BUF            => INCLUDE_WR_BUF
)
port map
(
  OPB_select           => OPB_select,
  OPB_DBus             => OPB_DBus,
  OPB_ABus             => OPB_ABus,
  OPB_BE               => OPB_BE,
  OPB_RNW              => OPB_RNW,
  OPB_seqAddr          => OPB_seqAddr,
  Sln_DBus             => Sl_DBus,
  Sln_xferAck          => Sl_xferAck,
  Sln_errAck           => Sl_errAck,
  Sln_retry            => Sl_retry,
  Sln_toutSup          => Sl_toutSup,
  Bus2IP_CS            => open,
  Bus2IP_CE            => open,
  Bus2IP_RdCE          => iBus2IP_RdCE,
  Bus2IP_WrCE          => iBus2IP_WrCE,
  Bus2IP_Data          => iBus2IP_Data,
  Bus2IP_Addr          => open,
  Bus2IP_AddrValid     => open,
  Bus2IP_BE            => iBus2IP_BE,
  Bus2IP_RNW           => open,
  Bus2IP_Burst         => open,
  IP2Bus_Data          => iIP2Bus_Data,
  IP2Bus_Ack           => iIP2Bus_Ack,
  IP2Bus_AddrAck       => '0',
  IP2Bus_Error         => iIP2Bus_Error,
  IP2Bus_Retry         => iIP2Bus_Retry,
  IP2Bus_ToutSup       => iIP2Bus_ToutSup,
  IP2Bus_PostedWrInh   => ZERO_IP2Bus_PostedWrInh,
  IP2RFIFO_Data        => ZERO_IP2RFIFO_Data,
  IP2RFIFO_WrMark      => '0',
  IP2RFIFO_WrRelease   => '0',
  IP2RFIFO_WrReq       => '0',
  IP2RFIFO_WrRestore   => '0',
  RFIFO2IP_AlmostFull  => open,
  RFIFO2IP_Full        => open,
  RFIFO2IP_Vacancy     => open,
  RFIFO2IP_WrAck       => open,
  IP2WFIFO_RdMark      => '0',
  IP2WFIFO_RdRelease   => '0',
  IP2WFIFO_RdReq       => '0',
  IP2WFIFO_RdRestore   => '0',
  WFIFO2IP_AlmostEmpty => open,
  WFIFO2IP_Data        => ZERO_WFIFO2IP_Data,
  WFIFO2IP_Empty       => open,
```

```
    WFIFO2IP_Occupancy   => open,
    WFIFO2IP_RdAck       => open,
    IP2Bus_IntrEvent     => ZERO_IP2Bus_IntrEvent,
    IP2INTC_Irpt         => open,
    Freeze               => '0',
    Bus2IP_Freeze        => open,
    OPB_Clk              => OPB_Clk,
    Bus2IP_Clk           => iBus2IP_Clk,
    IP2Bus_Clk           => '0',
    Reset                => OPB_Rst,
    Bus2IP_Reset         => iBus2IP_Reset
  );

------------------------------------------
-- instantiate the User Logic
------------------------------------------
USER_LOGIC_I : entity ADC2_OPB_v1_00_a.user_logic
  generic map
  (
    C_DWIDTH       => USER_DWIDTH,
    C_NUM_CE       => USER_NUM_CE
  )
  port map
  (
    ADC2_data      => ADC2_data,
    ADC2_otr       => ADC2_otr,
    ADC2_en        => ADC2_en,
    CLK_ADC        => CLK_ADC,
    ADC2_clk       => ADC2_clk,
    ADC2_LED1      => ADC2_LED1,
    ADC2_LED2      => ADC2_LED2,
    ADC2_mux       => ADC2_mux,
    ADC2_temp1     => ADC2_temp1,
    ADC2_temp2     => ADC2_temp2,
    Bus2IP_Clk     => iBus2IP_Clk,
    Bus2IP_Reset   => iBus2IP_Reset,
    Bus2IP_Data    => uBus2IP_Data,
    Bus2IP_BE      => uBus2IP_BE,
    Bus2IP_RdCE    => uBus2IP_RdCE,
    Bus2IP_WrCE    => uBus2IP_WrCE,
    IP2Bus_Data    => uIP2Bus_Data,
    IP2Bus_Ack     => iIP2Bus_Ack,
    IP2Bus_Retry   => iIP2Bus_Retry,
    IP2Bus_Error   => iIP2Bus_Error,
    IP2Bus_ToutSup => iIP2Bus_ToutSup
  );

------------------------------------------
-- hooking up signal slicing
------------------------------------------
uBus2IP_BE   <= iBus2IP_BE(0 to USER_DWIDTH/8-1);
uBus2IP_Data <= iBus2IP_Data(0 to USER_DWIDTH-1);
uBus2IP_RdCE <= iBus2IP_RdCE(USER00_CE_INDEX to
                             USER00_CE_INDEX+USER_NUM_CE-1);
uBus2IP_WrCE <= iBus2IP_WrCE(USER00_CE_INDEX to
                             USER00_CE_INDEX+USER_NUM_CE-1);
iIP2Bus_Data(0 to USER_DWIDTH-1) <= uIP2Bus_Data;
```

```
end IMP;
```

- Codes for the MPD file

```
##############################################################################
## Name     : ADC2_OPB                                                      ##
## Desc     : Microprocessor Peripheral Description                         ##
##          : Automatically generated by PsfUtility                         ##
##############################################################################
BEGIN ADC2_OPB

## Peripheral Options
OPTION IPTYPE = PERIPHERAL
OPTION IMP_NETLIST = TRUE
OPTION HDL = VHDL
OPTION IP_GROUP = MICROBLAZE:PPC:USER
OPTION CORE_STATE = DEVELOPMENT

## Bus Interfaces
BUS_INTERFACE BUS = SOPB, BUS_TYPE = SLAVE, BUS_STD = OPB

## Generics for VHDL or Parameters for Verilog
PARAMETER C_BASEADDR = 0xffffffff, DT = std_logic_vector,
      MIN_SIZE = 0x100, BUS = SOPB, ADDRESS = BASE,
      PAIR = C_HIGHADDR
PARAMETER C_HIGHADDR = 0x00000000, DT = std_logic_vector,
      BUS = SOPB, ADDRESS = HIGH, PAIR = C_BASEADDR
PARAMETER C_OPB_AWIDTH = 32, DT = INTEGER, BUS = SOPB
PARAMETER C_OPB_DWIDTH = 32, DT = INTEGER, BUS = SOPB
PARAMETER C_FAMILY = virtex2p, DT = STRING

## Ports
PORT OPB_Clk = "", DIR = I, SIGIS = Clk, BUS = SOPB
PORT OPB_Rst = OPB_Rst, DIR = I, SIGIS = Rst, BUS = SOPB
PORT Sl_DBus = Sl_DBus, DIR = O, VEC = [0:(C_OPB_DWIDTH-1)],
      BUS = SOPB
PORT Sl_errAck = Sl_errAck, DIR = O, BUS = SOPB
PORT Sl_retry = Sl_retry, DIR = O, BUS = SOPB
PORT Sl_toutSup = Sl_toutSup, DIR = O, BUS = SOPB
PORT Sl_xferAck = Sl_xferAck, DIR = O, BUS = SOPB
PORT OPB_ABus = OPB_ABus, DIR = I, VEC = [0:(C_OPB_AWIDTH-1)],
      BUS = SOPB
PORT OPB_BE = OPB_BE, DIR = I, VEC = [0:((C_OPB_DWIDTH/8)-1)],
      BUS = SOPB
PORT OPB_DBus = OPB_DBus, DIR = I, VEC = [0:(C_OPB_DWIDTH-1)],
      BUS = SOPB
PORT OPB_RNW = OPB_RNW, DIR = I, BUS = SOPB
PORT OPB_select = OPB_select, DIR = I, BUS = SOPB
PORT OPB_seqAddr = OPB_seqAddr, DIR = I, BUS = SOPB

## ADC_ctrl2 signals
PORT ADC2_data = "", DIR = I, VEC = [0:11]
PORT ADC2_otr = "", DIR = I
PORT ADC2_en = "", DIR = I
PORT CLK_ADC = "", DIR = I, SIGIS = CLK
PORT ADC2_clk = "", DIR = O, SIGIS = CLK
```

```
PORT ADC2_LED1 = "", DIR = O
PORT ADC2_LED2 = "", DIR = O
PORT ADC2_mux = "", DIR = O, VEC = [0:3]
PORT ADC2_temp1 = "",DIR = O
PORT ADC2_temp2 = "",DIR = O,VEC=[0:12]
END
```

C.4. PWM

The PWM module is the PWM controller circuit. It controls the duration of each subinterval and keeps track of the subinterval. It provides data representing a converter configuration for each subinterval, turn-off, and turn-on signals as outputs.

- Codes for the user logic file

```
------------------------------------------------------------------
-- user_logic.vhd - entity/architecture pair
------------------------------------------------------------------
-- Filename:          user_logic.vhd
-- Version:           1.00.a
-- Description:       User logic module.
-- Date:              Tue Aug 02 11:33:01 2005
--                      (by Create/Import Peripheral Wizard)
-- VHDL-Standard:     VHDL'93
------------------------------------------------------------------
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;
use ieee.std_logic_unsigned.all;

library proc_common_v1_00_b;
use proc_common_v1_00_b.proc_common_pkg.all;

entity user_logic is
  generic
    (
      -- Bus protocol parameters, do not add to or delete
      C_DWIDTH    : integer   := 32;
      C_NUM_CE    : integer   := 10
     );
  port
    (
      CLK_PWM        : in  bit;
      enable         : out std_logic;
      data_valid     : out std_logic;
      lut_data       : out std_logic_vector(0 to 18);
      subin          : out std_logic_vector(0 to 2);
      switch_off     : out bit;
      switch_on      : out bit;
      -- Bus protocol ports, do not add to or delete
      Bus2IP_Clk     : in  std_logic;
      Bus2IP_Reset   : in  std_logic;
      Bus2IP_Data    : in  std_logic_vector(0 to C_DWIDTH-1);
      Bus2IP_BE      : in  std_logic_vector(0 to C_DWIDTH/8-1);
```

```
      Bus2IP_RdCE    : in  std_logic_vector(0 to C_NUM_CE-1);
      Bus2IP_WrCE    : in  std_logic_vector(0 to C_NUM_CE-1);
      IP2Bus_Data    : out std_logic_vector(0 to C_DWIDTH-1);
      IP2Bus_Ack     : out std_logic;
      IP2Bus_Retry   : out std_logic;
      IP2Bus_Error   : out std_logic;
      IP2Bus_ToutSup : out std_logic
    );
end entity user_logic;

------------------------------------------------------------------------
-- Architecture section
------------------------------------------------------------------------

architecture IMP of user_logic is

      ---------------------------------------
      -- User logic S/W accessible registers
      ---------------------------------------
      signal reg0 : std_logic_vector(0 to C_DWIDTH-1);
      signal reg1 : std_logic_vector(0 to C_DWIDTH-1);
      signal reg2 : std_logic_vector(0 to C_DWIDTH-1);
      signal reg3 : std_logic_vector(0 to C_DWIDTH-1);
      signal reg4 : std_logic_vector(0 to C_DWIDTH-1);
      signal reg5 : std_logic_vector(0 to C_DWIDTH-1);
      signal reg6 : std_logic_vector(0 to C_DWIDTH-1);
      signal reg7 : std_logic_vector(0 to C_DWIDTH-1);
      signal reg8 : std_logic_vector(0 to C_DWIDTH-1);
      signal reg9 : std_logic_vector(0 to C_DWIDTH-1);
      signal reg_write_select : std_logic_vector(0 to 9);
      signal reg_read_select  : std_logic_vector(0 to 9);
      signal update,sub0      : std_logic
        signal data_valid1      : std_logic;
        signal skip             : std_logic;
      signal data0_temp,data1_temp : std_logic_vector(0 to 18);
        signal data2_temp,data3_temp : std_logic_vector(0 to 18);
        signal data4_temp,data5_temp : std_logic_vector(0 to 18);
        signal data6_temp            : std_logic_vector(0 to 18);
      signal timer0_temp,timer1_temp : std_logic_vector(0 to 9);
        signal timer2_temp,timer3_temp : std_logic_vector(0 to 9);
        signal timer4_temp,timer5_temp : std_logic_vector(0 to 9);
        signal timer6_temp             : std_logic_vector(0 to 9);
      signal subinterval      : std_logic_vector(0 to 2);
        signal next_subinterval : std_logic_vector(0 to 2);
      signal next_lut_data    : std_logic_vector(0 to 18);
      signal timer_ref        : std_logic_vector(0 to 9);
        signal next_timer_ref   : std_logic_vector(0 to 9);
      signal timer_ref2         std_logic_vector(0 to 4);
        signal next_timer_ref2  : std_logic_vector(0 to 4);
      signal reset1,count_done,counter2_en,reset2 : bit;
      signal count1 : std_logic_vector(0 to 9);
      signal count2 : integer range 0 to 30;
begin

      ---------------------------------------
      -- Map user logic S/W register read/write select signal
      ---------------------------------------
```

```
reg_write_select <= Bus2IP_WrCE;
reg_read_select <= Bus2IP_RdCE;

---------------------------------------
-- User logic S/W accessible registers write example
---------------------------------------
REG_WRITE_PROC : process( Bus2IP_Clk ) is
begin
    if Bus2IP_Clk'event and Bus2IP_Clk = '1' then
      if Bus2IP_Reset = '1' then
        reg0 <= (others => '0');
        reg1 <= (others => '0');
        reg2 <= (others => '0');
        reg3 <= (others => '0');
        reg4 <= (others => '0');
        reg5 <= (others => '0');
        reg6 <= (others => '0');
        reg7 <= (others => '0');
        reg8 <= (others => '0');
        reg9 <= (others => '0');
      else
        case reg_write_select is
          when "1000000000" => reg0 <= Bus2IP_Data;
          when "0100000000" => reg1 <= Bus2IP_Data;
          when "0010000000" => reg2 <= Bus2IP_Data;
          when "0001000000" => reg3 <= Bus2IP_Data;
          when "0000100000" => reg4 <= Bus2IP_Data;
          when "0000010000" => reg5 <= Bus2IP_Data;
          when "0000001000" => reg6 <= Bus2IP_Data;
          when "0000000100" => reg7 <= Bus2IP_Data;
          when "0000000010" => reg8 <= Bus2IP_Data;
          when "0000000001" => reg9 <= Bus2IP_Data;
          when others => null;
        end case;
      end if;
    end if;
end process REG_WRITE_PROC;

---------------------------------------
-- User logic S/W accessible registers read example
---------------------------------------
REG_READ_PROC : process( reg_read_select, reg0, reg1,
                         reg2, reg3, reg4, reg5, reg6,
                         reg7, reg8, reg9 ) is
begin
    case reg_read_select is
      when "1000000000" => IP2Bus_Data <= reg0;
      when "0100000000" => IP2Bus_Data <= reg1;
      when "0010000000" => IP2Bus_Data <= reg2;
      when "0001000000" => IP2Bus_Data <= reg3;
      when "0000100000" => IP2Bus_Data <= reg4;
      when "0000010000" => IP2Bus_Data <= reg5;
      when "0000001000" => IP2Bus_Data <= reg6;
      when "0000000100" => IP2Bus_Data <= reg7;
      when "0000000010" => IP2Bus_Data <= reg8;
      when "0000000001" => IP2Bus_Data <= reg9;
      when others => IP2Bus_Data <= (others => '0');
```

```
      end case;
end process REG_READ_PROC;

---------------------------------------
-- Simple example to drive IP2Bus signals
---------------------------------------
IP2Bus_Ack     <= Bus2IP_WrCE(0) or Bus2IP_WrCE(1) or
                  Bus2IP_WrCE(2) or Bus2IP_WrCE(3) or
                  Bus2IP_WrCE(4) or Bus2IP_WrCE(5) or
                  Bus2IP_WrCE(6) or Bus2IP_WrCE(7) or
                  Bus2IP_WrCE(8) or Bus2IP_WrCE(9) or
                  Bus2IP_RdCE(0) or Bus2IP_RdCE(1) or
                  Bus2IP_RdCE(2) or Bus2IP_RdCE(3) or
                  Bus2IP_RdCE(4) or Bus2IP_RdCE(5) or
                  Bus2IP_RdCE(6) or Bus2IP_RdCE(7) or
                  Bus2IP_RdCE(8) or Bus2IP_RdCE(9);
IP2Bus_Error   <= '0';
IP2Bus_Retry   <= '0';
IP2Bus_ToutSup <= '0';
data_valid1    <= reg9(31);
sub0   <= (not subinterval(0)) and (not subinterval(1))
           and (not subinterval(2));
update <= data_valid1 and sub0;

process(update)
  begin
    if (update'event and update = '1') then
      data0_temp <= reg0(3 to 21);
      data1_temp <= reg1(3 to 21);
      data2_temp <= reg2(3 to 21);
      data3_temp <= reg3(3 to 21);
      data4_temp <= reg4(3 to 21);
      data5_temp <= reg5(3 to 21);
      data6_temp <= reg6(3 to 21);
      timer0_temp <= reg0(22 to 31);
      timer1_temp <= reg1(22 to 31);
      timer2_temp <= reg2(22 to 31);
      timer3_temp <= reg3(22 to 31);
      timer4_temp <= reg4(22 to 31);
      timer5_temp <= reg5(22 to 31);
      timer6_temp <= reg6(22 to 31);
    end if;
  end process;

process(subinterval,skip,data1_temp,data2_temp,data3_temp,
          data4_temp,data5_temp,data6_temp,timer1_temp,
          timer2_temp,timer3_temp,timer4_temp,timer5_temp,
          timer6_temp,timer0_temp,data0_temp)
  begin
    next_subinterval <= "000";
    next_lut_data <= b"000_0000_0000_0000_0000";
    next_timer_ref <= b"10_0000_0000";
    next_timer_ref2 <= b"1_0000";
    case subinterval is
      when "000" =>
        if (skip = '1') then
          next_subinterval <= "010";
```

```
    next_lut_data    <= data2_temp;
    next_timer_ref   <= timer2_temp;
    next_timer_ref2  <= timer3_temp(0 to 4);
  else
    next_subinterval <= "001";
    next_lut_data    <= data1_temp;
    next_timer_ref   <= timer1_temp;
    next_timer_ref2  <= timer2_temp(0 to 4);
  end if;
when "001" =>
  if (skip = '1') then
    next_subinterval <= "011";
    next_lut_data    <= data3_temp;
    next_timer_ref   <= timer3_temp;
    next_timer_ref2  <= timer4_temp(0 to 4);
  else
    next_subinterval <= "010";
    next_lut_data    <= data2_temp;
    next_timer_ref   <= timer2_temp;
    next_timer_ref2  <= timer3_temp(0 to 4);
  end if;
when "010" =>
  if (skip = '1') then
    next_subinterval <= "100";
    next_lut_data    <= data4_temp;
    next_timer_ref   <= timer4_temp;
    next_timer_ref2  <= timer5_temp(0 to 4);
  else
    next_subinterval <= "011";
    next_lut_data    <= data3_temp;
    next_timer_ref   <= timer3_temp;
    next_timer_ref2  <= timer4_temp(0 to 4);
  end if;
when "011" =>
  if (skip = '1') then
    next_subinterval <= "101";
    next_lut_data    <= data5_temp;
    next_timer_ref   <= timer5_temp;
    next_timer_ref2  <= timer6_temp(0 to 4);
  else
    next_subinterval <= "100";
    next_lut_data    <= data4_temp;
    next_timer_ref   <= timer4_temp;
    next_timer_ref2  <= timer5_temp(0 to 4);
  end if;
when "100" =>
  if (skip = '1') then
    next_subinterval <= "110";
    next_lut_data    <= data6_temp;
    next_timer_ref   <= timer6_temp;
    next_timer_ref2  <= timer0_temp(0 to 4);
  else
    next_subinterval <= "101";
    next_lut_data    <= data5_temp;
    next_timer_ref   <= timer5_temp;
    next_timer_ref2  <= timer6_temp(0 to 4);
  end if;
```

```
            when "101" =>
              if (skip = '1') then
                next_subinterval <= "000";
                next_lut_data    <= data0_temp;
                next_timer_ref   <= timer0_temp;
                next_timer_ref2  <= timer1_temp(0 to 4);
              else
                next_subinterval <= "110";
                next_lut_data    <= data6_temp;
                next_timer_ref   <= timer6_temp;
                next_timer_ref2  <= timer0_temp(0 to 4);
              end if;
            when "110" =>
              if (skip = '1') then
                next_subinterval <= "001";
                next_lut_data    <= data1_temp;
                next_timer_ref   <= timer1_temp;
                next_timer_ref2  <= timer2_temp(0 to 4);
              else
                next_subinterval <= "000";
                next_lut_data    <= data0_temp;
                next_timer_ref   <= timer0_temp;
                next_timer_ref2  <= timer1_temp(0 to 4);
              end if;
            when others =>
          end case;
        end process;

skip <= not ( timer_ref2(0) or timer_ref2(1) or timer_ref2(2) or
              timer_ref2(3) or timer_ref2(4));

counter1: process(Bus2IP_Reset,CLK_PWM)
          begin
            if (Bus2IP_Reset = '1') then
              count1 <= "0000000000";
            elsif (CLK_PWM'event and CLK_PWM = '1') then
              if (RESET1 = '1') then
                count1 <= "0000000000";
              else
                count1 <= count1 + 1;
              end if;
            end if;
          end process;

compare1: process(CLK_PWM)
          begin
            if (CLK_PWM'event and CLK_PWM = '0') then
              if(count1 = timer_ref) then
                count_done <= '1';
              else
                count_done <= '0';
              end if;
            end if;
          end process;

state: process(Bus2IP_Reset,CLK_PWM)
       begin
```

```
      if (Bus2IP_Reset = '1') then
        subinterval <= "000";
        lut_data    <= b"000_0000_0000_0000_0000";
        timer_ref   <= b"10_0000_0000";
        timer_ref2  <= b"1_0000";
      elsif (CLK_PWM'event and CLK_PWM = '1') then
        if (count_done = '1') then
          subinterval <= next_subinterval;
          lut_data    <= next_lut_data;
          timer_ref   <= next_timer_ref;
          timer_ref2  <= next_timer_ref2;
        end if;
      end if;
    end process;

    process(CLK_PWM)
    begin
      if ( CLK_PWM'event and CLK_PWM = '1') then
        if ( count_done = '1' ) then
          counter2_en <= '1';
        elsif ( RESET2 = '1') then
          counter2_en <= '0';
        end if;
      end if;
    end process;

    process(CLK_PWM)
    begin
      if (CLK_PWM'event and CLK_PWM = '1') then
        if (counter2_en = '1') then
          count2 <= count2 + 1;
        else
          count2 <= 0;
        end if;
      end if;
    end process;

    switch_off <= '1' when (count2 = 3) else '0';
    switch_on <= '1' when (count2 = 7) else '0';
    RESET2 <= '1' when (count2 = 30) else '0';
    RESET1 <= count_done;
    data_valid <= data_valid1;
    enable <= '1' when (count2 = 0) else '0';
    subin <= subinterval;
end IMP;
```

- Codes for the HDL peripheral definition file

```
------------------------------------------------------------------
-- pwm.vhd - entity/architecture pair
------------------------------------------------------------------
-- Filename:          pwm.vhd
-- Version:
-- Description:       Top level design, instantiates IPIF
--                      and user logic.
-- Date:              Wed Aug 03 20:09:23 2005
```

```
--                       (by Create/Import Peripheral Wizard)
-- VHDL-Standard:     VHDL'93
------------------------------------------------------------------
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;
use ieee.std_logic_unsigned.all;

library proc_common_v1_00_b;
use proc_common_v1_00_b.proc_common_pkg.all;

library ipif_common_v1_00_c;
use ipif_common_v1_00_c.ipif_pkg.all;

library opb_ipif_v3_00_a;
use opb_ipif_v3_00_a.all;

library pwm;
use pwm.all;

entity pwm is
  generic
    (
      -- Bus protocol parameters, do not add to or delete
      C_BASEADDR     : std_logic_vector := X"FFFFFFFF";
      C_HIGHADDR     : std_logic_vector := X"00000000";
      C_OPB_AWIDTH   : integer := 32;
      C_OPB_DWIDTH   : integer := 32;
      C_USER_ID_CODE : integer := 3;
      C_FAMILY       : string  := "virtex2p"
     );
  port
    (
      CLK_PWM     : in bit;
      enable      : out std_logic;
      data_valid  : out std_logic;
      lut_data    : out std_logic_vector(0 to 18);
      subin       : out std_logic_vector(0 to 2);
      switch_off  : out bit;
      switch_on   : out bit;
      -- Bus protocol ports, do not add to or delete
      OPB_Clk     : in  std_logic;
      OPB_Rst     : in  std_logic;
      Sl_DBus     : out std_logic_vector(0 to C_OPB_DWIDTH-1);
      Sl_errAck   : out std_logic;
      Sl_retry    : out std_logic;
      Sl_toutSup  : out std_logic;
      Sl_xferAck  : out std_logic;
      OPB_ABus    : in  std_logic_vector(0 to C_OPB_AWIDTH-1);
      OPB_BE      : in  std_logic_vector(0 to C_OPB_DWIDTH/8-1);
      OPB_DBus    : in  std_logic_vector(0 to C_OPB_DWIDTH-1);
      OPB_RNW     : in  std_logic;
      OPB_select  : in  std_logic;
      OPB_seqAddr : in  std_logic
     );

      attribute MIN_SIZE : string;
```

```
      attribute MIN_SIZE of C_BASEADDR : constant is "0x100";
      attribute SIGIS : string;
      attribute SIGIS of OPB_Clk : signal is "Clk";
      attribute SIGIS of OPB_Rst : signal is "Rst";

end entity pwm;

------------------------------------------------------------------------
-- Architecture section
------------------------------------------------------------------------

architecture IMP of pwm is

      ---------------------------------------
      -- Constant: array of address range identifiers
      ---------------------------------------
      constant ARD_ID_ARRAY : INTEGER_ARRAY_TYPE :=
          (
            0 => USER_00  -- user logic S/W register address space
            );

      ---------------------------------------
      -- Constant: array of address pairs for each address range
      ---------------------------------------
      constant ZERO_ADDR_PAD  : std_logic_vector(0 to
                            4-C_OPB_AWIDTH-1) := (others => '0');

      constant USER_BASEADDR  : std_logic_vector
                                  := C_BASEADDR or X"00000000";
      constant USER_HIGHADDR  : std_logic_vector
                                  := C_BASEADDR or X"000000FF";
      constant ARD_ADDR_RANGE_ARRAY : SLV64_ARRAY_TYPE :=
          (
            ZERO_ADDR_PAD & USER_BASEADDR,--user logic base address
            ZERO_ADDR_PAD & USER_HIGHADDR --user logic high address
            );

      ---------------------------------------
      -- Constant: array of data widths for each
        --              target address range
      ---------------------------------------
      constant USER_DWIDTH : integer := 32;
      constant ARD_DWIDTH_ARRAY : INTEGER_ARRAY_TYPE :=
          (
            0 => USER_DWIDTH  -- user logic data width
            );

      ---------------------------------------
      -- Constant: array of desired number of chip enables
        --              for each address range
      ---------------------------------------
      constant USER_NUM_CE      : integer            := 10;
      constant ARD_NUM_CE_ARRAY : INTEGER_ARRAY_TYPE :=
          (
            0 => pad_power2(USER_NUM_CE)-- user logic number of CEs
            );
```

```
---------------------------------------
-- Constant: array of unique properties
  --              for each address range
---------------------------------------
constant ARD_DEPENDENT_PROPS_ARRAY :
                     DEPENDENT_PROPS_ARRAY_TYPE :=
    (
      0 => (others => 0)            -- user logic
      );

---------------------------------------
constant PIPELINE_MODEL : integer := 5;

---------------------------------------
-- Constant: user core ID code
---------------------------------------
constant DEV_BLK_ID     : integer := 0;

---------------------------------------
-- Constant: enable MIR/Reset register
---------------------------------------
constant DEV_MIR_ENABLE : integer := 0;

---------------------------------------
constant IP_INTR_MODE_ARRAY : INTEGER_ARRAY_TYPE :=
    (
      0 => 0      -- not used
      );

---------------------------------------
-- Constant: include device interrupt source controller
---------------------------------------
constant INCLUDE_DEV_ISC : integer := 0;

---------------------------------------
-- Constant: include device IID register in device ISC
---------------------------------------
constant INCLUDE_DEV_IID : integer := 0;

---------------------------------------
-- Constant: enable device burst
---------------------------------------
constant DEV_BURST_ENABLE : integer := 0;

---------------------------------------
-- Constant: index for CS/CE
---------------------------------------
constant USER00_CS_INDEX : integer
                   := get_id_index(ARD_ID_ARRAY, USER_00);
constant USER00_CE_INDEX : integer
  := calc_start_ce_index(ARD_NUM_CE_ARRAY, USER00_CS_INDEX);

---------------------------------------
-- IP Interconnect (IPIC) signal declarations
---------------------------------------
signal iBus2IP_RdCE : std_logic_vector(0 to
              calc_num_ce(ARD_NUM_CE_ARRAY)-1);
```

```
      signal iBus2IP_WrCE : std_logic_vector(0 to
                    calc_num_ce(ARD_NUM_CE_ARRAY)-1);
      signal iBus2IP_Data : std_logic_vector(0 to
                    C_OPB_DWIDTH-1);
      signal iBus2IP_BE : std_logic_vector(0 to
                    C_OPB_DWIDTH/8-1);
      signal iIP2Bus_Data : std_logic_vector(0 to
                    C_OPB_DWIDTH*calc_num_ce(ARD_NUM_CE_ARRAY)-1)
                    := (others => '0');
      signal iIP2Bus_Ack : std_logic_vector(0 to
                    ARD_ID_ARRAY'length-1) := (others => '0');
      signal iIP2Bus_Error : std_logic_vector(0 to
                    ARD_ID_ARRAY'length-1) := (others => '0');
      signal iIP2Bus_Retry : std_logic_vector(0 to
                    ARD_ID_ARRAY'length-1) := (others => '0');
      signal iIP2Bus_ToutSup : std_logic_vector(0 to
                    ARD_ID_ARRAY'length-1) := (others => '0');
      signal ZERO_IP2Bus_PostedWrInh : std_logic_vector(0 to
                    ARD_ID_ARRAY'length-1) := (others => '0');
      signal iBus2IP_Clk      : std_logic;
      signal iBus2IP_Reset    : std_logic;
      signal ZERO_IP2Bus_Intr : std_logic_vector(0 to
                    IP_INTR_MODE_ARRAY'length-1)
                    := (others => '0');
      signal uBus2IP_Data     : std_logic_vector(0 to
                                    USER_DWIDTH-1);
      signal uBus2IP_BE       : std_logic_vector(0 to
                                    USER_DWIDTH/8-1);
      signal uBus2IP_RdCE     : std_logic_vector(0 to
                                    USER_NUM_CE-1);
      signal uBus2IP_WrCE     : std_logic_vector(0 to
                                    USER_NUM_CE-1);
      signal uIP2Bus_Data     : std_logic_vector(0 to
                                    USER_DWIDTH-1);
      signal uIP2Bus_Ack      : std_logic;
      signal uIP2Bus_Retry    : std_logic;
      signal uIP2Bus_Error    : std_logic;
      signal uIP2Bus_ToutSup  : std_logic;

begin

     ---------------------------------------
     -- instantiate the OPB IPIF
     ---------------------------------------
     OPB_IPIF_I : entity opb_ipif_v3_00_a.opb_ipif
       generic map
       (
         C_ARD_ID_ARRAY => ARD_ID_ARRAY,
         C_ARD_ADDR_RANGE_ARRAY => ARD_ADDR_RANGE_ARRAY,
         C_ARD_DWIDTH_ARRAY => ARD_DWIDTH_ARRAY,
         C_ARD_NUM_CE_ARRAY => ARD_NUM_CE_ARRAY,
         C_ARD_DEPENDENT_PROPS_ARRAY => ARD_DEPENDENT_PROPS_ARRAY,
         C_PIPELINE_MODEL => PIPELINE_MODEL,
         C_DEV_BLK_ID     => DEV_BLK_ID,
         C_DEV_MIR_ENABLE => DEV_MIR_ENABLE,
         C_AWIDTH => C_OPB_AWIDTH,
         C_DWIDTH => C_OPB_DWIDTH,
```

```
   C_FAMILY => C_FAMILY,
   C_IP_INTR_MODE_ARRAY => IP_INTR_MODE_ARRAY,
   C_INCLUDE_DEV_ISC    => INCLUDE_DEV_ISC,
   C_INCLUDE_DEV_IID    => INCLUDE_DEV_IID,
   C_DEV_BURST_ENABLE   => DEV_BURST_ENABLE
   )
 port map
    (
      OPB_select          => OPB_select,
      OPB_DBus            => OPB_DBus,
      OPB_ABus            => OPB_ABus,
      OPB_BE              => OPB_BE,
      OPB_RNW             => OPB_RNW,
      OPB_seqAddr         => OPB_seqAddr,
      OPB_xferAck         => '0',
      Sln_DBus            => Sl_DBus,
      Sln_xferAck         => Sl_xferAck,
      Sln_errAck          => Sl_errAck,
      Sln_retry           => Sl_retry,
      Sln_toutSup         => Sl_toutSup,
      Bus2IP_CS           => open,
      Bus2IP_CE           => open,
      Bus2IP_RdCE         => iBus2IP_RdCE,
      Bus2IP_WrCE         => iBus2IP_WrCE,
      Bus2IP_Data         => iBus2IP_Data,
      Bus2IP_Addr         => open,
      Bus2IP_BE           => iBus2IP_BE,
      Bus2IP_RNW          => open,
      Bus2IP_Burst        => open,
      IP2Bus_Data         => iIP2Bus_Data,
      IP2Bus_Ack          => iIP2Bus_Ack,
      IP2Bus_Error        => iIP2Bus_Error,
      IP2Bus_Retry        => iIP2Bus_Retry,
      IP2Bus_ToutSup      => iIP2Bus_ToutSup,
      IP2Bus_PostedWrInh  => ZERO_IP2Bus_PostedWrInh,
      OPB_Clk             => OPB_Clk,
      Bus2IP_Clk          => iBus2IP_Clk,
      IP2Bus_Clk          => '0',
      Reset               => OPB_Rst,
      Bus2IP_Reset        => iBus2IP_Reset,
      IP2Bus_Intr         => ZERO_IP2Bus_Intr,
      Device_Intr         => open
      );

---------------------------------------
-- instantiate the User Logic
---------------------------------------
USER_LOGIC_I : entity pwm.user_logic
    generic map
    (
      C_DWIDTH => USER_DWIDTH,
      C_NUM_CE => USER_NUM_CE
      )
    port map
    (
      CLK_PWM        => CLK_PWM,
      enable         => enable,
```

```
            data_valid     => data_valid,
            lut_data       => lut_data,
            subin          => subin,
            switch_off     => switch_off,
            switch_on      => switch_on,
            Bus2IP_Clk     => iBus2IP_Clk,
            Bus2IP_Reset   => iBus2IP_Reset,
            Bus2IP_Data    => uBus2IP_Data,
            Bus2IP_BE      => uBus2IP_BE,
            Bus2IP_RdCE    => uBus2IP_RdCE,
            Bus2IP_WrCE    => uBus2IP_WrCE,
            IP2Bus_Data    => uIP2Bus_Data,
            IP2Bus_Ack     => uIP2Bus_Ack,
            IP2Bus_Retry   => uIP2Bus_Retry,
            IP2Bus_Error   => uIP2Bus_Error,
            IP2Bus_ToutSup => uIP2Bus_ToutSup
            );

  ----------------------------------------
  -- hooking up signal slicing
  ----------------------------------------
  uBus2IP_BE   <= iBus2IP_BE(0 to USER_DWIDTH/8-1);
  uBus2IP_Data <= iBus2IP_Data(0 to USER_DWIDTH-1);
  uBus2IP_RdCE <= iBus2IP_RdCE(USER00_CE_INDEX to
                        USER00_CE_INDEX+USER_NUM_CE-1);
  uBus2IP_WrCE <= iBus2IP_WrCE(USER00_CE_INDEX to
                        USER00_CE_INDEX+USER_NUM_CE-1);
  iIP2Bus_Data(USER00_CE_INDEX*C_OPB_DWIDTH to
    USER00_CE_INDEX*C_OPB_DWIDTH+USER_DWIDTH-1) <= uIP2Bus_Data;
  iIP2Bus_Data((USER00_CE_INDEX+1)*C_OPB_DWIDTH to
    (USER00_CE_INDEX+1)*C_OPB_DWIDTH+USER_DWIDTH-1) <= uIP2Bus_Data;
  iIP2Bus_Data((USER00_CE_INDEX+2)*C_OPB_DWIDTH to
    (USER00_CE_INDEX+2)*C_OPB_DWIDTH+USER_DWIDTH-1) <= uIP2Bus_Data;
  iIP2Bus_Data((USER00_CE_INDEX+3)*C_OPB_DWIDTH to
    (USER00_CE_INDEX+3)*C_OPB_DWIDTH+USER_DWIDTH-1) <= uIP2Bus_Data;
  iIP2Bus_Data((USER00_CE_INDEX+4)*C_OPB_DWIDTH to
    (USER00_CE_INDEX+4)*C_OPB_DWIDTH+USER_DWIDTH-1) <= uIP2Bus_Data;
  iIP2Bus_Data((USER00_CE_INDEX+5)*C_OPB_DWIDTH to
    (USER00_CE_INDEX+5)*C_OPB_DWIDTH+USER_DWIDTH-1) <= uIP2Bus_Data;
  iIP2Bus_Data((USER00_CE_INDEX+6)*C_OPB_DWIDTH to
    (USER00_CE_INDEX+6)*C_OPB_DWIDTH+USER_DWIDTH-1) <= uIP2Bus_Data;
  iIP2Bus_Data((USER00_CE_INDEX+7)*C_OPB_DWIDTH to
    (USER00_CE_INDEX+7)*C_OPB_DWIDTH+USER_DWIDTH-1) <= uIP2Bus_Data;
  iIP2Bus_Data((USER00_CE_INDEX+8)*C_OPB_DWIDTH to
    (USER00_CE_INDEX+8)*C_OPB_DWIDTH+USER_DWIDTH-1) <= uIP2Bus_Data;
  iIP2Bus_Data((USER00_CE_INDEX+9)*C_OPB_DWIDTH to
    (USER00_CE_INDEX+9)*C_OPB_DWIDTH+USER_DWIDTH-1) <= uIP2Bus_Data;
  iIP2Bus_Ack     <= (others => uIP2Bus_ACK);
  iIP2Bus_Retry   <= (others => uIP2Bus_Retry);
  iIP2Bus_Error   <= (others => uIP2Bus_Error);
  iIP2Bus_ToutSup <= (others => uIP2Bus_ToutSup);
end IMP;
```

- Codes for the MPD file

```
##############################################################
## Name     : pwm                                           ##

## Desc     : Microprocessor Peripheral Description         ##
##          : Automatically generated by PsfUtility         ##
##############################################################
BEGIN pwm

## Peripheral Options
OPTION IPTYPE = PERIPHERAL
OPTION IMP_NETLIST = TRUE
OPTION HDL = VHDL

## Bus Interfaces
BUS_INTERFACE BUS = SOPB, BUS_STD = OPB, BUS_TYPE = SLAVE

## Generics for VHDL or Parameters for Verilog
PARAMETER C_BASEADDR = 0xffffffff, DT = std_logic_vector,
   MIN_SIZE = 0x100, BUS = SOPB, ADDRESS = BASE, PAIR = C_HIGHADDR
PARAMETER C_HIGHADDR = 0x00000000, DT = std_logic_vector,
   BUS = SOPB, ADDRESS = HIGH, PAIR = C_BASEADDR
PARAMETER C_OPB_AWIDTH = 32, DT = INTEGER, BUS = SOPB
PARAMETER C_OPB_DWIDTH = 32, DT = INTEGER, BUS = SOPB
PARAMETER C_USER_ID_CODE = 3, DT = INTEGER
PARAMETER C_FAMILY = virtex2p, DT = STRING

## Ports
PORT OPB_Clk = "", DIR = I, SIGIS = Clk, BUS = SOPB
PORT OPB_Rst = OPB_Rst, DIR = I, SIGIS = Rst, BUS = SOPB
PORT Sl_DBus = Sl_DBus, DIR = O, VEC = [0:(C_OPB_DWIDTH-1)],
            BUS = SOPB
PORT Sl_errAck = Sl_errAck, DIR = O, BUS = SOPB
PORT Sl_retry = Sl_retry, DIR = O, BUS = SOPB
PORT Sl_toutSup = Sl_toutSup, DIR = O, BUS = SOPB
PORT Sl_xferAck = Sl_xferAck, DIR = O, BUS = SOPB
PORT OPB_ABus = OPB_ABus, DIR = I, VEC = [0:(C_OPB_AWIDTH-1)],
            BUS = SOPB
PORT OPB_BE = OPB_BE, DIR = I, VEC = [0:((C_OPB_DWIDTH/8)-1)],
            BUS = SOPB
PORT OPB_DBus = OPB_DBus, DIR = I, VEC = [0:(C_OPB_DWIDTH-1)],
            BUS = SOPB
PORT OPB_RNW = OPB_RNW, DIR = I, BUS = SOPB
PORT OPB_select = OPB_select, DIR = I, BUS = SOPB
PORT OPB_seqAddr = OPB_seqAddr, DIR = I, BUS = SOPB

## PWM_ctrl signals
PORT CLK_PWM = "", DIR = I, SIGIS = CLK
PORT enable = "",DIR = O
PORT data_valid = "",DIR = O
PORT lut_data = "",DIR = O, VEC = [0:18]
PORT switch_off = "",DIR = O, SIGIS = CLK
PORT switch_on = "",DIR = O, SIGIS = CLK

END
```

C.5. SW_CTRL

The SW_CTRL module receives 2-bit data from the external lookup table, and decodes them into gate signals. The ``break before make'' logic was also implemented in this module using ``turn-off'' and ``turn-on'' signals from the PWM controller circuit. The prototype of the control circuit contains nine of the switch cell controller circuits; one per each switch cell.

Note that these modules were not connected to any bus; hence, there is no HDL peripheral definition file for these modules.

- Codes for the user logic file

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity sw_ctrl is
  port(
          SS : in std_logic_vector(0 to 1);
          switch_on  : in bit;
          switch_off : in bit;
          S_out : out std_logic_vector(0 to 3)
      );
end sw_ctrl;

architecture Behavioral of sw_ctrl is
  signal next_switch : std_logic_vector(0 to 3);
  signal CLK_S0,CLK_S1,CLK_S2,CLK_S3 : bit;
  signal S0_temp,S1_temp,S2_temp,S3_temp : std_logic;
  signal S0,S1,S2,S3 : std_logic;
  signal upper_S, lower_s, L_ctrl : std_logic;
  signal L : bit := '1';

begin
process (SS,L)
begin
  case (SS) is
    when "00" =>
      next_switch <= "0000";
    when "01" =>
      next_switch <= "1001";
    when "10" =>
      next_switch <= "0110";
    when "11" =>
      if (L ='0') then
        next_switch <= "0011";
      else
        next_switch <= "1100";
      end if;
    when others =>
  end case;
end process;

CLK_S0 <= switch_off when (next_switch(0) and ( not S0_temp))
```

```
          = '0' else switch_on;
CLK_S1 <= switch_off when (next_switch(1) and ( not S1_temp))
          = '0' else switch_on;
CLK_S2 <= switch_off when (next_switch(2) and ( not S2_temp))
          = '0' else switch_on;
CLK_S3 <= switch_off when (next_switch(3) and ( not S3_temp))
          = '0' else switch_on;

process (CLK_S0)
begin
  if (CLK_S0'event and CLK_S0 = '1') then
    S0_temp <= next_switch(0);
  end if;
end process;

process (CLK_S1)
begin
  if (CLK_S1'event and CLK_S1 = '1') then
    S1_temp <= next_switch(1);
  end if;
end process;

process (CLK_S2)
begin
  if (CLK_S2'event and CLK_S2 = '1') then
    S2_temp <= next_switch(2);
  end if;
end process;

process (CLK_S3)
begin
  if (CLK_S3'event and CLK_S3 = '1') then
    S3_temp <= next_switch(3);
  end if;
end process;

S0 <= S0_temp and (not S2_temp);
S1 <= S1_temp and (not S3_temp);
S2 <= S2_temp and (not S0_temp);
S3 <= S3_temp and (not S1_temp);

upper_S <= S2 and S3;
lower_S <= S0 and S1;
L_ctrl <= upper_S or lower_S;

process (L_ctrl)
begin
  if (L_ctrl'event and L_ctrl = '0') then
    L <= not L;
  end if;
end process;

S_out(0) <= S0;
S_out(1) <= S1;
S_out(2) <= S2;
S_out(3) <= S3;
```

```
end Behavioral;
```

- Codes for the MPD file

```
##############################################################################
## Name     : sw_ctrl                                                       ##
## Desc     : Microprocessor Peripheral Description                         ##
##          : Automatically generated by PsfUtility                         ##
##############################################################################

BEGIN sw_ctrl

## Peripheral Options
OPTION IPTYPE = PERIPHERAL
OPTION IMP_NETLIST = TRUE
OPTION HDL = VHDL

## Ports
PORT SS = "", DIR = I, VEC = [0:1]
PORT switch_on = "", DIR = I, SIGIS = CLK
PORT switch_off = "", DIR = I, SIGIS = CLK
PORT S_out = "", DIR = O, VEC = [0:3]

END
```

C.6. CAP_REG

The CAP_REG module is used in the capacitor voltage balancing scheme. It receives combinations of two capacitors as an input, and provides set of opposite space vectors and currents as an output.

- Codes for the user logic file

```
------------------------------------------------------------------------------
-- user_logic.vhd - entity/architecture pair
------------------------------------------------------------------------------
-- Filename:          user_logic.vhd
-- Version:
-- Description:       User logic module.
-- Date:              Thu May 12 10:46:42 2005
--                      (by Create/Import Peripheral Wizard)
-- VHDL-Standard:     VHDL'93
------------------------------------------------------------------------------
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;
use ieee.std_logic_unsigned.all;

library proc_common_v1_00_b;
use proc_common_v1_00_b.proc_common_pkg.all;

entity user_logic is
  generic
    (
```

```
      current : std_logic_vector :=x"000A";
      C_DWIDTH    : integer   := 16;
      C_NUM_CE    : integer   := 11
      );
  port
    (
      Iin_A,Iin_B,Iin_C    : in std_logic_vector(0 to 15);
      Iout_a,Iout_b,Iout_c : in std_logic_vector(0 to 15);
      -- Bus protocol ports, do not add to or delete
      Bus2IP_Clk     : in  std_logic;
      Bus2IP_Reset   : in  std_logic;
      Bus2IP_Data    : in  std_logic_vector(0 to C_DWIDTH-1);
      Bus2IP_BE      : in  std_logic_vector(0 to C_DWIDTH/8-1);
      Bus2IP_RdCE    : in  std_logic_vector(0 to C_NUM_CE-1);
      Bus2IP_WrCE    : in  std_logic_vector(0 to C_NUM_CE-1);
      Bus2IP_RdReq   : in  std_logic;
      Bus2IP_WrReq   : in  std_logic;
      IP2Bus_Data    : out std_logic_vector(0 to C_DWIDTH-1);
      IP2Bus_Retry   : out std_logic;
      IP2Bus_Error   : out std_logic;
      IP2Bus_ToutSup : out std_logic;
      IP2Bus_RdAck   : out std_logic;
      IP2Bus_WrAck   : out std_logic
      );
end entity user_logic;

------------------------------------------------------------------------
-- Architecture section
------------------------------------------------------------------------
architecture IMP of user_logic is

      ---------------------------------------
      -- User logic S/W accessible registers
      ---------------------------------------
      signal reg0 : std_logic_vector(0 to C_DWIDTH-1);
      signal reg1 : std_logic_vector(0 to C_DWIDTH-1);
      signal reg2 : std_logic_vector(0 to C_DWIDTH-1);
      signal reg3 : std_logic_vector(0 to C_DWIDTH-1);
      signal reg4 : std_logic_vector(0 to C_DWIDTH-1);
      signal reg5 : std_logic_vector(0 to C_DWIDTH-1);
      signal reg6 : std_logic_vector(0 to C_DWIDTH-1);
      signal reg7 : std_logic_vector(0 to C_DWIDTH-1);
      signal reg8 : std_logic_vector(0 to C_DWIDTH-1);
      signal reg9 : std_logic_vector(0 to C_DWIDTH-1);
      signal reg10      : std_logic_vector(0 to C_DWIDTH-1);
      signal reg_write_select : std_logic_vector(0 to 10);
      signal reg_read_select  : std_logic_vector(0 to 10);
      signal reg_2cap : std_logic_vector(0 to 8);

begin
      ---------------------------------------
      -- Map user logic S/W register read/write select signal
      ---------------------------------------
      reg_write_select <= Bus2IP_WrCE;
      reg_read_select <= Bus2IP_RdCE;

      ---------------------------------------
```

```
-- User logic S/W accessible registers write example
---------------------------------------
REG_WRITE_PROC : process( Bus2IP_Clk ) is
begin
    if Bus2IP_Clk'event and Bus2IP_Clk = '1' then
      if Bus2IP_Reset = '1' then
        reg0 <= (others => '0');
      else
        case reg_write_select is
          when "10000000000" => reg0 <= Bus2IP_Data;
          when others => null;
        end case;
      end if;
    end if;
end process REG_WRITE_PROC;

---------------------------------------
-- User logic S/W accessible registers read example
---------------------------------------
REG_READ_PROC : process( reg_read_select, reg0, reg1,
                         reg2, reg3, reg4, reg5, reg6,
                         reg7, reg8, reg9, reg10 ) is
begin
    case reg_read_select is
      when "10000000000" => IP2Bus_Data <= reg0;
      when "01000000000" => IP2Bus_Data <= reg1;
      when "00100000000" => IP2Bus_Data <= reg2;
      when "00010000000" => IP2Bus_Data <= reg3;
      when "00001000000" => IP2Bus_Data <= reg4;
      when "00000100000" => IP2Bus_Data <= reg5;
      when "00000010000" => IP2Bus_Data <= reg6;
      when "00000001000" => IP2Bus_Data <= reg7;
      when "00000000100" => IP2Bus_Data <= reg8;
      when "00000000010" => IP2Bus_Data <= reg9;
      when "00000000001" => IP2Bus_Data <= reg10;
      when others => IP2Bus_Data <= (others => '0');
    end case;
end process REG_READ_PROC;

---------------------------------------
-- Simple example to drive IP2Bus signals
---------------------------------------
IP2Bus_WrAck <= Bus2IP_WrCE(0) or Bus2IP_WrCE(1) or
                Bus2IP_WrCE(2) or Bus2IP_WrCE(3) or
                Bus2IP_WrCE(4) or Bus2IP_WrCE(5) or
                Bus2IP_WrCE(6) or Bus2IP_WrCE(7) or
                Bus2IP_WrCE(8) or Bus2IP_WrCE(9) or
                Bus2IP_WrCE(10);
IP2Bus_RdAck <= Bus2IP_RdCE(0) or Bus2IP_RdCE(1) or
                Bus2IP_RdCE(2) or Bus2IP_RdCE(3) or
                Bus2IP_RdCE(4) or Bus2IP_RdCE(5) or
                Bus2IP_RdCE(6) or Bus2IP_RdCE(7) or
                Bus2IP_RdCE(8) or Bus2IP_RdCE(9) or
                Bus2IP_RdCE(10);
IP2Bus_Error <= '0';
IP2Bus_Retry <= '0';
IP2Bus_ToutSup <= '0';
```

```
reg_2cap <= reg0(7 to 15);

process(reg_2cap) is
begin
    case reg_2cap is
      when b"0_0000_0011" =>  reg1 <= x"0000";-(CAa,CAb)
                              reg2 <= current;
                              reg3 <= x"1040";
                              reg4 <= (Iin_A);
                              reg5 <= x"1542";
                              reg6 <= (Iin_A-Iout_c);
                              reg7 <= x"5225";
                              reg8 <= (Iin_C+Iout_c);
                              reg9 <= x"3265";
                              reg10 <= (Iin_B+Iout_c);
      when b"0_0000_0101" =>  reg1 <= x"0000";--(CAa,CAc)
                              reg2 <= current;
                              reg3 <= x"1040";
                              reg4 <= (Iin_A);
                              reg5 <= x"1346";
                              reg6 <= (Iin_A-Iout_b);
                              reg7 <= x"5623";
                              reg8 <= (Iin_C+Iout_b);
                              reg9 <= x"3663";
                              reg10 <= (Iin_B+Iout_b);
      when b"0_0000_1001" =>  reg1 <= x"0000";--(CAa,CBa)
                              reg2 <= current;
                              reg3 <= x"0401";
                              reg4 <= (Iout_a);
                              reg5 <= x"5623";
                              reg6 <= (Iin_C+Iout_b);
                              reg7 <= x"5124";
                              reg8 <= (Iin_C-Iout_a);
                              reg9 <= x"5225";
                              reg10 <= (Iin_C+Iout_c);
      when b"0_0001_0001" =>  reg1 <= x"1346";--Aa,CBb)
                              reg2 <= (Iin_A-Iout_b);
                              reg3 <= x"1441";
                              reg4 <= (Iin_A+Iout_a);
                              reg5 <= x"5225";
                              reg6 <= (Iin_C+Iout_c);
                              reg7 <= x"3164";
                              reg8 <= (Iin_B-Iout_a);
                              reg9 <= x"3663";
                              reg10 <= (Iin_B+Iout_b);
      when b"0_0010_0001" =>  reg1 <= x"1441";--(CAa,CBc)
                              reg2 <= (Iin_A+Iout_a);
                              reg3 <= x"1542";
                              reg4 <= (Iin_A-Iout_c);
                              reg5 <= x"5623";
                              reg6 <= (Iin_C+Iout_b);
                              reg7 <= x"3164";
                              reg8 <= (Iin_B-Iout_a);
                              reg9 <= x"3265";
                              reg10 <= (Iin_B+Iout_c);
      when b"0_0100_0001" =>  reg1 <= x"0000";--(CAa,CCa)
```

```
                        reg2 <= current;
                        reg3 <= x"0401";
                        reg4 <= (Iout_a);
                        reg5 <= x"3164";
                        reg6 <= (Iin_B-Iout_a);
                        reg7 <= x"3265";
                        reg8 <= (Iin_B+Iout_c);
                        reg9 <= x"3663";
                        reg10 <= (Iin_B+Iout_b);
when b"0_1000_0001" =>  reg1 <= x"1346";--(CAa,CCb)
                        reg2 <= (Iin_A-Iout_b);
                        reg3 <= x"1441";
                        reg4 <= (Iin_A+Iout_a);
                        reg5 <= x"5623";
                        reg6 <= (Iin_C+Iout_b);
                        reg7 <= x"5124";
                        reg8 <= (Iin_C-Iout_a);
                        reg9 <= x"3265";
                        reg10 <= (Iin_B+Iout_c);
when b"1_0000_0001" =>  reg1 <= x"1441";--(CAa,CCc)
                        reg2 <= (Iin_A+Iout_a);
                        reg3 <= x"1542";
                        reg4 <= (Iin_A-Iout_c);
                        reg5 <= x"5124";
                        reg6 <= (Iin_C-Iout_a);
                        reg7 <= x"5225";
                        reg8 <= (Iin_C+Iout_c);
                        reg9 <= x"3663";
                        reg10 <= (Iin_B+Iout_b);
when b"0_0000_0110" =>  reg1 <= x"0000";--(CAb,CAc)
                        reg2 <= current;
                        reg3 <= x"1040";
                        reg4 <= (Iin_A);
                        reg5 <= x"1144";
                        reg6 <= (Iin_A-Iout_a);
                        reg7 <= x"5421";
                        reg8 <= (Iin_C+Iout_a);
                        reg9 <= x"3461";
                        reg10 <= (Iin_B+Iout_a);
when b"0_0000_1010" =>  reg1 <= x"1144";--(CAb,CBa)
                        reg2 <= (Iin_A-Iout_a);
                        reg3 <= x"1643";
                        reg4 <= (Iin_A+Iout_b);
                        reg5 <= x"5225";
                        reg6 <= (Iin_C+Iout_c);
                        reg7 <= x"3366";
                        reg8 <= (Iin_B-Iout_b);
                        reg9 <= x"3461";
                        reg10 <= (Iin_B+Iout_a);
when b"0_0001_0010" =>  reg1 <= x"0000";--(CAb,CBb)
                        reg2 <= current;
                        reg3 <= x"0603";
                        reg4 <= (Iout_b);
                        reg5 <= x"5421";
                        reg6 <= (Iin_C+Iout_a);
                        reg7 <= x"5225";
                        reg8 <= (Iin_C+Iout_c);
```

```
                        reg9 <= x"5326";
                        reg10 <= (Iin_C-Iout_b);
when b"0_0010_0010" =>  reg1 <= x"1542";--(CAb,CBc)
                        reg2 <= (Iin_A-Iout_c);
                        reg3 <= x"1643";
                        reg4 <= (Iin_A+Iout_b);
                        reg5 <= x"5421";
                        reg6 <= (Iin_C+Iout_a);
                        reg7 <= x"3265";
                        reg8 <= (Iin_B+Iout_c);
                        reg9 <= x"3366";
                        reg10 <= (Iin_B-Iout_b);
when b"0_0100_0010" =>  reg1 <= x"1144";--(CAb,CCa)
                        reg2 <= (Iin_A-Iout_a);
                        reg3 <= x"1643";
                        reg4 <= (Iin_A+Iout_b);
                        reg5 <= x"5421";
                        reg6 <= (Iin_C+Iout_a);
                        reg7 <= x"5326";
                        reg8 <= (Iin_C-Iout_b);
                        reg9 <= x"3265";
                        reg10 <= (Iin_B+Iout_c);
when b"0_1000_0010" =>  reg1 <= x"0000";--(CAb,CCb)
                        reg2 <= current;
                        reg3 <= x"0603";
                        reg4 <= (Iout_b);
                        reg5 <= x"3265";
                        reg6 <= (Iin_B+Iout_c);
                        reg7 <= x"3366";
                        reg8 <= (Iin_B-Iout_b);
                        reg9 <= x"3461";
                        reg10 <= (Iin_B+Iout_a);
when b"1_0000_0010" =>  reg1 <= x"1542";--(CAb,CCc)
                        reg2 <= (Iin_A-Iout_c);
                        reg3 <= x"1643";
                        reg4 <= (Iin_A+Iout_b);
                        reg5 <= x"5225";
                        reg6 <= (Iin_C+Iout_c);
                        reg7 <= x"5326";
                        reg8 <= (Iin_C-Iout_b);
                        reg9 <= x"3461";
                        reg10 <= (Iin_B+Iout_a);
when b"0_0000_1100" =>  reg1 <= x"1144";--(CAc,CBa)
                        reg2 <= (Iin_A-Iout_a);
                        reg3 <= x"1245";
                        reg4 <= (Iin_A+Iout_c);
                        reg5 <= x"5623";
                        reg6 <= (Iin_C+Iout_b);
                        reg7 <= x"3461";
                        reg8 <= (Iin_B+Iout_a);
                        reg9 <= x"3562";
                        reg10 <= (Iin_B-Iout_c);
when b"0_0001_0100" =>  reg1 <= x"1245";--(CAc,CBb)
                        reg2 <= (Iin_A+Iout_c);
                        reg3 <= x"1346";
                        reg4 <= (Iin_A-Iout_b);
                        reg5 <= x"5421";
```

```
                        reg6 <= (Iin_C+Iout_a);
                        reg7 <= x"3562";
                        reg8 <= (Iin_B-Iout_c);
                        reg9 <= x"3663";
                        reg10 <= (Iin_B+Iout_b);
when b"0_0010_0100" =>  reg1 <= x"0000";--(CAc,CBc)
                        reg2 <= current;
                        reg3 <= x"0205";
                        reg4 <= (Iout_c);
                        reg5 <= x"5421";
                        reg6 <= (Iin_C+Iout_a);
                        reg7 <= x"5522";
                        reg8 <= (Iin_C-Iout_c);
                        reg9 <= x"5623";
                        reg10 <= (Iin_C+Iout_b);
when b"0_0100_0100" =>  reg1 <= x"1144";--(CAc,CCa)
                        reg2 <= (Iin_A-Iout_a);
                        reg3 <= x"1245";
                        reg4 <= (Iin_A+Iout_c);
                        reg5 <= x"5421";
                        reg6 <= (Iin_C+Iout_a);
                        reg7 <= x"5522";
                        reg8 <= (Iin_C-Iout_c);
                        reg9 <= x"3663";
                        reg10 <= (Iin_B+Iout_b);
when b"0_1000_0100" =>  reg1 <= x"1245";--(CAc,CCb)
                        reg2 <= (Iin_A+Iout_c);
                        reg3 <= x"1346";
                        reg4 <= (Iin_A-Iout_b);
                        reg5 <= x"5522";
                        reg6 <= (Iin_C-Iout_c);
                        reg7 <= x"5623";
                        reg8 <= (Iin_C+Iout_b);
                        reg9 <= x"3461";
                        reg10 <= (Iin_B+Iout_a);
when b"1_0000_0100" =>  reg1 <= x"0000";--(CAc,CCc)
                        reg2 <= current;
                        reg3 <= x"0205";
                        reg4 <= (Iout_c);
                        reg5 <= x"3461";
                        reg6 <= (Iin_B+Iout_a);
                        reg7 <= x"3562";
                        reg8 <= (Iin_B-Iout_c);
                        reg9 <= x"3663";
                        reg10 <= (Iin_B+Iout_b);
when b"0_0001_1000" =>  reg1 <= x"0000";--(CBa,CBb)
                        reg2 <= current;
                        reg3 <= x"1245";
                        reg4 <= (Iin_A+Iout_c);
                        reg5 <= x"5225";
                        reg6 <= (Iin_C+Iout_c);
                        reg7 <= x"3060";
                        reg8 <= (Iin_B);
                        reg9 <= x"3562";
                        reg10 <= (Iin_B-Iout_c);
when b"0_0010_1000" =>  reg1 <= x"0000";--(CBa,CBc)
                        reg2 <= current;
```

```
                        reg3 <= x"1643";
                        reg4 <= (Iin_A+Iout_b);
                        reg5 <= x"5623";
                        reg6 <= (Iin_C+Iout_b);
                        reg7 <= x"3060";
                        reg8 <= (Iin_B);
                        reg9 <= x"3366";
                        reg10 <= (Iin_B-Iout_b);
when b"0_0100_1000" =>  reg1 <= x"0000";--(CBa,CCa)
                        reg2 <= current;
                        reg3 <= x"0401";
                        reg4 <= (Iout_a);
                        reg5 <= x"1144";
                        reg6 <= (Iin_A-Iout_a);
                        reg7 <= x"1245";
                        reg8 <= (Iin_A+Iout_c);
                        reg9 <= x"1643";
                        reg10 <= (Iin_A+Iout_b);
when b"0_1000_1000" =>  reg1 <= x"1245";--(CBa,CCb)
                        reg2 <= (Iin_A+Iout_c);
                        reg3 <= x"5623";
                        reg4 <= (Iin_C+Iout_b);
                        reg5 <= x"5124";
                        reg6 <= (Iin_C-Iout_a);
                        reg7 <= x"3366";
                        reg8 <= (Iin_B-Iout_b);
                        reg9 <= x"3461";
                        reg10 <= (Iin_B+Iout_a);
when b"1_0000_1000" =>  reg1 <= x"1643";--(CBa,CCc)
                        reg2 <= (Iin_A+Iout_b);
                        reg3 <= x"5124";
                        reg4 <= (Iin_C-Iout_a);
                        reg5 <= x"5225";
                        reg6 <= (Iin_C+Iout_c);
                        reg7 <= x"3461";
                        reg8 <= (Iin_B+Iout_a);
                        reg9 <= x"3562";
                        reg10 <= (Iin_B-Iout_c);
when b"0_0011_0000" =>  reg1 <= x"0000";--(CBb,CBc)
                        reg2 <= current;
                        reg3 <= x"1441";
                        reg4 <= (Iin_A+Iout_a);
                        reg5 <= x"5421";
                        reg6 <= (Iin_C+Iout_a);
                        reg7 <= x"3060";
                        reg8 <= (Iin_B);
                        reg9 <= x"3164";
                        reg10 <= (Iin_B-Iout_a);
when b"0_0101_0000" =>  reg1 <= x"1245";--(CBb,CCa)
                        reg2 <= (IIn_A+Iout_c);
                        reg3 <= x"5421";
                        reg4 <= (Iin_C+Iout_a);
                        reg5 <= x"5326";
                        reg6 <= (Iin_C-Iout_b);
                        reg7 <= x"3164";
                        reg8 <= (Iin_B-Iout_a);
                        reg9 <= x"3663";
```

```
                            reg10 <= (Iin_B+Iout_b);
when b"0_1001_0000" =>      reg1 <= x"0000";--(CBb,CCb)
                            reg2 <= current;
                            reg3 <= x"1245";
                            reg4 <= (Iin_A+Iout_c);
                            reg5 <= x"0603";
                            reg6 <= (Iout_b);
                            reg7 <= x"1346";
                            reg8 <= (Iin_A-Iout_b);
                            reg9 <= x"1441";
                            reg10 <= (Iin_A+Iout_a);
when b"1_0001_0000" =>      reg1 <= x"1441";--(CBb,CCc)
                            reg2 <= (Iin_A+Iout_a);
                            reg3 <= x"5225";
                            reg4 <= (Iin_C+Iout_c);
                            reg5 <= x"5326";
                            reg6 <= (Iin_C-Iout_b);
                            reg7 <= x"3562";
                            reg8 <= (Iin_B-Iout_c);
                            reg9 <= x"3663";
                            reg10 <= (Iin_B+Iout_b);
when b"0_0110_0000" =>      reg1 <= x"1643";--(CBc,CCa)
                            reg2 <= (Iin_A+Iout_b);
                            reg3 <= x"5421";
                            reg4 <= (Iin_C+Iout_a);
                            reg5 <= x"5522";
                            reg6 <= (Iin_C-Iout_c);
                            reg7 <= x"3164";
                            reg8 <= (Iin_B-Iout_a);
                            reg9 <= x"3265";
                            reg10 <= (Iin_B+Iout_c);
when b"0_1010_0000" =>      reg1 <= x"1441";--(CBc,CCb)
                            reg2 <= (Iin_A+Iout_a);
                            reg3 <= x"5522";
                            reg4 <= (Iin_C-Iout_c);
                            reg5 <= x"5623";
                            reg6 <= (Iin_C-Iout_b);
                            reg7 <= x"3265";
                            reg8 <= (Iin_B+Iout_c);
                            reg9 <= x"3366";
                            reg10 <= (Iin_B-Iout_b);
when b"1_0010_0000" =>      reg1 <= x"0000";--(CBc,CCc)
                            reg2 <= current;
                            reg3 <= x"0205";
                            reg4 <= (Iout_c);
                            reg5 <= x"1441";
                            reg6 <= (Iin_A+Iout_a);
                            reg7 <= x"1542";
                            reg8 <= (Iin_A-Iout_c);
                            reg9 <= x"1643";
                            reg10 <= (Iin_A+Iout_b);
when b"0_1100_0000" =>      reg1 <= x"0000";--(CCa,CCb)
                            reg2 <= current;
                            reg3 <= x"1245";
                            reg4 <= (Iin_A+Iout_c);
                            reg5 <= x"5020";
                            reg6 <= (Iin_C);
```

```
                                    reg7 <= x"5522";
                                    reg8 <= (Iin_C-Iout_c);
                                    reg9 <= x"3265";
                                    reg10 <= (Iin_B+Iout_c);
            when b"1_0100_0000" =>  reg1 <= x"0000";--(CCa,CCc)
                                    reg2 <= current;
                                    reg3 <= x"1643";
                                    reg4 <= (Iin_A+Iout_b);
                                    reg5 <= x"5020";
                                    reg6 <= (Iin_C);
                                    reg7 <= x"5326";
                                    reg8 <= (Iin_C-Iout_b);
                                    reg9 <= x"3663";
                                    reg10 <= (Iin_B+Iout_b);
            when b"1_1000_0000" =>  reg1 <= x"0000";--(CCb,CCc)
                                    reg2 <= current;
                                    reg3 <= x"1441";
                                    reg4 <= (Iin_A+Iout_a);
                                    reg5 <= x"5020";
                                    reg6 <= (Iin_C);
                                    reg7 <= x"5124";
                                    reg8 <= (Iin_C-Iout_a);
                                    reg9 <= x"3461";
                                    reg10 <= (Iin_B+Iout_a);
            when others =>          reg1 <= x"0000";
                                    reg2 <= current;
                                    reg3 <= x"0000";
                                    reg4 <= current;
                                    reg5 <= x"0000";
                                    reg6 <= current;
                                    reg7 <= x"0000";
                                    reg8 <= current;
                                    reg9 <= x"0000";
                                    reg10 <= current;
        end case;
    end process;
end IMP;
```

- Codes for the HDL peripheral definition file

```
------------------------------------------------------------------
-- Cap_reg.vhd - entity/architecture pair
------------------------------------------------------------------
-- Filename:          Cap_reg.vhd
-- Version:
-- Description:       Top level design, instantiates IPIF and
--                              user logic.
-- Date:              Thu May 12 10:46:42 2005
--                         (by Create/Import Peripheral Wizard)
-- VHDL-Standard:     VHDL'93
------------------------------------------------------------------
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;
use ieee.std_logic_unsigned.all;
```

```
library proc_common_v1_00_b;
use proc_common_v1_00_b.proc_common_pkg.all;

library ipif_common_v1_00_b;
use ipif_common_v1_00_b.ipif_pkg.all;

library plb_ipif_v1_00_e;
use plb_ipif_v1_00_e.all;

library Cap_reg;
use Cap_reg.all;

------------------------------------------------------------------------
-- Entity section
------------------------------------------------------------------------

entity Cap_reg is
  generic
    (
      -- Bus protocol parameters, do not add to or delete
      C_BASEADDR  : std_logic_vector := X"FFFFFFFF";
      C_HIGHADDR  : std_logic_vector := X"00000000";
      C_PLB_AWIDTH      : integer := 32;
      C_PLB_DWIDTH      : integer := 64;
      C_PLB_NUM_MASTERS : integer := 8;
      C_PLB_MID_WIDTH   : integer := 3;
      C_USER_ID_CODE    : integer := 3;
      C_FAMILY          : string  := "virtex2p"
      );
  port
    (
      Iin_A,Iin_B,Iin_C : in std_logic_vector(0 to 15);
      Iout_a,Iout_b,Iout_c : in std_logic_vector(0 to 15);
      -- Bus protocol ports, do not add to or delete
      PLB_Clk        : in  std_logic;
      PLB_Rst        : in  std_logic;
      Sl_addrAck     : out std_logic;
      Sl_rdBTerm     : out std_logic;
      Sl_rdComp      : out std_logic;
      Sl_rdDAck      : out std_logic;
      Sl_rdWdAddr    : out std_logic_vector(0 to 3);
      Sl_rearbitrate : out std_logic;
      Sl_SSize       : out std_logic_vector(0 to 1);
      Sl_wait        : out std_logic;
      Sl_wrBTerm     : out std_logic;
      Sl_wrComp      : out std_logic;
      Sl_wrDAck      : out std_logic;
      PLB_abort      : in  std_logic;
      PLB_busLock    : in  std_logic;
      PLB_compress   : in  std_logic;
      PLB_guarded    : in  std_logic;
      PLB_lockErr    : in  std_logic;
      PLB_MSize      : in  std_logic_vector(0 to 1);
      PLB_ordered    : in  std_logic;
      PLB_PAValid    : in  std_logic;
      PLB_pendPri    : in  std_logic_vector(0 to 1);
      PLB_pendReq    : in  std_logic;
```

```
      PLB_rdBurst    : in  std_logic;
      PLB_rdPrim     : in  std_logic;
      PLB_reqPri     : in  std_logic_vector(0 to 1);
      PLB_RNW        : in  std_logic;
      PLB_SAValid    : in  std_logic;
      PLB_size       : in  std_logic_vector(0 to 3);
      PLB_type       : in  std_logic_vector(0 to 2);
      PLB_wrBurst    : in  std_logic;
      PLB_wrPrim     : in  std_logic;
      PLB_wrDBus     : in  std_logic_vector(0 to C_PLB_DWIDTH-1);
      PLB_ABus       : in  std_logic_vector(0 to C_PLB_AWIDTH-1);
      PLB_BE       : in  std_logic_vector(0 to C_PLB_DWIDTH/8-1);
      PLB_masterID : in  std_logic_vector(0 to C_PLB_MID_WIDTH-1);
      Sl_rdDBus : out std_logic_vector(0 to C_PLB_DWIDTH-1);
      Sl_MBusy  : out std_logic_vector(0 to C_PLB_NUM_MASTERS-1);
      Sl_MErr   : out std_logic_vector(0 to C_PLB_NUM_MASTERS-1)
      );

  attribute MIN_SIZE : string;
  attribute MIN_SIZE of C_BASEADDR : constant is "0x100";
  attribute SIGIS : string;
  attribute SIGIS of PLB_Clk : signal is "Clk";
  attribute SIGIS of PLB_Rst : signal is "Rst";

end entity Cap_reg;

------------------------------------------------------------------------
-- Architecture section
------------------------------------------------------------------------

architecture IMP of Cap_reg is

  ---------------------------------------
  -- Constant: array of address range identifiers
  ---------------------------------------
  constant ARD_ID_ARRAY : INTEGER_ARRAY_TYPE :=
    (
      0 => USER_00 -- user logic S/W register address space
      );

  ---------------------------------------
  -- Constant: array of address pairs for each address range
  ---------------------------------------
  constant ZERO_ADDR_PAD : std_logic_vector(0 to 64-C_PLB_AWIDTH-1)
                           := (others => '0');
  constant USER_BASEADDR : std_logic_vector
                           := C_BASEADDR or X"00000000";
  constant USER_HIGHADDR : std_logic_vector
                           := C_BASEADDR or X"000000FF";

  constant ARD_ADDR_RANGE_ARRAY     : SLV64_ARRAY_TYPE :=
    (
      ZERO_ADDR_PAD & USER_BASEADDR,-- user logic base address
      ZERO_ADDR_PAD & USER_HIGHADDR -- user logic high address
      );

  ---------------------------------------
```

```
-- Constant: array of data widths for each target address range
---------------------------------------
constant USER_DWIDTH      : integer            := 16;
constant ARD_DWIDTH_ARRAY : INTEGER_ARRAY_TYPE :=
  (
    0 => USER_DWIDTH        -- user logic data width
    );

---------------------------------------
-- Constant: array of desired number of chip enables
--           for each address range
---------------------------------------
constant USER_NUM_CE      : integer            := 11;
constant ARD_NUM_CE_ARRAY : INTEGER_ARRAY_TYPE :=
  (
    0 => pad_power2(USER_NUM_CE)-- user logic number of CEs
    );

---------------------------------------
-- Constant: user core ID code
---------------------------------------
constant DEV_BLK_ID : integer := 0;

---------------------------------------
-- Constant: enable MIR/Reset register
---------------------------------------
constant DEV_MIR_ENABLE : boolean := false;

---------------------------------------
-- Constant: enable burst support
---------------------------------------
constant DEV_BURST_ENABLE : boolean := false;

---------------------------------------
-- Constant: use fast transfer protocol for burst and cacheline
---------------------------------------
constant DEV_FAST_DATA_XFER : boolean := false;

---------------------------------------
-- Constant: max burst size in bytes - reserved
---------------------------------------
constant DEV_MAX_BURST_SIZE : integer := 64;

---------------------------------------
-- Constant: size of the largest target burstable memory
-- space in bytes - reserved
---------------------------------------
constant DEV_BURST_PAGE_SIZE : integer := 1024;

---------------------------------------
-- Constant: dataphase timeout value for IPIF
---------------------------------------
constant DEV_DPHASE_TIMEOUT : integer := 64;

---------------------------------------
-- Constant: include device interrupt source controller
---------------------------------------
```

```
constant INCLUDE_DEV_ISC : boolean := false;

---------------------------------------
-- Constant: include IPIF ISC priority encoder
---------------------------------------
constant INCLUDE_DEV_PENCODER : boolean := false;

---------------------------------------
constant IP_INTR_MODE_ARRAY : INTEGER_ARRAY_TYPE :=
  (
    0 => 0      -- not used
    );

---------------------------------------
-- Constant: include PLB master service - reserved
---------------------------------------
constant IP_MASTER_PRESENT : boolean := false;

---------------------------------------
-- Constant: write FIFO depth
---------------------------------------
constant WRFIFO_DEPTH : integer := 512;

---------------------------------------
-- Constant: include write FIFO packet mode service
---------------------------------------
constant WRFIFO_INCLUDE_PACKET_MODE : boolean := false;

---------------------------------------
-- Constant: include write FIFO vacancy status
---------------------------------------
constant WRFIFO_INCLUDE_VACANCY : boolean := true;

---------------------------------------
-- Constant: read FIFO depth
---------------------------------------
constant RDFIFO_DEPTH : integer := 512;

---------------------------------------
-- Constant: include read FIFO packet mode service
---------------------------------------
constant RDFIFO_INCLUDE_PACKET_MODE : boolean := false;

---------------------------------------
-- Constant: include read FIFO vacancy status
---------------------------------------
constant RDFIFO_INCLUDE_VACANCY : boolean := true;

---------------------------------------
-- Constant: PLB clock period in ps - reserved
---------------------------------------
constant PLB_CLK_PERIOD_PS : integer := 10000;

---------------------------------------
-- Constant: index for CS/CE
---------------------------------------
constant USER00_CS_INDEX : integer
```

```
                           := get_id_index(ARD_ID_ARRAY, USER_00);
  constant USER00_CE_INDEX : integer
        := calc_start_ce_index(ARD_NUM_CE_ARRAY, USER00_CS_INDEX);

  ---------------------------------------
  -- IP Interconnect (IPIC) signal declarations -- do not delete
  ---------------------------------------
  signal ZERO_PLB_MSSize : std_logic_vector(0 to 1)
                           := (others => '0');
  signal ZERO_PLB_MRdDBus : std_logic_vector(0 to (C_PLB_DWIDTH-1))
                            := (others => '0');
  signal ZERO_PLB_MRdWdAddr : std_logic_vector(0 to 3)
                              := (others => '0');
  signal iBus2IP_Clk   : std_logic;
  signal iBus2IP_Reset : std_logic;
  signal ZERO_IP2Bus_IntrEvent : std_logic_vector(0 to
                                 IP_INTR_MODE_ARRAY'length - 1)
                                 := (others => '0');
  signal iIP2Bus_Data  : std_logic_vector(0 to C_PLB_DWIDTH-1)
                         := (others => '0');
  signal iIP2Bus_WrAck : std_logic := '0';
  signal iIP2Bus_RdAck : std_logic := '0';
  signal iIP2Bus_Retry : std_logic := '0';
  signal iIP2Bus_Error : std_logic := '0';
  signal iIP2Bus_ToutSup : std_logic := '0';
  signal iBus2IP_Data  : std_logic_vector(0 to C_PLB_DWIDTH - 1);
  signal iBus2IP_BE    : std_logic_vector(0 to
                         (C_PLB_DWIDTH/8) - 1);
  signal iBus2IP_WrReq : std_logic;
  signal iBus2IP_RdReq : std_logic;
  signal iBus2IP_RdCE  : std_logic_vector(0 to
                         calc_num_ce(ARD_NUM_CE_ARRAY)-1);
  signal iBus2IP_WrCE  : std_logic_vector(0 to
                         calc_num_ce(ARD_NUM_CE_ARRAY)-1);
  signal ZERO_IP2Bus_Addr : std_logic_vector(0 to
                            C_PLB_AWIDTH - 1) := (others => '0');
  signal ZERO_IP2Bus_MstBE : std_logic_vector(0 to
                             (C_PLB_DWIDTH/8) - 1)
                             := (others => '0');
  signal ZERO_IP2IP_Addr : std_logic_vector(0 to
                           C_PLB_AWIDTH - 1) := (others => '0');
  signal ZERO_IP2RFIFO_Data : std_logic_vector(0 to
                              find_id_dwidth(ARD_ID_ARRAY,
                              ARD_DWIDTH_ARRAY, IPIF_RDFIFO_DATA,
                              C_PLB_DWIDTH)-1) := (others => '0');
  signal uBus2IP_Data : std_logic_vector(0 to USER_DWIDTH-1);
  signal uBus2IP_BE   : std_logic_vector(0 to USER_DWIDTH/8-1);
  signal uBus2IP_RdCE : std_logic_vector(0 to USER_NUM_CE-1);
  signal uBus2IP_WrCE : std_logic_vector(0 to USER_NUM_CE-1);
  signal uIP2Bus_Data : std_logic_vector(0 to USER_DWIDTH-1);

begin

  ---------------------------------------
  -- instantiate the PLB IPIF
  ---------------------------------------
  PLB_IPIF_I : entity plb_ipif_v1_00_e.plb_ipif
```

```
generic map
(
  C_ARD_ID_ARRAY => ARD_ID_ARRAY,
  C_ARD_ADDR_RANGE_ARRAY => ARD_ADDR_RANGE_ARRAY,
  C_ARD_DWIDTH_ARRAY => ARD_DWIDTH_ARRAY,
  C_ARD_NUM_CE_ARRAY => ARD_NUM_CE_ARRAY,
  C_DEV_BLK_ID => DEV_BLK_ID,
  C_DEV_MIR_ENABLE => DEV_MIR_ENABLE,
  C_DEV_BURST_ENABLE => DEV_BURST_ENABLE,
  C_DEV_FAST_DATA_XFER => DEV_FAST_DATA_XFER,
  C_DEV_MAX_BURST_SIZE => DEV_MAX_BURST_SIZE,
  C_DEV_BURST_PAGE_SIZE => DEV_BURST_PAGE_SIZE,
  C_DEV_DPHASE_TIMEOUT => DEV_DPHASE_TIMEOUT,
  C_INCLUDE_DEV_ISC => INCLUDE_DEV_ISC,
  C_INCLUDE_DEV_PENCODER => INCLUDE_DEV_PENCODER,
  C_IP_INTR_MODE_ARRAY => IP_INTR_MODE_ARRAY,
  C_IP_MASTER_PRESENT => IP_MASTER_PRESENT,
  C_WRFIFO_DEPTH => WRFIFO_DEPTH,
  C_WRFIFO_INCLUDE_PACKET_MODE => WRFIFO_INCLUDE_PACKET_MODE,
  C_WRFIFO_INCLUDE_VACANCY => WRFIFO_INCLUDE_VACANCY,
  C_RDFIFO_DEPTH => RDFIFO_DEPTH,
  C_RDFIFO_INCLUDE_PACKET_MODE => RDFIFO_INCLUDE_PACKET_MODE,
  C_RDFIFO_INCLUDE_VACANCY => RDFIFO_INCLUDE_VACANCY,
  C_PLB_MID_WIDTH => C_PLB_MID_WIDTH,
  C_PLB_NUM_MASTERS => C_PLB_NUM_MASTERS,
  C_PLB_AWIDTH => C_PLB_AWIDTH,
  C_PLB_DWIDTH => C_PLB_DWIDTH,
  C_PLB_CLK_PERIOD_PS => PLB_CLK_PERIOD_PS,
  C_IPIF_DWIDTH => C_PLB_DWIDTH,
  C_IPIF_AWIDTH => C_PLB_AWIDTH,
  C_FAMILY => C_FAMILY
  )
port map
(
  PLB_clk => PLB_Clk,
  Reset => PLB_Rst,
  Freeze => '0',
  IP2INTC_Irpt => open,
  PLB_ABus => PLB_ABus,
  PLB_PAValid => PLB_PAValid,
  PLB_SAValid => PLB_SAValid,
  PLB_rdPrim => PLB_rdPrim,
  PLB_wrPrim => PLB_wrPrim,
  PLB_masterID => PLB_masterID,
  PLB_abort => PLB_abort,
  PLB_busLock => PLB_busLock,
  PLB_RNW => PLB_RNW,
  PLB_BE => PLB_BE,
  PLB_MSize => PLB_MSize,
  PLB_size => PLB_size,
  PLB_type => PLB_type,
  PLB_compress => PLB_compress,
  PLB_guarded => PLB_guarded,
  PLB_ordered => PLB_ordered,
  PLB_lockErr => PLB_lockErr,
  PLB_wrDBus => PLB_wrDBus,
  PLB_wrBurst => PLB_wrBurst,
```

```
PLB_rdBurst => PLB_rdBurst,
PLB_pendReq => PLB_pendReq,
PLB_pendPri => PLB_pendPri,
PLB_reqPri => PLB_reqPri,
Sl_addrAck => Sl_addrAck,
Sl_SSize => Sl_SSize,
Sl_wait => Sl_wait,
Sl_rearbitrate => Sl_rearbitrate,
Sl_wrDAck => Sl_wrDAck,
Sl_wrComp => Sl_wrComp,
Sl_wrBTerm => Sl_wrBTerm,
Sl_rdDBus => Sl_rdDBus,
Sl_rdWdAddr => Sl_rdWdAddr,
Sl_rdDAck => Sl_rdDAck,
Sl_rdComp => Sl_rdComp,
Sl_rdBTerm => Sl_rdBTerm,
Sl_MBusy => Sl_MBusy,
Sl_MErr => Sl_MErr,
PLB_MAddrAck => '0',
PLB_MSSize => ZERO_PLB_MSSize,
PLB_MRearbitrate => '0',
PLB_MBusy => '0',
PLB_MErr => '0',
PLB_MWrDAck => '0',
PLB_MRdDBus => ZERO_PLB_MRdDBus,
PLB_MRdWdAddr => ZERO_PLB_MRdWdAddr,
PLB_MRdDAck => '0',
PLB_MRdBTerm => '0',
PLB_MWrBTerm => '0',
M_request => open,
M_priority => open,
M_busLock => open,
M_RNW => open,
M_BE => open,
M_MSize => open,
M_size => open,
M_type => open,
M_compress => open,
M_guarded => open,
M_ordered => open,
M_lockErr => open,
M_abort => open,
M_ABus => open,
M_wrDBus => open,
M_wrBurst => open,
M_rdBurst => open,
IP2Bus_Clk => '0',
Bus2IP_Clk => iBus2IP_Clk,
Bus2IP_Reset => iBus2IP_Reset,
Bus2IP_Freeze => open,
IP2Bus_IntrEvent => ZERO_IP2Bus_IntrEvent,
IP2Bus_Data => iIP2Bus_Data,
IP2Bus_WrAck => iIP2Bus_WrAck,
IP2Bus_RdAck => iIP2Bus_RdAck,
IP2Bus_Retry => iIP2Bus_Retry,
IP2Bus_Error => iIP2Bus_Error,
IP2Bus_ToutSup => iIP2Bus_ToutSup,
```

```
IP2Bus_PostedWrInh => '0',
IP2Bus_Busy => '0',
IP2Bus_AddrAck => '0',
IP2Bus_BTerm => '0',
Bus2IP_Addr => open,
Bus2IP_Data => iBus2IP_Data,
Bus2IP_RNW => open,
Bus2IP_BE => iBus2IP_BE,
Bus2IP_Burst => open,
Bus2IP_IBurst => open,
Bus2IP_WrReq => iBus2IP_WrReq,
Bus2IP_RdReq => iBus2IP_RdReq,
Bus2IP_RNW_Early => open,
Bus2IP_PselHit => open,
Bus2IP_CS => open,
Bus2IP_CE => open,
Bus2IP_RdCE => iBus2IP_RdCE,
Bus2IP_WrCE => iBus2IP_WrCE,
IP2DMA_RxLength_Empty => '0',
IP2DMA_RxStatus_Empty => '0',
IP2DMA_TxLength_Full => '0',
IP2DMA_TxStatus_Empty => '0',
IP2Bus_Addr => ZERO_IP2Bus_Addr,
IP2Bus_MstBE => ZERO_IP2Bus_MstBE,
IP2IP_Addr => ZERO_IP2IP_Addr,
IP2Bus_MstWrReq => '0',
IP2Bus_MstRdReq => '0',
IP2Bus_MstBurst => '0',
IP2Bus_MstBusLock => '0',
Bus2IP_MstWrAck => open,
Bus2IP_MstRdAck => open,
Bus2IP_MstRetry => open,
Bus2IP_MstError => open,
Bus2IP_MstTimeOut => open,
Bus2IP_MstLastAck => open,
IP2RFIFO_WrReq => '0',
IP2RFIFO_Data => ZERO_IP2RFIFO_Data,
IP2RFIFO_WrMark => '0',
IP2RFIFO_WrRelease => '0',
IP2RFIFO_WrRestore => '0',
RFIFO2IP_WrAck => open,
RFIFO2IP_AlmostFull => open,
RFIFO2IP_Full => open,
RFIFO2IP_Vacancy => open,
IP2WFIFO_RdReq => '0',
IP2WFIFO_RdMark => '0',
IP2WFIFO_RdRelease => '0',
IP2WFIFO_RdRestore => '0',
WFIFO2IP_Data => open,
WFIFO2IP_RdAck => open,
WFIFO2IP_AlmostEmpty => open,
WFIFO2IP_Empty => open,
WFIFO2IP_Occupancy => open,
IP2Bus_DMA_Req => '0',
Bus2IP_DMA_Ack => open
);
```

```
  ---------------------------------------
  -- instantiate the User Logic
  ---------------------------------------
  USER_LOGIC_I : entity Cap_reg.user_logic
    generic map
    (
      C_DWIDTH => USER_DWIDTH,
      C_NUM_CE => USER_NUM_CE
      )
    port map
    (
      Iin_A          => Iin_A,
      Iin_B          => Iin_B,
      Iin_C          => Iin_C,
      Iout_a         => Iout_a,
      Iout_b         => Iout_b,
      Iout_c         => Iout_c,
      Bus2IP_Clk     => iBus2IP_Clk,
      Bus2IP_Reset   => iBus2IP_Reset,
      Bus2IP_Data    => uBus2IP_Data,
      Bus2IP_BE      => uBus2IP_BE,
      Bus2IP_RdCE    => uBus2IP_RdCE,
      Bus2IP_WrCE    => uBus2IP_WrCE,
      Bus2IP_RdReq   => iBus2IP_RdReq,
      Bus2IP_WrReq   => iBus2IP_WrReq,
      IP2Bus_Data    => uIP2Bus_Data,
      IP2Bus_Retry   => iIP2Bus_Retry,
      IP2Bus_Error   => iIP2Bus_Error,
      IP2Bus_ToutSup => iIP2Bus_ToutSup,
      IP2Bus_RdAck   => iIP2Bus_RdAck,
      IP2Bus_WrAck   => iIP2Bus_WrAck
      );

  ---------------------------------------
  -- hooking up signal slicing
  ---------------------------------------
  uBus2IP_BE <= iBus2IP_BE(0 to USER_DWIDTH/8-1);
  uBus2IP_Data <= iBus2IP_Data(0 to USER_DWIDTH-1);
  uBus2IP_RdCE <= iBus2IP_RdCE(USER00_CE_INDEX to
                          USER00_CE_INDEX+USER_NUM_CE-1);
  uBus2IP_WrCE <= iBus2IP_WrCE(USER00_CE_INDEX to
                          USER00_CE_INDEX+USER_NUM_CE-1);
  iIP2Bus_Data(0 to USER_DWIDTH-1) <= uIP2Bus_Data;
end IMP;
```

- Codes for the MPD file

```
##############################################################################
## Name     : Cap_reg                                                       ##
## Desc     : Microprocessor Peripheral Description                         ##
##          : Automatically generated by PsfUtility                         ##
##############################################################################

BEGIN Cap_reg

## Peripheral Options
```

```
OPTION IPTYPE = PERIPHERAL
OPTION IMP_NETLIST = TRUE
OPTION HDL = VHDL

## Bus Interfaces
BUS_INTERFACE BUS = SPLB, BUS_STD = PLB, BUS_TYPE = SLAVE

## Generics for VHDL or Parameters for Verilog
PARAMETER C_BASEADDR = 0xffffffff, DT = std_logic_vector,
   MIN_SIZE = 0x100, BUS = SPLB, ADDRESS = BASE, PAIR = C_HIGHADDR
PARAMETER C_HIGHADDR = 0x00000000, DT = std_logic_vector,
   BUS = SPLB, ADDRESS = HIGH, PAIR = C_BASEADDR
PARAMETER C_PLB_AWIDTH = 32, DT = INTEGER, BUS = SPLB
PARAMETER C_PLB_DWIDTH = 64, DT = INTEGER, BUS = SPLB
PARAMETER C_PLB_NUM_MASTERS = 8, DT = INTEGER, BUS = SPLB
PARAMETER C_PLB_MID_WIDTH = 3, DT = INTEGER, BUS = SPLB
PARAMETER C_USER_ID_CODE = 3, DT = INTEGER
PARAMETER C_FAMILY = virtex2p, DT = STRING

## Ports
PORT PLB_Clk = "", DIR = I, SIGIS = Clk, BUS = SPLB
PORT PLB_Rst = PLB_Rst, DIR = I, SIGIS = Rst, BUS = SPLB
PORT Sl_addrAck = Sl_addrAck, DIR = O, BUS = SPLB
PORT Sl_MBusy = Sl_MBusy, DIR = O, VEC = [0:(C_PLB_NUM_MASTERS-1)],
                BUS = SPLB
PORT Sl_MErr = Sl_MErr, DIR = O, VEC = [0:(C_PLB_NUM_MASTERS-1)],
               BUS = SPLB
PORT Sl_rdBTerm = Sl_rdBTerm, DIR = O, BUS = SPLB
PORT Sl_rdComp = Sl_rdComp, DIR = O, BUS = SPLB
PORT Sl_rdDAck = Sl_rdDAck, DIR = O, BUS = SPLB
PORT Sl_rdDBus = Sl_rdDBus, DIR = O, VEC = [0:(C_PLB_DWIDTH-1)],
                 BUS = SPLB
PORT Sl_rdWdAddr = Sl_rdWdAddr, DIR = O, VEC = [0:3], BUS = SPLB
PORT Sl_rearbitrate = Sl_rearbitrate, DIR = O, BUS = SPLB
PORT Sl_SSize = Sl_SSize, DIR = O, VEC = [0:1], BUS = SPLB
PORT Sl_wait = Sl_wait, DIR = O, BUS = SPLB
PORT Sl_wrBTerm = Sl_wrBTerm, DIR = O, BUS = SPLB
PORT Sl_wrComp = Sl_wrComp, DIR = O, BUS = SPLB
PORT Sl_wrDAck = Sl_wrDAck, DIR = O, BUS = SPLB
PORT PLB_abort = PLB_abort, DIR = I, BUS = SPLB
PORT PLB_ABus = PLB_ABus, DIR = I, VEC = [0:(C_PLB_AWIDTH-1)],
                BUS = SPLB
PORT PLB_BE = PLB_BE, DIR = I, VEC = [0:((C_PLB_DWIDTH/8)-1)],
              BUS = SPLB
PORT PLB_busLock = PLB_busLock, DIR = I, BUS = SPLB
PORT PLB_compress = PLB_compress, DIR = I, BUS = SPLB
PORT PLB_guarded = PLB_guarded, DIR = I, BUS = SPLB
PORT PLB_lockErr = PLB_lockErr, DIR = I, BUS = SPLB
PORT PLB_masterID = PLB_masterID, DIR = I, VEC =
                    [0:(C_PLB_MID_WIDTH-1)], BUS = SPLB
PORT PLB_MSize = PLB_MSize, DIR = I, VEC = [0:1], BUS = SPLB
PORT PLB_ordered = PLB_ordered, DIR = I, BUS = SPLB
PORT PLB_PAValid = PLB_PAValid, DIR = I, BUS = SPLB
PORT PLB_pendPri = PLB_pendPri, DIR = I, VEC = [0:1], BUS = SPLB
PORT PLB_pendReq = PLB_pendReq, DIR = I, BUS = SPLB
PORT PLB_rdBurst = PLB_rdBurst, DIR = I, BUS = SPLB
PORT PLB_rdPrim = PLB_rdPrim, DIR = I, BUS = SPLB
```

```
PORT PLB_reqPri = PLB_reqPri, DIR = I, VEC = [0:1], BUS = SPLB
PORT PLB_RNW = PLB_RNW, DIR = I, BUS = SPLB
PORT PLB_SAValid = PLB_SAValid, DIR = I, BUS = SPLB
PORT PLB_size = PLB_size, DIR = I, VEC = [0:3], BUS = SPLB
PORT PLB_type = PLB_type, DIR = I, VEC = [0:2], BUS = SPLB
PORT PLB_wrBurst = PLB_wrBurst, DIR = I, BUS = SPLB
PORT PLB_wrDBus = PLB_wrDBus, DIR = I, VEC = [0:(C_PLB_DWIDTH-1)],
                  BUS = SPLB
PORT PLB_wrPrim = PLB_wrPrim, DIR = I, BUS = SPLB

## ADC_ctrl1 signals
PORT Iin_A = "", DIR = I, VEC = [0:15]
PORT Iin_B = "", DIR = I, VEC = [0:15]
PORT Iin_C = "", DIR = I, VEC = [0:15]
PORT Iout_a = "", DIR = I, VEC = [0:15]
PORT Iout_b = "", DIR = I, VEC = [0:15]
PORT Iout_c = "", DIR = I, VEC = [0:15]
END
```

C.7. POWERPC ASSEMBLY CODES

The PowerPC microprocessor was programmed using the Assembly language. The PowerPC performs the following tasks:

- converts all variables from the three-phase system into variables in *dq* coordinate.
- performs the space vector modulation
- determines the capacitor to be employed in each switching period
- performs capacitor voltage balancing scheme
- generates data set for each subinterval in a switching period
- sends all information to the PWM controller circuit

- Assembly codes for the PowerPC microprocessor

```
/*-------------------------------------------------------------*/
/*-- FILE: mml_withVcap_reg.s                                --*/
/*-- By Sitthipong Angkititrakul                             --*/
/*-- Assembly code for PowerPC                               --*/
/*--   - Calculate SVM and choose Capacitor for each        --*/
/*--          switching period                               --*/
/*--   - Capacitor voltage regulation                         --*/
/*-------------------------------------------------------------*/

      .text
      .global calculate
      .equ d_tic_in,1623
      .equ d_tic_out,2050
      .equ period_tic,1000

/*-- period_tic is used to calculate duty cycle of          --*/
/*--         space vector                                    --*/
/*--                                                         --*/
/*--             d = (1/Vcap)*Vref*sin()                     --*/
/*-- in term of number of ticks                              --*/
/*--                                                         --*/
```

```
/*-- d = (Vref--in adc*5/4096*1000/6.06)*sin()*switch period--*/
/*--     ------------------------------       ------------ --*/
/*--        (Vcap--in adc*5/4096*100)           clk period  --*/
/*--                                                        --*/
/*-- switch period = 50 us, clk period = 0.05 us            --*/
/*-- period_tic = 1000                                      --*/
/*--  d =  Vref--in adc *   10   * period_tic * sin()       --*/
/*--       ------------   ------                            --*/
/*--       Vcap--in adc     6.06                            --*/
/*--  gain of the sensor circuit @60Hz = 6.06               --*/
/*--  d = Vref--in adc * sin() * d_tic                      --*/
/*--      -------------                                     --*/
/*--      Vcap--in adc                                      --*/
/*--                                                        --*/
/*-- d_tic = 1650                                           --*/

/*--  ADCs' channel 1 address starts at 0xF0000500--*/
/*--  0xF0000500 for VAB                           --*/
/*--  0xF0000502 for VBC                           --*/
/*--  0xF0000504 for Vab                           --*/
/*--  0xF0000506 for Vbc                           --*/
/*--  0xF0000508 for IA                            --*/
/*--  0xF000050A for IB                            --*/
/*--  0xF000050C for IC                            --*/
/*--  0xF000050E for Ia                            --*/
/*--  0xF0000510 for Ib                            --*/
/*--  0xF0000512 for Ic                            --*/

calculate:
            lis 31,0xF000
            ori 31,31,0x0500
Read_VAB:
            lha 1,0(31) /* read VAB */
            lha 30,0(31)
            isync
            cmp 0,0,1,30
            bne Read_VAB
            li 30,Vin_AB_x1@l
            lha 2,0(30)
            lha 3,2(30)
            lha 4,4(30)
            lha 5,6(30)
            lha 6,8(30)
            lha 7,10(30)
            lha 8,12(30)
            lha 9,14(30)
            isync
            mulli 11,1,7
            mulli 12,2,28
            mulli 13,3,42
            mulli 14,4,28
            mulli 15,5,7
            mulli 16,6,4768
            mulli 17,7,-4409
            mulli 18,8,1896
            mulli 19,9,-317
            add 11,11,12
```

```
            add 11,11,13
            add 11,11,14
            add 11,11,15
            add 11,11,16
            add 11,11,17
            add 11,11,18
            add 11,11,19
            srawi 11,11,11
            sth 1,0(30)
            sth 2,2(30)
            sth 3,4(30)
            sth 4,6(30)
            sth 11,8(30)
            sth 6,10(30)
            sth 7,12(30)
            sth 8,14(30)
            isync
Read_VinBC:
            lha 1,2(31) /* read VBC */
            lha 30,2(31)
            isync
            cmp 0,0,1,30
            bne Read_VinBC
            li 30,Vin_BC_x1@l
            lha 2,0(30)
            lha 3,2(30)
            lha 4,4(30)
            lha 5,6(30)
            lha 6,8(30)
            lha 7,10(30)
            lha 8,12(30)
            lha 9,14(30)
            isync
            mulli 21,1,7
            mulli 22,2,28
            mulli 23,3,42
            mulli 24,4,28
            mulli 25,5,7
            mulli 26,6,4768
            mulli 27,7,-4409
            mulli 28,8,1896
            mulli 29,9,-317
            add 12,21,22
            add 12,12,23
            add 12,12,24
            add 12,12,25
            add 12,12,26
            add 12,12,27
            add 12,12,28
            add 12,12,29
            srawi 12,12,11
            sth 1,0(30)
            sth 2,2(30)
            sth 3,4(30)
            sth 4,6(30)
            sth 12,8(30)
            sth 6,10(30)
```

```
            sth 7,12(30)
            sth 8,14(30)
            isync

/*--  Converter into dq-data  --*/
            mr 21,11  /*-- R21 = Vd_in --*/
            add 22,12,12
            add 22,22,11
            mulli 22,22,591
            srawi 22,22,10 /*-- R22 = Vq_in --*/
            bl rec2pol
            li 30,Vin_ph@l
            sth 24,0(30)
            bl pol2dq
            sth 25,2(30)
            sth 26,4(30)
            sth 27,6(30)

/*-------------------------------------------------------------*/
/*--  Generate output reference space vector                 --*/
/*-------------------------------------------------------------*/
/*-- NOTE: Time base is a 64-bit unsigned register          --*/
/*--           TBU is upper 32 bits of time base           --*/
/*--           TBL is lower 32 bits of time base           --*/
/*--  - Calculate angle of the space vector                --*/
/*--     for 300MHz clock => period = 3.33 ns              --*/
/*--                                                       --*/
/*--     angle = 2*180*f*n*3.33*10^(-9) degree             --*/
/*--         f = output line frequency                     --*/
/*--         n = data from time base                       --*/
/*--     angle = 1.2*10^(-6)*f*n                           --*/
/*--     for f = 30 Hz                                     --*/
/*--     angle = n*36*10^(-6)                              --*/
/*--           = n*19/2^(19)                               --*/
/*--     for f = 40 Hz: angle = n*201/2^(22)               --*/
/*--     for f = 50 Hz: angle = n*63/2^(20)                --*/

tb_loop:
            mftbu 1
            mftb 2
            mftbu 3
            cmp 0,0,3,1
            bne tb_loop
            /*-- R1 = upper 32 bits of time base --*/
            /*-- R2 = lower 32 bits of time base --*/
            li 11,19  /*-- change for line frequency --*/
            mullw 12,2,11  /*-- R12 = R2*R11[32:63] --*/
            mulhwu 13,2,11  /*-- R13 = R2*R11[0:31] --*/
            mullw 14,1,11  /*-- R14 = R1*R11[32:63] --*/
            add 13,13,14
            srwi 12,12,19  /*-- change for line frequency --*/
            rlwimi 12,13,13,0,18

/*---  Extract angle: 0 <= output_phase <= 360  --*/
            li 13,360
            divwu 14,12,13
            mullw 15,14,13
```

```
            subf 24,15,12
            li 30,Vout_ph@l
            sth 24,0(30)
            bl pol2dq
            sth 25,2(30)
            sth 26,4(30)
            sth 27,6(30)

/*-------------------------------------------------------------*/
/*--  Read all Capacitor voltages                            --*/
/*-------------------------------------------------------------*/
/*--     0xF0000600 for VCAa                                 --*/
/*--     0xF0000602 for VCAb                                 --*/
/*--     0xF0000604 for VCAc                                 --*/
/*--     0xF0000606 for VCBa                                 --*/
/*--     0xF0000608 for VCBb                                 --*/
/*--     0xF000060A for VCBc                                 --*/
/*--     0xF000060C for VCCa                                 --*/
/*--     0xF000060E for VCCb                                 --*/
/*--     0xF0000610 for VCCc                                 --*/

            lis 31,0xF800
            ori 31,31,0x0300
Read_VC_Aa:
            lhz 1,0(31)
            lhz 11,0(31)
            isync
            cmp 0,0,1,11
            bne Read_VC_Aa
Read_VC_Ab:
            lhz 2,2(31)
            lhz 11,2(31)
            isync
            cmp 0,0,2,11
            bne Read_VC_Ab
Read_VC_Ac:
            lhz 3,4(31)
            lhz 11,4(31)
            isync
            cmp 0,0,3,11
            bne Read_VC_Ac
Read_VC_Ba:
            lhz 4,6(31)
            lhz 11,6(31)
            isync
            cmp 0,0,4,11
            bne Read_VC_Ba
Read_VC_Bb:
            lhz 5,8(31)
            lhz 11,8(31)
            isync
            cmp 0,0,5,11
            bne Read_VC_Bb
Read_VC_Bc:
            lhz 6,10(31)
            lhz 11,10(31)
            isync
```

```
            cmp 0,0,6,11
            bne Read_VC_Bc
Read_VC_Ca:
            lhz 7,12(31)
            lhz 11,12(31)
            isync
            cmp 0,0,7,11
            bne Read_VC_Ca
Read_VC_Cb:
            lhz 8,14(31)
            lhz 11,14(31)
            isync
            cmp 0,0,8,11
            bne Read_VC_Cb
Read_VC_Cc:
            lhz 9,16(31)
            lhz 11,16(31)
            isync
            cmp 0,0,9,11
            bne Read_VC_Cc

/*--  Determine most positive capacitor voltage variation    --*/
/*--     R11 = most pos. V^cap                               --*/
/*--     R12 = Cap 9-bit                                     --*/

            mr 11,1
            li 12,1  /* use Cap_Aa */
            cmpl 0,0,11,2
            bge most_pos_vcap1
            mr 11,2  /* use Cap_Ab */
            li 12,2
most_pos_vcap1:
            cmpl 0,0,11,3
            bge most_pos_vcap2
            mr 11,3  /* use Cap_Ac */
            li 12,4
most_pos_vcap2:
            cmpl 0,0,11,4
            bge most_pos_vcap3
            mr 11,4  /* use Cap_Ba */
            li 12,8
most_pos_vcap3:
            cmpl 0,0,11,5
            bge most_pos_vcap4
            mr 11,5  /* use Cap_Bb */
            li 12,16
most_pos_vcap4:
            cmpl 0,0,11,6
            bge most_pos_vcap5
            mr 11,6  /* use Cap_Bc */
            li 12,32
most_pos_vcap5:
            cmpl 0,0,11,7
            bge most_pos_vcap6
            mr 11,7  /* use Cap_Ca */
            li 12,64
most_pos_vcap6:
```

```
            cmpl 0,0,11,8
            bge most_pos_vcap7
            mr 11,8  /* use Cap_Cb */
            li 12,128
most_pos_vcap7:
            cmpl 0,0,11,9
            bge most_pos_vcap8
            mr 11,9  /* use Cap_Cc */
            li 12,256
most_pos_vcap8:

/*--  Determine most negative capacitor voltage variation    --*/
/*--      R13 = most neg. V^cap                               --*/
/*--      R14 = cap 9-bit                                     --*/

            mr 13,1  /* use Cap_Aa */
            li 14,1
            cmpl 0,0,13,2
            ble most_neg_vcap1
            mr 13,2  /* use Cap_Ab */
            li 14,2
most_neg_vcap1:
            cmpl 0,0,13,3
            ble most_neg_vcap2
            mr 13,3  /* use Cap_Ac */
            li 14,4
most_neg_vcap2:
            cmpl 0,0,13,4
            ble most_neg_vcap3
            mr 13,4  /* use Cap_Ba */
            li 14,8
most_neg_vcap3:
            cmpl 0,0,13,5
            ble most_neg_vcap4
            mr 13,5  /* use Cap_Bb */
            li 14,16
most_neg_vcap4:
            cmpl 0,0,13,6
            ble most_neg_vcap5
            mr 13,6  /* use Cap_Bc */
            li 14,32
most_neg_vcap5:
            cmpl 0,0,13,7
            ble most_neg_vcap6
            mr 13,7  /* use Cap_Ca */
            li 14,64
most_neg_vcap6:
            cmpl 0,0,13,8
            ble most_neg_vcap7
            mr 13,8  /* use Cap_Cb */
            li 14,128
most_neg_vcap7:
            cmpl 0,0,13,9
            ble deter_SVs
            mr 13,9  /* use Cap_Cc */
            li 14,256
```

```
/*--  Determine opposite SVs  --*/
deter_SVs:
            or 15,12,14
            lis 31,0xF800
            ori 31,31,0x0100
            sth 15,0(31)

/*--  Calculate average of capacitor voltages  --*/
            add 10,1,2
            add 10,10,3
            add 10,10,4
            add 10,10,5
            add 10,10,6
            add 10,10,7
            add 10,10,8
            add 10,10,9
            mulli 10,10,455
            srwi 10,10,12  /* R10 = average Vcap */

/*--  Calculate deviations of capacitor voltages  --*/
            subf 11,10,11
            subf 13,13,10
            cmpl 0,0,11,13
            blt ccc1
            mr 15,11
            b ccc2
ccc1:
            mr 15,13
ccc2:

/*--  Load possible combinations of opposite SVs  --*/
            lha 16,4(31)
            lha 18,8(31)
            lha 20,12(31)
            lha 22,16(31)
            lha 24,20(31)
            isync
            cmpi 0,0,16,0
            blt aaa1
            lhz 17,2(31)
            b aaa2
aaa1:
            neg 16,16
            li 26,2
            lhbrx 17,31,26
aaa2:
            cmpi 0,0,18,0
            blt aaa3
            lhz 19,6(31)
            b aaa4
aaa3:
            neg 18,18
            li 26,6
            lhbrx 19,31,26
aaa4:
            cmpi 0,0,20,0
            blt aaa5
```

```
            lhz 21,10(31)
            b aaa6
aaa5:
            neg 20,20
            li 26,10
            lhbrx 21,31,26
aaa6:
            cmpi 0,0,22,0
            blt aaa7
            lhz 23,14(31)
            b aaa8
aaa7:
            neg 22,22
            li 26,14
            lhbrx 23,31,26
aaa8:
            cmpi 0,0,24,0
            blt aaa9
            lhz 25,18(31)
            b aaa10
aaa9:
            neg 24,24
            li 26,18
            lhbrx 25,31,26
aaa10:

/*--  Determine Maximum current combination  --*/
            cmpl 0,0,16,18
            bge bbb1
            mr 16,18
            mr 17,19
bbb1:
            cmpl 0,0,16,20
            bge bbb2
            mr 16,20
            mr 17,21
bbb2:
            cmpl 0,0,16,22
            bge bbb3
            mr 16,22
            mr 17,23
bbb3:
            cmpl 0,0,16,24
            bge bbb4
            mr 16,24
            mr 17,25
bbb4:

/*--  Calculate duty cycles  --*/

duty_cycle:
            /*--- input side ---*/
            li 20,538
            /*input modulation index = 0.85*/
            mulli 20,20,d_tic_in
            li 21,Vin_theta@l
            lhz 21,0(21)
```

```
            add 30,21,21
            li 22,Sin@l
            lhzx 23,22,30
            mullw 1,20,23
            srwi 1,1,18  /*-- dk --*/

            subfic 21,21,60
            add 30,21,21
            lhzx 23,22,30
            mullw 2,20,23
            srwi 2,2,18  /*-- dl--*/
            subfic 3,1,period_tic
            subf 3,2,3  /*-- d0_in --*/

            /*--- output side ---*/
            li 20,350
            /*output modulation index = 0.7*/
            mulli 20,20,d_tic_out
            li 21,Vout_theta@l
            lhz 21,0(21)
            add 30,21,21
            li 22,Sin@l
            lhzx 23,22,30
            mullw 4,20,23
            srwi 4,4,18  /*-- dm --*/

            subfic 21,21,60
            add 30,21,21
            lhzx 23,22,30
            mullw 5,20,23
            srwi 5,5,18  /*-- dn --*/
            subfic 6,4,period_tic
            subf 6,5,6  /*-- d0-out --*/

/*--  Calculate duty cycle of the additional subinterval  --*/
            cmpi 0,0,16,10
            blt xxx
            cmpi 0,0,15,20
            blt xxx
            mulli 15,15,540
            divwu 15,15,16
            b limit1
xxx:
            li 15,0

/*--  Limitation on duty cycle  --*/
limit1:
            cmp 0,0,3,6
            blt d_0in_lt_d_0out
d_0in_gt_d_0out:
            srwi 0,6,2
            subf 30,0,6
            srwi 30,30,1
            b compare1
d_0in_lt_d_0out:
            srwi 0,3,2
            subf 30,0,3
```

```
            srwi 30,30,1
            /* d' is less than 3/8 of d of null SV */
compare1:
            cmpl 0,0,15,30
            ble update1
            mr 15,30
update1:
            add 30,15,15
            subf 3,30,3
            subf 6,30,6  /* Update d0_in,d0_out */

/*--  Determine the single capacitor  --*/
            /*--- Compare d0_in and d0_out ---*/
            li 7,Vin_ph@l
            lhz 7,0(7)
            li 8,Vout_ph@l
            lhz 8,0(8)
            cmp 0,0,3,6
            blt case2
case1:
            cmpli 0,0,8,60
            blt case1_1
            cmpli 0,0,8,120
            blt case1_2
            cmpli 0,0,8,180
            blt case1_3
            cmpli 0,0,8,240
            blt case1_4
            cmpli 0,0,8,300
            blt case1_5
case1_6:
            cmpli 0,0,7,90
            blt case160
            cmpli 0,0,7,210
            blt case161
            cmpli 0,0,7,330
            blt case162
case160:
            li 9,2
            b gen_SCCS_pattern
case161:
            li 9,16
            b gen_SCCS_pattern
case162:
            li 9,128
            b gen_SCCS_pattern
case1_5:
            cmpli 0,0,7,30
            blt case152
            cmpli 0,0,7,150
            blt case150
            cmpli 0,0,7,270
            blt case151
case152:
            li 9,32
            b gen_SCCS_pattern
case151:
```

```
            li 9,4
            b gen_SCCS_pattern
case150:
            li 9,256
            b gen_SCCS_pattern
case1_4:
            cmpli 0,0,7,90
            blt case140
            cmpli 0,0,7,210
            blt case141
            cmpli 0,0,7,330
            blt case142
case140:
            li 9,1
            b gen_SCCS_pattern
case141:
            li 9,8
            b gen_SCCS_pattern
case142:
            li 9,64
            b gen_SCCS_pattern
case1_3:
            cmpli 0,0,7,30
            blt case132
            cmpli 0,0,7,150
            blt case130
            cmpli 0,0,7,270
            blt case131
case132:
            li 9,16
            b gen_SCCS_pattern
case131:
            li 9,2
            b gen_SCCS_pattern
case130:
            li 9,128
            b gen_SCCS_pattern
case1_2:
            cmpli 0,0,7,90
            blt case120
            cmpli 0,0,7,210
            blt case121
            cmpli 0,0,7,330
            blt case122
case120:
            li 9,4
            b gen_SCCS_pattern
case121:
            li 9,32
            b gen_SCCS_pattern
case122:
            li 9,256
            b gen_SCCS_pattern
case1_1:
            cmpli 0,0,7,30
            blt case112
            cmpli 0,0,7,150
```

```
            blt case110
            cmpli 0,0,7,270
            blt case111
case112:
            li 9,8
            b gen_SCCS_pattern
case111:
            li 9,1
            b gen_SCCS_pattern
case110:
            li 9,64
            b gen_SCCS_pattern

case2:
            cmpli 0,0,7,60
            blt case2_1
            cmpli 0,0,7,120
            blt case2_2
            cmpli 0,0,7,180
            blt case2_3
            cmpli 0,0,7,240
            blt case2_4
            cmpli 0,0,7,300
            blt case2_5
case2_6:
            cmpli 0,0,8,90
            blt case260
            cmpli 0,0,8,210
            blt case261
            cmpli 0,0,8,330
            blt case262
case260:
            li 9,8
            b gen_SCCS_pattern
case261:
            li 9,16
            b gen_SCCS_pattern
case262:
            li 9,32
            b gen_SCCS_pattern
case2_5:
            cmpli 0,0,8,30
            blt case252
            cmpli 0,0,8,150
            blt case250
            cmpli 0,0,8,270
            blt case251
case252:
            li 9,128
            b gen_SCCS_pattern
case251:
            li 9,64
            b gen_SCCS_pattern
case250:
            li 9,256
            b gen_SCCS_pattern
case2_4:
```

```
            cmpli 0,0,8,90
            blt case240
            cmpli 0,0,8,210
            blt case241
            cmpli 0,0,8,330
            blt case242
case240:
            li 9,1
            b gen_SCCS_pattern
case241:
            li 9,2
            b gen_SCCS_pattern
case242:
            li 9,4
            b gen_SCCS_pattern
case2_3:
            cmpli 0,0,8,30
            blt case232
            cmpli 0,0,8,150
            blt case230
            cmpli 0,0,8,270
            blt case231
case232:
            li 9,16
            b gen_SCCS_pattern
case231:
            li 9,8
            b gen_SCCS_pattern
case230:
            li 9,32
            b gen_SCCS_pattern
case2_2:
            cmpli 0,0,8,90
            blt case220
            cmpli 0,0,8,210
            blt case221
            cmpli 0,0,8,330
            blt case222
case220:
            li 9,64
            b gen_SCCS_pattern
case221:
            li 9,128
            b gen_SCCS_pattern
case222:
            li 9,256
            b gen_SCCS_pattern
case2_1:
            cmpli 0,0,8,30
            blt case212
            cmpli 0,0,8,150
            blt case210
            cmpli 0,0,8,270
            blt case211
case212:
            li 9,2
            b gen_SCCS_pattern
```

```
case211:
            li 9,1
            b gen_SCCS_pattern
case210:
            li 9,4

/*-----------------------------------------------*/

gen_SCCS_pattern:
/*R28 = data for the seventh subinterval
        for discharging capacitor*/
            li 28,0
            rlwimi 28,17,12,4,7
            rlwimi 28,17,11,9,12
            rlwimi 28,14,10,13,21
            rlwimi 28,15,0,22,31
/*R23 = data for sixth subinterval for
        charging capacitor */
            li 23,0
            rlwimi 23,17,20,4,7
            rlwimi 23,17,19,9,12
            rlwimi 23,12,10,13,21
            rlwimi 23,15,0,22,31

/*--  Generate data for five subintervals  -----*/
            li 31,Vin_Valpha@l
            lhz 10,0(31)
            lhz 11,2(31)
            lhz 12,10(31)
            lhz 13,12(31)
            cmpl 0,0,1,2
            blt dk_lt_dl
bl_lt_dk:
            mr 14,2   /*-- R14 = min d_in --*/
            mr 15,1   /*-- R15 = max d_in --*/
            mr 16,11  /*-- R16 = Vector with min d_in --*/
            mr 17,10  /*-- R17 = Vector with max d_in --*/
            b next1
dk_lt_dl:
            mr 14,1
            mr 15,2
            mr 16,10
            mr 17,11
next1:
            cmpl 0,0,4,5
            blt dm_lt_dn
dn_lt_dm:
            mr 18,5   /*-- R18 = min d_out --*/
            mr 19,4   /*-- R19 = max d_out --*/
            mr 20,13  /*-- R20 = Vector with min d_out --*/
            mr 21,12  /*-- R21 = Vector with max d_out --*/
            b next2
dm_lt_dn:
            mr 18,4
            mr 19,5
            mr 20,12
            mr 21,13
```

```
next2:
            add 12,1,2  /*-- R12 = dk + dl --*/
            add 13,4,5  /*-- R13 = dm + dn --*/
            /*5th subinterval c5=min_v,min_v*/
            /* R27 = data for fifth subinterval*/
            slwi 27,16,24
            rlwimi 27,20,19,8,12
            rlwimi 27,9,10,13,21
            cmpl 0,0,14,18
            blt min.in_lt_min.out
            rlwimi 27,18,0,22,31

            /*-- R26 = data for forth subinterval --*/
            slwi 26,16,24  /* C4 = min,max*/
            rlwimi 26,21,19,8,12
            rlwimi 26,9,10,13,21
            subf 0,18,14  /* T4 = d.min_in-d.min_out*/
            rlwimi 26,0,0,22,31

            cmpl 0,0,12,13
            blt din_lt_dout1
din_gt_dout1:
            slwi 25,17,24  /*C3 = max,max*/
            rlwimi 25,21,19,8,12
            rlwimi 25,9,10,13,21
            subf 0,14,13
            rlwimi 25,0,0,22,31

            slwi 24,17,24  /*C2 = max,0*/
            rlwimi 24,9,10,13,21
            subf 0,13,12  /* T2 = dk+dl-dm-dn*/
            rlwimi 24,0,0,22,31

            li 22,0
            rlwimi 22,9,10,13,21
            rlwimi 22,3,0,22,31  /* T1 = d.0_in*/
            b done

din_lt_dout1:
            slwi 25,17,24  /*C3 = max,max*/
            rlwimi 25,21,19,8,12
            rlwimi 25,9,10,13,21
            rlwimi 25,15,0,22,31

            li 24,0
            rlwimi 24,21,19,8,12
            rlwimi 24,9,10,13,21
            subf 0,12,13
            rlwimi 24,0,0,22,31

            li 22,0
            rlwimi 22,9,10,13,21
            rlwimi 22,6,0,22,31
            b done

min.in_lt_min.out:
```

```
            rlwimi 27,14,0,22,31

            slwi 26,17,24  /* C4 = max,min*/
            rlwimi 26,20,19,8,12
            rlwimi 26,9,10,13,21
            subf 0,14,18  /* T4 = d.min_out-d.min_in*/
            rlwimi 26,0,0,22,31

            cmpl 0,0,13,12
            blt dout_lt_din2

dout_gt_din2:
            slwi 25,17,24  /*C3 = max,max*/
            rlwimi 25,21,19,8,12
            rlwimi 25,9,10,13,21
            subf 0,18,12  /*T3 = dk+dl-min.out*/
            rlwimi 25,0,0,22,31

            li 24,0
            rlwimi 24,21,19,8,12  /*C2 = 0,max*/
            rlwimi 24,9,10,13,21
            subf 0,12,13  /* T2 = dm+dn-dk-dl*/
            rlwimi 24,0,0,22,31

            li 22,0
            rlwimi 22,9,10,13,21
            rlwimi 22,6,0,22,31  /* T1 = d.0_out */
            b done

dout_lt_din2:
            slwi 25,17,24  /*C3 = max,max*/
            rlwimi 25,21,19,8,12
            rlwimi 25,9,10,13,21
            rlwimi 25,19,0,22,31  /* T3 = dmax.out*/

            slwi 24,17,24  /*C2 = max,0*/
            rlwimi 24,9,10,13,21
            subf 0,13,12  /* T2 = dk+dl-dm-dn*/
            rlwimi 24,0,0,22,31

            li 22,0
            rlwimi 22,9,10,13,21
            rlwimi 22,3,0,22,31  /* T1 = d.0_in */

done:
            li 29,0
            li 30,0
            lis 21,0xF000
            ori 21,21,0x0700
            li 31,0
            stw 31,36(21)
            isync
            stmw 22,0(21)
            isync
            li 31,1
            stw 31,36(21)
            eieio
```

```
            b calculate

/*--  Function to convert rectangular coordinate  --*/
/*--      to polar coordinate                     --*/
/*--  Effected register:                          --*/
/*--     R21,R22 : input data (x,y)               --*/
/*--     R23,R24 : output data (mag,ph)           --*/
/*--     R25,R26,R27 : temp data                  --*/

rec2pol:
            li 25,Atan@l
            cmpi 0,0,22,0
            blt sec5678
            cmpi 0,0,21,0
            blt sec34
            cmpl 0,0,21,22
            blt sec2
sec1:
            cmpi 0,0,21,0  /* d(r21) >= 0 */
            beq sec1_vd_0  /* d(r21) >= d(r22) >= 0 */
            mulli 24,22,100
            divwu 24,24,21
            lbzx 24,25,24
            b got_phase
sec1_vd_0:
            li 24,0
            b got_phase
sec2:
            mulli 24,21,100
            divwu 24,24,22
            lbzx 24,25,24
            subfic 24,24,90
            b got_phase
sec34:
            neg 26,21  /*-- d(r26) > 0 --*/
            cmpl 0,0,22,26
            blt sec4
sec3:
            mulli 24,26,100  /*-- d(r22) >= d(r26) > 0 --*/
            divwu 24,24,22
            lbzx 24,25,24
            addi 24,24,90
            b got_phase
sec4:
            mulli 24,22,100
            divwu 24,24,26
            lbzx 24,25,24
            subfic 24,24,180
            b got_phase
sec5678:
            neg 27,22  /*-- d(r27)=-d(r22)=-Vq >0 --*/
            cmpi 0,0,21,0
            blt sec56
            cmpl 0,0,21,27
            blt sec7
sec8:
            mulli 24,27,100  /*-- d(r21) >= d(r26) >0 --*/
```

```
            divwu 24,24,21
            lbzx 24,25,24
            subfic 24,24,360
            b got_phase
sec7:
            mulli 24,21,100
            divwu 24,24,27
            lbzx 24,25,24
            addi 24,24,270
            b got_phase
sec56:
            neg 26,21  /*-- d(r26)=-d(r21)=-vd >0 --*/
            cmpl 0,0,27,26
            blt sec5
sec6:
            mulli 24,26,100
            divwu 24,24,27
            lbzx 24,25,24
            subfic 24,24,270
            b got_phase
sec5:
            mulli 24,27,100
            divwu 24,24,26
            lbzx 24,25,24
            addi 24,24,180
got_phase:
            blr

/*--  Function to polar data to dq data                        --*/
/*--    Effected register:                                     --*/
/*--      R24 : input data (phase: 0 to 360)                   --*/
/*--      R25,R26,R27 : output data : V_alpha,V_gamma,theta    --*/

pol2dq:
            cmpli 0,0,24,30
            blt sector1
            cmpli 0,0,24,90
            blt sector2
            cmpli 0,0,24,150
            blt sector3
            cmpli 0,0,24,210
            blt sector4
            cmpli 0,0,24,270
            blt sector5
            cmpli 0,0,24,330
            blt sector6
            /*-- else sector = 1 --*/
            li 25,1
            li 26,6
            subi 27,24,330
            b got_theta
sector6:
            li 25,6
            li 26,5
            subi 27,24,270
            b got_theta
sector5:
```

```
            li 25,5
            li 26,4
            subi 27,24,210
            b got_theta
sector4:
            li 25,4
            li 26,3
            subi 27,24,150
            b got_theta
sector3:
            li 25,3
            li 26,2
            subi 27,24,90
            b got_theta
sector2:
            li 25,2
            li 26,1
            subi 27,24,30
            b got_theta
sector1:
            li 25,1
            li 26,6
            addi 27,24,30
got_theta:
            blr

            .rodata
            .byte 0,0
Atan:
            .byte 0,1,1,2,2,3,3,4,5,5
            .byte 6,6,7,7,8,9,9,10,10,11
            .byte 11,12,12,13,13,14,15,15,16,16
            .byte 17,17,18,18,19,19,20,20,21,21
            .byte 22,22,23,23,24,24,25,25,26,26
            .byte 27,27,27,28,28,29,29,30,30,31
            .byte 31,31,32,32,33,33,33,34,34,35
            .byte 35,35,36,36,37,37,37,38,38,38
            .byte 39,39,39,40,40,40,41,41,41,42
            .byte 42,42,43,43,43,44,44,44,44,45
            .byte 45,45,0,0
Sin:
            .short 0,4,9,13,18,22,27,31,36,40
            .short 44,49,53,58,62,66,71,75,79,83
            .short 88,92,96,100,104,108,112,116,120,124
            .short 128,132,136,139,143,147,150,154,158,161
            .short 165,168,171,175,178,181,184,187,190,193
            .short 196,199,202,204,207,210,212,215,217,219
            .short 222,224,226,228,230,232,234,236,237,239
            .short 241,242,243,245,246,247,248,249,250,251
            .short 252,253,254,254,255,255,255,256,256,256
            .short 256,256,256,256,255,255,255,254,254,253
            .short 252,251,250,249,248,247,246,245,243,242
            .short 241,239,237,236,234,232,230,228,226,224,222
            .short 222,222

                        .data
second_switching:       .byte 0
```

```
cap_temp:             .byte 0b100000
Vin_mag:              .short 100
Vin_ph:               .short 0
Vin_Valpha:           .short 0
Vin_Vgamma:           .short 0
Vin_theta:            .short 0
Vout_mag:             .short 100
Vout_ph:              .short 0
Vout_Valpha:          .short 0
Vout_Vgamma:          .short 0
Vout_theta:           .short 0
Iin_A:                .short 0
Iin_B:                .short 0
Iin_C:                .short 0
Iout_a:               .short 0
Iout_b:               .short 0
Iout_c:               .short 0
Iin_ph:               .short 0
Iout_ph:              .short 0
Vcap_Aa:              .short 0
Vcap_Ab:              .short 0
Vcap_Ac:              .short 0
Vcap_Ba:              .short 0
Vcap_Bb:               short 0
Vcap_Bc:              .short 0
Vcap_Ca:              .short 0
Vcap_Cb:              .short 0
Vcap_Cc:              .short 0
volt_dev:             .short 20
cap_temp1:            .short 1
cap_temp2:            .short 1
Vin_AB_x1:            .short 0
Vin_AB_x2:            .short 0
Vin_AB_x3:            .short 0
Vin_AB_x4:            .short 0
Vin_AB_y1:            .short 0
Vin_AB_y2:            .short 0
Vin_AB_y3:            .short 0
Vin_AB_y4:            .short 0
Vin_BC_x1:            .short 0
Vin_BC_x2:            .short 0
Vin_BC_x3:            .short 0
Vin_BC_x4:            .short 0
Vin_BC_y1:            .short 0
Vin_BC_y2:            .short 0
Vin_BC_y3:            .short 0
Vin_BC_y4:            .short 0
temp_temp:            .short 0
```

APPENDIX D

FLASH MEMORY TABLE

This appendix documents the details of the flash memory table. The lookup table consists of three 512 kB flash memory chips. Each chip contains data for the three switch cells that are connected to the same input phase. The inputs for this lookup table are the data denoted the input-side and output-side space vectors, and the capacitor to be used from the PWM controller circuit. The outputs of the lookup table are data specifying the states of all nine switch cells. A high-level description of the lookup table is given in Chapter 6.

The lookup table receives data from the PWM controller circuit, which was implemented inside the Virtex-II Pro. The inputs (address) of this lookup table are 19-bit data, with the bits defined as illustrated in Fig. D.1. Each 19-bit word is divided into three groups: the input-side space vector, the output-side space vector, and the choice of capacitor(s). Given these three data groups, the lookup table provides all nine switch cell states.

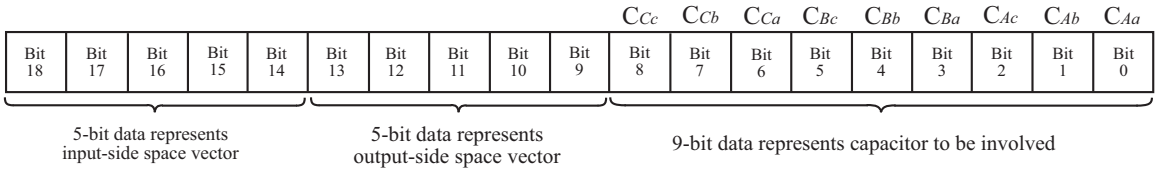


Figure D.1: Assignment of bits for the address of the flash memory.

The space vector for each side is denoted by five-bit data, which can represents all possible 19 space vectors (numbered from 0 to 18) in the basic nine-switch network configuration for the multilevel matrix converter. For any space vector that exceeds this range, the corresponding outputs are all programmed at ``00'', causing all IGBTs to be turned off.

The last nine bits of data specify which capacitor is employed in the current subinterval. Each capacitor is represented by one bit, in the order defined in Fig. D.1. The asserted bit (set to ``1'') means that the corresponding capacitor is connected through conducting switch state. Note that, for a given combination of input space vector and output space vector, not all nine capacitors can be employed. As a result, any combination that includes an invalid choice of capacitor is programmed to turn off all IGBTs.

The outputs of this lookup table are 2-bit data for each of the nine switch cells. Each flash memory chip contains three of 2-bit data for three switch cells that connected in the same input phase. The bit assignment for the output data of each chip is illustrated in Fig. 6.5. The data in the unused bits are set to ``0''.

The following table lists all valid input (address) of the lookup table and the corresponding output data. Chips A, B, and C contain data for the three switch cells that are connected in the input phases A, B, and C, respectively. The remaining addresses (not included in the table) are considered as invalid combinations; hence, the corresponding data are set to all ``0''.

Table D.1: Flash memory data.

Address (hex)	Input-side SV (bin)	Output-side SV (bin)	Capacitor (bin)	Data from chip A (bin)	Data from chip B (bin)	Data from chip C (bin)
0x00001	00000	00000	000000001	0011_1111	0011_1111	0011_1111
0x00002	00000	00000	000000010	0011_1111	0011_1111	0011_1111
0x00004	00000	00000	000000100	0011_1111	0011_1111	0011_1111
0x00008	00000	00000	000001000	0011_1111	0011_1111	0011_1111
0x00010	00000	00000	000010000	0011_1111	0011_1111	0011_1111
0x00020	00000	00000	000100000	0011_1111	0011_1111	0011_1111
0x00040	00000	00000	001000000	0011_1111	0011_1111	0011_1111
0x00080	00000	00000	010000000	0011_1111	0011_1111	0011_1111
0x00100	00000	00000	100000000	0011_1111	0011_1111	0011_1111
0x00201	00000	00001	000000001	0011_1100	0011_1100	0011_1110
0x00208	00000	00001	000001000	0011_1100	0011_1110	0011_1100
0x00240	00000	00001	001000000	0011_1110	0011_1100	0011_1100
0x00404	00000	00010	000000100	0000_1111	0000_1111	0001_1111
0x00420	00000	00010	000100000	0000_1111	0001_1111	0000_1111
0x00500	00000	00010	100000000	0001_1111	0000_1111	0000_1111
0x00602	00000	00011	000000010	0011_0011	0011_0011	0011_1011
0x00610	00000	00011	000010000	0011_0011	0011_1011	0011_0011
0x00680	00000	00011	010000000	0011_1011	0011_0011	0011_0011
0x00801	00000	00100	000000001	0011_1100	0011_1100	0011_1101
0x00808	00000	00100	000001000	0011_1100	0011_1101	0011_1100
0x00840	00000	00100	001000000	0011_1101	0011_1100	0011_1100
0x00A04	00000	00101	000000100	0000_1111	0000_1111	0010_1111
0x00A20	00000	00101	000100000	0000_1111	0010_1111	0000_1111
0x00B00	00000	00101	100000000	0010_1111	0000_1111	0000_1111
0x00C02	00000	00110	000000010	0011_0011	0011_0011	0011_0111
0x00C10	00000	00110	000010000	0011_0011	0011_0111	0011_0011
0x00C80	00000	00110	010000000	0011_0111	0011_0011	0011_0011
0x00E03	00000	00111	000000011	0011_0000	0011_0000	0011_0110
0x00E0A	00000	00111	000001010	0011_0000	0011_0010	0011_0100
0x00E11	00000	00111	000010001	0011_0000	0011_0100	0011_0010
0x00E18	00000	00111	000011000	0011_0000	0011_0110	0011_0000
0x00E42	00000	00111	001000010	0011_0010	0011_0000	0011_0100
0x00E50	00000	00111	001010000	0011_0010	0011_0100	0011_0000
0x00E81	00000	00111	010000001	0011_0100	0011_0000	0011_0010
0x00E88	00000	00111	010001000	0011_0100	0011_0010	0011_0000
0x00EC0	00000	00111	011000000	0011_0110	0011_0000	0011_0000
0x01005	00000	01000	000000101	0000_1100	0000_1100	0001_1110
0x0100C	00000	01000	000001100	0000_1100	0000_1110	0001_1100
0x01021	00000	01000	000100001	0000_1100	0001_1100	0000_1110
0x01028	00000	01000	000101000	0000_1100	0001_1110	0000_1100

Address (hex)	Input-side SV (bin)	Output-side SV (bin)	Capacitor (bin)	Data from chip A (bin)	Data from chip B (bin)	Data from chip C (bin)
0x01044	00000	01000	001000100	0000_1110	0000_1100	0001_1100
0x01060	00000	01000	001100000	0000_1110	0001_1100	0000_1100
0x01101	00000	01000	100000001	0001_1100	0000_1100	0000_1110
0x01108	00000	01000	100001000	0001_1100	0000_1110	0000_1100
0x01140	00000	01000	101000000	0001_1110	0000_1100	0000_1100
0x01206	00000	01001	000000110	0000_0011	0000_0011	0001_1011
0x01214	00000	01001	000010100	0000_0011	0000_1011	0001_0011
0x01222	00000	01001	000100010	0000_0011	0001_0011	0000_1011
0x01230	00000	01001	000110000	0000_0011	0001_1011	0000_0011
0x01284	00000	01001	010000100	0000_1011	0000_0011	0001_0011
0x012A0	00000	01001	010100000	0000_1011	0001_0011	0000_0011
0x01302	00000	01001	100000010	0001_0011	0000_0011	0000_1011
0x01310	00000	01001	100010000	0001_0011	0000_1011	0000_0011
0x01380	00000	01001	110000000	0001_1011	0000_0011	0000_0011
0x01403	00000	01010	000000011	0011_0000	0011_0000	0011_1001
0x0140A	00000	01010	000001010	0011_0000	0011_0001	0011_1000
0x01411	00000	01010	000010001	0011_0000	0011_1000	0011_0001
0x01418	00000	01010	000011000	0011_0000	0011_1001	0011_0000
0x01442	00000	01010	001000010	0011_0001	0011_0000	0011_1000
0x01450	00000	01010	001010000	0011_0001	0011_1000	0011_0000
0x01481	00000	01010	010000001	0011_1000	0011_0000	0011_0001
0x01488	00000	01010	010001000	0011_1000	0011_0001	0011_0000
0x014C0	00000	01010	011000000	0011_1001	0011_0000	0011_0000
0x01605	00000	01011	000000101	0000_1100	0000_1100	0010_1101
0x0160C	00000	01011	000001100	0000_1100	0000_1101	0010_1100
0x01621	00000	01011	000100001	0000_1100	0010_1100	0000_1101
0x01628	00000	01011	000101000	0000_1100	0010_1101	0000_1100
0x01644	00000	01011	001000100	0000_1101	0000_1100	0010_1100
0x01660	00000	01011	001100000	0000_1101	0010_1100	0000_1100
0x01701	00000	01011	100000001	0010_1100	0000_1100	0000_1101
0x01708	00000	01011	100001000	0010_1100	0000_1101	0000_1100
0x01740	00000	01011	101000000	0010_1101	0000_1100	0000_1100
0x01806	00000	01100	000000110	0000_0011	0000_0011	0010_0111
0x01814	00000	01100	000010100	0000_0011	0000_0111	0010_0011
0x01822	00000	01100	000100010	0000_0011	0010_0011	0000_0111
0x01830	00000	01100	000110000	0000_0011	0010_0111	0000_0011
0x01884	00000	01100	010000100	0000_0111	0000_0011	0010_0011
0x018A0	00000	01100	010100000	0000_0111	0010_0011	0000_0011
0x01902	00000	01100	100000010	0010_0011	0000_0011	0000_0111
0x01910	00000	01100	100010000	0010_0011	0000_0111	0000_0011
0x01980	00000	01100	110000000	0010_0111	0000_0011	0000_0011
0x01A4F	00000	01101	001001111	0000_0010	0000_0010	0001_0110

Address (hex)	Input-side SV (bin)	Output-side SV (bin)	Capacitor (bin)	Data from chip A (bin)	Data from chip B (bin)	Data from chip C (bin)
0x01A79	00000	01101	001111001	0000_0010	0001_0110	0000_0010
0x01A97	00000	01101	010010111	0000_0100	0000_0100	0001_0110
0x01ABA	00000	01101	010111010	0000_0100	0001_0110	0000_0100
0x01B27	00000	01101	100100111	0001_0000	0001_0000	0001_0110
0x01B3C	00000	01101	100111100	0001_0000	0001_0110	0001_0000
0x01BC9	00000	01101	111001001	0001_0110	0000_0010	0000_0010
0x01BD2	00000	01101	111010010	0001_0110	0000_0100	0000_0100
0x01BE4	00000	01101	111100100	0001_0110	0001_0000	0001_0000
0x01C4F	00000	01110	001001111	0000_0010	0000_0010	0001_1010
0x01C79	00000	01110	001111001	0000_0010	0001_1010	0000_0010
0x01C97	00000	01110	010010111	0000_1000	0000_1000	0001_1010
0x01CBA	00000	01110	010111010	0000_1000	0001_1010	0000_1000
0x01D27	00000	01110	100100111	0001_0000	0001_0000	0001_1010
0x01D3C	00000	01110	100111100	0001_0000	0001_1010	0001_0000
0x01DC9	00000	01110	111001001	0001_1010	0000_0010	0000_0010
0x01DD2	00000	01110	111010010	0001_1010	0000_1000	0000_1000
0x01DE4	00000	01110	111100100	0001_1010	0001_0000	0001_0000
0x01E4F	00000	01111	001001111	0000_0001	0000_0001	0001_1001
0x01E79	00000	01111	001111001	0000_0001	0001_1001	0000_0001
0x01E97	00000	01111	010010111	0000_1000	0000_1000	0001_1001
0x01EBA	00000	01111	010111010	0000_1000	0001_1001	0000_1000
0x01F27	00000	01111	100100111	0001_0000	0001_0000	0001_1001
0x01F3C	00000	01111	100111100	0001_0000	0001_1001	0001_0000
0x01FC9	00000	01111	111001001	0001_1001	0000_0001	0000_0001
0x01FD2	00000	01111	111010010	0001_1001	0000_1000	0000_1000
0x01FE4	00000	01111	111100100	0001_1001	0001_0000	0001_0000
0x0204F	00000	10000	001001111	0000_0001	0000_0001	0010_1001
0x02079	00000	10000	001111001	0000_0001	0010_1001	0000_0001
0x02097	00000	10000	010010111	0000_1000	0000_1000	0010_1001
0x020BA	00000	10000	010111010	0000_1000	0010_1001	0000_1000
0x02127	00000	10000	100100111	0010_0000	0010_0000	0010_1001
0x0213C	00000	10000	100111100	0010_0000	0010_1001	0010_0000
0x021C9	00000	10000	111001001	0010_1001	0000_0001	0000_0001
0x021D2	00000	10000	111010010	0010_1001	0000_1000	0000_1000
0x021E4	00000	10000	111100100	0010_1001	0010_0000	0010_0000
0x0224F	00000	10001	001001111	0000_0001	0000_0001	0010_0101
0x02279	00000	10001	001111001	0000_0001	0010_0101	0000_0001
0x02297	00000	10001	010010111	0000_0100	0000_0100	0010_0101
0x022BA	00000	10001	010111010	0000_0100	0010_0101	0000_0100
0x02327	00000	10001	100100111	0010_0000	0010_0000	0010_0101
0x0233C	00000	10001	100111100	0010_0000	0010_0101	0010_0000
0x023C9	00000	10001	111001001	0010_0101	0000_0001	0000_0001

Address (hex)	Input-side SV (bin)	Output-side SV (bin)	Capacitor (bin)	Data from chip A (bin)	Data from chip B (bin)	Data from chip C (bin)
0x023D2	00000	10001	111010010	0010_0101	0000_0100	0000_0100
0x023E4	00000	10001	111100100	0010_0101	0010_0000	0010_0000
0x0244F	00000	10010	001001111	0000_0010	0000_0010	0010_0110
0x02479	00000	10010	001111001	0000_0010	0010_0110	0000_0010
0x02497	00000	10010	010010111	0000_0100	0000_0100	0010_0110
0x024BA	00000	10010	010111010	0000_0100	0010_0110	0000_0100
0x02527	00000	10010	100100111	0010_0000	0010_0000	0010_0110
0x0253C	00000	10010	100111100	0010_0000	0010_0110	0010_0000
0x025C9	00000	10010	111001001	0010_0110	0000_0010	0000_0010
0x025D2	00000	10010	111010010	0010_0110	0000_0100	0000_0100
0x025E4	00000	10010	111100100	0010_0110	0010_0000	0010_0000
0x04001	00001	00000	000000001	0011_1111	0011_1111	0000_0001
0x04002	00001	00000	000000010	0011_1111	0011_1111	0000_0100
0x04004	00001	00000	000000100	0011_1111	0011_1111	0001_0000
0x04202	00001	00001	000000010	0011_1100	0011_1100	0000_0111
0x04204	00001	00001	000000100	0011_1100	0011_1100	0001_0011
0x04208	00001	00001	000001000	0011_1100	0011_1110	0000_0011
0x04240	00001	00001	001000000	0011_1110	0011_1100	0000_0011
0x04404	00001	00010	000000100	0011_0000	0011_0000	0001_1111
0x04408	00001	00010	000001000	0011_0000	0011_0010	0000_1111
0x04410	00001	00010	000010000	0011_0000	0011_1000	0000_1111
0x04440	00001	00010	001000000	0011_0010	0011_0000	0000_1111
0x04480	00001	00010	010000000	0011_1000	0011_0000	0000_1111
0x04601	00001	00011	000000001	0011_0011	0011_0011	0000_1101
0x04604	00001	00011	000000100	0011_0011	0011_0011	0001_1100
0x04610	00001	00011	000010000	0011_0011	0011_1011	0000_1100
0x04680	00001	00011	010000000	0011_1011	0011_0011	0000_1100
0x04801	00001	00100	000000001	0000_0011	0000_0011	0011_1101
0x04810	00001	00100	000010000	0000_0011	0000_1011	0011_1100
0x04820	00001	00100	000100000	0000_0011	0010_0011	0011_1100
0x04880	00001	00100	010000000	0000_1011	0000_0011	0011_1100
0x04900	00001	00100	100000000	0010_0011	0000_0011	0011_1100
0x04A01	00001	00101	000000001	0000_1111	0000_1111	0011_0001
0x04A02	00001	00101	000000010	0000_1111	0000_1111	0011_0100
0x04A20	00001	00101	000100000	0000_1111	0010_1111	0011_0000
0x04B00	00001	00101	100000000	0010_1111	0000_1111	0011_0000
0x04C02	00001	00110	000000010	0000_1100	0000_1100	0011_0111
0x04C08	00001	00110	000001000	0000_1100	0000_1110	0011_0011
0x04C20	00001	00110	000100000	0000_1100	0010_1100	0011_0011
0x04C40	00001	00110	001000000	0000_1110	0000_1100	0011_0011
0x04D00	00001	00110	100000000	0010_1100	0000_1100	0011_0011
0x08040	00010	00000	001000000	0000_0010	0011_1111	0011_1111

Address (hex)	Input-side SV (bin)	Output-side SV (bin)	Capacitor (bin)	Data from chip A (bin)	Data from chip B (bin)	Data from chip C (bin)
0x08080	00010	00000	010000000	0000_1000	0011_1111	0011_1111
0x08100	00010	00000	100000000	0010_0000	0011_1111	0011_1111
0x08202	00010	00001	000000010	0011_1100	0000_0011	0000_0111
0x08204	00010	00001	000000100	0011_1100	0000_0011	0001_0011
0x08210	00010	00001	000010000	0011_1100	0000_0111	0000_0011
0x08220	00010	00001	000100000	0011_1100	0001_0011	0000_0011
0x08240	00010	00001	001000000	0011_1110	0000_0011	0000_0011
0x08404	00010	00010	000000100	0011_0000	0000_1111	0001_1111
0x08420	00010	00010	000100000	0011_0000	0001_1111	0000_1111
0x08440	00010	00010	001000000	0011_0010	0000_1111	0000_1111
0x08480	00010	00010	010000000	0011_1000	0000_1111	0000_1111
0x08601	00010	00011	000000001	0011_0011	0000_1100	0000_1101
0x08604	00010	00011	000000100	0011_0011	0000_1100	0001_1100
0x08608	00010	00011	000001000	0011_0011	0000_1101	0000_1100
0x08620	00010	00011	000100000	0011_0011	0001_1100	0000_1100
0x08680	00010	00011	010000000	0011_1011	0000_1100	0000_1100
0x08801	00010	00100	000000001	0000_0011	0011_1100	0011_1101
0x08808	00010	00100	000001000	0000_0011	0011_1101	0011_1100
0x08880	00010	00100	010000000	0000_1011	0011_1100	0011_1100
0x08900	00010	00100	100000000	0010_0011	0011_1100	0011_1100
0x08A01	00010	00101	000000001	0000_1111	0011_0000	0011_0001
0x08A02	00010	00101	000000010	0000_1111	0011_0000	0011_0100
0x08A08	00010	00101	000001000	0000_1111	0011_0001	0011_0000
0x08A10	00010	00101	000010000	0000_1111	0011_0100	0011_0000
0x08B00	00010	00101	100000000	0010_1111	0011_0000	0011_0000
0x08C02	00010	00110	000000010	0000_1100	0011_0011	0011_0111
0x08C10	00010	00110	000010000	0000_1100	0011_0111	0011_0011
0x08C40	00010	00110	001000000	0000_1110	0011_0011	0011_0011
0x08D00	00010	00110	100000000	0010_1100	0011_0011	0011_0011
0x0C008	00011	00000	000001000	0011_1111	0000_0001	0011_1111
0x0C010	00011	00000	000010000	0011_1111	0000_0100	0011_1111
0x0C020	00011	00000	000100000	0011_1111	0001_0000	0011_1111
0x0C201	00011	00001	000000001	0011_1100	0000_0011	0011_1110
0x0C210	00011	00001	000010000	0011_1100	0000_0111	0011_1100
0x0C220	00011	00001	000100000	0011_1100	0001_0011	0011_1100
0x0C240	00011	00001	001000000	0011_1110	0000_0011	0011_1100
0x0C401	00011	00010	000000001	0011_0000	0000_1111	0011_0010
0x0C402	00011	00010	000000010	0011_0000	0000_1111	0011_1000
0x0C420	00011	00010	000100000	0011_0000	0001_1111	0011_0000
0x0C440	00011	00010	001000000	0011_0010	0000_1111	0011_0000
0x0C480	00011	00010	010000000	0011_1000	0000_1111	0011_0000
0x0C602	00011	00011	000000010	0011_0011	0000_1100	0011_1011

Address (hex)	Input-side SV (bin)	Output-side SV (bin)	Capacitor (bin)	Data from chip A (bin)	Data from chip B (bin)	Data from chip C (bin)
0x0C608	00011	00011	000001000	0011_0011	0000_1101	0011_0011
0x0C620	00011	00011	000100000	0011_0011	0001_1100	0011_0011
0x0C680	00011	00011	010000000	0011_1011	0000_1100	0011_0011
0x0C802	00011	00100	000000010	0000_0011	0011_1100	0000_1011
0x0C804	00011	00100	000000100	0000_0011	0011_1100	0010_0011
0x0C808	00011	00100	000001000	0000_0011	0011_1101	0000_0011
0x0C880	00011	00100	010000000	0000_1011	0011_1100	0000_0011
0x0C900	00011	00100	100000000	0010_0011	0011_1100	0000_0011
0x0CA04	00011	00101	000000100	0000_1111	0011_0000	0010_1111
0x0CA08	00011	00101	000001000	0000_1111	0011_0001	0000_1111
0x0CA10	00011	00101	000010000	0000_1111	0011_0100	0000_1111
0x0CB00	00011	00101	100000000	0010_1111	0011_0000	0000_1111
0x0CC01	00011	00110	000000001	0000_1100	0011_0011	0000_1110
0x0CC04	00011	00110	000000100	0000_1100	0011_0011	0010_1100
0x0CC10	00011	00110	000010000	0000_1100	0011_0111	0000_1100
0x0CC40	00011	00110	001000000	0000_1110	0011_0011	0000_1100
0x0CD00	00011	00110	100000000	0010_1100	0011_0011	0000_1100
0x10001	00100	00000	000000001	0011_1111	0011_1111	0000_0010
0x10002	00100	00000	000000010	0011_1111	0011_1111	0000_1000
0x10004	00100	00000	000000100	0011_1111	0011_1111	0010_0000
0x10201	00100	00001	000000001	0000_0011	0000_0011	0011_1110
0x10210	00100	00001	000010000	0000_0011	0000_0111	0011_1100
0x10220	00100	00001	000100000	0000_0011	0001_0011	0011_1100
0x10280	00100	00001	010000000	0000_0111	0000_0011	0011_1100
0x10300	00100	00001	100000000	0001_0011	0000_0011	0011_1100
0x10401	00100	00010	000000001	0000_1111	0000_1111	0011_0010
0x10402	00100	00010	000000010	0000_1111	0000_1111	0011_1000
0x10420	00100	00010	000100000	0000_1111	0001_1111	0011_0000
0x10500	00100	00010	100000000	0001_1111	0000_1111	0011_0000
0x10602	00100	00011	000000010	0000_1100	0000_1100	0011_1011
0x10608	00100	00011	000001000	0000_1100	0000_1101	0011_0011
0x10620	00100	00011	000100000	0000_1100	0001_1100	0011_0011
0x10640	00100	00011	001000000	0000_1101	0000_1100	0011_0011
0x10700	00100	00011	100000000	0001_1100	0000_1100	0011_0011
0x10802	00100	00100	000000010	0011_1100	0011_1100	0000_1011
0x10804	00100	00100	000000100	0011_1100	0011_1100	0010_0011
0x10808	00100	00100	000001000	0011_1100	0011_1101	0000_0011
0x10840	00100	00100	001000000	0011_1101	0011_1100	0000_0011
0x10A04	00100	00101	000000100	0011_0000	0011_0000	0010_1111
0x10A08	00100	00101	000001000	0011_0000	0011_0001	0000_1111
0x10A10	00100	00101	000010000	0011_0000	0011_0100	0000_1111
0x10A40	00100	00101	001000000	0011_0001	0011_0000	0000_1111

Address (hex)	Input-side SV (bin)	Output-side SV (bin)	Capacitor (bin)	Data from chip A (bin)	Data from chip B (bin)	Data from chip C (bin)
0x10A80	00100	00101	010000000	0011_0100	0011_0000	0000_1111
0x10C01	00100	00110	000000001	0011_0011	0011_0011	0000_1110
0x10C04	00100	00110	000000100	0011_0011	0011_0011	0010_1100
0x10C10	00100	00110	000010000	0011_0011	0011_0111	0000_1100
0x10C80	00100	00110	010000000	0011_0111	0011_0011	0000_1100
0x14040	00101	00000	001000000	0000_0001	0011_1111	0011_1111
0x14080	00101	00000	010000000	0000_0100	0011_1111	0011_1111
0x14100	00101	00000	100000000	0001_0000	0011_1111	0011_1111
0x14201	00101	00001	000000001	0000_0011	0011_1100	0011_1110
0x14208	00101	00001	000001000	0000_0011	0011_1110	0011_1100
0x14280	00101	00001	010000000	0000_0111	0011_1100	0011_1100
0x14300	00101	00001	100000000	0001_0011	0011_1100	0011_1100
0x14401	00101	00010	000000001	0000_1111	0011_0000	0011_0010
0x14402	00101	00010	000000010	0000_1111	0011_0000	0011_1000
0x14408	00101	00010	000001000	0000_1111	0011_0010	0011_0000
0x14410	00101	00010	000010000	0000_1111	0011_1000	0011_0000
0x14500	00101	00010	100000000	0001_1111	0011_0000	0011_0000
0x14602	00101	00011	000000010	0000_1100	0011_0011	0011_1011
0x14610	00101	00011	000010000	0000_1100	0011_1011	0011_0011
0x14640	00101	00011	001000000	0000_1101	0011_0011	0011_0011
0x14700	00101	00011	100000000	0001_1100	0011_0011	0011_0011
0x14802	00101	00100	000000010	0011_1100	0000_0011	0000_1011
0x14804	00101	00100	000000100	0011_1100	0000_0011	0010_0011
0x14810	00101	00100	000010000	0011_1100	0000_1011	0000_0011
0x14820	00101	00100	000100000	0011_1100	0010_0011	0000_0011
0x14840	00101	00100	001000000	0011_1101	0000_0011	0000_0011
0x14A04	00101	00101	000000100	0011_0000	0000_1111	0010_1111
0x14A20	00101	00101	000100000	0011_0000	0010_1111	0000_1111
0x14A40	00101	00101	001000000	0011_0001	0000_1111	0000_1111
0x14A80	00101	00101	010000000	0011_0100	0000_1111	0000_1111
0x14C01	00101	00110	000000001	0011_0011	0000_1100	0000_1110
0x14C04	00101	00110	000000100	0011_0011	0000_1100	0010_1100
0x14C08	00101	00110	000001000	0011_0011	0000_1110	0000_1100
0x14C20	00101	00110	000100000	0011_0011	0010_1100	0000_1100
0x14C80	00101	00110	010000000	0011_0111	0000_1100	0000_1100
0x18008	00110	00000	000001000	0011_1111	0000_0010	0011_1111
0x18010	00110	00000	000010000	0011_1111	0000_1000	0011_1111
0x18020	00110	00000	000100000	0011_1111	0010_0000	0011_1111
0x18202	00110	00001	000000010	0000_0011	0011_1100	0000_0111
0x18204	00110	00001	000000100	0000_0011	0011_1100	0001_0011
0x18208	00110	00001	000001000	0000_0011	0011_1110	0000_0011
0x18280	00110	00001	010000000	0000_0111	0011_1100	0000_0011

Address (hex)	Input-side SV (bin)	Output-side SV (bin)	Capacitor (bin)	Data from chip A (bin)	Data from chip B (bin)	Data from chip C (bin)
0x18300	00110	00001	100000000	0001_0011	0011_1100	0000_0011
0x18404	00110	00010	000000100	0000_1111	0011_0000	0001_1111
0x18408	00110	00010	000001000	0000_1111	0011_0010	0000_1111
0x18410	00110	00010	000010000	0000_1111	0011_1000	0000_1111
0x18500	00110	00010	100000000	0001_1111	0011_0000	0000_1111
0x18601	00110	00011	000000001	0000_1100	0011_0011	0000_1101
0x18604	00110	00011	000000100	0000_1100	0011_0011	0001_1100
0x18610	00110	00011	000010000	0000_1100	0011_1011	0000_1100
0x18640	00110	00011	001000000	0000_1101	0011_0011	0000_1100
0x18700	00110	00011	100000000	0001_1100	0011_0011	0000_1100
0x18801	00110	00100	000000001	0011_1100	0000_0011	0011_1101
0x18810	00110	00100	000010000	0011_1100	0000_1011	0011_1100
0x18820	00110	00100	000100000	0011_1100	0010_0011	0011_1100
0x18840	00110	00100	001000000	0011_1101	0000_0011	0011_1100
0x18A01	00110	00101	000000001	0011_0000	0000_1111	0011_0001
0x18A02	00110	00101	000000010	0011_0000	0000_1111	0011_0100
0x18A20	00110	00101	000100000	0011_0000	0010_1111	0011_0000
0x18A40	00110	00101	001000000	0011_0001	0000_1111	0011_0000
0x18A80	00110	00101	010000000	0011_0100	0000_1111	0011_0000
0x18C02	00110	00110	000000010	0011_0011	0000_1100	0011_0111
0x18C08	00110	00110	000001000	0011_0011	0000_1110	0011_0011
0x18C20	00110	00110	000100000	0011_0011	0010_1100	0011_0011
0x18C80	00110	00110	010000000	0011_0111	0000_1100	0011_0011

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The goal of this project was to develop a new modular multilevel matrix converter for wind power applications and to demonstrate a working scale model in the laboratory.

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wind energy; wind turbine; grid; generator; voltage; converter

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