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# Breakthrough in Power Electronics from SiC

## May 25, 2004 to May 31, 2005

D.A. Marckx
*Peregrine Power LLC*
*Wilsonville, Oregon*

*Subcontract Report*
**NREL/SR-500-38515**
**March 2006**

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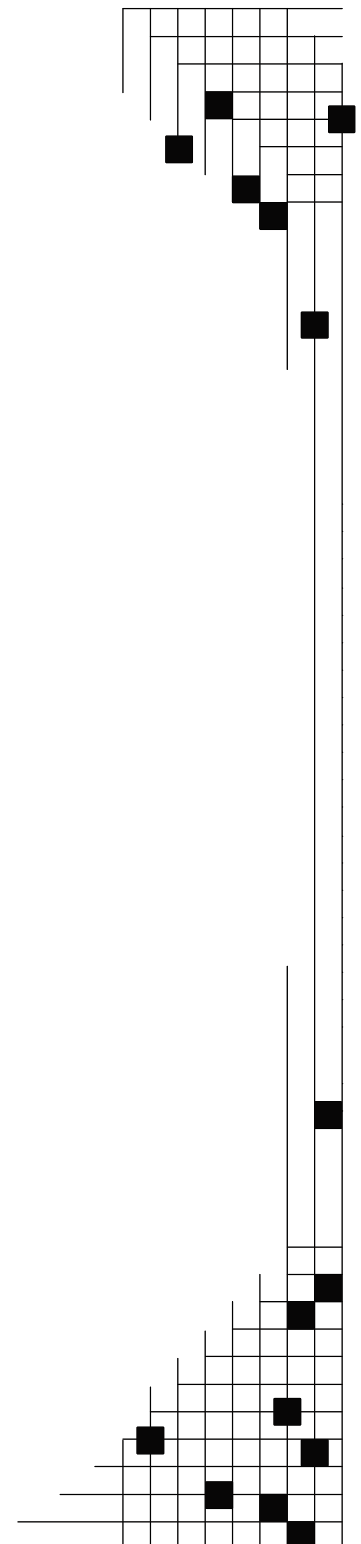

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# List of Abbreviations

| | |
|---|---|
| AIN | aluminum nitride |
| BJT | bipolar junction transistor |
| CAD | computer aided design |
| COE | cost of energy |
| CTE | coefficient of thermal expansion |
| CVD | chemical-vapor-disposition |
| DARPA | Defense Advanced Research Projects Agency |
| DBC | direct bonded copper |
| dv/dt | rate of change of voltage with respect to time |
| di/dt | rate of change of current with respect to time |
| FEA | finite element analysis |
| GTO | gate turn-off thyristor |
| IGBT | insulated gate bipolar transistor |
| IC | integrated circuit |
| JFET | function field effect transistors |
| LLC | limited liability company |
| LED | light emitting diode |
| MOSFET | metal oxide semiconductor field excited transistor |
| MW | megawatt |
| NREL | National Renewable Energy Laboratory |
| PM | permanent magnet |
| PN | regions of a power semiconductor doped as P and N material |
| PWM | pulse-width modulation |
| R&D | research and development |
| SCR | silicon controlled rectifier |
| SiC | silicon carbide |
| SKiiP | Semikron integrated intelligent power (module) |
| SOI | silicon-on-insulator |
| UTenn | University of Tennessee |

# 1.0 EXECUTIVE SUMMARY

## 1.1 Background

The premise of the project was that silicon carbide (SiC) devices would substantially reduce the cost of energy (COE) of large wind turbines that need power electronics for variable-speed generation systems. Variable-speed capability allows the wind turbine to operate at the speed that produces the greatest amount of power and minimizes torque perturbations in the drive train. This capability tends to decrease the overall COE because the amount of energy generated is increased, and the cost of the drive train and its maintenance is reduced. Because the voltage and frequency of the generated power varies with turbine speed, a solid-state converter is required to reconcile the output with the fixed voltage and frequency of the grid.

As a wide band-gap material, SiC in power devices has several advantages, including lower losses, higher temperature, and faster switching. These can be exploited to reduce losses and increase energy production. The lower losses, along with higher temperature, can be exploited to reduce material and potentially the cost of the converter. SiC devices have been in development over 20 years due to widespread expectations of their superior performance and are now becoming available as practical prototypes. One of the key activities of the project was to obtain SiC devices that might be used in a wind turbine converter and then test and characterize them relative to the commonly used insulated gate bipolar transistor (IGBT).

## 1.2 Baseline Turbine

The point of comparison in the project is the NREL baseline wind turbine described in Reference 1, a report carried out by Global Energy Concepts for NREL (the Drive Train Report). The Drive Train Report considers a number of alternatives for the drive train components, including the generator, gearbox and power electronics. The alternative from the Drive Train Report, which became the baseline for this project, is rated at 1.5 MW and uses a single permanent magnet (PM) generator rated nominally at 690 volts, along with a gearbox and a bi-directional converter providing power conditioning for the full output of the generator. The baseline converter is thus rated at 1.5 MW and comprised of two back-to-back inverters with IGBTs rated at 1,700 volts using a hard switching PWM strategy at 3,000 Hz. Due to lack of availability of adequately rated devices, the baseline converter is made up of two sets of inverters of half rating which operate in parallel.

## 1.3 Adjustments in the Statement of Work

The initial expectation of this project was that the development of a converter using SiC devices would have many similarities to more conventional converter design work with commonly known device characteristics and packaging techniques. The second expectation was that the inverter could be designed in a straight-forward manner. The major exception to that process was expected to be the characterization of real SiC devices to get new loss data. This was naïve. Much more basic work had to be carried out.

It was much more difficult to characterize SiC device technologies than expected. The team had to develop comparative summaries of the various types of SiC devices. In addition, if SiC devices were to be used to maximum advantage (at higher temperature), virtually every element of a device and inverter package had to be completely redesigned using new materials, fabrication processes and geometries, and a host of thermal and stress calculations using computer aided design (CAD) tools had to be completed.

Finally, we concluded that SiC devices should be used at higher voltage where there was little or no information available to evaluate.

## 1.4 Project Team

The project team consisted of several people directly associated with Peregrine Power LLC, along with Cree, Inc., who supplied the SiC metal oxide semiconductor field excited transistors (MOSFETs), and the University of Tennessee and Oak Ridge National Laboratory, who tested and modeled SiC devices. In addition, the principal investigator communicated with numerous firms and individuals with expertise in power semiconductors, SiC, high temperature packaging, and other pertinent disciplines.

## 1.5 Conclusions

The major conclusions are as follows:

- Appropriate SiC devices will be available during the next five years for use in wind turbines.
- SiC devices are ideally suited to the higher voltages needed in multi-megawatt wind turbines of the future.
- Future prices for SiC dies cannot be predicted, but the cost of fabricating power semiconductors of all types is highly impacted by increased yields and volume, giving optimism that prices will become competitive. Cost competitiveness must be determined by considering a dramatic reduction in material and increased voltage, both enabled by SiC.
- A SiC-based converter is expected to have losses of about one-third of that for a silicon-based converter in a wind turbine, leading to an increase in energy production in the 2% to 3% range.
- A reduction in the 30% to 50% range of the switching losses (or 15% to 25% range of the total losses) can be realized by replacing the standard silicon free wheeling diode with a SiC Schottky diode. This has been translated to a 0.4% increase in average efficiency and energy production, a modest improvement.
- Improvements in efficiency are particularly significant at low power levels where wind turbines operate most of the time.
- Using SiC devices to maximum advantage requires that the nominal voltage of the wind turbine be increased from 690 to 4,160 VAC.
- Using SiC devices to maximum advantage also requires that the packaging for the SiC dies and inverter power block be increased to 300°C. Such packaging is believed to be feasible in the near future.

- The size and material content of a SiC-based inverter power block operating at 300ºC and 4,160 VAC will be about one-sixth of that for a silicon-based version operating at 125ºC and 690 VAC.

## 1.6 Recommendations

The team believes it would be highly advantageous to the U.S. energy community in general, and wind turbine industry in particular, to develop an extraordinarily compact SiC-based inverter module that could be used in multi-megawatt power electronic converters. The following general tasks are recommended:

- Work with one or more potential suppliers of SiC devices in specifying and obtaining SiC devices for use at medium voltage.
- Test, characterize, and model the high-voltage devices.
- Develop and test a high temperature device/inverter package.
- Develop detailed pricing with the assistance of appropriate vendors.

# 2.0 PROJECT GOALS AND WORK PLAN

## 2.1 Contract Objectives and Tasks

The underlying premise of the project was that SiC devices would reduce substantially the COE of large wind turbines. Most, if not all, future large wind turbines used for generating bulk power at the lowest cost will have variable-speed generation systems. Variable-speed capability allows the wind turbine to (1) operate at the speed that produces the greatest amount of power at any given wind speed, and (2) minimize torque on the drive train. Power factor control might be another benefit. This capability tends to decrease the overall COE because the amount of energy generated is increased, and the cost of the drive train and its maintenance is reduced. Because the voltage and frequency of the generated power varies with speed, a solid-state converter is required to reconcile the output with the fixed voltage and frequency of the grid.

SiC devices were expected to have two general advantages on COE. The first expected SiC advantage was greater efficiency and a reduction in converter losses from the 5% to 6% range to the 1% to 2% range (thereby increasing net output by 4% to 5%.) The second expected advantage was higher temperature operations. Reduced losses and higher operating temperature can be exploited to reduce material and cost of the converter.

SiC devices have been in development for more than 20 years and have gained widespread recognition for superior performance as a wide band-gap material. The availability of SiC device prototypes in the last two years has allowed testing to determine improvements and the cost of improvements using the National Renewable Energy Laboratory (NREL) baseline wind turbine. Therefore, one of the key activities of the project was to actually obtain SiC devices that might be used in a wind turbine converter, and to test and characterize them relative to the commonly used IGBT. Peregrine obtained SiC MOSFET prototypes from Cree, Inc., (Cree) rated at 1,200 V, the appropriate voltage for use in a converter operating in a 480 V environment. Although the baseline wind turbine operated at 690 V, these devices were sufficiently close to those required in the baseline turbine so that the results are still meaningful.

The substantive tasks proposed for the project (omitting purely administrative and reporting tasks 1 and 2) were as follows:

- Task 3. Obtain Prototype SiC MOSFETs and Related Technical Information
- Task 4. Design Gate Drive Circuits
- Task 5. Characterize SiC MOSFETs Through Testing
- Task 6. Develop Semiconductor Model
- Task 7. Define Appropriate Converter for Wind Turbine
- Task 8. Apply Model to Predict Performance
- Task 9. Determine the impact of SiC Semiconductors on Filter Elements
- Task 10. Plan Next Project Phase
- Task 11. Determine the Readiness of SiC Technology
- Task 16. Update Cost of Energy

## 2.2 Baseline Turbine

The point of comparison for the project is the baseline design described in NREL's *Alternative Design Study Report: WindPACT Advanced Wind Turbine Drive Train Designs Study* [1]. The report considers a number of alternatives for the drive train components (other than the rotor), including the generator, gearbox and power electronics. Included in the comparison of alternatives is other electrical equipment that is not technically part of the drive train but is impacted by the drive train (transformers, VAR control equipment, filters, etc.)

One of the most common electrical configurations today for large wind turbines uses a so-called doubly-fed generator (wound rotor machine with slip rings) with a 33% rated converter. The converter is bidirectional and generally comprised of two back-to-back inverters for providing active control on both the generator and utility sides. Other more innovative configurations were analyzed, but this well recognized approach became the baseline in the report. Some of the other alternatives were close in terms of COE.

Since the report was published, a new requirement has been proposed–wind turbines must be able to stay grid-connected and feed a fault for a period of 0.625 ms at a grid voltage of 15%. Because the doubly-fed generator configuration would be difficult to control in these circumstances, another configuration has replaced this as the baseline.

The baseline configuration has the following characteristics: 1.5 MW rating, permanent magnet (PM) generator rated nominally at 690 V, gearbox, and a bidirectional converter providing power conditioning for the full rating of the generator. More specifically, the converter is rated at 1.5 MW and comprised of two back-to-back inverters with IGBTs rated at 1,700 V using a hard switching PWM strategy at 3,000 Hz. Because adequate devices are not readily available, the baseline converter is made up of two sets of inverters operating in parallel at half rating. The technical operating data for this configuration can be found on page G-9 of the report [1]. Any comparison of SiC devices to silicon devices is made in this context. Other specifications for the baseline wind turbine are not germane to the project.

## 2.3 Reorientation of Some Project Work

The initial expectation of the team was that the development of a converter in this project using SiC devices would have many similarities to more conventional converter design work, where device characterization and packaging techniques are largely known, and all of elements of an inverter can be selected and assembled in a straight-forward manner. The major exception to that process was expected to be the characterization of real SiC devices, thus getting new heating data that could be inserted into thermal models for semiconductor blocks that use well known materials and geometries. This was naïve. Much more basic work had to be carried out.

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The first goal of a concept study is to determine feasibility. It was more difficult to evaluate SiC device technologies than expected. The development of power semiconductors involves very complex and sophisticated technologies. Information about SiC is spread among many different organizations and is sometimes difficult to acquire. No useful comparative summaries of the various types of SiC devices existed. Such summaries had to be developed during this project.

Having actual SiC MOSFETS for testing helped immensely, but did not answer all questions about technology readiness or future potential.

In addition, if SiC devices are to be used to maximum advantage (at higher temperature), virtually every element of a device and inverter package must be completely redesigned. That exercise requires extensive knowledge of semiconductor packaging and many new materials, fabrication processes and geometries, and the completion of a multitude of thermal and stress calculations using CAD tools. The information needed about packaging was fragmented with no one organization seriously integrating an entire, high performance SiC device package. It was not clear what was even technically feasible, let alone how much it would cost.

Finally, SiC devices should be used at higher voltage, which requires efforts that are not part of the statement of work. There is little or no information available at higher voltage. While significant quantitative information is being presented here, a major fraction of the work was refocused to more basic questions and fundamental scientific obstacles. These difficulties indicated the lack of readiness of SiC as a power semiconductor.

The team carried out more feasibility work than expected in the following areas:

- Determining how the various types of SiC devices will perform and which ones make sense in wind turbines
- Identifying how the unique properties of SiC devices can be exploited to best advantage
- Developing a high temperature power semiconductor package that will be reliable and cost effective
- Estimating the ultimate impact of SiC at a high level.

## 2.4 Project Team

The project team members associated directly with Peregrine included the following:

- Dallas A. Marckx, Principal Investigator
- Brian Ratliff, Engineer–Mechanical & Thermal
- Larry Rinehart, Consultant–Semiconductors
- Chris Carlson, Senior Engineer–Power Electronics
- Dr. Cathy Biber, Consultant–Thermal Management

Other individuals and organizations include the following:

- Cree Inc.– provided prototype SiC MOSFETs
- Dr. Leon Tolbert, employed by both the University of Tennessee & Oak Ridge National Laboratory–tested the SiC MOSFET prototypes (See Appendix )
- NREL–provided wind turbine information and other guidance

In addition, the principal investigator communicated with numerous firms and individuals with expertise in power semiconductors, SiC, high temperature packaging, and other pertinent disciplines. Key people in this group include

- Dr. Philip Neudeck of NASA (Glen Research Center in Cleveland, Ohio)
- Dr. Peter Friedrichs of SiCED (subsidiary of Siemens/Infineon in Erlangen, Germany)
- Dr. James Scofield of the Air Force Research Laboratory (Dayton, Ohio)

- Dr. James Cooper of Purdue University (West Lafayette, Indiana)
- Dr. Werner Tursky of Semikron (Nürnberg, Germany)
- Dr. Jian Zhao of Rutgers University (Piscataway, New Jersey).

The project took the Peregrine team into technical areas that seem distant from their experience in the design, fabrication and application of power electronics converters. The pertinent disciplines included semiconductors at the most sophisticated level, advanced materials, and micro level fabrication processes. However, the work being done by others in those disciplines must ultimately be evaluated by companies, like Peregrine, who will use the results and apply hardnosed commercial criteria. A researcher specializing in a narrow slice of this would not have the proper perspective. In addition, Peregrine is in a better position to integrate the various, fragmented technologies.

## 3.0 SILICON CARBIDE – PROMISE AND PROBLEMS

### 3.1 Merits of Silicon Carbide Semiconductors

Essentially all commonly used power semiconductors in power converters today are based on standard silicon technologies with a variety of known limitations that challenge power electronics designers. Based on the potential of better performance, SiC has been awarded substantial development funding from government and private organizations.

SiC is termed a wide band-gap material, referring to the stability of the outer electrons. It possesses extremely high thermal, chemical, and mechanical stability. A large amount of energy must be injected to lift the electrons to a state where they will facilitate molecular processes. It is reported to be the third hardest known material. SiC is by far the most developed of the wide band-gap semiconductors due to 1) the availability of high quality SiC substrates, 2) advances in chemical-vapor-deposition (CVD) growth of epitaxial structures, 3) the ability to easily dope n- and p-type materials, and 4) the ability to produce high quality native oxide.

SiC has over 170 polytypes, each of which has different physical properties. The best-known polytypes are 3C-SiC, 4H-SiC, and 6H-SiC, but only the last two are commercially available. The polytype 4H-SiC is preferred for power devices because of its high carrier mobility and its low dopant ionization energy. Some of the properties of semiconductor materials are given in the Table 1.

**Table 1. Basic Properties of Semiconductor Materials**

| Material | Bandgap Energy (eV) | Breakdown Field (MV/cm) | Electron Mobility ($cm^2$/V-s) | Electron Drift Vsat (cm/s) | Thermal Conductivity (W/m/K) |
|---|---|---|---|---|---|
| Si | 1.12 | 0.6 | 1,100 | $1 \times 10^7$ | 150 |
| GaAs | 1.42 | 0.6 | 6,000 | $8 \times 10^8$ | 50 |
| GaN | 3.39 | 3.3 | 1,000 | $2.5 \times 10^7$ | 130 |
| 3C-SiC | 2.2 | 2 | 750 | $2.5 \times 10^7$ | 500 |
| 4H-SiC | 3.26 | 3 | 800 | $2 \times 10^7$ | 490 |
| 6H-SiC | 3 | 3.2 | 370 | $2 \times 10^7$ | 490 |
| Diamond | 5.5 | 6 | 2,200 | $2.7 \times 10^7$ | 2000 |

The favorable characteristics of SiC compared to silicon are discussed in detail in a variety of technical reports. An excellent example is found in *Impact of SiC Power Electronic Devices for Hybrid Electric Vehicles,* by Dr. Leon M. Tolbert [2]. Pertinent information can also be found in

many of the other listed references. Each of the potential SiC benefits will now be summarized and qualified where there are factors that may reduce the benefits significantly.

- ***Lower resistance and conduction losses.*** A SiC semiconductor die is much thinner on account of its high dielectric strength and is doped to a much higher level. This may lead to lower losses and smaller, less expensive heat removal hardware. The basic physics indicate that the forward resistance across the blocking layer of a MOSFET, for example, is about 1/400$^{th}$ of that for silicon. Qualification: This is a startling theoretical limit that has turned many heads. Experts will quickly add that this figure is highly misleading. The statement describes only the blocking or drift region. This is often the thickest layer through which the current must past from source to drain and is important, but the current must pass through other regions and connections, and these generally do not have such low resistances. The other resistances, which are additive when placed in series, generally dilute the forward conduction benefit substantially. In fact, some SiC devices have higher conduction losses than their silicon counterparts. To bring this point home, the SiC MOSFETs tested in this project had considerably higher conduction losses (over a factor of two) at full power than the silicon IGBTs they would replace, but they had about the same conduction losses on the average given a realistic operating scenario that includes operation at low power much of the time. The conduction loss for the SiC MOSFET will undoubtedly improve in the years ahead and beat the silicon counterpart, but it will not be an order of magnitude better at high current levels.

- ***Lower switching losses, due to faster, cleaner turn-on/ turn-off characteristics.*** This is a true statement without much need for qualification. In addition, devices with extraordinarily fast, low loss switching (e.g., MOSFETs and Schottky diodes) can be used at higher voltages when made of SiC. Thus, a SiC MOSFET can be realistically used in a 480 V or 690 V converter, rather than a silicon IGBT, to increase switching frequency from, say, 5 kHz to 50 kHz. A MOSFET could not be used in this application if made of silicon. While a Schottky diode might be rated at less than 200 volts when made of silicon, it can easily withstand 1,200 to 1,700 V when made of SiC. A Schottky can then be used as the reverse or anti-parallel diode which accompanies a transistor to protect it from reverse voltage bias. The SiC Schottky, which is in the market today, has little reverse recovery current, a significant source of switching losses in a typical inverter bridge, particularly at low power. Qualification: Translating the switching improvements into a bottom line product improvement is, however, a function of the application. If higher speed switching is not needed, the product improvement would be small.

- ***Higher dielectric constant, permitting higher voltage applications.*** Some types of SiC devices will be able to withstand 10,000 V and some may be able to withstand more than 20,000 V. This characteristic can be used to increase the voltage of the variable-speed wind turbine to, say, 2,300 VAC or 4,160 VAC (standard industrial medium voltages), thus decreasing current substantially, along with the size and cost of all current-carrying components, including the generator. This benefit is quite real and requires no qualification. Indeed, this is the basis for recommending in this report that a large wind turbine use medium voltage.

- ***Higher thermal conductivity.*** SiC has conductivity about three times as high as standard silicon; thus losses in the form of heat will be conducted from within the semiconductor with a much lower temperature drop across the semiconductor material. That, coupled with its lesser thickness, allows the die to be driven much harder and reduces material and cost. Qualification: Higher conductivity is always a plus, but this scientific fact is probably not as important as the next listed benefit. If the device temperature is increased to, say 300°C or more, the conductivity within the thin layer of the SiC die is not particularly important. The maximum temperature difference within the SiC die to drive its heat outward is not even 1°C.

- ***Much higher operating temperature, well over 400°C.*** This should be compared to 125° to 150°C with standard silicon technology. This characteristic leads to the use of much greater temperature differentials and less material and potentially cost. It also leads to the ability to use low-cost air-cooling hardware rather than liquid cooling to a much higher power level. It almost does not matter what the ambient air temperature is if the semiconductor die can operate at over 350°C (662°F); there will always be ample temperature differential to drive the heat out of the semiconductor package. Qualifications: The first qualification is that some devices, such as the MOSFET, contain an oxide that is fundamental to their operation. The oxide layer will breakdown in the 200°C area. Ongoing R & D may increase the temperature at which the oxide degrades to over 250°C, but it is clear that with these types of devices, the high temperature capability of SiC cannot be fully exploited. The second qualification is that while the SiC device can withstand the higher temperature, nothing else in the semiconductor package can – at least at this time. Higher temperature packaging designs must be developed if the high temperature benefit is to be realized. The final qualification is that, if high temperature is not an absolute requirement for a given application, this capability will have value only where high temperature can be exploited to reduce material and cost.

- ***Much greater ruggedness and reliability.*** This is the natural product of being a wide band-gap material. Qualification: The greater ruggedness will undoubtedly be necessary because the devices will be subject to much greater punishment. With higher voltages and currents, there may be exposure to much higher dv/dt and di/dt. Until these conditions are actually experienced in SiC devices, it is not clear if the devices will be sufficiently rugged without protective measures. In addition, high reliability will require time to realize. The primary failure mechanisms in a mature power semiconductor are delamination of substrates and detachment of wire bonds, both caused by wide and frequent thermal cycling. The use of much higher operating temperatures will only exacerbate the thermal cycling problem and require better matching of coefficients of thermal expansion (CTEs) in the device package.

- ***Positive feedback as to resistance***. This property automatically causes current to be shared well among SiC dies that are paralleled to achieve higher currents. Increases in current cause increases in temperature, which in turn increases resistance and prevents current runaway in any particular die. This property will be extraordinarily important over the next few years, because the ampacity of SiC devices will be inadequate without

the paralleling of dies. As the defect rate in SiC wafers falls, larger die will become available, but the paralleling of die will probably continue, as it has for IGBTs.

- ***High current density.*** The maximum current density for most types of SiC dies is at least 200 A/cm$^2$ and in some types will exceed 300 A/cm$^2$. This is two to three times the maximum current density of silicon devices. This property will eventually tend to reduce cost and offset some of the cost disadvantages of SiC device fabrication.

## 3.2 Readiness of SiC

### *3.2.1 Timeframe*

Currently, SiC devices are not ready to be used in a 1.5 MW converter in the NREL baseline wind turbine. The devices do not have sufficient current capability due to defect levels, and there are no facilities capable of fabricating dies with consistent properties with the high yields necessary to give reasonable cost. In addition, there is insufficient operating experience with any SiC device to ensure reliable operation over a period of years. Finally, appropriate device and inverter packaging is not available. If it were available, it would require long-term testing. These challenges were known at the outset of the project and were confirmed during the project. The important question is whether SiC devices will be ready during the next five years and if designers should begin to consider now how they can exploit SiC devices in large-scale wind turbines.

The author forecasts that in five years practical SiC devices will indeed be available for use in 480 VAC and 690 VAC converters, as well as other applications. Sufficient improvement in defect levels, packaging, and operating experience will be designed into a variety of products. Those products will have special needs in the form of high temperature, high voltage, or high switching speed. The displacement of silicon IGBTs for sheer economic reasons in the major civilian markets (drives, for example) at 480 VAC and 690 VAC will not happen during this five-year planning period. For wind turbines, the higher cost of SiC devices will be partially or completely offset by the dramatic size reduction of an inverter and the increase in energy production. Of greater significance, SiC will enable simple six-device inverters to operate at medium voltage, increasing the voltage in the entire system.

It would appear obvious that developing high voltage devices would be more difficult and require more time than developing low voltage devices. However, with its wide band gap and high breakdown voltage, SiC is ideally suited to high voltage. A number of SiC devices have already been produced in prototype form at over 5,000 V. This has been done to show off this exciting property and to work toward specific applications of interest to funding agencies, such as DARPA and the Navy. One must assume that the availability of high voltage devices will require a couple of years more than the low voltage versions, but there is serious interest that is pushing this along. Based on discussions with potential suppliers, the author believes that a medium voltage, high temperature inverter could be readied for demonstration within five years. It is worth noting that the current requirement of a 4,160 V inverter is only 208 A for a 1.5 MW rating.

### 3.2.2 Suppliers and Prices for SiC Devices

The following is a list of organizations that are capable of fabricating a SiC die (as opposed to device package). The list is by no means complete, but it does show how serious the interest in SiC is. The list is perhaps a little misleading in that some organizations are focused on narrow applications or R&D, while others have broad commercial objectives.

- Cree
- SiCED (subsidiary of Infineon/Siemens)
- Rockwell Scientific (subsidiary of Rockwell Collins/Rockwell Automation)
- GE
- Northrop Grumman
- United Silicon Carbide/Rutgers University
- Linköpings University/TRANSiC (Sweden)
- SemiSouth/Mississippi State University
- NASA (Glen Research Center)
- Toyota/Denso
- Purdue University

Cree supplied the SiC prototypes tested in this project. Cree probably owns the largest body of intellectual property in the field and has the largest professional research staff. Cree is one of the largest manufacturers in the world of high performance light emitting diodes (LEDs), which have undergone a tremendous market upsurge in the last 10 years. Their LEDs are primarily a gallium nitride epitaxy grown on a SiC base, so SiC materials have always been fundamental to their operations. No one in the United States (or probably the world) has received more governmental funding for SiC development than Cree. Cree has raced ahead in a variety of special areas because of funding by the U.S. Department of Defense, including DARPA. By contrast, some other organizations have moved slower, funded only by internally generated funds and motivated only by near-term markets. Cree supplies the SiC substrate crystal upon which many other organizations grow their SiC devices. Cree also sells packaged Schottky diodes and unpackaged Schottky diode dies to others to package and resell.

The cost of prototype SiC devices runs all over the map, depending upon what kind of projects the supplier has underway. They can be inexpensive if the buyer can obtain extra dies out of a batch being run for someone else or extremely expensive if the buyer must pay for an entire batch of wafers with unpredictable yields. No SiC devices, other than perhaps SiC Schottky diodes, are fabricated in a commercial facility. Moreover, many of the developers – both organizations and staff – are new to the field of volume power semiconductor fabrication. Any prices quoted today simply cannot be used as a measure of what SiC devices might cost in the future with the inevitable reduction in defect levels, increase in yields, increase in volume, evolution of technologies, optimization of fabrication processes and all other factors that bear on cost. Any comparisons to silicon, which has evolved over a 40-year period, are simply inappropriate.

### 3.3.3 Defects

Because SiC does not have a liquid phase, the standard technique of controlled solidification of a liquid used to make silicon and other semiconductors can not be used. Instead, a CVD method in which SiC is sublimed onto a seed crystal is used. But this technique leads to misalignment of some SiC molecular layers, introducing lattice defects that interfere with performance and have limited material use. A noteworthy technical report on defects in SiC power devices was written by Dr. Philip G. Neudeck, who leads the SiC development effort at NASA at Glen Research Center in Cleveland, Ohio [3].

The nature of the various types of defects and why they occur are highly complex topics that are well beyond the scope of this report. The major defect categories include the following:

- Micro pipes or hollow core screw dislocations – good progress being made
- Closed core screw dislocations – slow progress being made
- Triangular 3C inclusions – good progress being made
- Carrots & comet tails – good progress being made
- Small growth pits - slow progress being made
- Basal plane dislocations – good progress being made
- Threading edge dislocations – slow progress being made.

Several of the defect types cannot be allowed to be present in the device at all. They compromise greatly the breakdown voltage of the device and defeat its basic purpose. Other defect types might be allowed; experiments have not yet shown whether they are prohibitive either on a short-term basis or after considerable usage.

Fundamentally, device yield and current capability of a single die are functions of the level of defects (e.g., micro pipes) in the wafer. Many of the defects start first in the seed substrate and replicate as new epitaxial crystal grows. In fact, the growth technique being used today for some types of devices requires the presence of defects. With a current density of 150 $A/cm^2$, a yield of 87% (commercially attractive) 20 A-rated device is expected when the micropipe density is less than $1/cm^2$. Additionally, if SiC devices operate at higher current densities, yield improvements can also be observed. For example, a yield of 95% for a 20 A device operating at 350 $A/cm^2$ can be expected for the same defect density of $1/cm^2$. To achieve high device yield, a recent program funded by DARPA demonstrated SiC substrates with micropipe densities reduced to $0.2/cm^2$. Note that other prohibitive (fatal) types of defects must also be reduced. Because of this recent work, commercial “high quality”3-inch, n-type 4H-SiC wafers are being produced, albeit at a higher per unit cost than silicon. Currently, the defect density is such that the available die area gives a maximum ampacity of about 100 A for Schottky diodes and 20 A for transistors.

Due to their current expense, SiC devices will first enter the market for use in high value applications where their superior performance is demanded [3].

Voltage level is a matter of thickness and is affected by the defect level of the underlying seed substrate. High voltages can be achieved in prototype dies, even though ampacity is still severely limited by the defect concentration. Most types of SiC die can be readily paralleled to

achieve higher ratings because of their positive temperature/resistance feedback characteristic, but cost will still be greatly impacted by poor yields and undeveloped processes.

In August 2004, Toyota Central R&D Laboratories, Inc., Japan Research Laboratories, and DENSO Corporation published a technical paper about a breakthrough in the production of defect-free SiC. The complete methodology is commercially sensitive and is not shared in the field at this time. The full implications of this work are not yet known, but it is heartening to see breakthroughs in defect density, as it is perhaps the major obstacle today in SiC. It would appear that this consortium of Japanese companies is targeting electric and hybrid vehicles.

### *3.3.4 Signal Level Uses of SiC*

This project focuses on high power electronics, not signal level electronics. In studying SiC, however, the question arises as to how SiC would fare in signal level circuits or integrated circuits (ICs). SiC would be inferior. SiC would lead to slower logic and larger circuits, even in maturity. It has at least one fundamental deficiency in this role relative to silicon; lower electron mobility. The future of SiC is in power devices.

An exception to this conclusion is high temperature applications. Where logic and other control circuits are required in an extreme environment, SiC could again be a candidate, assuming any compromises in speed and size are offset by the temperature requirement. Silicon logic elements using silicon-on-insulator (SOI) techniques should, in time, achieve 300ºC.

# 4.0 SIC DEVICES AND CHARACTERISTICS

This chapter will summarize the characteristics of devices and multiple device configurations. No attempt will be made to explain the basic construction of devices or how they operate, rather various devices will be discussed to the extent necessary to compare and contrast general performance characteristics of each when using both silicon and SiC. Numerous sources are available at all levels of sophistication on the construction and operation of power semiconductors. Chapter 20 of *Power Electronics*, by Mohan [4], is a good starting point.

The point of comparison for most devices will be the silicon IGBT along with the silicon PN junction diode that is normally included in the same package as the free-wheeling or reverse diode. This type of device package is used throughout the world in nearly all 200 to 1000 VAC converters, including the converters used in wind turbines.

## 4.1 Device Comparisons

### *4.1.1 Introduction*

The world of semiconductors is highly evolved and complex; it is so broad that no one person can say that he or she is an expert in all pertinent disciplines. Collecting information and attempting to translate it into useful conclusions required much more time than expected. Good summary tables were not available. Virtually all written or oral information focused on a small part of the picture, so it was difficult to gain perspective and determine what is important.

Many of the well-known types of power semiconductors have been constructed with SiC. However, few of these devices could be classified as mature or well optimized. With the exception of SiC Schottky diodes, they are prototypes and often raise questions about whether their deficiencies are fundamental or just the result of being early stage versions. For this report to have maximum value, the devices must be evaluated not only with respect to their current demonstrable characteristics but also with respect to their predicted characteristics at maturity.

The prospective virtues of SiC in power semiconductors were covered earlier. In this section, two basic tables are presented. Like all summary tables, many of the entries must be qualified. The tables should not be considered without the qualifying remarks in the accompanying discussion. Across the top of both tables can be found most of the commonly used power semiconductors; down the left side are the most important parameters or characteristics to the converter designer. Performance numbers have been inserted where possible. Where it has not been possible to use numbers, more subjective ratings are given on a five point scale using the following five symbols: ++, +, o, -, --. Power semiconductor experts use a variety of other figures of merit too, but they are simply too esoteric for this report. They tend to describe the fundamental science and are often theoretical limits, rather than indicators about how a power semiconductor might actually operate now or during the next five years.

Finally, the subject of how to grade devices may be subjective. Generally, the selection of a power semiconductor is dominated by the application, so a reader might not believe a grade is correct for his particular application. The application assumed by the author in this report is

always the converter for a large wind turbine that operates at 690 V. Table 2, which covers silicon devices, focuses on standard, commercially available devices with standard doping, not specialty devices for unusual applications. Table 3, which covers SiC devices, focuses primarily on the polytype known as 4H-SiC, the most common in power semiconductors. These tables should not imply that all of the characteristics of SiC devices have been achieved, but that SiC devices with these characteristics should be feasible during the next five years.

**Table 2. Power Semiconductor Characteristics - Silicon Versions**

| Device Characteristic | PN Junction Diode | Schottky Diode | Power BJT | JFET Normally On | JFET Normally Off | MOSFET | IGBT Slow | IGBT Fast | SCR | GTO | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| On State Voltage (1,200 volt device) | 1.5 | NA at voltage | 2 | NA at voltage | NA | NA at voltage | 2 | 4 | 1.5 | 2 | Volts |
| Conduction Loss | ++ | NA at voltage | + | NA at voltage | NA | NA at voltage | + | o | + | + | See discussion |
| Switching Speed | o | NA at voltage | - | NA at voltage | NA | NA at voltage | o | + | -- | - | See discussion |
| Switching Loss | o | NA at voltage | - | NA at voltage | NA | NA at voltage | - | o | - | - | See discussion |
| Voltage Maximum | >5,000 | 300 | >3,000 | 300 | NA | 500 | 6,500 | 3,000 | >10,000 | >5,000 | Volts |
| Current Maximum | >5,000 | 100 | >500 | >20 | NA | 200 | 2400 | 800 | >10,000 | >3,000 | Amps |
| Operating Temperature | 125 | 175 | 125 | 125 | NA | 125 | 125 | 125 | 125 | 125 | Degrees C |
| Gate Drive Circuit Difficulty | None | None | -- | + | NA | + | + | + | - | -- | See discussion |
| Likely Commercial Introduction | Done | NA at voltage | Obsolete | NA at voltage | Not likely | NA at voltage | Done | Done | Done | Done | Years |
| Fabrication Cost | ++ | NA at voltage | o | o | NA | ++ | + | o | ++ | - | See discussion |

**Table 3. Power Semiconductor Characteristics - SiC Versions**

| Device Characteristic | PN Junction Diodes | Schottky Diodes | Power BJT | JFET Normally On | JFET Normally Off | MOSFET | IGBT Slow | IGBT Fast | SCR | GTO | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| On State Voltage (1,200 volt device) | o | - | + | o | - | - | NA | + | NA | NA | Volts |
| Conduction Loss | o | - | + | o | - | - | NA | + | NA | NA | See discussion |
| Switching Speed | + | ++ | o | + | + | ++ | NA | + | NA | NA | See discussion |
| Switching Loss | + | ++ | o | + | + | ++ | NA | + | NA | NA | See discussion |
| Voltage Maximum (Potential) | >10,000 | 10,000 | >10,000 | 10,000 | 10,000 | 10,000 | NA | >>10,000 | NA | NA | Volts |
| Current Maximum (Potential) | >1,000 | >100 | >>100 | >100 | <50 | >100 | NA | >500 | NA | NA | Amps |
| Operating Temperature (Potential) | >400 | 250 | >400 | >400 | >400 | 250 | NA | >400 | NA | NA | Degrees C |
| Gate Drive Circuit Difficulty | None | None | -- | o | o | + | NA | + | NA | NA | See discussion |
| Initial Commercial Introduction | 3 | Done | 3 | Done | 1 | 1.5 | See fast IGBT | 5 | Not likely | Not likely | Years |
| Fabrication Cost (Potential) | + | o | o | + | - | o | NA | o | NA | NA | See discussion |

### *4.1.2 Device Characteristics*

***PN Junction Diodes.*** Diodes are the simplest of all useful power semiconductors and represent a one-way valve without any active turn-on or turn-off mechanism. Diodes are commonly used in the front-end rectification bridges of, for example, a motor drive that is powered by an AC source. When used as free wheeling diodes, they are placed anti-parallel to power transistors to protect them from excessive reverse voltage that would otherwise occur routinely during the switching cycle in typical PWM applications. They are so important for this purpose that essentially every commercial power transistor package contains a reverse diode. The most commonly used type of silicon diode for this purpose today is the PN junction type.

Diodes are a source of not only conduction losses, but also turn-on and turn-off losses when the applied voltage reverses, as it does in any typical PWM application. The source of the conduction loss is obviously the electrical resistance along the current path from the input to the output. Due to its simplicity, the resistance of a diode tends to be lower than for an active device.

Switching the reverse diode often contributes significantly to the overall power losses in a converter, particularly at low power. Reverse recovery losses caused by the reverse diodes can be as much as 50% of the overall switching losses in an inverter bridge, including the switching losses in the accompanying transistors. When the voltage reverses on the diode during the switching cycle, a large fraction of the charge stored in the device is swept out in the reverse direction as the so-called reverse recovery current. The reverse recovery current does not combine with the current that flows to the load, but rather is lost as heat in both the diodes and the transistors. The amount of charge stored in the diode is more a function of the voltage imposed on the device than the power (current) level that was being conducted prior to turn-off. Therefore, the losses do not fall off proportionally to power level, but contribute a higher fraction of the overall converter losses as power is decreased, a circumstance important to wind turbines that operate most of the time well below their design rating.

In a 480 V system, the forward voltage drop (a direct measure of the conduction loss) in a silicon PN diode can be as low as 1.4 V, compared to the voltage drop in the accompanying IGBT of 2% to 4%, depending upon whether the IGBT was doped to minimize conduction or switching losses. The conduction loss is often not important in the reverse diode because it may not conduct much of the current, which flows primarily through the transistor. In a typical drive inverter, the reverse diode will be subject to a switching frequency of 5 to 10 kHz. The converter of the 1.5 MW baseline wind turbine, which operates nominally at 690 V, has a PWM switching frequency of 3 kHz. The switching characteristics and reverse recovery current of the reverse diode are generally more important here. By contrast, in a passive rectification bridge made up of only diodes, all of the current is conducted through the diodes and the switching frequency is that of the input AC (often the grid measures only 50 Hz or 60 Hz). The frequency might be several times that (still relatively low) if a variable-speed wind turbine generator is the source. If the input is a high-speed generator on a gas turbine, the AC frequency might be as much as 2,000 Hz. In this scenario, the switching characteristics have more importance, but the conduction loss will still probably be most important in the diodes with passive rectification.

There are circumstances when another entire inverter is inserted in reverse – so-called back-to-back inverters - as an active input rectification stage of a converter. These circumstances include the need to provide high power quality on the input lines, to give the converter bi-directional capability, to give voltage step-up capability or to allow precise control of the generator (imposition of field orientation control). Here the reverse diodes assist in the rectification function, but they also act as the reverse diodes in protecting of the transistor during high speed switching in the same way as in the output inverter of the converter. Because the PWM switching speed of the input inverter might be similar to the output inverter, the switching component of the losses in the input inverter is much higher, giving importance again to the switching characteristic. The converter for the baseline NREL wind turbine uses an input

inverter, but there are alternative electrical configurations for wind turbines where that is not necessary. In this project, it assumed that an input inverter is used.

Silicon PN junction diodes are rugged, inexpensive, and available at high ratings–up to several kV and kiloamps. They can be placed in series to achieve higher voltages and placed in parallel to achieve higher currents. However, they are limited to 125°C like other silicon devices.

The SiC version of the PN junction diode should eventually offer improvements; the switching speed should be about ten times that of the silicon version and the forward losses should be somewhat better. In addition, they will be able to operate at much higher voltage (over 20 kV) and much higher temperature. However, to date they have had technical difficulties. When prototypes have been operated, the properties of some of them have deteriorated over time. The reason for this is not yet totally understood, but it appears that the problem is being addressed. For this reason, all SiC diodes in the current market are the Schottky barrier type.

Even after this technical problem is solved, the SiC PN junction diode may not be greatly superior to its silicon counterpart in all applications. At 480 V or 690 V and below, it may not have a sufficiently low conduction loss to justify its use in a passive rectification bridge. The trade--off between the advantages and disadvantages, including cost, will have to be considered carefully in view of the application. In a DARPA project, SiC PN diodes were demonstrated with reverse blocking capability of over 9,000 V and a forward voltage drop of only 4.2 V. The high voltage, high temperature, and high switching capability will definitely give this device a place in the market.

***Schottky Barrier Diodes.*** The Schottky diode is formed by depositing a thin film of metal in direct contact with a semiconductor, usually on an n-type semiconductor. The forward conduction loss tends to be lower in the Schottky, compared to the PN junction diode, and it is generally used in very low-voltage circuits where the low-voltage drop (typically 0.3 V) is important. The Schottky leakage current in the reverse direction is somewhat larger than for the PN junction diode but this does not have great significance in some applications. The Schottky turns on and off faster than a comparable PN junction diode. The silicon Schottky diode is limited to approximately 200 V, so the silicon version is simply not a candidate for a large wind turbine.

With SiC, the blocking voltage and power level is dramatically increased, as it is for other types of devices. SiC Schottkys are now commercially available at 1,200 V and 75 A. These limits will increase significantly in the next several years. Prototypes have been made (Rutgers University) at over 10,000 V. The greatest benefit with a SiC Schottky is that its reverse recovery current is virtually eliminated, lowering switching losses when used as a reverse diode. Experiments have shown the reduction in switching losses to be as high as 50% in a 230 V, 1 hp drive switching at 10 kHz [5]. The benefits are sufficiently great that at least two power semiconductor suppliers are now developing IGBT packages that contain a silicon transistor with a reverse SiC Schottky diode for high-speed switching applications.

The other primary application of diodes, the passive input rectification bridge for a DC link converter fed by AC, does not benefit similarly from the use of SiC. As noted above, the diodes

carry all of the current and the switching frequency is low, so the conduction loss is more important. Some tests show the conduction loss is actually increased with the SiC Schottky. There would appear to be little reason to use any type of SiC diode in a passive input rectification bridge in the 480 V or 690 V area or below, unless high temperature or high frequency were involved. It is expected that the SiC PN junction diode will have lower conduction losses than the SiC Schottky above 2 or 3 kV, but higher conduction losses below this level. Therefore, the SiC PN junction diode might have application in wind turbines operating at 4,160 V.

All of the SiC diodes being sold today are of the Schottky barrier type. Testing results indicate superior switching characteristics, although they are expensive. Today several companies (Cree, Infineon, Semisouth, and Rockwell Scientific) fabricate SiC Schottky diode dies and mount them in commercial packages for sale. Other companies as well mount them in commercial packages for sale.

***Bipolar Junction Transistors (BJTs).*** The silicon BJT is an older type of device whose active use faded out over 10 years ago. It has been replaced in essentially all applications by the improved version called an IGBT, which now has much higher voltage and amperage capability than the BJT ever had. The primary deficiencies of the BJT are its need for current gating and slow switching speed. Both problems were reduced greatly in the IGBT, which requires only a voltage gate signal. The designer always prefers voltage gating because the gate circuit will be smaller and it can provide more consistent, higher speed gating. Because of the need for current gating, an important figure of merit with the BJT is the "gain," the ratio of the current being controlled by the device to the gate current. A gain of less than 10 would be unacceptable and a gain of over 40 would be acceptable, with gains in between entailing some degree of pain from the designer's point of view. The low conduction loss (only one or two V of forward drop) in the silicon BJT is its sterling advantage.

BJTs are available up to 1500 V and several hundred amps. They have a negative temperature coefficient of on-state resistance and are more difficult to parallel to achieve higher current ratings. With careful design this can be achieved.

A Darlington device is basically two BJTs stacked on top of each other, one being used as the gate for the second. The net effect is that the gain is equal to the two gains in the two BJTs multiplied times each other, thereby minimizing the gate drive circuit problem, but it also significantly increases the forward conduction loss, making the device quite inefficient in many applications. Darlingtons have also faded from the scene with the advent of the IGBT.

The use of SiC in BJTs leads to certain beneficial changes. The operating voltage and switching speed are increased greatly. The deficiency in the gate drive circuit remains, so recent SiC prototypes have strived to increase the gain. Gains of less than five were experienced initially, but are now over 30 in some versions. A case has been reported at 400. A Darlington has been reported to have a gain in excess of 1,000. The SiC BJT has no oxide layer and can operate at higher temperatures than the SiC MOSFET. Both the BJT and Darlington may again in time be replaced by the IGBT, even when constructed of SiC.

***Junction Field Effect Transistors (JFETs) – Normally-On.*** The practical application of the silicon JFET in the future can be debated. According to one source (Fairchild), the silicon JFET is not a significant commercial product because it is normally on and raises protection issues, is difficult to manufacture, and requires a high gate voltage. It is strictly a low power device and the popular MOSFET can serve in virtually every application where the JFET might be considered. Relative to the MOSFET, the JFET has somewhat lower forward conduction losses and somewhat higher switching losses, although this is relative as it still has excellent switching characteristics (better than the IGBT).

Nearly every organization that has fabricated SiC devices has fabricated JFETs of some form because they are on the path to more difficult and desirable types of SiC devices. Several organizations have designed and demonstrated inverters for controlling motors using JFETs (Siemens and Rockwell Scientific). With SiC, the potential power rating is increased greatly for this type of device; however, the potential voltage rating is increased similarly for its competitor, the SiC MOSFET, which is normally-off and has superb switching characteristics.

JFETs may have the lowest overall losses of the SiC devices. Another standout advantage of the SiC JFET is that it can operate at temperatures over 400ºC. In comparison, the oxide layer of the MOSFET will degrade at temperatures far below this. The temperature limit for the MOSFET will be increased substantially in the future, but the oxide layer in the SiC MOSFET will remain a fundamental deficiency relative to other devices.

In spite of their availability and favorable performance characteristics, SiC JFETs have been rejected by many designers because they are normally-on. That is, in a converter, the gate drive circuits would have to be energized and working correctly to prevent any current from flowing through the device most of the time. This process is reversed in most commercial power switches sold in the world today, where the device is off (non-conducting) until the gate driver turns it on. The normally-on characteristic definitely is controversial, but it should not eliminate the device from consideration. The specific technical problems created by this characteristic should be addressed with an open mind. For some applications, the normally-on feature probably is not a practical concern, given the normal startup sequence of a complex electronics system and a typical firing strategy during operation. For other applications, it might be prohibitive. The designers of motor drives, the largest market in the world for power electronics, have been reluctant to embrace the JFET because their products are subject to the greatest cost challenges and the solutions for the normally-on problem would add to the cost. In addition, the use of a normally-on device would require a change in mindset and design techniques, which will require time. Several organizations (e.g., Siemens and SemiSouth) have given considerable thought to how the normally-on characteristic can be dealt with both in the gate drive circuit and system operating control. Since the MOSFET is normally-off, all of the standard techniques for system startup, protection, and diagnostics can be used. The MOSFET may displace the JFET on these grounds, too.

***Junction Field Effect Transistors (JFETs) – Normally-Off.*** It is possible to modify the SiC JFET concept to give it a normally-off characteristic. However, this leads to certain compromises with respect to current capability and forward resistance, and may give rise to a very narrow fabrication window with difficult tolerances. Therefore, the normally-off SiC JFET would

appear to be even less likely to become a viable long-term candidate in practical power electronics, although it is available today in prototype form.

***Metal Oxide Semiconductor Field Excited Transistor (MOSFET).*** The silicon MOSFET is considered to be a low power device because of its low voltage and current limits. However, its switching characteristics are extraordinary and switching frequencies over 100 KHz are found in commercial products. While switching losses are very low, conduction losses are relatively high (compared to the IGBT), depending upon how the MOSFET is applied. The forward conduction loss mechanism in a MOSFET is different than in an IGBT. The dominant contribution to the on-state loss in the IGBT tends to be fixed, that is, not a function of current, whereas in the MOSFET, and most other types of devices, the on-state loss is proportional to current. Therefore, the forward voltage drop with the MOSFET can be reduced by providing more device area to limit the current density. Some low-voltage products (inverters for small photovoltaic systems) use up to 30 MOSFETs in parallel to reduce current density thereby reducing the voltage drop to an acceptable level when operating in a 12 V system. Paralleling devices in this way might be impractical in high power situations, even if the voltage capability of the device would permit its use there.

All things considered, the MOSFET is one of the most promising devices in the SiC field; more money has been invested in its development than any other type of SiC device. When made of SiC, it is normally-off and its rating can be increased to over 10,000 V. It definitely becomes a high power device and it makes higher frequency switching at high power possible.

At this early stage, the forward loss of the SiC MOSFET is not very impressive at 480 V or 690 V, but the low switching loss characteristic is preserved in the SiC version. See reference [6] on the forward voltage drop in a DC-DC (270VDC/500VDC) power converter with 600 V MOSFETs–both silicon and SiC. The primary contributions to $R_{ds\text{-}on}$ in the 600 V SiC MOSFET are the channel (37%) and JFET (31%) components, as opposed to the dominance of the drift layer (80%) in the 600 V silicon MOSFET. This reference also reports that improvements are being made in this area. It is likely that devices designed and used for applications above several thousand V would have more acceptable conduction losses because conduction losses become relatively smaller as voltage is increased with any power device.

As noted earlier, one of the major weaknesses of the SiC MOSFET is the oxide layer, which is susceptible to breakdown with temperature. Peregrine's work in the project to develop packaging for reliable operation at 300°C can not be exploited with the SiC MOSFET for some time, if ever. Of the three major benefits from SiC devices: 1) high voltage, 2) high temperature, and 3) high switching speed, only high temperature is limited for the MOSFET, leaving high voltage (high power) and high switching speed as standout qualities.

With either silicon or SiC, MOSFETs use a simple, inexpensive gate drive circuit that applies a low-voltage signal. While the prototype devices supplied by Cree required widely varying gate voltages, one should expect production versions to have more uniformity, permitting identical gate circuits to be used. No practical problems in the gate area are expected.

***Insulated Gate Bipolar Transistors (IGBTs).*** The silicon IGBT is the most widely used power semiconductor in power electronics in the 200 to 2,000 VAC range, which encompasses most industrial power electronics products and the converters for wind turbines. The IGBT can be considered a BJT combined with the highly superior gate approach of a MOSFET. It has relatively low forward conduction losses and better switching characteristics than the BJT, but still not as good as the MOSFET. Due to its popularity, the IGBT must be the object of comparison in this report for all devices in terms of performance and cost. Since their introduction about 15 years ago, ratings have increased steadily; products are now offered at 4,500 V and 1,600 A. One supplier advertises a version at 6,500 V and 2,400 A. IGBT dies are routinely paralleled in a single package to achieve high current, so there is essentially no current limit on an IGBT package.

With the IGBT, the device designer can trade off conduction and switching losses by the level and type of doping. Some IGBT packages are considered "slow" while others are considered "fast". In the 480-V environment, the forward conduction drop will vary from less than 2 to 4 V with the higher end associated with the lowest switching losses. Switching losses are substantially higher than in the MOSFET, but at 5 to 10 kHz, where most products fall, the losses are acceptable. In this frequency range, the conduction losses and switching losses are comparable in magnitude. Total losses, for example, in a 480-V, three-phase inverter bridge switching at 5 kHz, will fall in the 1.5% to 2.0% range, split equally between conduction and switching. Operation at significantly higher switching rates is possible with de-rating and at least two suppliers advertise IGBT modules designed for 30 kHz switching speed. Obviously, these have been doped for low loss switching, but have compromised forward voltage drop (over 5 V).

The SiC versions of the IGBT offer exciting possibilities. The voltage can be boosted to well over 20,000 V and IGBTs can be stacked to withstand virtually any voltage. Observers say that over 40 kV will be achievable. They should have the lowest forward losses of all of the SiC devices being developed and should have over 20 times lower switching losses compared to the silicon counterpart. With the SiC IGBT, some observers believe it will be possible to use conventional, hard-switching designs, without multi-levels or cascaded modules, in applications from medium voltage (1,000 to 4,160 V) up to over 13,800 V. Major power plants typically generate at 13,800 V and utilities often distribute power at 12,500 V. SiC IGBTs are expected to have lower forward conduction losses than the silicon version, and at higher voltage these losses will be even lower. The Navy is now considering the development of core power distribution (substation) equipment using SiC IGBTs for large military ships that generate at 13,800 V. Cree is one of the developers of the prototype SiC IGBTs. The medium- and high-voltage world may be opened up to an entire array of new power electronics products.

The IGBT has an oxide layer in its gating system, as does the MOSFET. Due to differences in its configuration, however, it is not yet clear how this will affect the maximum operating temperature of the device at maturity. It will probably impose a lower limit, but perhaps not as low as for the MOSFET.

However, the availability of commercial, high-voltage SiC IGBTs is not close at hand. Commercial introduction will require at least five and perhaps ten more years. They are not being considered seriously in this project due to lack of readiness within a five-year timeframe.

Virtually all experts agree that the SiC MOSFET will be commercially available up to 10,000 V substantially before the SiC IGBT.

***Other Devices.*** The thyristor (SCR) is the oldest of the active devices, and is rugged and inexpensive. It has served high power applications for several decades and has the lowest forward conduction losses of any active device. Silicon thyristors are already capable of withstanding over 10,000 V; strings of thyristors are used in the highest voltage systems (over 700 kV in DC transmission lines). Main weaknesses are slow speed and the inability to control turn off, which is done by natural commutation at a zero crossing. Temperature limit is that for all silicon devices-125ºC to 150º C. When packaged as “hockey pucks,” they can be cooled on both sides, improving thermal management potential.

Gate turn-off thyristors (GTOs) were the early answer to the turn-off problem of the thyristor. The GTO still has several weaknesses, including slow switching speed and the need for a gate drive circuit with a current rating of about 20% of the current being turned off. GTOs have been displaced one-for-one by IGBTs as the power capability of IGBTs has increased.

Although early stage prototypes of SiC thyristors and certain other devices have been fabricated, they are not believed to have any future importance in the time prospective of this project. SiC may eventually infiltrate the high-voltage world, but probably not in the form of thyristors, GTOs, or IGCTs. Rather the form will be the SiC MOSFET and SiC IGBT, because they will also have the high voltage capability and are superior in every other way.

***Composite Or Hybrid Device Configurations.*** At least two composite or hybrid configurations using SiC devices are available. The first hybrid configuration is comprised of a standard silicon transistor (e.g., IGBT) with a SiC Schottky as the reverse diode. This was described earlier as an advantageous use of a SiC Schottky diode, which has much lower reverse recovery current than its silicon counterpart. Other things being equal, this is expected to decrease switching losses by 30% to 50% in typical applications. If the switching losses are half of the total, the net impact is a 15% to 25% reduction in total losses, a significant amount. This configuration is of special interest in high switching applications.

This is one technique for exploiting SiC in the very near future. This configuration has sufficient promise in the market that several suppliers are now developing semiconductor packages with silicon IGBTs and SiC Schottky diodes. The SiC Schottky is still quite expensive and the overall package will still be limited in temperature by the silicon transistor. This approach has been considered in this report and appropriate converter efficiency calculations are presented later.

The second hybrid configuration, offered by Infineon (or SiCED, its subsidiary), deals with the unfavorable normally-on characteristic of the JFET. Here a silicon MOSFET is put in series with a normally-on SiC JFET in a cascode configuration. Multiple SiC JFETs can even be lined up in a string to achieve high voltage levels, using only the one silicon MOSFET [7]. The string of devices is normally-off due to the presence of the silicon MOSFET. The silicon MOSFET can be rated at relatively low voltage, because most of the voltage on the string can be made to be borne by the SiC JFETs. SiCED reports that a SiC JFET and silicon MOSFET, plus the appropriate gate drive circuits, can be integrated into a single package that is outwardly simple; it

has no more leads or terminals than a single device. The argument is that the designer should not care what is inside, because it can be used just like a single, conventional, normally-off device. This more complicated hybrid obviously does not have the extensive operating history of other common devices, so reliability is unknown. Performance and ruggedness have probably been compromised to some extent relative to a full SiC package due to its internal complexity, and the temperature is still limited by the silicon MOSFET. The cascode is obviously a stop-gap configuration to be used until a full normally-off SiC alternative is available.

## 4.2 Experimental and Modeling Work

### *4.2.1 Testing and Modeling at University of Tennessee*

Cree, one of the foremost developers of SiC devices in the world, supplied four prototype SiC MOSFETs for this project. They enabled the team to characterize real SiC devices and then to develop an accurate model of the devices that could be applied to a converter for a wind turbine. The characterization and modeling work was carried out under contract with the University of Tennessee (UTenn), which in turn carried out some of the work at nearby Oak Ridge National Laboratory. The work was carried out under the supervision of Dr. Leon M. Tolbert, who is employed by both institutions. Peregrine had several alternatives for carrying out this work, but because Dr. Tolbert's team had considerable experience in the testing, modeling, and application of SiC devices, the principal investigator believed this alternative would lead to better results with less capital investment. In addition, the team would develop relationships that would give access to other data and experts to assure consistency with other work.

The work carried out by Dr. Tolbert and his associates fits into a larger program at UTenn and will continue into the future. The four documents in the appendix contain their work. Because of the complexity of some of the UTenn methodologies, particularly the device modeling, the reports will not be described here.

Short of actually building a full-scale wind turbine and converter, modeling to some degree is necessary. The mechanisms in a solid-state device that impact steady state and dynamic performance are reasonably well known and can be represented with equations. These equations describe the physics but are still completely abstract until factual information for the exact semiconductors in question are inserted. The factual information was collected through actual testing when possible. When test information was not available, more basic physical properties were used. Measured characteristics, not theoretical promises, dominated the results.

Once a realistic model has been developed, it can be applied to the devices in a converter that experiences specific voltage and current conditions. Tables of these voltages and currents for each power level for the bidirectional converter used in the baseline wind turbine were provided by the authors of the drive train report [1]. The tables were used by UTenn to arrive at loss information at each power level. With the loss information as a function of power level, Peregrine was then able to create a new set of efficiency and energy production spreadsheets that incorporate the baseline wind distribution.

The prototypes are certainly not yet commercial devices. Their characteristics are not uniform among the samples and the gate drive requirements were quite different. The prototypes would not be acceptable in a commercial application where identical drive circuits would be necessary and the losses must be predicted accurately. But the necessary uniformity will be achieved as more prototypes are produced and the processes are optimized. In addition, improvements in performance can be expected.

### *4.2.2 Assumptions*

The SiC MOSFET was selected in this project for several reasons. The first is the practical one of availability. Prototype BJTs and JFETs are probably also available in SiC, but the SiC MOSFET was generously offered by Cree. Second, the Cree SiC MOSFET is probably more advanced than the other SiC devices and it was provided in a standard, usable package (T0247). Third, Cree intends to introduce the SiC MOSFET in the near future because it has many desirable features: excellent switching characteristics, the normally-off property and high voltage (up to 10,000 volts) capability. Thus, it really represents a likely commercial SiC power semiconductor that could be used in the converter of wind turbines.

The baseline converter topology studied in this project is shown in Figure 1. This is a standard inverter configuration that has been used routinely in wind turbines. It has back-to-back inverter bridges, each with 6 silicon IGBTs and 6 reverse or free wheeling diodes of the silicon PN junction type. The SiC version is assumed to use SiC MOSFETs provided by Cree along with SiC Schottky reverse diodes. Although Peregrine did not supply SiC

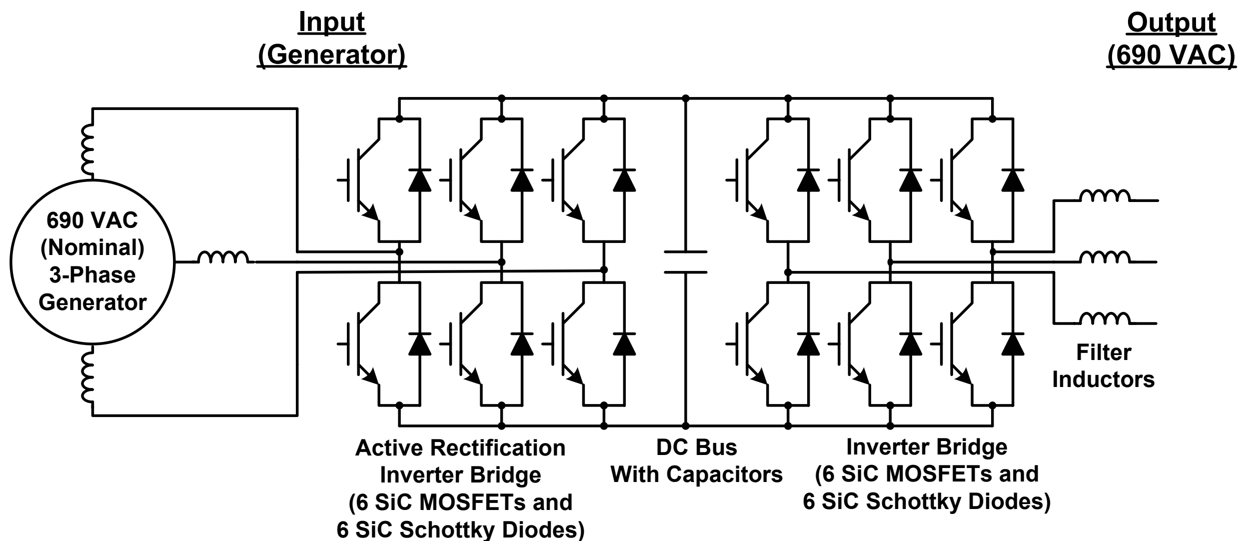



**Figure 1. SiC-based converter for baseline wind turbine**

Schottky diodes to UTenn for testing and modeling, experimental data was available for them because that work had already been carried out by UTenn.

The modeling work required assumptions about how the converter would be modularized. The 1.5-MW converter was assumed to be comprised of 10 SiC-based converters rated at 150 kW

each, while the baseline converter in the drive train report was comprised of two converters of 750 kW each. Whether this is practical or not for SiC can be debated, but performance results were not impacted. A fully rated inverter bridge with single SiC dies would be impossible to design today due to severe current limitations caused by defect levels. Multiple dies must be paralleled. The designer can parallel the devices at the die level, at the semiconductor package level, or at the inverter level. Electrically, the dies are operated in parallel no matter how this is done. SiC MOSFETs dies parallel well due to their excellent resistance/temperature feedback characteristic, so there is no reason to expect performance to differ fundamentally for different inverter module ratings. Ultimately, the selection of module rating would involve a tradeoff study involving many factors, including the materials and fabrication processes involved in a new high temperature semiconductor package discussed later. In any event, each die is assumed to handle the full voltage and its share of the total current, as specified in the spreadsheets for the converter in the baseline wind turbine.

In the modeling, the switching frequency was assumed to be 3 kHz for the silicon devices and 50 kHz for the SiC MOSFETs. Little or no penalty in the form of losses was expected (incorrectly) for the increase in frequency when using the SiC MOSFETs because the MOSFET is a remarkably fast device that often uses frequencies in the area of 50 kHz. This frequency was intended to minimize the size of filter elements.

In its reports, UTenn compared the performance of 1.5-MW converters using both silicon MOSFETs and SiC based MOSFETs. This comparison is not pertinent here because the baseline wind turbine uses silicon IGBTs rather than silicon MOSFETs. There are internal programmatic reasons at UTenn why this comparison was made, but their work does include the desired data for the SiC MOSFETs, which Peregrine was then able to compare separately to the baseline converter with silicon IGBTs.

### 4.2.3 Basic Performance Results and Interpretations

***Efficiency Calculations.*** The appropriate performance data has been excerpted by Peregrine from the UTenn spreadsheets and reformatted as Table 4. Then the data were modified appropriately and compared to the baseline data silicon-based converter described in the Drive Train Report. Comparisons are recorded in Table 5 through 10. Table 5 is a baseline table from the Drive Train Report that has been modified in two respects: 1) it has been updated to improve the computation of the losses in the filter inductor based on more recent work by Dr. William Erdman, and 2) the baseline energy production profile has been added to assist in computing a weighted average efficiency. This average represents the best figure of merit for comparison of different converter approaches.

Data in Tables 6 through 9 can be interpreted in the following ways. The SiC MOSFET and SiC diode losses, as shown for each wind speed for each inverter, were summed and multiplied times six. Added to this value was the fixed inverter loss of 150 W (explained below) to get the total losses for an inverter. Then, the result was multiplied by 10 to get the losses for all of the10 paralleled inverter modules totaling 1.5 MW. This computation is carried out for both the generator and grid inverters. Those are added together, along with the filter loss, to get the total converter loss for each wind speed.

***Interpretation and Analysis.*** The average efficiencies (including filter inductor losses) from these tables are as follows:

| | | |
|---|---|---|
| Table 5. | Baseline, silicon IGBTs/silicon diodes, 3 kHz | 95.5% |
| Table 6. | SiC MOSFETs/SiC Schottky diodes, 50 kHz | 94.9% |
| Table 7. | SiC MOSFETs/SiC Schottky diodes, 9 kHz | 97.0% |
| Table 8. | SiC MOSFETs/SiC Schottky diodes, 3 kHz | 97.3% |
| Table 9. | SiC MOSFETs/SiC Schottky diodes, 3 kHz, ½ conduction loss | 97.9% |
| Table 10. | Silicon IGBTs/SiC Schottky diodes, 3 kHz | 95.9% |

In all of these tables, the inverter bridges are assumed to have a fixed loss due to fans (the largest share), power supplies, circuit boards, etc. For the silicon bridges, the fixed loss is assumed to be 3 kW per bridge, and because there are two input bridges and two output bridges, the total fixed loss is 12 kW. For the SiC bridges, the fixed loss is assumed to be 25% of total fixed loss or 3 kW. Justification of these results will become more apparent later as the device packaging portions of the project are discussed. In brief, when the greater efficiency is combined with higher temperature packaging, the heat sink size and fan power is reduced by roughly a factor of 6 and only single input and output bridges are necessary. A 1.5 MW inverter can be designed with only 6 devices (each containing paralleled dies) that require only 6 gate drives and 1 set of control boards. When the 3-kW loss was spread over the 20 inverter bridges (input and output inverters for each of the ten 150-kW converter modules), each inverter bridge experienced a 150-W loss. The reduction in fixed losses was important, particularly at low power where they represented a larger fraction of the total losses.

Table 6 shows an efficiency of 94.9% with SiC; less than the baseline with silicon. This reflects the losses associated with 50 kHz switching. From the basic data generated by UTenn, the use of SiC MOSFETs appears to have doubled the switching losses. A poor strategy for the use of SiC devices was clearly selected by Peregrine and given to UTenn for its modeling. With the belief that little penalty would be paid in the form of losses for increasing the switching frequency when using a MOSFET type of switch, 50 kHz was arbitrarily selected. This would, of course, make a dramatic reduction in the size of the filter, one of the goals. However, the switching losses were found to be non-trivial. They are in fact much lower with SiC, but 50 kHz is too high and overshadows this fact. Since switching losses are directly proportional to switching frequency, they can be readily reduced by a factor of roughly 17 if 3 kHz is used, as it was for the evaluation of silicon IGBTs. Tables 7 and 8 show the same data with the switching frequency reduced to 9 kHz, which preserves some of the filter size reducing benefit, and 3 kHz, which allows a direct comparison with the silicon IGBTs with no change in the filter size.

Table 7 makes a further modification by assuming that the conduction losses were reduced by a factor of two. The SiC MOSFETs at full power had a forward conduction drop of 6 to 7 V, which is two to three times that experienced with the silicon IGBTs. This was surprising, and it can be explained in two ways. First, the conduction losses now are too high and will likely be reduced in the next several years as a matter of course. In addition to ohmic contacts, several regions of the SiC MOSFET contribute to its total forward resistance, including the channel

region, JFET components, and drift (blocking) region.  One or two of these contributors are amenable to improvement with work underway.

**Table 4. Loss Data for Each of Ten 150-kW SiC-Based Converters**
**50 kHz Switching Frequency, 690 VAC Nominal (Projected by UTenn)**

| Wind Speed | Gen Inv | Gen Inv | Gen Inv | Gen Inv | Gen Inv | Grid Inv | Grid Inv | Grid Inv | Grid Inv |
|---|---|---|---|---|---|---|---|---|---|
| | MOSFET | MOSFET | Diode | Diode | Loss | MOSFET | MOSFET | Diode | Diode |
| (m/s) | Cond Loss (W) | Sw Loss (W) | Cond Loss (W) | Sw Loss (W) | (per Inv)(kW) | Cond Loss (W) | Sw Loss (W) | Cond Loss (W) | Sw Loss (W) |
| 3.0 | 0.4 | 15 | 1.7 | 6.3 | 0.14 | 0.04 | 4 | 0.13 | 1.7 |
| 3.5 | 0.9 | 20.7 | 2.3 | 8.6 | 0.2 | 0.12 | 6 | 0.21 | 2.6 |
| 4.0 | 1.5 | 27.2 | 2.9 | 11.4 | 0.26 | 0.3 | 10 | 0.3 | 4 |
| 4.5 | 2.5 | 34.1 | 3.5 | 14.3 | 0.33 | 0.6 | 14 | 0.5 | 6 |
| 5.0 | 4 | 42 | 4 | 18 | 0.4 | 1 | 19 | 0.7 | 8 |
| 5.5 | 6 | 51 | 5 | 21 | 0.5 | 2 | 26 | 0.9 | 10 |
| 6.0 | 9 | 61 | 6 | 25 | 0.6 | 3 | 34 | 1 | 14 |
| 6.5 | 13 | 72 | 7 | 30 | 0.7 | 5 | 43 | 2 | 18 |
| 7.0 | 17 | 83 | 7 | 35 | 0.9 | 8 | 54 | 2 | 23 |
| 7.5 | 24 | 96 | 8 | 40 | 1 | 13 | 66 | 3 | 28 |
| 8.0 | 32 | 110 | 9 | 46 | 1.2 | 19 | 80 | 3 | 34 |
| 8.5 | 42 | 126 | 9 | 52 | 1.4 | 28 | 97 | 4 | 41 |
| 9.0 | 55 | 143 | 10 | 58 | 1.6 | 40 | 117 | 5 | 48 |
| 9.5 | 70 | 163 | 10 | 58 | 1.8 | 56 | 140 | 6 | 57 |
| 10.0 | 88 | 185 | 11 | 58 | 2.1 | 78 | 167 | 8 | 58 |
| 10.5 | 108 | 212 | 15 | 58 | 2.4 | 106 | 202 | 9 | 58 |
| 11.0 | 133 | 247 | 19 | 58 | 2.7 | 140 | 241 | 11 | 58 |
| 11.5 | 148 | 269 | 22 | 58 | 3 | 158 | 262 | 12 | 58 |
| 12.0 | 148 | 269 | 22 | 58 | 3 | 158 | 262 | 12 | 58 |
| 12.5 | 148 | 269 | 22 | 58 | 3 | 158 | 262 | 12 | 58 |
| 13.0 | 148 | 269 | 22 | 58 | 3 | 158 | 262 | 12 | 58 |
| 13.5 | 148 | 269 | 22 | 58 | 3 | 158 | 262 | 12 | 58 |
| 14.0 | 148 | 269 | 22 | 58 | 3 | 158 | 262 | 12 | 58 |
| 14.5 | 148 | 269 | 22 | 58 | 3 | 158 | 262 | 12 | 58 |
| 15.0 | 148 | 269 | 22 | 58 | 3 | 158 | 262 | 12 | 58 |
| 15.5 | 148 | 269 | 22 | 58 | 3 | 158 | 262 | 12 | 58 |
| 16.0 | 148 | 269 | 22 | 58 | 3 | 158 | 262 | 12 | 58 |
| 16.5 | 148 | 269 | 22 | 58 | 3 | 158 | 262 | 12 | 58 |
| 17.0 | 148 | 269 | 22 | 58 | 3 | 158 | 262 | 12 | 58 |
| 17.5 | 148 | 269 | 22 | 58 | 3 | 158 | 262 | 12 | 58 |
| 18.0 | 148 | 269 | 22 | 58 | 3 | 158 | 262 | 12 | 58 |
| 18.5 | 148 | 269 | 22 | 58 | 3 | 158 | 262 | 12 | 58 |
| 19.0 | 148 | 269 | 22 | 58 | 3 | 158 | 262 | 12 | 58 |
| 19.5 | 148 | 269 | 22 | 58 | 3 | 158 | 262 | 12 | 58 |
| 20.0 | 148 | 269 | 22 | 58 | 3 | 158 | 262 | 12 | 58 |
| 20.5 | 148 | 269 | 22 | 58 | 3 | 158 | 262 | 12 | 58 |
| 21.0 | 148 | 269 | 22 | 58 | 3 | 158 | 262 | 12 | 58 |
| 21.5 | 148 | 269 | 22 | 58 | 3 | 158 | 262 | 12 | 58 |
| 22.0 | 148 | 269 | 22 | 58 | 3 | 158 | 262 | 12 | 58 |
| 22.5 | 148 | 269 | 22 | 58 | 3 | 158 | 262 | 12 | 58 |
| 23.0 | 148 | 269 | 22 | 58 | 3 | 158 | 262 | 12 | 58 |
| 23.5 | 148 | 269 | 22 | 58 | 3 | 158 | 262 | 12 | 58 |
| 24.0 | 148 | 269 | 22 | 58 | 3 | 158 | 262 | 12 | 58 |
| 24.5 | 148 | 269 | 22 | 58 | 3 | 158 | 262 | 12 | 58 |
| 25.0 | 148 | 269 | 22 | 58 | 3 | 158 | 262 | 12 | 58 |
| 25.5 | 148 | 269 | 22 | 58 | 3 | 158 | 262 | 12 | 58 |
| 26.0 | 148 | 269 | 22 | 58 | 3 | 158 | 262 | 12 | 58 |
| 26.5 | 148 | 269 | 22 | 58 | 3 | 158 | 262 | 12 | 58 |

## Table 5. Converter Efficiency for Baseline Wind Turbine
## Silicon-Based, 3 kHz Switching Frequency, 690 VAC Nominal

| Wind Speed (m/s) | Gen Inv IGBT Cond Loss (w) | Gen Inv IGBT Sw loss (w) | Gen Inv Diode Cond Loss (w) | Gen Inv Diode Sw loss (w) | Gen Inv loss (per inv) (kW) | Util Inv IGBT Cond Loss (w) | Util Inv IGBT Sw loss (w) | Util Inv Diode Cond Loss (w) | Util Inv Diode Sw loss (w) | Util Inv Loss (per inv) (kW) | Filter Loss (kW) | Total Loss (kW) | Total PE Eff. | | Energy Prod for Weighting | Energy Times Eff |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 3 | 18 | 40 | 10 | 13 | 3 | 6 | 10 | 1 | 13 | 3.2 | 4.0 | 17.3 | 39.2% | | 0.0 | 0.0 |
| 3.5 | 26 | 57 | 13 | 14 | 4 | 10 | 17 | 2 | 13 | 3.3 | 4.0 | 17.8 | 61.9% | | 1.0 | 0.6 |
| 4 | 36 | 75 | 17 | 14 | 4 | 16 | 26 | 3 | 13 | 3.3 | 4.0 | 18.4 | 73.9% | | 10.0 | 7.4 |
| 4.5 | 47 | 95 | 21 | 14 | 4 | 23 | 38 | 4 | 13 | 3.5 | 4.0 | 19.1 | 81.1% | | 23.0 | 18.6 |
| 5 | 61 | 119 | 25 | 14 | 4 | 33 | 53 | 5 | 14 | 3.6 | 4.1 | 20.0 | 85.7% | | 41.0 | 35.1 |
| 5.5 | 78 | 144 | 29 | 15 | 5 | 45 | 71 | 7 | 14 | 3.8 | 4.2 | 21.0 | 88.7% | | 63.0 | 55.9 |
| 6 | 97 | 172 | 34 | 15 | 5 | 59 | 93 | 10 | 14 | 4.1 | 4.3 | 22.2 | 90.8% | | 89.0 | 80.8 |
| 6.5 | 119 | 203 | 38 | 16 | 5 | 77 | 119 | 12 | 14 | 4.3 | 4.5 | 23.7 | 92.3% | | 117.0 | 108.0 |
| 7 | 145 | 236 | 42 | 16 | 6 | 99 | 149 | 16 | 15 | 4.7 | 4.7 | 25.4 | 93.4% | | 148.0 | 138.3 |
| 7.5 | 174 | 272 | 46 | 16 | 6 | 125 | 184 | 20 | 15 | 5.1 | 5.1 | 27.4 | 94.2% | | 182.0 | 171.5 |
| 8 | 208 | 311 | 50 | 17 | 7 | 156 | 224 | 24 | 16 | 5.5 | 5.7 | 29.8 | 94.9% | | 216.0 | 204.9 |
| 8.5 | 246 | 352 | 54 | 17 | 7 | 193 | 269 | 29 | 16 | 6.0 | 6.4 | 32.6 | 95.3% | | 251.0 | 239.2 |
| 9 | 289 | 396 | 57 | 18 | 8 | 237 | 320 | 35 | 17 | 6.7 | 7.5 | 35.9 | 95.7% | | 286.0 | 273.6 |
| 9.5 | 337 | 441 | 60 | 19 | 8 | 288 | 376 | 42 | 18 | 7.3 | 8.8 | 39.7 | 95.9% | | 316.0 | 303.0 |
| 10 | 393 | 491 | 62 | 19 | 9 | 349 | 440 | 50 | 19 | 8.1 | 10.5 | 44.4 | 96.1% | | 346.0 | 332.4 |
| 10.5 | 455 | 542 | 64 | 20 | 9 | 420 | 510 | 59 | 20 | 9.1 | 12.8 | 49.8 | 96.2% | | 371.0 | 356.9 |
| 11 | 529 | 607 | 70 | 21 | 10 | 497 | 580 | 68 | 21 | 10.0 | 15.3 | 56.0 | 96.2% | | 387.0 | 372.5 |
| 11.5 | 569 | 642 | 75 | 21 | 11 | 533 | 612 | 72 | 21 | 10.4 | 16.6 | 59.2 | 96.2% | | 358.0 | 344.6 |
| 12 | 569 | 642 | 75 | 21 | 11 | 533 | 612 | 72 | 21 | 10.4 | 16.6 | 59.2 | 96.2% | | 322.0 | 309.9 |
| 12.5 | 569 | 642 | 75 | 21 | 11 | 533 | 612 | 72 | 21 | 10.4 | 16.6 | 59.2 | 96.2% | | 287.0 | 276.2 |
| 13 | 569 | 642 | 75 | 21 | 11 | 533 | 612 | 72 | 21 | 10.4 | 16.6 | 59.2 | 96.2% | | 254.0 | 244.5 |
| 13.5 | 569 | 642 | 75 | 21 | 11 | 533 | 612 | 72 | 21 | 10.4 | 16.6 | 59.2 | 96.2% | | 223.0 | 214.6 |
| 14 | 569 | 642 | 75 | 21 | 11 | 533 | 612 | 72 | 21 | 10.4 | 16.6 | 59.2 | 96.2% | | 194.0 | 186.7 |
| 14.5 | 569 | 642 | 75 | 21 | 11 | 533 | 612 | 72 | 21 | 10.4 | 16.6 | 59.2 | 96.2% | | 168.0 | 161.7 |
| 15 | 569 | 642 | 75 | 21 | 11 | 533 | 612 | 72 | 21 | 10.4 | 16.6 | 59.2 | 96.2% | | 144.0 | 138.6 |
| 15.5 | 569 | 642 | 75 | 21 | 11 | 533 | 612 | 72 | 21 | 10.4 | 16.6 | 59.2 | 96.2% | | 122.0 | 117.4 |
| 16 | 569 | 642 | 75 | 21 | 11 | 533 | 612 | 72 | 21 | 10.4 | 16.6 | 59.2 | 96.2% | | 103.0 | 99.1 |
| 16.5 | 569 | 642 | 75 | 21 | 11 | 533 | 612 | 72 | 21 | 10.4 | 16.6 | 59.2 | 96.2% | | 87.0 | 83.7 |
| 17 | 569 | 642 | 75 | 21 | 11 | 533 | 612 | 72 | 21 | 10.4 | 16.6 | 59.2 | 96.2% | | 72.0 | 69.3 |
| 17.5 | 569 | 642 | 75 | 21 | 11 | 533 | 612 | 72 | 21 | 10.4 | 16.6 | 59.2 | 96.2% | | 60.0 | 57.7 |
| 18 | 569 | 642 | 75 | 21 | 11 | 533 | 612 | 72 | 21 | 10.4 | 16.6 | 59.2 | 96.2% | | 49.0 | 47.2 |
| 18.5 | 569 | 642 | 75 | 21 | 11 | 533 | 612 | 72 | 21 | 10.4 | 16.6 | 59.2 | 96.2% | | 40.0 | 38.5 |
| 19 | 569 | 642 | 75 | 21 | 11 | 533 | 612 | 72 | 21 | 10.4 | 16.6 | 59.2 | 96.2% | | 32.0 | 30.8 |
| 19.5 | 569 | 642 | 75 | 21 | 11 | 533 | 612 | 72 | 21 | 10.4 | 16.6 | 59.2 | 96.2% | | 26.0 | 25.0 |
| 20 | 569 | 642 | 75 | 21 | 11 | 533 | 612 | 72 | 21 | 10.4 | 16.6 | 59.2 | 96.2% | | 21.0 | 20.2 |
| 20.5 | 569 | 642 | 75 | 21 | 11 | 533 | 612 | 72 | 21 | 10.4 | 16.6 | 59.2 | 96.2% | | 16.0 | 15.4 |
| 21 | 569 | 642 | 75 | 21 | 11 | 533 | 612 | 72 | 21 | 10.4 | 16.6 | 59.2 | 96.2% | | 13.0 | 12.5 |
| 21.5 | 569 | 642 | 75 | 21 | 11 | 533 | 612 | 72 | 21 | 10.4 | 16.6 | 59.2 | 96.2% | | 10.0 | 9.6 |
| 22 | 569 | 642 | 75 | 21 | 11 | 533 | 612 | 72 | 21 | 10.4 | 16.6 | 59.2 | 96.2% | | 8.0 | 7.7 |
| 22.5 | 569 | 642 | 75 | 21 | 11 | 533 | 612 | 72 | 21 | 10.4 | 16.6 | 59.2 | 96.2% | | 6.0 | 5.8 |
| 23 | 569 | 642 | 75 | 21 | 11 | 533 | 612 | 72 | 21 | 10.4 | 16.6 | 59.2 | 96.2% | | 5.0 | 4.8 |
| 23.5 | 569 | 642 | 75 | 21 | 11 | 533 | 612 | 72 | 21 | 10.4 | 16.6 | 59.2 | 96.2% | | 4.0 | 3.8 |
| 24 | 569 | 642 | 75 | 21 | 11 | 533 | 612 | 72 | 21 | 10.4 | 16.6 | 59.2 | 96.2% | | 3.0 | 2.9 |
| 24.5 | 569 | 642 | 75 | 21 | 11 | 533 | 612 | 72 | 21 | 10.4 | 16.6 | 59.2 | 96.2% | | 2.0 | 1.9 |
| 25 | 569 | 642 | 75 | 21 | 11 | 533 | 612 | 72 | 21 | 10.4 | 16.6 | 59.2 | 96.2% | | 1.0 | 1.0 |
| 25.5 | 569 | 642 | 75 | 21 | 11 | 533 | 612 | 72 | 21 | 10.4 | 16.6 | 59.2 | 96.2% | | 1.0 | 1.0 |
| 26 | 569 | 642 | 75 | 21 | 11 | 533 | 612 | 72 | 21 | 10.4 | 16.6 | 59.2 | 96.2% | | 1.0 | 1.0 |
| 26.5 | 569 | 642 | 75 | 21 | 11 | 533 | 612 | 72 | 21 | 10.4 | 16.6 | 59.2 | 96.2% | | 1.0 | 1.0 |
| 27 | 569 | 642 | 75 | 21 | 11 | 533 | 612 | 72 | 21 | 10.4 | 16.6 | 59.2 | 96.2% | | 0.0 | 0.0 |
| 27.5 | 569 | 642 | 75 | 21 | 11 | 533 | 612 | 72 | 21 | 10.4 | 16.6 | 59.2 | 96.2% | | 0.0 | 0.0 |
| 28 | 569 | 642 | 75 | 21 | 11 | 533 | 612 | 72 | 21 | 10.4 | 16.6 | 59.2 | 96.2% | | 0.0 | 0.0 |
| 28.5 | 569 | 642 | 75 | 21 | 11 | 533 | 612 | 72 | 21 | 10.4 | 16.6 | 59.2 | 96.2% | | 0.0 | 0.0 |
| 29 | 569 | 642 | 75 | 21 | 11 | 533 | 612 | 72 | 21 | 10.4 | 16.6 | 59.2 | 96.2% | | 0.0 | 0.0 |
| 29.5 | 569 | 642 | 75 | 21 | 11 | 533 | 612 | 72 | 21 | 10.4 | 16.6 | 59.2 | 96.2% | | 0.0 | 0.0 |
| 30 | 569 | 642 | 75 | 21 | 11 | 533 | 612 | 72 | 21 | 10.4 | 16.6 | 59.2 | 96.2% | | 0.0 | 0.0 |
| | | | | | | | | | | | | | | | 5.48E+03 | 5.23E+03 |
| | | | | | | | | | | | | | | | | 95.49% |

## Table 6. Concept Converter Efficiency with SiC MOSFETs/SiC Schottkys, 50 kHz

| Wind Speed (m/s) | Gen Inv MOS Cond Loss (w) | Gen Inv MOS Sw loss (w) | Gen Inv Diode Cond Loss (w) | Gen Inv Diode Sw loss (w) | Gen Inv loss (per inv) (kW) | Util Inv MOS Cond Loss (w) | Util Inv MOS Sw loss (w) | Util Inv Diode Cond Loss (w) | Util Inv Diode Sw loss (w) | Util Inv Loss (per inv) (kW) | Filter Loss (kW) | Total Loss (kW) | Total PE Eff. | | Energy Prod for Weighting | Energy Times Eff |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | | | | | | | |
| 3 | 0.4 | 15 | 1.7 | 6.3 | 0.29 | 0.04 | 4 | 0.13 | 1.7 | 0.19 | 4.0 | 8.8 | 69.3% | | 0.0 | 0.0 |
| 3.5 | 0.9 | 20.7 | 2.3 | 8.6 | 0.35 | 0.12 | 6 | 0.21 | 2.6 | 0.20 | 4.0 | 9.5 | 79.7% | | 1.0 | 0.8 |
| 4 | 1.5 | 27.2 | 2.9 | 11.4 | 0.41 | 0.3 | 10 | 0.3 | 4 | 0.24 | 4.0 | 10.5 | 85.2% | | 10.0 | 8.5 |
| 4.5 | 2.5 | 34.1 | 3.5 | 14.3 | 0.48 | 0.6 | 14 | 0.5 | 6 | 0.28 | 4.1 | 11.6 | 88.5% | | 23.0 | 20.4 |
| 5 | 4 | 42 | 4 | 18 | 0.56 | 1 | 19 | 0.7 | 8 | 0.32 | 4.1 | 12.9 | 90.7% | | 41.0 | 37.2 |
| 5.5 | 6 | 51 | 5 | 21 | 0.65 | 2 | 26 | 0.9 | 10 | 0.38 | 4.2 | 14.5 | 92.2% | | 63.0 | 58.1 |
| 6 | 9 | 61 | 6 | 25 | 0.76 | 3 | 34 | 1 | 14 | 0.46 | 4.3 | 16.5 | 93.2% | | 89.0 | 82.9 |
| 6.5 | 13 | 72 | 7 | 30 | 0.88 | 5 | 43 | 2 | 18 | 0.56 | 4.5 | 18.9 | 93.9% | | 117.0 | 109.8 |
| 7 | 17 | 83 | 7 | 35 | 1.00 | 8 | 54 | 2 | 23 | 0.67 | 4.8 | 21.5 | 94.4% | | 148.0 | 139.8 |
| 7.5 | 24 | 96 | 8 | 40 | 1.16 | 13 | 66 | 3 | 28 | 0.81 | 5.2 | 24.8 | 94.8% | | 182.0 | 172.5 |
| 8 | 32 | 110 | 9 | 46 | 1.33 | 19 | 80 | 3 | 34 | 0.97 | 5.7 | 28.7 | 95.0% | | 216.0 | 205.3 |
| 8.5 | 42 | 126 | 9 | 52 | 1.52 | 28 | 97 | 4 | 41 | 1.17 | 6.5 | 33.4 | 95.2% | | 251.0 | 238.9 |
| 9 | 55 | 143 | 10 | 58 | 1.75 | 40 | 117 | 5 | 48 | 1.41 | 7.5 | 39.1 | 95.3% | | 286.0 | 272.5 |
| 9.5 | 70 | 163 | 10 | 58 | 1.96 | 56 | 140 | 6 | 57 | 1.70 | 8.8 | 45.4 | 95.3% | | 316.0 | 301.2 |
| 10 | 88 | 185 | 11 | 58 | 2.20 | 78 | 167 | 8 | 58 | 2.02 | 10.6 | 52.8 | 95.3% | | 346.0 | 329.9 |
| 10.5 | 108 | 212 | 15 | 58 | 2.51 | 106 | 202 | 9 | 58 | 2.40 | 12.8 | 61.9 | 95.3% | | 371.0 | 353.5 |
| 11 | 133 | 247 | 19 | 58 | 2.89 | 140 | 241 | 11 | 58 | 2.85 | 15.5 | 72.9 | 95.1% | | 387.0 | 368.1 |
| 11.5 | 148 | 269 | 22 | 58 | 3.13 | 158 | 262 | 12 | 58 | 3.09 | 16.8 | 79.0 | 95.0% | | 358.0 | 340.1 |
| 12 | 148 | 269 | 22 | 58 | 3.13 | 158 | 262 | 12 | 58 | 3.09 | 16.8 | 79.0 | 95.0% | | 322.0 | 305.9 |
| 12.5 | 148 | 269 | 22 | 58 | 3.13 | 158 | 262 | 12 | 58 | 3.09 | 16.8 | 79.0 | 95.0% | | 287.0 | 272.6 |
| 13 | 148 | 269 | 22 | 58 | 3.13 | 158 | 262 | 12 | 58 | 3.09 | 16.8 | 79.0 | 95.0% | | 254.0 | 241.3 |
| 13.5 | 148 | 269 | 22 | 58 | 3.13 | 158 | 262 | 12 | 58 | 3.09 | 16.8 | 79.0 | 95.0% | | 223.0 | 211.8 |
| 14 | 148 | 269 | 22 | 58 | 3.13 | 158 | 262 | 12 | 58 | 3.09 | 16.8 | 79.0 | 95.0% | | 194.0 | 184.3 |
| 14.5 | 148 | 269 | 22 | 58 | 3.13 | 158 | 262 | 12 | 58 | 3.09 | 16.8 | 79.0 | 95.0% | | 168.0 | 159.6 |
| 15 | 148 | 269 | 22 | 58 | 3.13 | 158 | 262 | 12 | 58 | 3.09 | 16.8 | 79.0 | 95.0% | | 144.0 | 136.8 |
| 15.5 | 148 | 269 | 22 | 58 | 3.13 | 158 | 262 | 12 | 58 | 3.09 | 16.8 | 79.0 | 95.0% | | 122.0 | 115.9 |
| 16 | 148 | 269 | 22 | 58 | 3.13 | 158 | 262 | 12 | 58 | 3.09 | 16.8 | 79.0 | 95.0% | | 103.0 | 97.8 |
| 16.5 | 148 | 269 | 22 | 58 | 3.13 | 158 | 262 | 12 | 58 | 3.09 | 16.8 | 79.0 | 95.0% | | 87.0 | 82.6 |
| 17 | 148 | 269 | 22 | 58 | 3.13 | 158 | 262 | 12 | 58 | 3.09 | 16.8 | 79.0 | 95.0% | | 72.0 | 68.4 |
| 17.5 | 148 | 269 | 22 | 58 | 3.13 | 158 | 262 | 12 | 58 | 3.09 | 16.8 | 79.0 | 95.0% | | 60.0 | 57.0 |
| 18 | 148 | 269 | 22 | 58 | 3.13 | 158 | 262 | 12 | 58 | 3.09 | 16.8 | 79.0 | 95.0% | | 49.0 | 46.5 |
| 18.5 | 148 | 269 | 22 | 58 | 3.13 | 158 | 262 | 12 | 58 | 3.09 | 16.8 | 79.0 | 95.0% | | 40.0 | 38.0 |
| 19 | 148 | 269 | 22 | 58 | 3.13 | 158 | 262 | 12 | 58 | 3.09 | 16.8 | 79.0 | 95.0% | | 32.0 | 30.4 |
| 19.5 | 148 | 269 | 22 | 58 | 3.13 | 158 | 262 | 12 | 58 | 3.09 | 16.8 | 79.0 | 95.0% | | 26.0 | 24.7 |
| 20 | 148 | 269 | 22 | 58 | 3.13 | 158 | 262 | 12 | 58 | 3.09 | 16.8 | 79.0 | 95.0% | | 21.0 | 19.9 |
| 20.5 | 148 | 269 | 22 | 58 | 3.13 | 158 | 262 | 12 | 58 | 3.09 | 16.8 | 79.0 | 95.0% | | 16.0 | 15.2 |
| 21 | 148 | 269 | 22 | 58 | 3.13 | 158 | 262 | 12 | 58 | 3.09 | 16.8 | 79.0 | 95.0% | | 13.0 | 12.3 |
| 21.5 | 148 | 269 | 22 | 58 | 3.13 | 158 | 262 | 12 | 58 | 3.09 | 16.8 | 79.0 | 95.0% | | 10.0 | 9.5 |
| 22 | 148 | 269 | 22 | 58 | 3.13 | 158 | 262 | 12 | 58 | 3.09 | 16.8 | 79.0 | 95.0% | | 8.0 | 7.6 |
| 22.5 | 148 | 269 | 22 | 58 | 3.13 | 158 | 262 | 12 | 58 | 3.09 | 16.8 | 79.0 | 95.0% | | 6.0 | 5.7 |
| 23 | 148 | 269 | 22 | 58 | 3.13 | 158 | 262 | 12 | 58 | 3.09 | 16.8 | 79.0 | 95.0% | | 5.0 | 4.7 |
| 23.5 | 148 | 269 | 22 | 58 | 3.13 | 158 | 262 | 12 | 58 | 3.09 | 16.8 | 79.0 | 95.0% | | 4.0 | 3.8 |
| 24 | 148 | 269 | 22 | 58 | 3.13 | 158 | 262 | 12 | 58 | 3.09 | 16.8 | 79.0 | 95.0% | | 3.0 | 2.8 |
| 24.5 | 148 | 269 | 22 | 58 | 3.13 | 158 | 262 | 12 | 58 | 3.09 | 16.8 | 79.0 | 95.0% | | 2.0 | 1.9 |
| 25 | 148 | 269 | 22 | 58 | 3.13 | 158 | 262 | 12 | 58 | 3.09 | 16.8 | 79.0 | 95.0% | | 1.0 | 0.9 |
| 25.5 | 148 | 269 | 22 | 58 | 3.13 | 158 | 262 | 12 | 58 | 3.09 | 16.8 | 79.0 | 95.0% | | 1.0 | 0.9 |
| 26 | 148 | 269 | 22 | 58 | 3.13 | 158 | 262 | 12 | 58 | 3.09 | 16.8 | 79.0 | 95.0% | | 1.0 | 0.9 |
| 26.5 | 148 | 269 | 22 | 58 | 3.13 | 158 | 262 | 12 | 58 | 3.09 | 16.8 | 79.0 | 95.0% | | 1.0 | 0.9 |
| 27 | 148 | 269 | 22 | 58 | 3.13 | 158 | 262 | 12 | 58 | 3.09 | 16.8 | 79.0 | 95.0% | | 0.0 | 0.0 |
| 27.5 | 148 | 269 | 22 | 58 | 3.13 | 158 | 262 | 12 | 58 | 3.09 | 16.8 | 79.0 | 95.0% | | 0.0 | 0.0 |
| 28 | 148 | 269 | 22 | 58 | 3.13 | 158 | 262 | 12 | 58 | 3.09 | 16.8 | 79.0 | 95.0% | | 0.0 | 0.0 |
| 28.5 | 148 | 269 | 22 | 58 | 3.13 | 158 | 262 | 12 | 58 | 3.09 | 16.8 | 79.0 | 95.0% | | 0.0 | 0.0 |
| 29 | 148 | 269 | 22 | 58 | 3.13 | 158 | 262 | 12 | 58 | 3.09 | 16.8 | 79.0 | 95.0% | | 0.0 | 0.0 |
| 29.5 | 148 | 269 | 22 | 58 | 3.13 | 158 | 262 | 12 | 58 | 3.09 | 16.8 | 79.0 | 95.0% | | 0.0 | 0.0 |
| 30 | 148 | 269 | 22 | 58 | 3.13 | 158 | 262 | 12 | 58 | 3.09 | 16.8 | 79.0 | 95.0% | | 0.0 | 0.0 |
| | | | | | | | | | | | | | | | 5.48E+03 | 5.20E+03 |
| | | | | | | | | | | | | | | | | 94.90% |

## Table 7. Concept Converter Efficiency with SiC MOSFETs/SiC Schottkys, 9kHz

| Wind Speed (m/s) | Gen Inv MOS Cond Loss (w) | Gen Inv MOS Sw loss (w) | Gen Inv Diode Cond Loss (w) | Gen Inv Diode Sw loss (w) | Gen Inv loss (per inv) (kW) | Util Inv MOS Cond Loss (w) | Util Inv MOS Sw loss (w) | Util Inv Diode Cond Loss (w) | Util Inv Diode Sw loss (w) | Util Inv Loss (per inv) (kW) | Filter Loss (kW) | Total Loss (kW) | Total PE Eff. | | Energy Prod for Weighting | Energy Times Eff |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | | | | | | | |
| 3 | 0.4 | 2.70 | 1.7 | 1.13 | 0.19 | 0.04 | 0.72 | 0.13 | 0.31 | 0.16 | 4.0 | 7.4 | 73.9% | | 0.0 | 0.0 |
| 3.5 | 0.9 | 3.73 | 2.3 | 1.55 | 0.20 | 0.12 | 1.08 | 0.21 | 0.47 | 0.16 | 4.0 | 7.6 | 83.7% | | 1.0 | 0.8 |
| 4 | 1.5 | 4.90 | 2.9 | 2.05 | 0.22 | 0.3 | 1.80 | 0.3 | 0.72 | 0.17 | 4.0 | 7.9 | 88.8% | | 10.0 | 8.9 |
| 4.5 | 2.5 | 6.14 | 3.5 | 2.57 | 0.24 | 0.6 | 2.52 | 0.5 | 1.08 | 0.18 | 4.1 | 8.2 | 91.9% | | 23.0 | 21.1 |
| 5 | 4 | 7.56 | 4 | 3.24 | 0.26 | 1 | 3.42 | 0.7 | 1.44 | 0.19 | 4.1 | 8.6 | 93.8% | | 41.0 | 38.5 |
| 5.5 | 6 | 9.18 | 5 | 3.78 | 0.29 | 2 | 4.68 | 0.9 | 1.80 | 0.21 | 4.2 | 9.2 | 95.1% | | 63.0 | 59.9 |
| 6 | 9 | 10.98 | 6 | 4.50 | 0.33 | 3 | 6.12 | 1 | 2.52 | 0.23 | 4.3 | 9.9 | 95.9% | | 89.0 | 85.4 |
| 6.5 | 13 | 12.96 | 7 | 5.40 | 0.38 | 5 | 7.74 | 2 | 3.24 | 0.26 | 4.5 | 10.9 | 96.5% | | 117.0 | 112.9 |
| 7 | 17 | 14.94 | 7 | 6.30 | 0.42 | 8 | 9.72 | 2 | 4.14 | 0.29 | 4.8 | 11.9 | 96.9% | | 148.0 | 143.4 |
| 7.5 | 24 | 17.28 | 8 | 7.20 | 0.49 | 13 | 11.88 | 3 | 5.04 | 0.35 | 5.2 | 13.5 | 97.2% | | 182.0 | 176.8 |
| 8 | 32 | 19.80 | 9 | 8.28 | 0.56 | 19 | 14.40 | 3 | 6.12 | 0.41 | 5.7 | 15.4 | 97.3% | | 216.0 | 210.2 |
| 8.5 | 42 | 22.68 | 9 | 9.36 | 0.65 | 28 | 17.46 | 4 | 7.38 | 0.49 | 6.5 | 17.9 | 97.4% | | 251.0 | 244.5 |
| 9 | 55 | 25.74 | 10 | 10.44 | 0.76 | 40 | 21.06 | 5 | 8.64 | 0.60 | 7.5 | 21.1 | 97.4% | | 286.0 | 278.7 |
| 9.5 | 70 | 29.34 | 10 | 10.44 | 0.87 | 56 | 25.20 | 6 | 10.26 | 0.73 | 8.8 | 24.9 | 97.4% | | 316.0 | 307.9 |
| 10 | 88 | 33.30 | 11 | 10.44 | 1.01 | 78 | 30.06 | 8 | 10.44 | 0.91 | 10.6 | 29.8 | 97.4% | | 346.0 | 336.9 |
| 10.5 | 108 | 38.16 | 15 | 10.44 | 1.18 | 106 | 36.36 | 9 | 10.44 | 1.12 | 12.9 | 35.9 | 97.3% | | 371.0 | 360.9 |
| 11 | 133 | 44.46 | 19 | 10.44 | 1.39 | 140 | 43.38 | 11 | 10.44 | 1.38 | 15.5 | 43.2 | 97.1% | | 387.0 | 375.8 |
| 11.5 | 148 | 48.42 | 22 | 10.44 | 1.52 | 158 | 47.16 | 12 | 10.44 | 1.52 | 16.8 | 47.2 | 97.0% | | 358.0 | 347.3 |
| 12 | 148 | 48.42 | 22 | 10.44 | 1.52 | 158 | 47.16 | 12 | 10.44 | 1.52 | 16.8 | 47.2 | 97.0% | | 322.0 | 312.4 |
| 12.5 | 148 | 48.42 | 22 | 10.44 | 1.52 | 158 | 47.16 | 12 | 10.44 | 1.52 | 16.8 | 47.2 | 97.0% | | 287.0 | 278.4 |
| 13 | 148 | 48.42 | 22 | 10.44 | 1.52 | 158 | 47.16 | 12 | 10.44 | 1.52 | 16.8 | 47.2 | 97.0% | | 254.0 | 246.4 |
| 13.5 | 148 | 48.42 | 22 | 10.44 | 1.52 | 158 | 47.16 | 12 | 10.44 | 1.52 | 16.8 | 47.2 | 97.0% | | 223.0 | 216.3 |
| 14 | 148 | 48.42 | 22 | 10.44 | 1.52 | 158 | 47.16 | 12 | 10.44 | 1.52 | 16.8 | 47.2 | 97.0% | | 194.0 | 188.2 |
| 14.5 | 148 | 48.42 | 22 | 10.44 | 1.52 | 158 | 47.16 | 12 | 10.44 | 1.52 | 16.8 | 47.2 | 97.0% | | 168.0 | 163.0 |
| 15 | 148 | 48.42 | 22 | 10.44 | 1.52 | 158 | 47.16 | 12 | 10.44 | 1.52 | 16.8 | 47.2 | 97.0% | | 144.0 | 139.7 |
| 15.5 | 148 | 48.42 | 22 | 10.44 | 1.52 | 158 | 47.16 | 12 | 10.44 | 1.52 | 16.8 | 47.2 | 97.0% | | 122.0 | 118.3 |
| 16 | 148 | 48.42 | 22 | 10.44 | 1.52 | 158 | 47.16 | 12 | 10.44 | 1.52 | 16.8 | 47.2 | 97.0% | | 103.0 | 99.9 |
| 16.5 | 148 | 48.42 | 22 | 10.44 | 1.52 | 158 | 47.16 | 12 | 10.44 | 1.52 | 16.8 | 47.2 | 97.0% | | 87.0 | 84.4 |
| 17 | 148 | 48.42 | 22 | 10.44 | 1.52 | 158 | 47.16 | 12 | 10.44 | 1.52 | 16.8 | 47.2 | 97.0% | | 72.0 | 69.8 |
| 17.5 | 148 | 48.42 | 22 | 10.44 | 1.52 | 158 | 47.16 | 12 | 10.44 | 1.52 | 16.8 | 47.2 | 97.0% | | 60.0 | 58.2 |
| 18 | 148 | 48.42 | 22 | 10.44 | 1.52 | 158 | 47.16 | 12 | 10.44 | 1.52 | 16.8 | 47.2 | 97.0% | | 49.0 | 47.5 |
| 18.5 | 148 | 48.42 | 22 | 10.44 | 1.52 | 158 | 47.16 | 12 | 10.44 | 1.52 | 16.8 | 47.2 | 97.0% | | 40.0 | 38.8 |
| 19 | 148 | 48.42 | 22 | 10.44 | 1.52 | 158 | 47.16 | 12 | 10.44 | 1.52 | 16.8 | 47.2 | 97.0% | | 32.0 | 31.0 |
| 19.5 | 148 | 48.42 | 22 | 10.44 | 1.52 | 158 | 47.16 | 12 | 10.44 | 1.52 | 16.8 | 47.2 | 97.0% | | 26.0 | 25.2 |
| 20 | 148 | 48.42 | 22 | 10.44 | 1.52 | 158 | 47.16 | 12 | 10.44 | 1.52 | 16.8 | 47.2 | 97.0% | | 21.0 | 20.4 |
| 20.5 | 148 | 48.42 | 22 | 10.44 | 1.52 | 158 | 47.16 | 12 | 10.44 | 1.52 | 16.8 | 47.2 | 97.0% | | 16.0 | 15.5 |
| 21 | 148 | 48.42 | 22 | 10.44 | 1.52 | 158 | 47.16 | 12 | 10.44 | 1.52 | 16.8 | 47.2 | 97.0% | | 13.0 | 12.6 |
| 21.5 | 148 | 48.42 | 22 | 10.44 | 1.52 | 158 | 47.16 | 12 | 10.44 | 1.52 | 16.8 | 47.2 | 97.0% | | 10.0 | 9.7 |
| 22 | 148 | 48.42 | 22 | 10.44 | 1.52 | 158 | 47.16 | 12 | 10.44 | 1.52 | 16.8 | 47.2 | 97.0% | | 8.0 | 7.8 |
| 22.5 | 148 | 48.42 | 22 | 10.44 | 1.52 | 158 | 47.16 | 12 | 10.44 | 1.52 | 16.8 | 47.2 | 97.0% | | 6.0 | 5.8 |
| 23 | 148 | 48.42 | 22 | 10.44 | 1.52 | 158 | 47.16 | 12 | 10.44 | 1.52 | 16.8 | 47.2 | 97.0% | | 5.0 | 4.9 |
| 23.5 | 148 | 48.42 | 22 | 10.44 | 1.52 | 158 | 47.16 | 12 | 10.44 | 1.52 | 16.8 | 47.2 | 97.0% | | 4.0 | 3.9 |
| 24 | 148 | 48.42 | 22 | 10.44 | 1.52 | 158 | 47.16 | 12 | 10.44 | 1.52 | 16.8 | 47.2 | 97.0% | | 3.0 | 2.9 |
| 24.5 | 148 | 48.42 | 22 | 10.44 | 1.52 | 158 | 47.16 | 12 | 10.44 | 1.52 | 16.8 | 47.2 | 97.0% | | 2.0 | 1.9 |
| 25 | 148 | 48.42 | 22 | 10.44 | 1.52 | 158 | 47.16 | 12 | 10.44 | 1.52 | 16.8 | 47.2 | 97.0% | | 1.0 | 1.0 |
| 25.5 | 148 | 48.42 | 22 | 10.44 | 1.52 | 158 | 47.16 | 12 | 10.44 | 1.52 | 16.8 | 47.2 | 97.0% | | 1.0 | 1.0 |
| 26 | 148 | 48.42 | 22 | 10.44 | 1.52 | 158 | 47.16 | 12 | 10.44 | 1.52 | 16.8 | 47.2 | 97.0% | | 1.0 | 1.0 |
| 26.5 | 148 | 48.42 | 22 | 10.44 | 1.52 | 158 | 47.16 | 12 | 10.44 | 1.52 | 16.8 | 47.2 | 97.0% | | 1.0 | 1.0 |
| 27 | 148 | 48.42 | 22 | 10.44 | 1.52 | 158 | 47.16 | 12 | 10.44 | 1.52 | 16.8 | 47.2 | 97.0% | | 0.0 | 0.0 |
| 27.5 | 148 | 48.42 | 22 | 10.44 | 1.52 | 158 | 47.16 | 12 | 10.44 | 1.52 | 16.8 | 47.2 | 97.0% | | 0.0 | 0.0 |
| 28 | 148 | 48.42 | 22 | 10.44 | 1.52 | 158 | 47.16 | 12 | 10.44 | 1.52 | 16.8 | 47.2 | 97.0% | | 0.0 | 0.0 |
| 28.5 | 148 | 48.42 | 22 | 10.44 | 1.52 | 158 | 47.16 | 12 | 10.44 | 1.52 | 16.8 | 47.2 | 97.0% | | 0.0 | 0.0 |
| 29 | 148 | 48.42 | 22 | 10.44 | 1.52 | 158 | 47.16 | 12 | 10.44 | 1.52 | 16.8 | 47.2 | 97.0% | | 0.0 | 0.0 |
| 29.5 | 148 | 48.42 | 22 | 10.44 | 1.52 | 158 | 47.16 | 12 | 10.44 | 1.52 | 16.8 | 47.2 | 97.0% | | 0.0 | 0.0 |
| 30 | 148 | 48.42 | 22 | 10.44 | 1.52 | 158 | 47.16 | 12 | 10.44 | 1.52 | 16.8 | 47.2 | 97.0% | | 0.0 | 0.0 |
| | | | | | | | | | | | | | | | 5.48E+03 | 5.32E+03 |
| | | | | | | | | | | | | | | | | 97.02% |

## Table 8. Concept Converter Efficiency with SiC MOSFETs/SiC Schottkys, 3 kHz

| Wind Speed (m/s) | Gen Inv MOS Cond Loss (w) | Gen Inv MOS Sw loss (w) | Gen Inv Diode Cond Loss (w) | Gen Inv Diode Sw loss (w) | Gen Inv loss (per inv) (kW) | Util Inv MOS Cond Loss (w) | Util Inv MOS Sw loss (w) | Util Inv Diode Cond Loss (w) | Util Inv Diode Sw loss (w) | Util Inv Loss (per inv) (kW) | Filter Loss (kW) | Total Loss (kW) | Total PE Eff. | | Energy Prod for Weighting | Energy Times Eff |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | | | | | | | |
| 3 | 0.4 | 0.90 | 1.70 | 0.38 | 0.17 | 0.04 | 0.24 | 0.13 | 0.10 | 0.15 | 4.0 | 7.2 | 74.6% | | 0.0 | 0.0 |
| 3.5 | 0.9 | 1.24 | 2.30 | 0.52 | 0.18 | 0.12 | 0.36 | 0.21 | 0.16 | 0.16 | 4.0 | 7.4 | 84.3% | | 1.0 | 0.8 |
| 4 | 1.5 | 1.63 | 2.90 | 0.68 | 0.19 | 0.30 | 0.60 | 0.30 | 0.24 | 0.16 | 4.0 | 7.5 | 89.4% | | 10.0 | 8.9 |
| 4.5 | 2.5 | 2.05 | 3.50 | 0.86 | 0.20 | 0.60 | 0.84 | 0.50 | 0.36 | 0.16 | 4.1 | 7.7 | 92.4% | | 23.0 | 21.2 |
| 5 | 4 | 2.52 | 4.00 | 1.08 | 0.22 | 1.00 | 1.14 | 0.70 | 0.48 | 0.17 | 4.1 | 8.0 | 94.3% | | 41.0 | 38.6 |
| 5.5 | 6 | 3.06 | 5.00 | 1.26 | 0.24 | 2.00 | 1.56 | 0.90 | 0.60 | 0.18 | 4.2 | 8.4 | 95.5% | | 63.0 | 60.2 |
| 6 | 9 | 3.66 | 6.00 | 1.50 | 0.27 | 3.00 | 2.04 | 1.00 | 0.84 | 0.19 | 4.3 | 8.9 | 96.3% | | 89.0 | 85.7 |
| 6.5 | 13 | 4.32 | 7.00 | 1.80 | 0.31 | 5.00 | 2.58 | 2.00 | 1.08 | 0.21 | 4.5 | 9.7 | 96.9% | | 117.0 | 113.3 |
| 7 | 17 | 4.98 | 7.00 | 2.10 | 0.34 | 8.00 | 3.24 | 2.00 | 1.38 | 0.24 | 4.8 | 10.5 | 97.3% | | 148.0 | 144.0 |
| 7.5 | 24 | 5.76 | 8.00 | 2.40 | 0.39 | 13.00 | 3.96 | 3.00 | 1.68 | 0.28 | 5.2 | 11.9 | 97.5% | | 182.0 | 177.5 |
| 8 | 32 | 6.60 | 9.00 | 2.76 | 0.45 | 19.00 | 4.80 | 3.00 | 2.04 | 0.32 | 5.7 | 13.5 | 97.7% | | 216.0 | 211.0 |
| 8.5 | 42 | 7.56 | 9.00 | 3.12 | 0.52 | 28.00 | 5.82 | 4.00 | 2.46 | 0.39 | 6.5 | 15.6 | 97.8% | | 251.0 | 245.4 |
| 9 | 55 | 8.58 | 10.00 | 3.48 | 0.61 | 40.00 | 7.02 | 5.00 | 2.88 | 0.48 | 7.5 | 18.4 | 97.8% | | 286.0 | 279.6 |
| 9.5 | 70 | 9.78 | 10.00 | 3.48 | 0.71 | 56.00 | 8.40 | 6.00 | 3.42 | 0.59 | 8.8 | 21.9 | 97.7% | | 316.0 | 308.9 |
| 10 | 88 | 11.10 | 11.00 | 3.48 | 0.83 | 78.00 | 10.02 | 8.00 | 3.48 | 0.75 | 10.6 | 26.4 | 97.7% | | 346.0 | 337.9 |
| 10.5 | 108 | 12.72 | 15.00 | 3.48 | 0.99 | 106.00 | 12.12 | 9.00 | 3.48 | 0.93 | 12.9 | 32.1 | 97.6% | | 371.0 | 361.9 |
| 11 | 133 | 14.82 | 19.00 | 3.48 | 1.17 | 140.00 | 14.46 | 11.00 | 3.48 | 1.16 | 15.5 | 38.8 | 97.4% | | 387.0 | 376.9 |
| 11.5 | 148 | 16.14 | 22.00 | 3.48 | 1.29 | 158.00 | 15.72 | 12.00 | 3.48 | 1.29 | 16.8 | 42.5 | 97.3% | | 358.0 | 348.3 |
| 12 | 148 | 16.14 | 22.00 | 3.48 | 1.29 | 158.00 | 15.72 | 12.00 | 3.48 | 1.29 | 16.8 | 42.5 | 97.3% | | 322.0 | 313.3 |
| 12.5 | 148 | 16.14 | 22.00 | 3.48 | 1.29 | 158.00 | 15.72 | 12.00 | 3.48 | 1.29 | 16.8 | 42.5 | 97.3% | | 287.0 | 279.3 |
| 13 | 148 | 16.14 | 22.00 | 3.48 | 1.29 | 158.00 | 15.72 | 12.00 | 3.48 | 1.29 | 16.8 | 42.5 | 97.3% | | 254.0 | 247.1 |
| 13.5 | 148 | 16.14 | 22.00 | 3.48 | 1.29 | 158.00 | 15.72 | 12.00 | 3.48 | 1.29 | 16.8 | 42.5 | 97.3% | | 223.0 | 217.0 |
| 14 | 148 | 16.14 | 22.00 | 3.48 | 1.29 | 158.00 | 15.72 | 12.00 | 3.48 | 1.29 | 16.8 | 42.5 | 97.3% | | 194.0 | 188.8 |
| 14.5 | 148 | 16.14 | 22.00 | 3.48 | 1.29 | 158.00 | 15.72 | 12.00 | 3.48 | 1.29 | 16.8 | 42.5 | 97.3% | | 168.0 | 163.5 |
| 15 | 148 | 16.14 | 22.00 | 3.48 | 1.29 | 158.00 | 15.72 | 12.00 | 3.48 | 1.29 | 16.8 | 42.5 | 97.3% | | 144.0 | 140.1 |
| 15.5 | 148 | 16.14 | 22.00 | 3.48 | 1.29 | 158.00 | 15.72 | 12.00 | 3.48 | 1.29 | 16.8 | 42.5 | 97.3% | | 122.0 | 118.7 |
| 16 | 148 | 16.14 | 22.00 | 3.48 | 1.29 | 158.00 | 15.72 | 12.00 | 3.48 | 1.29 | 16.8 | 42.5 | 97.3% | | 103.0 | 100.2 |
| 16.5 | 148 | 16.14 | 22.00 | 3.48 | 1.29 | 158.00 | 15.72 | 12.00 | 3.48 | 1.29 | 16.8 | 42.5 | 97.3% | | 87.0 | 84.7 |
| 17 | 148 | 16.14 | 22.00 | 3.48 | 1.29 | 158.00 | 15.72 | 12.00 | 3.48 | 1.29 | 16.8 | 42.5 | 97.3% | | 72.0 | 70.1 |
| 17.5 | 148 | 16.14 | 22.00 | 3.48 | 1.29 | 158.00 | 15.72 | 12.00 | 3.48 | 1.29 | 16.8 | 42.5 | 97.3% | | 60.0 | 58.4 |
| 18 | 148 | 16.14 | 22.00 | 3.48 | 1.29 | 158.00 | 15.72 | 12.00 | 3.48 | 1.29 | 16.8 | 42.5 | 97.3% | | 49.0 | 47.7 |
| 18.5 | 148 | 16.14 | 22.00 | 3.48 | 1.29 | 158.00 | 15.72 | 12.00 | 3.48 | 1.29 | 16.8 | 42.5 | 97.3% | | 40.0 | 38.9 |
| 19 | 148 | 16.14 | 22.00 | 3.48 | 1.29 | 158.00 | 15.72 | 12.00 | 3.48 | 1.29 | 16.8 | 42.5 | 97.3% | | 32.0 | 31.1 |
| 19.5 | 148 | 16.14 | 22.00 | 3.48 | 1.29 | 158.00 | 15.72 | 12.00 | 3.48 | 1.29 | 16.8 | 42.5 | 97.3% | | 26.0 | 25.3 |
| 20 | 148 | 16.14 | 22.00 | 3.48 | 1.29 | 158.00 | 15.72 | 12.00 | 3.48 | 1.29 | 16.8 | 42.5 | 97.3% | | 21.0 | 20.4 |
| 20.5 | 148 | 16.14 | 22.00 | 3.48 | 1.29 | 158.00 | 15.72 | 12.00 | 3.48 | 1.29 | 16.8 | 42.5 | 97.3% | | 16.0 | 15.6 |
| 21 | 148 | 16.14 | 22.00 | 3.48 | 1.29 | 158.00 | 15.72 | 12.00 | 3.48 | 1.29 | 16.8 | 42.5 | 97.3% | | 13.0 | 12.6 |
| 21.5 | 148 | 16.14 | 22.00 | 3.48 | 1.29 | 158.00 | 15.72 | 12.00 | 3.48 | 1.29 | 16.8 | 42.5 | 97.3% | | 10.0 | 9.7 |
| 22 | 148 | 16.14 | 22.00 | 3.48 | 1.29 | 158.00 | 15.72 | 12.00 | 3.48 | 1.29 | 16.8 | 42.5 | 97.3% | | 8.0 | 7.8 |
| 22.5 | 148 | 16.14 | 22.00 | 3.48 | 1.29 | 158.00 | 15.72 | 12.00 | 3.48 | 1.29 | 16.8 | 42.5 | 97.3% | | 6.0 | 5.8 |
| 23 | 148 | 16.14 | 22.00 | 3.48 | 1.29 | 158.00 | 15.72 | 12.00 | 3.48 | 1.29 | 16.8 | 42.5 | 97.3% | | 5.0 | 4.9 |
| 23.5 | 148 | 16.14 | 22.00 | 3.48 | 1.29 | 158.00 | 15.72 | 12.00 | 3.48 | 1.29 | 16.8 | 42.5 | 97.3% | | 4.0 | 3.9 |
| 24 | 148 | 16.14 | 22.00 | 3.48 | 1.29 | 158.00 | 15.72 | 12.00 | 3.48 | 1.29 | 16.8 | 42.5 | 97.3% | | 3.0 | 2.9 |
| 24.5 | 148 | 16.14 | 22.00 | 3.48 | 1.29 | 158.00 | 15.72 | 12.00 | 3.48 | 1.29 | 16.8 | 42.5 | 97.3% | | 2.0 | 1.9 |
| 25 | 148 | 16.14 | 22.00 | 3.48 | 1.29 | 158.00 | 15.72 | 12.00 | 3.48 | 1.29 | 16.8 | 42.5 | 97.3% | | 1.0 | 1.0 |
| 25.5 | 148 | 16.14 | 22.00 | 3.48 | 1.29 | 158.00 | 15.72 | 12.00 | 3.48 | 1.29 | 16.8 | 42.5 | 97.3% | | 1.0 | 1.0 |
| 26 | 148 | 16.14 | 22.00 | 3.48 | 1.29 | 158.00 | 15.72 | 12.00 | 3.48 | 1.29 | 16.8 | 42.5 | 97.3% | | 1.0 | 1.0 |
| 26.5 | 148 | 16.14 | 22.00 | 3.48 | 1.29 | 158.00 | 15.72 | 12.00 | 3.48 | 1.29 | 16.8 | 42.5 | 97.3% | | 1.0 | 1.0 |
| 27 | 148 | 16.14 | 22.00 | 3.48 | 1.29 | 158.00 | 15.72 | 12.00 | 3.48 | 1.29 | 16.8 | 42.5 | 97.3% | | 0.0 | 0.0 |
| 27.5 | 148 | 16.14 | 22.00 | 3.48 | 1.29 | 158.00 | 15.72 | 12.00 | 3.48 | 1.29 | 16.8 | 42.5 | 97.3% | | 0.0 | 0.0 |
| 28 | 148 | 16.14 | 22.00 | 3.48 | 1.29 | 158.00 | 15.72 | 12.00 | 3.48 | 1.29 | 16.8 | 42.5 | 97.3% | | 0.0 | 0.0 |
| 28.5 | 148 | 16.14 | 22.00 | 3.48 | 1.29 | 158.00 | 15.72 | 12.00 | 3.48 | 1.29 | 16.8 | 42.5 | 97.3% | | 0.0 | 0.0 |
| 29 | 148 | 16.14 | 22.00 | 3.48 | 1.29 | 158.00 | 15.72 | 12.00 | 3.48 | 1.29 | 16.8 | 42.5 | 97.3% | | 0.0 | 0.0 |
| 29.5 | 148 | 16.14 | 22.00 | 3.48 | 1.29 | 158.00 | 15.72 | 12.00 | 3.48 | 1.29 | 16.8 | 42.5 | 97.3% | | 0.0 | 0.0 |
| 30 | 148 | 16.14 | 22.00 | 3.48 | 1.29 | 158.00 | 15.72 | 12.00 | 3.48 | 1.29 | 16.8 | 42.5 | 97.3% | | 0.0 | 0.0 |
| | | | | | | | | | | | | | | | 5.48E+03 | 5.33E+03 |
| | | | | | | | | | | | | | | | | 97.33% |

## Table 9. Concept Converter Efficiency with SiC MOSFETs/SiC Schottkys, 3 kHz, 50% Conduction Loss

| Wind Speed (m/s) | Gen Inv MOS Cond Loss (w) | Gen Inv MOS Sw loss (w) | Gen Inv Diode Cond Loss (w) | Gen Inv Diode Sw loss (w) | Gen Inv loss (per inv) (kW) | Util Inv MOS Cond Loss (w) | Util Inv MOS Sw loss (w) | Util Inv Diode Cond Loss (w) | Util Inv Diode Sw loss (w) | Util Inv Loss (per inv) (kW) | Filter Loss (kW) | Total Loss (kW) | Total PE Eff. | | Energy Prod for Weighting | Energy Times Eff |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | | | | | | | |
| 3 | 0.2 | 0.90 | 0.85 | 0.38 | 0.16 | 0.02 | 0.24 | 0.065 | 0.10 | 0.15 | 4.0 | 7.2 | 74.8% | | 0.0 | 0.0 |
| 3.5 | 0.45 | 1.24 | 1.15 | 0.52 | 0.17 | 0.06 | 0.36 | 0.105 | 0.16 | 0.15 | 4.0 | 7.3 | 84.5% | | 1.0 | 0.8 |
| 4 | 0.75 | 1.63 | 1.45 | 0.68 | 0.18 | 0.15 | 0.60 | 0.15 | 0.24 | 0.16 | 4.0 | 7.4 | 89.6% | | 10.0 | 9.0 |
| 4.5 | 1.25 | 2.05 | 1.75 | 0.86 | 0.19 | 0.3 | 0.84 | 0.25 | 0.36 | 0.16 | 4.1 | 7.5 | 92.6% | | 23.0 | 21.3 |
| 5 | 2 | 2.52 | 2 | 1.08 | 0.20 | 0.5 | 1.14 | 0.35 | 0.48 | 0.16 | 4.1 | 7.7 | 94.5% | | 41.0 | 38.7 |
| 5.5 | 3 | 3.06 | 2.5 | 1.26 | 0.21 | 1 | 1.56 | 0.45 | 0.60 | 0.17 | 4.2 | 8.0 | 95.7% | | 63.0 | 60.3 |
| 6 | 4.5 | 3.66 | 3 | 1.50 | 0.23 | 1.5 | 2.04 | 0.5 | 0.84 | 0.18 | 4.3 | 8.4 | 96.5% | | 89.0 | 85.9 |
| 6.5 | 6.5 | 4.32 | 3.5 | 1.80 | 0.25 | 2.5 | 2.58 | 1 | 1.08 | 0.19 | 4.5 | 8.9 | 97.1% | | 117.0 | 113.6 |
| 7 | 8.5 | 4.98 | 3.5 | 2.10 | 0.26 | 4 | 3.24 | 1 | 1.38 | 0.21 | 4.8 | 9.5 | 97.5% | | 148.0 | 144.4 |
| 7.5 | 12 | 5.76 | 4 | 2.40 | 0.29 | 6.5 | 3.96 | 1.5 | 1.68 | 0.23 | 5.2 | 10.4 | 97.8% | | 182.0 | 178.0 |
| 8 | 16 | 6.60 | 4.5 | 2.76 | 0.33 | 9.5 | 4.80 | 1.5 | 2.04 | 0.26 | 5.7 | 11.6 | 98.0% | | 216.0 | 211.7 |
| 8.5 | 21 | 7.56 | 4.5 | 3.12 | 0.37 | 14 | 5.82 | 2 | 2.46 | 0.30 | 6.5 | 13.1 | 98.1% | | 251.0 | 246.3 |
| 9 | 27.5 | 8.58 | 5 | 3.48 | 0.42 | 20 | 7.02 | 2.5 | 2.88 | 0.34 | 7.5 | 15.1 | 98.2% | | 286.0 | 280.8 |
| 9.5 | 35 | 9.78 | 5 | 3.48 | 0.47 | 28 | 8.40 | 3 | 3.42 | 0.41 | 8.8 | 17.6 | 98.2% | | 316.0 | 310.3 |
| 10 | 44 | 11.10 | 5.5 | 3.48 | 0.53 | 39 | 10.02 | 4 | 3.48 | 0.49 | 10.6 | 20.8 | 98.2% | | 346.0 | 339.6 |
| 10.5 | 54 | 12.72 | 7.5 | 3.48 | 0.62 | 53 | 12.12 | 4.5 | 3.48 | 0.59 | 12.9 | 24.9 | 98.1% | | 371.0 | 364.0 |
| 11 | 66.5 | 14.82 | 9.5 | 3.48 | 0.72 | 70 | 14.46 | 5.5 | 3.48 | 0.71 | 15.5 | 29.8 | 98.0% | | 387.0 | 379.3 |
| 11.5 | 74 | 16.14 | 11 | 3.48 | 0.78 | 79 | 15.72 | 6 | 3.48 | 0.78 | 16.8 | 32.3 | 97.9% | | 358.0 | 350.7 |
| 12 | 74 | 16.14 | 11 | 3.48 | 0.78 | 79 | 15.72 | 6 | 3.48 | 0.78 | 16.8 | 32.3 | 97.9% | | 322.0 | 315.4 |
| 12.5 | 74 | 16.14 | 11 | 3.48 | 0.78 | 79 | 15.72 | 6 | 3.48 | 0.78 | 16.8 | 32.3 | 97.9% | | 287.0 | 281.1 |
| 13 | 74 | 16.14 | 11 | 3.48 | 0.78 | 79 | 15.72 | 6 | 3.48 | 0.78 | 16.8 | 32.3 | 97.9% | | 254.0 | 248.8 |
| 13.5 | 74 | 16.14 | 11 | 3.48 | 0.78 | 79 | 15.72 | 6 | 3.48 | 0.78 | 16.8 | 32.3 | 97.9% | | 223.0 | 218.4 |
| 14 | 74 | 16.14 | 11 | 3.48 | 0.78 | 79 | 15.72 | 6 | 3.48 | 0.78 | 16.8 | 32.3 | 97.9% | | 194.0 | 190.0 |
| 14.5 | 74 | 16.14 | 11 | 3.48 | 0.78 | 79 | 15.72 | 6 | 3.48 | 0.78 | 16.8 | 32.3 | 97.9% | | 168.0 | 164.6 |
| 15 | 74 | 16.14 | 11 | 3.48 | 0.78 | 79 | 15.72 | 6 | 3.48 | 0.78 | 16.8 | 32.3 | 97.9% | | 144.0 | 141.0 |
| 15.5 | 74 | 16.14 | 11 | 3.48 | 0.78 | 79 | 15.72 | 6 | 3.48 | 0.78 | 16.8 | 32.3 | 97.9% | | 122.0 | 119.5 |
| 16 | 74 | 16.14 | 11 | 3.48 | 0.78 | 79 | 15.72 | 6 | 3.48 | 0.78 | 16.8 | 32.3 | 97.9% | | 103.0 | 100.9 |
| 16.5 | 74 | 16.14 | 11 | 3.48 | 0.78 | 79 | 15.72 | 6 | 3.48 | 0.78 | 16.8 | 32.3 | 97.9% | | 87.0 | 85.2 |
| 17 | 74 | 16.14 | 11 | 3.48 | 0.78 | 79 | 15.72 | 6 | 3.48 | 0.78 | 16.8 | 32.3 | 97.9% | | 72.0 | 70.5 |
| 17.5 | 74 | 16.14 | 11 | 3.48 | 0.78 | 79 | 15.72 | 6 | 3.48 | 0.78 | 16.8 | 32.3 | 97.9% | | 60.0 | 58.8 |
| 18 | 74 | 16.14 | 11 | 3.48 | 0.78 | 79 | 15.72 | 6 | 3.48 | 0.78 | 16.8 | 32.3 | 97.9% | | 49.0 | 48.0 |
| 18.5 | 74 | 16.14 | 11 | 3.48 | 0.78 | 79 | 15.72 | 6 | 3.48 | 0.78 | 16.8 | 32.3 | 97.9% | | 40.0 | 39.2 |
| 19 | 74 | 16.14 | 11 | 3.48 | 0.78 | 79 | 15.72 | 6 | 3.48 | 0.78 | 16.8 | 32.3 | 97.9% | | 32.0 | 31.3 |
| 19.5 | 74 | 16.14 | 11 | 3.48 | 0.78 | 79 | 15.72 | 6 | 3.48 | 0.78 | 16.8 | 32.3 | 97.9% | | 26.0 | 25.5 |
| 20 | 74 | 16.14 | 11 | 3.48 | 0.78 | 79 | 15.72 | 6 | 3.48 | 0.78 | 16.8 | 32.3 | 97.9% | | 21.0 | 20.6 |
| 20.5 | 74 | 16.14 | 11 | 3.48 | 0.78 | 79 | 15.72 | 6 | 3.48 | 0.78 | 16.8 | 32.3 | 97.9% | | 16.0 | 15.7 |
| 21 | 74 | 16.14 | 11 | 3.48 | 0.78 | 79 | 15.72 | 6 | 3.48 | 0.78 | 16.8 | 32.3 | 97.9% | | 13.0 | 12.7 |
| 21.5 | 74 | 16.14 | 11 | 3.48 | 0.78 | 79 | 15.72 | 6 | 3.48 | 0.78 | 16.8 | 32.3 | 97.9% | | 10.0 | 9.8 |
| 22 | 74 | 16.14 | 11 | 3.48 | 0.78 | 79 | 15.72 | 6 | 3.48 | 0.78 | 16.8 | 32.3 | 97.9% | | 8.0 | 7.8 |
| 22.5 | 74 | 16.14 | 11 | 3.48 | 0.78 | 79 | 15.72 | 6 | 3.48 | 0.78 | 16.8 | 32.3 | 97.9% | | 6.0 | 5.9 |
| 23 | 74 | 16.14 | 11 | 3.48 | 0.78 | 79 | 15.72 | 6 | 3.48 | 0.78 | 16.8 | 32.3 | 97.9% | | 5.0 | 4.9 |
| 23.5 | 74 | 16.14 | 11 | 3.48 | 0.78 | 79 | 15.72 | 6 | 3.48 | 0.78 | 16.8 | 32.3 | 97.9% | | 4.0 | 3.9 |
| 24 | 74 | 16.14 | 11 | 3.48 | 0.78 | 79 | 15.72 | 6 | 3.48 | 0.78 | 16.8 | 32.3 | 97.9% | | 3.0 | 2.9 |
| 24.5 | 74 | 16.14 | 11 | 3.48 | 0.78 | 79 | 15.72 | 6 | 3.48 | 0.78 | 16.8 | 32.3 | 97.9% | | 2.0 | 2.0 |
| 25 | 74 | 16.14 | 11 | 3.48 | 0.78 | 79 | 15.72 | 6 | 3.48 | 0.78 | 16.8 | 32.3 | 97.9% | | 1.0 | 1.0 |
| 25.5 | 74 | 16.14 | 11 | 3.48 | 0.78 | 79 | 15.72 | 6 | 3.48 | 0.78 | 16.8 | 32.3 | 97.9% | | 1.0 | 1.0 |
| 26 | 74 | 16.14 | 11 | 3.48 | 0.78 | 79 | 15.72 | 6 | 3.48 | 0.78 | 16.8 | 32.3 | 97.9% | | 1.0 | 1.0 |
| 26.5 | 74 | 16.14 | 11 | 3.48 | 0.78 | 79 | 15.72 | 6 | 3.48 | 0.78 | 16.8 | 32.3 | 97.9% | | 1.0 | 1.0 |
| 27 | 74 | 16.14 | 11 | 3.48 | 0.78 | 79 | 15.72 | 6 | 3.48 | 0.78 | 16.8 | 32.3 | 97.9% | | 0.0 | 0.0 |
| 27.5 | 74 | 16.14 | 11 | 3.48 | 0.78 | 79 | 15.72 | 6 | 3.48 | 0.78 | 16.8 | 32.3 | 97.9% | | 0.0 | 0.0 |
| 28 | 74 | 16.14 | 11 | 3.48 | 0.78 | 79 | 15.72 | 6 | 3.48 | 0.78 | 16.8 | 32.3 | 97.9% | | 0.0 | 0.0 |
| 28.5 | 74 | 16.14 | 11 | 3.48 | 0.78 | 79 | 15.72 | 6 | 3.48 | 0.78 | 16.8 | 32.3 | 97.9% | | 0.0 | 0.0 |
| 29 | 74 | 16.14 | 11 | 3.48 | 0.78 | 79 | 15.72 | 6 | 3.48 | 0.78 | 16.8 | 32.3 | 97.9% | | 0.0 | 0.0 |
| 29.5 | 74 | 16.14 | 11 | 3.48 | 0.78 | 79 | 15.72 | 6 | 3.48 | 0.78 | 16.8 | 32.3 | 97.9% | | 0.0 | 0.0 |
| 30 | 74 | 16.14 | 11 | 3.48 | 0.78 | 79 | 15.72 | 6 | 3.48 | 0.78 | 16.8 | 32.3 | 97.9% | | 0.0 | 0.0 |
| | | | | | | | | | | | | | | | 5.48E+03 | 5.36E+03 |
| | | | | | | | | | | | | | | | | 97.86% |

## Table 10. Converter Efficiency for Baseline with SiC Schottkys, 3 kHz

| Wind Speed (m/s) | Gen Inv IGBT Cond Loss (w) | Gen Inv IGBT Sw loss (w) | Gen Inv Diode Cond Loss (w) | Gen Inv Diode Sw loss (w) | Gen Inv loss (per inv) (kW) | Util Inv IGBT Cond Loss (w) | Util Inv IGBT Sw loss (w) | Util Inv Diode Cond Loss (w) | Util Inv Diode Sw loss (w) | Util Inv Loss (per inv) (kW) | Filter Loss (kW) | Total Loss (kW) | Total PE Eff. | | Energy Prod for Weighting | Energy Times Eff |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | | | | | | | |
| 3 | 18 | 24 | 10 | 8 | 3.359 | 6 | 6 | 1 | 8 | 3.124 | 4.0 | 17.0 | 40.5% | | 0.0 | 0.0 |
| 3.5 | 26 | 34 | 13 | 8 | 3.490 | 10 | 10 | 2 | 8 | 3.180 | 4.0 | 17.3 | 62.9% | | 1.0 | 0.6 |
| 4 | 36 | 45 | 17 | 8 | 3.637 | 16 | 16 | 3 | 8 | 3.254 | 4.0 | 17.8 | 74.8% | | 10.0 | 7.5 |
| 4.5 | 47 | 57 | 21 | 8 | 3.805 | 23 | 23 | 4 | 8 | 3.349 | 4.0 | 18.4 | 81.8% | | 23.0 | 18.8 |
| 5 | 61 | 71 | 25 | 9 | 3.999 | 33 | 32 | 5 | 8 | 3.470 | 4.1 | 19.0 | 86.3% | | 41.0 | 35.4 |
| 5.5 | 78 | 87 | 29 | 9 | 4.215 | 45 | 43 | 7 | 8 | 3.619 | 4.2 | 19.8 | 89.3% | | 63.0 | 56.3 |
| 6 | 97 | 103 | 34 | 9 | 4.458 | 60 | 56 | 10 | 8 | 3.801 | 4.3 | 20.8 | 91.4% | | 89.0 | 81.4 |
| 6.5 | 119 | 122 | 38 | 9 | 4.729 | 78 | 71 | 12 | 9 | 4.019 | 4.5 | 22.0 | 92.9% | | 117.0 | 108.7 |
| 7 | 145 | 142 | 42 | 10 | 5.029 | 99 | 89 | 16 | 9 | 4.279 | 4.7 | 23.4 | 93.9% | | 148.0 | 139.0 |
| 7.5 | 174 | 163 | 46 | 10 | 5.361 | 125 | 110 | 20 | 9 | 4.586 | 5.1 | 25.0 | 94.7% | | 182.0 | 172.4 |
| 8 | 208 | 187 | 50 | 10 | 5.727 | 156 | 134 | 24 | 9 | 4.946 | 5.7 | 27.0 | 95.3% | | 216.0 | 205.9 |
| 8.5 | 246 | 211 | 54 | 10 | 6.129 | 194 | 161 | 29 | 10 | 5.365 | 6.4 | 29.4 | 95.8% | | 251.0 | 240.4 |
| 9 | 289 | 238 | 57 | 11 | 6.569 | 238 | 192 | 35 | 10 | 5.851 | 7.5 | 32.3 | 96.1% | | 286.0 | 274.8 |
| 9.5 | 337 | 265 | 60 | 11 | 7.039 | 289 | 226 | 42 | 11 | 6.403 | 8.8 | 35.7 | 96.3% | | 316.0 | 304.4 |
| 10 | 393 | 294 | 62 | 12 | 7.563 | 349 | 264 | 50 | 11 | 7.046 | 10.5 | 39.7 | 96.5% | | 346.0 | 333.9 |
| 10.5 | 455 | 325 | 64 | 12 | 8.134 | 421 | 306 | 59 | 12 | 7.785 | 12.8 | 44.6 | 96.6% | | 371.0 | 358.4 |
| 11 | 529 | 364 | 70 | 13 | 8.853 | 497 | 348 | 68 | 12 | 8.554 | 15.4 | 50.2 | 96.6% | | 387.0 | 374.0 |
| 11.5 | 569 | 385 | 75 | 13 | 9.251 | 533 | 367 | 72 | 13 | 8.915 | 16.7 | 53.0 | 96.6% | | 358.0 | 346.0 |
| 12 | 569 | 385 | 75 | 13 | 9.251 | 533 | 367 | 72 | 13 | 8.915 | 16.7 | 53.0 | 96.6% | | 322.0 | 311.2 |
| 12.5 | 569 | 385 | 75 | 13 | 9.251 | 533 | 367 | 72 | 13 | 8.915 | 16.7 | 53.0 | 96.6% | | 287.0 | 277.3 |
| 13 | 569 | 385 | 75 | 13 | 9.251 | 533 | 367 | 72 | 13 | 8.915 | 16.7 | 53.0 | 96.6% | | 254.0 | 245.5 |
| 13.5 | 569 | 385 | 75 | 13 | 9.251 | 533 | 367 | 72 | 13 | 8.915 | 16.7 | 53.0 | 96.6% | | 223.0 | 215.5 |
| 14 | 569 | 385 | 75 | 13 | 9.251 | 533 | 367 | 72 | 13 | 8.915 | 16.7 | 53.0 | 96.6% | | 194.0 | 187.5 |
| 14.5 | 569 | 385 | 75 | 13 | 9.251 | 533 | 367 | 72 | 13 | 8.915 | 16.7 | 53.0 | 96.6% | | 168.0 | 162.4 |
| 15 | 569 | 385 | 75 | 13 | 9.251 | 533 | 367 | 72 | 13 | 8.915 | 16.7 | 53.0 | 96.6% | | 144.0 | 139.2 |
| 15.5 | 569 | 385 | 75 | 13 | 9.251 | 533 | 367 | 72 | 13 | 8.915 | 16.7 | 53.0 | 96.6% | | 122.0 | 117.9 |
| 16 | 569 | 385 | 75 | 13 | 9.251 | 533 | 367 | 72 | 13 | 8.915 | 16.7 | 53.0 | 96.6% | | 103.0 | 99.5 |
| 16.5 | 569 | 385 | 75 | 13 | 9.251 | 533 | 367 | 72 | 13 | 8.915 | 16.7 | 53.0 | 96.6% | | 87.0 | 84.1 |
| 17 | 569 | 385 | 75 | 13 | 9.251 | 533 | 367 | 72 | 13 | 8.915 | 16.7 | 53.0 | 96.6% | | 72.0 | 69.6 |
| 17.5 | 569 | 385 | 75 | 13 | 9.251 | 533 | 367 | 72 | 13 | 8.915 | 16.7 | 53.0 | 96.6% | | 60.0 | 58.0 |
| 18 | 569 | 385 | 75 | 13 | 9.251 | 533 | 367 | 72 | 13 | 8.915 | 16.7 | 53.0 | 96.6% | | 49.0 | 47.4 |
| 18.5 | 569 | 385 | 75 | 13 | 9.251 | 533 | 367 | 72 | 13 | 8.915 | 16.7 | 53.0 | 96.6% | | 40.0 | 38.7 |
| 19 | 569 | 385 | 75 | 13 | 9.251 | 533 | 367 | 72 | 13 | 8.915 | 16.7 | 53.0 | 96.6% | | 32.0 | 30.9 |
| 19.5 | 569 | 385 | 75 | 13 | 9.251 | 533 | 367 | 72 | 13 | 8.915 | 16.7 | 53.0 | 96.6% | | 26.0 | 25.1 |
| 20 | 569 | 385 | 75 | 13 | 9.251 | 533 | 367 | 72 | 13 | 8.915 | 16.7 | 53.0 | 96.6% | | 21.0 | 20.3 |
| 20.5 | 569 | 385 | 75 | 13 | 9.251 | 533 | 367 | 72 | 13 | 8.915 | 16.7 | 53.0 | 96.6% | | 16.0 | 15.5 |
| 21 | 569 | 385 | 75 | 13 | 9.251 | 533 | 367 | 72 | 13 | 8.915 | 16.7 | 53.0 | 96.6% | | 13.0 | 12.6 |
| 21.5 | 569 | 385 | 75 | 13 | 9.251 | 533 | 367 | 72 | 13 | 8.915 | 16.7 | 53.0 | 96.6% | | 10.0 | 9.7 |
| 22 | 569 | 385 | 75 | 13 | 9.251 | 533 | 367 | 72 | 13 | 8.915 | 16.7 | 53.0 | 96.6% | | 8.0 | 7.7 |
| 22.5 | 569 | 385 | 75 | 13 | 9.251 | 533 | 367 | 72 | 13 | 8.915 | 16.7 | 53.0 | 96.6% | | 6.0 | 5.8 |
| 23 | 569 | 385 | 75 | 13 | 9.251 | 533 | 367 | 72 | 13 | 8.915 | 16.7 | 53.0 | 96.6% | | 5.0 | 4.8 |
| 23.5 | 569 | 385 | 75 | 13 | 9.251 | 533 | 367 | 72 | 13 | 8.915 | 16.7 | 53.0 | 96.6% | | 4.0 | 3.9 |
| 24 | 569 | 385 | 75 | 13 | 9.251 | 533 | 367 | 72 | 13 | 8.915 | 16.7 | 53.0 | 96.6% | | 3.0 | 2.9 |
| 24.5 | 569 | 385 | 75 | 13 | 9.251 | 533 | 367 | 72 | 13 | 8.915 | 16.7 | 53.0 | 96.6% | | 2.0 | 1.9 |
| 25 | 569 | 385 | 75 | 13 | 9.251 | 533 | 367 | 72 | 13 | 8.915 | 16.7 | 53.0 | 96.6% | | 1.0 | 1.0 |
| 25.5 | 569 | 385 | 75 | 13 | 9.251 | 533 | 367 | 72 | 13 | 8.915 | 16.7 | 53.0 | 96.6% | | 1.0 | 1.0 |
| 26 | 569 | 385 | 75 | 13 | 9.251 | 533 | 367 | 72 | 13 | 8.915 | 16.7 | 53.0 | 96.6% | | 1.0 | 1.0 |
| 26.5 | 569 | 385 | 75 | 13 | 9.251 | 533 | 367 | 72 | 13 | 8.915 | 16.7 | 53.0 | 96.6% | | 1.0 | 1.0 |
| 27 | 569 | 385 | 75 | 13 | 9.251 | 533 | 367 | 72 | 13 | 8.915 | 16.7 | 53.0 | 96.6% | | 0.0 | 0.0 |
| 27.5 | 569 | 385 | 75 | 13 | 9.251 | 533 | 367 | 72 | 13 | 8.915 | 16.7 | 53.0 | 96.6% | | 0.0 | 0.0 |
| 28 | 569 | 385 | 75 | 13 | 9.251 | 533 | 367 | 72 | 13 | 8.915 | 16.7 | 53.0 | 96.6% | | 0.0 | 0.0 |
| 28.5 | 569 | 385 | 75 | 13 | 9.251 | 533 | 367 | 72 | 13 | 8.915 | 16.7 | 53.0 | 96.6% | | 0.0 | 0.0 |
| 29 | 569 | 385 | 75 | 13 | 9.251 | 533 | 367 | 72 | 13 | 8.915 | 16.7 | 53.0 | 96.6% | | 0.0 | 0.0 |
| 29.5 | 569 | 385 | 75 | 13 | 9.251 | 533 | 367 | 72 | 13 | 8.915 | 16.7 | 53.0 | 96.6% | | 0.0 | 0.0 |
| 30 | 569 | 385 | 75 | 13 | 9.251 | 533 | 367 | 72 | 13 | 8.915 | 16.7 | 53.0 | 96.6% | | 0.0 | 0.0 |
| | | | | | | | | | | | | | | | 5.48E+03 | 5.26E+03 |
| | | | | | | | | | | | | | | | | 95.92% |

The second way of explaining the high forward conduction drop is that the dominating loss mechanisms for IGBTs and MOSFETs are different in some respects. The voltage drop across an IGBT (1,200 V device in a 480 VAC converter) does not increase linearly with current, but varies within a fairly narrow range from, say, 2 to 3 V. However, the voltage drop across a MOSFET (also a 1,200 V device in a 480 V converter) would increase nearly linearly with current from essentially zero to perhaps 6 V. Therefore, the SiC MOSFET actually has significantly lower forward conduction losses at low power where a wind turbine operates most of the time. Total converter efficiency with the SiC MOSFETs actually peaks well below half power and then falls slightly as power continues to increase, reflecting the increasing conduction loss. The change from an IGBT to MOSFET type of device particularly benefits the low power range.

This resistance characteristic for the SiC MOSFET gives rise to another strategy in the design. The designer can halve the losses by doubling the device area. This is not possible with IGBTs. The SiC MOSFETs tested in this project were pushed fairly hard (to a current density of around 200 $A/cm^2$), which gives maximum conduction losses. Increasing the device area does not create any other hardware cost; in fact, the heat sink material is actually decreased in amount due to lower losses. This strategy seems inappropriate at a time when device area is severely limited by defect density in SiC wafers, but the problem will eventually be solved. Designers of converters using silicon MOSFETs exploit this technique often to reduce forward losses in low voltage systems.

SiC enables most devices to be increased greatly in voltage rating compared to silicon due to the order of magnitude increase in breakdown voltage of the blocking layer. No attempt has been made to estimate losses with 10,000 V SiC MOSFETs (feasible) operating at 4,160 VAC. No test information was produced in this project, nor is any other test data available to the author, that would form a reasonable basis for estimating either conduction or switching losses in such devices. However, it is expected that a significant further reduction in conduction losses would occur, making SiC devices even more attractive from a performance and size standpoint. The design of a simple 6-device inverter that operates at 4,160 VAC is one of the primary recommendations resulting from this project.

Therefore, the author believes reducing the forward losses by a factor of two is justified by 1) improvements currently being made in the forward resistance of SiC MOSFETs, 2) potential increases in the device area and associated reductions in current density by the converter designer, and 3) use of much higher voltages.

Table 10 is an attempt to calculate efficiency when using a silicon IGBT with a SiC Schottky diode rather than the normal silicon PN diode. Research indicates this will reduce total switching losses in both the transistors and diodes from 30% to 50% due to the extraordinary reduction in reverse recovery current in the SiC Schottky. In Table 10, a fixed 40% of the switching losses was removed at all power levels. This strategy favors the low power range, where the reverse recovery losses are a relatively higher fraction of the losses. However, Peregrine did not have sufficient data to determine the actual loss reduction for each power level. A more accurate approach would probably show a somewhat higher average efficiency. The use of a SiC Schottky

diode with a silicon IGBT represents the minimum use SiC devices. It will not allow the designer to take advantage of the high temperature or high-voltage capability of SiC, but it does realize some of the high speed switching benefits. The standard silicon PN diode is easily replaced with the SiC Schottky. In fact, this type of configuration is now being developed commercially by at least two major device suppliers.

Finally, one should note that the baseline converter efficiency is already quite high: 95.5% average and 96.2% at full power. With only 4.5% in losses, not much loss reduction is really achievable. Since about 1% of this is in the filter inductor, there is only about 3.5% available with the SiC devices. The best projected average SiC efficiency shown in Table 9 is 97.9% and the best efficiency at full power is the same at 97.9%. The 2.4% increase with SiC is good, but it is not the expected 5% to 6%.

The small efficiency differences and the importance of being accurate in the low power area presents questions about the methodologies employed. Computational models generally give reasonable overall trends and magnitudes, but they often do not deal well with the boundary conditions (low power here). The low power scenario has been represented by models for the rotor, gearbox, generator, and converter. None of these will necessarily compute fringe numbers accurately, nor was this their purpose. The low power region will likely become even more important in the future if direct drive PM generators are used. These will eliminate the gearbox efficiency curve, which dives to zero at low speed, and enable the use of generator designs that have their peak efficiency at power levels well below their maximum rating. While the numerical impact of PM generators is not yet known, it is clear that the gain in energy production from SiC will be improved. This result is consistent with NREL's long term objective to improve the economics of wind turbines at low wind speed sites.

# 5.0 APPLICATION OF SiC DEVICES

## 5.1 Introduction

When the project commenced, the team believed that, in time, SiC devices might eventually displace all silicon devices in power electronics in the broadest industrial markets. Those markets include motor drives; uninterruptible power supplies; industrial power supplies for metal coating, heating, and welding as well as large wind turbines in the power range from one kW to several megawatts. In the U.S., these products are often designed for a 480 V, three-phase environment. North America also supplies 575 V, and Europe and some other parts of the world supply industrial three-phase power at 400 and 690 V. This project used 690 V because it was specified for the baseline wind turbine.

At the high end of the power spectrum, some products are designed for medium voltage, typically 2,300 V or 4,160 V. Medium voltage is subject to an entirely different set of safety codes. The definition of medium voltage is sometimes extended to include the utility distribution voltage, which falls in the range of 10,000 to 20,000V, with 12,500 V being the standard in the United States. Generation, even in the largest power plants, is often at 13,800 V, which is sometimes classified as medium voltage. Medium voltage was not expected to be of great interest in this project, but that has changed.

Some researchers have stated that SiC devices will simply cost too much to widely displace silicon devices. This view is based on the challenge of finding solutions to the many technical problems associated with SiC and a reluctance to accept the proposition that SiC cost can ever be competitive to silicon. A comparison today is misleading because silicon technologies have developed over a 40-year period; the resulting devices are inexpensive and almost defect free. The author has a different, largely unsupported opinion about cost. No product is subject to the impact of yields and economies of scale as much as the semiconductor. Hard work and creative minds driven by competitive pressure to improve products in the electronics market, will chip away at the problems until in 20 years or so SiC power semiconductors will be cost competitive and dominate.

The question in this project is whether SiC devices can be applied advantageously prior to that time, particularly the converter used in wind turbines. To answer that question, one must expand the definition of cost competitiveness beyond just the device. The definition must also include the impact of SiC on an entire system, including the size, performance, and cost of all other system components. Here, the unique attributes of SiC must be identified and discussed. The unique characteristics of SiC as a wide band-gap material stand out: high temperature, high voltage (power), and high switching speed. Each of these will be discussed next.

## 5.2 High Temperature

High temperature electronics are increasing markedly in importance. The total market for high power electronics is expected to be nearly $1 billion in 2008. High temperature electronics have a leverage effect by increasing the capabilities of many larger systems. Silicon in power devices is limited to less than 150°C and manufacturers routinely limit operation to 125°C. SOI (silicon

on insulator) techniques can raise that limit for signal level devices to well above 200°C with a potential of raising that limit to over 250°C. However, those techniques are not feasible in high power devices. When it comes to power semiconductors, temperature increases are at an end with silicon.

Where high temperature operation is necessary, SiC devices might be the only acceptable option for high power levels because they (not SiC MOSFETs) can operate at over 400°C. This capability is a direct result of being a wide band-gap material. As temperature is increased, a number of physical processes increase in intensity to interfere with the operation of a device, as intended by the designer. These include an increase in intrinsic carriers, increase in P-N junction leakage, increase in thermionic leakage, and decrease in carrier mobility. A wide band-gap causes these processes to be less intense at any given temperature, so higher temperatures will be necessary for unacceptable levels of intensity to be reached.

Currently, the primary applications driving high temperature electronics development include vehicles, space and aviation, and deep well drilling.

## 5.3 High Voltage (High Power)

Higher breakdown voltage is another consequence of wide band-gap material and leads directly to much higher-voltage devices. The prospect of single devices that can withstand 5,000 to 40,000 V is very appealing in high power systems. Currently, achieving medium voltage in silicon IGBTs requires multilevel converters, or the stacking or cascading of multiple inverter modules. A simple 6-device inverter that operates with high switching frequency at 4,160 VAC (requires a 10,000 V device) would make a serious impact on size, cost, and reliability.

In the 400 to 690 V range, some SiC reduction in conduction losses may occur, but it will not be dramatically lower compared to its silicon counterpart. The results so far do not show a significant reduction in conduction losses. However, higher voltage leads to significantly lower conduction losses no matter what device is used, and SiC makes the higher voltage possible. A significant forward conduction loss at 690 V might be insignificant at 4,160 V.

Theoretically, the resistance of the blocking layer in a power semiconductor increases as the voltage blocking capability is increased. In fact, for most devices, the resistance increases with the square of the voltage. However, this is quite misleading in predicting the practical result. The conduction loss is proportional to the square of the current, which decreases inversely with the increase in voltage. The conduction loss determined by this simple analysis would thus remain the same. However, the device has regions other than the blocking layer where the resistance does not increase commensurately with the voltage. The practical outcome of increasing voltage is usually quite favorable.

Some examples of what happens to forward voltage drop when the voltage is increased will be enlightening. A major supplier of IGBTs reports the forward voltage drop to be 3.4 V in one of its 1,200 V devices and 5.3 V in its 6,500 V device. Another supplier reports the forward voltage drop to be 2.4 V in a 1,200 V IGBT and 3.3 V in a 4,500 V IGBT. The higher-voltage devices obviously must be thicker, causing more forward resistance, but the conduction loss is not

commensurate with the increase in voltage. One can readily project substantial reductions in conduction loss when operating at 4,160 V rather than 480 V. A similar reduction in forward voltage drop should occur with SiC. In extremely high-voltage situations (for example, over 500 kV), converters using strings of thyristors have efficiencies nearing 100%. The primary benefit from SiC may not be a reduction in conduction losses relative to a comparable silicon device, but rather the capability of using a higher voltage that reduces conduction losses.

One of the major negative implications of targeting SiC at higher voltages is longer development time. If a commercial 1,200 V MOSFET will be available in 2 years, a commercial 10,000 V SiC MOSFET would surely require 2 more years. However, there is considerable work being carried out in this area today by the Office of Naval Research and DARPA.

## 5.4 High Switching Frequency

Higher switching speeds are achieved with SiC for two reasons: (1) the higher speed, lower loss, switching properties of SiC devices, and (2) the ability to use faster switching types of devices at higher voltages. Silicon MOSFETs have excellent switching characteristics but are limited to lower voltages and currents. With SiC, the MOSFET might be designed for operation up to 10,000 V, making its superior switching characteristics available at industrial voltages for the first time.

Whether the improved switching speed is financially beneficial, depends on the application. For example, in a typical 2-quadrant drive, which comprises well over 90% of the drive market, there is no supplemental filter whose size would be reduced by higher switching frequency. The only filtering is provided by the inductance of the motor. The inductance is determined entirely by the motor requirements and that inductance generally is adequate for current smoothing with the switching speeds now found in drives. Without the need for higher speed switching, the designer would have to look elsewhere for a reason to use SiC devices rather than the standard silicon IGBTs.

## 5.5 Wind Turbine Applications

### *5.5.1 High Voltage Aspects*

The baseline turbine for this project is 1.5 MW, but utility-scale turbines are offered up to at least 3.4 MW. With full power conditioning in the variable-speed system, the necessary converters need to be rated the same as the turbine. Increasing the voltage from 690 V to the medium-voltage range makes sense at any rating over 1 MW. That this has not happened already in the wind industry is surprising. Higher voltages reduce current levels inversely, along with the size of all current carrying components – generator, wires, relays and breakers. The most common medium voltages in industry in North America are 2,300 V and 4,160 V, for which many standard components and products are available.

Medium-voltage components require more material for electrical insulation, and they must withstand more extreme electrical events and tougher safety codes. But the cost of these is generally more than offsets by the substantial reduction in material. The tradeoff analysis

associated with using medium voltage was not part of the statement of work in this project. Also not part of the statement of work is the projection of the performance and cost of a converter rated at medium voltage, using for example 10,000 V SiC devices. However, that type of analysis is highly recommended for subsequent work.

Based on the physics of power devices in general, and SiC power devices in particular, it is almost certain that conduction losses will be significantly reduced as the voltage is increased. The modest reduction in conduction losses at 480 V and 690 V, as measured in this project for SiC, would be improved considerably (perhaps to the expected result) with an increase in voltage. With the increases seen in the ratings of commercial utility-scale wind turbines, there is a natural incentive to increase voltage anyway, so there is a convergence of strategies. The capability to design very compact, six-device, high speed switching inverters at medium voltage is uniquely enabled by SiC. This is one of the most useful conclusions reached in the project. The full impact of this conclusion will be seen later where the potential size of a medium-voltage inverter is shown.

The use of higher voltages with SiC devices leads to other possibilities. Today, the Navy is attempting to develop core power distribution equipment (a substation) for future ships using SiC power devices. Navy generators would supply power at 13,800 VAC to be distributed at 4,160 VAC and 450 VAC. The power electronics might operate at 13,800 VAC, 4,160 VAC, or 450 VAC. When fabricated of SiC, IGBTs are expected to have stopping voltages exceeding 20 kV. New and interesting approaches come to mind if power electronics converters can operate at up to 13,800 volt rms. These will be discussed later.

### *5.5.2 High Temperature Aspects*

High temperature can be beneficial in two circumstances: (1) if it is dictated by the application, as it might be in electric vehicles, high performance aircraft, or down-hole drilling, or (2) if it leads to less material and lower cost. A wind turbine application does not require a converter with a fundamental need for high temperature operation. However, temperature will be important in reducing size and cost. When higher temperature is combined with lower losses (in part due to higher voltage), the resulting inverter bridge will be perhaps one-sixth the size of a current inverter bridge, a fact that the designer should be able to translate into lower cost. How this will be done is discussed at length later.

### *5.5.3 High Switching Frequency Aspects*

Like high temperature, high speed switching in a wind turbine is not a requirement by itself. It is beneficial only if it can make passive filter components smaller and less expensive. One must first identify what types of filter elements are necessary for a variable-speed generation system with the full conditioning configuration. Generally, only a single filter inductor has been used to remove the 3 kHz PWM switching signal from the lines. Any distortion from a single wind turbine will to some extent be cancelled by distortion from other wind turbines in an array of wind turbines whose power is being collected at a common point. If the wind turbine generates alone, or power quality requirements are particularly high, an L-C-L filter might be used. Since the second L is significantly smaller than the first, and the C is not very expensive, the entire L-

C-L filter array is not much more expensive than the single large filter inductor. In any event, it is assumed here that the baseline wind turbine uses a single inductor between the converter and the grid. On the generator side of the converter, the current will be smoothed by the inductance of the generator. The baseline turbine is expected to use a PM generator, which tends to have lower inductance than other types, but it is still expected to have sufficient inductance without supplementation with another inductor or without increasing the frequency.

Another potential problem on the generator side of the converter that might require passive elements is excessive dv/dt, which is well known in the drive business as damaging to the first several turns of the stator windings of industrial motors. Increasing voltage would increase this problem. The solution is to beef up the motor (better insulation, form wound stator winding, etc.) to withstand the dv/dt beating or to insert a minimal filter to reduce dv/dt. It is difficult to analyze this problem because the voltage will undoubtedly be increased substantially and there is little data available on medium-voltage motors or generators.

The bottom line is that the converter for the baseline turbine is assumed to have an inductor on the grid side and no extra filter element on the generator side. With minimal filter elements, the potential cost benefit from a reduction in size due to an increase in switching frequency is minimal. In addition, a higher frequency itself leads to higher costs in some cases because it increases core losses and skin effect. Therefore, there are competing cost effects associated with increased switching frequency. The net outcome has not been determined in this project because, contrary to initial expectation, the frequency probably will not be increased significantly with SiC power devices. While switching losses are clearly lower with SiC, they are not negligible. They can be kept low by operating at the lowest acceptable frequency, the same criterion that is imposed by the converter designer for silicon IGBTs. It is not clear why that frequency would be much different than it is for silicon IGBTs (3 kHz). A tradeoff analysis could be carried out, but the targeted benefits will be small and would not likely swing any conclusions reached in this project. In addition, the trade off study should be carried out for the correct voltage, which will likely be much higher than the 690 V specified for the baseline turbine. Designing a high current, high frequency, medium-voltage inductor is a significant design exercise; there are no such products in the market to the author's knowledge. It is the understanding of the author that further work of this nature is being done in another NREL concept study in parallel to this project.

## 5.6 Promising New Wind Turbine Configurations Using SiC

This project has led to the conclusion that SiC devices will not be exploited to greatest advantage if they are just used as one-for-one replacements of existing silicon devices in power electronics rated at 690 V. However, SiC devices have unique characteristics that can be exploited to great advantage if the overall configuration is allowed to change. An existing baseline wind turbine should not dictate how the SiC devices are used, but rather the unique characteristics of SiC devices should dictate how the system is configured. The pertinent SiC characteristics for wind turbines are high voltage and temperature capability. Several new approaches capitalizing on the high-voltage capability are described in this section. They are not exhaustive, but rather illustrate some of the new possibilities with SiC devices. How to capitalize on the high temperature capability is covered later.

### 5.6.1 Medium Voltage with Standard Transformer

In this alternative, the baseline converter shown in Figure 1 would be made entirely of SiC MOSFETs (or SiC BJTs) and SiC PN junction diodes (or Schottkys) capable of operating at 2,300 VAC and 4,160 VAC, which requires devices that can withstand 5,500 V and 10,000 V, respectively. The generator feeding this converter, in addition to the filter inductor, would also be rated nominally at 2,300 VAC or 4,160 VAC. The converter would be connected to the grid through a standard 60 Hz transformer. The 1.5 MW of power from the baseline turbine can be handled by a single inverter bridge that carries only 208 amps and is about one-sixth the size of that required with silicon IGBTs rated for operation at 690 V rms. This relatively simple topology cannot be developed with standard silicon IGBTs and is therefore uniquely enabled by SiC.

Given DARPA and Navy work now being carried out, along with other Peregrine work, the necessary inverter bridge could be designed and tested during the next two to five years. It is impossible to be precise about the reduction in losses due to lack of real test data for high-voltage SiC devices, but a factor of three to five should be possible because of the relatively low forward conduction losses with higher voltage and significant reduction in switching losses.

### 5.6.2 Medium Voltage With High Frequency Transformer

Figure 2 shows in block form the next interesting configuration, which contains a high frequency transformer. This is a well-known approach to reducing the size of transformers, and is currently being pursued by the Navy using SiC. The general strategy is to create smooth DC with a rectifier, and then feed the transformer with a high frequency train of square AC pulses created by an H-bridge. The width of the pulses can be varied using standard PWM techniques to regulate the voltage on the output side of the transformer. The high frequency output is again rectified into smooth DC, which is inverted using PWM techniques and filtered. The frequency of the transformer in the Navy project is expected to be in the area of 20 kHz. If only transformation is required, the cost for this approach is generally higher than for a 60 Hz transformer because a number of conversion stages are needed. But since a complex converter will be used anyway in the variable-speed turbine, the overall cost for solid-state conversion plus high frequency transformation might be lower. Galvanic isolation of the turbine from the grid (probably required) is provided by the high frequency transformer.

All three of the unique characteristics of SiC devices are being exploited here (high-voltage, high switching speed, and high temperature). The system requires a significant number of passive filter elements, most of which are reduced in size by the high frequency of SiC devices. As before, high voltage and high temperature will be exploited to reduce the size of each switching bridge.

For simplicity, this configuration is not shown with an inverter against the generator. It could have such an inverter, but it is assumed here that the generator is designed to tolerate an

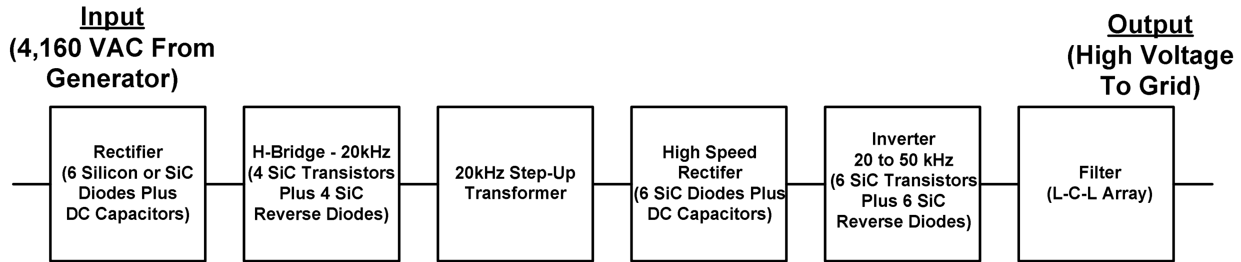



**Figure 2. High Frequency Conversion & Transformation**

uncontrolled six pulse signal imposed by the input diode bridge and that torque regulation on the generator shaft can be implemented through management of the current flow through the conversion system. This system is not bidirectional as shown. The varying voltage from the variable-speed generator can be regulated up or down by the duty cycle of the H-bridge. Further voltage regulation (down only) is available through the duty cycle of the output inverter.

It is difficult to estimate either the performance or cost of this system without further study, but it has a number of fundamental advantages, which might lead to better performance and cost compared to more conventional approaches. This approach has been enabled by SiC and could not be implemented well using silicon IGBTs. This approach could be implemented in the next two to five years.

### *5.6.3 Generation at Distribution Voltage*

The third configuration is not unusual, except that the wind turbine generates at 13,800 V, where most large generators on the grid operate. The converter can be either a two or four quadrant design depending upon pertinent tradeoffs. Although many voltages can be found on utility distribution systems, utilities are standardizing on 12,500 V. Any discrepancy between the generation and distribution can readily be reconciled by the converter, which has an effective variable in the form of duty cycle.

In this configuration, no transformation is needed for the wind turbine; it can be connected directly to a typical distribution system. If the transmission voltage must be increased for transmission to population centers, or if galvanic isolation is required, this approach would still require transformation.

This configuration is made possible through the use of SiC IGBTs, which are expected to eventually be capable of over 20,000 V, which is necessary for 13,800 VAC operation. Losses would be the lowest of all approaches due to the extraordinarily high voltage and the properties of SiC IGBTs. SiC device technology is clearly not ready for this configuration, but substantial R&D is underway. The time frame for implementing this configuration may be 10 years.

# 6.0 DEVICE AND CONVERTER PACKAGING

## 6.1 Need for High Temperature Packaging

There are two principal reasons SiC can potentially lead to a reduction in the size and cost of a converter. The first is a reduction in losses, the driver in the design of the heat removal hardware that dominates the size of the power semiconductor block in a converter. The ability to achieve a major reduction in losses using SiC is covered in other parts of this report and represents one of the major feasibility questions. The second reason SiC can potentially reduce the size and cost of a converter is its capability to operate at higher temperatures, thereby increasing the die-to-ambient temperature difference that drives the heat flux from the device. If the temperature difference is greater, less heat transfer surface is required, reducing the quantity of material in the heat removal hardware. How to achieve this favorable result with SiC is covered in this section and represents another of the major feasibility questions.

The key boundary conditions in the thermal problem are the maximum permissible temperature of the device (125°C for a standard silicon IGBT) and the temperature of the ambient air at about 50°C. Although detailed thermal calculations must be done for specific designs, one can rough out certain relationships using just the boundary condition information. As just noted, the maximum overall temperature difference for driving the heat from the device is about 75°C. If the designer increases the permissible die temperature to 200ºC, 275°C, and 350ºC, he increases the overall temperature difference by factors of 2, 3, and 4. A competent designer should be able to translate those into reductions in heat removal material by similar factors. Again, this is not a precise analysis, but the relationship is as dominant as this crude analysis would suggest. When combined with lower losses from the SiC devices, the overall size can be dramatic.

Today, all power electronics designers are pushing the limits of air cooling, the lowest cost and most reliable method for cooling power semiconductors. Air cooling also leads to the smallest size if the entire cooling system is considered, including all auxiliary cooling components in a liquid cooling system. Thermal designers already have developed heat sinks with clever fin geometries to maximize effective fin area and they know all about enhancing surface convention coefficients through turbulence and high air mass flow rates. The designer can also put exotic materials with high thermal conductivities in the thermal path between the die and the fins. But the flux is still limited at the surface by the surface area and surface convection coefficient; little or no further improvement can be made when using silicon devices with the 125°C barrier. If, on the other hand, the device temperature is allowed to increase substantially by using SiC, the surface gradient can be increased by factors of two, three, and four, thereby enhancing and re-vitalizing the potential of air cooling.

The need to carry out R&D work in this area in this project was unexpected. It was mistakenly believed that at least the major power semiconductor suppliers, who design and fabricate device packages today, would be working hard to be ready for the introduction of SiC or other wide band-gap devices. They would then have or be nearing design solutions. However, all prior work was found to be lacking and highly fragmented, and was often not aimed at the problems that need to be solved in this project. Peregrine needed to take on the role of an integrator of the technologies of others and supplement any missing pieces with its own original work.

Micro processors for computers, games, and other applications are also limited in their clock speeds by cooling techniques. While there are some differences in the thermal management problem, the packaging solutions do overlap to some extent. Therefore, Peregrine looked into some of the thermal solutions in the IC industry whose design problems have not traditionally overlapped those in power electronics.

Finally, by way of introduction, some effort has been expended by others to develop SiC packaging at 500ºC and even 600ºC, primarily for sensors that are used in or near various types of engines–jets, rockets, and reciprocating engines. These temperatures do not seem necessary for most power electronics applications, certainly not wind turbines, and push the frontiers of materials and processes to the limit. A much more feasible and practical limit is 300ºC, which is adequate to achieve the objectives set forth in this project.

## 6.2 Semiconductor Packaging Today

The basic connections and substrates in a state-of-the-art power semiconductor package are shown in Figure 3. Starting at the top of the stack, the current flows to the source through wires bonded to the top of the die. Generally the wires are made of aluminum and sonically welded to the top of the die, which has small metal plates to provide connection points. Multiple wires will generally be used not only to distribute the current more evenly over the die area, but also to reduce stray inductance. Most undesirable voltage perturbations are the result of the interaction of inductance and capacitance. The layering within a semiconductor design makes it impossible to eliminate capacitance, but the inductance can be minimized. It can easily be shown mathematically that the spreading of the current over multiple paths reduces the stray inductance. The gate drive circuit will be connected to the gate access points on the top of the die by its own wires and wire bonds in a similar way.

The surfaces of the die, as delivered by the fabricator of the die, are metalized to facilitate bonding. Bonding techniques and materials are a key ingredient to device packaging.
The die is soldered to the next substrate, which must be electrically conducting in order to provide a current path out to the external electric circuit. The material will generally be a metal, such as copper. That substrate is then soldered to another substrate that is generally not electrically conducting, so that the electrical portions of the package are isolated from the outer non-electric portions. In most device packages (IGBTs) the outer materials of the package are not energized electrically, but in other device packages (SCRs) might be energized electrically. The non-electrically conducting material might be a ceramic, such as aluminum oxide ($Al_2O_3$) or aluminum nitride (AlN). The next and final required substrate of the device package can be made of any material with high thermal conductivity–usually copper or aluminum. This provides a durable surface on the bottom and is the base plate that is attached to the heat sink.

The entire stack is then surrounded by a plastic enclosure with appropriate electrical leads protruding out for connection to the external circuit. That completes the overall semiconductor

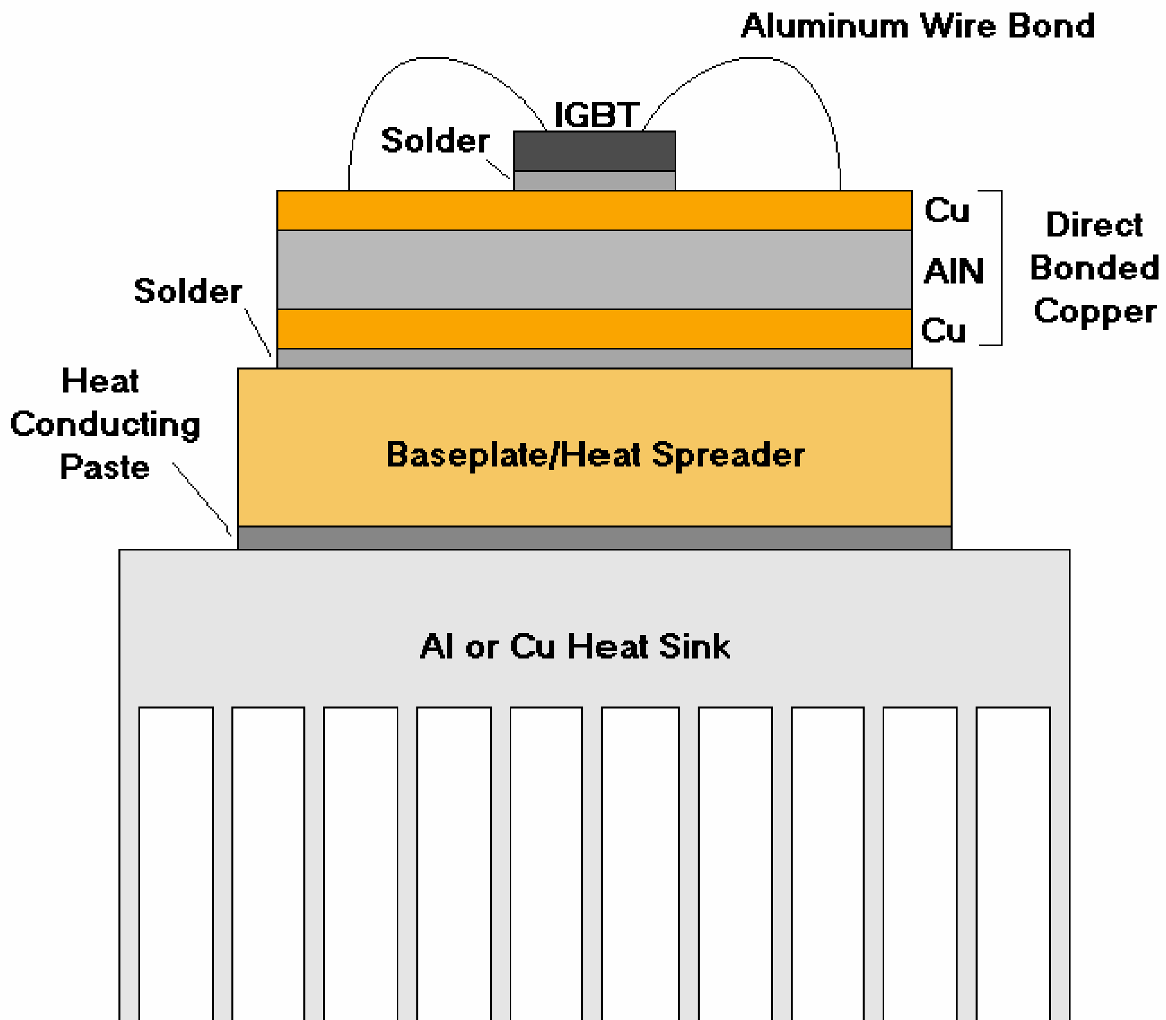



**Figure 3. Typical Semiconductor and Substrates for Silicon Devices**

package, which is now a tightly integrated and generally hermetically sealed unit. It can be used by the converter designer and fabricator in this form.

When installed in a converter, the integrated unit will be attached to a heat sink made of a material with high thermal conductivity, such aluminum. This attachment is usually done by wiping a heat conducting paste over the area of attachment and bolting the semiconductor package to the heat sink. The bolts will be spaced appropriately to distribute the bonding pressure uniformly over the attachment area and then torqued down to a specified pressure that minimizes the thickness of the paste (it generally has low conductivity), but still fills in all anomalies in the two surfaces so as to fill in the heat path completely with solid material.

All of the substrate and bonding materials were selected with several characteristics in mind: high thermal conductivity, matching CTEs, and the capability of being bonded in high volume fabrication processes. Unfortunately, not all of these characteristics are present in one material so

compromises are necessary. In a mature power semiconductor, the dominant mechanisms for failure are delamination of substrates and detachment of wire bonds, both caused by thermal cycling. Due to the mismatch in CTEs of the die and the next substrate (often copper), an intermediate layer with an intermediate CTE might be inserted to minimize the mismatch of adjacent substrates. The thermal cycling problem is accentuated if the die temperature is allowed to hit higher temperatures, as will be the case with SiC devices.

The upper temperature limits on key components, such as the solder and plastic enclosure, might only be 200ºC or so, because with the 125ºC limit of any silicon die, there is no reason to use higher temperature materials. In addition, the equipment necessary to fabricate semiconductor packages often has operating temperature limits that preclude fabrication much above 200ºC. Figure 4 is a photo of a final IGBT package ready for use in assembling a converter.

**Figure 4. Typical Power Semiconductor Packages**

## 6.3 Direct Bonded Copper

Special attention should be given to direct bonded copper (DBC). DBC is a sandwich with layers of copper on both sides of a layer of ceramic–usually $Al_2O_3$ or AlN. The bonding of these substrates is well understood and extremely effective. Although a bonding agent is used between the layers, after completion of bonding at temperature, there is essentially no residual material between the copper and ceramic, and they are highly resistant to delamination. There are at least a half dozen well-known suppliers of DBC, including Curamic (Germany), Toshiba (Japan), and IXYS (U.S.). Prices are competitive and reasonable.

DBC is a stack of substrates that can carry out precisely those functions carried out by the substrates immediately under the die shown in Figure 3. DBC is thin and has reasonably high composite thermal conductivity. The composite CTE of the overall sandwich is dominated by the

ceramic, which is close to that of the device die, so DBC is effective in improving reliability by providing a reasonably good CTE match.

Moreover, DBC offers higher temperature capability than some other approaches. It is used for a variety of things, including high temperature printed circuit boards and power semiconductors. The copper on one side can be etched in a process similar to the fabrication of an ordinary printed circuit board. That is, a designer, using one of the many available CAD tools, can lay out circuit traces on one of the copper sides, which will then be masked. The balance of the copper in that layer will be chemically etched away leaving only the desired copper traces to which components can be soldered. The DBC in that case takes the place of the typical FR4 material used for most printed circuit boards. The DBC can withstand temperatures well over 600ºC, far above the limit of typical electronic components.

Figure 5 shows a six-device inverter module known as a SKiiP, a product of Semikron of Germany. This particular module is used in a power electronics product (active filter) developed by an engineering team of the principal investigator in a prior project. In addition to the power devices, it also contains gate drive circuits with diagnostics and protection, and a heat sink with fans. DBC is used in the module in the manner described above. The bottom copper layer of the DBC here is attached to an aluminum heat sink with heat conducting paste and bolts, as described. In this project, several basic packaging concepts were studied; it is virtually a requirement that one of these concepts be based on DBC due to its current role and high temperature capability.

## 6.4 Elements of High Temperature Device Packaging

### *6.4.1 Introduction*

High temperature packaging for electronics has become an active area for worldwide R&D. Major applications, as noted earlier, include consumer products with higher microprocessor clock speeds, automobiles, civilian and military aircraft, and deep-well petrochemical drilling. There has been an explosion in the development of new materials, geometries, and processes that can contribute to this effort under the moniker of micro, pico, and nano technology. The disciplines here are as complex as those pertaining to semiconductors and SiC. Research is highly fragmented and is often being carried out for purposes entirely different than the packaging of power semiconductors. Peregrine has had to integrate several different technologies in developing high temperature device package concepts that are feasible. Other designs are undoubtedly possible with further work.

As the designer increases the temperature of the device package, various temperature limits for its components are exceeded. One can systematically replace each limiting component with a

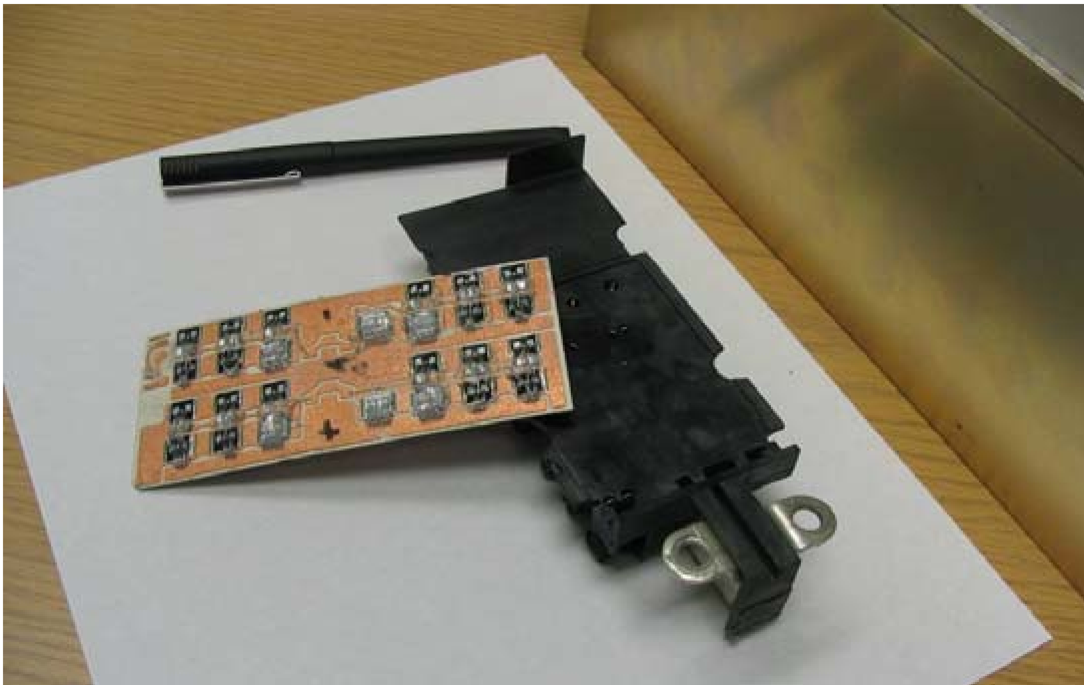


**Figure 5. Semikron SkiiP Inverter Module (Six Pack) Using DBC Substrates**

higher temperature version as he increases the temperature, but when he gets to 300°C or so (project objective), serious questions arise, particularly as to reliability. It would be straight-

forward to design a package that can operate once or a few times at 300°C, but to withstand frequency thermal cycling between the highest and lowest temperatures associated with SiC is another matter. Achieving a close CTE match is even more critical than before, but adjacent materials must also have appropriate elasticity so as to absorb some differential movement without cracking.

The high temperature device package must be completely redesigned from scratch. The designer may integrate not just the device and adjacent substrates, but also a heat sink with a better CTE. This integrated unit would be extremely small and tailored specifically to wide band-gap devices. A desirable feature would be the replacement of wire bonds with another substrate on top of the die to eliminate completely the bond wire detachment problem and permit two-sided cooling. All of these changes are believed to be feasible in time, based on discussions with knowledgeable people.

The need to start over also is dictated by another factor – a substantial increase in voltage to 2,300 V or 4,160 V, for which SiC is best adapted. That will influence the materials and geometries in the power semiconductor package design.

### *6.4.2 Materials*

Tables 11 through 14 summarize the properties of important materials to be considered in developing high temperature semiconductor packaging. These include materials that are currently used in state-of-the-art semiconductor package designs, as well as additional, new materials. It is unlikely that all potential candidate materials have been identified–too much is happening in the scientific community. With the development of composites, materials can actually be designed to meet specific objectives, such as matching CTEs. Note that the reported properties of most materials vary by a surprising amount due to differences in material structure (single crystal versus multi-crystal), manufacturing techniques and other factors.

Table 11 shows conductivity, which the designer wants to maximize in a thermal package. The standout material is CVD diamond. But this material is expensive and not shapeable; it is usable only in thin layers for specialized purposes. SiC-C (diamond) and Al-C (diamond) composites are promising candidates from strictly a conductivity point of view. SiC has high conductivity, which suggests it might be used in ways other than as a semiconductor. SiC is actually easily made and the basic ingredients are extraordinarily common. SiC has been used for decades because of its hardness and luster (carborundum blades and jewelry). BeO dust is highly toxic and has been eliminated from most designer list of candidates. Essentially all suppliers of civilian power semiconductors have ceased using BeO over the last 10 years. The old standbys of copper and aluminum are still very viable candidates in a high temperature package in places where CTE matching is not important.

**Table 11. Conductivity of Materials**

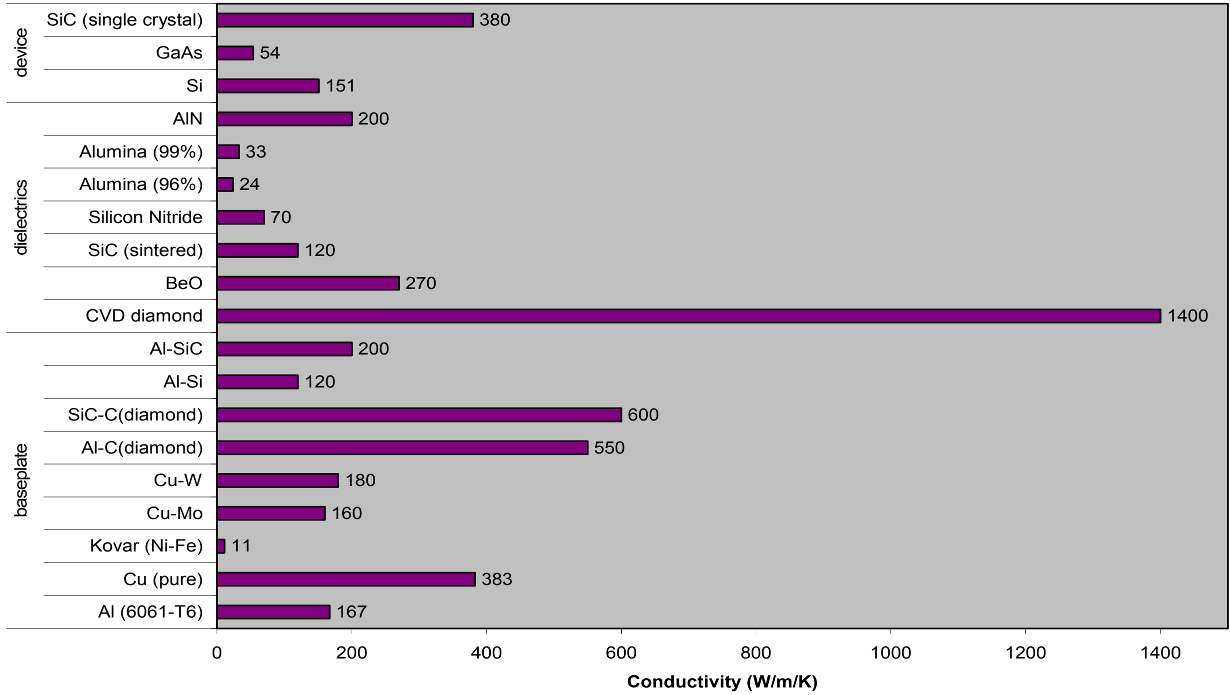



**Table 12. CTE of Materials**

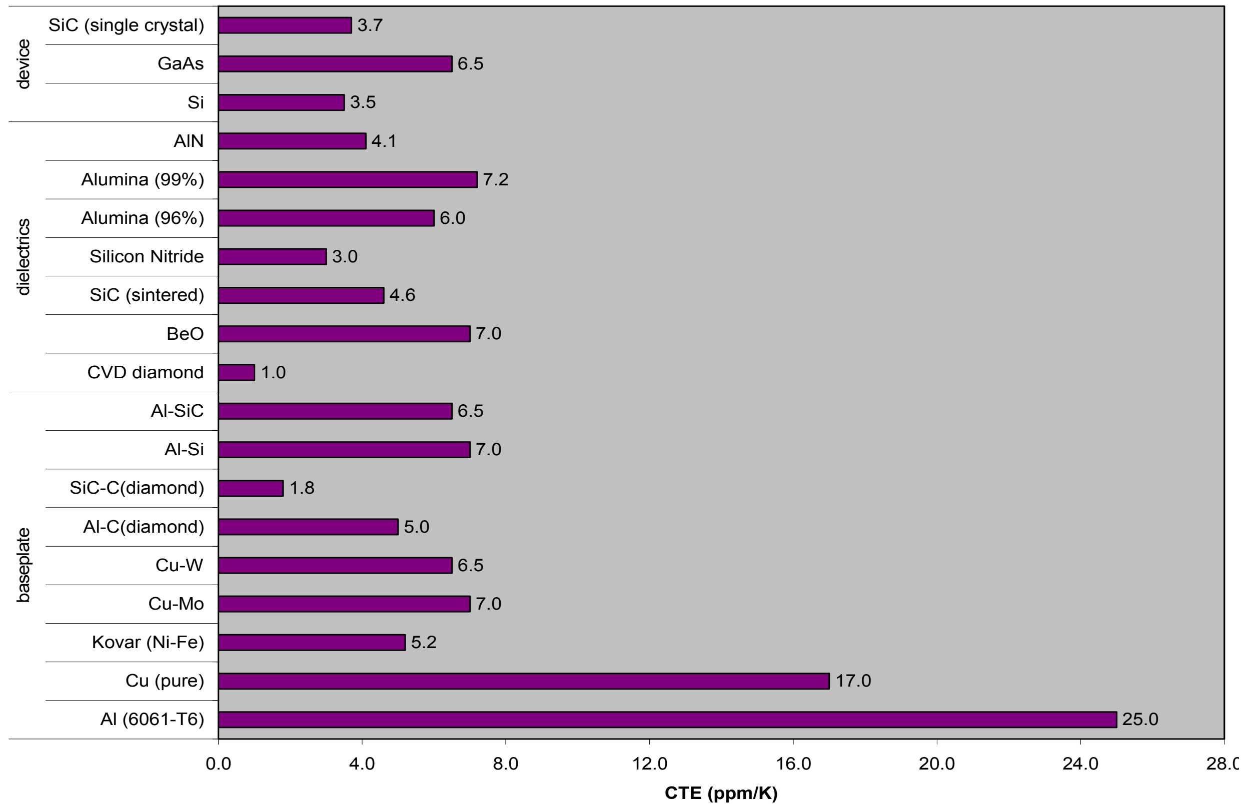


**Table 13. Density of Materials**

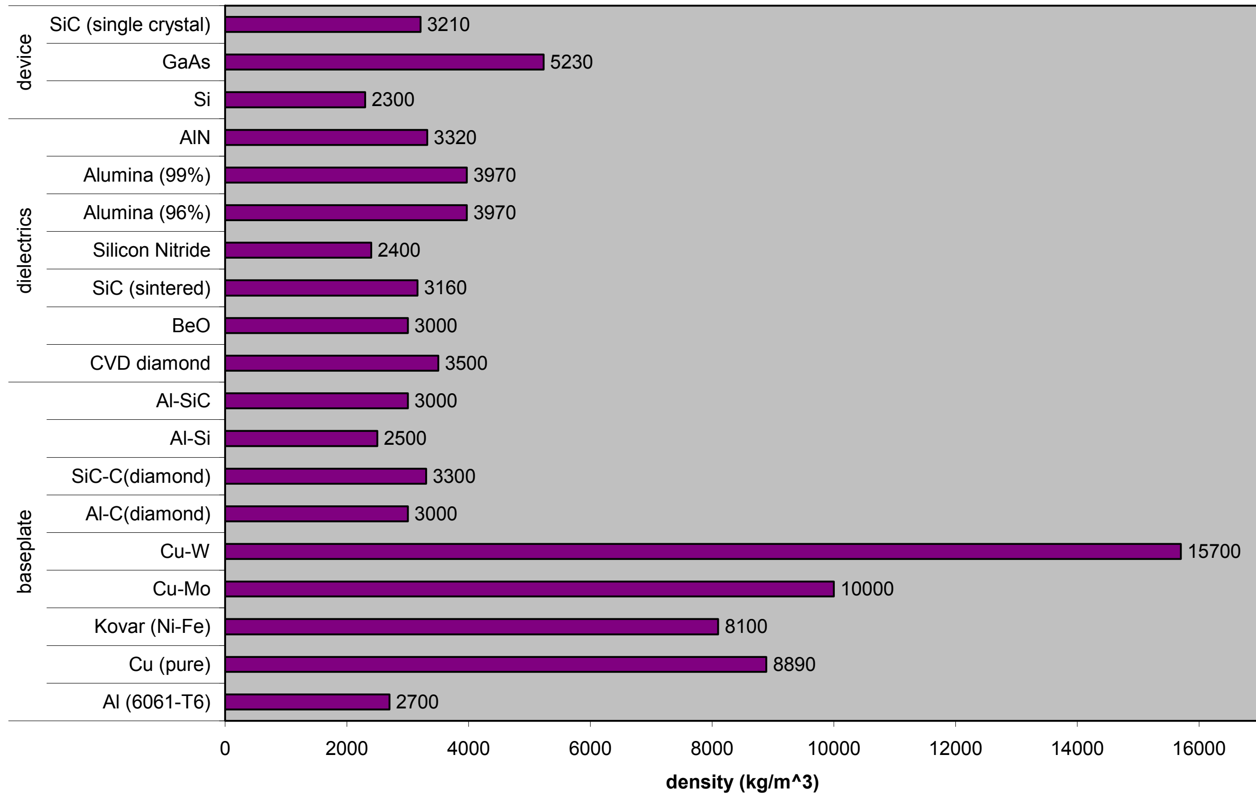



**Table 14. Cost of Selected Materials**

| Material | Density (g/cm3) | Cost ($/Kg) | Cost ($/cm3) |
|---|---|---|---|
| Copper | 8.9 | 18 | 0.16 |
| Aluminum | 2.7 | 2 | 0.06 |
| Boron Nitride | 2.25 | 132 to 176 | 0.30 to 0.40 |
| SiC Particles | 3.2 | 5.5 | 0.02 |
| Disc Carbon Fiber | 2.2 | 15 to 100 | 0.07 to 0.48 |
| Diamond Particles | 3.52 | 350 to 5,000 | 1.20 to 17.60 |
| Highly Oriented Pyrolytic Graphite | 2.53 | 1,320 to 1,760 | 3.30 to 4.50 |

From presentation by Carl Zweben on March 13, 2005

Table 11 shows the CTEs for the same materials. CTE of a SiC die is about 3.7 ppm/K, which becomes the target for all other materials. Aluminum and copper are the standouts from a cost and conductivity standpoint, but they are among the worst possible materials from a CTE standpoint. In fact, virtually all today's power semiconductor problems with CTE occur because aluminum or copper is being used somewhere in the package. This problem occurs with essentially all pure metals. Larger temperature swings experienced with SiC devices motivate the designer to consider ceramics with a lower CTE. Composites show promise, too.

The importance of CTE matching should be qualified. The objective is really to avoid excessive stress, which tends to involve *strain* matching more than simple CTE matching. When a large temperature gradient is present, the designer might elect to have appropriate differences in CTEs in adjacent materials. In addition, elasticity is desirable to allow strain differences to be absorbed without inducing cracks. Solders and other bonding materials particularly should have significant elasticity. The outcome of the interaction of all of the important material properties requires sophisticated modeling.

Table 13 shows density. Density is not a driver for wind turbines, but it is for other Peregrine applications, such as mobile power. One generally associates high density with high conductivity, but some of the ceramics and composites have surprisingly high conductivities without high densities.

Table 14 addresses cost to some extent. This table is a reprint from a recent conference in high temperature electronics packaging attended by a member of the Peregrine team. The table is highly incomplete as it contains only those materials that are actually produced in volume and have a recognized price. Some of the important materials in the previous tables do not fall in this class and are not listed because they cannot be priced. Nor can the processes that would be used in fabricating device packages with these materials be priced. Still, with this incomplete information, some conclusions can be drawn. The reason for the widespread use of aluminum is obviously low cost. When ease of fabrication is coupled with low material cost, it is a tough competitor to other materials. But the table also reveals the low cost of SiC particles that can be mixed with other materials in a composite. In fact, it can be mixed with aluminum, a process that is 20 years old and has a reasonable existing production infrastructure. Al-SiC would have a lower bulk cost than even copper when used in a heat sink and its CTE is much more favorable.

After candidate materials are identified, a tradeoff analysis must be carried out to select final materials. That is, an appropriate balance between conductivity, CTE, cost, and manufacturability must be struck. The material and results of the tradeoffs for this project are apparent from the three packaging concepts discussed later.

One of the important conclusions from the thermal modeling in this project is while high thermal conductivity is a plus, it is less important to the designer when the device can operate at over 300°C than when the die temperature is limited to 125°C. A few degrees more or less in the stack of substrates have little impact on a final design. The total temperature differential across all material in the thermal path up to and including the material in the fins of the heat sink is small in most cases–only around 25°C, whereas the temperature differential at the surface to drive

surface convention is about 225ºC. The designer would happily substitute thermal conductivity for a better CTE match or lower cost. If the absolute minimization of size were the criteria (space applications, but not wind turbines), the tradeoff result might be quite different.

A composite can be viewed as a "designer" material. Here the designer can simply select different mixtures of materials to meet different objectives. If the designer prefers to trade off conductivity for CTE, he can do it. The CTE of Al-SiC can be reduced to approximately 6 while for Al-C (diamond) it can be reduced to approximately 5. Obviously the resulting composite must still be capable of being manufactured in volume, as it is for Al-SiC.

### 6.4.3 Bonding and Attachments

Bonding and attachments represent a complex discipline that involve materials, processes, and specialized machinery. They generally are developed in direct response to a specific application. The bonding and attachments for a state-of-the-art power semiconductor using silicon were covered above. The techniques employed now are well developed and highly competitive, but they must be reviewed again since they will be changed greatly for a high temperature package. Not only must they be able to withstand much higher temperature, they must be capable of bonding the new materials. Otherwise promising materials must be eliminated from further consideration if bonding is not possible. With some innovative materials, it is not clear if reliable bonding is possible in a semiconductor package. While thermal and stress modeling has been accomplished in this project for several packaging concepts (discussed later), substantial experimentation is still required.

The available types of bonding include diffusion bonding, diffusion welding, thermal-compression bonding, DBC, brazing, soldering, and epoxy bonding. These will not be covered in any detail here, other than to give a few remarks about soldering, the current method for joining the die, and substrates. Power semiconductors typically use solders whose permissible operating temperatures can be as low as 200 to 225ºC, which has been acceptable to date since the device itself is limited to 125ºC. Some of the solders have reflow temperatures up to 280° to 312°C, but even those are not adequate for a package that operates at 300°C. However, several solders are available that can be used at temperatures above 300°C. Two candidates meeting the temperature requirement are the gold-silicon eutectic, which has a reflow temperature of 363°C, and the gold-germanium eutectic, which has a reflow temperature of 356°C.

The large suppliers of solder, such as Indium Corporation of America, sell dozens of types of solder, including the two just named, which can operate at over 300°C. Most of these suppliers will formulate a solder to specifications supplied by the customer. One of the solders recommended by Indium for high temperature packages in this project (Indium product designated #184) is 96.76% gold and 3.24% silicon. Gold sounds expensive, but it used throughout the electronics world where corrosion might be a problem. It is common to use gold in printed circuit boards. It does not lead to exorbitant cost, although the cost of a printed circuit board using gold is somewhat higher than for a printed circuit card with only copper.

One of the characteristics of high temperature solders is that they are harder and more inclined to crack under stress. This factor should be correctly represented in any thermal and stress

modeling of a packaging concept. More details will be given below when Peregrine's recommended packaging concepts and associated thermal/stress models are described.

There are also a few other die attach materials that are not used traditionally with power semiconductors, but show some promise at high temperature. These include silver filled glass, which has a lower CTE and modulus of elasticity than gold-silicon solder, and sintered silver paste, which has been demonstrated but is still in the research phase of its development.

# 7.0 SPECIFIC HIGH TEMPERATURE DEVICE PACKAGING CONCEPTS

## 7.1 Analytical Methods

### *7.1.1 Material Selection*

Obviously the methods selected must assist in answering the key questions. In this project, there are two primary areas of concern with the high temperature package, as enabled by SiC: (1) stresses from thermal dissipation that would cause the package to fail, and (2) overall thermal dissipation and the resulting size reduction of the semiconductor bridges. The materials that make up the semiconductor package impact both of these areas of concern.

The selection of materials for a high temperature package is based on a combination of material properties: conductivity, CTE, elasticity, cost, manufacturability, and maturity. Strictly from a stress standpoint, CTE is the most important, followed by elasticity. As noted above, conductivity is relatively less important at the higher temperatures being considered because the surface temperature differential will be about 225ºC in any case, while the temperature drop across the material in the substrate stack and heat sink will be only 25°or so. The relative insensitivity in the problem to material conductivity is caused by the dramatic increase in overall temperature differential from the use of SiC. The advantage of this is that the designer can select from a longer list of materials with CTEs that more closely match the CTE of SiC and can compromise the conductivity more than he would with a temperature cap of only 125ºC and maximum overall differential of 75°C.

If materials had similar advantages, their selection was based on price and maturity. There are a significant number of innovative materials being developed in the scientific community, particularly composites. Their properties are unconfirmed in some cases and their practicality in a cost sensitive world has not been evaluated. Peregrine has taken a conservative position on materials, but believes that significant improvement in materials will indeed occur during the next five years.

### *7.1.2 Failure Criteria*

In general, the von Mises yield condition or the maximum shear stress failure condition is used for evaluating materials that fail in a ductile manner. For materials that fail in a primarily brittle manner, the maximum principle stress failure condition is used. In the static thermal stress analyses, ceramic substrates and the semiconductor die were assumed to fail in a brittle manner and were evaluated using the maximum principle stress failure condition. Other materials, including metallizations, metal matrix composites, and solders were assumed to fail in a ductile manner and analyzed using the von Mises yield condition to determine where the materials started to yield.

The solder layers used in this analysis are a mixed breed. Static analysis can give a good idea of the magnitude of the stresses during one temperature excursion, but they do not shed much light on what happens during fatigue cycling. The safe option is not to allow the material to plastically

deform. Unfortunately, standard practice for silicon semiconductor packages is to push the limits of the fatigue cycling of solder and allow the solder to plastically deform to absorb the thermal stresses during a cycle. The effects of this type of stress relief method are hard to determine from a static analysis; only with the help of a load-cycle curve for the material can a conclusion be drawn from static analysis. Unfortunately, load-cycle curves exist for few materials and for solders load–cycle curves are non-existent. Ultimately, testing of real hardware is required.

Another issue with solder is the fact that hard solders of the type that can be applied to high temperature packages sometimes fail in a brittle manner. The safe assumption is to disallow the von Mises stress to exceed the yield strength of the solder and similarly with the principle stress. This is the assumption made for the design of the high temperature packages.

### *7.1.3 Modeling*

The general design strategy was to choose a set of materials that appears to work by looking at the material properties, and then develop a package that puts these properties to best use. For stress calculations, the semiconductor package was simplified to include only the power semiconductors and the free-wheeling (reverse) diodes that make up an inverter bridge in the converter, in addition to the substrate materials underneath the devices that will transfer the heat out of the devices and into the heat sink. After being drawn up physically with the SolidWorks CAD system, this simplified version of the semiconductor package was then modeled for its thermal and mechanical performance using a finite element analysis (FEA) program. The FEA program that was used for the analysis is CosmosWorks, also a product of SolidWorks Corp. (a Dassault Systemes company). Using two CAD products from the same company ensured compatibility.

The most promising designs were analyzed from both a two-dimensional (2D) and a three-dimensional (3D) point of view. The 2D model is primarily used to evaluate the thermal stresses in the various packages. Modeling stresses in the 3D model to less than 5% error is extremely computationally expensive and does not provide much value over modeling the stresses in the 2D model at this stage in the package development. The 3D model is used to evaluate the thermal capabilities of the package. Here, a 2D model is inadequate because heat spreads significantly in three dimensions, which greatly affects the thermal evaluation of the package. Three-dimensional thermal modeling is much less computationally intensive because each node has only one degree of freedom, verses three in the stress model, allowing for a much coarser mesh to come to an accurate solution.

### *7.1.4 Two-Dimensional Design Evaluation*

The 2D models used for analysis are highly simplified but still adequate for the job. A standard power semiconductor package does not have any obvious lines of symmetry (internally) that are useful, so the package is reduced to a single die, insulated on the top, with a material stack underneath that forms the heat path from the die to the air. The heat sink is simplified as a simple heat transfer coefficient, coupled with the bulk air temperature, to form the thermal boundary on the underside of the material stack.

Both the temperature distribution and the thermal stress distribution are modeled in this way. Because the fins of the heat sink are not available to act as a heat spreader, this 2D case is more severe from a thermal stress standpoint than the full 3D model. An evaluation of the design is based on the calculated thermal stresses under the failure theories explained above.

### *7.1.5 Three-Dimensional Design Evaluation*

Once the design has been evaluated from a 2D perspective, a 3D model of the design is constructed and analyzed. The model is simplified to consist only of the six-pack of switches and diodes forming the three-phase inverter bridge, and the material stack forming the thermal path from the devices to the heat sink. The heat sink model includes fins to determine the extent of the heat spreading within the fin.

Meshing a 3D FEA model is by far the most difficult part of the 3D analysis. For this reason, the 3D model was analyzed with a much coarser mesh than with the 2D model. The primary purpose of the 3D model was to evaluate the thermal performance of the overall design, and to verify that the stresses found in the 2D model were sufficiently accurate to apply to the 3D case. The design was then evaluated on its thermal performance and feasibility.

## 7.2 General Approach

The analysis pertaining to thermal packaging has two primary parts: stress determinations around the device and overall sizing for gross heat removal. The first part involves, as indicated above, the use of two CAD tools for the thermal and stress computations. This part can be abstracted from a total inverter block with devices, substrates, and heat sink. That is, it can be carried out by focusing only on the device and immediate substrates with everything else represented in the form of boundary conditions. When done this way, there is great latitude in how the models are set up. The power level, for example, does not need to match the specifications for any part of the converter for the 1.5 MW wind turbine. All that is important is that the local conditions simulate the real conditions in the wind turbine converter. That is, the models and its assumptions must produce the appropriate temperature gradients and differential movement of adjacent materials that will be found in the device stack.

The stress analyses were accomplished using an inverter module rated at about 60 kW, but the current densities, heat flux loadings, and temperature gradients were similar to that experienced in a converter comprised of two back-to-back inverters rated at 1.5 MW. Each inverter contained only six devices (transistor/diode sets). Note that each transistor or diode might be comprised of multiple dies that provide sufficient area to make current densities realistic.

One of the unknowns remaining in this project is the appropriate rating of a high temperature inverter module. The converter for the baseline 1.5-MW turbine is comprised of two 750-kW converters operating side-by-side. This was believed to be appropriate by its designer given the needs of the turbine, and the availability and cost of power semiconductors at the time. With SiC devices, this issue must be considered again, but most of the variables are not known. With entirely new materials, geometries, and fabrication processes, the results would be different. Emphasis should be placed on the unknown fabrication processes. If heat sinks were made of

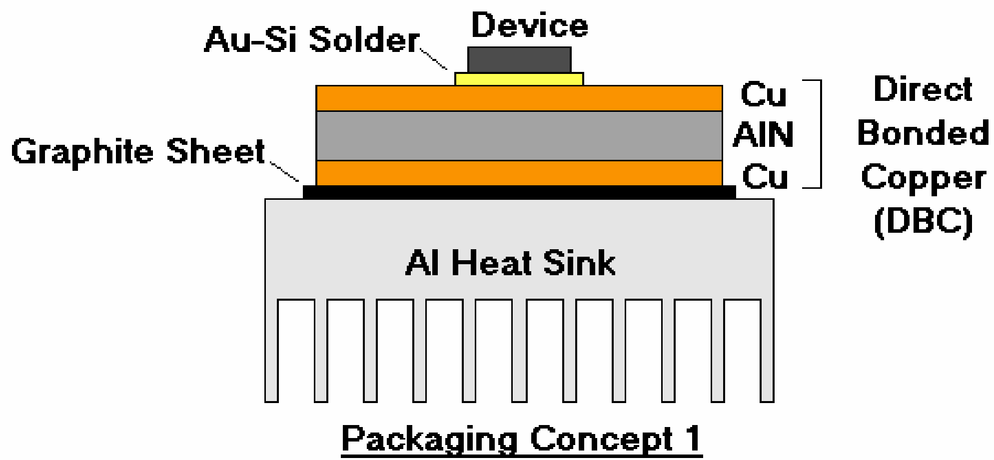
AlN (one of several possibilities), large heat sinks might not be possible to fabricate because AlN is “grown” in a complex and costly process. Conversely, it might be possible to readily manufacture small, rugged versions at low cost in highly automated processes. An inverter module rated at 250 kW for example, might have the minimum cost on an installed, per-kW basis. The selection of the appropriate overall module rating for carrying out the thermal stress computations is quite arbitrary. No one rating is better than another as long as the thermal conditions critical to the determination of stress and failure have been accurately depicted. Therefore, one should not interpret the use of a 60 kW module in these calculations as indicative of the rating of an optimized, commercial inverter.

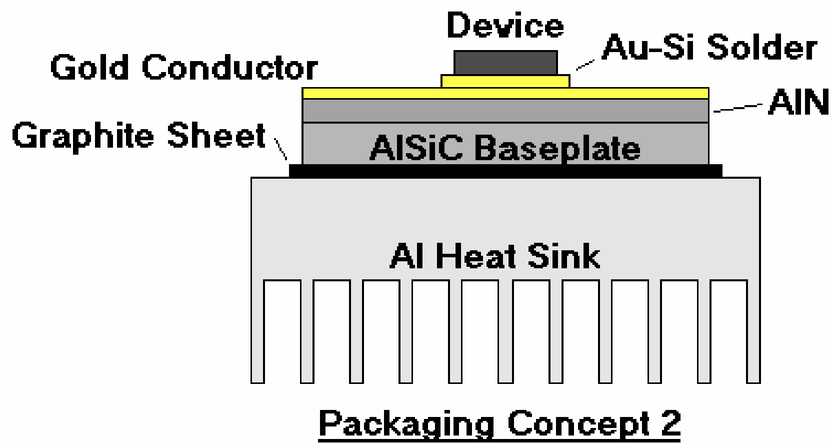
On the other hand, the reader should still get from this project a perspective as to the amount of size reduction possible when using SiC devices in a 1.5 MW converter. Therefore, 1.5-MW inverter blocks are also presented in a later section for both silicon IGBTs and SiC devices. Those inverters also have thermal stress conditions similar to those present in the modeling work with 60 kW modules.

## 7.3 Packaging Concept 1: State-of-the-Art Silicon Package Modified for High Temperature

### *7.3.1. Basic Package Design*

Figure 6 shows the stacks for all three concepts. One of the current state-of-the-art approaches in power semiconductor design uses DBC, a sandwich of copper layers around a center layer of Al2O3 or AlN ceramic, to which the die is soldered. The DBC is often mechanically attached to a heat sink without using another intervening base plate. This approach was described earlier as used by Semikron in its SKiiP power module. The design has a low profile and reasonably good heat path due to the thinness of the DBC. It has good thermal cycling reliability because the CTE of the DBC is dominated by the low CTE of the ceramic layer and because the mechanical attachment of the DBC to the heat sink can accommodate differential movement during cycling. Packages using a copper base plate to stiffen the substrate layer and make the package suitable for attachment to a heat sink have to contend with the solder attachment to the base plate. Semikron eliminated the base plate by using DBC with a plastic frame to evenly distribute pressure across the DBC when pressed directly against the heat sink. Built into this plastic frame are the leads that conduct current into and out of the package. Because this package eliminates materials that have high differences in CTEs, it would seem an ideal candidate to modify for high temperature use. Between the DBC substrate and the heat sink there is a layer of thermal interface material, which in the high temperature concept would most likely be graphite that can withstand 300ºC. All plastics could be replaced with higher temperature plastics, a number of which are available.



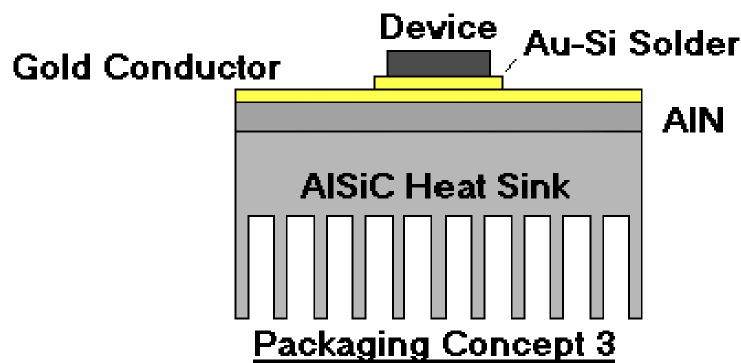




Figure 6. Die/Substrate Stacks

### *7.3.2 Die Attachment and Material Selection*

Besides the plastic in the frame, the solder used in the package must be replaced with a solder able to withstand temperature over 300°C. With this first design concept, the goal is to keep the package as conventional as possible, so the commonly used gold-silicon eutectic solder (Indium product) has been chosen. This ensures that the package can be readily assembled with minimal change to the processes established for standard temperature power semiconductor packages.

Next, the materials and geometry of the DBC layer have to be chosen. Commercial DBC offers a choice between two ceramics: $Al_2O_3$ (alumina) and AlN. There are tradeoffs in selecting between the two. The thermal conductivity of alumina is almost an order of magnitude less than that of AlN. The CTE of Alumina is roughly 6 to 7 ppm/K, compared to AlN with a CTE of 4.5 ppm/K. The CTE difference is important; alumina is better suited for use in DBC because the CTE difference between alumina and copper is smaller than with AlN. This makes alumina based DBC less prone to thermal shock failure than AlN based DBC. In this design, however, the stresses in the AlN DBC were not enough to cause failure, so AlN was chosen for the ceramic due to the better match of the CTE with the device, thereby lowering the stresses in the semiconductor die and the solder layer attaching the die to the substrate. The following thermal stress analysis will elaborate.

### 7.3.3 *Thermal Analysis*

Figure 7 shows the 3D package with the overall thermal profile. The pressure frame and the external structure are omitted for clarity. By allowing the junction temperature of the die to reach 300°C, the thermal package can be made very small–only about 4 inches on a side. The model predicts these temperatures by assuming a 0.5% loss in a 60 kW inverter bridge, which is 33% of the 1.5% losses assumed in a silicon IGBT bridge. The losses are assumed to occur 2/3 in the transistor and 1/3 in the diode. Also assumed is an effective surface heat transfer coefficient of the heat sink fins of 25 $W/m^2/K$. This heat transfer coefficient is probably conservative (low), but is still believed to fall within a typical range of the heat transfer coefficients obtained when using forced convection with a fan.

### *7.3.4 Stress Analysis*

There are two places in the Concept 1 package that warrant a stress analysis. The first place is in the ceramic substrate where it is being put into tension at the edge of the copper layer. The second place is in the solder layer at the outer edge of the semiconductor die.

With DBC, the substrate layer is put under considerable stress due to the CTE mismatch between the ceramic substrate and the copper metallization layer. DBC is provided with options for many different material layer thicknesses to satisfy several requirements. It is important to satisfy the current carrying requirements with the thinnest layer of copper as possible, and to satisfy the heat transfer requirements with the thickest layer of ceramic possible.

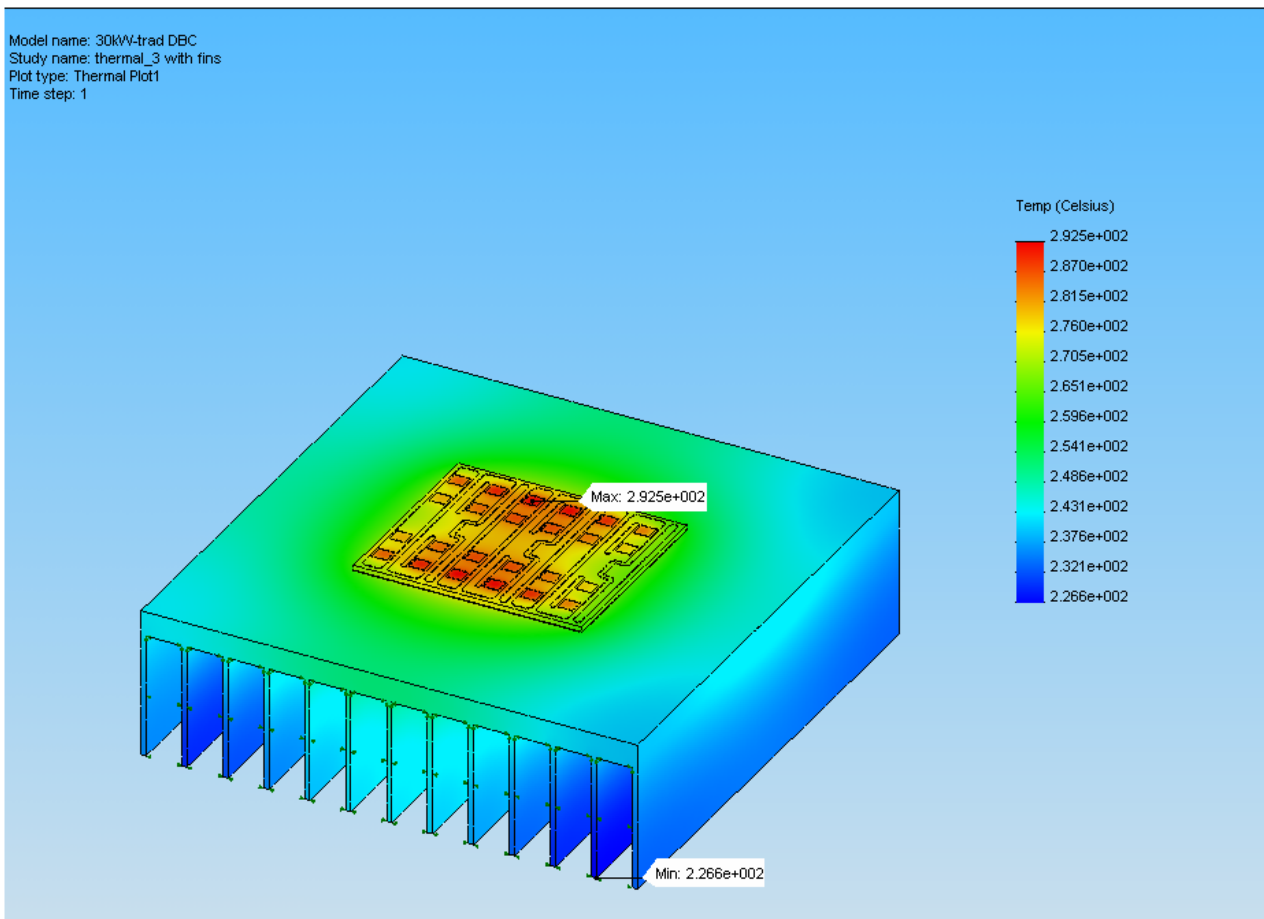



**Figure 7. Concept 1 - 3D Thermal Profile**

As noted earlier, DBC is offered with a choice of two different ceramics to use as the substrate: AlN and alumina. One of the objectives is to use the thermal stress analysis to provide guidance in choosing one of these materials over the other.

***Substrate analysis method.*** A 2D FEA was done on the cross section of a single die mounted on the DBC metalized substrate. The model was meshed in such a way as to provide a mesh density of roughly 200 nodes/mm along the interface between the upper copper pad and the substrate. This is the location where a crack in the substrate will likely form and start growing to cause the package to fail. At this node density, the stress solution can be assumed to have less than 5% error according to a mesh resolution study done previously.

A thermal analysis is first carried out with an appropriate heat load for a 60-kW SiC converter put onto the die, and an appropriate convection coefficient on the underside of the package, sufficient to keep the maximum temperature of the package below 300°C. The solution of the thermal problem is then used as the load condition for the stress analysis. The ceramic substrate is assumed to fail in a brittle way, so the maximum principle stress criterion is applied to a plot of the first principle stress.

***Stress analysis results.*** Figure 8 shows the first principle stress plot in the region of the substrate at the copper metallization edge. For the AlN substrate of 1 mm thickness and a copper layer of 0.127 mm, the maximum principle stress along the interface between the copper and the substrate was found to be 156 MPa, which was well below the tensile strength of 310 MPa for AlN. For the alumina substrate of the same thickness, the maximum principle stress in the same area was 174 MPa. This was below the tensile strength of 99% alumina of 207 MPa, but with a lesser margin. The stress can be reduced in alumina by increasing the thickness of the substrate layer, but the penalties brought about by the low conductivity of alumina are felt more. One mm is the maximum thickness offered for AlN, and 0.127 mm is the minimum thickness for the copper layer in commercial DBC, so the stress levels of the AlN DBC are at the minimum.

***Thermal stress analysis on solder layer.*** The solder layer is made up of gold-silicon eutectic solder. Because the CTE of the SiC semiconductor die and the DBC are different, it is expected that significant stress will develop at the edge of the solder layer, possibly causing failure.

***Solder layer analysis method.*** For the solder layer analysis, the mesh node density is set to 200 nodes/mm in the solder layer to obtain an error of less than 5%. The solder layer is assumed to be 1 mil (0.0254 mm) thick and to form a fillet at the edge of the semiconductor die. Modeling this fillet prevents a nonphysical discontinuity in the von Mises stress at the corner between the solder layer and the copper layer. The thermal stress analysis is then carried out in the same way as described for the substrate thermal stress analysis method.

Because the solder is a metal that is within 60°C of its eutectic melting point, it is assumed that the solder will display considerable yielding before failure. In this case, the von Mises stress criteria for yielding is used to predict if the solder layer will yield. This yielding does not necessarily suggest that the package will fail right off, but suggests that, with cycling, the package will fail by fatigue mechanisms. The further the solder yields, the shorter the life of the package.

***Stress analysis results.*** Figure 9 shows a plot of the von Mises stress in the outer edge of the solder layer. Both the package made with AlN DBC and the package made with alumina DBC predict stresses in the solder layer that exceed the yield strength of gold-silicon eutectic solder. For the AlN DBC package, the maximum von Mises stress at the surface of the solder fillet amounts to 441 MPa. The maximum von Mises stress for the alumina DBC package amounts to 1073 MPa.

Because the von Mises stresses in both cases were significantly higher than the solder tensile strength of 255 MPa, the solder was found to yield as the package was thermally cycled. Due to lack of fatigue strength data for gold-silicon solder, it is difficult to predict the actual life of the package for either configuration; however, it is obvious that the Aluminum Nitride DBC package performs better than the Alumina DBC package.

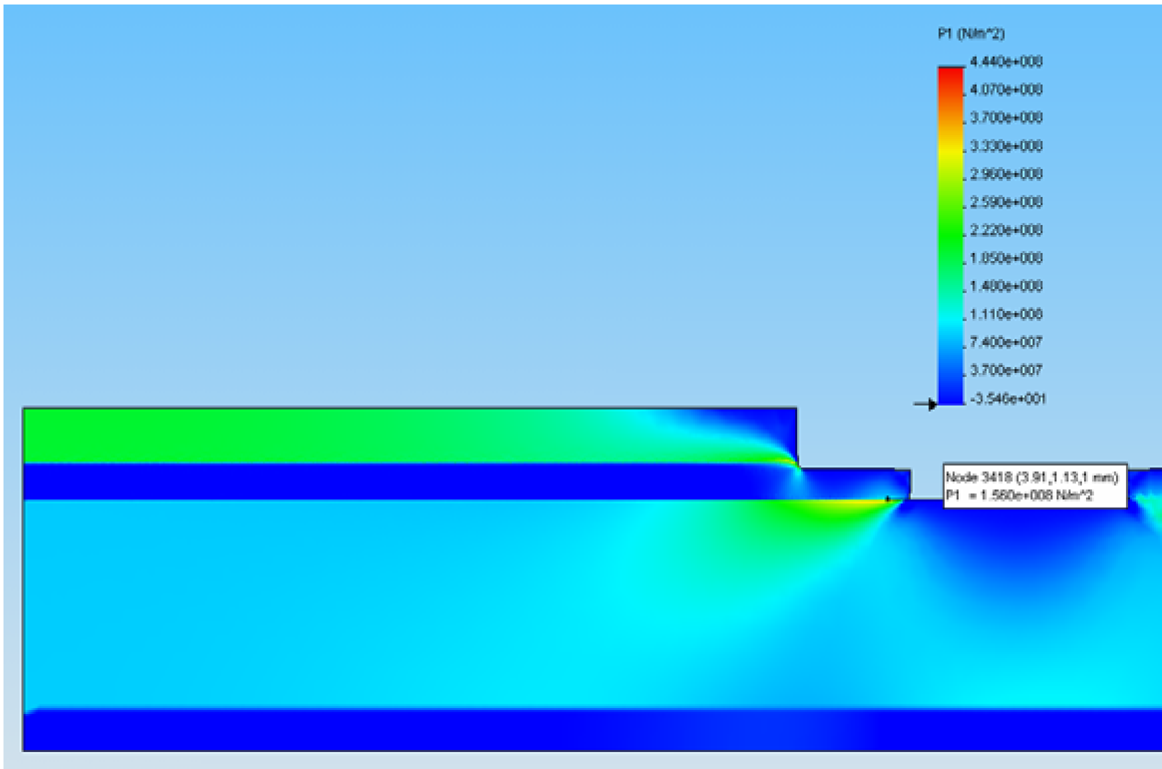



**Figure 8. Concept 1 – 2D Stress Profile of Ceramic Substrate**

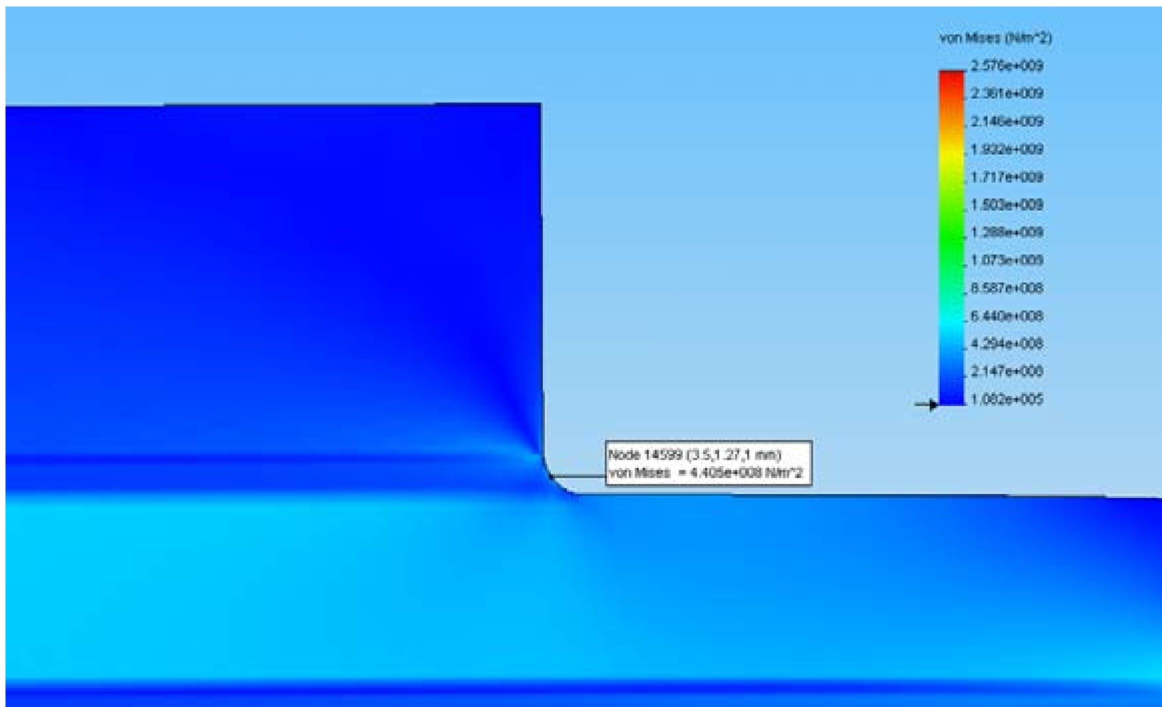



**Figure 9. Concept 1 – 2D Stress Profile of Solder Layer**

### 7.3.5 Conclusions on Concept 1

These results indicate the best package obtained using DBC technology, both from a thermal dissipation aspect and a thermal stress aspect, uses AlN as the substrate layer. AlN DBC provides better margin of safety for stress in the ceramic layer, and provides lower stresses in the solder layer, due primarily to its lower CTE, which is better matched to SiC.

Overall, the DBC metalized substrate of Concept 1 makes for a marginal package from a thermal stress perspective. Because the stresses in the solder layer are double the tensile strength of the solder material, this package is unlikely to be reliable under thermal cycling. Other die attach materials such as silver filled glass or sintered silver paste hold promise for this package, as these materials are much less stiff and will be more resistant to fatigue failure. However, these materials are still unproven in power electronics use and will necessitate a large change in equipment and manufacturing techniques.

The design might be made to work with proper testing of different configurations, particularly in the area of thermal cycling. It is not an optimal design, but it has the advantage of being manufactured with minimal change in standard power semiconductor packaging processes.

Another cause for concern is the high thermal stresses in the die itself caused by the stiffness of the DBC package. It is difficult to find mechanical properties such as the tensile strength for single crystal SiC and every indication is that the mechanical properties vary greatly compared to polycrystalline SiC ceramic used for more common applications. A single source from an IEEE proceedings paper in 1982 indicates that the tensile strength of single crystal silicon carbide is 22 GPa, which is much higher than any stress level predicted by the model. Still, this value is in question since the failure stress will be influenced downward by surface defects in the die, the effects of which are unknown.

## 7.4 Packaging Concept 2: Entirely New Approach

### 7.4.1 Basic Package Design

The stack was shown earlier in Figure 6. The major difference between this package concept and Concept 1 is the metallization used on the substrate. Most of the problems with the first concept revolve around the high stiffness of the DBC substrate. This package represents an alternative that uses gold conductor as the substrate metallization to relieve thermal stresses on both the substrate and the die attachment material.

The package consists of a 1 mm thick AlN substrate with a thick film gold metallization layer to carry current to and from the semiconductor die. Brazed to this thick film gold metallization layer is a 0.1 mm layer of pure gold to act as the main current conducting layer. The semiconductor die is bonded to the top of this gold layer either by solder or a direct thick film bonding technique that was uniquely developed for high temperature packaging of SiC devices.

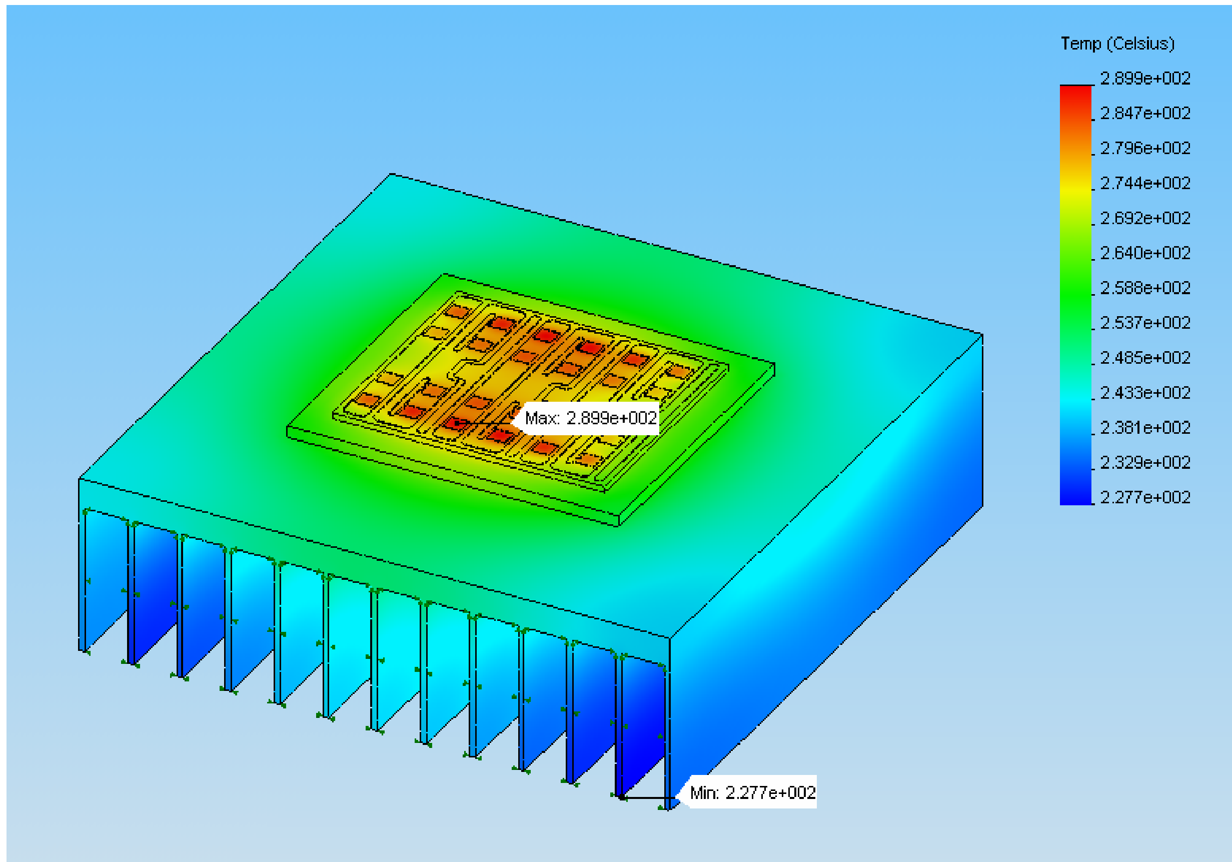



**Figure 10. Concept 2 - 3D Thermal Profile**

Below the substrate layer is a base plate made from a CTE matched, high thermally conductive material. The base plate serves to stiffen the AlN substrate for mechanical attachment of the package to an aluminum or copper heat sink. The mechanical attachment of the thermal package to a heat sink is what separates this packaging Concept 2 from packaging Concept 3. Similar to the first concept, the thermal interface material between the package and the heat sink will be a graphite-based sheet of material that can withstand temperatures in excess of 300ºC. Figure 10 shows the 3D model used for packaging concept 2, along with the temperature plot illustrating the thermal performance of the package.

### *7.4.2 Die Attachment and Material Selection*

This new approach takes some major ideas from hybrid circuit design where power semiconductors are put on the same substrate as IC circuitry. These packages traditionally use a ceramic substrate, such as alumina, and a thick film metallization for the current path. Hybrid circuit manufacturers use this process because it allows for thinner traces that are useful on the IC side of the board. In general, thick film metallization is more expensive than DBC, which is why power semiconductor manufacturers use DBC.

Thick film metallization is a process where a mixture of metal and glassy ceramic are mixed into a paste. This paste is applied by a screening technique to the ceramic substrate in the shape of the

final circuit. The substrate and paste are then put into an oven where the thick film paste is fired, bonding the metallization to the ceramic substrate surface. The result is a durable metallization layer, but one which cannot carry much current because of the thinness of the metallization layer and the nature of the material. Because of the lack of current carrying capability, thick film metallization is usually used in low power semiconductor circuits. However, the thick film layer can be used as a base for applying a new layer of pure material by way of a brazing process. This can be used to create a conductor pattern that can carry the current necessary for high power devices. This thick film conductor pattern can be used up to temperatures well exceeding 300°C.

Thick film conductor can be made with a number of different metals. The most promising in this application is to use gold as both the thick film layer as well as the brazed-on conduction layer. Gold has a low electrical resistivity, as well as a high thermal conductivity. It also has a low modulus of elasticity that aids in stress relief.

For the die attach material, there are two options. For temperatures limited to 300°C, gold-silicon eutectic solder is the ideal choice because it is a very mature material, readily available, and will bond well with the gold conductor layer. A more exotic die attach method that is possible with thick film is to directly attach the die to the thick film during the thick film firing process. This die attach method has been demonstrated up to temperatures exceeding 500°C. Although the direct die attachment has been proven, the disadvantage is the method is still proprietary and is still in the development stage. The thermal cycling behavior of the direct die attach is still unknown. The direct die attach has been demonstrated with a SiC pressure sensor (NASA application), but has yet to be demonstrated with a power semiconductor device. Because the gold silicon solder is a more proven material and is more readily available, it is the most practical choice for the 300°C package.

Because of the strain relieving properties of gold in a thick film conductor layer, there is much more freedom in material selection for the substrate and the die attach material. The obvious choice for the substrate layer is AlN, because this material has a very high thermal conductivity, and a CTE that is very well matched with silicon carbide.

The AlN substrate will be mounted to a base plate made of a CTE matched material. There are several materials that have CTE values similar to that of SiC and AlN. Among these are the metal alloys Kovar and copper-tungsten, and metal matrix composites, including aluminum-silicon carbide (AlSiC), aluminum-silicon, and aluminum-diamond. Other materials exist, particularly ones that fall into the category of metal matrix composites, but almost all of these are experimental and very expensive.

Of all the materials, Kovar has the closest CTE match with AlN. The overriding disadvantage is its low conductivity that is a full order of magnitude lower than other popular materials. Because of the high temperature of the package, this is not nearly so great a problem as it would be with a standard temperature package, but it is certainly less than ideal. Copper-tungsten has a conductivity and CTE very similar to that of AlN. Copper-tungsten would also make a workable base plate, but it is hard to process and is not as dimensionally stable as other materials.

Of the metal matrix composite materials, aluminum-diamond is possibly the best material. Its CTE is very close to that of AlN, and its conductivity is very high due to the diamond particles. The only disadvantage of using this material is that it is likely to be expensive. Aluminum-diamond composite is not widely used and diamond powder is expensive.

Aluminum-silicon is a material somewhere in-between a metal matrix composite and a metal alloy. It has many of the properties of a metal matrix composite, including the low CTE, but has the advantage of being machineable. The disadvantages of this material are the high cost and the relative lack of mechanical strength. Its primary use is in the aerospace industry where cost is less an issue and its light weight makes it attractive.

An inexpensive compromise to aluminum-diamond is aluminum-silicon carbide (AlSiC). AlSiC has a CTE that is similar to AlN and a thermal conductivity that slightly exceeds that of pure aluminum. It is more easily processed than copper-tungsten. AlSiC is made by loosely sintering SiC powder to a preform in a near net shape. This preform is then put into an injection mold, where it is infused with molten aluminum. Because of this injection molding process, a ceramic substrate can be in-molded into the AlSiC base plate, making a solder or brazing layer between the substrate and the base plate unnecessary. Because of all the advantages of AlSiC, it has been chosen for the base plate material in this package.

### *7.4.3 Heat Sink and Attachment*

This concept uses a standard aluminum heat sink. Because a base plate is used in the package, it must be mechanically attached to the heat sink, in this case using appropriately spaced bolts and a graphite-based, thermal interface material. Note that the graphite-based material is new since the standard heat conducting silicon paste can not be used due to temperature limitations.

### *7.4.4 Thermal Stress Analysis*

The procedure for stress analysis for Concept 2 is identical to the procedure for Concept 1. First a two dimensional cross section of a single semiconductor die and the stack of material responsible for heat removal is modeled. Similar to Concept 1, the critical areas of stress are 1) in the substrate layer at the edge of the metallization, and 2) at the edge of the solder layer. The model is meshed in a way to provide a 200 node/mm node density in the two critical locations, which results in a less then 5% error based on a mesh resolution study.

***Stress results for substrate.*** Figure 11 shows the first principle stress profile in the substrate layer at the edge of the metallization layer. As AlN is used as the substrate, and the metallization layer is, again, of a higher CTE than the AlN ceramic, the failure mechanism of the substrate under thermal cycling will be in the form of a conchoidal crack, starting at the edge of the

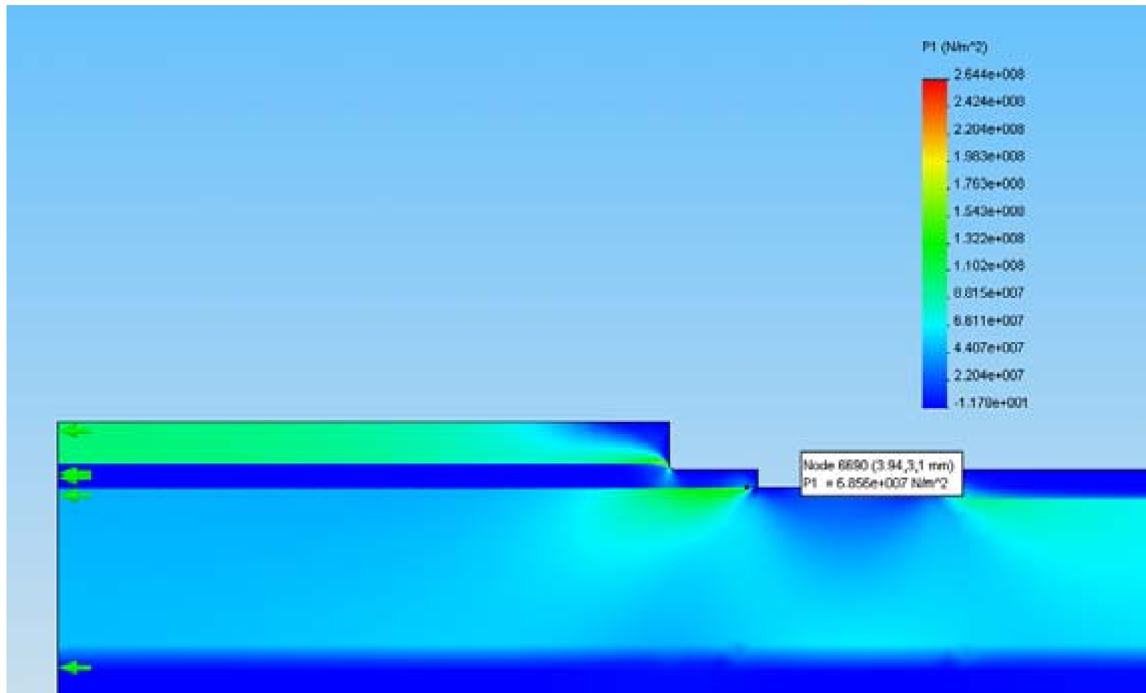



**Figure 11. Concept 2 – 2D Stress Profile of Ceramic Substrate**

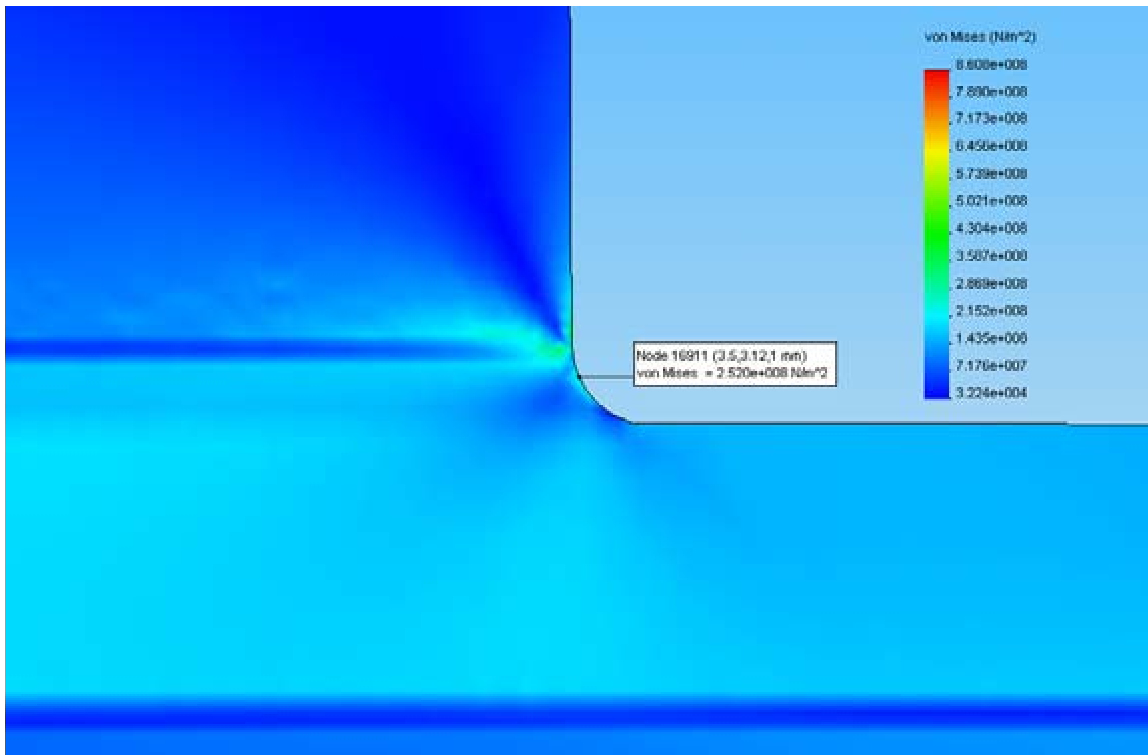



**Figure 12. Concept 2 – 2D Stress Profile of Solder Layer**

metallization and extending under the metallization layer. The maximum principle stress failure criterion is applied.

At the interface between the metallization layer and the ceramic substrate, the highest principle stress is 68.6 MPa, which is well below the tensile strength of AlN of 310 MPa. This amounts to a large safety factor regarding the failure of the substrate layer due to thermal stresses.

***Stress results for solder layer.*** The solder layer represents the second critical area. The solder is gold-silicon eutectic and is modeled with a fillet at the edge of the semiconductor die. The solder layer is expected to fail by way of plastic deformation which will lead to limited life due to thermal cycling fatigue.

At the edge of the solder layer, on the surface of the fillet, the von Mises stress comes to 252 MPa, which is at the edge of the solder tensile strength. This is expected to be marginally acceptable because the solder is expected to yield in a ductile manner and the amount of plastic deformation at this stress level is expected to be low. Even if the solder fails by brittle cracking, the maximum principle stress in the solder layer is 257 MPa, which is, again, right at the tensile strength of the solder. Because the stress levels are right on the boundary, it is difficult to tell what the package reliability will be without further experimentation. It is apparent that the stress levels in this package are much lower than the stresses seen in the Concept 1 DBC package.

### *7.4.5 Conclusions on Concept 2*

This package concept is much better suited to 300°C operation than the DBC package. Uncertainties regarding the reliability of the solder layer can only be quantified by an experimental prototype. In any case, this package concept is seen as a potentially reliable package that combines a specifically designed high temperature substrate and metallization with a standard aluminum or copper heat sink to keep costs as low as possible.

This design entails more technology risk than the DBC design because of the use of processes and materials that are not commonly associated with the manufacture of power semiconductor packages. The ability to plate thick gold on top of a gold metallization film presents some risk to the reliability of the package simply because it is not well known what will happen when these materials are thermally cycled. At the same time, because the stresses in the solder, die, and ceramic substrate layers are lower, their reliabilities should be higher. After discussions with experts in the field, the team knows of no reason why this approach could not be used. Confirming experiments would be important in the development process. This package design has the potential to be far superior to the DBC package in the first concept.

## 7.5 Packaging Concept 3: Small Form Factor Package

### *7.5.1 Basic Package Design*

The stack was shown earlier in Figure 6. The material stack for packaging Concept 3 is similar to that in packaging Concept 2. The major difference between these two concepts is package

Concept 3 skips the aluminum heat sink and extends the AlSiC base plate layer from Concept 2 into full heat sink made from AlSiC. Because the mechanical interface between the AlSiC base plate from Concept 2 is not there, the thermal resistance of the whole package is greatly reduced. This means there is less temperature drop between the semiconductor die and the bottom of the heat sink, so the material in the heat sink will be half that for the heat sinks of Concepts 1 and 2.

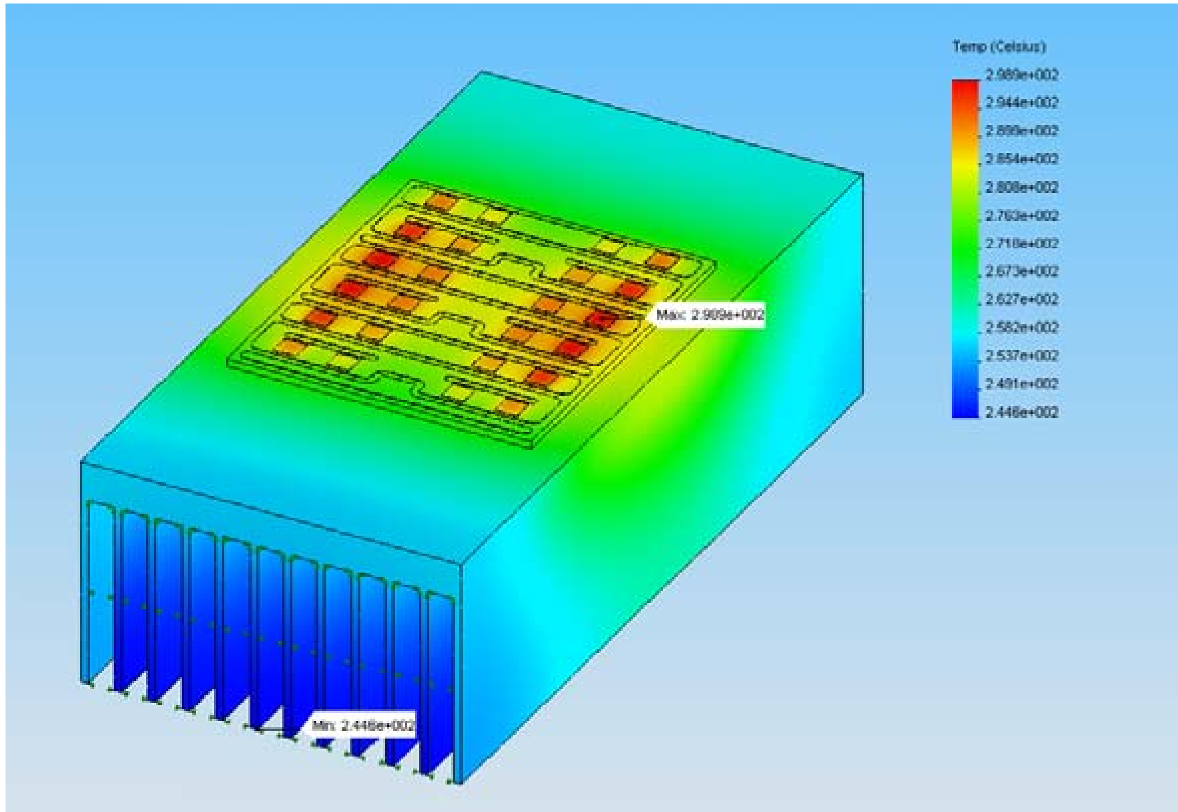



**Figure 13. Concept 3 - 3D Thermal Profile**

The substrate is a 1 mm thick layer of AlN in-molded into an AlSiC base plate/heat sink in the same way as described in the package concept 2 section. The AlSiC heat sink is 2 inches by 4 inches, which is half the size of the Concept 1 and 2 packages. On top of the substrate layer, a layer of thick film gold is used as a metallization layer, with a 0.1 mm layer of pure gold on top of this to carry the current from the semiconductor die. Figure 13 shows the 3D model of packaging concept 3, as well as the temperature plot to evaluate the thermal performance of the package.

### *7.5.2 Die Attachment and Materials Selection*

A 300°C temperature limit means that with the right materials the thermal package can be made very small with very high performance. The smallest package will be achieved by integrating the heat sink into the base plate or even the substrate of the package. As long as the materials are selected with cost and manufacturability in mind, the smallest package could well be the lowest cost after the fabrication infrastructure and volume develop in the years ahead.

Both AlSiC and AlN can be formed into a heat sink like shape. However, the mechanical properties of AlN (a ceramic) make turning this material into a heat sink risky, not because of the thermal stresses generated in the package, but because of its low bend strength and corresponding vulnerability to mechanical shock as might occur if the converter is dropped or bumped. AlSiC is a much more durable material due to the aluminum matrix. The CTE is well matched with AlN, and the AlN substrate can be in-molded into an AlSiC heat sink. From Table 14 one can interpret the cost of AlSiC as competitive.

All the materials for die attachment and bonding of other substrates are exactly the same for this package as for Concept 2.

### 7.5.3 Thermal Analysis

Figure 13 shows the thermal profile for Concept 3. The fin design is very basic and is chosen to produce the necessary cooling with a 25 $W/m^2K$ convection coefficient. The primary reason the packageis half the size of the first two concept packages is the lack of a significant thermal contact resistance at the boundary between the heat sink and the substrate.

### 7.5.4 Stress Analysis

Concept 3 takes the substrate and metallization from Concept 2 and uses a CTE matched, permanently bonded (not mechanically attached) heat sink to produce a package with the smallest form factor possible. The stress analysis method for this package is identical to the methods used for the other two concepts. The critical stress areas are in the same place, in the substrate at the edge of the metallization, and at the edge of the solder layer. A 2D model is created for a single die attached to the material stack for heat removal. The model is meshed to provide a 200 node/mm node density that keeps the numerical error in the stress results to less than 5%.

***Stress results for substrate layer.*** Figure 14 shows a plot of the first principle stress in the substrate at the edge of the metallization layer. The substrate is most likely to fail by thermal cycling by conchoidal fracture, so the maximum principle stress is modeled to predict cracking in the substrate layer. The most severe tensile stress happens at the interface between the substrate and the metallization layer near the edge of the metallization layer. At this point, the maximum principle stress is 64.6 MPa, which is much lower than the tensile strength of AlN of 310 MPa. This indicates that under thermal cycling, the substrate is unlikely to fail.

***Stress results for solder layer.*** Figure 15 shows the von Mises stress in the solder layer. The solder layer is likely to fail by fatigue due to plastic deformation. The solder layer is modeled to terminate with a fillet at the edge of the semiconductor die. The maximum von Mises stress at the edge of the fillet is 181 MPa, which is well below the tensile strength of the solder. This indicates that the solder will not deform plastically, so the package should not fail in a short time

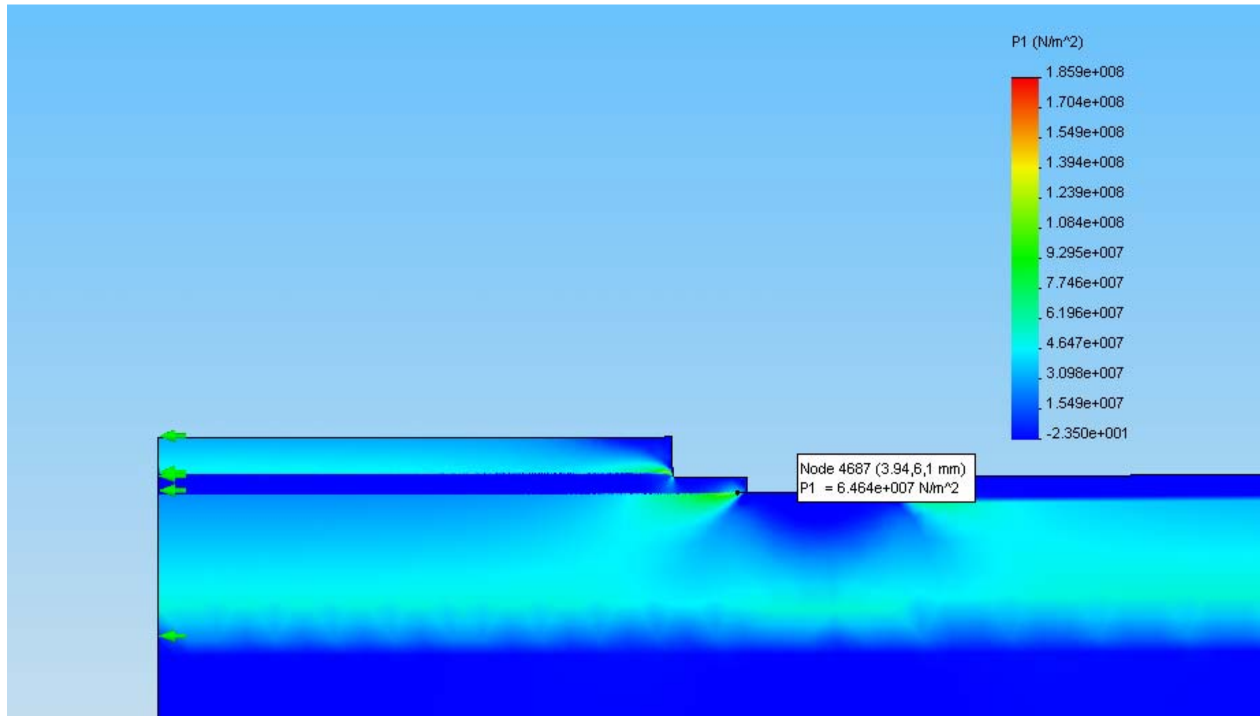



**Figure 14. Concept 3 – 2D Stress Profile of Ceramic Substrate**

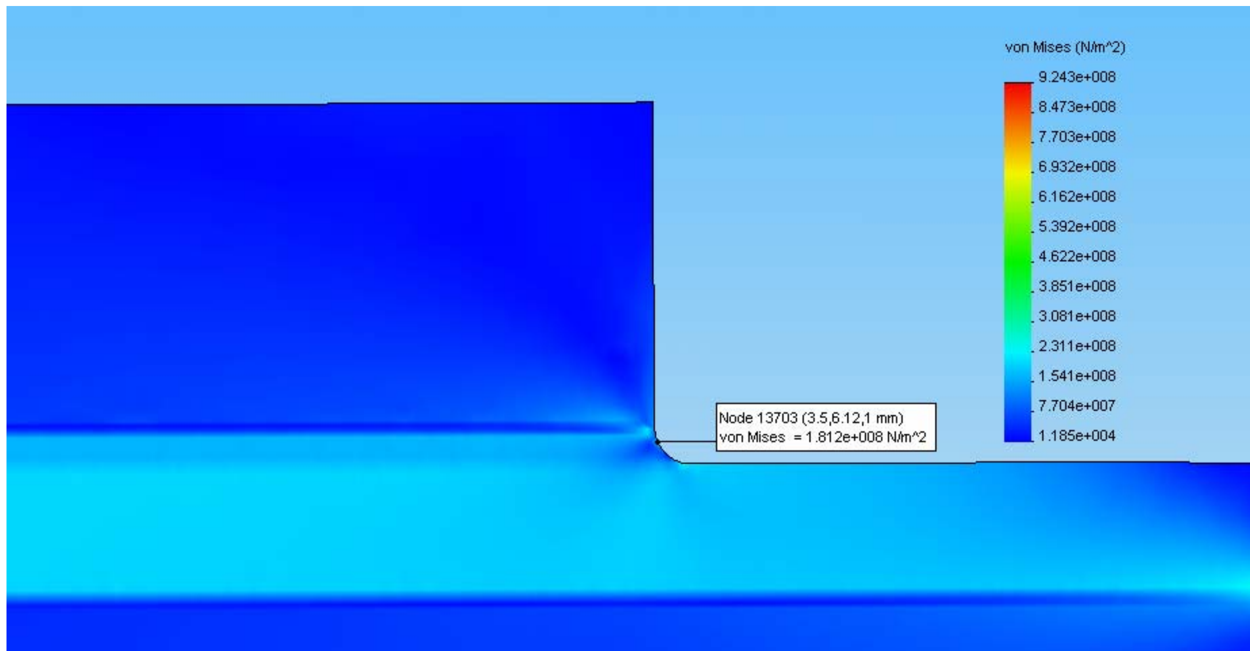



**Figure 15. Concept 3 – 2D Stress Profile of Solder Layer**

because of fatigue failure in the solder layer. The principle stress at the edge of the solder layer is 186 MPa, which indicates that the solder will not fail in a brittle manner, even if this turns out to be the primary failure mode.

It is not immediately obvious why the stress levels were different between Concept 3 and Concept 2. Both the substrate layers were 1 mm thick and both used a gold conductor metallization. The semiconductor was attached to the substrate by gold-silicon solder in both cases. The difference turns out to be in the way the model of the package was constrained. Concept 2 was held flat against a stiff aluminum heat sink. Because the package was held flat against a surface, the stresses at the die edge were higher than if the package were unrestrained and able to warp. In Concept 3, there was no restraining heat sink, so the package was free to warp slightly due to the difference in the CTE of the AlN substrate and the AlSiC base plate/heat sink. The CTE of the AlSiC was higher, so the package warps very slightly toward the semiconductor die, lowering the stresses at the die edge. In reality, both packages warp slightly due to CTE mismatches, but Concept 3 will warp more because 1) the base of the AlSiC heat sink in Concept 3 is thicker than the AlSiC base plate of Concept 2, and 2) the aluminum heat sink in Concept 2 is not metallurgically attached to the base plate, so the package does not warp under the influence of the aluminum heat sink, but is restrained to a nearly flat plane instead.

### *7.5.5 Conclusions on Concept 3*

This package may be the most expensive of the three concepts to produce because it uses AlSiC for the heat sink instead of aluminum, but all three were designed with low cost in mind. At the same time, because the thermal resistance of the mechanical interface between the base plate and the heat sink that plagues the first two concepts were absent from this one, the package can be about half the size of the first two concepts to dissipate the same amount of heat. This package concept also seems to produce the lowest thermal stress and is predicted to have the best reliability of the three packages, though all the packaging concepts and prototypes will have to be built and thermally cycled before any conclusions about package reliability can be finalized.

## 7.6 Summary of Concept Evaluation

Table 15 compares the stress in the critical areas for each of the three concepts. Of these concepts, Concept 3 has the most potential to turn into a reliable package. Packaging Concept 2 is less optimal due to the stress levels in the solder layer, but with careful design, this concept could represent the best compromise between cost and performance.

## 7.7 1.5 MW Converters Using Silicon and SiC Devices

The baseline power electronics converter is comprised of back-to-back inverters, as shown in Figure 1. The primary parts of any converter (not including the filter inductor) are the power semiconductor blocks with heat sinks, the DC bus capacitors, one or more control boards, and an enclosure with a variety of auxiliary components, such as terminal blocks, breakers, fuses, wires, standoffs, and so on. The use of SiC devices impacts the two power semiconductor blocks only,

**Table 15. Stress Comparison of Concepts**

| | Substrate Stress (MPa) | Max Allowable (MPa) | Solder Stress (MPa) | Max Allowable (MPa) |
|---|---|---|---|---|
| **Concept 1** | 156.0 | 310 | 440.5 | 255 |
| **Concept 2** | 68.6 | 310 | 252.0 | 255 |
| **Concept 3** | 64.6 | 310 | 181.2 | 255 |

but these are the most dominant and costly components. Designs are presented here for two power semiconductor blocks for a six-device inverter, one using silicon and other SiC. They are shown in Figures 5 and Figure 16.

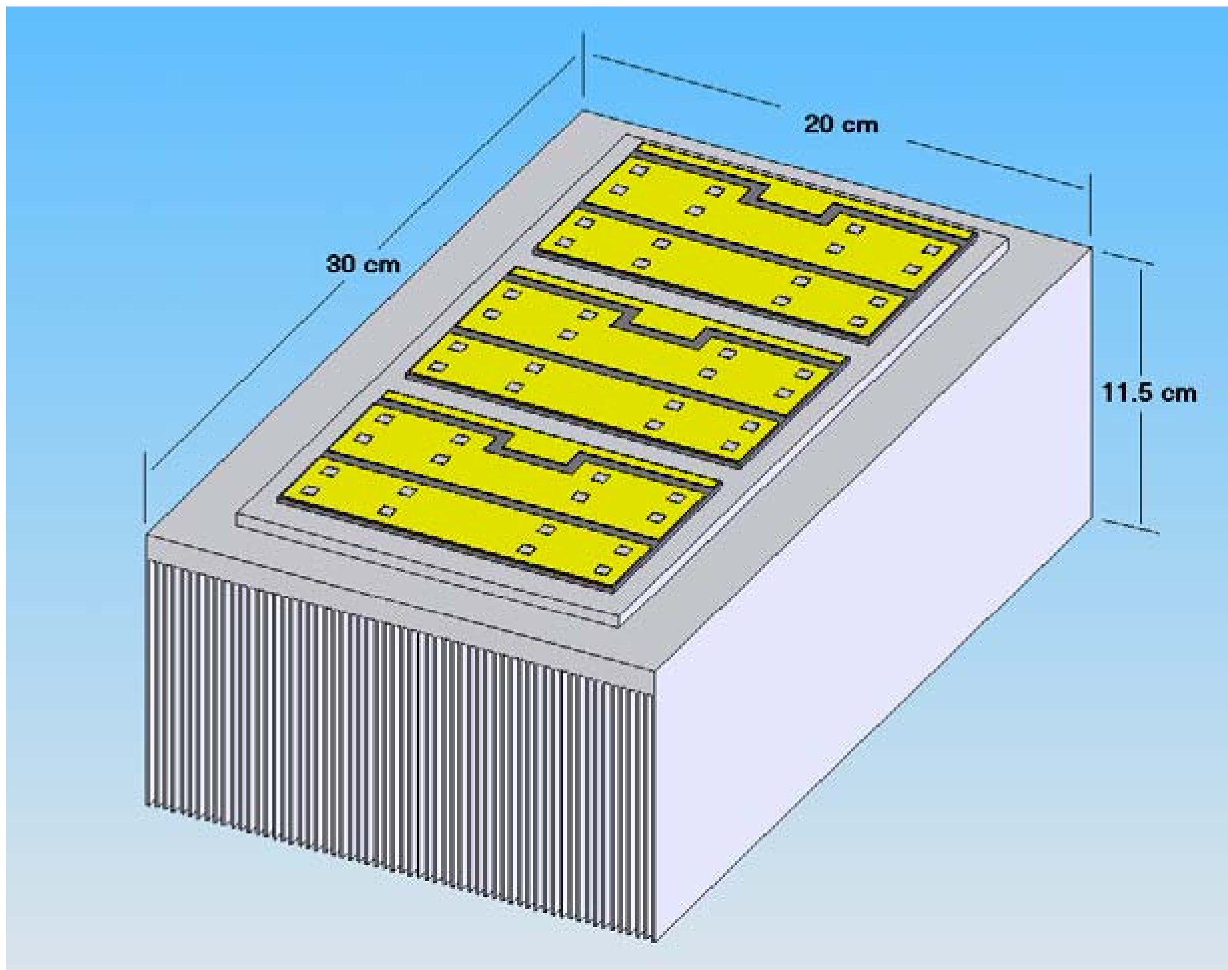



**Figure 16. 1.5 MW SiC-Based Inverter, 4,160 VAC, 208 amps, 300ºC**

### 7.7.1 Silicon Based Inverter - 1.5 MW, 690 VAC, 1255 Amps, 3 kHz Switching, 1.5% Losses, 125ºC Limit

Rather than designing the semiconductor blocks anew in this project, a standard commercial module from Semikron is used. This product is designated 342GD120-314CTV6 and was shown in Figure 5. This is a state-of-the-art commercial inverter used in a variety of products now in the market, including a product developed by the principal investigator's engineering team. When switching in the 3 to 5 kHz range, it is capable of handling currents of about 200 amps rms, so at least six of these modules would need to be paralleled to achieve the 1255 amps required at 690 V.

Semikron and other suppliers have IGBT products that can handle much higher current. Higher rated modules could be readily designed, but the losses and size/weight of heat removal hardware would be similar. The total die area would be similar, and a fin design that has been optimized for the smaller module would still represent the optimum for a higher power module. The heat sinks would have greater lateral area in proportion to the current being carried. The use of the Semikron module ensures that the silicon version of the inverter is reasonable and competitive, and can be validly compared to a SiC version.

### 7.7.2 SiC-Based Inverter - 1.5 MW, 4,160 VAC, 208 Amps, 3 kHz, 0.5% Losses, 300 ºC Limit

This inverter has been completely redesigned according to the results in this project. Operation at 4,160 VAC will require devices rated at about 10,000 V, which is made possible by SiC. No special measures need to be incorporated, such as multilevel circuits; only six devices per inverter bridge are needed. High speed switching (only 3 kHz in this project) is still possible at the higher voltage due to the high speed capability of a SiC device. The thermal modeling uses a die temperature of 300 °C, also enabled by SiC. Note that 10,000 V prototype SiC devices have been produced not only in MOSFET form (more limited in temperature) but also BJT and JFET form. Both SiC Schottky and SiC PN junction diodes have also been produced in prototype form at comparable voltages. Lesser voltage levels in the medium-voltage category (2,300 V, for example) could be used as a stepping stone to 4,160 V, but 4,160 V is clearly feasible in time.

The obvious result was the SiC-based inverter is one-sixth the size of the silicon-based inverter. That is, the entire SiC-based inverter was basically the same size as a single SKiiP module that used silicon IGBTs. The size reduction was due approximately half to higher efficiency and half to higher temperature. The inverter used Concept 3, as described above. We project the inverter will be feasible in all respects in the next three to five years, assuming appropriate development effort and resources are expended. The cost is still highly uncertain, however. All components of the SiC-based inverter will undoubtedly be more expensive on a per-pound basis, but the dramatic reduction in material could lead to a lower net cost. For lower cost to be achieved, reasonable production volume and the supporting infrastructure would have to evolve.

In addition, the higher voltage enabled by SiC will lead to major cost reductions elsewhere in the wind turbine since it will reduce currents substantially in all other electrical power equipment,

such as the generator, filter elements, and transformer. This conclusion dovetails with the conclusions of other parallel work sponsored by NREL in which higher voltages are being studied for multi-megawatt wind turbines [8]. To achieve higher voltage with silicon devices would require design features that would be more costly. For example, the designer might use, as examples, a multi-level inverter with either (a) a three or four level, diode clamped bridge or (b) six level cascaded bridge (similar to the Robicon 4,160 V drive). These all require many more power semiconductors and complex hardware for connectivity. In addition, switching speeds would be more limited with standard silicon compared to any type of SiC device.

The development of this inverter is recommended in subsequent work.

### *7.7.3 High Temperature Electronics – Other Components*

In some respects, it is misleading to consider only the high temperature capability of power semiconductors and the adjacent packaging materials. Power converters are made up of many other temperature sensitive elements. For example, a converter for wind turbines, in addition to the power semiconductor block, requires gate driver circuits, DC bus capacitors, control boards, inductors, and sensors, all of which have troublesome temperature limits. Because the silicon devices have historically imposed the limiting temperature, higher temperature capability in the other components would have been wasted. They have not evolved very far with regard to temperature. Depending on the application, an attempt to boost the temperature of the power devices might require solving the problems with the other components too.

In some applications (automobiles, deep hole drilling, and space/aviation, all of the converter components are integrated tightly into a relatively small volume. Those applications might also involve an inherently high temperature environment and would be a serious challenge in realizing the 300°C goal in this project. However, this is not the case for wind turbines where the power level is high and the relatively large subsystems are not integrated tightly. Moreover, an inherently high temperature environment was not present. The protection of the other temperature sensitive components was fairly straight-forward using spacing and modest amounts of thermal insulation.

However, comments will be necessary to status the other components since more and more integration of high temperature components can be expected over the years ahead.

***Printed Circuit Boards.*** The controls and gate drive circuits use printed circuit boards that cannot operate even close to 300ºC if standard materials are used. They are usually made of so-called FR-4, which is limited in temperature to about 400°F (204°C). Higher temperature board materials (polyimide, e.g.) are available for temperatures to about 260ºC. From there on, one can use DBC, as described earlier. DBC is in fact commonly used for high temperature circuit boards since it can be readily masked and etched like a standard printed circuit board. DBC can be used at over 600°C, far higher than would be needed in a wind turbine.

***Solder.*** High temperature solders were discussed earlier.

***Capacitors.*** Typical DC and AC capacitors used in industrial power electronics have thermal limits that are significantly lower than silicon power devices–approximately 95ºC. The same industries that are trying to increase the temperature limits of semiconductors (automobile suppliers, aircraft designers, and deep well drillers) are encouraging the development of high temperature capacitors. Significant advancements are being made here by a number of companies. An example is Johanson Dielectrics Inc. in California, who just introduced a line of capacitors for operation at 250°C. Plans to develop capacitors that can withstand over 300°C during the next year are in progress. This is made possible by new materials, including better dielectrics.

***Passive components – inductors.*** Inductors are also being addressed by important potential users, such as the Air Force. One might assume the temperature limit is set by insulation, but that is not the case. Some insulating materials, such as ceramics, can withstand very high temperatures. The problem is primarily one of maintaining magnetic properties at high temperature so as to avoid saturation and other negative effects. Inductors are available at over 225°C and this can be expected to increase substantially over the next several years.

***Logic devises and ICs.*** Many logic devices are amenable to SOI design and manufacturing techniques, which will permit them to operate at up to 250ºC. One of the primary problems with silicon devices is excessive leakage current with higher temperatures. By using a special geometry, SOI minimizes the leakage area by a factor of up to 100, thereby making the leakage acceptable to higher temperatures and possibly raising the temperature limit to 300°C. As the current level is increased, this approach is less and less effective, so it cannot be used in the high power circuits of any of the converters discussed in this report. At least one logic device fabrication facility (Honeywell in Minneapolis) is dedicated to SOI design and production, largely for the automotive and deep well drilling markets.

***Integrated electronic systems.*** The pursuant question is whether or not entire converters or other high power electronics systems can be developed and are capable of operating in an environment that heat saturates all elements at a temperature of 300°C. The answer is no. The major deficiencies include the power semiconductor block, which might be solved by this project and other work Peregrine is currently conducting. But even if an entire high power electronics system were possible, it would not likely be cost justified in a wind turbine. At this early stage, every single component would cost at least several times the cost of more conventional components. The proper course would be to design the power device block for a temperature well over 300°C with SiC power semiconductors, thereby reducing size and cost. For the rest of the converter, the proper design course would be to use standard, inexpensive components that are thermally isolated from the power block. As indicated before, high temperature is not an objective in the wind turbine, only low cost.

# 8.0 COSTS & COST OF ENERGY

Attempting to determine costs of any major component in a converter using SiC devices has been frustrating and to some extent unsuccessful. Table 16 gives the best estimate today of the impact on COE with the use of SiC devices. This reflects an increase in energy production of 2.4% with no change in capital or operating cost. This estimate is believed to be conservative relative to the outcome after (1) SiC devices have matured, (2) a commercial infrastructure has been put in place, (3) production volume has developed, and (4) the wind turbine design has been modified to exploit SiC, particularly high-voltage capability.

A determination of capital cost has been difficult for the following reasons:

- No organizations produce any type of SiC device, with the exception of SiC Schottky diodes, on a commercial scale. Even the market for Schottky diodes is not yet active and competitive. Current prices are not likely representative of a more mature product in five years. On the other hand, because useable prototypes are being produced regularly by several potential suppliers, basic feasibility does not seem to be in doubt. They can be purchased, but they lack necessary uniformity and are produced with equipment that is not capable of commercial volumes. With the exception of Schottkys, the suppliers will not warrant performance or long-term reliability. This is expected to change during the next 24 months, but meaningful prices are not available today.

- With the defect levels in SiC wafers being experienced today, current ratings are low–perhaps up to 15 to 20 amps for an active device and up to 100 amps for a diode. Production yields are low and the processes are not highly optimized. Conversely, no product has a cost more directly tied to yield levels and volume than the semiconductor. In spite of the absence of meaningful cost information, the fundamentals of semiconductor fabrication along with competitive pressures, lead one to be optimistic about ultimate prices.

- Unknown and potential prices for SiC devices is only part of the cost problem in this project. The rest of the materials in a high temperature device package and inverter block, along with the processes for fabricating a product, are all new. The packaging is a multidisciplinary endeavor with fragmented technologies and little or no supporting infrastructure. The only way to develop realistic projections of price would be to actually build and test fully integrated prototypes. This would allow the designer to determine which materials and processes could actually be used and to work directly with the suppliers of each component or fabrication service with the costing of a specific product in mind. No one today is in a position to contribute intelligently to a cost projection. However, with a reduction in the size and weight of the inverter block by a factor of six, it would appear that the probability of an overall reduction in cost might be achieved.

- Finally, the cost impact of using 4,160 V, as enabled by SiC devices, requires work well beyond that outlined in the statement of work. That work includes

determining the cost of all wind turbine components that are impacted (generator, filters, wires, breakers, etc.) as well as the cost of the converter.

## Table 15. COE PROJECTION WORK SHEET

**Baseline Turbine: 1.5 MW - 3 Bladed Upwind/Pitch Controlled/Single PM Generator with Silicon-Based Converter**
**Improved Turbine: Same except SiC-Based Converter**

| Component | Baseline Component Costs $1000 | Projected Component Costs $1000 | Component Percent Improvement | Major Cost Element % Improvement |
|---|---|---|---|---|
| **Rating (kWs)** | 1500 | 1500 | | |
| **Rotor** | **248** | **248** | 0.0% | |
| Blades | 148 | 148 | 0.0% | |
| Hub | 64 | 64 | 0.0% | |
| Pitch mchnsm & bearings | 36 | 36 | 0.0% | |
| **Drive train,nacelle** | **563** | **563** | 0.0% | |
| Low speed shaft | 20 | 20 | 0.0% | |
| Bearings | 12 | 12 | 0.0% | |
| Gearbox | 151 | 151 | 0.0% | |
| Mech brake, HS cpling etc | 3 | 3 | 0.0% | |
| Generator | 98 | 98 | 0.0% | |
| Variable spd electronics | 101 | 101 | 0.0% | |
| Yaw drive & bearing | 12 | 12 | 0.0% | |
| Main frame | 64 | 64 | 0.0% | |
| Electrical connections | 60 | 60 | 0.0% | |
| Hydraulic system | 7 | 7 | 0.0% | |
| Nacelle cover | 36 | 36 | 0.0% | |
| **Control, safety system** | **10** | **10** | 0.0% | |
| **Tower** | **101** | **101** | 0.0% | |
| **TURBINE CAPITAL COST (TCC)** | **921** | **921** | 0.0% | 0.0% |
| | | | | |
| Foundations | 49 | 49 | 0.0% | |
| Transportation | 51 | 51 | 0.0% | |
| Roads, civil works | 79 | 79 | 0.0% | |
| Assembly & installation | 51 | 51 | 0.0% | |
| Elect interfc/connect | 127 | 127 | 0.0% | |
| Permits, engineering | 33 | 33 | 0.0% | |
| **BALANCE OF STATION COST (BOS)** | **388** | **388** | 0.0% | 0.0% |
| | | | | |
| **Project Uncertainty** | **162** | **162** | 0.0% | |
| | | | | |
| **Initial capital cost (ICC)** | **1,472** | **1,472** | 0.0% | |
| **Installed Cost per kW for 1.5 MW turbine (cost in $)** | **981** | **981** | 0.0% | |
| **Turbine Capital per kW sans BOS (cost in $)** | **690** | **690** | 0.0% | |
| **LEVELIZED REPLACEMENT COSTS (LRC) ($10.7 kW)** | 16 | 16 | 0.0% | 0.0% |
| **O&M $20/kW/Yr (O&M)** | 30 | 30 | 0.0% | 0.0% |
| **Land ($/year/turbine)** | 5 | 5 | 0.0% | |
| **NET 5.8 m/s ANNUAL ENERGY PRODUCTION MWh (AEP)** | 4439 | 4546 | 2.4% | 2.4% |
| **Net 8 m/s ANNUAL ENERGY PRODUCTION Energy MWh (AEP)** | 5519 | 5651 | 2.4% | 2.4% |
| **Fixed Charge Rate** | 11.85% | | | |
| **COE at 5.8 m/s $/kWh** | **0.0480** | **0.0469** | -2.3% | |
| **COE at 8.4 m/s $/kWh** | **0.0386** | **0.0377** | -2.3% | |

DAM06/15/05

# 9.0 CONCLUSIONS & RECOMMENDATIONS

## 9.1 Major Conclusions

The major conclusions can be put in question and answer form:

- ***Will appropriate SiC devices be available commercially during the next five years?*** Yes. After over 20 years of development, SiC devices are nearing commercial readiness. First generation Schottky diodes are in the market now and are available at up to 1,200 V and 100 amps. SiC PN junction diodes have had some development problems (degradation of properties with usage), but progress is being made; introduction can be expected during the next 24 months. Active SiC devices rated at up to 1200 V are nearing commercial introduction. Considerable amount of investment has been made especially in the SiC MOSFET, which is perhaps 18 months away from commercial introduction by Cree. During the 24 months after that, other devices, such as the BJT, can be commercialized, assuming the proper development support. JFETs also are nearing readiness, but they are highly disfavored in some applications due to their normally-on characteristic. Since prototype SiC MOSFETs, BJTs and JFETs are now available, work on some commercial applications is highly justified. However, development work on SiC IGBT applications is not yet justified since this device will not be ready until after the five-year time horizon of this project.

- ***Will SiC devices facilitate the needed increase in voltage in large wind turbines?*** Yes. SiC MOSFETs and most other SiC devices can be rated at over 10,000 V and will be usable in a wide variety of medium voltage applications. For a converter rated at 4,160 VAC (standard industrial voltage), devices rated at 10,000 V are needed. The development of such high voltage devices is underway, but a couple of additional years can be added for their likely introduction, relative to lower voltage versions. This still puts some potential medium voltage applications of SiC devices within (barely) the five year horizon of the project, if proper support is given. The SiC IGBT should be capable of blocking over 20,000 V, but its introduction will be significantly beyond the five year horizon. .

- ***Is the ampacity of available prototype SiC devices sufficient for the converters of large wind turbines?*** Close, but not quite. Ampacity of currently available SiC devices of all types is sharply limited by high defect levels in the SiC wafers. Ampacity at 1,200 V is in the 5 to 20-amp range for active devices and perhaps 100 amps for passive devices. SiC device developers are focusing on the defect problem, and a substantial reduction in defects with associated increase in yields can be expected over the next several years. Most SiC die can be readily paralleled to achieve higher current levels. Note that a 1.5 MW converter handles only 208 amps when operating at 4,160 VAC. Only 14 paralleled die of the type tested in this project, could handle that if the voltage blocking capability were increased to 10,000 V. It is common for 10 IGBT dies to be paralleled in an inverter module.

- ***What will be the price of a SiC device?*** Since active SiC devices are not sold commercially, no prices are available as bench marks. For the next several years, prices will be high and SiC devices will be used only in highly specialized applications that require their unique capabilities–high temperature, high voltage, or high switching speed. The supply of SiC devices will remain concentrated in the hands of a few organizations, particularly Cree, for at least several years. Eventually, the market for SiC power devices will be competitive because (a) at least half a dozen organizations in the United States, Europe, and Japan intend to be commercial suppliers, (b) yields will increase significantly as defect levels drop, (c) a commercial production infrastructure will be established, and (d) volume will develop. The price of a bare die does not tell the full story, however. Also critical to the cost of using SiC is the cost of the device and inverter package, in addition to the cost impact on other major components in an overall energy system.

  ***What will be the performance impact of a SiC based converter in a wind turbine?*** SiC MOSFETs will reduce total losses (conduction and switching) in an inverter bridge operating at 690 V by a factor or 2 or 3 compared to a comparable bridge using silicon IGBTs when both inverter bridges are switching at a frequency of 3 kHz. SiC MOSFETs will enable the operation of an inverter at 4,160 V, thereby reducing conduction losses further. But the losses in the baseline converter using silicon IGBTs are already fairly low–only about 4.5%, 1.2 % of which is in the filter inductor. The losses in each of the two silicon based inverter bridges are in the 1.6% area and this figure is expected to be reduced to the 0.5% area using SiC devices. The bottom line impact when using SiC devices is a calculated increase in energy production of about 2.4%.This is impressive considering there is only about 3.3% in device losses to be had. These figures are small and subject to potential modeling inaccuracies; the figure in the first decimal place should not be regarded as accurate. The best characterization of SiC performance is a 2% to 3% energy production gain.

- ***Is there any alternative to a full SiC based converter that represents a "baby step" in the direction of SiC exploitation?*** Yes. Several organizations report that total switching losses in an inverter can be reduced by 30% to 50% when switching at typical frequencies if the standard silicon free wheeling diode is replaced with a SiC Schottky diode. This translates to 15% to 25%of the total (conduction and switching) losses if the conduction and losses are equal, as they are (approximately) in a converter for wind turbines switching at 3 kHz. In the baseline converter, this translates to a 0.4% increase in average efficiency and energy production. This may not be sufficiently large to justify pursuing. In addition, the temperature of the package cannot be increased due to the presence of the silicon transistor. Therefore, the reduction in material and potentially cost would not be substantial. Since silicon IGBT/SiC Schottky packages are now being developed by several power semiconductor suppliers, they should be available to evaluate soon. If the prices are competitive (not likely yet), this might

be a good approach, but it is expected that these packages will be most advantageous in applications where the switching speeds are much higher than found in a wind turbine.

- ***Will SiC devices solve the problem of low converter efficiency at low power?*** The reduction in losses in the SiC based converter is larger at low power because the conduction losses in a MOSFET, unlike an IGBT, are proportional to current level and because the reverse recovery current is minimal in a SiC Schottky. This would seem to benefit a wind turbine, which operates most of the time at low wind speed, but the benefit might be diluted by the low energy production at low wind speed and low efficiency of the generator and gearbox at low power. Conversely, a shift to direct drive PM generators would eliminate the gearbox efficiency curve entirely and enable the use of generator designs that have peak efficiencies at less than full power. Low power improvements are particularly important given the NREL objective of increasing overall efficiency at sites with lower speed wind regimes.

- ***How can SiC devices be used to maximum advantage in a wind turbine?*** The optimum strategy for using SiC devices is to exploit their unique, superior characteristics–high voltage, high temperature, or high switching speed. They should not be used as one-for-one replacements of silicon IGBTs in 690 V converters. Rather than having the baseline wind turbine determine how SiC devices are applied, the capabilities of SiC should determine the conditions for the other equipment in the baseline turbine. Specifically, the voltage of the entire electrical system should be increased to 4,160 V, which is enabled without any special measures by SiC devices. This strategy may dovetail with the results of other NREL work, which recommends increasing the voltage level of multi-megawatt wind turbines.

- ***How can the high temperature capability of SiC devices be exploited?*** Wind turbines do not inherently require high temperature capability, but material and potential cost can be reduced if the SiC device is permitted to operate at a much higher temperature, such as 300°C. High temperature packaging for wide band gap power semiconductors is not currently available. However, a 300°C package is believed to be feasible now; that is, technologies exist in various fields that can be pulled together to accomplish this. Although there is considerable work being carried out to increase the temperature of signal level electronics, the team knows of no significant project to develop an entire high temperature power device and inverter package. Due to the extraordinary reduction in size achieved with such a package, the development of a high temperature SiC-based inverter for wind turbines is highly recommended.

- ***What is the expected impact on size and material when exploiting the unique capabilities of SiC devices?*** When the impact of both the efficiency and temperature improvements due to SiC are considered, a SiC-based inverter block at medium voltage will be reduced in size by a factor of about six, relative to its

690 V, silicon IGBT counterpart. While the cost of the SiC-based inverter cannot be determined now due to uncertainties in the cost of SiC dies, packaging materials, and fabrication processes, this remarkable reduction in material will tend to offset any increase in the unit cost for material. In addition, the increase in voltage enabled by SiC will favorably impact the cost of other major electrical components, such as the generator.

## 9.2 Recommended Follow-Up Work

The team believes that a high temperature inverter module rated for operation at 4,160 V rms could be demonstrated within three years from these results with sufficient focus and resources. A single, six-device inverter block that can handle 1.5 MW would be 6 inches by 8 inches by 12 inches in size. Other, smaller modules might be more cost effective to fabricate, but a reduction in size by a factor of six, relative to a silicon IGBT based inverter, would be achieved. This would likely lead to a cost reduction in the power electronics and enable much higher voltages that would favorably impact the cost of other wind turbine components.

The following general tasks are recommended:

- Develop high-voltage devices. The project team should work with one or more potential suppliers of SiC devices in specifying and obtaining appropriate devices for use in a 2,300 V or 4,160 V converter. The potential suppliers include (but are not limited to) Cree, Purdue University, and United Silicon Carbide.

- Characterize, model, and project performance. Once obtained, they should be characterized and modeled, as performed in this project. Performance will again be projected, but this time for high-voltage inverters.

- Develop and test high temperature device/inverter package. A high temperature and high-voltage inverter module that can be used in the baseline wind turbine would be designed in detail, fabricated, and tested. The inverter module would be rated for 4,160 V, at least 500 kW, and 300ºC. The inverter module would be based on Concept 3 described earlier. The team would select appropriate materials, fabrication processes, and vendors.

- Develop pricing. Pricing of the package would be developed with the assistance of the final vendors to support an accurate COE calculation for wind turbines.

Already a consortium of eight companies led by Alstom (called "ESCAPEE") has been organized in Europe to give European companies a commercial advantage in the international market in applying SiC technology in power electronics. Continuing work in this project will give substantial timing advantages to Peregrine and other U.S. companies in developing and manufacturing SiC-based power converters for energy generation systems and other applications.

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# APPENDIX

## Documents from University of Tennessee
## Characterizing SiC Devices

1. "High Temperature and High-Frequency Performance Evaluation of 4H-SiC Unipolar Power Devices", Leon M. Tolbert et al, University of Tennessee and Oak Ridge National Laboratory (2005)

2. "Enhancing Power Electronic Devices with Wide Bandgap Semiconductors", Presentation at Workshop in Aruba on Frontiers in Electronics (2004), Leon M. Tolbert and Burak Ozpineci, University of Tennessee and Oak Ridge National Laboratory

3. "Power Losses for Si- and SiC-Based Back-to-back Inverter in Wind Generation Application", Leon M. Tolbert et al, University of Tennessee (2005)

4. Spreadsheets for Performance Calculations for Converter for Wind Turbine, University of Tennessee (2005)

# High-Temperature and High-Frequency Performance Evaluation of 4H-SiC Unipolar Power Devices

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***Abstract*- Silicon carbide (SiC) unipolar devices have much higher breakdown voltages because of the 10 times greater electric field strength compared with Silicon (Si). 4H-SiC unipolar devices have higher switching speeds due to the higher bulk mobility of 4H-SiC compared to other ploytypes. Four commercially available SiC Schottky diodes at different voltage and current ratings, an experimental SiC VJFET and MOSFET samples have been tested to characterize their performance at different temperatures. Their forward characteristics and switching characteristics in a temperature range of -50°C to 175°C are presented. The results for the SiC Schottky diodes are compared with the results for a Si pn diode with comparable ratings. A gate drive designed using a commercially available gate drive chip is presented. The experimental data was analyzed to obtain the device performance parameters like the on-state resistance, device switching times and the switching losses.**

## I. INTRODUCTION

With the increase in demand for more efficient, higher power, and higher temperature operation in several power electronic applications, the design engineers face the challenge of increasing the efficiency and power density of converters. Increasing the frequency of operation provides significant increase in system efficiency and results in compact design of the system. Also, the high temperature operation capability increases the power density due to, reduced thermal management and heat sink requirements. An increase in power density results in reduced weight and cost benefits. Development in power semiconductors is vital for achieving the design goals set by the industry. Currently, the Si based converters are in-efficient and require higher cooling requirements in spite of the advanced converter technologies like soft switching being used. Si power devices have been saturated in terms of higher temperature and higher power operation by virtue of their physical properties. SiC is is the best transition material compared to other wide band gap materials like GaN and diamond [1, 2]. Silicon carbide (SiC) has been identified as a material with the potential to replace Si devices due to their superior material advantages such as large bandgap, high thermal conductivity, and high critical breakdown field strength. SiC devices are capable of operating at higher voltages, higher frequencies, and at higher junction temperatures. SiC unipolar devices such as Schottky diodes, VJFETs, MOSFETs have much higher breakdown voltages (600V-3kV) compared to their Si counterparts which, make them suitable for use in medium voltage applications. At present, SiC Schottky diodes are the only commercially available SiC devices. These diodes have been used in several applications, and have proved to increase the system efficiency compared with Si device performance [3]. Significant reduction in weight and size of SiC power converters with an increase in the efficiency is projected [1, 2]. There are several hard switched converters using SiC switches designed for high power, high frequency and high temperature operation. The performance of these converters has been compared to be better than traditional Si converters [4, 5].

The gate drive design is an important aspect of the converter design which contributes to the device performance and hence the system. The SiC power switches in the converters listed above and some SiC VJFETs reported in [6, 7] were switched using use several gate drive circuits designed using discrete devices. However, in the circuit design presented in this paper, a commercial gate drive IC chip IXDD414 is used which, makes it more reliable in operation. These gate drives can be applied to SiC MOSFETs and also VJFETs by redesigning the passive components and modifying the output voltage polarity. The choice of the semiconductor device is very much application specific and with several devices available in the market it is always a challenge. This paper presents the characteristics curves for several diodes and power switches, and compares their performance. Most of the applications require that devices be able to handle extreme environments which include a wide range of operating temperature. In the following sections, the static and dynamic performance, for a wide temperature range, of some commercially available SiC Schottky diodes and experimental samples of SiC VJFETs and MOSFETs will be presented.

## II. SiC SCHOTTKY DIODES

SiC Schottky diodes are majority carrier devices and are attractive for high frequency applications because they have lower switching losses compared to pn diodes. However, Schottky diodes have higher leakage currents, which affect the breakdown voltage rating of the device [8]. A list of SiC

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Schottky diodes tested are S1 (1200V, 7.5A), S2 (600V, 4A), S3 (600 V, 10 A), and S4 (300 V, 10A).

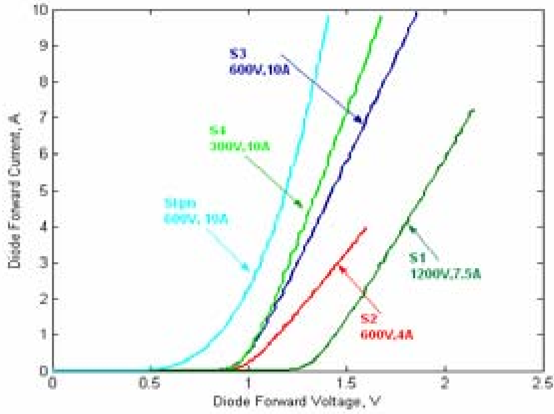



**Fig. 1.** *i-v* characteristics of Si pn and SiC Schottky diodes at 27°C.

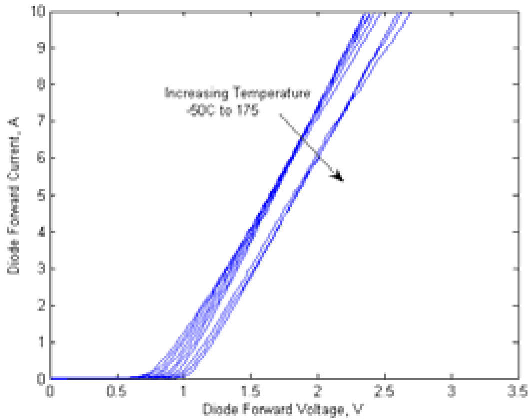



**Fig. 2.** *i-v* characteristics of S4 (300V, 10A) at different operating temperatures.

*A. Static Characteristics*

The static characteristics of different SiC Schottky diodes at room temperature are shown in Fig. 1. The threshold voltage or the knee voltage and the on-state resistance is different for the diodes because of differences in device dimensions for different ratings. Also, the threshold voltage varies with the contact metal used in the Schottky diodes because of the variation in the Fermi level for different metal to semiconductor contacts. The static characteristics of one of the diodes for a temperature range of -50°C to 175°C is shown in Fig. 2. The on-state voltage drop of a Schottky diode is dependent on barrier height and the on-state resistance. Both parameters vary with temperature and hence contribute to the temperature dependence of forward characteristics.

At lower current levels the built-in potential (barrier potential) decreases with increasing temperature due to reduction in barrier height [9]. As the temperature increases, the thermal energy of electrons increase which causes lowering of the barrier height. The on-state voltage drop of the diode is given as,

$$V_f = V_d + I_d \cdot R_d \tag{1}$$

where $V_d$ is the forward voltage drop and $R_d$ is the series resistance of the diode obtained from the piece-wise linear (PWL) model of the diode. The PWL model parameters were extracted from the experimental data. The variation in $V_d$ with temperature is plotted in Fig. 3.

At higher current levels the voltage drop is mainly due to the series resistance of the diode. The on-state resistance is one of the critical parameters, which determines the performance of the device and is a temperature sensitive parameter. $R_{on,sp}$ increases with temperature due to decrease in mobility at higher temperatures. The positive temperature coefficient characteristic increases the conduction losses at high temperatures; however, this is advantageous for current sharing and paralleling.

The $R_d$ for the diodes was calculated from the slope of the *i-v* characteristics and is plotted for different temperatures as shown in Fig. 4. The on-state resistance varies for each diode due to the difference in blocking voltages. The $R_{on,sp}$ for majority carrier devices can be expressed as a function of breakdown voltage and critical electric field.

$$R_{on,sp} = \frac{4V_B^2}{\varepsilon \ (E_c)^3 \mu_n} \tag{2}$$

where $\varepsilon$ is the permittivity (C/V·cm), $V_B$ is the breakdown voltage, $E_c$ is the breakdown field (V/cm), and $\mu_n$ is the electron mobility (cm$^2$/V·s). To withstand high breakdown voltages, the blocking layer thickness is increased, and doping concentrations are reduced. This results in increased series resistance of the diode. Hence, device S1 rated at 1200V, 7.5A has more on-resistance compared to S3 and S4. The resistance varies with forward current density and the area of the device. It is evident from Fig. 4 that S2 and S3 with the same voltage and different current ratings have different on-state resistances.

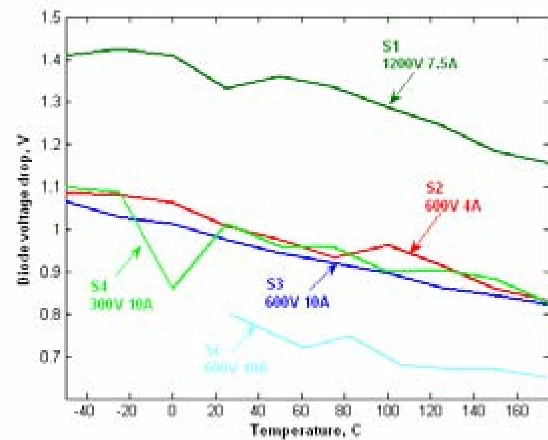



**Fig. 3.** $V_d$ for Si and SiC diodes at different operating temperatures.

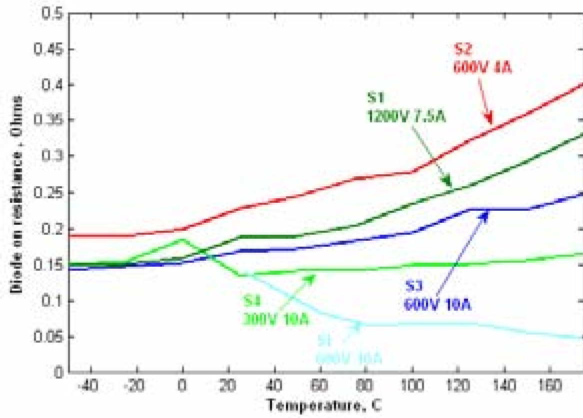



**Fig. 4.** $R_d$ for Si and SiC diodes at different operating temperatures.

*B. Dynamic Characteristics*

A buck chopper with an inductive load is built for evaluating the switching characteristics of the diodes. An IGBT is used as the main switch and is switched at 20 kHz with a 25% duty ratio.

The power losses for various forward peak currents and different temperatures are shown for the Si diode and diode S4 in Fig. 5. The power losses for the Si diode increase with temperature, because of the increase in peak reverse recovery current. The switching loss for diode S4 is almost independent of the change in temperature. The reverse recovery current is dependent on charge stored in the drift region. The SiC Schottky diode has no stored charge because it is a majority carrier device, and hence has virtually constant

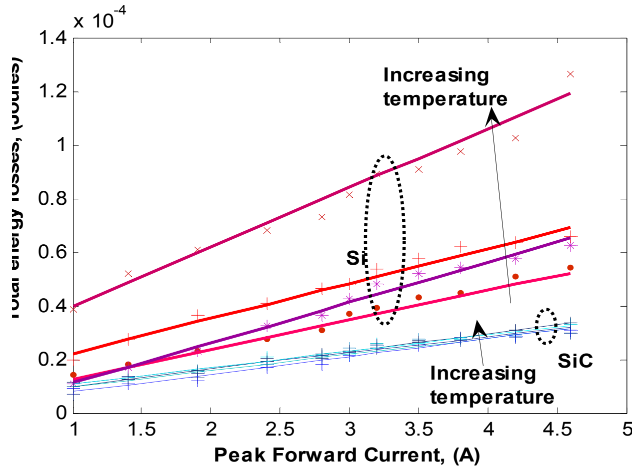



**Fig. 5.** Total energy losses with respect to forward current at different operating temperatures.

on energy loss for a wide temperature range. The negligible reverse recovery current reduces the oscillation due to ringing and also eliminates the need for a snubber for limiting the reverse recovery.

This results in increased efficiency as the losses are minimized. Also, the reduced blocking layer thickness, due to the wide band gap of the SiC material, contributes to the low switching losses of the SiC diode.

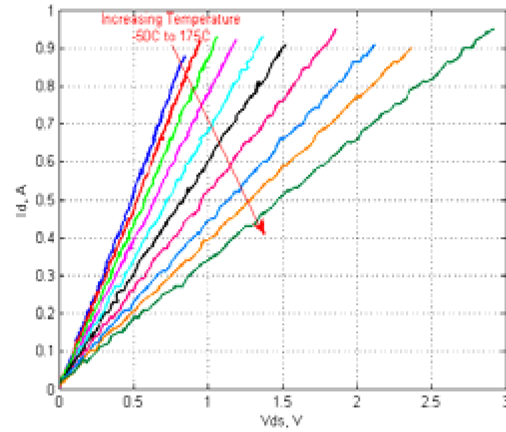



**Fig. 6.** *i-v* characteristics of SiC VJFET at different temperatures.

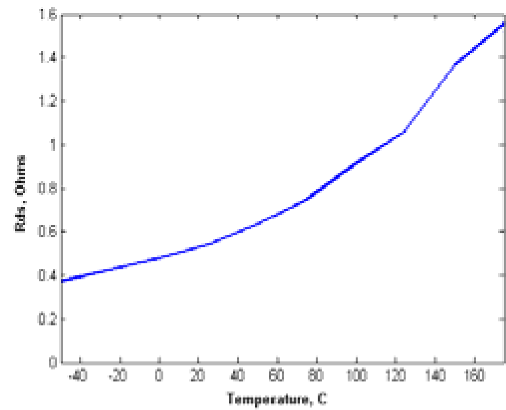



**Fig. 7.** On resistance of SiC VJFET at different temperatures.

## III .STATIC CHARACTERISTICS

*A. SiC Vertical JFET (VJFET)*

JFET is a unipolar device and has several advantages compared to MOSFET devices. JFET has low voltage drop and higher switching speed. JFET is free from the gate oxide interface problems unlike the MOSFET [10]. JFET is a normally-on device and conducts even though there is no gate voltage applied. Thus it requires protection circuit for system power failures to prevent a short circuit. This normally-on feature demands special gate drive designs increasing the complexity of design.

The VJFET can be used in high current and voltage applications, unlike Si JFET because of the vertical structure and the intrinsic properties of SiC. A normally-on SiC VJFET rated at 1200V and 2A was tested to study the high temperature behavior of the device. The forward characteristics for different temperatures are shown in Fig. 6. The on-resistance of the VJFET increases from 0.36Ω at -50°C to 1.4Ω at 175°C as shown in Fig. 7. The values of the on-resistance are high; however, these devices have positive temperature coefficient which enables easy paralleling of devices and the on-state resistance would decrease.

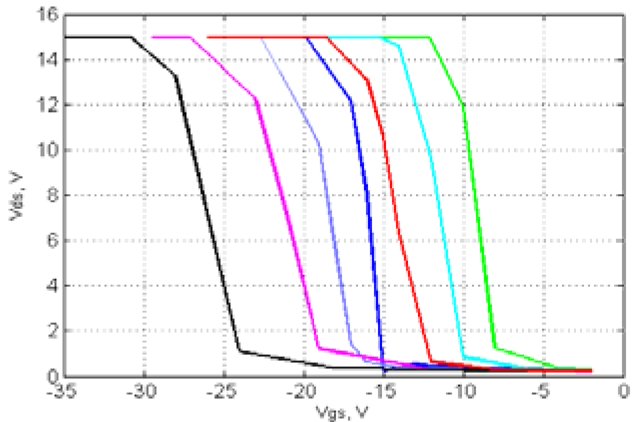



**Fig. 8.** Transfer characteristics of SiC VJFET.

The transfer characteristics of different VJFET samples are shown in Fig. 8. The negative gate pinch-off voltage required to turn-off the device does not vary much with an increase in drain to source voltage $V_{ds}$. This pinch-off voltage determines the voltage requirement of the gate drive circuit.

*B. SiC MOSFET*

MOSFET is an unipolar device which is normally off. Unlike the Si MOSFET, SiC MOSFET can block voltages up to 3kV due to the high electric breakdown field strength of SiC and has low on-state resistance. A 1.2kV, 15A SiC MOSFET was tested using the Tektronix 371B curve tracer to obtain the characteristic curves. The on-state characteristics at room temperature are shown in Fig. 9.

The gate voltage changes from 0 to 20V and a 10V drain to source voltage drop corresponds to 15A drain current for $V_{gs}$=20V. It would be reasonable to operate the device at 5A with a voltage drop of 1.5V for a gate bias voltage of 20V. The on-state curves for a temperature range of -50°C to 175°C is shown in Fig. 10. The on-state resistance calculated from the inverse slopes of the different curves is plotted as shown in Fig. 11. It is interesting to note that the resistance decreases at lower temperatures and then increases with increase in temperature

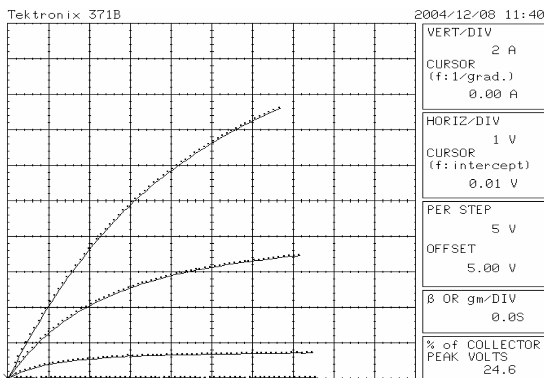



**Fig. 9.** Forward characteristics of SiC MOSFET at room temperature.

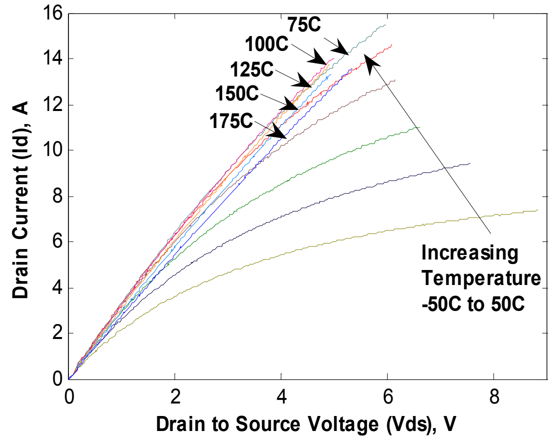



**Fig. 10.** Forward characteristics of SiC MOSFET at different temperatures

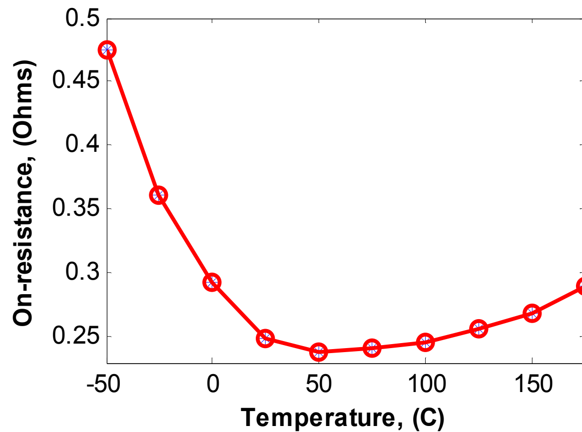



**Fig. 11.** On resistance of SiC MOSFET at different temperatures

The on-state resistance of a MOSFET can be expressed as sum of several different resistances due to different regions of the MOSFET structure. $R_{on}$ = contact resistance ($R_{cont}$)+substrate resistance($R_{sub}$)+ channel resistance ($R_{ch}$)+Accumulation layer resistance ($R_{acc}$) +resistance of JFET like region ($R_{jfet}$)+ resistance of drift region ($R_d$) [11].

The channel resistance depends on the mobility and applied gate voltage. At lower temperatures the contribution of the channel resistance to the total on-state resistance is dominant [12]. The channel resistance decreases with increase in temperature. This is due to the increase in channel mobility with increase temperature for SiC MOSFETs as reported in [12, 13].The increase in mobility is due to the interface traps closer to the conduction bandgap. This is contradictory to the unipolar device physics of operation. Also the gate threshold voltage decreases with increase in temperature. The variation in gate threshold voltage is measured from the transfer

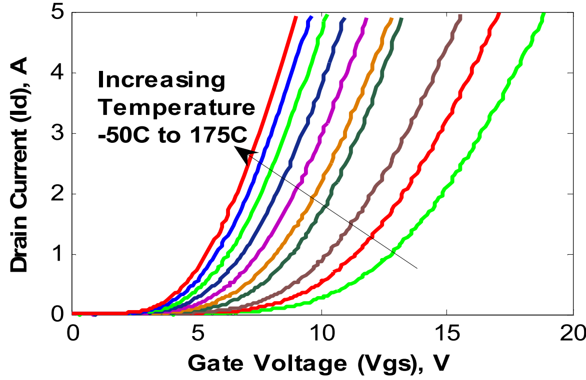



**Fig. 12.** Transfer charactersitcs of SiC MOSFET at different temperatures.

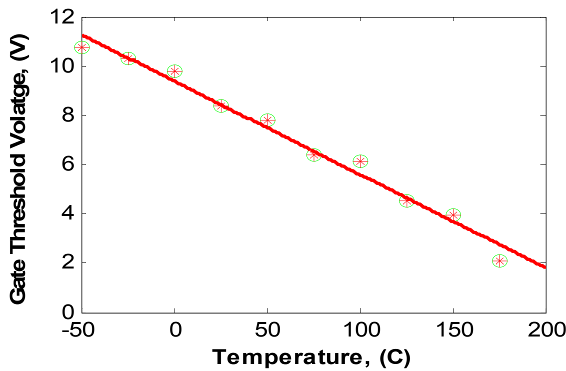



**Fig. 13.** Gate threshold voltage of SiC MOSFET at different temperatures.

characteristics as shown in Fig. 12. Fig. 13 shows the change in voltage from 10.74V at -50$^o$C to 2.82Vat 175$^o$C. This change is due to the trapped charge in the $SiO_2$ as well as the impurities at the interface of $SiO_2$. These trapped charges become active at high temperatures which result in a Fermi level shift towards the bandgap and causing the drain current to flow at low threshold voltages. However, at high temperatures the series resistance increases and the channel resistance decreases. As the series resistance has a larger effect on the overall resistance, the net resistance increases. In summary, the on-resistance at lower temperatures is dependent on gate voltage due to the dominance of channel resistance and the effect decreases at higher temperature.

## III. Gate Drive Requirements

SiC FET switches can be operated at higher switching frequencies and higher temperatures; therefore, they have different gate drive requirements than traditional Si power switches. The switching performance of the FET devices is determined by charging and discharging of the parasitic capacitances across the three terminals, input capacitance $C_{iss}=C_{gs}+C_{ds}$, $C_{rss}=C_{gd}$ reverse transfer capacitance, $C_{oss}=C_{ds} + C_{gd}$ output capacitance. These capacitances are proportional to the area of the device [5]. Since SiC devices have smaller area, even for high blocking voltages, the capacitances are reduced. This enables devices to operate at higher switching speeds. A comparison of capacitance values for SiC MOSFET and Si power switches is reported in [14].

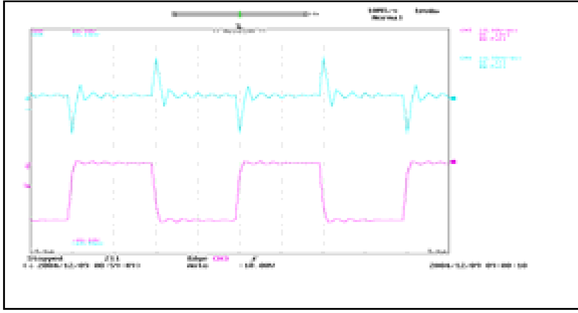
One of the important parameters in gate drive design is that the stray capacitance between the gate and the other terminals. Total input capacitance of VJFET, $C_{iss}$, determines the current required by the gate and the rate at which the applied gate voltage is built across the gate and source terminals. Therefore, the gate drive circuit is required to have the capability of providing peak currents to be able to charge the input capacitance quickly. The peak gate current is limited by series resistor between the gate and the gate driver output. The gate series resistance decreases the ringing effect due to the internal impedance of the device. However, increasing the gate resistance value results in slower turn-on times.

As mentioned earlier, there are several gate drive circuits designed for SiC VJFETs using discrete devices [6], [7]. The main objective of the project was to build a gate driver using commercially available gate driver chips in order to achieve reliable operation for faster switching speeds. In the circuit design presented in this paper, a commercial gate drive IC chip IXDD414 is used. These gate drives can also be applied to SiC MOSFETs by redesigning the passive components and modifying the output voltage polarity. The gate drive was tested with several capacitors as load before testing the driver circuit with the device. The peak gate currents and gate voltage waveforms with MOSFETs and VJFETs are shown in Fig. 14.

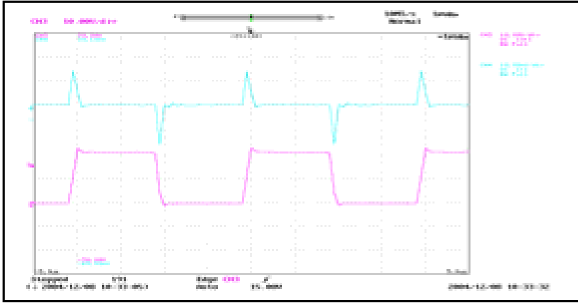
## IV. Dynamic Characteristics

The gate drive circuit discussed in the previous section was used to determine the dynamic characteristics of the MOSFET and VJFET. The gate drive voltage was designed to be 20V determined from the forward characteristics to obtain the optimum performance. A 250 kHz operation was achieved with a resistance of 7.2 Ω and with a peak gate current of 0.6A. The gate and switching waveforms are shown in Fig. 15. The device has a turn-off delay $t_{d,off}$ of 40ns, fall time $t_f$ of 100ns, turn-on delay $t_{d,on}$ of 20ns, and $t_r$ rise time of 100ns.

Since SiC VJFETs are normally-on devices they can be turned off by applying a negative voltage that is higher than what a typical Si switch requires. The gate drive needs protection circuitry to prevent the short circuit failure. One solution to this problem is to ensure that the gate drive circuit is turned on before system power up. When these are operated at high frequencies, they also need high peak gate currents. Based on the transfer characteristics, the gate drive was designed for a voltage of -25V since the pinch-off voltage for most of the samples tested was -20V. The gate series resistance was changed to achieve high frequency operation. A 250 kHz operation was achieved with a resistance of 7.2 ohms and with a peak gate current of 0.4A. The gate voltage and the switching waveforms of the VJFET are shown in Fig. 16. The device has a turn-off delay $t_{d,off}$ of 40ns, fall time $t_f$ of 80ns, turn-on delay $t_{d,on}$ of 20ns, and $t_r$ rise time of 100ns These times indicate that both the devices can be operated in

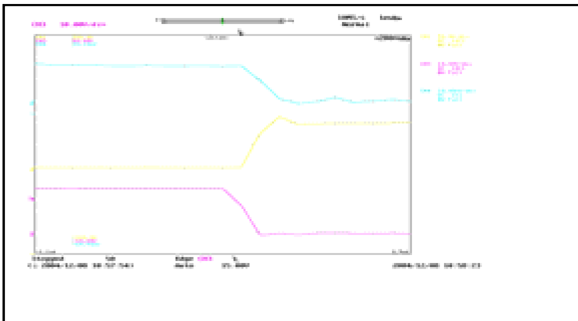


(a)

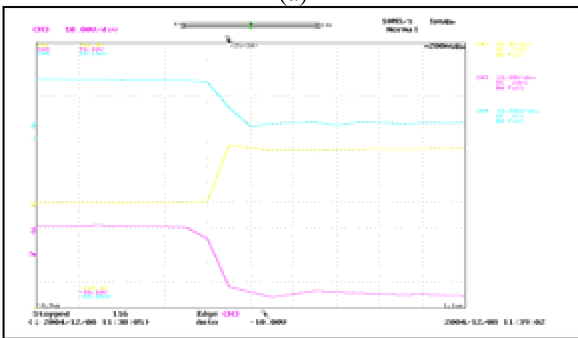


(b)

**Fig. 14.** The peak gate currents and gate voltage waveforms with (a) VJFETs, (b) MOSFETs.



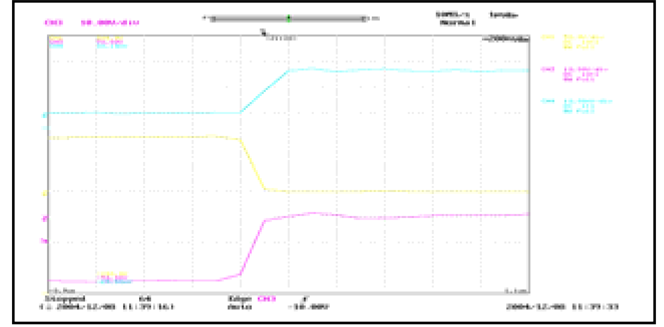
(a)



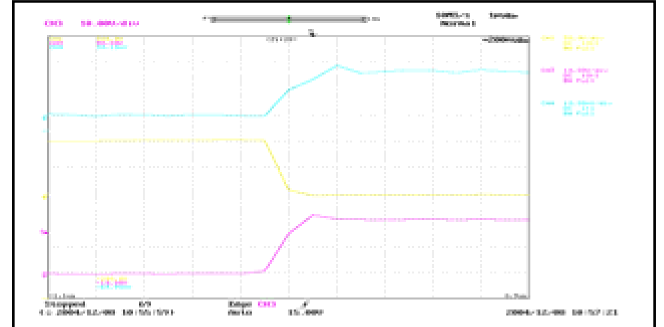
(b)

**Fig. 15.** The gate and switching waveforms of MOSFET.

MHz frequency range. The faster switching speeds of these devices is because of the high bulk mobility of the 4H-SiC The turn on and turn off energy losses for both MOSFET and JFET were calculated by integrating the instantaneous power over the turn on ($t_{on}$) and turn off times ($t_{off}$).



(a)



(b)

**Fig. 16.** The gate and switching waveforms of VJFET.

The energy losses calculated, for MOSFET and JEFT, at different temperatures for a 5kHz, 50% duty cycle, 100V, 1A operation is shown in Fig. 17. The total losses do not change much for a wide temperature range which show that the SiC devices are more reliable at higher temperatures.

## IV. Conclusion

The static and dynamic performances of some SiC Schottky diodes, SiC MOSFET and SiC VJFET characterized for a wide temperature range have been presented in this paper. The on-resistance was found to be increasing with temperature for the Schottky diodes and VJFET. However, the on-resistance for MOSFET was decreasing at lower temperatures and started to increase at higher temperatures. This is due to the interface trap defects in the SiC MOSFET. These defects will be addressed with improvements in manufacturing technology. All the Schottky diodes showed excellent reverse recovery characteristics compared to Si pn diode.

Thus, replacing Si devices with the appropriate SiC Schottky diode will improve the performance of the power switches in the converter by reducing the switching stress on the switches. In this paper, as opposed to the others in the literature, a commercial gate driver chip was used in the design and the same circuit was used to switch the MOSFET and VJFETs with some modifications.

It was shown that the switching losses were almost constant for a wide temperature range for all the unipolar devices reported in this paper. It was also shown that the power devices have very low switching times. The SiC devices presented in this paper have high blocking voltages up to 1.2kV.

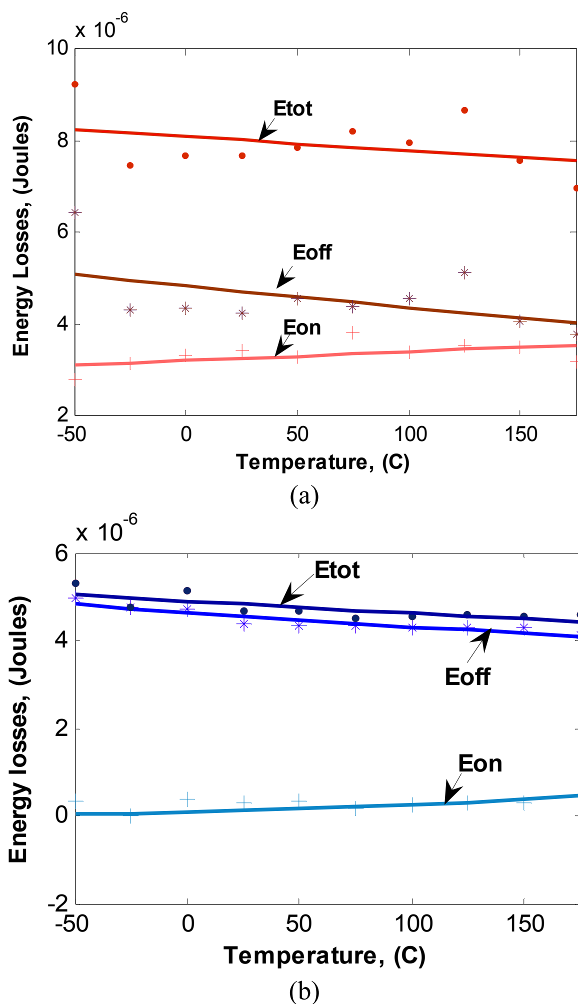



**Fig. 17**. Energy loss plots for (a) MOSFET, (b) VJFET.

Also, hard switching circuits at higher power levels and higher frequencies can be realized using SiC devices due to the excellent switching characteristics. With further improvements in current ratings the SiC unipolar devices can replace the IGBTs which have higher ratings but suffer from switching losses. MOSFETs would be the choice of device compared to VJFETs because of the normally off feature. However, the gate oxide reliability still remains an issue for MOSFETs. Even though the SiC devices can operate at high temperatures and high frequencies the system components and packaging techniques have to be developed to take advantage of these properties. The gate drive units also need to be designed for high temperature operation so that stray inductance due to the distance between the drive and device can be reduced. So further research is required for higher temperature operation of these gate drivers. The devices presented in this paper will eventually be used to develop more realistic system level models to show the system level benefits of SiC devices.

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# Enhancing Power Electronic Devices with Wide Bandgap Semiconductors

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Workshop on Frontiers in Electronics

Palm Beach, Aruba

December 21, 2004

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## Why Consider Alternatives to Si?

Today ⇒ Most power semiconductor switches are all-Si

- Limited breakdown voltages and limited power ratings
- Limited operation temperature (<150°C)
- Limited switching frequency (≤ 20 kHz) for power levels of more than a few tens of kW

∴ Present Si technology is approaching the material's theoretical limits, and it cannot meet all the requirements of the transportation, aerospace, or utility industries.

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# Why Consider SiC?

- **SiC semiconductor based device properties are superior to present Si devices**
  - **Can operate at high temperatures (up to 350°C)**
  - **Have low thermal resistivity**
  - **Higher breakdown (blocking) voltages**
  - **Excellent reverse recovery characteristics (low switching losses)**
  - **Can operate at high switching frequencies**
- **Challenges in applications of SiC**
  - **Material more expensive than Si**
  - **Low yield because manufacturing processes not mature**
  - **New circuits, passive components, gate drivers needed to take advantage of SiC properties**

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# SiC Devices – Testing and Modeling

**A list of SiC devices tested and models:**

**- Schottky diodes**

**S1 (1200 V, 7.5 A)**

**S2 (600 V, 4 A)**

**S3 (600 V, 10 A)**

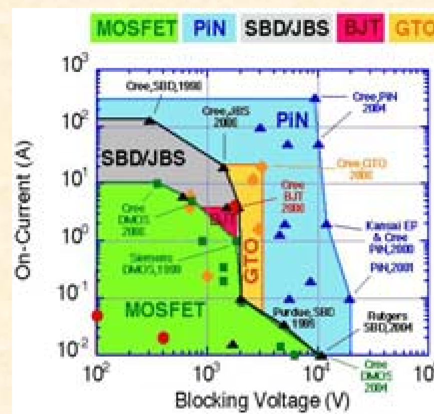
**S4 (300 V, 10 A)**

**- VJFET (1200 V, 2 A)**

**- MOSFET (1200 V, 15 A)**

**- GTO Thyristor loss model**

**- pn diode loss model**




*Purdue University

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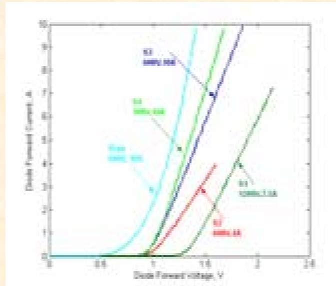
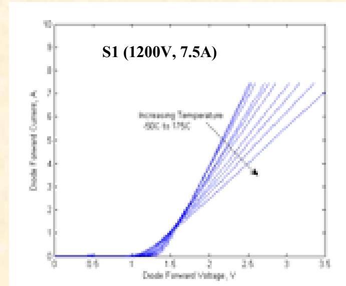
# Testing SiC Diodes

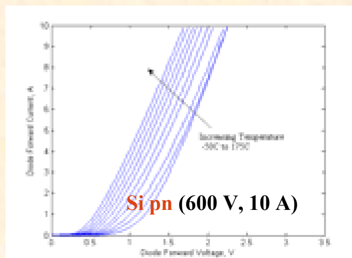
**Forward characteristics of Schottky diodes**

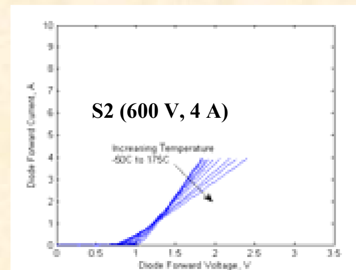




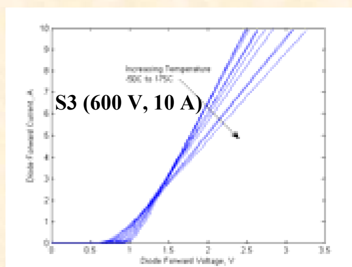

- **Majority carrier devices**
- **Attractive for high frequency applications**
- **Have positive temperature coefficient**
- **Have higher leakage currents**

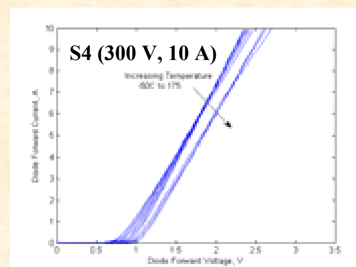
# Testing Si and SiC Diodes




**Forward characteristics of various diodes**

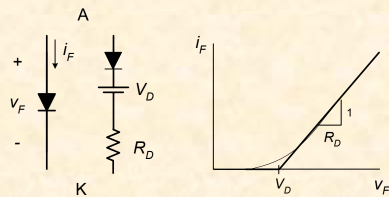


## Modeling SiC Diodes - Forward Characteristics

PWL diode model can be represented as:

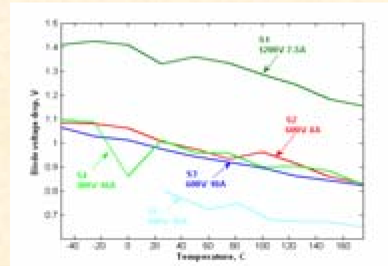
$$V_f = V_d + I_f \cdot R_d$$

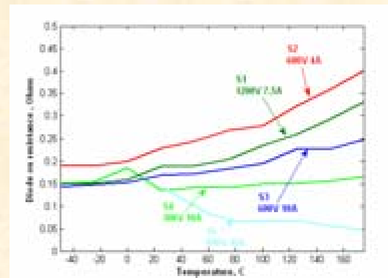



**(a)** Diode symbol and its PWL model

**(b)** *I–V* curve of the PWL model.

$$R_{on,sp} = \frac{4V_B^2}{\varepsilon \ (E_c)^3 \mu_n}$$





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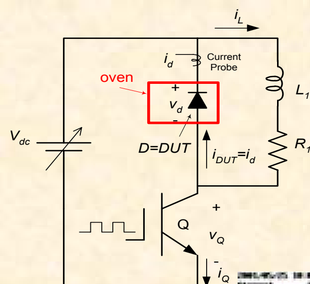
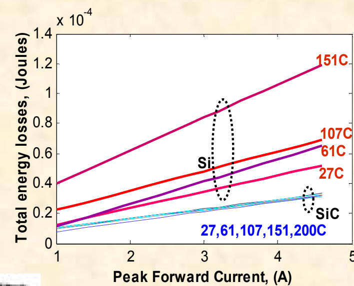
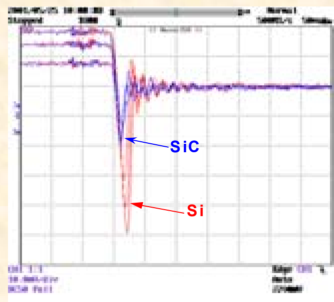
## Testing and Modeling SiC Diodes - Dynamic Characteristics




**Energy losses with respect to forward current at different operating temperatures.**




**Turn-off waveforms (2A/div)**

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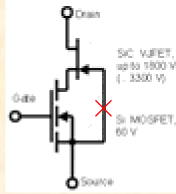
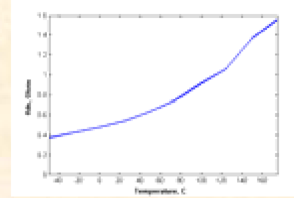
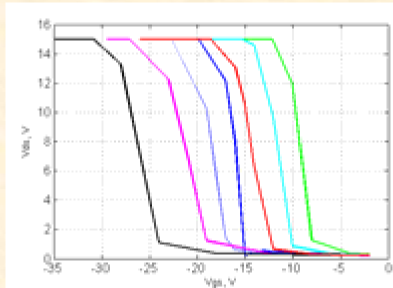
## Static Characteristics - SiC VJFET

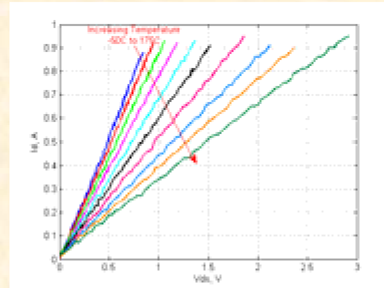




Pinch-off characteristics of SiC VJFET samples




Forward characteristics of a SiC VJFET

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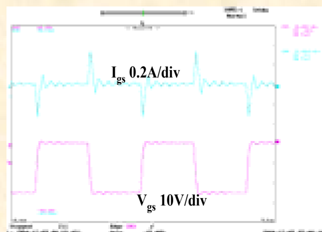
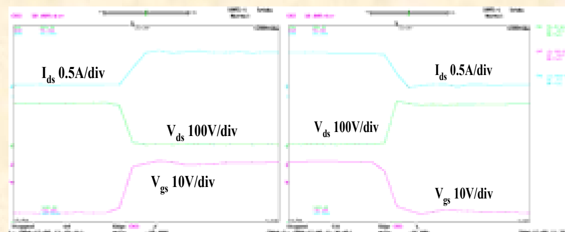
## Switching Characteristics - SiC VJFET

- **Normally on device**
- **Requires a negative gate voltage to turn off.**
- **No commercial gate drivers available.**
- **Turn-off delay $t_{d,off}$ - 40 ns, fall time $t_f$ - 80 ns turn-on delay $t_{d,on}$ - 20 ns, and $t_r$ rise time - 100 ns.**

Gate voltage and current (250 kHz)




Switching waveforms of a SiC VJFET

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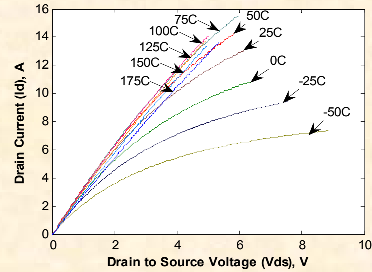
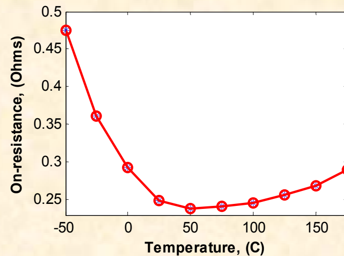
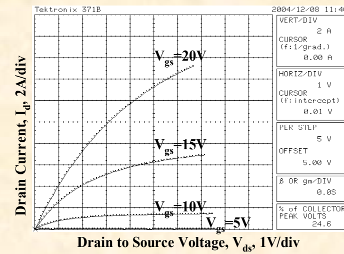
# Static Characteristics- SiC MOSFET

- 1.2 kV, 15 A SiC MOSFET.
- $V_{gs}$ = 20 V, there is a 6.7 V drain-to-source voltage drop that corresponds to 15 A drain current.
- Resistance decreases as temperature increases from -50°C to 50°C and then increases as the temperature increases beyond 50°C.




Forward characteristics of SiC MOSFET

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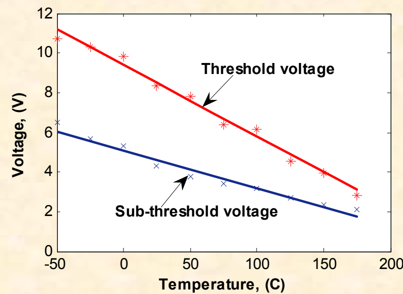
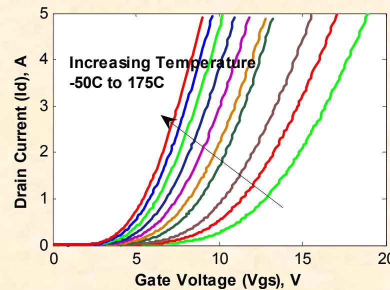
# Static Characteristics - SiC MOSFET

Transfer characteristics of SiC MOSFET




- **Channel resistance depends on the mobility and applied gate voltage.**
- **Change in threshold - due to the trapped charge in the $SiO_2$ and the impurities at the $SiO_2$ interface.**
- **However, at high temperatures the series resistance increases and the channel resistance decreases.**
- **The on-resistance at lower temperatures is dependent on the gate voltage because of the dominance of channel resistance. This effect decreases at higher temperatures.**

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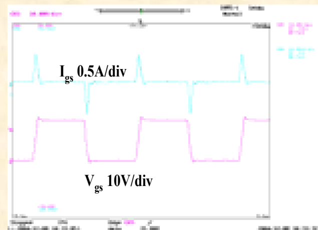
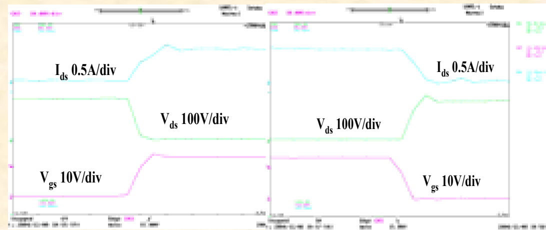
# Switching Characteristics - SiC MOSFET

- **Normally off device**
- **Requires a positive gate voltage to turn on.**
- **No commercial gate drivers available.**
- **Turn-off delay $t_{d,off}$ - 40 ns, fall time $t_f$ - 100 ns turn-on delay $t_{d,on}$ - 20 ns, and $t_r$ rise time - 100 ns.**

Gate voltage and current (250 kHz)

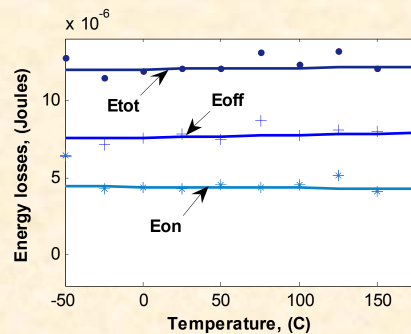



Switching waveforms of a SiC MOSFET

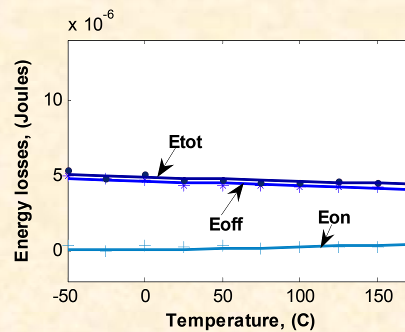


# Switching Characteristics- Energy Loss

**5 kHz, 50% duty cycle, 100 V, 0.8 A operation**

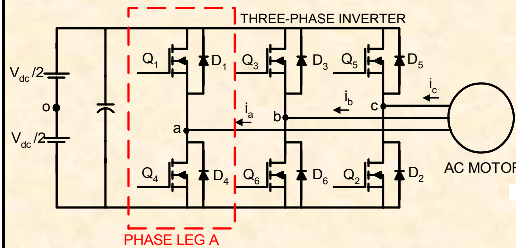


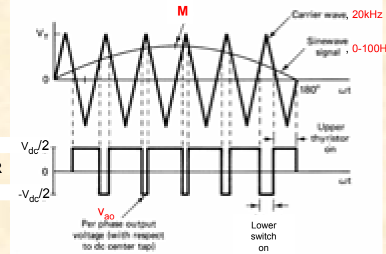

SiC MOSFET
15 A device



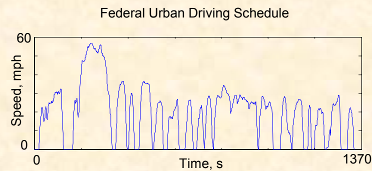

SiC VJFET
2 A device

# Electric Vehicle Traction Drive




- The electric traction drive system is modelled using an averaging technique and simulated over the FUDS cycle
- The results are analyzed for system level benefits (reduction in size and volume, increase in efficiency, etc.)

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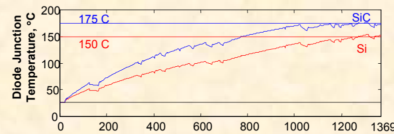
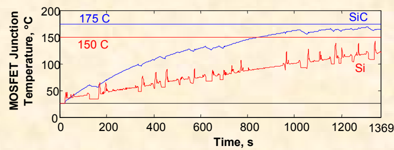
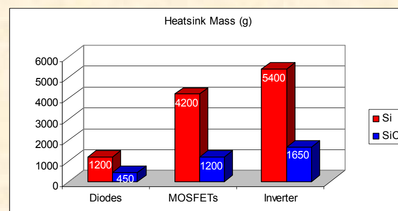
# Si vs. SiC - Heatsink Requirements




- If natural air cooled heatsinks are used, then
  - Si inverter needs a heatsink with a volume of 1998 $cm^3$ and a weight of 5.4 kg.
  - SiC inverter needs a heatsink with only a volume of 606 $cm^3$ and weight of 1.65 kg.

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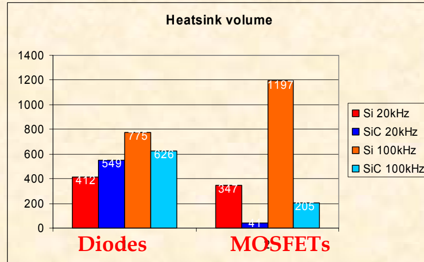
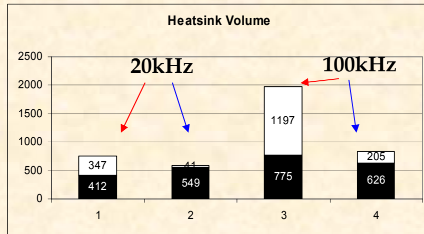
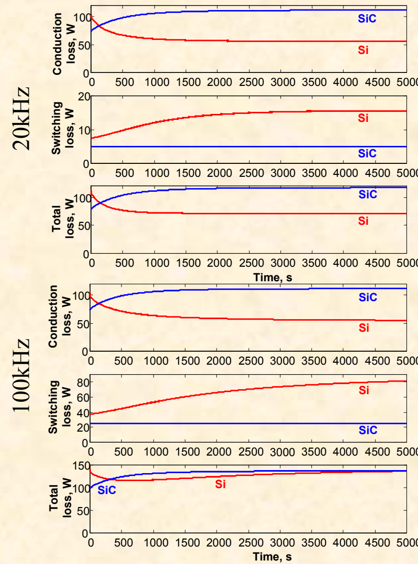
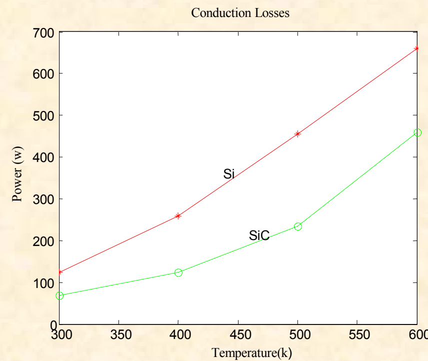
# Heatsink Requirements – 10 kW SiC dc-dc Converter




Diode losses

# GTO Loss Model

- SiC GTO thyristor losses are less because of lower $R_{on,sp.}$
- Electric breakdown field strength for SiC is higher
  ⇒ specific resistance is less

$$R_{sp} = \frac{4V_B^2}{\varepsilon_s \mu_n E_c^3}$$

- The conduction losses vary with the second term in the equation, which is a function of the on-state specific resistance.

Conduction Losses

Power (w)

Temperature(k)

Si

SiC

Conduction losses for V= 5000 V and J=100 A/cm²

$$P_{on-state} = J \cdot (E_g / q) + J \cdot (3\pi / 8) \cdot (kT / q) \cdot \exp(3V_B / 2L_a E_c)$$

# GTO Loss Model

Switching losses

$$E_{off} = 1/2 \cdot (\varepsilon_s \cdot E_c V/(1-\alpha_{npn})\sqrt{V/V_B} + J\alpha_{npn,\ max} \cdot \tau_a$$

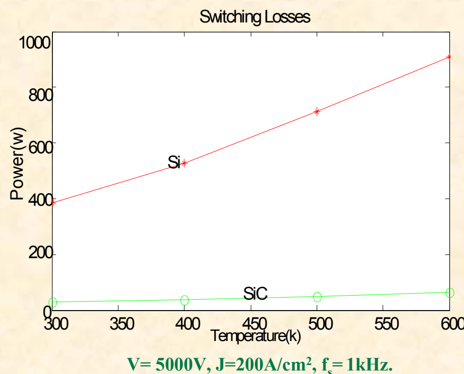
$$E_{on} = 1/3 \cdot \varepsilon_s \cdot E_c V\sqrt{V/V_B} + J^2 \cdot (3\tau_a \cdot V_B^2)/(\varepsilon_s \cdot \mu_n \cdot E_c^3) + (E_g/2q) \cdot J\tau_a$$

The switching power losses can be calculated using the total energy loss equation as,

$$P_{switching} = (E_{on} + E_{off}) \cdot f_s$$

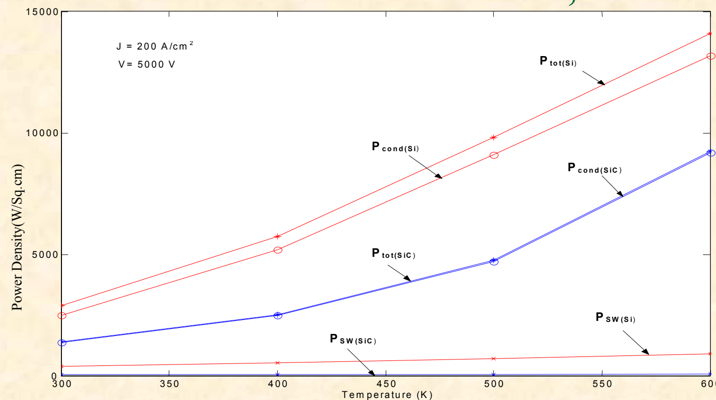
SiC GTO has lower switching losses

- Reduced drift width
  ⇒ less stored charge
  ⇒ faster switching
- Smaller ambipolar diffusion length
  ⇒ smaller lifetimes & low mobilities of electrons and holes




V= 5000V, J=200A/cm², $f_s$= 1kHz.

# GTO Simulation for J = 200 A/cm², V = 5000V




| T (K) | $P_{cond}$(W) | $P_{cond}$(W) | $P_{sw}$(W) | $P_{sw}$(W) | $P_{total}$(W) | $P_{total}$(W) |
|---|---|---|---|---|---|---|
| | Si | SiC | Si | SiC | Si | SiC |
| 300 | 2492 | 1376 | 3835 | 30 | 2875 | 2786 |
| 400 | 5195 | 2476.5 | 528 | 38 | 5722 | 2954 |
| 500 | 9094 | 4704 | 714 | 48 | 9807 | 3476 |
| 600 | 13810 | 9184 | 910 | 63 | 14090 | 4789 |

# Loss Model Equations – pn diode

Static losses

$$P_{static} = (J_f \cdot V_f + J_f^{\,2} \cdot R_{on}) \cdot d + J_r \cdot V_r (1 - d)$$

Where,

$$R_{on} = \frac{(V_b / E_c)}{q \cdot \mu_n \cdot N_D + \frac{(\mu_n + \mu_p) J_f \cdot \tau_a}{(V_b / E_c)}}$$

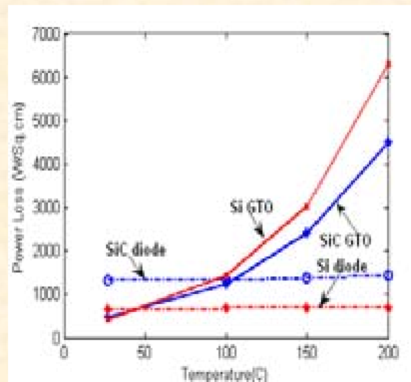
Switching losses

$$P_{sw} = J_f \cdot \tau_a \cdot V_r \cdot f_s$$

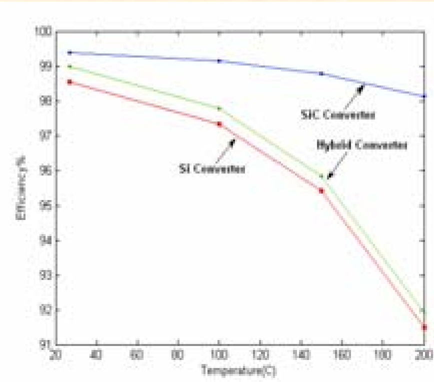
# Converter Efficiency Plots for Utility Application

SiC devices 20 kV, 200 A/cm²

Si devices 5 kV, 200 A/cm²




Average loss profiles for SiC and Si devices




Efficiency plot for different converters

## System Cost Savings – 100 kV, 100 MW HVDC Interface

Si Converter - 5 kV, 200 A/cm² devices

SiC Converter - 20 kV, 200 A/cm² devices

Hybrid Converter - 5 kV, 200 A/cm² Si GTO ;20 kV, 200 A/cm² SiC diode

No. of devices

Si - 1560

Hybrid - 936

SiC - 396

| Converter | Average Loss Difference | kW-hr/year | Cost Savings |
|---|---|---|---|
| Si/SiC | 1091 kW | 9,553,537 kW-hr | $ 382,141 |
| Si/Hybrid | 275 kW | 2,486,215 kW-hr | $ 96,249 |

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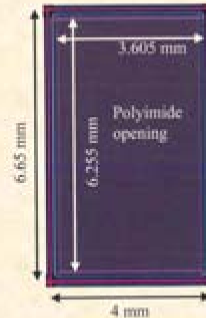
## 55kW Si-SiC Hybrid Inverter

- CREE has developed 75A, 1200 V, 4mm × 6.65mm SiC Schottky diodes
- Semikron will replace each Si pn diode (9mm × 9mm) in their AIPM with two 75A SiC Schottky diodes
- ORNL will test, characterize, and model the 55kW inverter.

# yield 67
% 45.9
Vf@75A= 1.42 V

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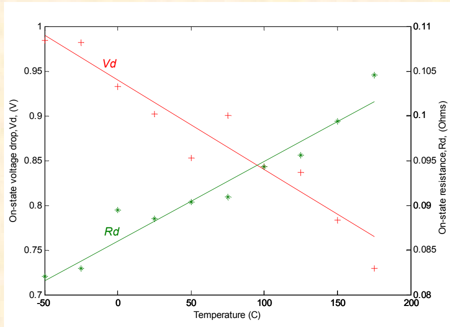
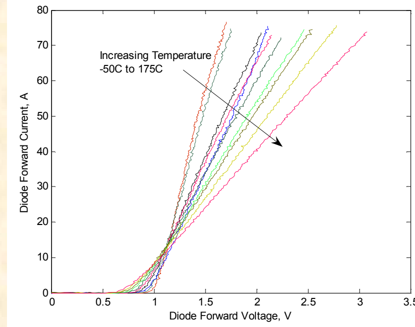
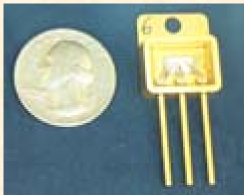
## 75 A SiC Schottky Diodes




$R_D$ and $V_D$ obtained from the experimental data



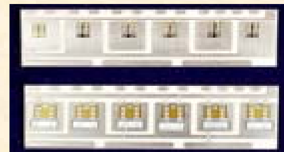

Experimental I-V curves of the 75A SiC Schottky diode





## 7.5 kW All-SiC Inverter

- Rockwell Scientific will build a 7.5 kW all-SiC power module using MOS enhanced JFETs and Schottky diodes.
- ORNL will
  - supply the controls to complete the inverter
  - test, characterize, and model it



Rockwell Scientific

## Future Work

- Acquire and test prototype SiC power electronics devices
- Develop and refine device, circuit, and system models
- Demonstrate SiC-based power electronic converters for transportation and utility applications
- Design and demonstrate new high frequency gate drivers
- Develop high temperature packaging techniques
- Develop novel circuit topologies to take advantage of SiC properties

## Conclusions

- The performances of some SiC Schottky diodes, a SiC JFET, and a SiC MOSFET have been characterized for a wide temperature range.
- Since the losses of SiC devices are less:
  - the efficiency for SiC converter is higher.
  - thermal management requirements can be reduced.
  - device operating area (DOA) limits can be increased.
- SiC Schottky diode has had the first impact on power electronics rather than SiC switches.
- Power converters using SiC power devices are expected to meet the application requirements. (Yield and cost issues will eventually be solved.)

# Final Report

**Of**

***Power Losses for Si- and SiC-Based***
***Back-to-back Inverter in Wind Generation Application***

**Submitted to**

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**Submitted date:** **June 2005**

# I. System Structure

This wind generation system is composed of wind turbine, PM generator, back-to-back inverter, DC link, and utility filter, as shown as Fig. 1. The electricity generated is delivered to the utility grid. Our purpose is to study the power losses in back-to-back inverter including the filter loss and make comparison between SiC and Si devices.

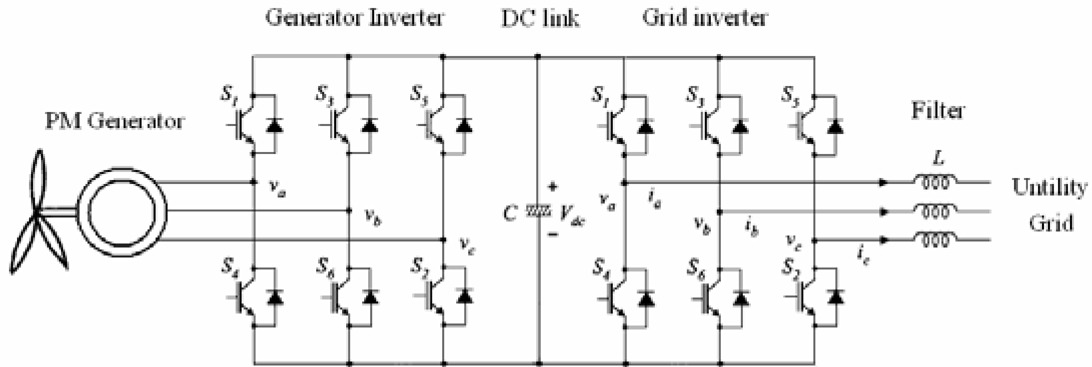



Fig. 1. System Structure

# II. Estimation of Generator Performance

The following assumptions have been made in this study:

a) Generator back emf in phase with generator current

b) The following parameters are known:

Rated speed $n_0$ (rpm)

Back emf at rated speed (line-neutral, peak) $Emf_0$ (V)

Relationship between input power $P_{in}$ (kW) and speed $n_g$ (rpm)

Pole number $p$

Stator phase resistance $R$ ($\Omega$)

Stator phase inductance $L$ (H)

Eddy loss at rated speed $P_{l_{e0}}$ (kW)

Hysteresis loss at rated speed $P_{l_{h0}}$ (kW)

The following equations relate to calculating values for the generator driven by the wind turbine:

(1) Generator frequency, $f_g$

$$f_g = \frac{p \cdot n}{120} \quad f_{g0} = \frac{p \cdot n_0}{120} \tag{1}$$

(2) Back Emf (line-neutral, peak), $Emf$

$$Emf = Emf_0 \cdot \frac{f_g}{f_{g0}} \tag{2}$$

(3) Core losses, $P_{l_c}$; eddy loss, $P_{l_e}$; and hysteresis loss, $P_{l_h}$

$$P_{l_c} = P_{l_e} + P_{l_h} \quad P_{l_e} = P_{l_{e0}} \cdot \frac{f_e}{f_{e0}} \quad P_{l_h} = P_{l_{h0}} \cdot \frac{f_e}{f_{e0}} \tag{3}$$

(4) Phase current on $q$-axis (peak), $I_{sq}$

$$I_{sq} = \frac{1000 \cdot P_{in} \cdot 2}{3 \cdot Emf} \tag{4}$$

(5) Output voltage without considering the core losses, $E_c$

$$E_c = \sqrt{(Emf - I_{sq}R)^2 + (I_{sq}X)^2} \quad X = \omega L \quad \omega = 2\pi f_e \tag{5}$$

(6) Effective current due to core losses (peak), $I_c$, $I_{cq}$ ($q$-axis component), $I_{cd}$ ($d$-axis component), and the same below.

$$I_c = \frac{1000 \cdot P_{l_c} \cdot 2}{3 \cdot E_c} \tag{6}$$

$$I_{cq} = I_c \cdot \cos\phi_c \qquad I_{cd} = I_c \cdot \sin\phi_c \qquad \phi_c = \arccos\left(\frac{E_c}{Emf}\right) \tag{7}$$

(7) Total phase current (peak), $I_s$

$$I_s = \sqrt{I_{stq}^2 + I_{std}^2} \quad I_{stq} = I_{sq} + I_c \cos\phi_c \quad I_{std} = I_c \sin\phi_c \tag{8}$$

(8) Output voltage (peak), $U_{gout}$

$$U_{gout} = \sqrt{U_{sq}^2 + U_{sd}^2} \quad U_{sq} = Emf - I_{std}X - I_{stq}R \quad U_{sd} = I_{stq}X - I_{std}R \tag{9}$$

(9) Power factor, $DPF$

$$DPF = cos(\alpha_I - \alpha_U) \quad \alpha_I = \arccos\left(\frac{I_{stq}}{I_{std}}\right) \quad \alpha_U = \arccos\left(\frac{U_{sq}}{U_{sd}}\right) \tag{10}$$

(10) Copper loss, $P_{l_{cu}}$

$$P_{l_{cu}} = \frac{3 \cdot I_s^2 \cdot R}{2 \cdot 1000} \tag{11}$$

(11) Generator Efficiency, $\eta_g$

$$\eta_g = \frac{P_{in} - P_{l_{cu}} - P_{l_c}}{P_{in}} \times 100\% \qquad (12)$$

## III. Computation of back-to-back inverter system losses

The following are the assumed rating requirements for a 1.5 MW wind turbine:

Input power 1568 kW

Phase current 1941 A

DC link voltage 1100 V

Switching frequency 50 kHz

Table 1 lists the power electronics devices used in the generator inverter and grid inverter. The links in the "Others" column will show the datasheets and technical papers that were used to obtain the parameters for the simulation in this report.

Table 1. Parts Information

| Item | Voltage rating | Current rating | Part number | Others |
|---|---|---|---|---|
| SiC MOSFETs | 1200 | 15×15* | | reference |
| SiC Schottky diodes | 1200 | 7.5×30 | Sch1200_7P5 | datasheet, reference |
| Si MOSFETs | 1200 | 3×70 | IXTP3N120 | datasheet |
| Si ultrafast recovery diode | 1200 | 75×3 | SML75SUZ12L | datasheet |

* The number of parts need to be paralleled in one inverter

In order to achieve the high power rating required, we made the following assumptions:

a) 10 (~150 kW each) back-to-back inverters paralleled

power rating per inverter: 1200V, 210A

b) The inverters are MOSFET-based. Detailed information is listed in Table 1.

c) Each MOSFET has a separate gate drive.

### 1. On-state Resistance Model

Table 2 lists the intrinsic parameters of silicon (Si) and silicon carbide (SiC) used in the simulation model of the MOSFETs and diodes.

Table 2. Comparison of electrical and material properties

| Property | Si | 4H-SiC | 6H-SiC | 3C-SiC |
|---|---|---|---|---|
| Bandgap $E_g$ (eV) | 1.11 | 3.26 | 2.86 | 2.2 |
| Breakdown electric field, $E_c$ (kV/cm) | 300 | 2200 | 2500 | 1200 |
| Relative dielectric constant, $\varepsilon_r$ | 11.8 | 10.1 | 9.7 | 9.66 |
| Electron mobility, $\mu_n$ (cm$^2$/V · s) | 1350 | 950 | 500<br>80 | 900 |
| Saturated Electron Drift Velocity, $v_{sat}$ (cm/s) | $1\times10^7$ | $2\times10^7$ | $2\times10^7$ | $2.5\times10^7$ |
| Thermal conductivity $G_{th}$ (W/cmK) | 1.5 | 4.9 | 4.9 | 4.9 |

The on-state specific resistance of majority carrier devices can be represented as

$$R_{on,sp} = \frac{4V_B^2}{\varepsilon E_c^3 \mu_n} \tag{13}$$

where $V_B$ is the breakdown voltage which is determined by design requirements. $\varepsilon$, $E_c$, and $\mu_n$ are dependent on material (refer to Table 2). $\mu_n$ is also influenced by doping density, applied electrical field, and saturation velocity. Equation (14) takes into account all these factors. Refer to Appendix III for an explanation of each of the symbols.

$$\mu_n{}^E(E) = \frac{\mu_0}{\left\{1+\left|\frac{\mu_0 E}{v_s}\right|^{\beta}\right\}^{1/\beta}}, \text{ where } \mu_0 = \mu_{\min} + \frac{\mu_{\max}-\mu_{\min}}{1+\left(N/N_{ref}\right)^{\alpha}} \tag{14}$$

In this equation, $\mu_{max}$, $\mu_{min}$, $N_{ref}$, and $v_s$ are temperature-dependent, as shown in equations (15) - (18).

$$\mu_{\max} = A_{\mu_{\max}} \times \left(\frac{T}{300}\right)^{-B_{\mu_{\max}}} \tag{15}$$

$$\mu_{\min} = A_{\mu_{\min}} \times \left(\frac{T}{300}\right)^{-B_{\mu_{\min}}} \tag{16}$$

$$N_{ref} = A_{N_{ref}} \times \left(\frac{T}{300}\right) \tag{17}$$

$$v_s(T) = \frac{v_{\max,600K}}{1+0.8\cdot\exp\left(\frac{T}{600}\right)} \tag{18}$$

## 2. System Power Losses Model

Based on the resistance model, an averaging technique was employed to set up a power losses model. This technique averages all variables in a switching cycle and uses this average as a sampling point for a new model.

The total power loss of this system is equal to the sum of the power losses of each MOSFET and Schottky (SiC) or ultrafast (Si) diode. Both the power losses of the MOSFET and diode are composed of conduction loss ($P_{cond,J}$, $P_{cond,D}$) and switching loss ($P_{sw,J}$, $P_{sw,D}$). The only difference is that the conduction loss of the MOSFET has an additional component ($P_{cond,D\to J}$) that is due to a diode's reverse recovery current. Applying the averaging technique, we can obtain the expression of conduction losses as follows (again see Appendix III for an explanation of all symbols):

$$P_{cond,M} = I^2 \cdot R_{DS,on}(\frac{1}{8}+\frac{1}{3\pi}M\cos\phi) \tag{19}$$

$$P_{cond,D\to M} = (\frac{dI_R}{dt})^2 \cdot \frac{f_c t_{rr}^{\ 3}}{3(S+1)^2} \cdot R_{DS,on} \tag{20}$$

$$P_{cond,D} = I^2 \cdot R_D\left(\frac{1}{8}-\frac{1}{3\pi}M\cos\phi\right) + I \cdot V_D \cdot \left(\frac{1}{2\pi}-\frac{M\cos\phi}{8}\right) \tag{21}$$

$$P_{sw,M} = \frac{Hf_c}{2\pi}\left\{\frac{G_1}{\sqrt{G_1^{\ 2}-J'^2}}\left[\pi+2\tan^{-1}\left(\frac{J'^2}{\sqrt{G_1^{\ 2}-J'^2}}\right)\right]+\frac{G_2}{\sqrt{G_2^{\ 2}-J'^2}}\left[-\pi+2\tan^{-1}\left(\frac{J'^2}{\sqrt{G_1^{\ 2}-J'^2}}\right)\right]\right\},$$

where $J' = \frac{I}{A}$, $H = \frac{1}{3}\varepsilon E_c V(\frac{V}{BV})^{1/2}$, $G_1 = g_m(V_{GH}-V_{th})$ , and $G_2 = g_m(V_{th}-V_{GL})$. (22)

$$P_{sw,D} = f_c \cdot \frac{V_R}{2S}\left(\frac{dI_R}{dt}\right)\left(\frac{St_{rr}}{S+1}\right)^2 \tag{23}$$

Note, the change of $t_{rr}$ and $S$ as temperature and forward current is also taken into consideration because this change is large for Si devices.

Thus, the total power losses of each inverter is

$$P_{l_{inv}} = \left(P_M+P_D\right)\times 6 = (P_{cond,M}+P_{cond,D\to M}+P_{sw,M}+P_{cond,D}+P_{sw,D})\times 6 \tag{24}$$

## 3. Thermal Model

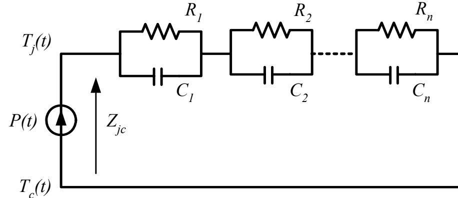


Fig. 2. Single Switch Thermal Model

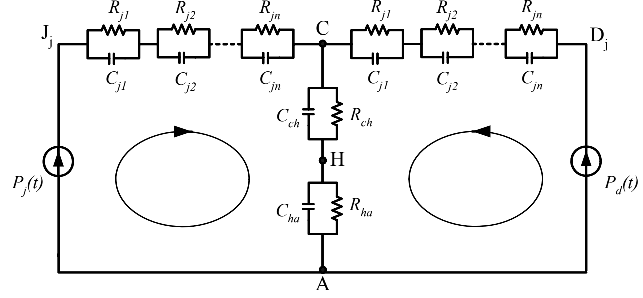


Fig. 3. Thermal Equivalent Circuit of Inverter Module

Thermal modeling is used to estimate the device performance under different temperatures. One method to set up a thermal model is using an equivalent circuit. In Fig. 2, an equivalent circuit originated from a finite difference discretization of the heat equation is shown. It can be represented by

$$Z_{jc}(s) = \frac{R_1}{1+s\tau_1} + \frac{R_2}{1+s\tau_2} + \cdots + \frac{R_3}{1+s\tau_3} \tag{25}$$

where $\tau_i = R_i C_i$ ($i$ = 1, 2, …, $n$) and the sum of $R_i$ is equal to the junction-case thermal resistance, $R_{jc}$. Fig. 3 shows the thermal model for the entire inverter system.

### 4. PWM Control Modulation Index

For the generator inverter, modulation index is computed by

$$M = \frac{U_{gout}}{V_{dc}/2}. \tag{26}$$

For the grid inverter, modulation index is equal to

$$M = \frac{2\sqrt{2}\cdot V_{ll}}{\sqrt{3}\cdot V_{dc}}, \tag{27}$$

where $V_{ll}$ is the output voltage of grid inverter (line-line rms), $V_{dc}$ is DC link voltage.

### 5. Filter Loss

Equation (27) is used to estimate the filter loss, $P_{l_f}$.

$$P_{l_f} = k \cdot I_{grid}^2, \tag{28}$$

where $k$ is the filter loss constant, $k$ = 0.0097 W/A$^2$ and $I_{grid}$ is the peak phase current of grid inverter.

$$I_{grid} = \frac{\sqrt{2} \cdot P_{in_{grid}}}{\sqrt{3} \cdot V_{grid} \cdot DPF} \quad (29)$$

**6. System Efficiency,** $\eta_{inv}$

The overall system efficiency is given by the following equation:

$$\eta_{inv} = \frac{P_{in_{gen}} - (P_{l_{gen}} + P_{l_{grid}}) \times 10 - P_{l_f}}{P_{in_{gen}}} \times 100\% \quad (30)$$

## III. Simulation & Results

Using Matlab Simulink, the system is shown in Appendix I. The heatsinks are designed so that the junction temperatures of all parts are around 150 °C at rated speed. Then, take each speed as a steady state status and find the corresponding power losses, temperatures, and efficiencies for both SiC and Si devices. These results are tabulated in a Table shown in Appendix II. Parameters used in the simulation are listed in Table 3. E1357 of Thermaflo, Inc. is selected for the heatsinks. The characteristics and the sizes of heatsinks of SiC and Si devices are shown in Table 4.

Table 3. Simulation Parameters

| Property | 4H-SiC | Si |
|---|---|---|
| Breakdown electric field, $E_c$ (kV/cm) | 2200 | 300 |
| Relative dielectric constant, $\varepsilon$ | 10.1 | 11.9 |
| Doping coefficient of $\mu$, $\alpha$ | 0.76 | 0.91 |
| Electric field coefficient of $\mu$, $\beta$ | 1 | 2 |
| Coefficient of $\mu_{\max}$, $\mu_{\max}A$ | 950 | 1350 |
| Coefficient of $\mu_{\max}$, $\mu_{\max}B$ | 2.4 | 2.5 |
| Coefficient of $\mu_{\min}$, $\mu_{\min}A$ | 40 | 92 |
| Coefficient of $\mu_{\min}$, $\mu_{\min}B$ | 0.5 | 0.91 |
| Coefficient of $N_{ref}$, $N_{ref}A$ | $2 \times 10^{17}$ | $1.3 \times 10^{17}$ |
| Maximum saturated velocity, $v_{s\max,600°C}$ (cm/s) | $4.77 \times 10^{7}$ | $2.4 \times 10^{7}$ |

The simulation results demonstrate that:

1. Conduction loss of the SiC MOSFET is 5 times less than that of the Si MOSFET

By equation (19), conduction loss of MOSFET is positively proportional to its on-state resistance. The on-state resistance of SiC is smaller than that of Si as shown in Fig. 4. This is mainly because of the high breakdown electrical field of SiC as shown in Table 2. As a result, conduction loss of the SiC MOSFET is much smaller than that of the Si MOSFET.

2. Switching loss of the SiC MOSFET is slightly larger than that of the Si MOSFET.

By equation (22), switching loss of MOSFET increases as breakdown electrical field *Ec* or current density *J* increases and decreases as transconductance $g_m$ increases. *Ec* of SiC is about 7 times that of Si. *J* of SiC is usually larger than that of Si. If the transconductance of SiC and Si MOSFETs are at the same level, the switching loss of SiC MOSFET should be higher, just as shown in this case.

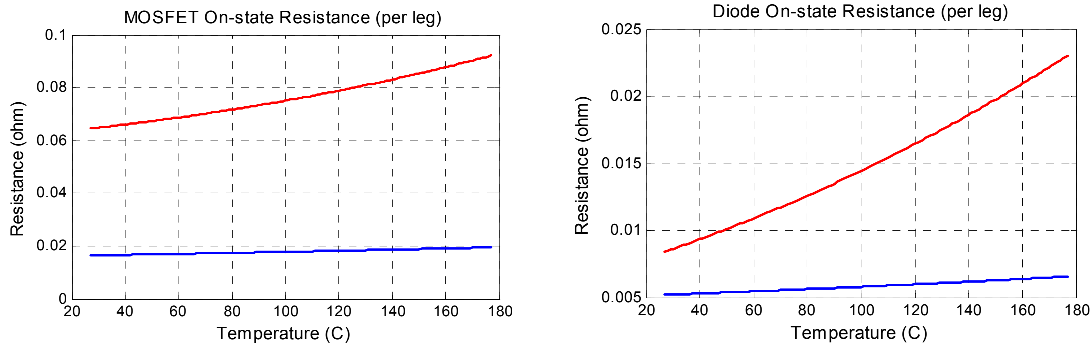



Fig. 4. Comparison of on-state resistances of SiC (solid line) and Si (dashed line) devices

3. Conduction loss of the SiC Schottky diode is smaller than that of the Si diode

The conduction loss of a diode goes up as the on-state resistance increases. The on-state resistances of the SiC and Si diodes used in this application are shown in the Fig. 4. The difference between these two are not very large. Thus, the resultant conduction loss of the Si diode is larger than that of SiC diode, but not very much.

4. Switching loss of the SiC Schottky diode is significantly smaller than that of the Si diode

Reverse recovery current is the main cause of the switching loss of the diode. The reverse recovery characteristic of a SiC Schottky diode is much better than that of its Si counterpart. It demonstrates a small peak reverse recovery current, short reverse recovery time, and small change with temperature, current changing rate, and forward current. So the simulation results show 4-6 times advantage of the SiC diode on switching loss and

this advantage becomes dramatic at large forward current and high temperature. In addition, the increase of reverse recovery current of a Si diode at high temperature and large forward current contributes much to rapid increase of the junction temperatures of Si devices around the rated power, and in turn a large volume of heatsink.

Table 4. Heatsinks for one back-to-back inverter

| Heatsink | | Weight (kg) | Volume ($cm^3$) | E1357 |
|---|---|---|---|---|
| Generator inverter | SiC | 2.3 | 1737 | Material: 6063-T6 Aluminum<br>Weight: 15.9 lbs/ft<br>Surface area: 392.6 $in^2$/in<br>Forced convection at 6.1 m/s |
| | Si | 9.1×2* | 7007×2* | |
| Grid inverter | SiC | 2.2 | 1679 | |
| | Si | 8.4×2* | 6435×2* | |
| Sum | SiC | 4.5 | 3416 | |
| | Si | 35.0 | 26883 | |

* To limit the junction temperatures of Si devices below 150°C, the parts have to be arranged on two separated heatsinks.

5. The size of heatsink of SiC devices is reduced to about 1/8 of that of Si devices.

Combining 1 - 4, the power loss of SiC devices is much smaller than that of Si devices. Moreover, the SiC material has better thermal conductivity (Table 2). Thus, it allows the heatsinks of SiC devices to be reduced significantly.

6. SiC inverters are more efficient than that of Si inverter.

For this case, the power efficiency is improved from 88.3% to 94.0% at rated generator speed as shown in Fig. 5 and Appendix II. This means 48.7% of power loss is saved in SiC inverters compared to the Si counterpart. It is equal to 89.3 kW. Moreover, the efficiency of SiC inverter over the entire operating range of the wind turbine does not change as much as that of Si with the variation of temperature and power (2.0% vs. 6.1%). This is a significant improvement.

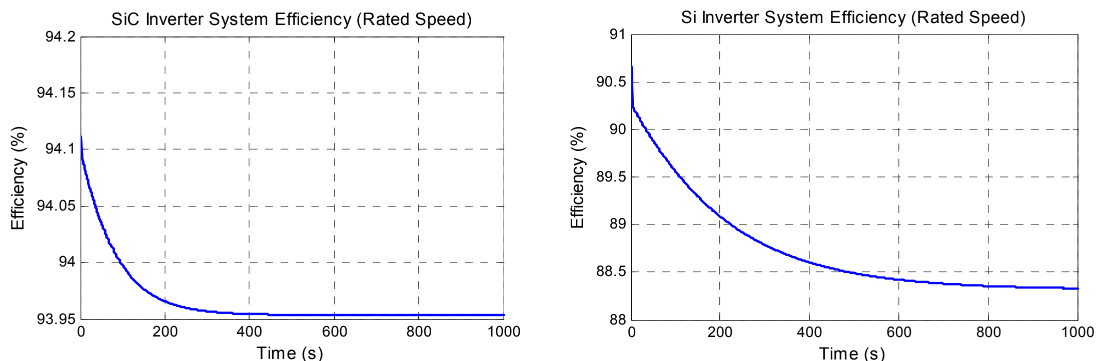


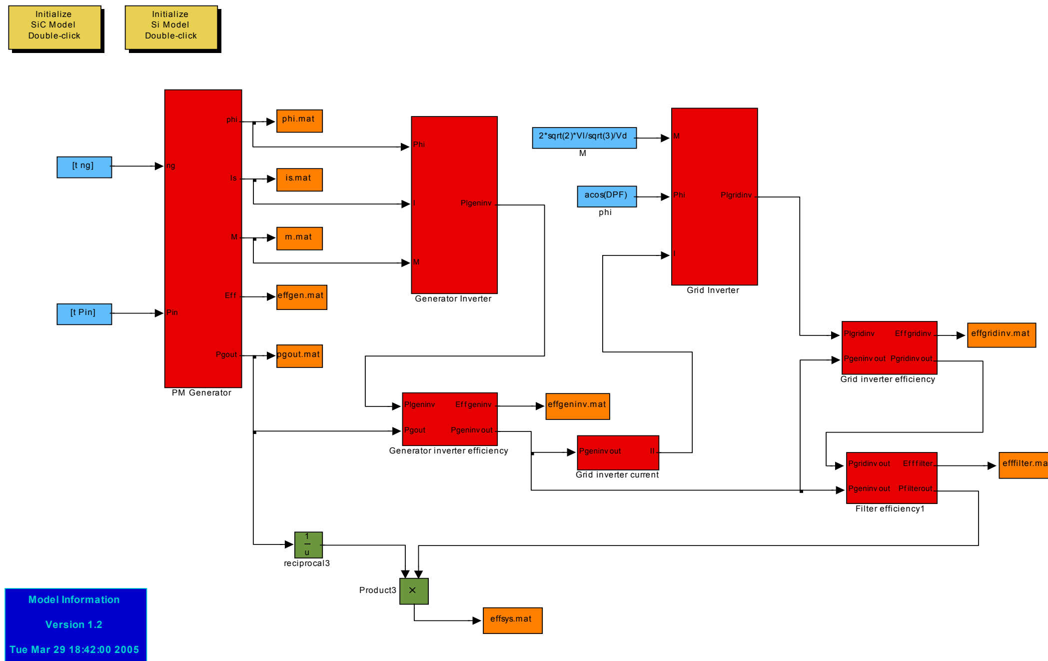

Fig. 5. Efficiency of back-to-back Inverter system at rated generator speed

7. SiC inverters are more reliable.

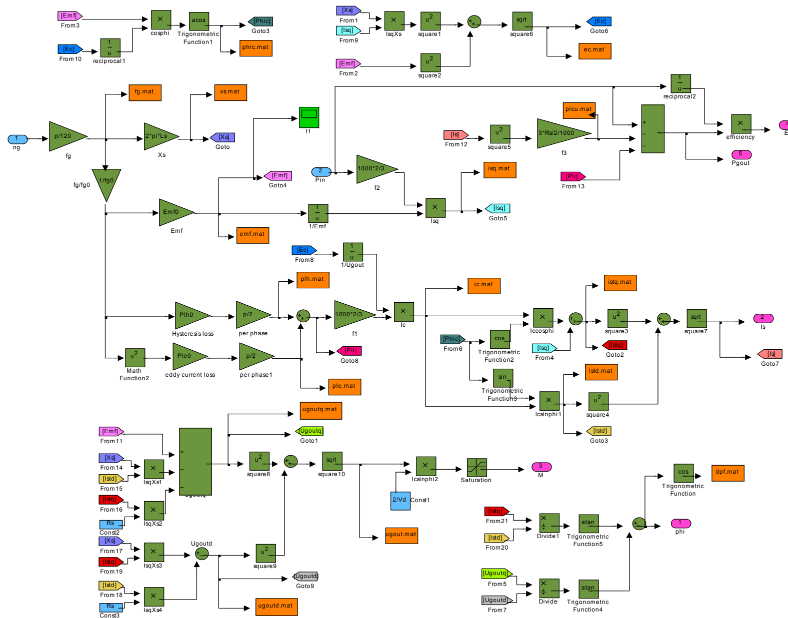
In this application, the junction temperatures of devices are confined within 150°C. It has approached the limit of Si devices. Operating Si devices above 100°C lessens the reliability of the devices significantly. On the other hand, for SiC devices this temperature is not too high as they can work well at this temperature (maximum junction temperature can be 600°C for SiC). Moreover, the switching frequency limit for Si to work reliably is 20 kHz. The switching frequency is 50 kHz in this case. It is difficult for Si devices and not a problem for SiC devices.

# Appendix I — Simulink Model Block Diagrams

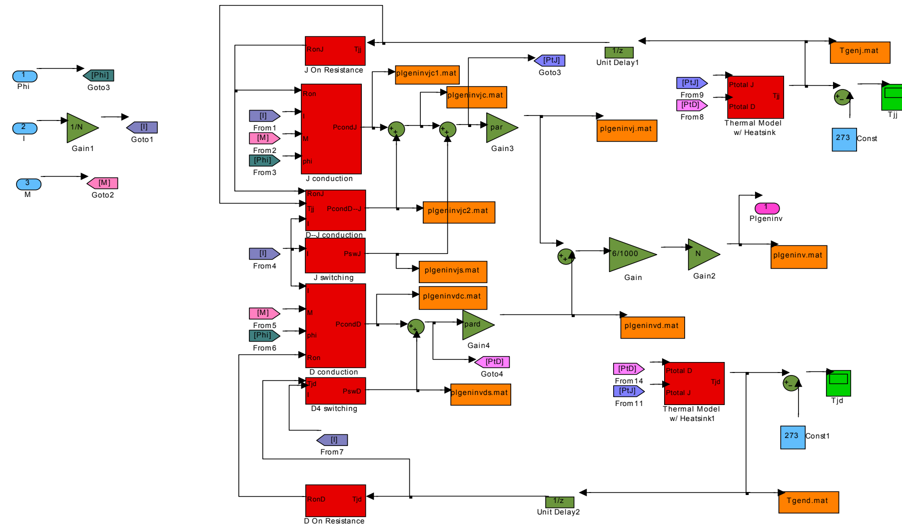
**1. Overview**: Yellow modules are for initialization.
Blue modules are inputs.
Orange modules are outputs.
Red modules are subsystem



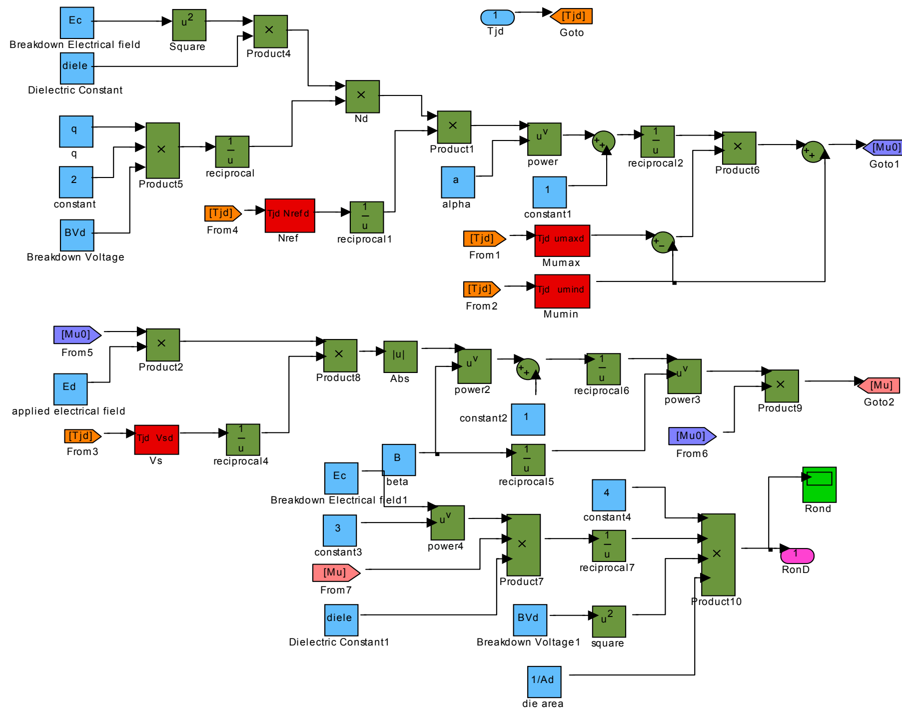

## 2. PM Generator Subsystem



## 3. Generator Inverter Subsystem (similar to grid inverter subsystem)




## 4. D on Resistance Subsystem



## Appendix II — Excel Data sheet showing losses in generator and inverters

## Appendix III

$V_B$ Breakdown voltage

$E_c$ Breakdown electric field

$\mu_n$ Electron Mobility

$\varepsilon$ Relative dielectric constant

$v_s$ Saturated velocity

$N$ Doping density

$V$ Applied voltage of devices

$E$ Applied electric field of devices

$V_{GH}$ Highest gate voltage of MOSFET

$V_{GL}$ Lowest gate voltage of MOSFET

$V_{th}$ Threshold voltage of MOSFET

$g_m$ Transconductance

$t_{rr}$ Total reverse recovery time

$S$ Snappiness factor

$I_R$ Peak reverse recovery current of diodes

$V_R$ Reverse voltage applied to diodes

$V_D$ Constant part of forward voltage drop of diode

$R_{on,sp}$ Specific on resistance

$R_D$ On resistance of diode

$R_{DS,on}$ On resistance of MOSFET

$M$ Modulation index

$\phi$ Phase angle of the current

$f_c$ Switching frequency

$I$ Peak phase current

$J$ Phase current density

$P_M$ Power loss of MOSFET

$P_D$ Power loss of Diode

$T_j$ Junction temperature

$R_{jc}$ Junction-to-case thermal resistance

$C$ Thermal Capacitance

$\tau$ Thermal Constant

**Spreadsheets for Performance Calculations for Converter for Wind Turbine**

| Wind Speed (m/s) nw | Gen Speed (rpm) ng | Gen Pwr In ( kW) pin | Gen Pwr Out ( kW) pgout | Gen EMF (pk I-n) emf | Gen DPF dpf | Gen Volts (pk I-n) ugout | Gen Phase I (A) is | Gen Eff. (%) effgen | Gen Mod Index m |
|---|---|---|---|---|---|---|---|---|---|
| 3.0 | 46 | 30 | 28.9 | 158 | 0.998 | 156.8 | 129.9 | 96.3 | 0.285 |
| 3.5 | 53 | 48 | 46.4 | 182.1 | 0.995 | 180.8 | 179.3 | 96.7 | 0.329 |
| 4.0 | 61 | 73 | 70.8 | 209.6 | 0.991 | 208.4 | 236 | 97 | 0.379 |
| 4.5 | 69 | 104 | 101 | 237 | 0.986 | 236.7 | 296.5 | 97.1 | 0.43 |
| 5.0 | 76 | 143 | 138.8 | 261.1 | 0.979 | 262.1 | 369.2 | 97.1 | 0.477 |
| 5.5 | 84 | 191 | 185.4 | 288.6 | 0.969 | 292.1 | 445.5 | 97.1 | 0.531 |
| 6.0 | 92 | 249 | 241.6 | 316 | 0.957 | 323.4 | 529.6 | 97 | 0.588 |
| 6.5 | 99 | 317 | 307.3 | 340.1 | 0.941 | 353.2 | 625.8 | 96.9 | 0.642 |
| 7.0 | 107 | 397 | 384.5 | 367.6 | 0.923 | 388.6 | 724.5 | 96.8 | 0.707 |
| 7.5 | 115 | 490 | 474.1 | 395.1 | 0.902 | 426.8 | 831.3 | 96.8 | 0.776 |
| 8.0 | 122 | 596 | 575.7 | 419.1 | 0.876 | 465.2 | 952.4 | 96.6 | 0.846 |
| 8.5 | 130 | 717 | 691.8 | 446.6 | 0.849 | 510.6 | 1074.6 | 96.4 | 0.928 |
| 9.0 | 138 | 853 | 822 | 474.1 | 0.819 | 560.5 | 1203.7 | 96.4 | 1.019 |
| 9.5 | 145 | 1004 | 965.8 | 498.1 | 0.786 | 612.3 | 1347.7 | 96.2 | 1.113 |
| 10.0 | 153 | 1174 | 1127.8 | 525.6 | 0.754 | 673 | 1429.9 | 96.1 | 1.178 |
| 10.5 | 160 | 1362 | 1305.9 | 549.6 | 0.718 | 737.1 | 1655.6 | 95.8 | 1.178 |
| 11.0 | 164 | 1554 | 1485.6 | 563.4 | 0.679 | 796.9 | 1842.2 | 95.6 | 1.178 |
| 11.5-27.5 | 164 | 1643 | 1567.3 | 563.4 | 0.657 | 821 | 1947.3 | 95.4 | 1.178 |

| Wind Speed (m/s) nw | Gen Inv MOSFET Cond Loss (W) plgeninvjc | | Gen Inv MOSFET Sw Loss (W) plgeninvjs | | Gen Inv Diode Cond Loss (W) plgeninvdc | | Gen Inv Diode Sw Loss (W) plgeninvds | | Gen Inv Loss (per Inv) (kW) plgeninv | |
|---|---|---|---|---|---|---|---|---|---|---|
| | SiC | Si | SiC | Si | SiC | Si | SiC | Si | SiC | Si |
| 3.0 | 0.4 | 2.5 | 15 | 11.8 | 1.7 | 1.7 | 6.3 | 23.4 | 0.14 | 0.24 |
| 3.5 | 0.9 | 4.5 | 20.7 | 16.2 | 2.3 | 2.4 | 8.6 | 27.2 | 0.2 | 0.3 |
| 4.0 | 1.5 | 7.5 | 27.2 | 21.2 | 2.9 | 3.1 | 11.4 | 32.5 | 0.26 | 0.39 |
| 4.5 | 2.5 | 11.9 | 34.1 | 26.5 | 3.5 | 3.8 | 14.3 | 37.9 | 0.33 | 0.48 |
| 5.0 | 4 | 18 | 42 | 33 | 4 | 5 | 18 | 44 | 0.4 | 0.6 |
| 5.5 | 6 | 27 | 51 | 40 | 5 | 6 | 21 | 52 | 0.5 | 0.7 |
| 6.0 | 9 | 39 | 61 | 47 | 6 | 6 | 25 | 60 | 0.6 | 0.9 |
| 6.5 | 13 | 56 | 72 | 55 | 7 | 8 | 30 | 70 | 0.7 | 1.1 |
| 7.0 | 17 | 77 | 83 | 64 | 7 | 9 | 35 | 80 | 0.9 | 1.4 |
| 7.5 | 24 | 104 | 96 | 74 | 8 | 10 | 40 | 92 | 1 | 1.7 |
| 8.0 | 32 | 140 | 110 | 85 | 9 | 11 | 46 | 107 | 1.2 | 2.1 |
| 8.5 | 42 | 184 | 126 | 97 | 9 | 12 | 52 | 123 | 1.4 | 2.5 |
| 9.0 | 55 | 240 | 143 | 109 | 10 | 13 | 58 | 141 | 1.6 | 3 |
| 9.5 | 70 | 312 | 163 | 124 | 10 | 14 | 58 | 164 | 1.8 | 3.7 |
| 10.0 | 88 | 395 | 185 | 141 | 11 | 17 | 58 | 190 | 2.1 | 4.5 |
| 10.5 | 108 | 494 | 212 | 161 | 15 | 24 | 58 | 223 | 2.4 | 5.4 |
| 11.0 | 133 | 630 | 247 | 186 | 19 | 36 | 58 | 270 | 2.7 | 6.7 |
| 11.5-27.5 | 148 | 721 | 269 | 203 | 22 | 44 | 58 | 301 | 3 | 7.6 |

**Spreadsheets for Performance Calculations for Converter for Wind Turbine (continued)**

| Wind Speed (m/s) nw | Grid Inv Pwr In (kW) Pgeninvout | | Grid Inv I (A) Igrid | | Grid Inv MOSFET Cond Loss (W) plgridinvjc | | Grid Inv MOSFET Sw Loss (W) plgridinvjs | | Grid Inv Diode Cond Loss (W) plgridinvdc | |
|---|---|---|---|---|---|---|---|---|---|---|
| | SiC | Si | SiC | Si | SiC | Si | SiC | Si | SiC | Si |
| 3.0 | 27.5 | 26.5 | 34.2 | 33 | 0.04 | 0.52 | 4 | 3 | 0.13 | 0.13 |
| 3.5 | 44.5 | 43.4 | 55.4 | 54 | 0.12 | 0.88 | 6 | 5 | 0.21 | 0.21 |
| 4.0 | 68.2 | 66.9 | 85 | 83.3 | 0.3 | 1.6 | 10 | 8 | 0.3 | 0.3 |
| 4.5 | 91.7 | 96.1 | 121.7 | 119.7 | 0.6 | 2.9 | 14 | 11 | 0.5 | 0.5 |
| 5.0 | 134.1 | 132.8 | 167.8 | 165.4 | 1 | 5 | 19 | 15 | 0.7 | 0.7 |
| 5.5 | 180.4 | 178 | 224.7 | 221.7 | 2 | 9 | 26 | 20 | 0.9 | 0.93 |
| 6.0 | 235.6 | 232.4 | 293.4 | 289.5 | 3 | 15 | 34 | 26 | 1 | 1 |
| 6.5 | 300 | 296 | 373.7 | 368.7 | 5 | 23 | 43 | 33 | 2 | 2 |
| 7.0 | 375.9 | 370.7 | 468.2 | 461.7 | 8 | 36 | 54 | 41 | 2 | 2 |
| 7.5 | 464 | 457.3 | 578 | 569.6 | 13 | 55 | 66 | 50 | 3 | 3 |
| 8.0 | 563.9 | 555.2 | 702.4 | 691.5 | 19 | 81 | 80 | 61 | 3 | 4 |
| 8.5 | 678 | 666.9 | 844.6 | 830.6 | 28 | 118 | 97 | 74 | 4 | 5 |
| 9.0 | 806 | 791.8 | 1004.1 | 986.2 | 40 | 168 | 117 | 88 | 5 | 6 |
| 9.5 | 947.7 | 928.9 | 1180.5 | 1157.1 | 56 | 236 | 140 | 105 | 6 | 8 |
| 10.0 | 1107.3 | 1083.2 | 1379.2 | 1349.3 | 78 | 332 | 167 | 125 | 8 | 11 |
| 10.5 | 1282.4 | 1251.8 | 1597.4 | 1559.3 | 106 | 463 | 202 | 149 | 9 | 14 |
| 11.0 | 1458.3 | 1418.4 | 1816.4 | 1766.7 | 140 | 633 | 241 | 176 | 11 | 19 |
| 11.5-27.5 | 1537.5 | 1491.1 | 1915.1 | 1857.4 | 158 | 724 | 262 | 189 | 12 | 22 |

| Wind Speed (m/s) nw | Grid Inv Diode Sw Loss (W) plgridinvds | | Grid Inv Loss (per Inv) (kW) plgridinv | | Filter Loss (kW) plfilter | | Total Loss (kW) pgout-plfilterout | | System Eff. (%) effsys | |
|---|---|---|---|---|---|---|---|---|---|---|
| | SiC | Si | SiC | Si | SiC | Si | SiC | Si | SiC | Si |
| 3.0 | 1.7 | 15 | 0.03 | 0.11 | 0.01 | 0.01 | 1.8 | 3.5 | 93.9 | 87.8 |
| 3.5 | 2.6 | 17 | 0.06 | 0.14 | 0.03 | 0.03 | 2.5 | 4.5 | 94.5 | 90.4 |
| 4.0 | 4 | 20 | 0.09 | 0.17 | 0.07 | 0.06 | 3.5 | 5.7 | 95 | 92 |
| 4.5 | 6 | 23 | 0.13 | 0.22 | 0.14 | 0.14 | 4.7 | 7.2 | 95.4 | 92.9 |
| 5.0 | 8 | 26 | 0.18 | 0.28 | 0.3 | 0.27 | 6.1 | 9.1 | 95.6 | 93.4 |
| 5.5 | 10 | 31 | 0.24 | 0.37 | 0.5 | 0.5 | 7.9 | 11.6 | 95.8 | 93.8 |
| 6.0 | 14 | 37 | 0.3 | 0.5 | 0.8 | 0.8 | 10 | 14.7 | 95.9 | 93.9 |
| 6.5 | 18 | 45 | 0.4 | 0.6 | 1.4 | 1.3 | 12.7 | 18.8 | 95.9 | 93.9 |
| 7.0 | 23 | 53 | 0.5 | 0.8 | 2.1 | 2.1 | 15.8 | 23.8 | 95.9 | 93.8 |
| 7.5 | 28 | 64 | 0.7 | 1 | 3.2 | 3.1 | 19.8 | 30.2 | 95.8 | 93.6 |
| 8.0 | 34 | 77 | 0.8 | 1.3 | 4.8 | 4.6 | 24.8 | 38.5 | 95.7 | 93.3 |
| 8.5 | 41 | 93 | 1 | 1.7 | 6.9 | 6.7 | 30.8 | 49 | 95.5 | 92.9 |
| 9.0 | 48 | 112 | 1.3 | 2.2 | 9.8 | 9.4 | 38.3 | 62.1 | 95.3 | 92.4 |
| 9.5 | 57 | 136 | 1.6 | 2.9 | 13.5 | 13 | 47.1 | 79 | 95.1 | 91.8 |
| 10.0 | 58 | 168 | 1.9 | 3.8 | 17.7 | 18 | 57.6 | 100.3 | 94.9 | 91.1 |
| 10.5 | 58 | 209 | 2.2 | 5 | 24.8 | 23.6 | 70.7 | 127.8 | 94.5 | 90.2 |
| 11.0 | 58 | 260 | 2.7 | 6.5 | 32 | 30.3 | 86.4 | 162.8 | 94.2 | 89 |
| 11.5-27.5 | 58 | 287 | 3 | 7.3 | 35.6 | 33.5 | 94.8 | 182.9 | 94 | 88.3 |

**Spreadsheets for Performance Calculations for Converter for Wind Turbine (continued)**

| Wind Speed (m/s) nw | Junction Temperature ( C ) | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | Generator Inverter | | | | Grid Inverter | | | |
| | MOSFET | | Diode | | MOSFET | | Diode | |
| | SiC | Si | SiC | Si | SiC | Si | SiC | Si |
| 3.0 | 33 | 29 | 33 | 33 | 28 | 28 | 28 | 30 |
| 3.5 | 35 | 30 | 35 | 34 | 29 | 29 | 29 | 31 |
| 4.0 | 38 | 31 | 38 | 36 | 31 | 29 | 31 | 32 |
| 4.5 | 40 | 32 | 40 | 38 | 32 | 29 | 32 | 33 |
| 5.0 | 44 | 33 | 44 | 40 | 34 | 30 | 34 | 34 |
| 5.5 | 48 | 35 | 47 | 42 | 37 | 31 | 37 | 35 |
| 6.0 | 52 | 37 | 51 | 45 | 40 | 32 | 40 | 37 |
| 6.5 | 57 | 39 | 56 | 49 | 44 | 34 | 43 | 40 |
| 7.0 | 62 | 41 | 61 | 53 | 49 | 36 | 48 | 43 |
| 7.5 | 68 | 44 | 67 | 58 | 54 | 39 | 53 | 47 |
| 8.0 | 76 | 49 | 74 | 64 | 61 | 42 | 60 | 53 |
| 8.5 | 84 | 53 | 82 | 70 | 70 | 47 | 68 | 59 |
| 9.0 | 93 | 59 | 90 | 78 | 80 | 53 | 78 | 68 |
| 9.5 | 102 | 66 | 100 | 88 | 92 | 60 | 90 | 79 |
| 10.0 | 112 | 74 | 109 | 100 | 105 | 71 | 102 | 90 |
| 10.5 | 124 | 84 | 121 | 115 | 121 | 84 | 118 | 112 |
| 11.0 | 140 | 98 | 136 | 136 | 140 | 101 | 136 | 137 |
| 11.5-27.5 | 150 | 107 | 146 | 150 | 150 | 111 | 145 | 150 |

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The premise of the project was that silicon carbide (SiC) devices would reduce substantially the cost of energy of large wind turbines that need power electronics for variable speed generaton systems. As a wide band gap material, SiC in power devices has several advantages, including lower losses, higher temperature and faster switching. One of the key activities of the project was to actually obtain SiC devices of a type which might be used in a wind turbine converter, and test and characterize them relative to the commonly used IGBT.

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