

Multicore Chip Design and Architecture: (MCDA)

A Joint Initiative between the National Science Foundation and the Semiconductor Research Corporation

Program Solicitation

NSF 08-584



National Science Foundation

Directorate for Computer & Information Science & Engineering
Division of Computing and Communication Foundations

Directorate for Engineering
Electrical, Communications and Cyber Systems

Full Proposal Deadline(s) (due by 5 p.m. proposer's local time):

October 17, 2008

SUMMARY OF PROGRAM REQUIREMENTS

General Information

Program Title:

Multicore Chip Design and Architecture (MCDA)
A Joint Initiative between NSF and SRC

Synopsis of Program:

As Moore's law scaling runs its course, researchers in industry and academia must explore new means by which to ensure continued technological advances in computing. CMOS scaling is increasingly limited by the realities imposed by physics, making architectural innovations the most likely means by which to achieve increased computational performance. Multicore-based systems that modularly integrate multiple, heterogeneous processor cores on a single chip promise computational performance enhancements for both high and low end computing platforms (e.g., from petaflop machines to embedded systems).

Novel research is needed on design, fabrication, architecture and programmability of homogeneous as well as heterogeneous multicore systems that will address virtually all hardware and software aspects of computing system design. NSF and the Semiconductor Research Corporation (SRC) recognize this need, and have agreed to embark on this new collaborative research program to address compelling research challenges in multicore-based systems that are of paramount importance to industry, academia and society at large.

Cognizant Program Officer(s):

- Sankar Basu, Program Director, CCF/CISE/NSF, telephone: (703)292-8910, fax: (703)292-9059, email: sabasu@nsf.gov
- Lawrence Goldberg, Senior Engineering Advisor, ECCS/ENG/NSF, telephone: (703)292-8339, email: lgoldber@nsf.gov

- William H. Joyner, Director/CADTS, SRC, telephone: (919)941-9472, email: william.joyner@src.org
- David Yeh, Director/ICSS, SRC, telephone: (919)941-9464, email: David.Yeh@src.org

Applicable Catalog of Federal Domestic Assistance (CFDA) Number(s):

- 47.041 --- Engineering
- 47.070 --- Computer and Information Science and Engineering

Award Information

Anticipated Type of Award: Standard Grant or Continuing Grant or Other Grant SRC Contract.

Estimated Number of Awards: 15 to 19 projects will be supported as a result of this competition.

Anticipated Funding Amount: \$5,850,000 of which \$3,600,000 will be contributed by NSF, pending availability of funds, and \$2,250,000 will be contributed by SRC.

Eligibility Information

Organization Limit:

Proposals may only be submitted by the following:

- Universities and Colleges: Universities and two- and four-year colleges (including community colleges) located and accredited in the US, acting on behalf of their faculty members. Such organizations also are referred to as academic institutions.

PI Limit:

None Specified

Limit on Number of Proposals per Organization:

None Specified

Limit on Number of Proposals per PI: 1

An individual may participate in at most one proposal as PI, co-PI, or senior personnel.

Proposal Preparation and Submission Instructions

A. Proposal Preparation Instructions

- **Letters of Intent:** Not Applicable
- **Preliminary Proposal Submission:** Not Applicable
- **Full Proposals:**
 - Full Proposals submitted via FastLane: NSF Proposal and Award Policies and Procedures Guide, Part I: Grant Proposal Guide (GPG) Guidelines apply. The complete text of the GPG is available electronically on the NSF website at: http://www.nsf.gov/publications/pub_summ.jsp?ods_key=gpg.
 - Full Proposals submitted via Grants.gov: NSF Grants.gov Application Guide: A Guide for the Preparation and Submission of NSF Applications via Grants.gov Guidelines apply (Note: The NSF Grants.gov Application Guide is available on the Grants.gov website and on the NSF website at: <http://www.nsf.gov/bfa/dias/policy/docs/grantsgovguide.pdf>)

B. Budgetary Information

- **Cost Sharing Requirements:** Cost Sharing is not required under this solicitation.
- **Indirect Cost (F&A) Limitations:** Not Applicable
- **Other Budgetary Limitations:** Other budgetary limitations apply. Please see the full text of this solicitation for further information.

C. Due Dates

- **Full Proposal Deadline(s)** (due by 5 p.m. proposer's local time):

October 17, 2008

Proposal Review Information Criteria

Merit Review Criteria: National Science Board approved criteria apply.

Award Administration Information

Award Conditions: Standard NSF award conditions apply.

Reporting Requirements: Additional reporting requirements apply. Please see the full text of this solicitation for further information.

TABLE OF CONTENTS

Summary of Program Requirements

- I. **Introduction**
- II. **Program Description**
- III. **Award Information**
- IV. **Eligibility Information**
- V. **Proposal Preparation and Submission Instructions**
 - A. Proposal Preparation Instructions
 - B. Budgetary Information
 - C. Due Dates
 - D. FastLane/Grants.gov Requirements
- VI. **NSF Proposal Processing and Review Procedures**
 - A. NSF Merit Review Criteria
 - B. Review and Selection Process
- VII. **Award Administration Information**
 - A. Notification of the Award
 - B. Award Conditions
 - C. Reporting Requirements
- VIII. **Agency Contacts**
- IX. **Other Information**

I. INTRODUCTION

The National Science Foundation (NSF), through its Divisions of Computing and Communication Foundations (CCF) and Electrical, Communications and Cyber Systems (ECCS), has established a partnership with the Semiconductor Research Corporation (SRC), through its Computer-Aided Design & Test Sciences (CADTS), Integrated Circuits & Systems Sciences (ICSS), Interconnect and Packaging Sciences (IPS), and Device Sciences (DS) organizations, to jointly support innovative research activities focused on multicore chip design and architecture.

In order to sustain the continued growth of computational performance, a paradigm shift in computing is needed to realize the full potential of highly and explicitly parallel - yet low power and resilient - computer systems. Parallel systems built from multicore processors (or multicores) modularly integrate multiple, possibly heterogeneous, processor cores on a single chip. Such chips are finding use in both high and low end computing platforms, ranging from petaflops supercomputing systems composed of several thousands of multicores to commodity computers and embedded systems. NSF and SRC have partnered to support state-of-the-art research projects that explore the promise of multicore parallel processing and related computer architectures of the future.

At this time, researchers have a timely opportunity to rethink the design of multicore chips and to design system architectures in ways that need not affect the revenue streams of entrenched manufacturers. Because heterogeneous multicores integrate both novel and conventional processor cores and software on the same chip, a seamless software migration path is achievable, easing the implementation and eventual widespread adoption of radically new processor architectures and platforms. This move to heterogeneous multicore architectures provides a convenient platform to incrementally incorporate domain-optimized specialized cores based on new technologies and architectures. This may lead to the emergence of new computing systems that offer substantial improvements over conventional, von Neumann style systems, in dimensions that include performance, power/energy, cost efficiency, reliability, robustness, security, and programmability.

II. PROGRAM DESCRIPTION

The goal of this NSF-SRC program is to initiate research that leads to significant advances in state-of-the-art multicore chip design and architecture. The program is intended to provide support for single investigators or small groups of investigators committed to realizing systems-level performance improvements and to establishing new and innovative research areas critical to future multicore systems. Proposal topics may range from basic to more applied research in areas such as those described below. Proposals should also discuss how the activities proposed will contribute to the preparation of a diverse, globally-competitive workforce.

1. Architectures for Multicore Systems

On-chip networks or networks-on-chips (NoCs) support the homogeneous or heterogeneous interconnection of processor cores and various levels of the memory hierarchy to facilitate the movement of large amounts of data in minimal time. These networks are key to realizing multicore architectures. Problems of communication latency and throughput, area overhead, design complexity, etc., must be overcome. Research is needed on modeling and evaluating alternative NoC topologies, routing strategies, flow control, coding techniques, router microarchitectures, NoC interfaces, and memory interconnect solutions. Related compiler and dynamic techniques for managing scalable on-chip communication are also needed.

Research into new parallel programming models, memory models/architectures, and hardware and software primitives that facilitate the programmability of multicores for existing and emerging applications is needed. This includes research into hardware and software transactional memories, scalable and highly concurrent synchronization primitives, and compiler and run-time system software support. Optimizing performance by mixing general purpose cores with special purpose cores for applications such as high-end graphics, signal processing, network processing, etc., is also important.

Since multicores are likely to be more useful for heterogeneous structures composed of multiple processor cores, accelerators, 3D structures, etc., research is needed on how to design software tailored to hardware structures in support of various applications. This hardware/software co-design effort will require identifying re-usable hardware functions (i.e., general purpose and application-specific accelerator functions) and software partitioning decompositions that support new applications and systems development.

Techniques for dynamic self-test/diagnosis, transient and permanent fault isolation, and reconfiguration/self-repair of components across multiple levels are needed. Architectures that maximize chip lifetime reliability by efficiently utilizing redundancy across all levels are also needed, including memory cell, memory block, logic module, pipeline stage, data path, and inter-core on-chip network levels. Efficient test methods for multicore systems will need to include design for test in a multicore environment. Improved test techniques

for multicore systems, post-silicon validation and repair, on-line test techniques enabled by multicores, and test techniques which enable resilient design and graceful degradation are also topics of interest.

2. CAD for Multicore Systems

Behavioral and logic synthesis of multicore systems will require advances beyond current techniques. Research challenges include tools for synthesis of both general purpose and special purpose (e.g., domain-optimized) systems; efficient allocation of system resources to cores; fast early estimation and design space exploration of multicore granularity options; system architecture resource virtualization to enable cores to efficiently access shared physical resources; tools for synthesizing asynchronous designs; and automated clocking solutions for process variation control.

Research on physical design tools specific to multicores is needed. These include place and route tools aware of thermal, power, voltage, and latency constraints; tools for the reduction of noise and crosstalk in multicore systems; tools to adapt individual cores to their local environments; and power/clock distribution tools.

Assuring correctness of multicore systems presents new challenges, including verification of parallel properties inherent in multicore systems, verification of distributed algorithm behavior, verification of resilient multicore systems which adapt to workload or error-detection factors at runtime, and pre-silicon formal verification and simulation based methods including mixed-mode and mixed-technology simulation. Methods for exploring hardware-assisted emulation technology to drastically accelerate validation over pure simulation-based approaches are of interest as well.

There is a need to co-evolve a fundamental understanding of manufacturing and multicore architecture design space exploration to facilitate data management and communication at exceptionally high data rates. Novel approaches for compression and decompression algorithms and associated hardware technologies are needed that enable the delivery of massive multicore data streams seamlessly from design hierarchy to layout. The challenge is the design of robust high-speed digital circuit implementations at the patterning element level for receiving, decompressing, and distributing pattern data, including compression algorithms that map efficiently into VLSI.

Multicore platforms will enable improved extraction algorithms, graph traversal and manipulation, applications involving searching and sorting, faster simulation, design rule checks, resolution enhancement techniques, grid-based applications, test and verification techniques, digital and analog simulation, synthesis, placement, routing and other CAD applications. Research is needed in leveraging multicore platforms for these applications.

3. Interconnect and Packaging Technologies for Multicores

Research targets in this area include interconnect system level optimization, interconnect technologies, and packaging technologies.

Simulation of multicore system-level performance and power as a function of interconnect bandwidth and latency for various architectures and applications are of interest. This also includes detailed simulation of multicore signal integrity and power delivery noise. Research on optical interconnect and 3D interconnect technologies are of interest. This includes the feasibility of optical interconnect with wavelength division multiplexing to provide optical crossbar, router, and high-bandwidth/low-latency resource sharing. The potential of variable pitch 3D interconnect technologies for increased die-to-die communication enabling multicore integration is of interest as are the issues of thermal/performance tradeoffs in this context. Heterogeneous integration of divergent technologies, e.g., multi-chip packages, stacked packages, and stacked die can be considered. Solutions for advanced hot-spot mitigation, such as thermoelectric coolers, liquid phase cooling, and core hopping also need further exploration.

4. Circuit Techniques for Multicore Design

Research on both low power digital and analog circuits is needed to reduce power consumption of multicore designs without sacrificing system level performance. Design and modeling techniques for thermal sensing circuits that can be integrated into multicore chips for use in power management systems is needed. Efficient voltage converters are needed to work with power management systems that optimize overall system performance with respect to system power by controlling supply voltage.

Research to understand techniques for moving large volumes of data within the multicore chip will be key to improved performance. To this end, optimal bus configurations, differential techniques, packetized switching fabrics, and coding techniques can all be re-visited in the multicore context as well.

Techniques to reduce noise and crosstalk grow in importance with number of cores. Performance and synchronization requirements dictate manufacturing for design capability that enables centered, low variability fabrication technologies. This research challenge at the design-technology interface involves exploring the effect of variability with respect to critical performance and multicore architecture requirements.

5. Low Power Innovations for Multicore

Research on hardware and software support for optimizing performance-per-watt and energy-per-instruction, and efficiently managing power and temperature of multicore resources is important. Tool development for power reduction and power analysis is also important, as are other tools aware of the multicore context. Relevant issues can be addressed at various levels of the design hierarchy, e.g., at the device, interconnect, circuit, or architectural level.

The potential for power delivery in multicores by integrated dynamic voltage transformers and inter-core power sharing concepts needs to be explored. Asynchronous signaling modes, 3D interconnects, and optical interconnects constitute other topics of research in the context of low power design. The potential for power minimization offered by multicore parallelism including that for novel memory structures, while maintaining performance by exploiting voltage scaling at the near-threshold or sub-threshold regime, needs to be examined as well.

III. AWARD INFORMATION

Each project will be jointly funded by the NSF and the SRC through separate NSF and SRC funding instruments. For each project, NSF support will be provided via an NSF grant and SRC support will be provided via a standard SRC contract. Depending upon the nature of the project, the total of the NSF grant plus SRC contract will range from \$100,000 to \$300,000 per year for 3 years, pending the availability of funds. It is anticipated that approximately 15-19 projects will be supported.

IV. ELIGIBILITY INFORMATION

Organization Limit:

Proposals may only be submitted by the following:

- Universities and Colleges: Universities and two- and four-year colleges (including community colleges) located and accredited in the US, acting on behalf of their faculty members. Such organizations also are referred to as academic institutions.

PI Limit:

None Specified

Limit on Number of Proposals per Organization:

None Specified

Limit on Number of Proposals per PI: 1

An individual may participate in at most one proposal as PI, co-PI, or senior personnel.

Additional Eligibility Info:

Synergistic collaborations or partnerships with industry or government are encouraged when appropriate, though no NSF or SRC funds will be provided to these organizations. Industrial participation need not be limited to SRC member companies.

Researchers from foreign academic institutions who contribute essential expertise to the project may

participate as co-PIs or Senior Personnel but may not receive NSF or SRC support.

V. PROPOSAL PREPARATION AND SUBMISSION INSTRUCTIONS

A. Proposal Preparation Instructions

Full Proposal Preparation Instructions: Proposers may opt to submit proposals in response to this Program Solicitation via Grants.gov or via the NSF FastLane system.

- Full proposals submitted via FastLane: Proposals submitted in response to this program solicitation should be prepared and submitted in accordance with the general guidelines contained in the NSF Grant Proposal Guide (GPG). The complete text of the GPG is available electronically on the NSF website at: http://www.nsf.gov/publications/pub_summ.jsp?ods_key=gpg. Paper copies of the GPG may be obtained from the NSF Publications Clearinghouse, telephone (703) 292-7827 or by e-mail from pubs@nsf.gov. Proposers are reminded to identify this program solicitation number in the program solicitation block on the NSF Cover Sheet For Proposal to the National Science Foundation. Compliance with this requirement is critical to determining the relevant proposal processing guidelines. Failure to submit this information may delay processing.
- Full proposals submitted via Grants.gov: Proposals submitted in response to this program solicitation via Grants.gov should be prepared and submitted in accordance with the NSF Grants.gov Application Guide: A Guide for the Preparation and Submission of NSF Applications via Grants.gov. The complete text of the NSF Grants.gov Application Guide is available on the Grants.gov website and on the NSF website at: (<http://www.nsf.gov/bfa/dias/policy/docs/grantsgovguide.pdf>). To obtain copies of the Application Guide and Application Forms Package, click on the Apply tab on the Grants.gov site, then click on the Apply Step 1: Download a Grant Application Package and Application Instructions link and enter the funding opportunity number, (the program solicitation number without the NSF prefix) and press the Download Package button. Paper copies of the Grants.gov Application Guide also may be obtained from the NSF Publications Clearinghouse, telephone (703) 292-7827 or by e-mail from pubs@nsf.gov.

In determining which method to utilize in the electronic preparation and submission of the proposal, please note the following:

Collaborative Proposals. All collaborative proposals submitted as separate submissions from multiple organizations must be submitted via the NSF FastLane system. Chapter II, Section D.3 of the Grant Proposal Guide provides additional information on collaborative proposals.

Supplementary Docs:

In order to be considered for funding in this program, every proposal MUST include a statement of consent from the proposing institution(s) that indicates that NSF may share the proposal, reviews generated for the proposal, and related information, with SRC. The statement of consent must be uploaded into the Supplementary Docs section in Fastlane or Grants.gov. Proposals that do not contain this statement will be returned without review.

For proposals involving academic institutions and industry, proposers should include a letter from the industrial partner(s) that confirm(s) the participation of one or more co-PIs from industry. This letter, uploaded in the Supplementary Documents section in FastLane or Grants.gov, should describe a plan for interaction between the industrial and academic partners, the time commitment of the industrial researcher(s), and the nature of the work.

B. Budgetary Information

Cost Sharing: Cost sharing is not required under this solicitation.

Other Budgetary Limitations:

Researchers from foreign academic institutions who contribute essential expertise to the project may participate as co-PIs or senior personnel but may not request NSF or SRC support. Synergistic collaborations or partnerships with industry or government are encouraged when appropriate, though no NSF or SRC funds will be provided to these organizations.

C. Due Dates

- **Full Proposal Deadline(s)** (due by 5 p.m. proposer's local time):

D. FastLane/Grants.gov Requirements

• For Proposals Submitted Via FastLane:

Detailed technical instructions regarding the technical aspects of preparation and submission via FastLane are available at: <https://www.fastlane.nsf.gov/a1/newstan.htm>. For FastLane user support, call the FastLane Help Desk at 1-800-673-6188 or e-mail fastlane@nsf.gov. The FastLane Help Desk answers general technical questions related to the use of the FastLane system. Specific questions related to this program solicitation should be referred to the NSF program staff contact(s) listed in Section VIII of this funding opportunity.

Submission of Electronically Signed Cover Sheets. The Authorized Organizational Representative (AOR) must electronically sign the proposal Cover Sheet to submit the required proposal certifications (see Chapter II, Section C of the Grant Proposal Guide for a listing of the certifications). The AOR must provide the required electronic certifications within five working days following the electronic submission of the proposal. Further instructions regarding this process are available on the FastLane Website at: <https://www.fastlane.nsf.gov/fastlane.jsp>.

• For Proposals Submitted Via Grants.gov:

Before using Grants.gov for the first time, each organization must register to create an institutional profile. Once registered, the applicant's organization can then apply for any federal grant on the Grants.gov website. The Grants.gov's Grant Community User Guide is a comprehensive reference document that provides technical information about Grants.gov. Proposers can download the User Guide as a Microsoft Word document or as a PDF document. The Grants.gov User Guide is available at: <http://www.grants.gov/CustomerSupport>. In addition, the NSF Grants.gov Application Guide provides additional technical guidance regarding preparation of proposals via Grants.gov. For Grants.gov user support, contact the Grants.gov Contact Center at 1-800-518-4726 or by email: support@grants.gov. The Grants.gov Contact Center answers general technical questions related to the use of Grants.gov. Specific questions related to this program solicitation should be referred to the NSF program staff contact(s) listed in Section VIII of this solicitation.

Submitting the Proposal: Once all documents have been completed, the Authorized Organizational Representative (AOR) must submit the application to Grants.gov and verify the desired funding opportunity and agency to which the application is submitted. The AOR must then sign and submit the application to Grants.gov. The completed application will be transferred to the NSF FastLane system for further processing.

VI. NSF PROPOSAL PROCESSING AND REVIEW PROCEDURES

Proposals received by NSF are assigned to the appropriate NSF program where they will be reviewed if they meet NSF proposal preparation requirements. All proposals are carefully reviewed by a scientist, engineer, or educator serving as an NSF Program Officer, and usually by three to ten other persons outside NSF who are experts in the particular fields represented by the proposal. These reviewers are selected by Program Officers charged with the oversight of the review process. Proposers are invited to suggest names of persons they believe are especially well qualified to review the proposal and/or persons they would prefer not review the proposal. These suggestions may serve as one source in the reviewer selection process at the Program Officer's discretion. Submission of such names, however, is optional. Care is taken to ensure that reviewers have no conflicts of interest with the proposal.

A. NSF Merit Review Criteria

All NSF proposals are evaluated through use of the two National Science Board (NSB)-approved merit review criteria: intellectual merit and the broader impacts of the proposed effort. In some instances, however, NSF will employ additional criteria as required to highlight the specific objectives of certain programs and activities.

The two NSB-approved merit review criteria are listed below. The criteria include considerations that help define them. These considerations are suggestions and not all will apply to any given proposal. While proposers must address both merit review criteria, reviewers will be asked to address only those considerations that are relevant to the proposal being considered and for which the reviewer is qualified to make judgements.

What is the intellectual merit of the proposed activity?

How important is the proposed activity to advancing knowledge and understanding within its own field or

across different fields? How well qualified is the proposer (individual or team) to conduct the project? (If appropriate, the reviewer will comment on the quality of the prior work.) To what extent does the proposed activity suggest and explore creative, original, or potentially transformative concepts? How well conceived and organized is the proposed activity? Is there sufficient access to resources?

What are the broader impacts of the proposed activity?

How well does the activity advance discovery and understanding while promoting teaching, training, and learning? How well does the proposed activity broaden the participation of underrepresented groups (e.g., gender, ethnicity, disability, geographic, etc.)? To what extent will it enhance the infrastructure for research and education, such as facilities, instrumentation, networks, and partnerships? Will the results be disseminated broadly to enhance scientific and technological understanding? What may be the benefits of the proposed activity to society?

Examples illustrating activities likely to demonstrate broader impacts are available electronically on the NSF website at: <http://www.nsf.gov/pubs/gpg/broaderimpacts.pdf>.

NSF staff also will give careful consideration to the following in making funding decisions:

Integration of Research and Education

One of the principal strategies in support of NSF's goals is to foster integration of research and education through the programs, projects, and activities it supports at academic and research institutions. These institutions provide abundant opportunities where individuals may concurrently assume responsibilities as researchers, educators, and students and where all can engage in joint efforts that infuse education with the excitement of discovery and enrich research through the diversity of learning perspectives.

Integrating Diversity into NSF Programs, Projects, and Activities

Broadening opportunities and enabling the participation of all citizens -- women and men, underrepresented minorities, and persons with disabilities -- is essential to the health and vitality of science and engineering. NSF is committed to this principle of diversity and deems it central to the programs, projects, and activities it considers and supports.

B. Review and Selection Process

Proposals submitted in response to this program solicitation will be reviewed by Panel Review.

Reviewers will be asked to formulate a recommendation to either support or decline each proposal. The working group consisting of NSF program officers and SRC program managers will consider the advice of the panel in making their recommendations to their respective organizations.

After scientific, technical and programmatic review and consideration of appropriate factors, the NSF Program Officer recommends to the cognizant Division Director whether the proposal should be declined or recommended for award. NSF is striving to be able to tell applicants whether their proposals have been declined or recommended for funding within six months. The time interval begins on the deadline or target date, or receipt date, whichever is later. The interval ends when the Division Director accepts the Program Officer's recommendation.

A summary rating and accompanying narrative will be completed and submitted by each reviewer. In all cases, reviews are treated as confidential documents. Verbatim copies of reviews, excluding the names of the reviewers, are sent to the Principal Investigator/Project Director by the Program Officer. In addition, the proposer will receive an explanation of the decision to award or decline funding.

Proposers will be contacted by a Program Officer of the NSF and SRC joint working group after the recommendation to award or decline funding has been approved by the respective organizations. This informal notification in the case of an award recommendation is not a guarantee of an eventual award. In all cases, after programmatic approval has been obtained, the proposals recommended for funding will be forwarded to the Division of Grants and Agreements for review of business, financial, and policy implications and the processing and issuance of a grant or other agreement. At the same time, the proposal will be forwarded to SRC for issuance of an independent award from SRC.

Proposers are cautioned that only a Grants and Agreements Officer may make commitments, obligations or awards on behalf of NSF or authorize the expenditure of funds. No commitment on the part of NSF should be inferred from technical or budgetary discussions with a NSF Program Officer. A Principal Investigator or organization that makes financial or personnel commitments in the absence of a grant or cooperative agreement signed by the NSF Grants and Agreements Officer does so at their own risk.

VII. AWARD ADMINISTRATION INFORMATION

A. Notification of the Award

Notification of the award is made to *the submitting organization* by a Grants Officer in the Division of Grants and Agreements. Organizations whose proposals are declined will be advised as promptly as possible by the cognizant NSF Program administering the program. Verbatim copies of reviews, not including the identity of the reviewer, will be provided automatically to the Principal Investigator. (See Section VI.B. for additional information on the review process.)

B. Award Conditions

Individual awards will be jointly funded by the NSF and SRC through separate NSF and SRC funding instruments. NSF awards will be made in FY 2009 as continuing or standard grants. SRC awards will be made as standard SRC contracts. For each award, NSF and SRC contributions will be in proportion to their overall contributions to the program. Beyond the base level of support, either organization may supplement a project for special purposes, such as education or development, without requiring the other party to provide any additional funds. The NSF/SRC awards will be made for three-year periods. All awards involving NSF funds will be subject to the intellectual property provisions of Bayh-Dole Act. All joint or separate awards involving SRC funds must also include an executed agreement on intellectual property, including publications and patent rights, signed by the representatives of the awardee organization and SRC. SRC contracts provide for non-exclusive, royalty free rights to all SRC members for any intellectual property generated as a result of the SRC-funded research.

An NSF award consists of: (1) the award letter, which includes any special provisions applicable to the award and any numbered amendments thereto; (2) the budget, which indicates the amounts, by categories of expense, on which NSF has based its support (or otherwise communicates any specific approvals or disapprovals of proposed expenditures); (3) the proposal referenced in the award letter; (4) the applicable award conditions, such as Grant General Conditions (GC-1); * or Research Terms and Conditions * and (5) any announcement or other NSF issuance that may be incorporated by reference in the award letter. Cooperative agreements also are administered in accordance with NSF Cooperative Agreement Financial and Administrative Terms and Conditions (CA-FATC) and the applicable Programmatic Terms and Conditions. NSF awards are electronically signed by an NSF Grants and Agreements Officer and transmitted electronically to the organization via e-mail.

*These documents may be accessed electronically on NSF's Website at http://www.nsf.gov/awards/managing/award_conditions.jsp?org=NSF. Paper copies may be obtained from the NSF Publications Clearinghouse, telephone (703) 292-7827 or by e-mail from pubs@nsf.gov.

More comprehensive information on NSF Award Conditions and other important information on the administration of NSF awards is contained in the NSF *Award & Administration Guide* (AAG) Chapter II, available electronically on the NSF Website at http://www.nsf.gov/publications/pub_summ.jsp?ods_key=aag.

C. Reporting Requirements

NSF and SRC will manage their respective awards/contracts in accordance with their own guidelines. Awardees will submit annual project reports to NSF via FastLane, subject to NSF procedures. Awardees will also submit annual reports to SRC, subject to SRC procedures.

For all multi-year NSF grants (including both standard and continuing grants), the Principal Investigator must submit an annual project report to the cognizant Program Officer at least 90 days before the end of the current budget period. (Some programs or awards require more frequent project reports). Within 90 days after expiration of a grant, the PI also is required to submit a final project report.

Failure to provide the required annual or final project reports will delay NSF review and processing of any future funding increments as well as any pending proposals for that PI. PIs should examine the formats of the required reports in advance to assure availability of required data.

PIs are required to use NSF's electronic project-reporting system, available through FastLane, for preparation and submission of annual and final project reports. Such reports provide information on activities and findings, project participants (individual and organizational) publications; and, other specific products and contributions. PIs will not be required to re-enter information previously provided, either with a proposal or in earlier updates using the electronic system. Submission of the report via FastLane constitutes certification by the PI that the contents of the report are accurate and complete.

SRC will organize and conduct annual reviews and will require certain deliverable reports to monitor the program and project

progress. SRC will seek to provide structured involvement of industry in the research and review process and will undertake the organization and cost of the annual review.

Grantees of this program will be expected to attend, and shall budget for, annual SRC grantee review meetings for the purpose of sharing research progress with SRC member company representatives as well as other interested individuals. The first such meeting will be held approximately nine months after the awards are made, and succeeding meetings will be held every 12 months thereafter. Thirty days before each of these meetings, the principal investigator will provide SRC an annotated power point viewgraph presentation of research results for posting on the SRC Web site.

Annual on-site reviews may also be conducted for larger awards, if deemed necessary by NSF and/or SRC.

VIII. AGENCY CONTACTS

General inquiries regarding this program should be made to:

- Sankar Basu, Program Director, CCF/CISE/NSF, telephone: (703)292-8910, fax: (703)292-9059, email: sabasu@nsf.gov
- Lawrence Goldberg, Senior Engineering Advisor, ECCS/ENG/NSF, telephone: (703)292-8339, email: lgolbber@nsf.gov
- William H. Joyner, Director/CADTS, SRC, telephone: (919)941-9472, email: william.joyner@src.org
- David Yeh, Director/ICSS, SRC, telephone: (919)941-9464, email: David.Yeh@src.org

For questions related to the use of FastLane, contact:

- FastLane Help Desk, telephone: 1-800-673-6188; e-mail: fastlane@nsf.gov.

For questions relating to Grants.gov contact:

- Grants.gov Contact Center: If the Authorized Organizational Representatives (AOR) has not received a confirmation message from Grants.gov within 48 hours of submission of application, please contact via telephone: 1-800-518-4726; e-mail: support@grants.gov.

Additional Program Contacts:

Chitaranjan Das, Program Director, CCF/CISE/NSF, telephone: (703)292-8910, email: cdas@nsf.gov

Timothy Pinkston, Program Director, OAD/CISE/NSF, telephone: (703)292-8910, email: tpinksto@nsf.gov

Pradeep Fulay, Program Director, ECCS/ENG/NSF, telephone: (703)292-8339, email: pfulay@nsf.gov

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IX. OTHER INFORMATION

The NSF Website provides the most comprehensive source of information on NSF Directorates (including contact information), programs and funding opportunities. Use of this Website by potential proposers is strongly encouraged. In addition, MyNSF (formerly the Custom News Service) is an information-delivery system designed to keep potential proposers and other interested parties apprised of new NSF funding opportunities and publications, important changes in proposal and award policies and procedures, and upcoming NSF Regional Grants Conferences. Subscribers are informed through e-mail or the user's Web browser each time new publications are issued that match their identified interests. MyNSF also is available on NSF's Website at <http://www.nsf.gov/mynsf/>.

Grants.gov provides an additional electronic capability to search for Federal government-wide grant opportunities. NSF funding opportunities may be accessed via this new mechanism. Further information on Grants.gov may be obtained at <http://www.grants.gov>.

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NSF funds research and education in most fields of science and engineering. It does this through grants and cooperative agreements to more than 2,000 colleges, universities, K-12 school systems, businesses, informal science organizations and other research organizations throughout the US. The Foundation accounts for about one-fourth of Federal support to academic institutions for basic research.

NSF receives approximately 40,000 proposals each year for research, education and training projects, of which approximately 11,000 are funded. In addition, the Foundation receives several thousand applications for graduate and postdoctoral fellowships. The agency operates no laboratories itself but does support National Research Centers, user facilities, certain oceanographic vessels and Antarctic research stations. The Foundation also supports cooperative research between universities and industry, US participation in international scientific and engineering efforts, and educational activities at every academic level.

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The National Science Foundation Information Center may be reached at (703) 292-5111.

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- **Location:** 4201 Wilson Blvd. Arlington, VA 22230
- **For General Information** (NSF Information Center): (703) 292-5111
- **TDD (for the hearing-impaired):** (703) 292-5090

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