MODELLING CHINA'S SEMICONDUCTOR INDUSTY FLUORINATED COMPOUND EMISSIONS AND DRAFTNG A ROADMAP FOR CLIMATE PROTECTION

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Abstract

We examine the fluorinated compound (FC) high-global warming potential (GWP) greenhouse gas emissions produced during the manufacture of silicon semiconductor devices over the period 1995 to 2020. The analysis includes the contributions of members of the World Semiconductor Council (WSC) charter members (Europe, Japan, Korea, Taiwan and the United States) and China, the newest WSC member. World uncontrolled FC emissions are assumed proportional to world total manufactured layer area (TMLA) for all devices made using silicon wafers in accordance with the U. S. EPA's PFC Emissions Vintage Model (PEVM).

Trends in the global consumption of TMLA indicate a compound annual growth rate of approximately 9 percent per year, higher than the silicon consumption growth rate of approximately 6 percent per year. We project global uncontrolled FC emissions by 2020 to be just below 70 Million Metric Tons of Carbon Equivalent (MMTCE), up from 5.4 MMTCE in 1995. Three TMLA growth scenarios for China are considered: conservative, intermediate and aggressive for which China's 2020 uncontrolled FC emissions equal 6.8, 10.2 and 15.0 MMTCE, respectively. For comparison, WSC charter members' aggregate emissions at 2020 are projected at 4.3 MMTCE, the result of charter members attaining their emissions reduction target. We conclude by exploring emissions from Chinese manufacturers under alternative emission reduction scenarios. We show that were Chinese manufacturers to adopt a baseline year of 2005 and a reduction target of 10 percent below baseline year emissions to be achieved by 2020, emissions would be 0.9 MMTCE, comparable to the controlled emissions of the average WSC charter member (=4.3/5 MMTCE) in 2020. We also show that the relative stringency of the alternative reduction scenarios considered for China vary between 50 to 95 percent reduction compared to business as usual (BAU). A climate protection commitment of this scale would be comparable to the stringency of the WSC charter members' goals, for which FC emission reduction technologies are currently available.

Introduction

In June of 2006 the Semiconductor Industry Association in China (SIAC) joined the World Semiconductor Council (WSC). WSC's charter members voluntarily committed in 2000 to reducing emissions of high-global warming potential (GWP) fluorinated compounds (FCs) to 10 percent below baseline emissions by 2010, and more recently have expressed their intention to limit emissions at or below 2010 levels through 2020.[1,2] SIAC, however, has not yet committed to limit its FC emissions, an important step for the WSC and global semiconductor industry to maintain its leadership role in climate protection.[3]

Semiconductor manufacturing requires the use of high GWP FCs including perfluorocarbons (e.g., CF_4, C_2F_6, C_3F_8), trifluoromethane (CHF_3), nitrogen trifluoride (NF_3), and sulfur hexafluoride (SF_6). FCs are unsurpassed in their process performance and vital to etching intricate circuitry features on silicon wafers and for cleaning chemical vapor deposition (CVD) tool chambers. Although PFC use did not begin until the late 1980s, their application facilitated the development of significantly more complex and faster processing semiconductors. Under normal operating conditions, anywhere from 10 to 80 percent of the FC gases may pass through the manufacturing tools to the air.

China's FC usage from integrated circuits (IC) fabrication is increasing, a consequence of its increasing global share in IC manufacturing capacity and its approaching parity in IC manufacturing complexity with other WSC members.[4] Depending on the ebb and flow of normal business cycles, the time for constructing new planned fabs, expanding existing fab capacity or ramping-up production in fabs may be extended. But if historical comparisons between SIAC and the WSC-Charter members hold even approximately, most or all of China's currently planned fab capacity increases will likely be operational by 2010-2012.[5,6] Then, China's share of global capacity would approach 10 percent, up from 7 percent in 2005.[7]

Underpinning China's manufacturing growth from the mid-1990s to the present are electronics and information products that play a huge role in its external trade, both imports and exports. To satisfy its domestic demand and to advance its export position, the Chinese government offers a range of financial incentives to domestic and foreign companies through 500 specialized investment zones.[8] These incentives and access to China's domestic markets are attracting world-class semiconductor manufacturers to build leading-edge greenfield fabs or to form novel partnerships with domestic manufacturers, which often entail exchanging leading-edge process technologies for manufacturing

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[1] International Technology Roadmap for Semiconductors, 2006 Update, see Tables 104a & 104b, pp.4 and 5. Charter members of WSC are Semiconductor Industry Association in Chinese Taipei, Semiconductor Industry Association in Europe, Semiconductor Industry Association in Korea, Semiconductor Industry Association in Japan and Semiconductor Industry Association in United States.

[2] Starting in 2010 WSC-Charter members from the United States, Europe, and Japan pledged to cap their emissions to 10 percent lower than their 1995 emissions. Although, Korea and Taiwan have pledged to cap their emissions to 10 percent lower than their 1997 and 1998 (average of 1997 and 1999) emissions, respectively, for simplicity our model assumes that their baseline year is 1995 as well. This assumption was analyzed, and its effects on the model results proved inconsequential.

[3] U.S. EPA Climate Protection Award winners have included several players in this industry, including the WSC, International SEMATECH, device manufacturers, industry vendors, and three individuals. Available at: http://www.epa.gov/cppd/awards/complistofwinners.html

[4] See World Fab Watch 2000, 2002, 2004, 2006 and 2007 Editions.

[5] cf. 2000-2004 growth in China amid global downturn as reported in **WaferNews**, "China establishing foundry market foothold", April 2005.

[6] See Montgomery, J. "Too much 300 mm capacity or not enough? Have faith says analyst", **WaferNews,** January 2007.

[7] Developed from 2007 edition of World Fab Watch, as will be described later in this paper.

[8] See Hufbauer, G. C. and Wong, Y. "China Bashing 2004", **International Economics Policy Briefs**, Number PB04-5, September 2004.

capacity with China's foundries.[9,10] The policies of some governments of WSC-Charter members to restrict or slow the transfer of leading-edge manufacturing technologies to China appear not to be working.[11,12,13,14,15] To the extent technology transfer is delayed, this seems attributable to manufacturers' concerns about China's approach to protect their innovations rather than restraints of their governments.[16]

China's IC industry took 10 years to grow from a scale of 1 billion Yuan in the early 1990s to 10 billion in 2000; it took just six years to grow to 100 billion Yuan, another 10-fold.[17] In light of China's rapidly strengthening role in the semiconductor industry our objective is to answer two questions: (1) in the face of the potential growth in FC usage from China, what are the implications for China's contribution to global FC emissions, and (2) what opportunities exist for limiting China's emissions growth? The data and methods used to model China FC emissions, and the resulting opportunities to reduce these emissions are discussed in the remaining sections of the paper.

Data and Methods

Our approach explains emissions via the framework of EPA's PFC Emissions Vintage Model (PEVM), which estimates annual uncontrolled aggregate FC emissions as a product of an unchanging emissions factor and total manufactured layer area (TMLA).[18,19] The TMLA includes both the silicon wafer and the metal interconnects used in IC fabrication, and is derived by multiplying the silicon wafer area by the total number of layers.[20] In this paper, area is described in terms of million square inches and denoted as MSI when referring to silicon and as *MSI* when referring to TMLA. The rationale for using TMLA in *MSI* as the unit of activity governing emissions stems from the IC fabrication process. Each manufactured layer, including the silicon wafer and metal interconnect layers, employs FC-use during etching and chamber cleaning, of which some is emitted to the atmosphere without explicit control. The relationship between emissions and TMLA formally defines an emissions factor with units of Million Metric Tons of Carbon Equivalent (MMTCE) per average manufactured *MSI*. In this paper the emissions factor is 6.11 x

[9] Doe, P. "Downturn pushes China foundries toward smaller geometries, more emphasis on service", **Solid State Technology**, April 2002.
[10] Clendenin, M., "Semiconductors aid China focus on IP issues", **EE Times**, March 20, 2006.
[11] (a) One policy is implemented through the Wassenaar Arrangement (short for "The Wassenaar Arrangement on Export Controls for Conventional Arms and Dual-Use Goods and Technologies), which is an arms control convention with 41 participating states: Argentina, Australia, Austria, Belgium, Bulgaria, Canada, Croatia, Czech Republic, Denmark, Estonia, Finland, France, Germany, Greece, Hungary, Ireland, Israel, Italy, Japan, Latvia, Lithuania, Luxembourg, Malta, Netherlands, New Zealand, Norway, Poland, Portugal, Republic of Korea, Romania, Russian Federation, Slovakia, Slovenia, South Africa, Spain, Sweden, Switzerland, Turkey, Ukraine, United Kingdom and United States.
(b) Until 2002, the Taiwan government, not a party to the Wassenaar Arrangement, had a total ban on semiconductor investment in China. Since then several revisions and relaxations of Taiwan's policy have occurred. Intel, ON Semiconductor (S. Deffree, "China industry hits $13b", **Electronic News,** March 23, 3007) and earlier STMicroelectronics and Hynix reported in "Why China will keep pushing 200mm as far as it will go", **WaferNews**, January 2005, *Op cit* footnote 6)
[12] Intel and ON Semiconductor recently announced investments in China that advances manufacturing technology in China (S. Deffree, "China industry hits $13b", **Electronic News,** March 23, 3007); earlier STMicroelectronics and Hynix announced bringing advanced manufacturing technology to China ("Why China will keep pushing 200mm as far as it will go", **WaferNews**, January 2005); *Op cit* footnote. 6; and "2005 Report to Congress of the U.S.-China Economic and Security Commissions", .pp.32-33 and 105, 109th Congress, 1st Session, U.S. Government Printing Office, Washington, DC, November 2005.
[13] "Semiconductor Report-Third Quarter-2003", **US-Taiwan Business Council**, pp. 11-13, October, 2003.
[14] Bishop, M. W., "Chips, cheap labor bridging Taiwan Strait", **Asia Times**, April 27, 2004.
[15] Williams, M. "Taiwan loosens up on China investments", **Network World**, January 23, 2007.
[16] *Op. cit.*, footnote 12.
[17] Deffree, S., "China IC industry hits $13B", **Electronics News**, March 23, 2007.
[18] Burton, C. S. and R. Beizaie. "EPA's PFC Emissions Model (PEVM) v.2.14: Description and Documentation", prepared for U. S. EPA, Washington, DC, November 2001.
[19] Burton, C. S. and Bartos, S. "Projecting PFC Emissions Using EPA's PEVM", presented at ISESH 2002, San Diego, CA. June 10-12, 2002.
[20] The total number of layers in an IC includes the silicon wafer base layer plus all the metal interconnect layers.

10^{-16} MMTCE/*MSI* and expresses aggregate FC emissions using 1995-1999 vintage manufacturing processes before adoption of FC-reduction measures.[19,20]

World Silicon Demand and TMLA

Before we can project TMLA, we must first project the portion of global FC-processed silicon demand to 2020 for each technology node.[21] We divide our estimates of silicon demand into two periods: 1995-2011 and 2012-2020. For the first period, we adapt data we obtain from VLSI Research, Inc. (VLSI) as will be described. For the second period, we then use the adapted VLSI data to guide projections of global FC-processed silicon demand.

Silicon Demand from 1995 to 2011

Worldwide silicon demand by linewidth interval[22], in units of MSI, is developed using data from VLSI.[23] VLSI tabulates actual silicon consumption through 2006 (most recent year available) and forecasts annual silicon demand to 2011, for linewidth intervals delineated in the ITRS. We include in our silicon demand totals only fully processed silicon.[24] For convenience but at the risk of some possible confusion, we refer to the silicon demand for the period 1995-2011 as "historical".

Silicon Demand from 2012 to 2020

Historical trends, provided by VLSI, guide and inform future year projections. We model historical VLSI silicon demand using two approaches, which we then average to arrive at our future demand projections. One approach used a linear growth model and resulted in a growth equivalent to a compound average growth rate (CAGR) of 4.9 percent over the period.[25] A second approach used an exponential growth model with a CAGR of 7.6 percent over the period.[26] The average of these two projections yielded an intermediate silicon demand CAGR of 6.3 percent.

Next, the projected silicon demand is disaggregated in accordance with VLSI-prescribed linewidth intervals.[27] The share of total worldwide demand attributed to each linewidth interval multiplied by the total silicon demand gives an estimate for silicon demand by linewidth interval. We project shares of linewidth intervals using a two-step approach. First we estimate shares of linewidth intervals after their 10^{th} year of production by 2012 (i.e., greater than 75nm linewidth intervals), and then we estimate the shares of linewidth intervals that have yet to reach their 10^{th} year of production by 2012 (i.e., less than 75nm linewidth intervals).[28] Analyses of historical VLSI data show that shares decrease at approximately 15.4 percent annually once linewidth technology reaches its 10^{th} year of production (R^2 =

[21] Silicon demand is assumed to equal silicon consumption and serves as a metric by which TMLA is estimated.
[22] The term linewidth interval refers to a range of linewidth technologies used in IC manufacture centered on each technology node.
[23] VLSI Research, Inc. at www.vlsiresearch.com at "Chip Making Markets" button.
[24] Between 10 - 20 percent of the total silicon demand is used for tracking process performance during IC fabrication (which we call test silicon). It is assumed that 95 percent of test silicon does not undergo full processing, and therefore does not contribute to FC emissions. Using VLSI provided data on annual test silicon demand, 95 percent of test silicon is subtracted from the silicon demand totals, which then reflect only fully processed silicon demand.
[25] A linear regression analysis was conducted on VLSI data between the years 2001 and 2011 (R^2 = 0.99), and was the basis for the linear growth projections of silicon demand.
[26] Exponential growth projections were conducted using the VLSI provided CAGR for years 2006 to 2011.
[27] Since our model used VLSI data, we adopted its convention to for linewidth intervals, where each linewidth intervals is centered on a technology node delineated in the ITRS 2006 Update. Smaller linewidths correspond to increasing IC complexity.
[28] Observations from historical data indicate that shares of each linewidth interval after their 10^{th} year of production decay at a constant rate, whereas, shares of each linewidth interval prior to their 10^{th} year of production follow a growth and decay trajectory.

0.93). By applying this reduction rate starting at year 2012, we project the share of each linewidth interval greater than 75 nm to 2020. The remaining share belongs to all linewidth intervals that are less than 75nm. We distribute this silicon into its constituent linewidth intervals by analogy to growth-decay profiles observed in the VLSI data for earlier linewidth technologies when they were at the leading edge of IC manufacture.[29] This method results in projected growth and decay trends for shares of less than 75nm linewidth intervals.

TMLA from 1995 to 2020

The TMLA from 1995 to 2020 for each linewidth interval are calculated by multiplying the average number of layers across all product types by the annual silicon demand in MSI for each linewidth interval.[30] Adding the TMLA across all linewidth intervals for a given year results in the annual TMLA.

China TMLA

Using the Worldwide annual TMLA estimates, China's TMLA estimates are derived for the following six years: 1995, 2000, 2005, 2010, 2015, and 2020. For 2010 and all preceding years, historical data was used. For years proceeding 2010, projections were estimated assuming three different China growth scenarios, which are explained below.

TMLA for 1995, 2000, 2005, and 2010

To estimate China's historical TMLA, world TMLA is attributed to China in the same proportion as China's share of world TMLA capacity.[31] Using TMLA capacity shares as a means of apportioning world TMLA to China, assumes the utilization rate of fabs in China equals the utilization rate of world fabs. The total TMLA and the TMLA by linewidth interval for China are thus estimated for 1995, 2000, 2005, and 2010.[32]

TMLA for 2015 and 2020

In order to project China's TMLA for 2015 and 2020 three growth scenarios are assumed: aggressive, intermediate, and conservative. For conservative growth, China's TMLA is assumed to grow at the same rate as the world projected TMLA growth rate of 9 percent annually; however, China's TMLA distribution among linewidth intervals remains five years behind the world's distribution.[33] For aggressive growth, China's TMLA is assumed to grow twice as fast as the world's at 18 percent annually

[29] Less than 75nm linewidth technologies are composed of the linewidth intervals: 55 – 75nm, 40 – 55nm, 25 – 40nm, 18 – 25nm, and <18nm. These correspond to the leading edge linewidth intervals post-2012, and are assumed to follow the same growth and decay trends observed in the leading edge linewidth intervals of today.

[30] To estimate the average number of layers by linewidth technology across various products types (i.e., memory, logic, discrete) the proportion of silicon demand used for each product type is determined from VLSI data. Then the International Technology Roadmap for Semiconductors (ITRS) is used to determine the number of layers by linewidth technology and product type, viz., logic, memory and discrete. By assuming the distribution of product type is constant between linewidth technology, the average number of layers for each linewidth interval is determined.

[31] TMLA capacity is derived using WFW data, from which silicon wafer capacity in MSI is converted into TMLA capacity in *MSI* by multiplying the silicon wafer capacity of each fab by the average number of layers produced per IC at each fab.

[32] TMLA capacity for China is derived using the Fabs on a Disk 1998 & 2001 and its successor World Fab Watch 2006 & 2007 databases, which includes capacity by country and linewidth technology for fabs worldwide. From this information, China's total TMLA capacity and capacity by linewidth interval is determined.

[33] Advanced technologies are associated with smaller linewidths, which currently are less prevalent in China than the rest of the world.

and China's TMLA distribution by linewidth interval is the same as the world's distribution by 2020. For intermediate growth China's TMLA is assumed to grow at one and a half times the world's, at 13.5 percent annually, and China's TMLA distribution among linewidth intervals is between the TMLA distribution assumed for the aggressive and conservative growth estimates (i.e. approximately 2 to 3 years behind the World's distribution). The assumptions for each growth scenario are summarized in Table 1, from which China's total TMLA and its TMLA by linewidth interval are projected for 2015 and 2020.

Table 1. China's Future Growth Scenarios

China Growth Scenario	TMLA Growth Rate (Multiple of World TMLA Growth Rate)	China's Technology Distribution Compared to World's at 2020
Conservative	9.0 percent/year (1)	5 years behind the World
Intermediate	13.5 percent/year (1.5)	2-3 years behind the World
Aggressive	18.0 percent/year (2)	Same as the World

Emission Reduction Estimates

WSC-Charter Member Reduction Goal

WSC-Charter member uncontrolled emissions are estimated by multiplying their share of world TMLA capacity by world uncontrolled emissions.[34] When accounting for the WSC-Charter member reduction goal, WSC-Charter member uncontrolled emissions are replaced with their aggregate controlled emissions, which is taken as 10 percent below their 1995 uncontrolled emissions.[35]

China Emission Reduction Scenarios

In addition to the already established WSC-Charter emission reduction goals, emission reduction scenarios for China are developed. The scenarios involve reducing China's 2020 emission by 10 percent below baseline year emissions, where the baseline year can be 2005, 2008, 2010, or 2012. These four alternative reduction goals are applied to the aggressive, intermediate, and conservative growth scenarios, resulting in a total of 12 reduction scenarios for China.

[34] WSC-Charter member TMLA capacity share is derived from the Fabs on a Disk 1998 & 2001 and World Fab Watch 2006 & 2007 databases. In projecting WSC-Charter member capacity from 2010, their TMLA capacity share is assumed to decrease at 0.5 percent/year, which is consistent with historical trends. Despite a reduction in TMLA capacity share, WSC-Charter members are projected to continue to grow their TMLA from 2010 to 2020. Additionally, WSC-Charter members have the opportunity to expand into non-WSC countries to further increase their growth.

[35] For simplicity this model assumes that all WSC-Charter members have adopted a baseline year of 1995. Recognizing that Korea and Taiwan have baseline years of 1997 and 1998 (average of 1997 and 1999), respectively, the effect of this assumption was examined. We determined that assuming a constant baseline 1995 year for all WSC-Charter members, resulted in WSC-Charter member controlled emissions in 2010 that was approximately 6 percent lower than when the actual baseline years for Korea and Taiwan were estimated and taken into account. This percent difference was considered inconsequential for our purposes; so a constant baseline year was assumed for all WSC-Charter members for the purposes of this model.

Results and Discussion

World Growth of Silicon Demand and TMLA

Global demand for electronic systems and a prosperous global economic environment drives long-term silicon consumption. Our projection period, which also matches the time horizon of the International Technology Roadmap for Semiconductors (ITRS), forecasts average growth in global silicon demand (and therefore average growth in global silicon consumption) to exceed the average growth in global gross domestic product (GDP).[36]

Growth in global silicon demand, expressed in MSI of silicon, also governs global growth in FC usage. However, growth in FC usage exceeds the growth in silicon demand due to increasing IC complexity, expressed as the number of manufactured layers. Therefore, as described earlier, *MSI* of TMLA rather than MSI of silicon governs FC usage and uncontrolled emissions.

Figure 1 shows growth in worldwide silicon demand, TMLA and estimates of the average number of layers manufactured over all product classes and linewidth technologies for the period 1995-2020. Growth in TMLA varies over the period and exceeds the growth in silicon demand 1.5- to 2-fold because of a monotonic increase in average number of layers per IC over time. The average annual increase in silicon demand is roughly 550 MSI while, on average, a new manufactured layer is added every five years. Between 1995 and 2010, TMLA has grown at 12 percent/year, whereas silicon demand has grown at 6.2 percent/year. Our model projects that between 2010 and 2020 TMLA will grow at 9 percent/year, whereas silicon demand will grow at 6.3 percent/year, somewhat less than twice the long-term average growth in GPD of 3.4 percent.[37] To achieve the projected growth over the 2010-2020 period, would require construction of approximately 150 new fabs and capital outlay of roughly $300 billion (2007 dollars).[38]

[36] "The McClean Report: A Complete Analysis and Forecast of the Integrated Circuit Industry", 9th Edition. IC Insights, Inc. Scottsdale, AZ.

[37] The decrease in projected TMLA growth compared to historical growth is due to the reduction in percent increase when adding layers to chips as the average number of layers per IC increases. Our estimate of number of layers relies on figures provided in the evolving ITRS for each technology node and accounts for greater complexity of logic devices compared to memory devices.

[38] Number and cost of new fabs required to meet increased demand between 2010 and 2020 is estimated using data from World Fab Watch, January 2007, from which we obtain the average capacity and cost of fabs by project type (foundry or IDM), product type (logic, memory and discrete) and wafer size (150, 200 and 300 mm wafers). The distribution of wafer size and product type in future years reflects recent trends (as evident in recent editions of WFW and industry reports) but does not include the currently debated future transition to 450 mm wafers and the very recent announcements of super-size memory fabs. In estimating the number of future fabs we assume an average fab utilization of 90 percent and historical average test wafer usage during IC manufacture.

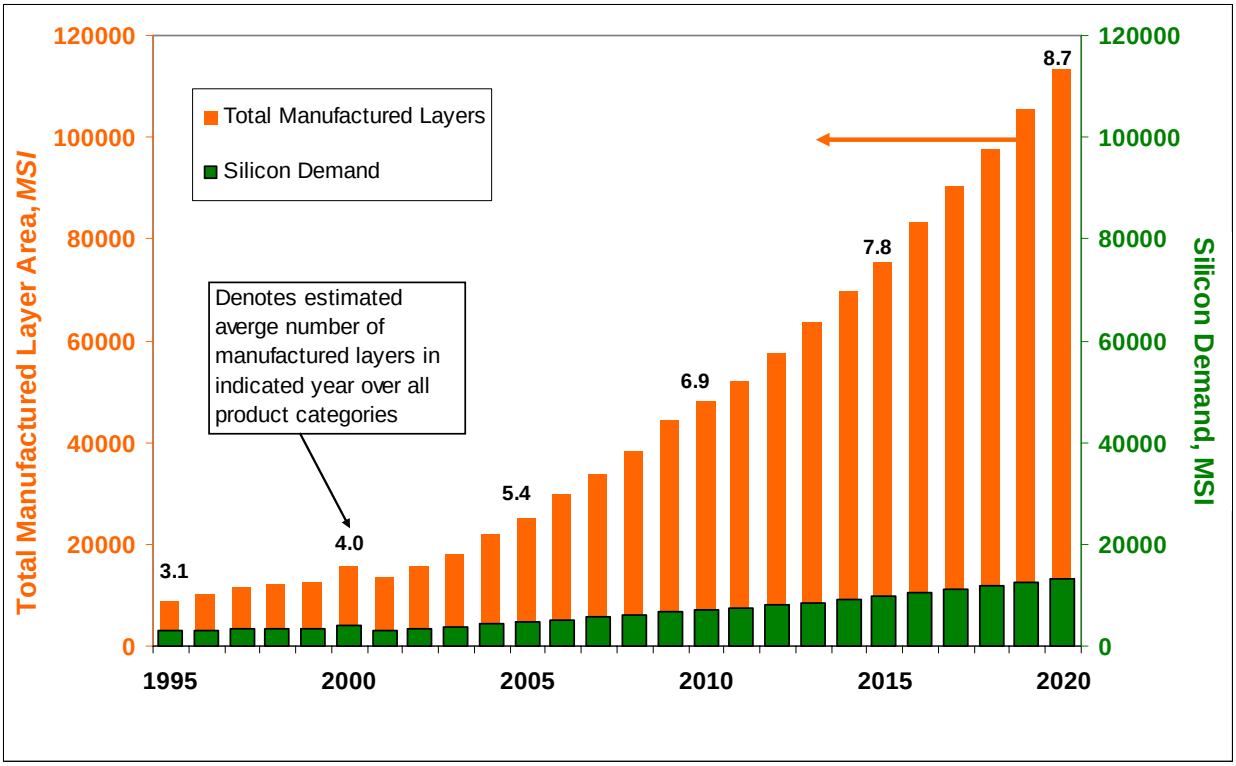

Figure 1. Worldwide Growth in Total Manufactured Layer Area and Silicon Demand in Million Square Inches

Figure 2 shows the composition of TMLA and uncontrolled emissions (right-hand axis) by linewidth interval over the period 1995-2020. The height of each column equals the corresponding height given in Figure 1. The stacked columns in Figure 2 reveal the growth and decay of each technological vintage—each linewidth interval as provided in previous and current updates to the International Technology Roadmap for Semiconductors (ITRS). The period to reach the maximum production for each linewidth interval is approximately 4 to 5 years.

As the demand for newer linewidth intervals increases moving towards 2020, so too does their contribution to uncontrolled FC emissions. By the year 2020, the ICs with less than 55nm linewidths are projected to account for close to 90 percent of TMLA and uncontrolled FC emissions.

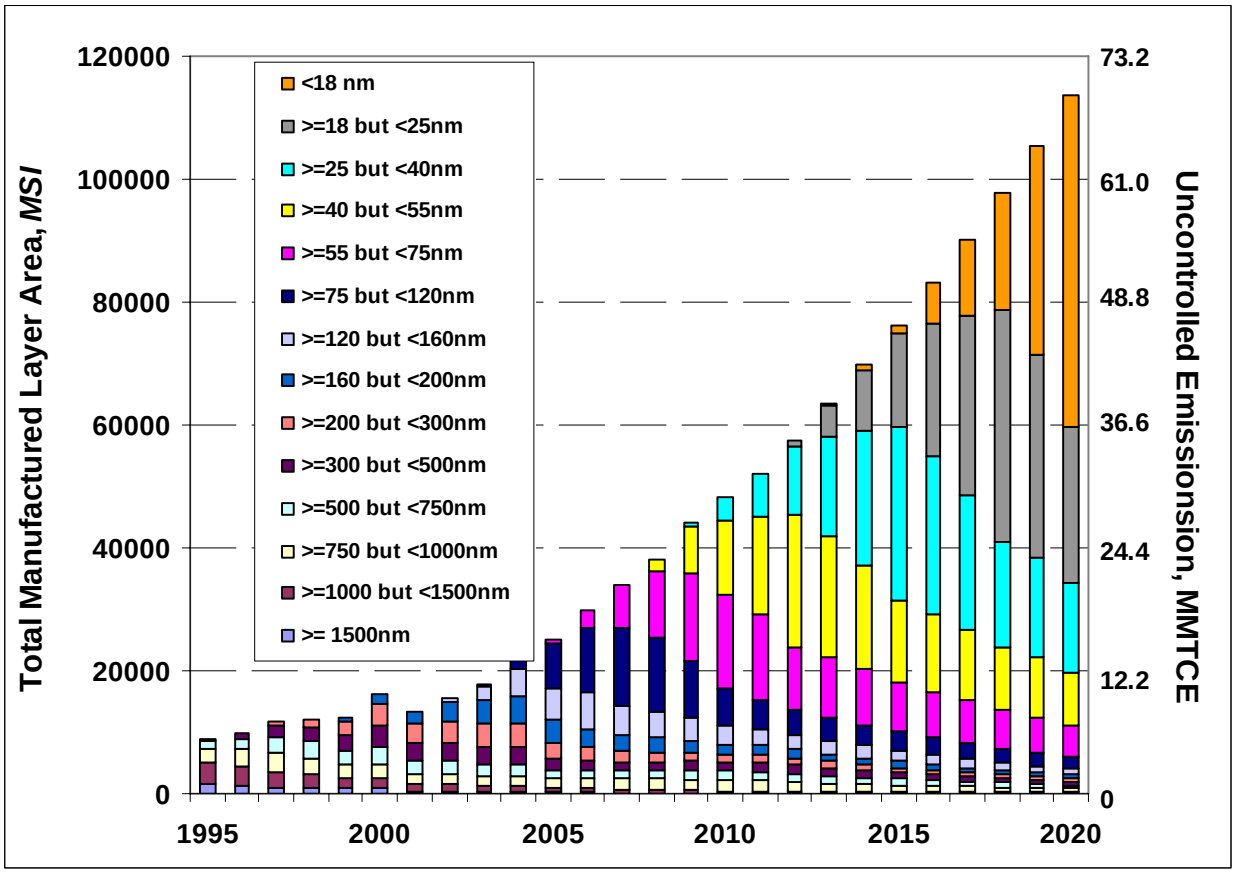

Figure 2. Worldwide Growth in Total Manufactured Layer Area and Uncontrolled Emissions by Linewidth Interval

Growth of China's TMLA

Figure 3 shows China's aggregate TMLA and uncontrolled emissions growth under three growth scenarios (i.e., conservative, aggressive, and intermediate). [39,40] Assuming conservative growth, China's TMLA is projected to grow at the same rate as the world and to account for 10 percent of the world's TMLA by 2020. In contrast, under the intermediate and aggressive growth assumptions, China's TMLA, by 2020, is projected to account for 15 and 22 percent of the world's TMLA, respectively, and to grow faster than the world. To put China's projected share of TMLA in perspective, each WSC-Charter region, by 2020, is projected in our model to account for approximately 15 percent of the World's TMLA, which is equivalent to the share China is expected to hold under the intermediate growth scenario. Under conservative growth China would have a less than average share of world TMLA compared to other WSC regions, while under aggressive growth China would have an above average share. China's uncontrolled emissions in 2020 are projected to be 6.8, 10.2, and 15.0 MMTCE for the conservative, intermediate, and aggressive growth scenarios, respectively, and are discussed in more detail in the following section.

[39] See Data and Methods section, Table 1, for list of growth assumptions for each scenario.
[40] Only under the aggressive growth scenario, does China continue to grow at a rate similar to that observed historically. From 2005 to 2010 China's TMLA growth was 23 percent/year, whereas, under the aggressive growth scenario China's projected TMLA growth rate is 18 percent/year. Under both the conservative and intermediate growth scenarios, China's growth rate is estimated to decrease with respect to its historical growth.

A large part of China's growth currently follows the foundry business model at the expense of growth among integrated device manufacturers (IDMs).[41] However, whether China's future growth occurs in one or the other type of fab does not affect our projections of TMLA or emissions, which are independent of the fab business model.

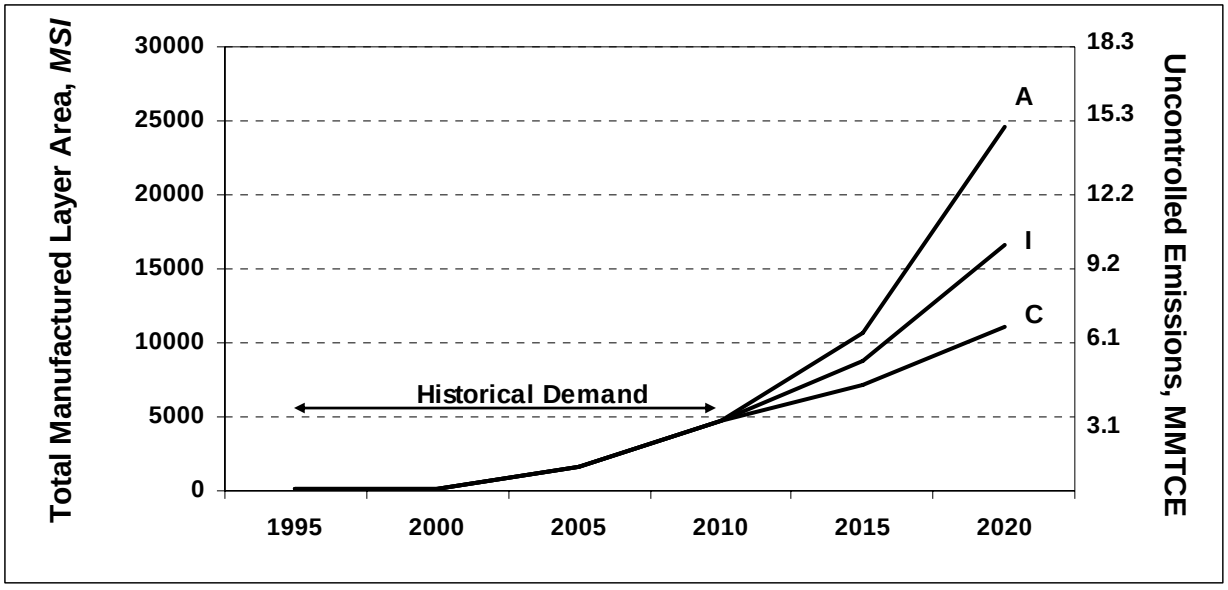

Figure 3. Growth of Total Manufactured Layer Area and Uncontrolled Emissions in China (C = Conservative, I=Intermediate, and A=Aggressive Growth)

Historically, China has lagged behind the world in leading-edge manufacturing technology (see Figure 4). However, in recent years China has been closing this difference. In 1995, according to previous editions of WFW, Chinese semiconductor manufacturers were three linewidth technology nodes behind the world; however, by 2010 Chinese manufacturers are projected to be just one technology node behind the world according to planned and announced fabs scheduled for 2010.[42] As demand within China for leading edge technologies increases towards 2020, it may be that China's production of leading edge technologies will follow suit due to the financial incentives of producing and selling within China. Alternatively, contrary to recent trends, governments of nations with leading edge technologies might be more effective in restricting the transfer of leading edge technologies to China.

If China remains behind the world in leading edge technology production (i.e., assuming conservative growth), approximately 80 percent of China's production capacity is projected to be concentrated in the less than 55nm linewidth intervals by 2020. When assuming aggressive growth, approximately 90 percent of China's production capacity is projected to be in the less 55nm linewidth intervals by 2020 (see Figure 5 for technology distributions under different assumptions). These technology distributions are important when considering which emission reduction options will become available to China, as discussed further in the next section.

[41] Traditionally, IC manufacturing has pursued a vertically integrated business model; however, Taiwan's and now China's industry, among others, is largely based on the Foundry business model, which provide manufacturing services to IDMs and fabless companies.
[42] World Fab Watch. April, 2007 Edition.

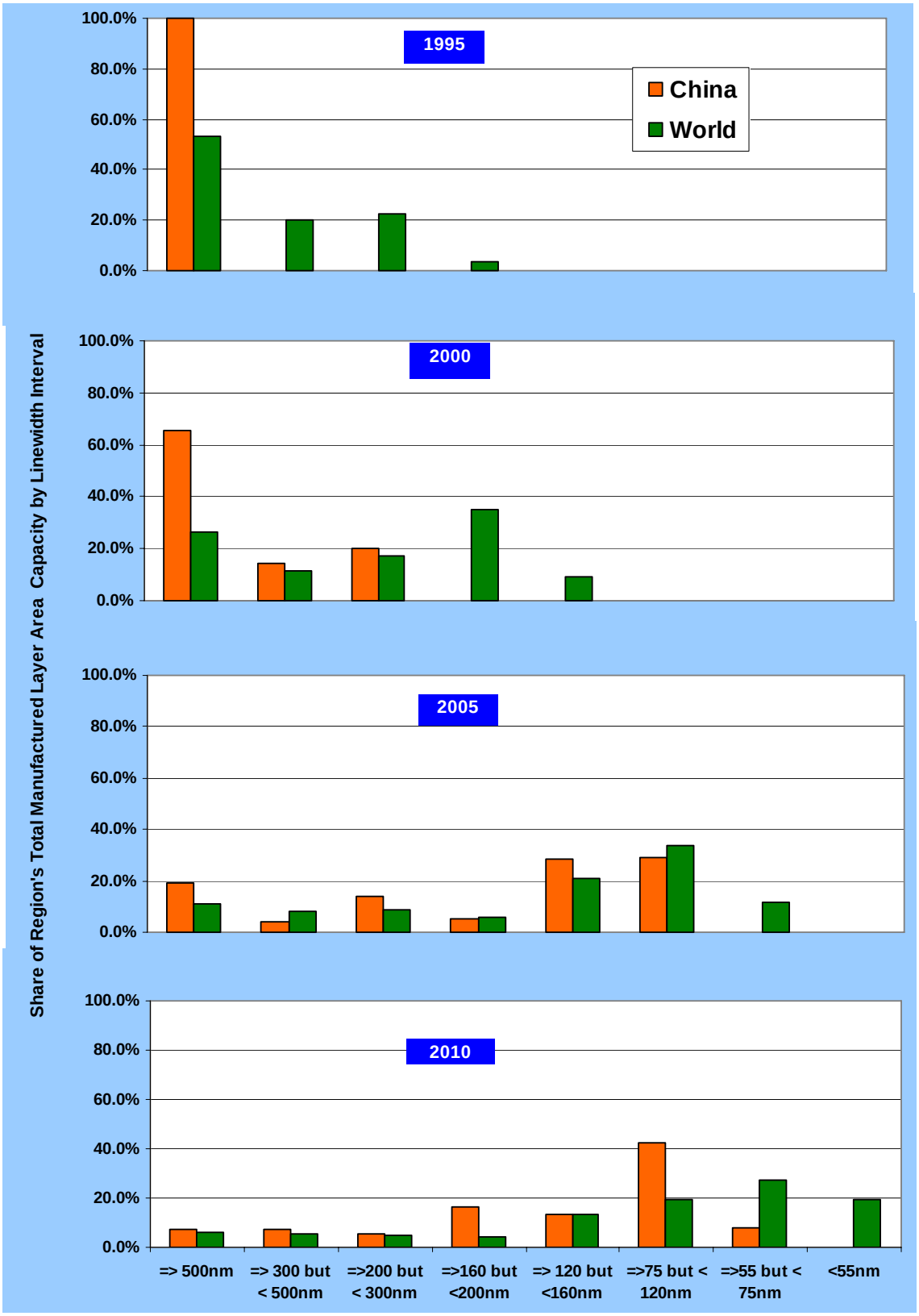

Figure 4. Historical Distribution of Total Manufactured Layer Area Capacity by Linewidth Interval

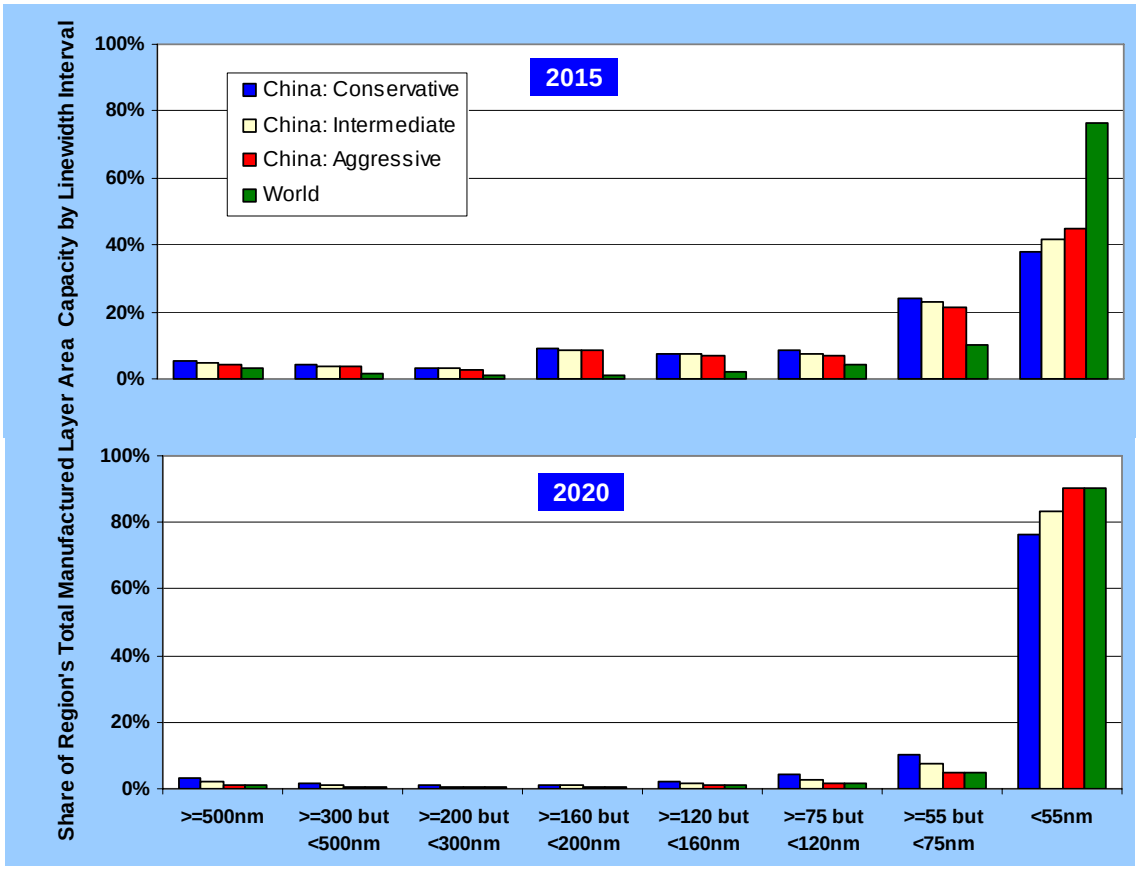

Figure 5. Projected Distribution of Total Manufactured Layer Area Capacity by Linewidth Interval

China's Fluorinated Compound Emissions

WSC-Charter members have agreed to hold their FC emissions at levels equal to 90 percent of their 1995 emissions after 2010.[2,35] By analogy with WSC-Charter members, the SIAC could choose a baseline year and an emission reduction target 10 percent below baseline emissions by some future year. Table 2 presents the controlled and uncontrolled emissions for China, for various baseline years, assuming that SIAC members reduce emissions to 10 percent below their baseline emissions by 2020. Shown for purposes of comparison are the controlled and uncontrolled emissions of the WSC-Charter members and the rest of the world (ROW).

Table 2. Projected Controlled and Uncontrolled Emissions in 2020

Growth Scenario	Baseline Year for Emission Reduction Scenario	Uncontrolled Emissions in Baseline Year (MMTCE)	China 2020 Controlled Emissions, MMTCE (Uncontrolled, Emissions, MMTCE)	WSC-Charter 2020 Controlled Emissions, MMTCE (Uncontrolled Emissions, MMTCE)	Rest of World 2020 Uncontrolled Emissions, MMTCE
Conservative	2005	1.0	0.9 (6.8)	4.3 (48.3)	14.4
	2008	2.1	1.6 (6.8)		
	2010	2.9	2.6 (6.8)		
	2012	3.7	3.3 (6.8)		
Intermediate	2005	1.0	0.9 (10.2)	4.3 (48.3)	11.0
	2008	2.1	1.6 (10.2)		
	2010	2.9	2.6 (10.2)		
	2012	4.3	3.9 (10.2)		
Aggressive	2005	1.0	0.9 (15.0)	4.3 (48.3)	6.2
	2008	2.1	1.6 (15.0)		
	2010	2.9	2.6 (15.0)		
	2012	5.3	4.8 (15.0)		

MMTCE = Million Metric Tons of Carbon Equivalent

Uncontrolled world emissions total 69.5 MMTCE at 2020 for each scenario. SIAC member uncontrolled emissions are 6.8, 10.2 and 15.0 MMTCE at 2020 for the conservative, intermediate and aggressive growth scenarios, respectively. SIAC member emissions targets vary for each growth and baseline year reduction scenario combination (2005, 2008, 2010 and 2012). WSC-Charter members, on average, appear on track to achieve their emission reduction targets by 2010. Thus, in absence of emission reductions by SIAC, SIAC members and the ROW manufacturers will contribute to the majority of semiconductor FC emissions by 2020. For example, for the intermediate growth scenario, uncontrolled emissions from SIAC members and ROW manufacturers are projected to exceed WSC-Charter member controlled emissions by almost 5-fold. It is also interesting to compare the reduction targets of SIAC members with the target of the average WSC-Charter member, 0.86 MMTCE (=4.3/5). Were SIAC members to adopt a 2005 baseline year and to cap their emissions at 90 percent of their baseline emissions by 2020 (roughly the same period WSC-Charter members afforded themselves to achieve their reductions), SIAC member emissions would be 0.9 MMTCE (essentially identical to the 0.86 MMTCE figure for the average WSC-Charter member). Figure 6 presents emissions under the intermediate growth scenario and an SIAC-reduction goal using the 2005 baseline: depicted in the figure are Uncontrolled, WSC-Charter controlled/China uncontrolled and WSC-Charter controlled/China controlled emissions. If both China and the WSC-Charter members control their emissions as depicted in Figure 6, emissions from ROW manufacturers would exceed all WSC-member emissions (SIAC and WSC-Charter members) by more than 2-fold.

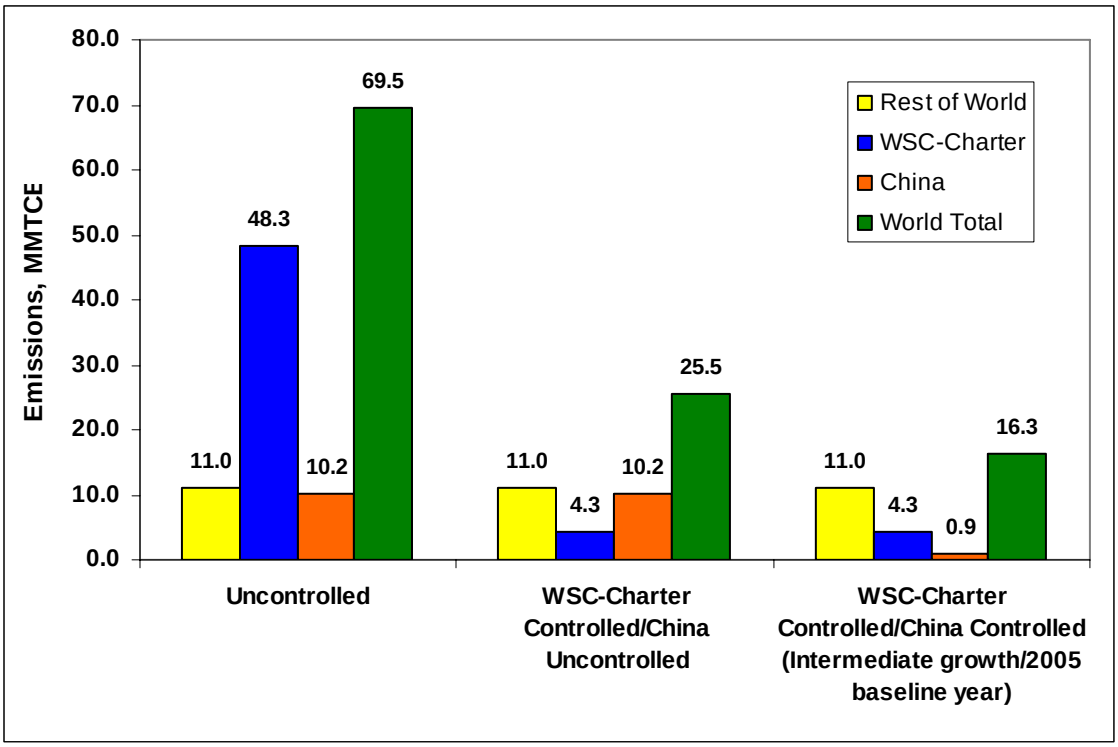

Figure 6. Projected Emissions in 2020 for Three Future Emission Scenarios (Totals may not sum due to rounding)

Potential Mitigation Opportunities in China

The implied emission reductions from projected 2020 uncontrolled emissions for each target range from roughly 50 to 95 percent, depending on the growth scenario and reduction goal (Table 3). This range is comparable to but somewhat broader than the implied reductions accepted by WSC-Charter members, which also varies among members, depending on growth of member regions beyond their baseline emissions. Because those members appear, according to WSC reports[43], on track to achieve their reduction targets it is reasonable to expect that the reduction measures available to WSC-Charter members would also be available to SIAC members, especially in view of China's push for technological parity. Even when assuming conservative growth, less than 120nm linewidths will account for 90 percent of China's MSI layer production capacity by 2020.[44] Therefore, it matters not whether China remains behind the world in leading edge technology or catches up: SIAC members are likely have access to the technology to reduce FC emissions using at least the options compatible with the advanced fabs of today.

Today's advanced fabs can accommodate a variety of emission reduction technologies including CVD chemistry substitution, remote NF_3 CVD cleaning, and abatement, as compared to older, smaller sized fabs, which are limited, for the most part, in their emission reduction options to process optimization and limited CVD chemistry substitution.[45] Currently available emission reduction options can reduce

[43] See May 2007 Joint Statement of the 9th Meeting of the World Semiconductor Council held in San Francisco, CA.
[44] See Figure 5. Projected Distribution of TMLA Capacity by Linewidth Interval for China and the World.
[45] Beu, Laurie, S. "Reductions in Perfluorocompound (PFC) Emissions: 2005 State-of-the-Technology Report." International SEMATECH Manufacturing Initiative. December, 2 2005.

uncontrolled emissions by greater than 95 percent.[46,47] Additionally, the cost-effectiveness of reducing FC emissions decidedly improved at the 180 nm technology node, when NF_3 Remote Clean and other new CVD chamber cleaning technologies were incorporated into the designs of semiconductor process equipment.[48]

Table 4 illustrates various emission reduction strategies that are compatible with today's production fabs—post-2000 vintage 200- and 300-mm wafer fabs.[49] FC emission reduction can be achieved in a variety of reduction technologies, with the cost-effectiveness of each and therefore the attainment strategy governed by company-specific circumstances. Although, it is beyond the scope of this paper to analyze the cost-effectiveness of emission reduction strategies, the emission reduction strategies presented in this paper are meant to initiate further discussion of the mitigation opportunities available to China in light of the reduction targets presented in Table 3.[50]

Table 3. China's Emission Reduction Targets Under Different Growth and Emission Reduction Scenarios

China Growth Scenario	2020 Uncontrolled Emissions (MMTCE)	Baseline Year for Emission Reduction Scenario	2020 Controlled Emissions (MMTCE)	Percent Reduction by 2020
Conservative	6.9	2005	0.9	86
		2008	1.6	72
		2010	2.6	62
		2012	3.3	52
Intermediate	10.2	2005	0.9	91
		2008	1.6	81
		2010	2.6	75
		2012	3.9	62
Aggressive	15.0	2005	0.9	94
		2008	1.6	87
		2010	2.6	83
		2012	4.8	68

Table 4. Emission Reduction Technologies

Emission Reduction Technology	Applicable Process	Percent Reduction over Baseline Emissions
Process Optimization	Typically CVD	10 – 56
Remote Plasma Clean	CVD	>15 – 99 (NF_3); >35 (C_3F_8)
Alternative Chemistry	CVD	10 – 90 (depending on particular chemical substitute)
Abatement	Etch, CVD	90 – >99

[a] Adapted from Beu (2005). For a more detailed listing of emission reduction technologies and their associated costs please see: Beu, Laurie, S. "Reductions in Perfluorocompound (PFC) Emissions: 2005 State-of-the-Technology Report." International SEMATECH Manufacturing Initiative. December, 2 2005

[46] *Op. cit.*, footnote 45.
[47] Raoux, S. "Implementing PFC Emission Reduction Technologies", **Solid State Technology,** January 2007.
[48] *Op cit*. footnote 45.
[49] It is outside the scope of this paper to consider cost-optimized strategies to achieve alternative reduction targets. Instead, we reason that in the globally competitive semiconductor industry what works for one fab will also work at technologically comparable fabs.
[50] For additional information, see Global Mitigation of Non-CO_2 Greenhouse Gases, U.S. EPA, June 2006. www.epa.gov/nonco2/econ-inv/downloads/GlobalMitigationFullReport.pdf.

Conclusions

China's increasing share of world leading-edge manufacturing capacity will lead to corresponding increases in its share of world FC emissions during semiconductor manufacture. Under our conservative, intermediate or aggressive manufacturing growth scenario, SIAC-member FC emissions, absent of an emission reduction target, are expected to exceed the combined controlled emissions of their WSC peers by 2020. Under our aggressive growth scenario, which is consistent with China's current and latest (11th) 5-year development plan and manufacturing growth profile, China's FC emissions without control would exceed the combined controlled emissions of its WSC peers and uncontrolled emissions from the ROW (which are not WSC-members).

SIAC's WSC membership alone suggests it join WSC-Charter members and establish an emission reduction target.[51] SIAC's manufacturing ambitions would support this course of action. We considered reduction targets of SIAC that are comparable in form and stringency to targets adopted in 2000 by WSC-Charter members. The implied FC reductions for each alternative reduction goal relative to a 2020 attainment year depend on growth scenario and baseline year. However, taken together the results are comparable to the voluntary reductions to which WSC-Charter members are publicly obligated. Further, the implied reductions appear achievable in light of the availability of proven FC-reduction measures that WSC-Charter members are currently adopting. Of course, what specific goal SIAC adopts is a matter for its members and for WSC to decide, as is when and how SAIC should report its emissions and what measures it adopts to achieve its reduction goal. If China does adopt a 2005 baseline year and follows WSC-Charter members by agreeing to reduce SIAC-member emissions to 10 percent below baseline emissions by 2020, SIAC member emissions in 2020 would equal emissions (0.9 MMTCE) for an average WSC member.

Our analysis is based on a range of assumptions and associated uncertainties and the limitations of our methods and results. Table 5 presents the most important assumptions. While it is outside the scope of this paper to discuss them, consideration of the entries reveals that our methods do not include known biases, albeit we cannot rule out the presence of some. By far, however, the largest uncertainty we must acknowledge is not knowing the future.

[51] As this paper was being finalized the WSC released its May 24, 2007 Joint Statement of the 11th Meeting of the World Semiconductor Council held in Geneva, Switzerland in which this, among other things, was said: "the Semiconductor Industry Association in China is currently determining the baseline and when it will be feasible to join the emissions reduction programme."

Table 5. China Semiconductor Fluorinated Compound Emissions Model: Assumptions and Uncertainties

Assumptions Used in China Model Category	Nature of assumption	Impact on result (+, -, ?, NC)	Comment
PEVM Framework	Q(uncontrolled) = e * (MSI-layers) for all years	+/-	Emission factor e reflects uncontrolled emissions and has units of MMTCE per average layers per MSI of silicon consumed during IC fabrication
MSI growth in silicon demand	6.3% CAGR 2010-2020	+/-	Approximately equals 2 times world GDP growth rate and equals VLSI Inc. Si-demand forecast through 2011
Distribution of product demand	Distribution held constant after 2010	+/-	If proportion of memory ICs increases relative to logic, as some evidence suggests, projected emissions would be overstated, provided all other variables remain unchanged
Country/region shares directly proportional to capacity (MSI)	Shares of world emissions directly proportional to shares of capacity	+/-	Valid provided country/region fab utilizations are close to corresponding global average utilization
FCs not used in fabrication of devices made of compound semiconductors	FCs assumed not used during fabrication of compound semiconductor devices	-	Other non-FC materials are better etchants than FCs. However, if FCs are used in compound semiconductor fabrication, FC emissions are understated
VLSI data	Reliably accounts for actual silicon consumption expressed in terms of wafer starts per week, test wafers used and proportions of silicon consumed during fabrication of logic, memory and discrete devices	+/-	A long-standing source of information for industry and its analysts. The only source that provides silicon demand by linewidth technology. Makes continuous improvements in data collection and treatment.
PEVM treatment of VLSI data	1. Method for distributing silicon demand by wafer size to silicon demand by linewidth technology. 2. 5% of test wafers fully exposed to FC-processing	+/-	1. Distribution errors cancel when summed over all linewidth technologies for any year, but distribution errors of unknown sign and magnitude likely exist for each node. 2. 5% figure may be high or low; same figure used in forming emission factor so any multiplicative errors should cancel when estimating emissions.
WFW databases	Missing entries, lags in entries and use of fully-ramped design capacities	+/-	Missing or lags in entries for geometry
Treatment of foundries	Foundries assumed to manufacturing both logic and	+/-	Affects number of layers and FC usage. Industry analysts use 75:25 proportion when estimating

Assumptions Used in China Model Category	Nature of assumption	Impact on result (+, -, ?, NC)	Comment
	memory devices in 75:25 mix		Industry tool-sets needed to equip foundries
International Technology Roadmap for Semiconductors (ITRS)	For any technology node, fabs employ number of metal layers specified in ITRS	+	While some evidence suggests that some manufacturers may exceed the number of metal layers, it appears more often than not that manufactures fabricate the maximum number of metal layers or less.
China's distribution of linewidth technology	Lags world distribution prior to but catches up with world average by 2020 (Aggressive Scenario)	+/-	If China catches up sooner than 2020, emissions would be understated. If China doesn't catch up by 2020, projected emissions would be overstated
Fabs located in regions not part of WSC	Fabs solely or partially owned by companies with HQ in WSC-member regions treated as uncontrolled	+	Fabs owned solely or partially by firms with HQs in WSC-member regions may be implementing FC-reduction measures, but model assumes such measures are not in use