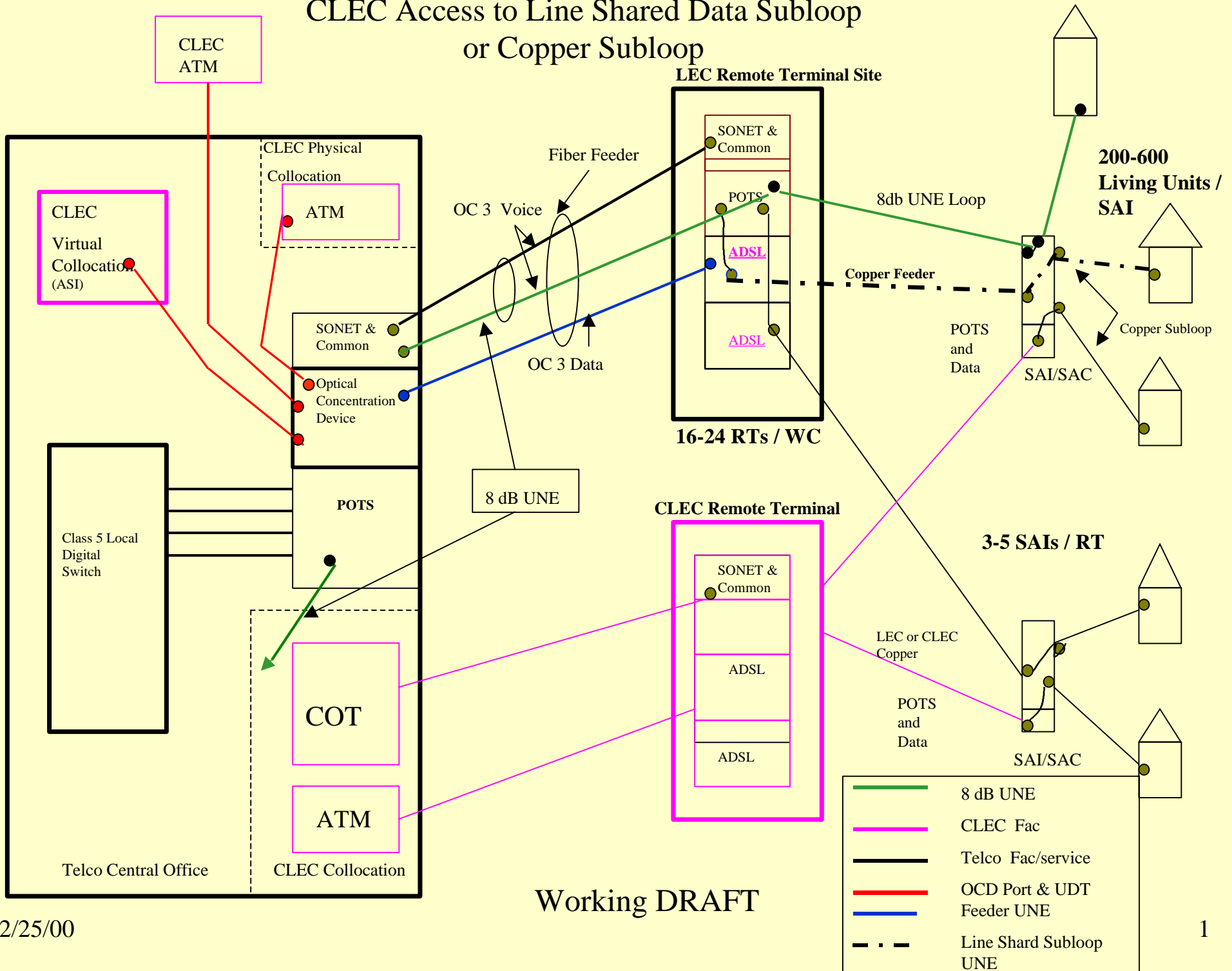


# CLEC Access to Line Shared Data Subloop or Copper Subloop



Working DRAFT