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Speech Processors for Auditory Prostheses

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submitted by

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1.0 Introduction

Work performed with the support of this contract is directed at the design, development, and evaluation of speech processors for use with auditory prostheses implanted in deaf humans. Major research efforts are proceeding in four areas: (1) developing and maintaining a laboratory based, software controlled, real time, speech processing facility where processor/stimulator algorithms for monaural and binaural eight-channel implants can be implemented/tested and a wide range of psychophysical measurements can be made, (2) using the laboratory facility to refine the sound processing algorithms used in the current commercial and laboratory processors, (3) using the laboratory facility to explore new sound processing algorithms for implanted subjects, and (4) designing and fabricating programmable, wearable speech processors/stimulators and using these systems to: (a) field test processor algorithms developed and tested in the laboratory, (b) evaluate the effects of learning using longitudinal evaluations of speech reception, and (c) compare asymptotic performance of different speech processors across subjects.

This QPR reports on progress associated with several ongoing hardware and software projects. In particular we report progress in the design of an upgrade to the wearable processor presently used by twenty of our Ineraid subjects. We also describe our ongoing work in designing and building a computer-controlled, high-rate stimulation system (HRSS) for both psychophysical and speech processing experiments. Finally we describe a new effort that will increase the range and precision of our control of Clarion implant systems. This will be especially important as we move forward with our experiments in bilateral stimulation of subjects implanted with an Ineraid system in one ear and a Clarion system in the other.

2.0 Wearable Processor Design

During this quarter, work continued on the design of new analog I/O circuits used with the Geneva Wearable Processor (GWP). The primary goal of this is to replace the single, switched current source capability in the present GWP. While a single switched current source arrangement is adequate for Continuous Interleaved Sampling (CIS) processors that stimulate a single electrode pair at any one time, it precludes implementing schemes that require simultaneous stimulation. The new design allows all six outputs of the processor to be active simultaneously; a feature that is necessary for implementing a larger range of sound processing schemes. At the same time the output circuits are undergoing redesign, we have also taken the opportunity to update and improve the analog input circuits. This will mean an I/O design that is more flexible and uses the lowest power technology.

New Analog Input Circuit Design

The present GWP analog input circuits that provide a digitized speech sample to the digital signal processing chip (DSP) use an A/D converter design (Burr Brown – ADS7807) that requires an external filter before the A/D stage to prevent aliasing. This external filter is set to eliminate frequencies above 6800 Hz in the present system. If a higher sampling rate than is presently used by the DSP (approximately 16 kHz) is desired to process a wider spectrum of analog signals, the cut-off frequency of the present filter would need to be increased. In the redesigned circuit, a new A/D converter part is used (Analog Devices-AD73311) that provides internal, flexible anti-aliasing filtering so that sampling frequencies and spectrum cut-off frequencies are linked as the sampling frequency is changed under program control. Besides the flexibility, such an arrangement also eliminates the space and power required by the antialiasing filter. Additionally, this new part provides several on-chip clock dividers that eliminate the need for several digital circuits used by the GWP. Taken together, this new design (shown in Figure 1) will provide more flexibility, be more space and power efficient, and extend the reliability of the overall system.

Simultaneous, Multichannel Output Circuit Design

Together with Draper Laboratory, we are designing and testing new circuits for the wearable processor that will form a six-channel, current-source output stage. This new design will allow simultaneous stimulation on up to six electrodes, which will make possible the implementation of speech processing strategies not possible with the GWP single current-source design. These strategies include continuous analog schemes, as well as hybrids of CA and CIS processors. This design effort was described in a previous report [Eddington, 1996 #93] where the new current source design was explained and the overall packaging and layout of the output circuits were described in some detail. The use of multi-chip-modules (MCMs) as an implementation technique was necessary to increase the number of outputs by six within the same physical space. While the overall design philosophy described in that earlier report has not changed, the circuit has undergone several design changes as our understanding of the required specifications have matured and as a consequence of defects discovered when testing prototype circuits.

In order to determine the maximum currents that the newly designed current sources would be required to provide for high-rate pulsatile stimulation, psychophysical testing was done on subjects using the very narrow pulses that will be available using the new, faster current source. Narrower pulse widths require higher currents to obtain the same subjective loudness perception that is obtained at present update rates (2 kHz with phase durations of approximately 30 μs). Conducting psychophysical tests with the Ineraid subject in our group who requires the highest currents to reach a comfortable listening level, we estimated that a minimum of 18 mA (pp) will be required for processors producing 40 kHz/channel stimulus trains (2 μs/phase). This is a factor of 6 greater than the present prototype design allows. Consequently the circuit is now being revised to allow for this higher current requirement.

While narrow stimulation pulses require very high current levels, the low-frequency stimulation required by CA processors (e.g. bandwidths of 100-400 Hz), require much lower current levels; on the order of 20 uApp to achieve comfortable loudness levels. This wide range of current output level poses a resolution problem since our present output circuit design uses 12 bit D/A converters. This means that if the maximum current output is set to 18 mApp, then the smallest current step available from a 12 bit output will be around 4 uApp. This level of current resolution will be inadequate for low-level CA stimulation. We are, therefore, adding the capability to independently program the gain of each current source. This will allow each channel to be adjusted for an appropriate maximum output level and resolution.

Prototype testing also revealed large transient signals at the electrode outputs during power on and power down. As power supplies rise or fall, integrated circuits can operate very differently than from their normal powered up mode, and their behavior is generally not specified by the manufacturer. Our circuit seemed to be especially affected by the non-symmetrical rise of the positive and negative supplies. The present wearable processor (GWP) addresses this problem by placing solid state switches between the electrodes and the output circuit. These switches remain open during power up or down and thus isolate the electrodes from the transients which do exist at the current source output. The switches are also then used to perform the multiplexing operation of connecting the single current source to multiple electrodes. On the new design however, multiplexing is not required, so the switches would need to be added and would require extra space and power. More importantly, the switches would add output capacitance to each electrode, which will act to limit the speed of the new circuit and work against our goal of producing a substantially faster current waveform.

A new technique has been implemented which will use a series of MOSFET transistors placed on the current source power supplies. These transistors hold the power supplies low until all the current source control circuits have stabilized, and then under control of the microprocessor, raise the supplies slowly and symmetrically. The MOSFETs are also under control of the power fail detection circuits which quickly zero the current source supplies early in the fall of the power supply output. This circuit conserves space when compared to switches, as only one set per processor, and not per channel, is required. The circuit has been tested and almost completely eliminated the power transients, although some low level transients still exist. The remaining output current transients are just above threshold for our subjects tested and therefore would probably be tolerated. However, we are making efforts to refine the circuit further so that all transients are below perceptual thresholds.

Although the circuit changes to make these modifications are straightforward, implementing them is complicated by the extreme space limitations of the circuit. The circuit is eventually to be manufactured as a MCM (hybrid) module, and therefore any change must not consume more space than will fit on the module.

3.0 Current Wearable Processor Support

The 20 subjects currently wearing the GWP have had ongoing problems with the cable that connects the sound processor to the earhook. This cable fails at the sound processor end where the cable is flexed the most severely. Average cable life has been approximately four months.

In this quarter, a new contract was signed with Precision Interconnect to redesign the strain relief at this failure point and to supply us with a new lot of cables. The Engineering collaboration between PI and MEEI has begun and we expect that the design will be completed early in the next quarter, prototype units should be available late in that quarter, and the completed batch of new cables will arrive in the middle of the third quarter.

4.0 Laboratory Processing System – High Rate Stimulation

Since the beginning of the present speech processors contract we have been upgrading our laboratory processing system so as to perform each of the research tasks required under the contract. Still in progress, at this time, is our DSP-based high rate stimulation system (HRSS) as shown in the upper right hand corner of Figure 2. The box labeled "percutaneous output" represents the segment of our laboratory sound processing system with the present capability of dual, eight-channel, 16-bit, D/A outputs that are used to drive percutaneously connected electrodes (through isolated current source circuits not shown). The system we have designed and are currently building is represented by the other two boxes of the "percutaneous output" system (arbitrary waveform generator and V/I converter). The DSP-based arbitrary waveform generator is controlled by a program that is downloaded from the SUN workstation and is able to produce arbitrary waveform samples with a 2 μs sample interval. The generated waveforms can be amplitude (or time-shift) modulated in real-time by inputs from the dual floating-point DSP system. The arbitrary waveform generator off-loads the modulation task from the floating-point DSP system and allows for the higher update rates as well as freeing floating-point processing power to be available for more complex speech processor implementations.

Figure 3 presents a detailed view of the new system. As shown, each channel includes a Motorola DSP 56002 running a program that is downloaded from the SUN workstation. This program then accepts real-time inputs from the floating-point Texas Instruments TMS320C30-based laboratory DSP system. The serial, digital data stream from each channel's 56002 that represent the 2 μs waveform samples are optically isolated before being connected to the input of a 16-bit, 2 us D/A converter. At the present time we have completed the design, fabrication, and debugging of the DSP portion of the HRSS which is implemented on a small, 3"x4" printed circuit board. These modules are in hand and available for integration with the module containing the remaining circuits of

Figure 3.

Isolated D/A and V/I Converter Module

Progress continues towards completion of the isolated D/A and V/I module of the laboratory stimulation system. The opto-isolator circuits and D/A converter (Burr-Brown PCM56) have been integrated and debugged, and a new current source designed by the Draper Laboratory has been debugged and modified. This new current source circuit trades off additional power dissipation (not a critical concern in the laboratory setting) to make a simpler and less expensive circuit than the one used for the new wearable processor design. It also contains a shield driver circuit that provides a "guard" function for the active electrode. Driving the shield 'guards" against signal loss due to the capacitance of the long cable used to connect subjects to our laboratory test system. The isolated D/A and V/I module has been sent to contractors for layout and manufacturing of a printed circuit board (PCB). A PCB was used in this system as opposed to the bread-board units used in previous systems because the newer system will operate at very fast pulsatile rates, high bandwidths, and high feedback gains, all of which require precise control of layout and grounding of the circuit to minimize the effects of parasitic elements and cross coupling. Most of the layout of this new board has been completed and we expect the module to be available for testing in the middle of the next quarter.

Software Development for the HRSS

Substantial progress has been made in the software required to control the new laboratory system. The new system replaces a hardware state-machine based sequencer with a bank of Motorola 56002 DSP processors. While the hardware sequencer was very fast, the new DSP software-based approach will allow for more flexibility in production of stimulation signals. All software was completed that allows the new system to perform its first intended task: psychophysical testing using waveforms of arbitrary shape (e.g., charge balanced tri-phasic pulses). The software written includes a module that allows experimenters to specify waveform shapes in a simple text file format as shown in Figure 3. The module converts the text file to a 56002 compatible binary format, and then downloads this data to one of the 56002 processors. The 56002 assembly language software that accepts the modulating signal from the floating-point C30 DSP, modulates the waveform defined by the text file and outputs modulated waveform, is also completed. This software frees the C30 DSP from the modulation task and allows it to concentrate on producing multichannel, real-time processor envelopes, each of which is used to amplitude modulate the arbitrary waveform set up in each channel of the HRSS. Each 56002 can also be programmed to "pass through" to the isolated current sources waveform samples from processors implemented in the floating-point, C30 DSP system. This "pass through" capability allows direct waveform outputs (albeit sampled) to the isolated V/I circuits as well as modulated pulsatile outputs. This means that a variety of hybrid processors can be implemented where some C30 DSP channels produce waveforms that are “passed through” to the V/I circuits and others are used to modulate the arbitrary stimulation waveforms specified for other channels of the HRSS.

Software development will be an ongoing effort as new research goes forward, indeed this is a feature of the new DSP-based approach. However the software completed is an important milestone in the completion of this new system.

5.0 Clarion RSP – Laboratory and wearable based control of a transcutaneous implant device

Work has began towards gaining control of the production of stimuli using the implanted current stimulators manufactured by Advanced Bionics.This long term project is necessary as we develop the need to better coordinate those stimuli with stimuli we deliver from our percutaneous system to Ineraid implants. While our present system enables us to test some new sound processing systems and do monolateral and some bilateral psychophysical testing, we still are not able to control bilateral stimuli with resolutions of less than 1 μs.

We received hardware, documentation and source code, developed at Advanced Bionics and at the House Ear Institute, that will, with some modifications and additions, provide the control we will require for experiments we plan to conduct in the next six months. Instead of performing a speech processing strategy, the Clarion sound processor will accept commands from an external serial port, translate them, and essentially pass them to the implanted receiver-stimulator device. These commands will allow complete control of the implant, including electrode configuration and stimulation current output for all 8 channels, at the full 76.9 us update rate. The investigator will be able to feed commands to the speech processor's serial port from a DSP processor, which in our case will be one of our laboratory system's TMS320C30s. The received source code has been shared with our engineering partners at Draper Laboratory, who will assist us in development of a software library for the C30 that will allow investigators to have high level access to the implant functions. Understanding the details of controlling the Clarion implant will then be used later, in our design of a research wearable system capable of controlling this same Clarion implant.

6.0 Future Work

In addition to continuing the hardware/software work described above, we also plan to concentrate in two areas of our experimental work. First, we expect to conduct bilateral stimulation experiments with two subjects. One is profoundly deaf in both ears with an Ineraid system implanted in one and a Clarion system implanted in the other. Our plan is to continue a set of basic psychophysical measures to assess her ability to demonstrate true binaural capabilities.

The second subject, RAK, is deaf in one ear with significant residual hearing in the other. RAK recently underwent surgery for the removal of a tumor from his auditory nerve on the right side. Even though the surgeon felt he had not damaged the auditory nerve, RAK had lost all hearing in the right ear after surgery. The left ear is impaired due to a tumor developing on the left auditory nerve. To maximize the time the patient is able to use the hearing remaining in the left ear, normally the surgeon would wait until the hearing loss in that ear became profound before operating on that side. Unfortunately, this wait also decreases the likelihood that the surgeon will be able to save any residual hearing in the process of removing the tumor. Because promontory stimulation of the right ear showed a very good response (low threshold, good pitch discrimination), that ear was implanted with a Clarion cochlear implant. The rationale was that if the subject does well with the implant, the surgeon may feel comfortable removing the tumor of the left ear sooner, thereby increasing the likelihood of saving the residual hearing in that ear.

RAK will receive his device during the next quarter and will be available for testing. The residual hearing in his left ear will provide an opportunity to investigate a number of issues related to binaural hearing and will also enable a better characterization of the electric hearing through matching and masking experiments using acoustic stimuli delivered to the hearing ear.

References

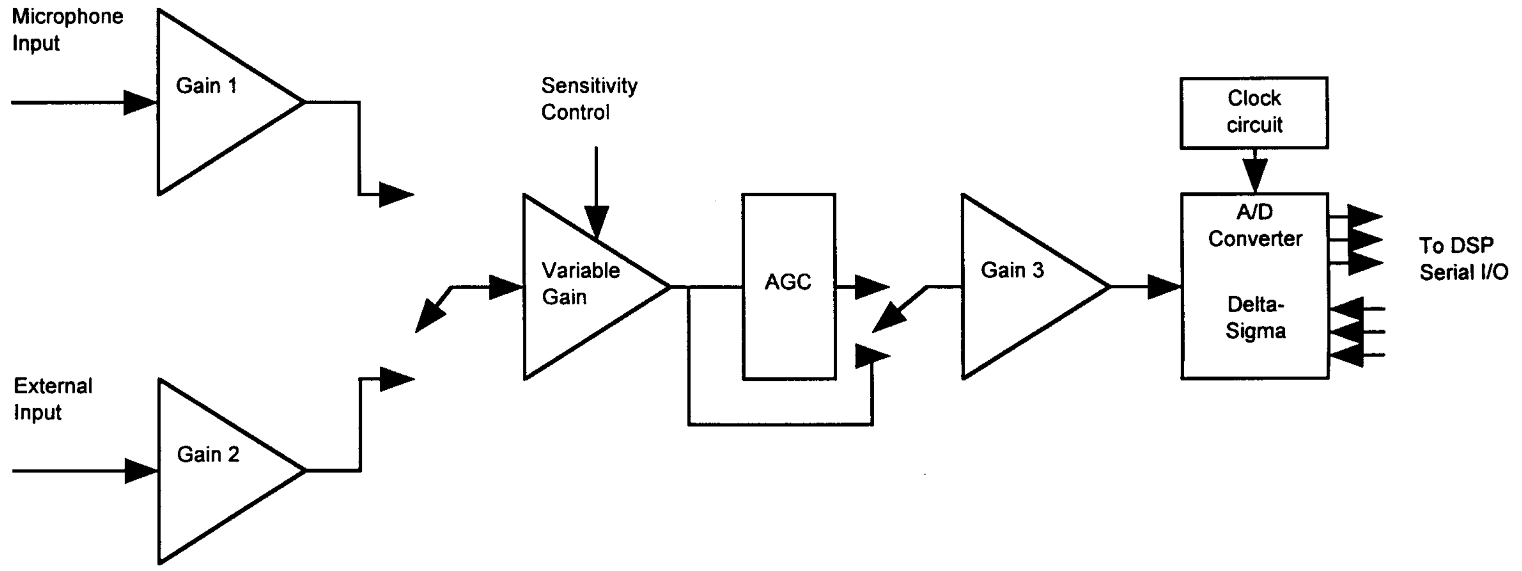
Eddington DK, Boex-Spano C, Delhorne L, Garcia N, Noel VA, Rabinowitz WM, Tierney J, Whearty ME (1996): Speech Processors for Auditory Prostheses, Fourth Quarterly Progress Report. NIH Contract N01-DC-6-2100: June 1996.

Figure Captions

Figure 1: The redesigned analog input circuit for the Geneva Wearable Processor (GWP). The two audio input paths allow for both earhook microphone and external sound inputs. Because the Delta-Sigma type of A/D converter includes an anti-aliasing filtering, there is a saving in external filter cicuitry as well as an increased operating flexibility compared to the present analog input structure.

Figure 2: This figure describes the laboratory sound processing system that is used for all psychophysical testing as well as speech processor development work. The upper right hand corner of the figure shows the present dual 8 channel 16-bit D/A outputs. these outputs can be used with a high speed sequencer for generation of pulsatile stimuli, or can drive isolated current sources directly. The portion presently under design is shown as the waveform generator and the V/I converter, and is modular so that single or multiple channels can be added as stimulation needs arise.

Figure 3: A block diagram detailing the high rate stimulation system (HRSS) presently under construction. A portion of a specification text file used to describe the desired output waveform is shown on the lower right hand portion of the figure. As shown, this waveform is scaled in amplitude by real-time inputs from the Dual Floating Point DSP system and then passed to the isolated 16-bit D/A converter and V/I circuit.


Microphone Input
Gain 1
External Input
Gain 2
Sensitivity Control
Variable Gain
AGC
Gain 3
Clock circuit
A/D Converter
Delta-Sigma
To DSP Serial I/O

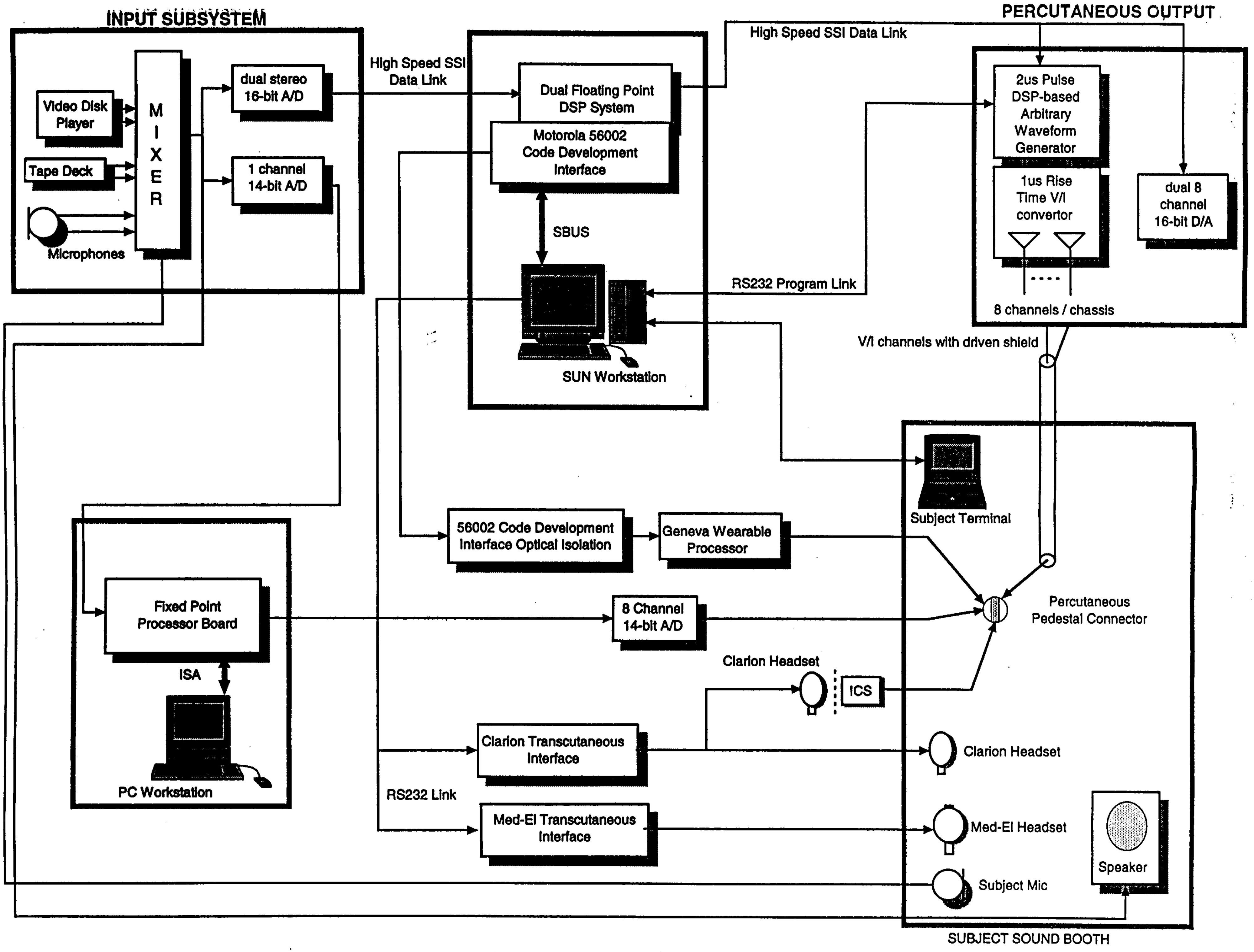
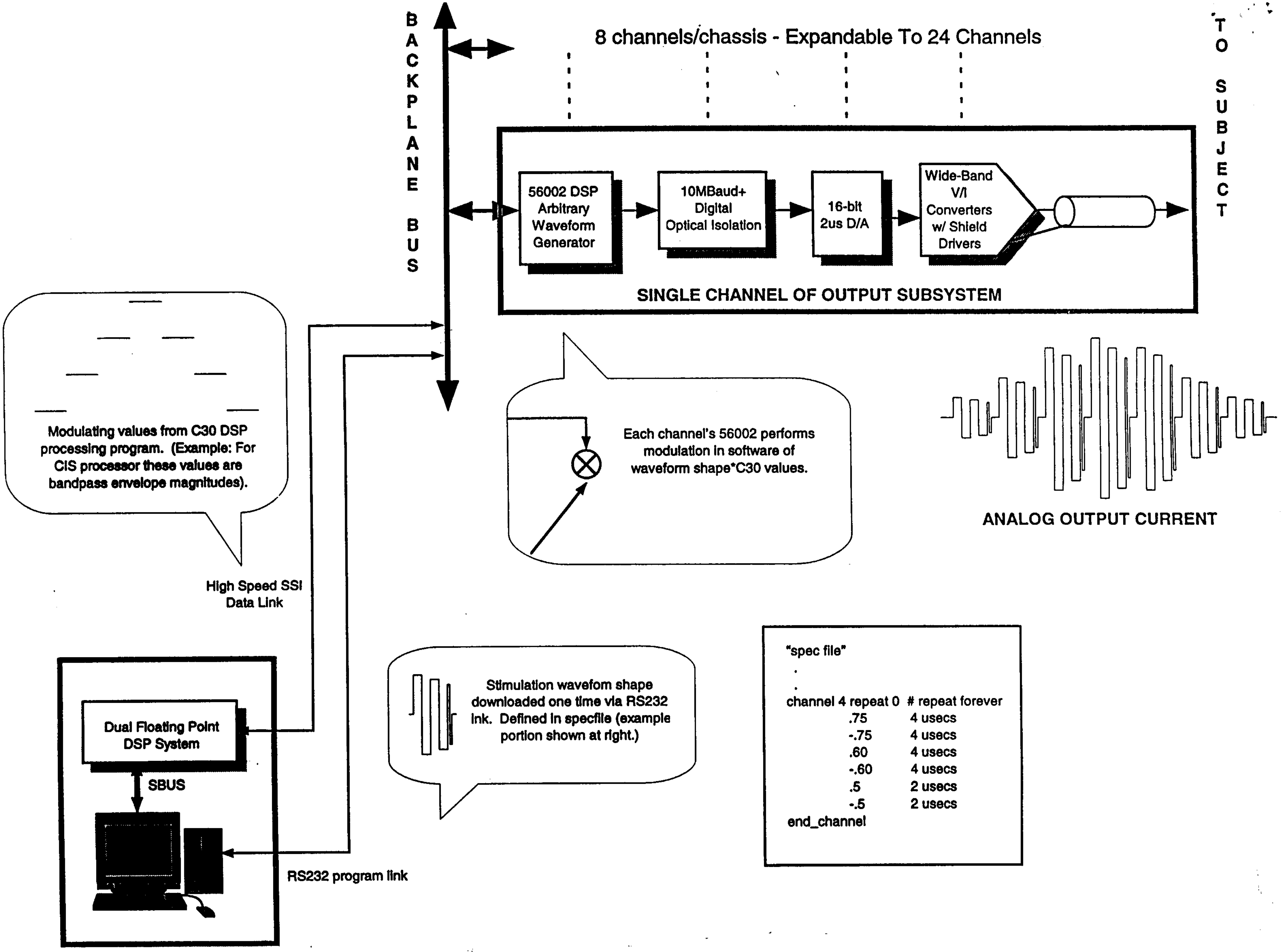

INPUT SUBSYSTEM
Video Disk Player
Tape Deck
Microphones
M I X E R
dual stereo 16-bit A/D
1 channel 14-bit A/D
High Speed SSI Data Link
Dual Floating Point DSP System
Motorola 56002 Code Development Interface
SBUS
SUN Workstation
High Speed SSI Data Link
PERCUTANEOUS OUTPUT
2us Pulse DSP-based Arbitrary Waveform Generator
1us Rise Time V/I convertor
dual 8 channel 16-bit D/A
8 channels / chassis
RS232 Program Link
V/I channels with driven shield
Subject Terminal
56002 Code Development Interface Optical Isolation
Geneva Wearable Processor
Percutaneous Pedestal Connector
Fixed Point Processor Board
8 Channel 14-bit A/D
ISA
PC Workstation
Clarion Headset
ICS
Clarion Transcutaneous Interface
Clarion Headset
RS232 Link
Med-El Transcutaneous Interface
Med-El Headset
Speaker
Subject Mic
SUBJECT SOUND BOOTH

FIG. 2



Modulating values from C30 DSP processing program. (Example: For CIS processor these values are bandpass envelope magnitudes).

Each channel's 56002 performs modulation in software of waveform shape*C30 values.

Stimulation wavefom shape downloaded one time via RS232 ink. Defined in specfile (example portion shown at right.)

```
"spec file"
 .
 .
channel 4 repeat 0  # repeat forever
         .75        4 usecs
         -.75       4 usecs
         .60        4 usecs
         -.60       4 usecs
         .5         2 usecs
         -.5        2 usecs
end_channel
```

FIG. 3