MINIATURIZED SYSTEM LEVEL PACKAGING FOR OPTICAL INTERCONNECTS

Dr. Volkan H. Ozguz

Irvine Sensors Corporation
3001 Redhill Avenue
Costa Mesa CA 92626

HIGH PERFORMANCE COMPUTING

The overall goal is to demonstrate a combination of technologies that will enable system functionalities and performance that can not be afforded by today's implementations

<u>Task</u>: to design a system with 1 Tb/s or more data throughput

<u>Problem:</u>

Planar electronic implementation can not support high data rates when system scales up (system grows larger, longer, slower interconnects)

<u>Potential Solutions:</u>

- ***Increase electronic density*** **(e.g 3D packaging and MCMs)**
  but interconnect performance and layout problems
- ***Use optical interconnects***
  more interconnect speed than processing can handle ?
- ***Use superconducting interconnects***
  implementation temperature and physical constraints

What optical interconnects are offering?

(concepts that we all know but need to be revisited every time)

- **very high speed, large bandwidths (already in place: optical fibers)**
- **parallel, random laid-out interconnects (without crosstalk, at least optically?)**
- **electrical isolation (already in place: opto-couplers)**

POTENTIAL PROBLEMS

- **When supporting electronic crosses single chip boundaries, tolerances resulting from various packaging schemes accumulates in the optical system design: chip placement on MCM, package placement on the board, board-to-board variations**
- **Optical interface becomes complicated: the regularity is lost, arrays of optical I/O ports spaced apart from each other**
- **Larger areas need to be covered optically, or more than optical component has to be used**

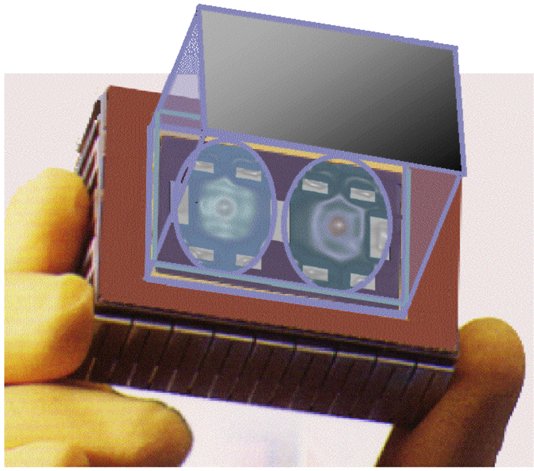
Solution:

- **more compact electronic packaging techniques**
- **more integrated submodules**

A HIGH PERFORMANCE FREE-SPACE OPTICALLY INTERCONNECTED SYSTEM INTEGRATION EXAMPLE - 3DOESP MODULE

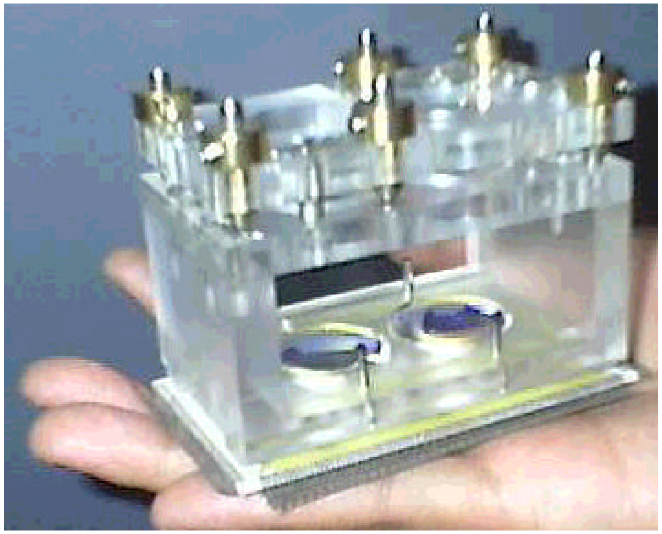
OBJECTIVE

To realize, compact, rugged reliable optically interconnected processing module that can be easily inserted in electronic systems



ACHIEVEMENT

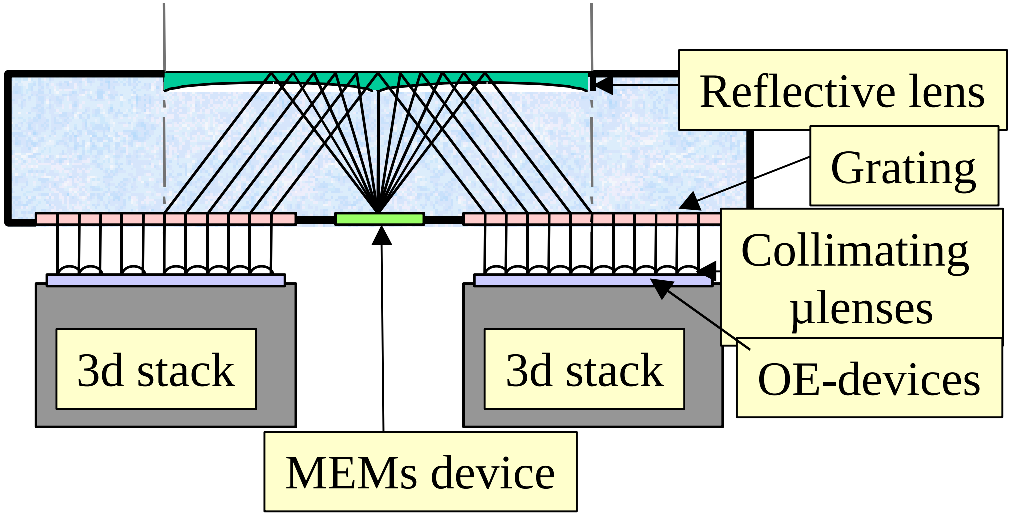
Combination of ceramic MCM and plastic optical packaging for compact module



Members of the DARPA supported Consortium are UCSD, HONEYWELL, ISC, UCSB, U. PITT, KOPIN, U. DELAWARE

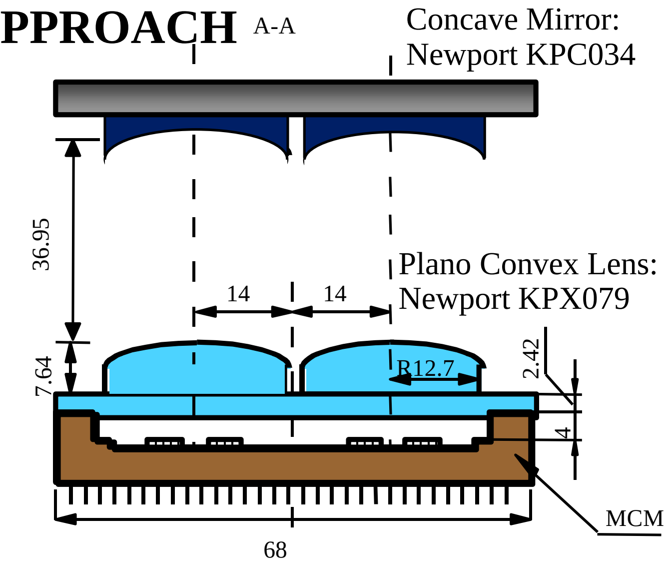
KEY APPROACHES IN 3DOESP

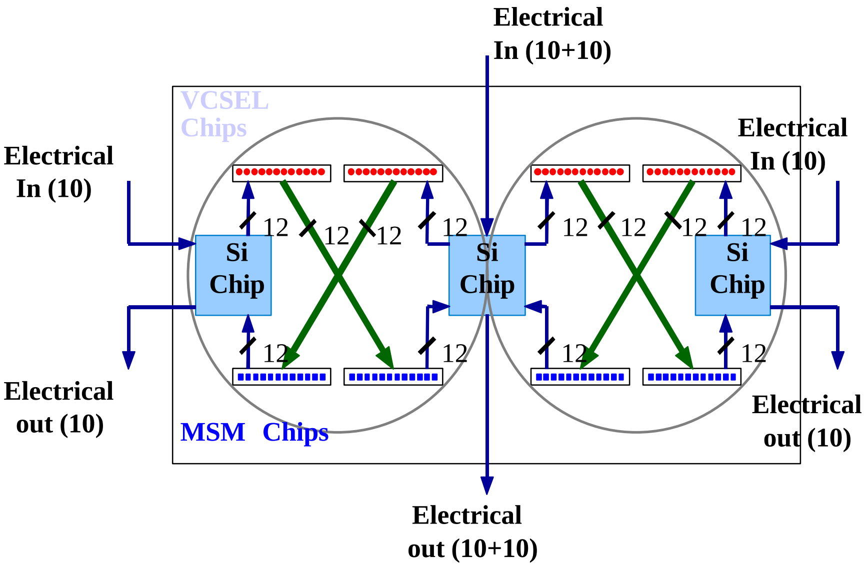
Issues in FSOI		3D-OESP solutions
• Compatibility with electronics	→	• Plastic/ceramic snap-on optics package
• Increase silicon real estate	→	• Use silicon chip stacks
• Reduce height and volume	→	• Hybrid optics increasingly using μ-optics
• Lower cost	→	• Wafer scale OE + μ-optics + flip-chip
	→	• General purpose
• Improve thermal stability	→	• Active compensation (High Power Systems)
• Signal Synchronization	→	• Serialization + minimal signal processing
• Error-free transmission	→	• Encoding - Decoding,

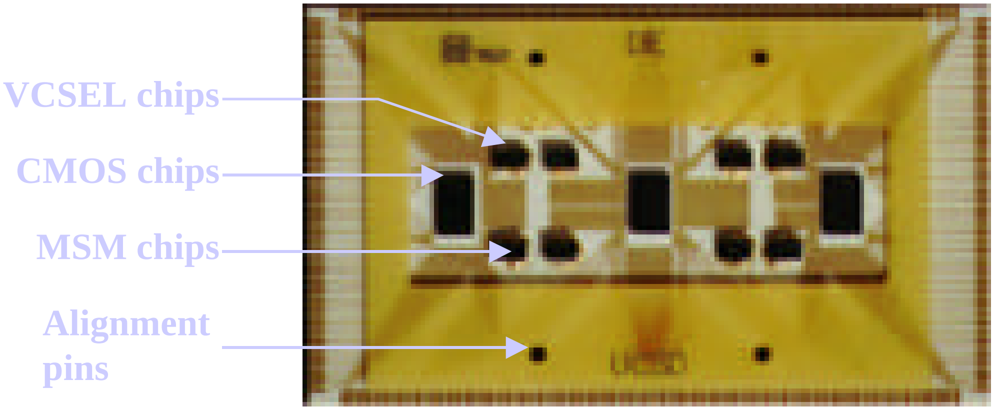


3D-OESP MULTI-CHIP FSOI MODULE

APPROACH

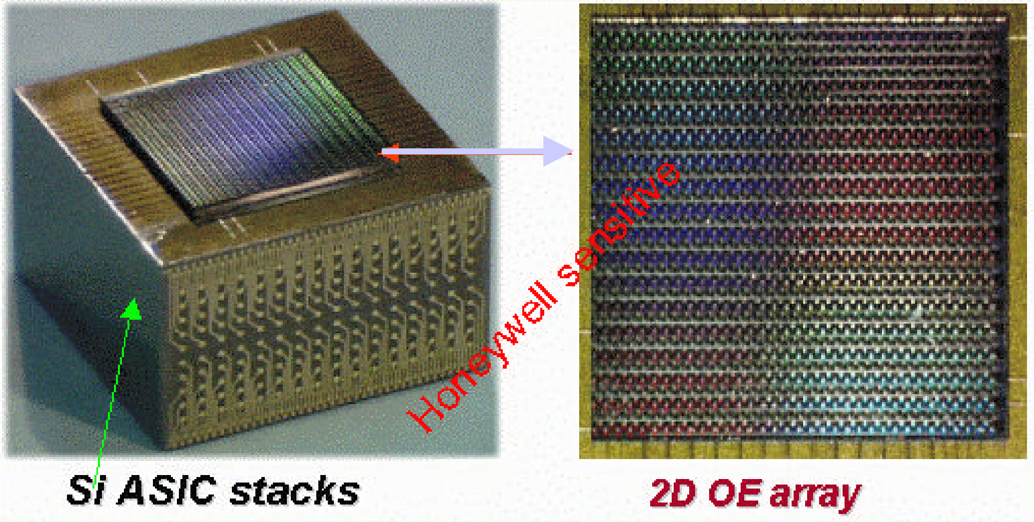




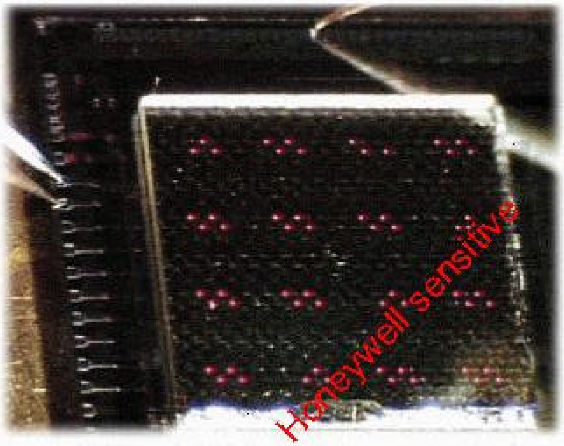


3D-OESP MULTI-CHIP FSOI MODULE

- **Hybrid Fab. of oxide VCSELs and MSMs**
- **Sub-300 μA Threshold VCSELs**
- **2.5 Gbit/sec link demonstration**

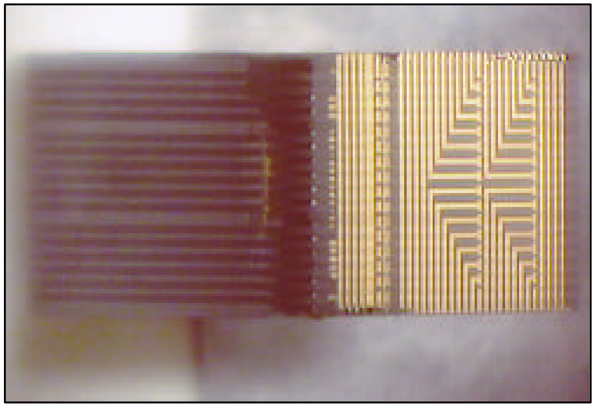


4x4 clusters (64 VCSELs) powered through the ASIC

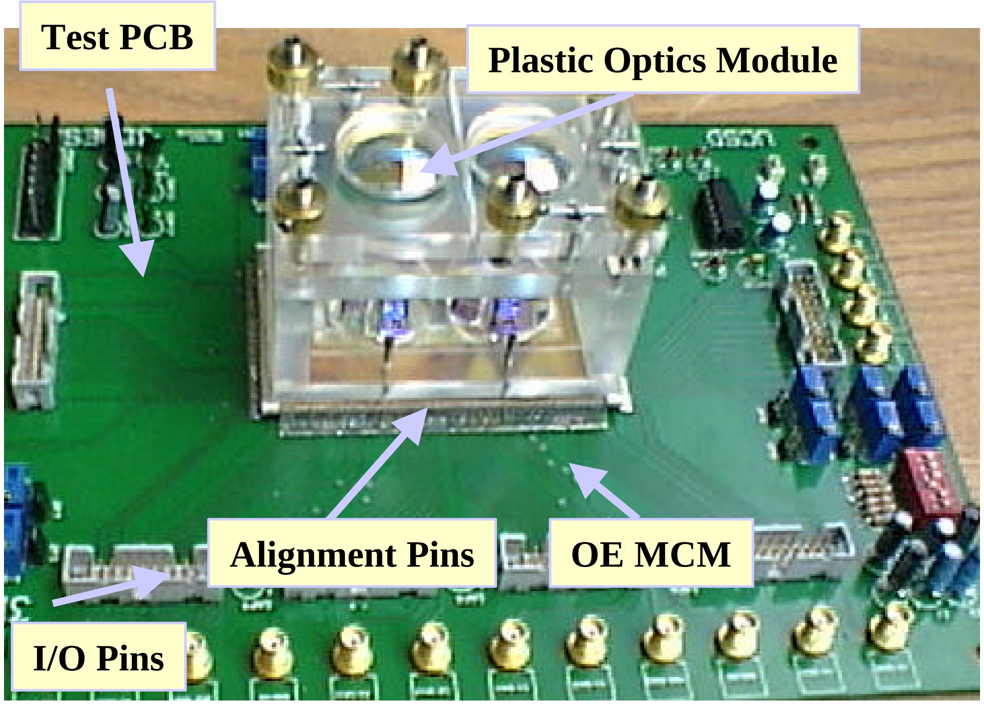


850nm VCSEL lights are perceived as red glow by the CCD camera.

Diamond interlaced stacking for high power dissipation 80W power at T=65 C

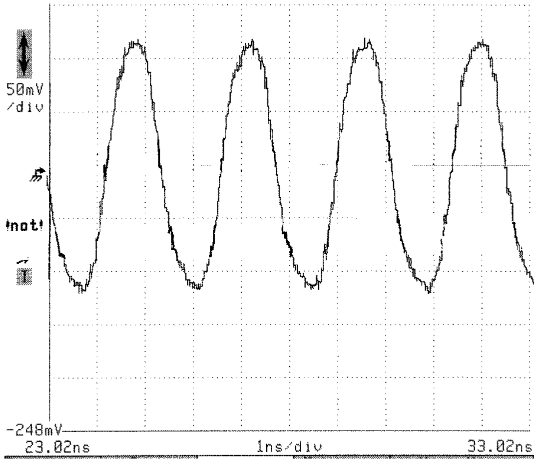


3D-OESP MULTI-CHIP FSOI MODULE



<u>Results</u>
- **48 channels**
- **4 VCSEL chips (1x12)**
- **4 MSM chips (1x12)**
- **3 CMOS chips (Rx/Tx and routing)**
- **Integration on ceramic carrier**
- **90% link efficiency**
- **-20dB Crosstalk**
- **840 Mb/s-channel**
- **Single hop and multi-hop operation**

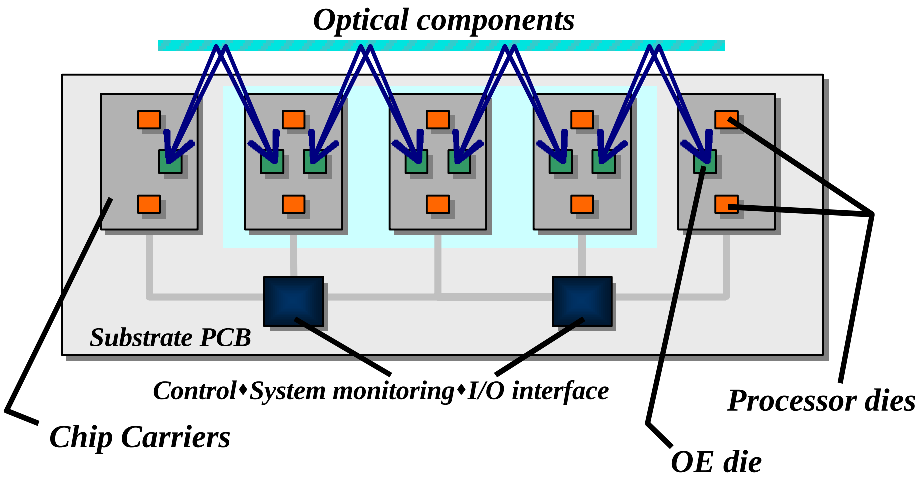
- **Electronics and Optics separated until final assembly step**
- **Passive assembly**
- **Permits rework (optical and electrical)**
- **Complete module snaps-on electrical system via I/O pins**
- **Same approach can be used with 2D-arrays for higher interconnect densities**

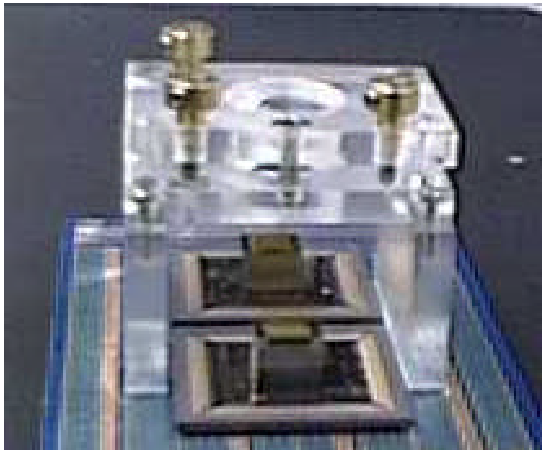


Single Channel at 840 Mbits/sec

3DOESP TECHNOLOGY INTEGRATION AND TRANSITION

Final System Demonstrator: 256 Gbit/sec crossbar switching, < 100 W, < 150 cm^3





- **Application: FFT -** ***(processor not rigidly bound to this application)*** **- Perform multiple, successive radix-2 butterfly operations over multiple chips at 150 MHz**
- **System Characteristics: Chains of pipelined processors with optical communication**
- **Flow of data: Intense use of optical interconnect as data is “bounced” between chips during calculation**
- **Enable packaging test platform**

- **Fully packaged system comprising:**
  - **3 silicon stacks with 16x16 OE device arrays**
  - **Electrical interface via flex cable and/or back side carrier**
  - **Free-space optics module**
- **Demonstrate interconnect operation at 1 Gbit/sec**

OPTICAL INTERCONNECTS IN HIGH PERFORMANCE COMPUTING

- **Techniques to reduce the overall size will be always needed**
- **Best example is the large scale integration techniques, more transistor per unit area (that created to problem to start with)**
- ***PACKAGING and INTEGRATION* is crucial**
- **Overall system design and implementation as a stand-alone, self supporting unit needs to be considered . Solutions to pieces of the problem is most of the time misleading**
- **Different interfaces may require different solutions**
- ***DETAILS - INFRASTRUCTURE***