Monolithic Integration of Optoelectronic Devices with VLSI Electronics

- using reduced-temperature epitaxy and bonding

Prof. Clifton G. Fonstad
MIT, Cambridge, MA, USA

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Colleagues and Collaborators:

Epi-on-Electronics: Joseph Ahadian, Dr. Aitor Postigo, Henry Choy, Sam Choy (U. Mass-Lowell, MIT Lincoln Lab), Prof. William Goodhue (U. Mass-Lowell, MIT Lincoln Lab), Prof. Sheila Prasad (Northeastern University)

Aligned Pillar Bonding: Wojciech Giziewicz, Dr. Guiseppe Lullo, Hao Wang

Silicon-on-Gallium Arsenide: Joanna London, Dr. Andrew Loomis (MIT Lincoln Lab) , Prof. Dimitri Antoniadis

GaAs VLSI: Mr. Jim Mikkelson (Vitesse Semiconductor)

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DOE Optical Interconnects for High Perfomance Computing Workshop (OIfHPC '99)

Where I'm coming from:

What this country needs is ....

.... a good monolithic VLSI OEIC process,

.... and access to it for researchers

What we are doing about it is ....

.... working on 3 OEIC technologies:

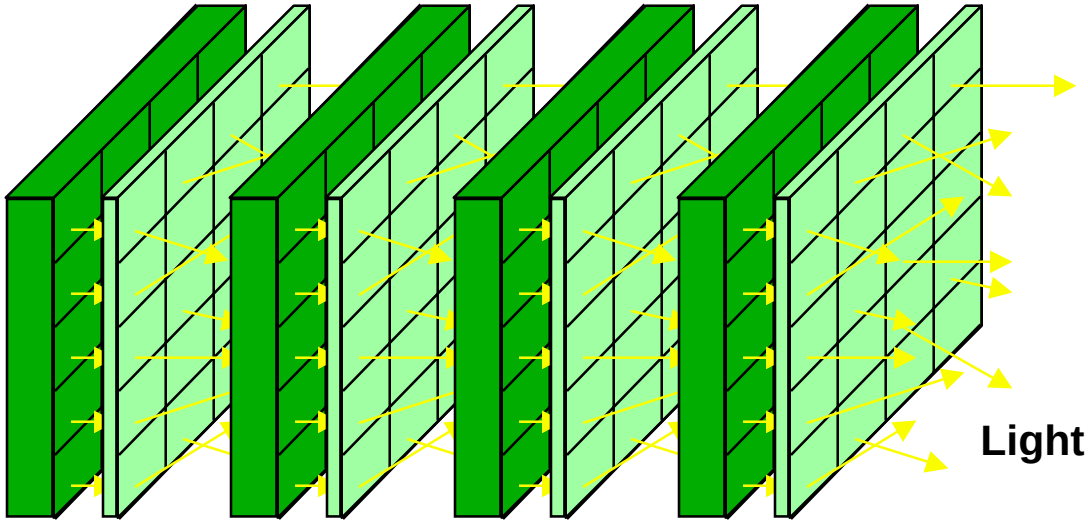
1. Epitaxy-on-Electronics (EoE)
2. Silicon-on-Gallium Arsenide (SonG)
3. Aligned Pillar Bonding (APB)

.... preparing OPTOCHIP-II research foundry:

1. H-GaAs IV electronics
2. Lateral p-i-n detectors
3. 850 nm VCSEL sources (EoE or APB)
4. SOS CMOS with APB'd VCSELs, and/or
   SonG CMOS with EoE VCSELs in future

OEIC Applications: Smart Pixel Arrays

"computation, parallel processing of data and images, en/decryption"



Information transfers -
In-plane: electrical
Plane-to-plane: optical

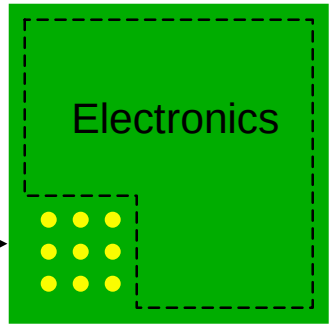
Light beams

Smart pixel arrays

Diffractive element arrays

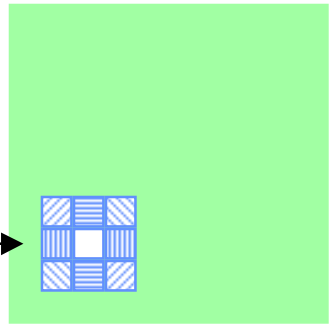
OEIC Pixel

VCSEL array over a detector



DE Pixel

3 x 3 beam-steering hologram



Concept:
The plane-to-plane coupling pattern can be dynamically re-configured by selecting which VCSELs are illuminated.

Very Large Scale Optoelectronic Integration

OBJECTIVES (our technology guidelines)

Electronics:	VLSI densities and complexities State-of-the -art performance Standard design/layout/simulation tools
Optoelectronics:	Unrestricted placement and quantities Uncompromised performance
Processing:	Full-wafer processing Batch processing Standard, manufacturable processes

→ Our goal is to make high performance, very large scale OEICs....
...economical and cost competitive,
...available and accessible, and
...useful and important.

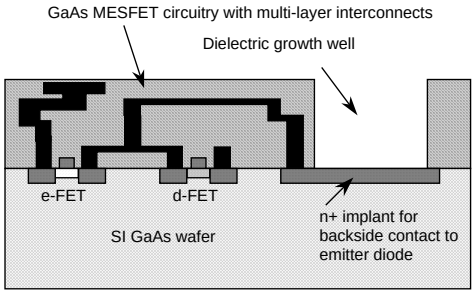
Very Large Scale Optoelectronic Integration

APPROACH (meeting our objectives)

Exploit monolithic integration:	economics of scale low parasitics, high reliability and yield high densities, small device footprints
Use a commercial IC foundation:	highly developed technologies state-of-the-art performance fully developed models and tools for simulation, design and layout
Match thermal expansion coefficients:	full-wafer processiing reliable operation, long lifetimes

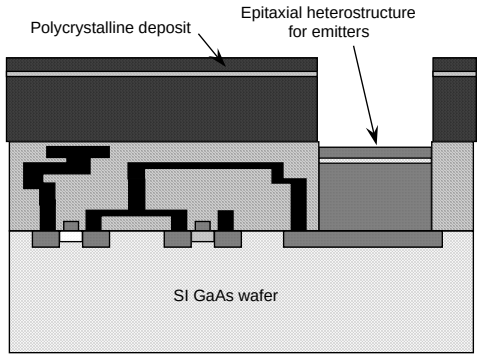
→ The key elements in our philosophy are...
- ...to reap all the benefits of monolithic integration
- ...to build on the investments of the Global IC industry
- ...to eliminate or accomodate thermal expansion mismatch

Epitaxy-on-Electronics (EoE)



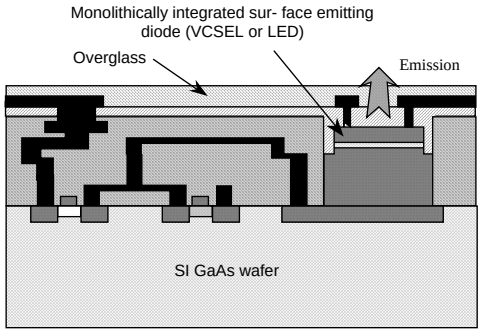
a.

Processed GaAs IC wafer as received from manufacturer



b.

After epitaxy and prior to removal of the polycrystalline deposit



c.

Optoelectronic device processing and interconnection completed

Commercially processed GaAs electronics (circuitry custom-designed using standard layout and simulation tools; chips obtained through MOSIS

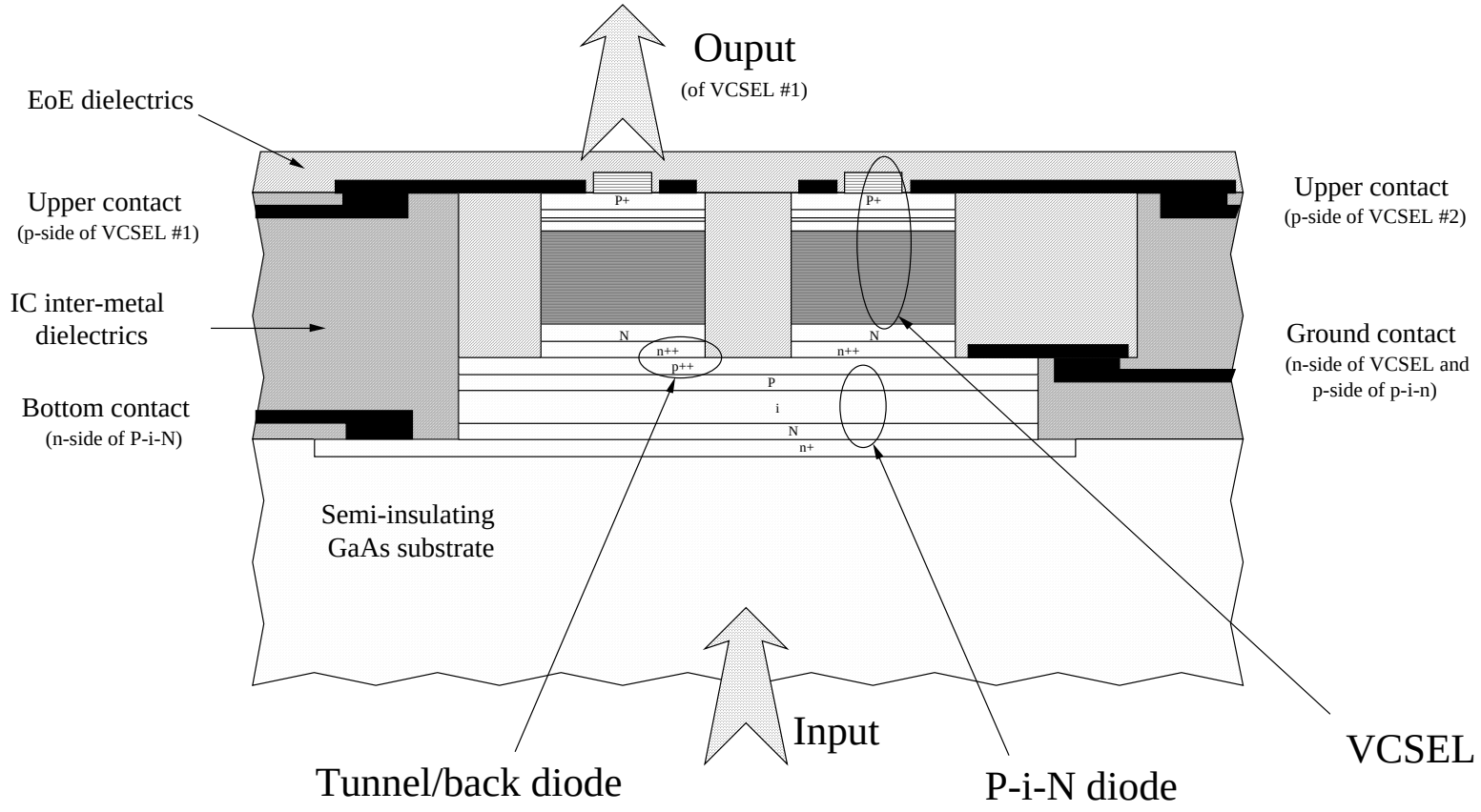
Monolithic processing, high surface planarity, no excessive overcoating of optoelectronic devices

All processing compatible with full-wafer and batch processing (no lattice or thermal expansion coefficient mismatch)

Conventional growth and fabrication of optoelectronic devices (growth temperatures must be under 475ÞC)

EoE-integrated P-i-N Diode/VCSEL Stack

- array of top-emitting VCSELs over a bottom-input photodetector
- illustrated on a GaAs MESFET DCFL integrated circuit



For many applications GaAs electronics is best, however...
for memory and microprocessor intensive applications Si CMOS is best
and for many people....Si CMOS is the*only* choice.

How can we do EoE with Si electronics?

Observation #1: GaAs-on-Si has not worked because there is too much stress

Observation #2: Optoelectronic devices are intrinsically thick, but silicon MOSFETs are very thin.

Observation #3: Thin materials can withstand large stresses, but thick materials can not.

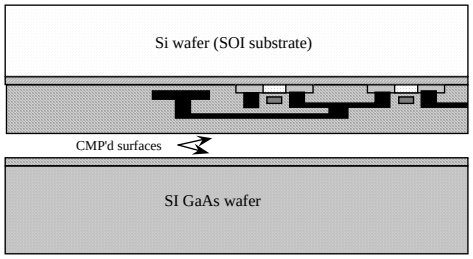
The answer: Thin silicon and thick GaAs can work together in the spirit of SOI, and especially SOS (Si-on-sapphire),

....Silicon-on-Gallium Arsenide (SonG)

Note: The clearest proof that this can work is SOS (Si-on-sapphire.
(The thermal expansion coeffiecient of GaAs equals that of sapphire.)

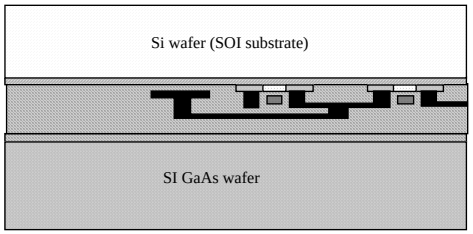
Silicon-on-GaAs (SonG)

providing CMOS substrates for EoE and APB



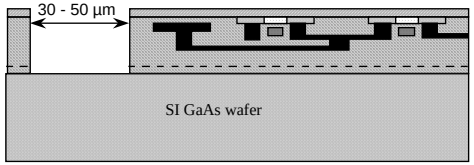
a.

The bulk GaAs wafer and the processed SOI CMOS wafer placed face to face prior to bonding.



b.

After hydrophillic room temperature bonding and prior to removal of the CMOS wafer substrate and high temperature fusion of the bond.



c.

After substrate removal, bond fusion, and preparation of windows for EoE or APB processing.

GaAs substrate provided for inherently thick, strain-sensitive optoelectronic devices

Silicon made no thicker than necessary to withstand stresses arising during high temperature processing steps

Building on advances in MEMS, SOI, CMOS, and EoE

Monolithic integration, full-wafer processing

- Aligned Pillar Bonding -

EoE has limitations (whether on GaAs or SonG):

* The epitaxy conditions are not always optimal
* The substrate choice is not totally free; may not be optimal

Thus we ask:

"How can we get the device heterostructures in dielectric windows on ICs other than through epitaxy?"

and the obvious response is: **"Wafer bonding"**

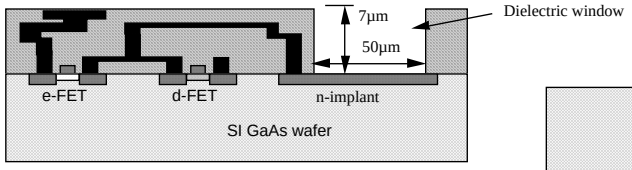
Specifically...aligning and bonding pillars etched on a heterostructure wafer in the dielectric windows on a processed integrated circuit wafer

...ALIGNED PILLAR BONDING (APB)

Notes:

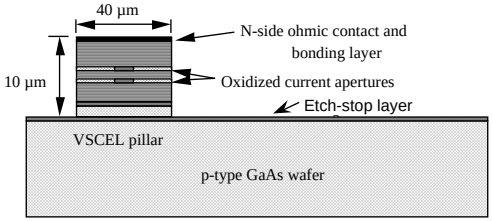
* The bonding temperature will be limited by the electronics.
* We must still match TECs, or we must bond at R.T. sufficiently to remove the substrate.
* The bonding must be uniform and complete on a very fine scale, and over the entire wafer.
* APB can be done on silicon-on-sapphire (SOS) wafers also!

Aligned Pillar Bonding (APB)



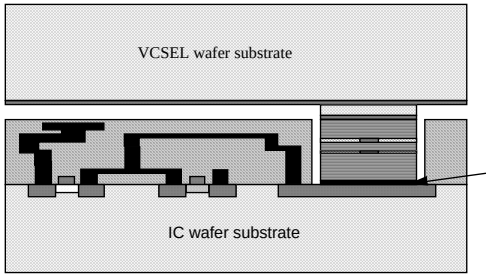
a.

The processed IC wafer as received from the manufacturer



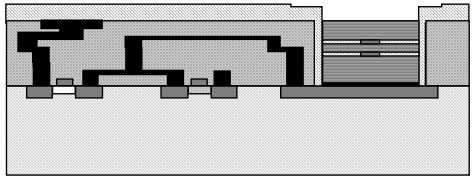
b.

The p-side down VCSEL wafer with pillars etched to match the windows on the IC wafer



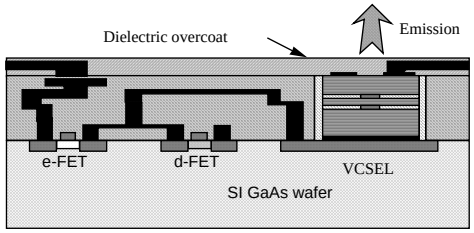
c.

After alignment and bonding of the VCSEL and IC wafers (note that only one well and pillar are shown, whereas many thousands are integrated simultaneously in the processing of full wafers)



d.

After removal of the substrate of the VCSEL wafer leaving VCSEL heterostructures bonded in windows. Further processing proceeds as in the EoE process.



e.

Device processing, integration complete

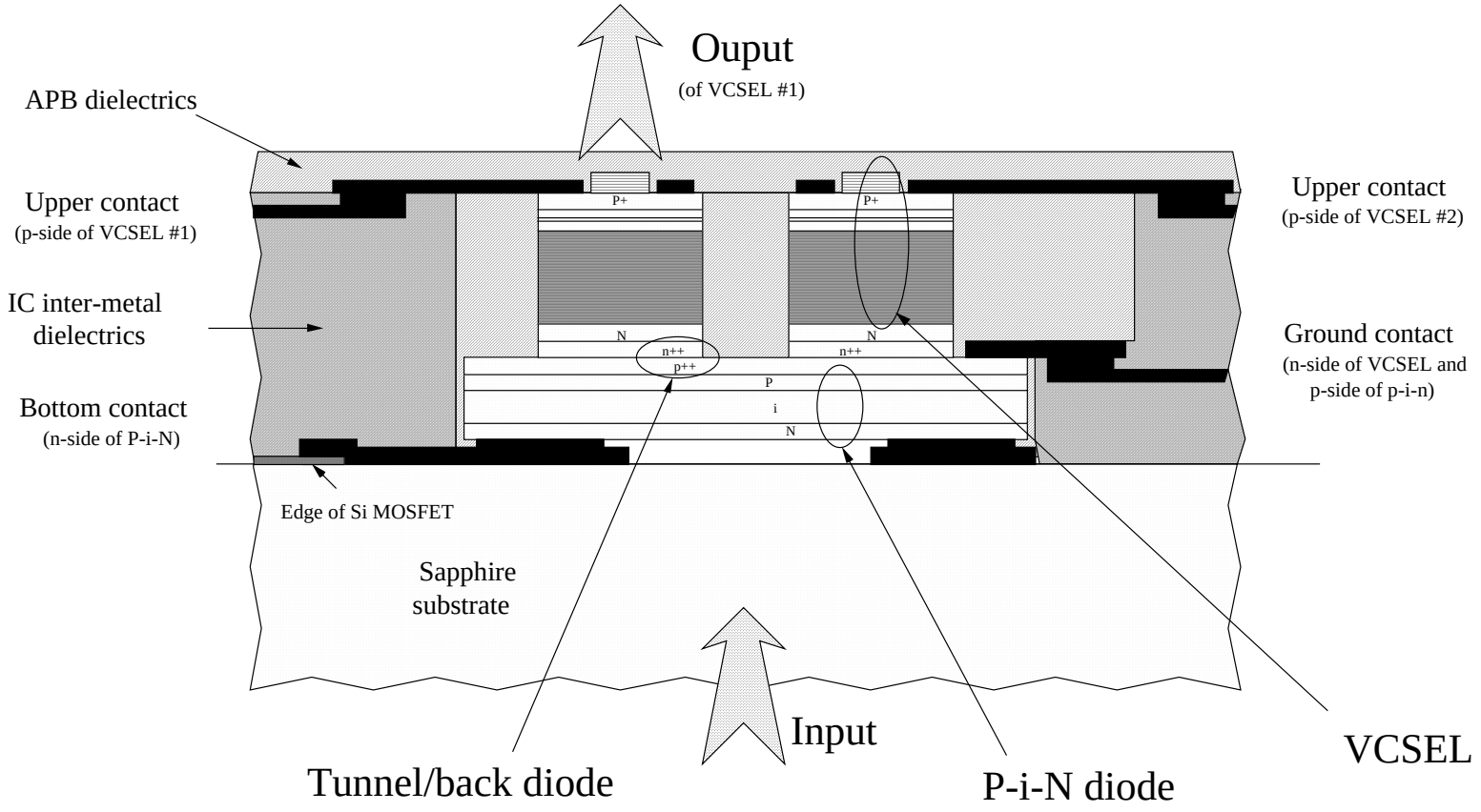
Optoelectronic heterostructures can be grown under optimal conditions on optimum substrates; bonded to GaAs or SOS

All features of EoE process retained

Near-room temperature bonding would enable integration of InP-based optoelectronics and silicon-based electronics

APB-integrated P-i-N Diode/VCSEL Stack

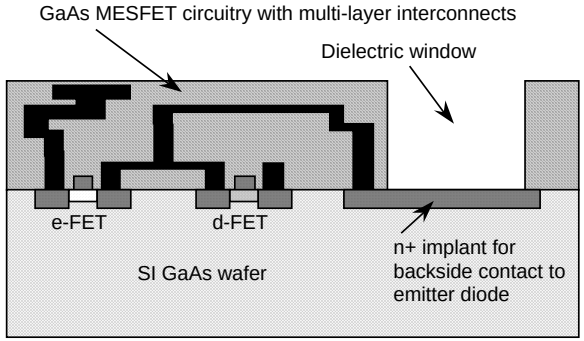
- array of top-emitting VCSELs over a bottom-input photodetector
- illustrated on a Silicon-on-Sapphire integrated circuit



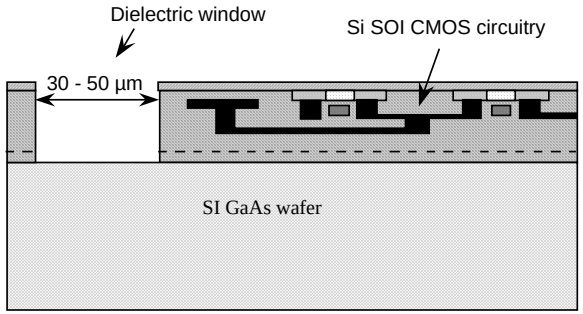
Monolithic Optoelectronic Integration

- options available with the MIT technologies -

Electronic Circuitry: GaAs MESFET VLSI or SonG Si CMOS VLSI

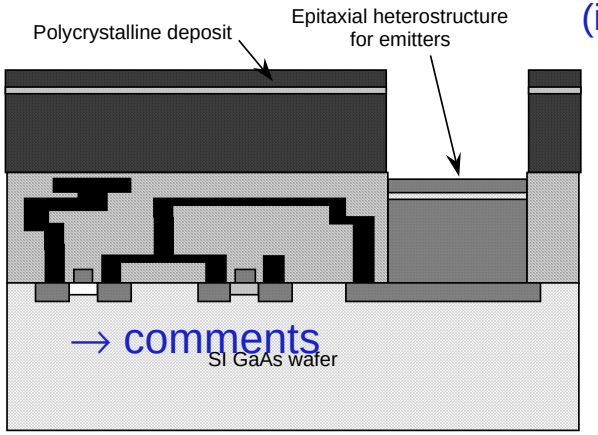


GaAs MESFET VLSI

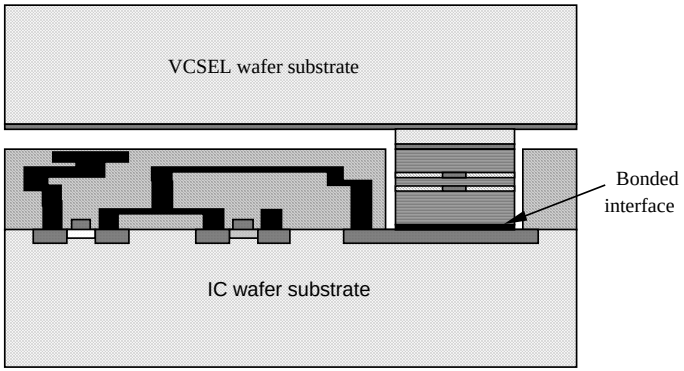


SonG Si CMOS

Integration Processes: Epitaxy-on-Electronics or Aligned Pillar Bonding
(illustrated using GaAs VLSI substrates)



Epitaxy on Electronics



Aligned Pillar Bonding

The MIT processes for Monolithic Very Large Scale Optoelectronic Integration

Epitaxy on Electronics (EoE)

Concept: Epitaxy on preprocessed electronics
Features: Full wafer, batch processing; monolithic integration; high planarity
Done: LED's on OPTOCHIP and other chips; SEEDs, RTDs, PINs, also
Next: VCSELs and IPSELs now being grown, integrated

Silicon on Gallium Arsenide (SonG)

Concept: Si-CMOS foundation for EoE and APB
Features: Thin Si to take the stress; unstressed optoelectronics for survival
Done: Preparation by bonding and thinning of 4" SonG wafers
Next: Epitaxy on SonG substrates; planarized CMOS bonding

Aligned Pillar Bonding (APB)

Concept: Aligned, Pd-bonding of heterostructures replacing direct epitaxy
Features: Optimal growth conditions, optimum substrate, all EoE features
Done: Pillars aligned and transferred; small features Pd-bonded
Next: More aligned bonding; VCSELs on OPTOCHIP; pin's on OEICs

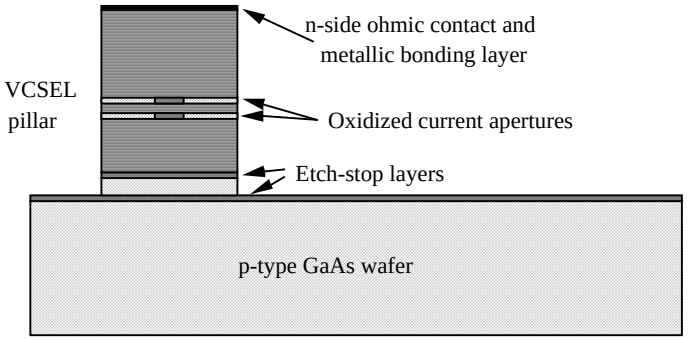
Looking further ahead:

Monolithic Integration of CMOS, DCFL, and VCSELs

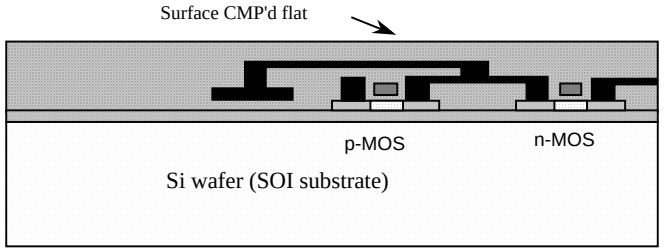
DCFL: multi-Gbps signal processing

CMOS: memory, µ-processors

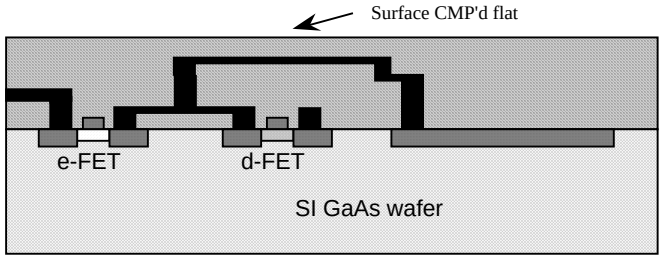
VCSELs: optical data transfer



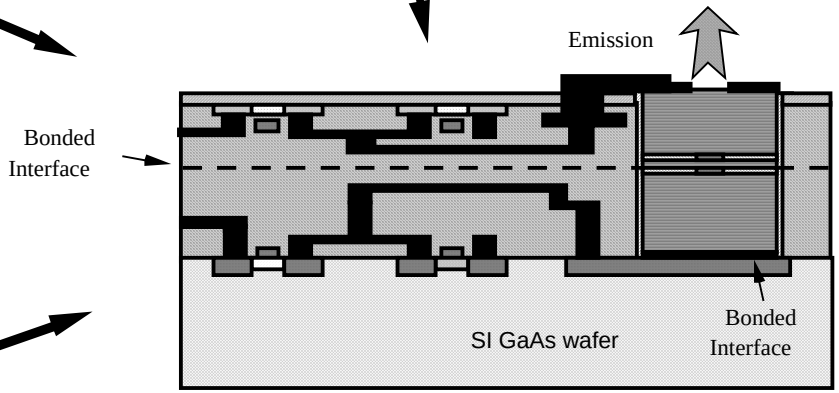
VCSEL wafer (partially processed)



SOI CMOS wafer (planarized)



GaAs DCFL wafer (planarized)



Note: Alternatively VCSEL layers can be EoE-grown directly into the device window on the bonded GaAs-CMOS wafer pair.