Materials & Processing for Si Compatibility

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Introductory overview
Photonic Bandgap Materials

Possible Options for On-Chip Waveguide Interconnects

- **Hard dielectric waveguides**
  - low-loss optical fiber compatibility
    - » low index contrast $\Delta N \sim 0.005$
    - » α = 0.1 dB/cm to < 0.01 dB/cm
    - » e.g., LPCVD-based buried BPSG/TEOS
  - higher-index for higher-density routing
    - » high index contrast $\Delta N > 0.1$
    - » α < 0.1 dB/cm ?
    - » e.g., LPCVD-based SiON/TEOS
- **Polymeric waveguides**
  - low-temperature post-processing
    - » low index contrast $\Delta N \sim 0.05$-0.005
    - » $\alpha \sim$ 0.1 dB/cm to 0.5 dB/cm, depending on λ
    - » e.g., fluorinated acrylates or polyimides

Possible Applications of PBG Materials

1) Passive devices

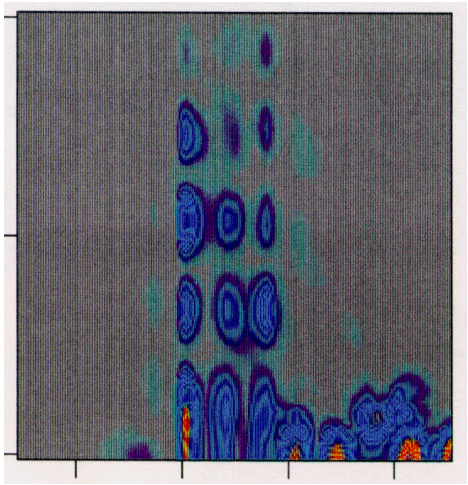
- Infrared Mirrors

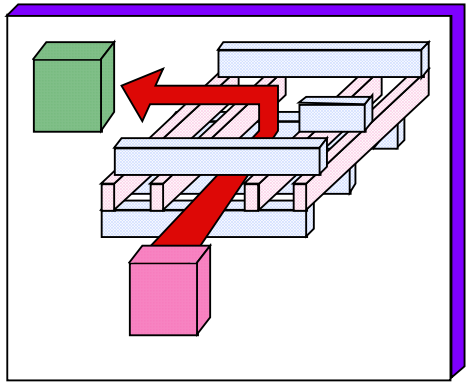
- Thermal Emissivity Modification

- Prisms
  - Optical Communications

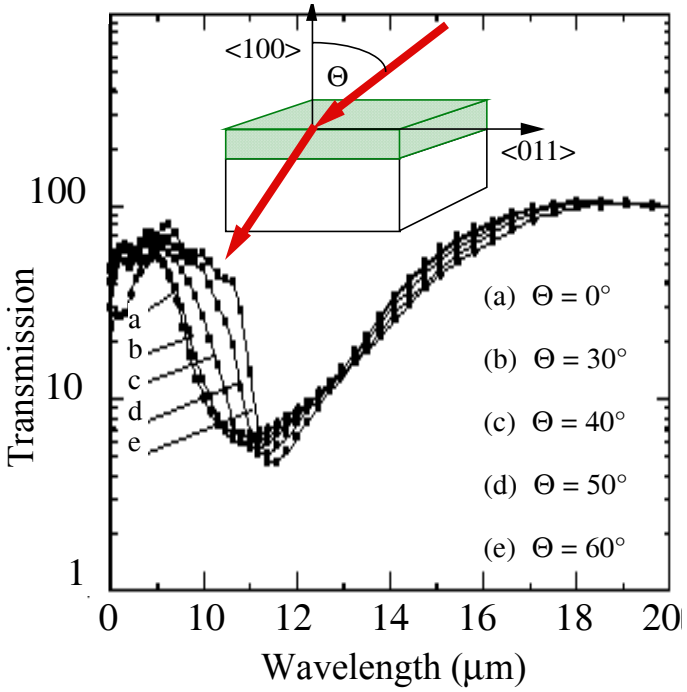
- Cavities
  - Spectroscopy
    - Military and Optical Communications

- Waveguides
  - 90° bends possible in three dimensions





Bandstop is Largely Independent of Angle



2) Active devices

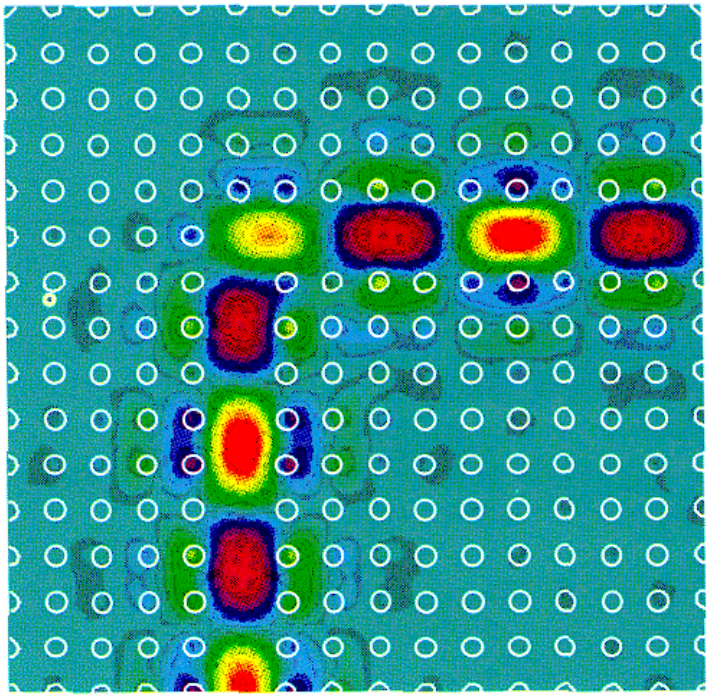
- Ultra-Fast Switches
- Si Infrared LED's
- Si Infrared Lasers

3) Integrated devices

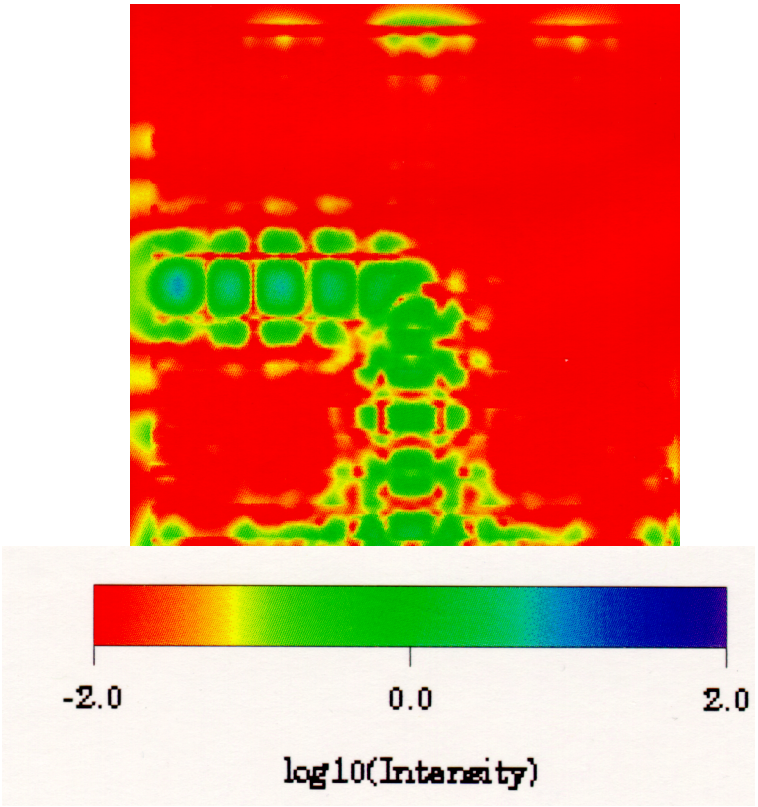
- Photonic circuits

Simulated Electric Field Patterns for 90-degree Waveguide Bend

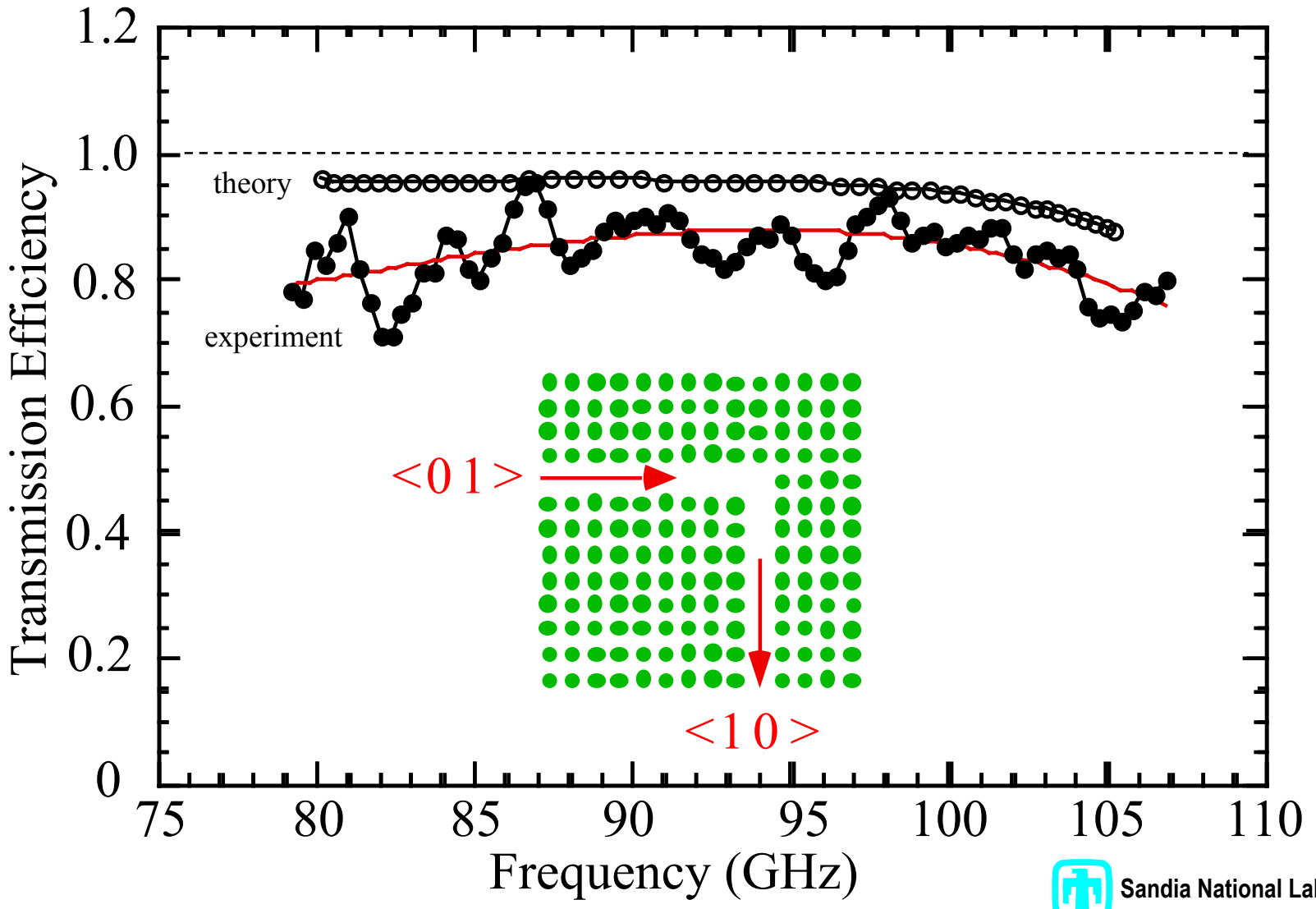
2D Square Lattice



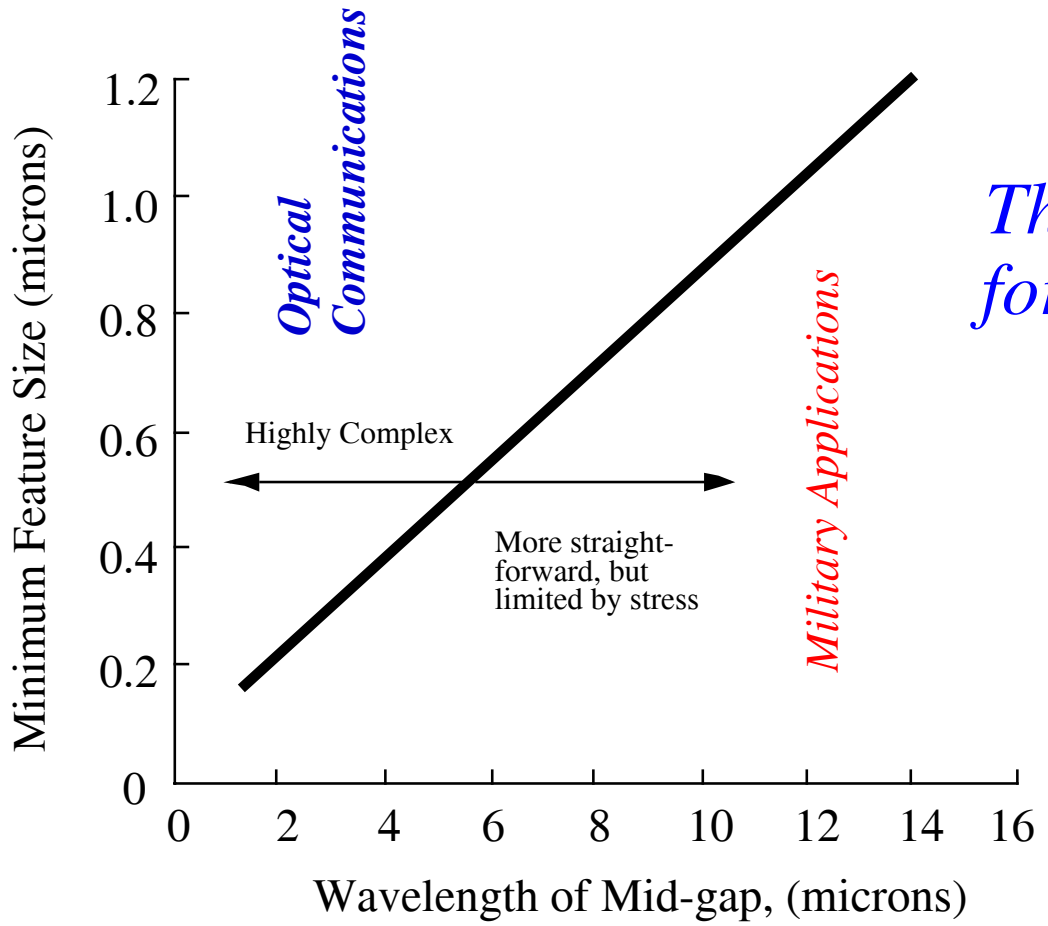
3D Square Lattice



90-degree Waveguide Bend at Millimeter-Wave Frequencies



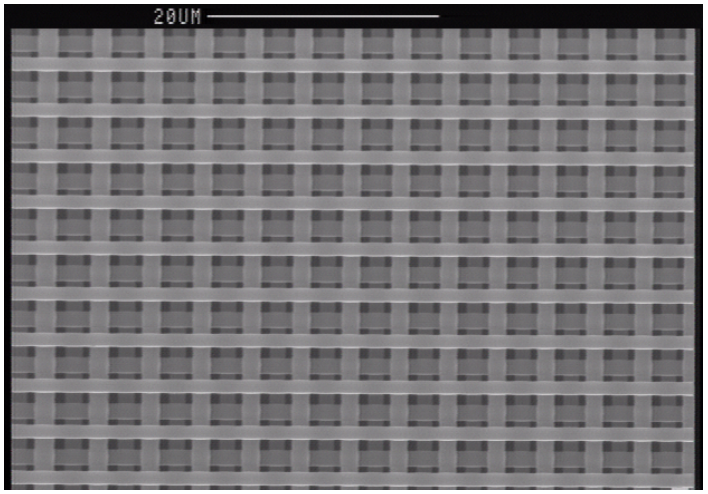
The Microfabrication Challenge



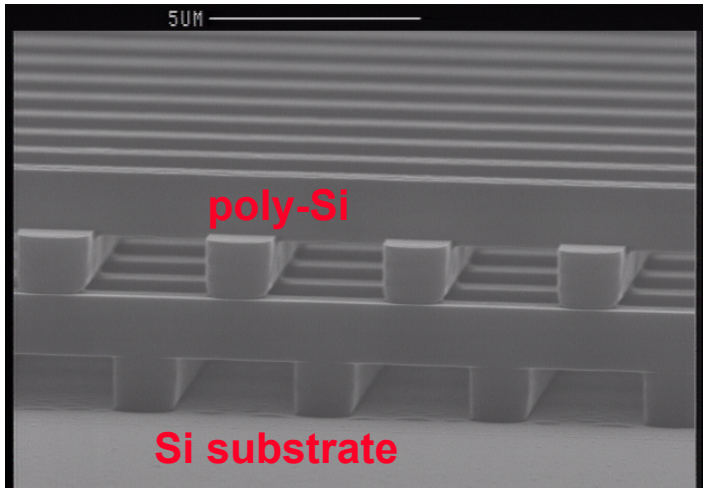
The minimum feature size for a lattice with bandgap of 1.5 micron is 0.18 microns!

3D Silicon Photonic Crystal at Mid-IR Frequencies

Top View



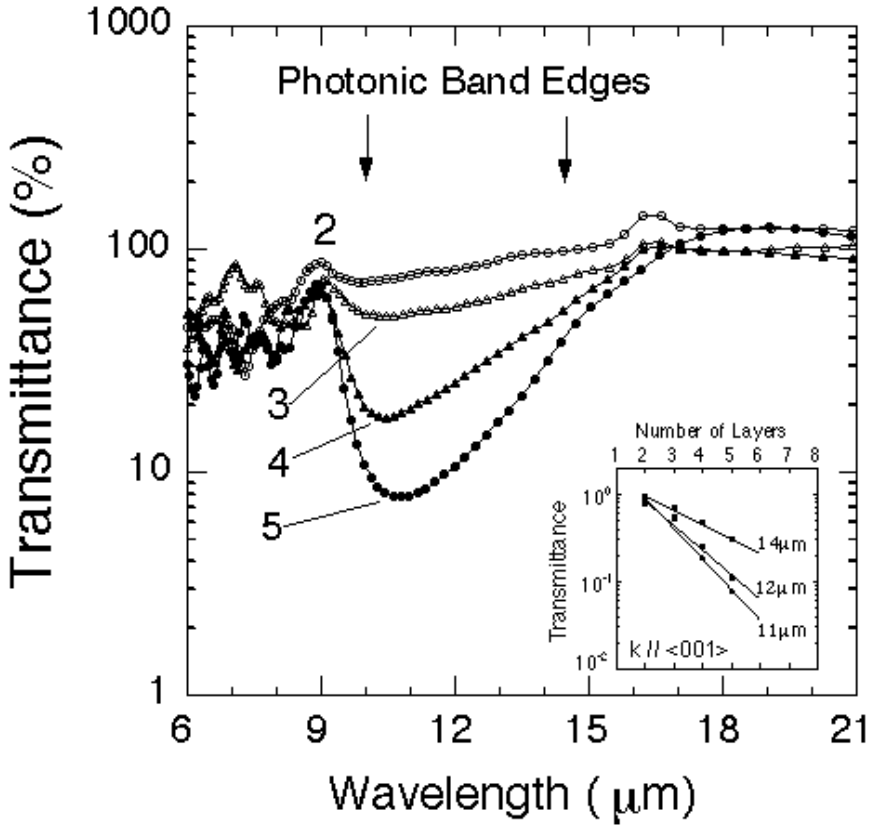
Side View



4-layer crystal

Technology Challenges

- precise stacking;
- smooth planarization;
- large area uniformity.



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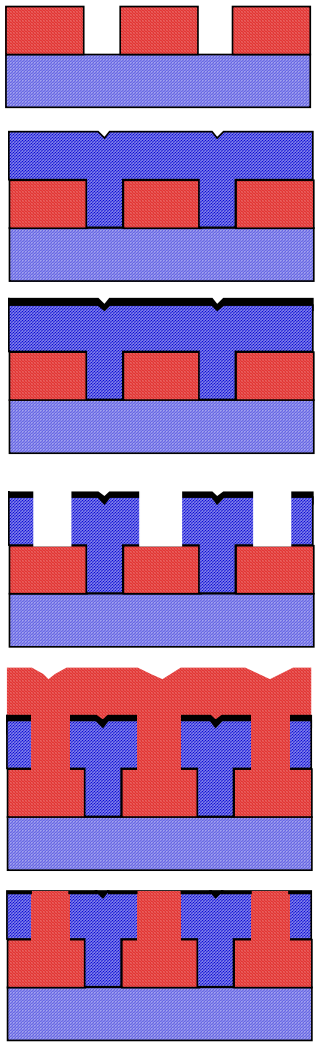
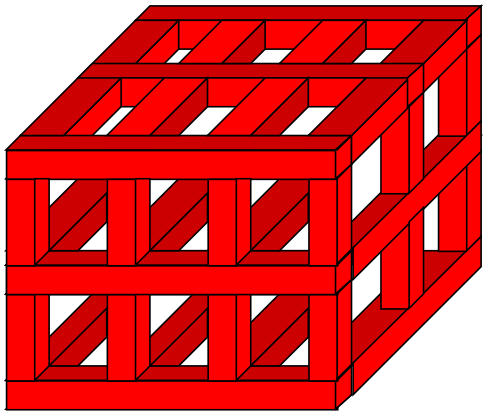
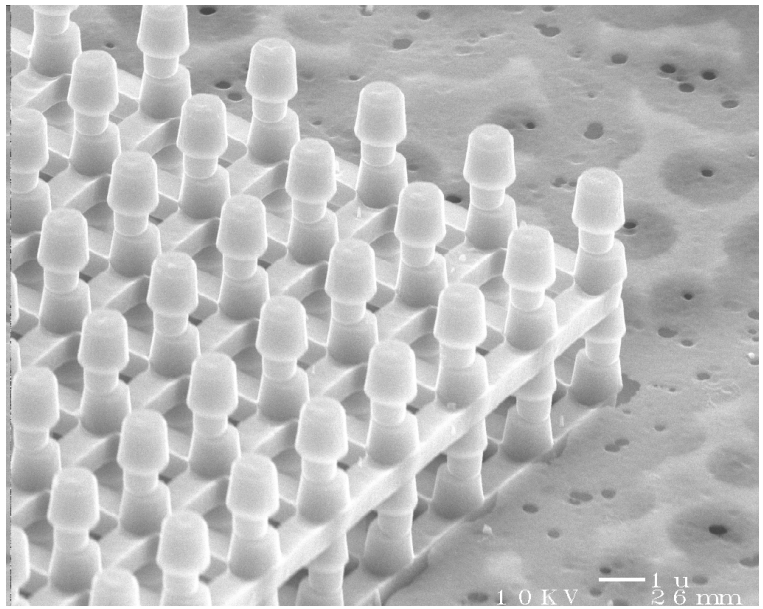
Mold Process Flow

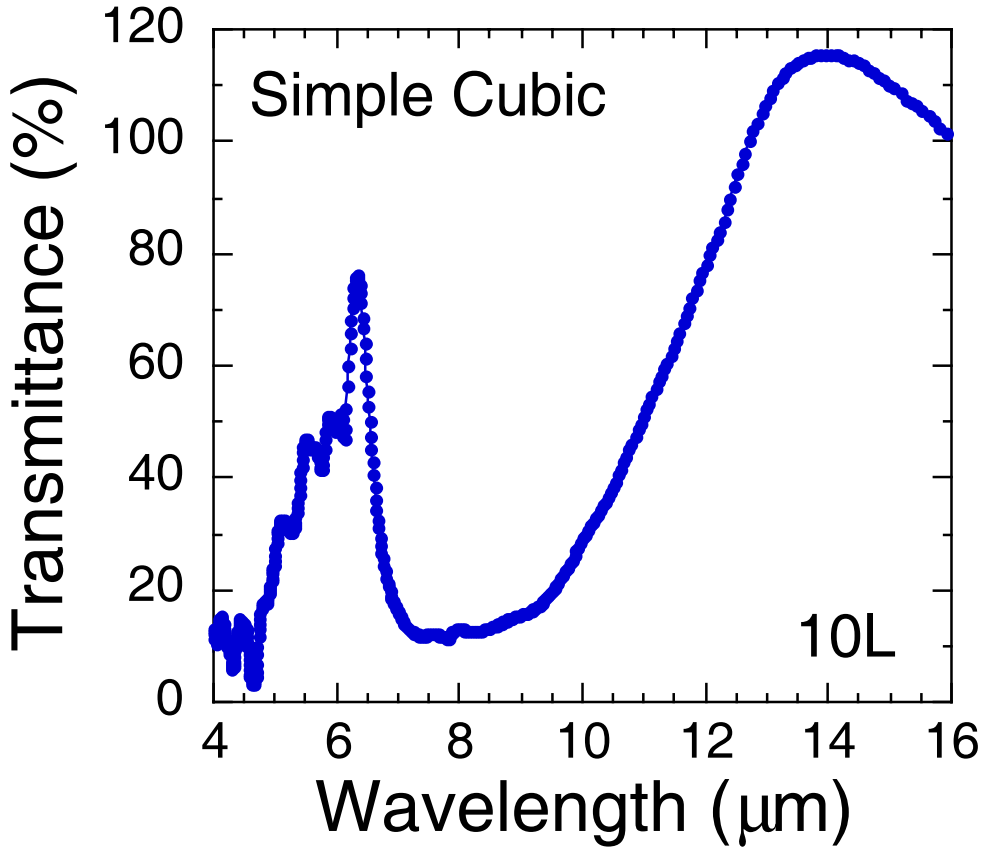


1) Deposit oxide with thickness equal to that of the layer.
2) Pattern and etch mold.
3) Fill mold with polysilicon. Poly thickness equal to that of the layer thickness.
(Only works for designs where $W \lesssim T$)
4) Deposit thin SiN, CMP stopping layer.
5) Pattern the second level.
6) Fill gaps between patterned poly with oxide.
7) Chemical mechanically polish, stopping on SiN.

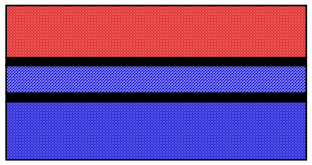
The Simple Cubic Structure Fabricated Using the Mold Process



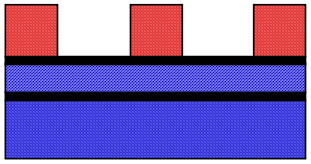




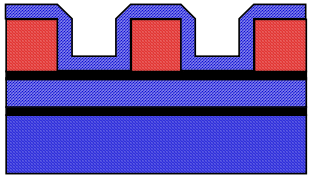
Fillet Flow Process



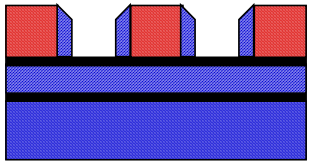
1) Deposit SiN (first layer only), poly with layer thickness (2200Å) and SiN hard mask (500Å). Deposit 5000Å oxide sacrifical layer.



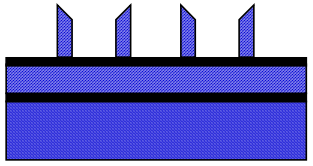
2) Pattern oxide with lines and spaces, 6500Å lines, 6500Å space. Etch oxide in HF, remove ~900Å isotropically.



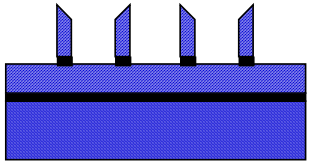
3) Deposit 1800Å polysilicon fillet layer



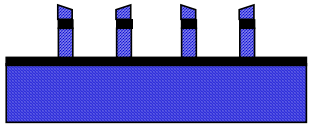
4) Form fillet using anisotropic RIE.



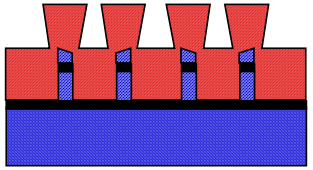
5 Remove sacrifical oxide in HF.



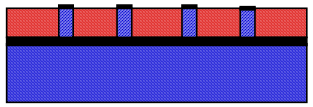
6) Etch SiN in hot phosphoric acid.



7) Use fillet as a mask for poly etch.

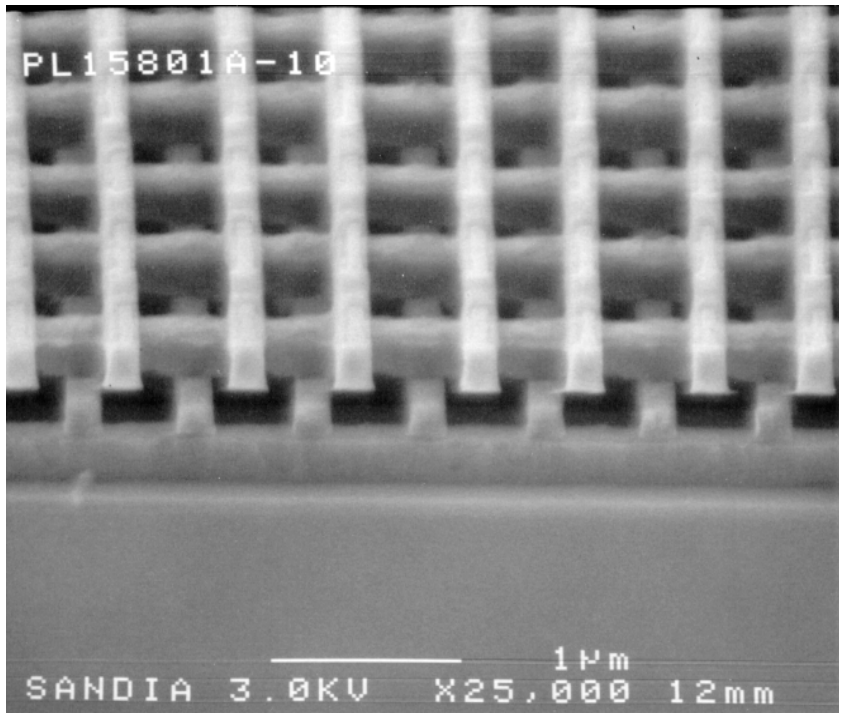


8) Fill spaces between lines with oxide.

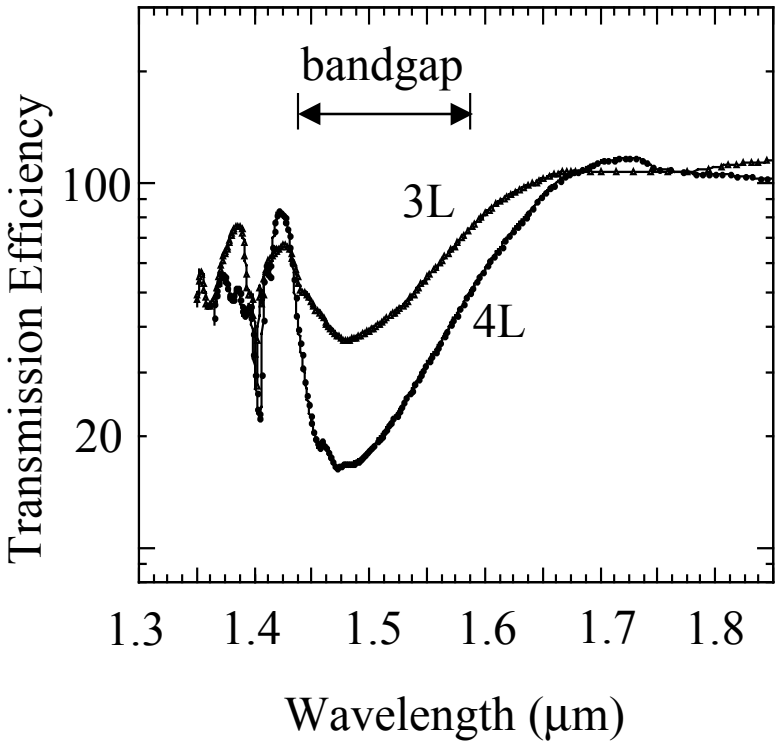


9) CMP, stopping on the SiN.

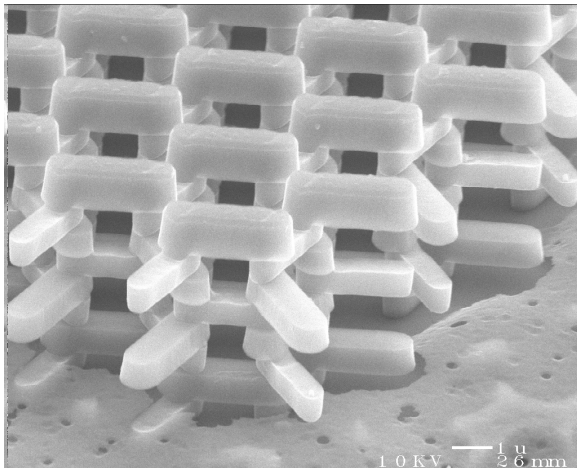
1.5µm Bandgap Fillet Structure

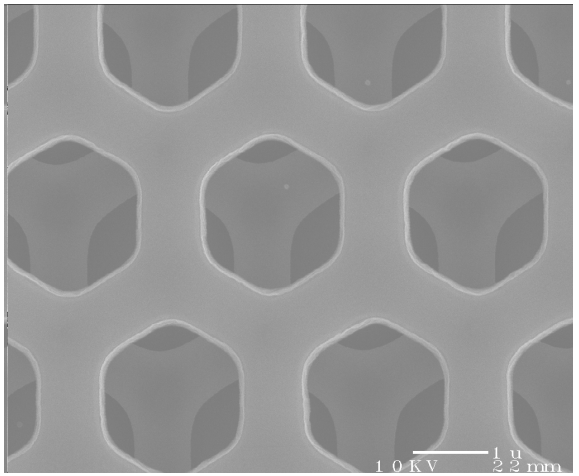


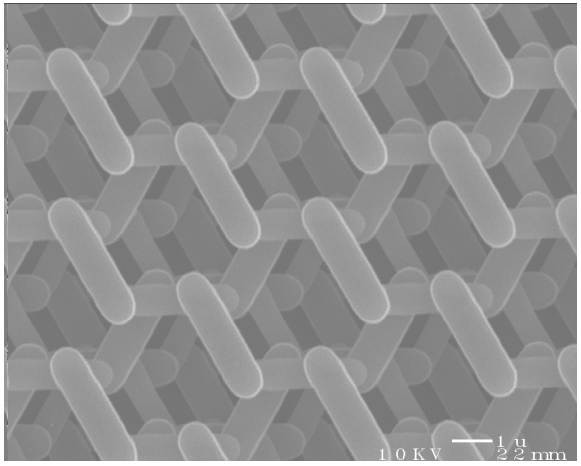
Measured Results

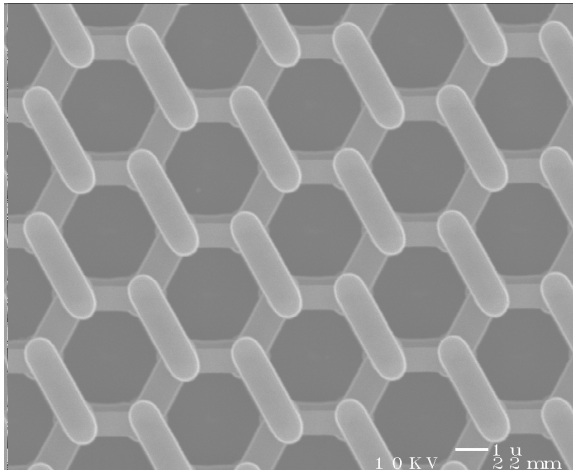


Novel Structures Under Investigation



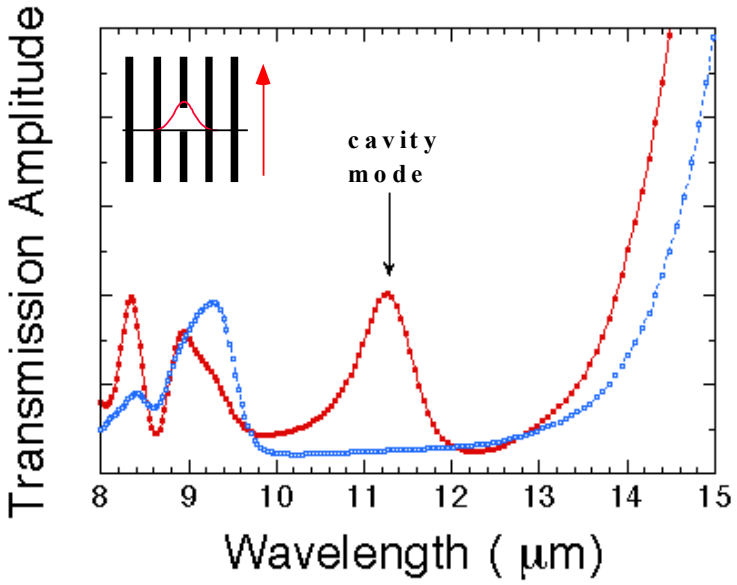




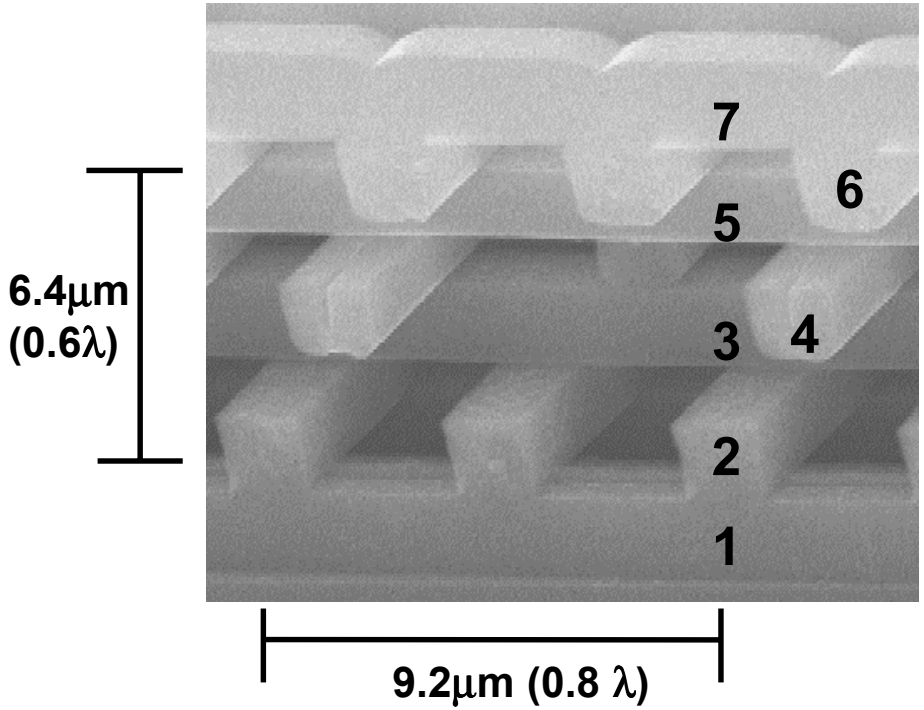


Singlemode 3D Defect Cavity

Modal Volume: $0.8\lambda^3$



Defect Volume: $0.2\lambda^3$



Higher-Q Results