Panel II: Technology Integration for Insertion of OI in Computing

What tasks must be addressed for effective integration of OI technology?

Introduction: Kevin Martin - Georgia Tech

Panel Presentations:

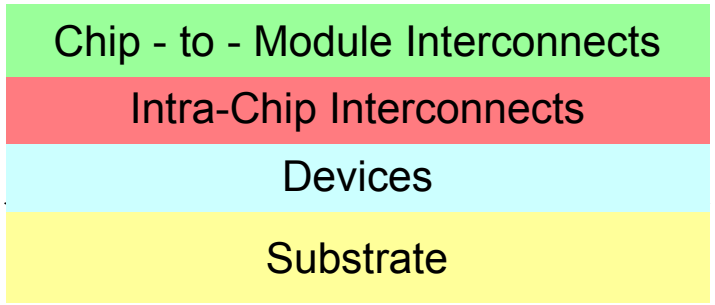
- Tim Drabik - Georgia Tech
- Clif Fonstad - MIT
- Volkan Ozguz - Irvine Sensors
- Perry Robertson - Sandia National Laboratory
- Jim Hutchby - SRC

Panel Discussion

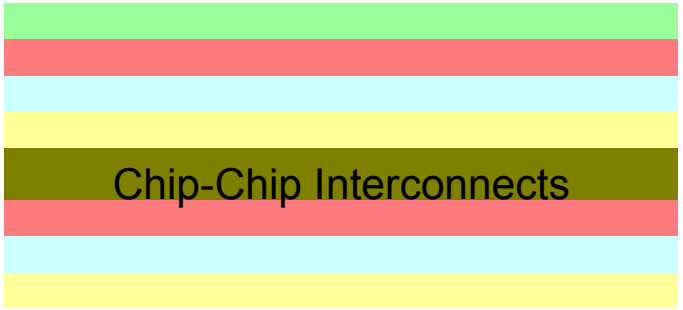
- What major tasks must be addressed for effective integration of OI technology?
- What activities should occur in these tasks?
- Identify and employ useful relationships between them.

Interconnects - *Hierarchy & Continuum*

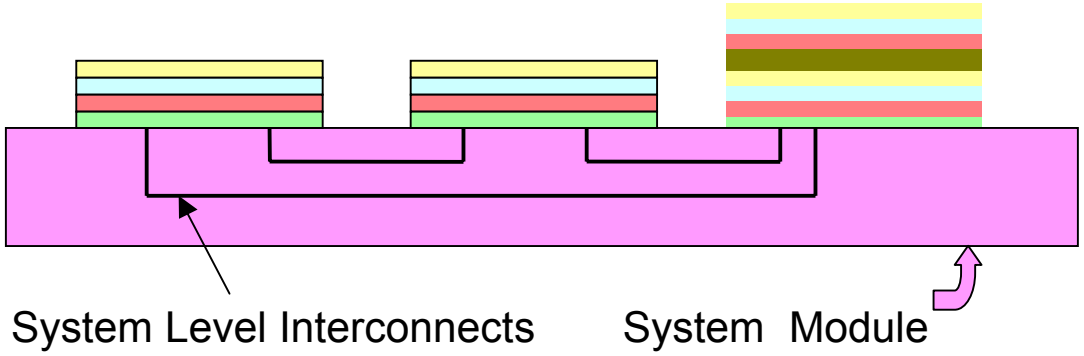
Chip-Level



3-D



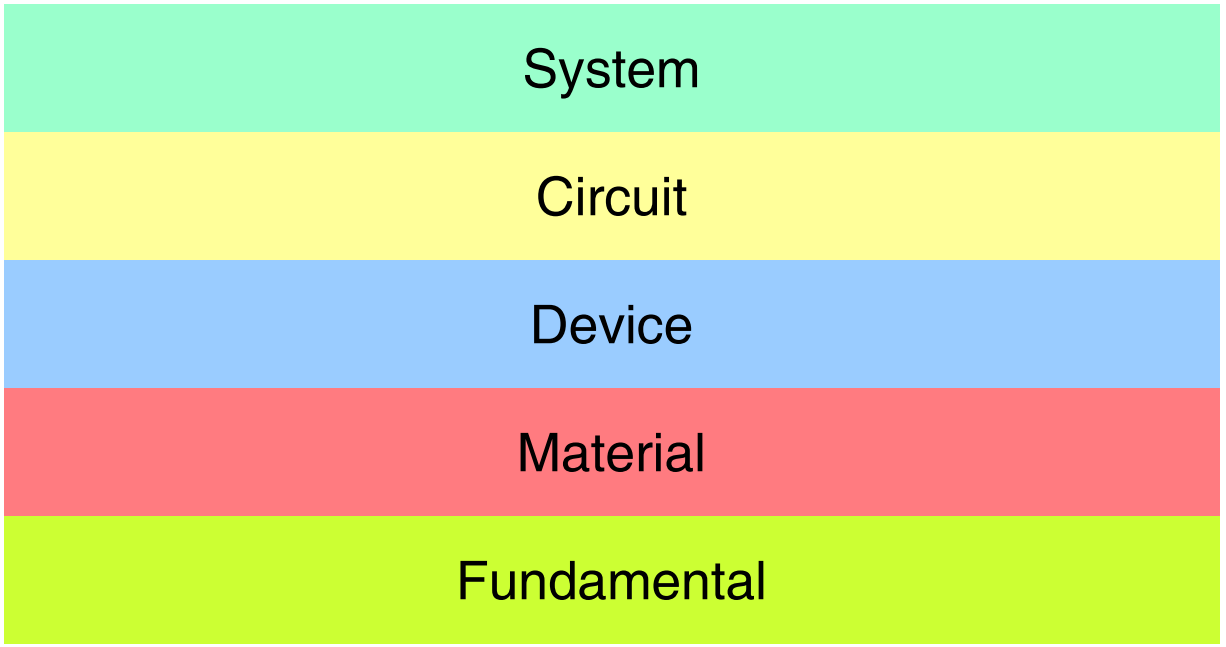
System Level



Interconnect Methods

- Wiring
- RF
- Optical

Hierarchy of Limits



1998 ITRS Expectations for High-Performance Chips (*update*)

Year of First Shipment	**2005**	**2008**	**2011**	**2014**
Chip Area (mm^2)	520	620	750	901
Chip Pad Count (CPC)	3492	4776	6532	8935
Area Array Chip Pad Pitch (mm)	0.385	0.360	0.338	0.318
Signal & Clock I/O Count (est. 50% of CPC)	1746	2388	3266	4467
Gate Delay (ps)	7	4 - 5	3 – 4	NA
On-Chip Local Clock (GHz)	3.5	6.0	10.0	16.9
On-Chip Speed (GHz)	2.0	2.5	3.0	3.7
Multiplexed Chip-Board Speed (GHz)	2.0	2.5	3.0	3.7
Power Consumption (W)	160	170	175	183
Operational Lateral CTE Mismatch (μm)*	17	19	20	23

* For an organic PWB with a CTE = 20 ppm/C, and operation at 45C

Technology Integration Tasks:

- System Architecture:

  Communication and Interconnect- Centric Architecture

- Physical Design Tools:

  Build a library of physical interconnect cells that can be combined to generate models of interconnect networks.

- Materials and Processing:

  Create hybridized systems composed of materials with dissimilar opto-electronic, chemical, and physical properties.

Technology Integration Tasks (cont.)

- Process Modeling and Simulation:

  Develop and implement integrated physically-based models to simulate the physical structure and properties.

- Technology Assessment:

  Evaluate the viability of different interconnect technologies.

- Reliability and Characterization:

  Develop software modeling and experimental characterization tools to conduct reliability prediction, optimization and diagnostics for new technologies.

Technology Integration Tasks (cont.)

- Design:

  Software tools and methodologies required to assist the design and verification of systems composed of heterogeneous elements

- Testing:

  Methodologies and hardware to conduct burn-in and testing of high speed and complex parts at the wafer, chip, and system level