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# Eleventh Quarterly Progress Report

March 26 through June 27, 1988

NIH Contract N01-NS-5-2396

## Speech Processors for Auditory Prostheses

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CONTENTS

## I. Introduction

The purpose of this project is to design and evaluate speech processors for auditory prostheses. Ideally, the processors will extract (or preserve) from speech those parameters that are essential for intelligibility and then appropriately encode these parameters for electrical stimulation of the auditory nerve. Work in the present quarter included the following:

1. Development of a detailed plan for upgrading the Cochlear Implant Laboratory at Duke for a series of studies to be conducted with MiniMed, Symbion and Nucleus patients this fall;

2. Initial implementation of this plan;

3. Refinement of algorithms and hardware for real-time extraction of the fundamental frequency of voiced speech sounds, for application in portable speech processors for auditory prostheses;

4. Detailed analysis and interpretation of results from recent studies conducted in our laboratory, including studies with (a) six patients implanted with the UCSF/Storz prosthesis and (b) two patients implanted with an experimental multichannel prosthesis developed by the 3M Company;

5. Continued collaboration with the UCSF team in the development of the speech processor and transcutaneous transmission system for a next-generation auditory prosthesis;

6. Presentation of project results at the Cochlear Implant Consensus Development Conference, held at the NIH on May 2-4, 1988; and

7. Continued preparation of manuscripts, including two for the book Models of the Electrically Stimulated Cochlea (to be edited by J. M. Miller and F. A. Spelman), one on our evaluation of two-channel, "Breeuwer/Plomp" processors for cochlear implants (see QPR 8, this project), and one on ensemble models of neural discharge patterns evoked by intracochlear electrical stimulation (see QPR 8, NIH project N01-NS-3-2356).

In this report we will present our plan for extending the capabilities of our Cochlear Implant Laboratory and indicate the present status of work implementing this plan. We also will describe briefly our efforts to date in the collaboration with UCSF to develop a next-generation auditory prosthesis. A complete review of results from the studies listed in point 4 above will be presented in the next progress report for this project.

## II. Extension of Cochlear Implant Laboratory Capabilities

In anticipation of extensive series of tests with implant patients this fall, much effort was expended in the present quarter to upgrade the Cochlear Implant Laboratory at Duke. A prime motivation for this effort is the need to replace our obsolete and failure-prone Eclipse computer with a modern 80386-based machine. Use of the 80386 machine will greatly increase the reliability of laboratory operation during the critical periods of patient testing. In addition, the new machine will speed up many of the computational tasks associated with speech processing and with the conduct and analysis of speech perception tests.

An integral element of the new 80386 machine will be a TMS320C25 coprocessor card. This card will be programmed for real-time execution of our "block diagram compiler" software (Wilson and Finley, 1985). In the remainder of this section we will describe the hardware configuration of the new system and provide a status report on the implementation of this system.

### Hardware Configuration

The hardware configuration of the new laboratory system is presented in Fig. 1. The core of the system is a 20MHz, 80386-based personal computer (PC). This PC is equipped with a bus-compatible TMS320C25 development system. Real-time speech processor emulations will be executed by the TMS320C25 under the control of the PC. The powerful block compiler facility is retained in the software running on the PC. The operator interacts with the compiler software on the PC to specify a speech processor design. When specification is completed, the compiler automatically generates an intermediate TMS320C25 assembly code listing that is cross-assembled by the PC, loaded into the TMS320C25 system, and executed there.

Once running on the TMS320C25, a block-compiled real-time processor receives its input primarily by A/D conversion of analog signals from any of a variety of sources. Available sources include microphones, video disc, audio

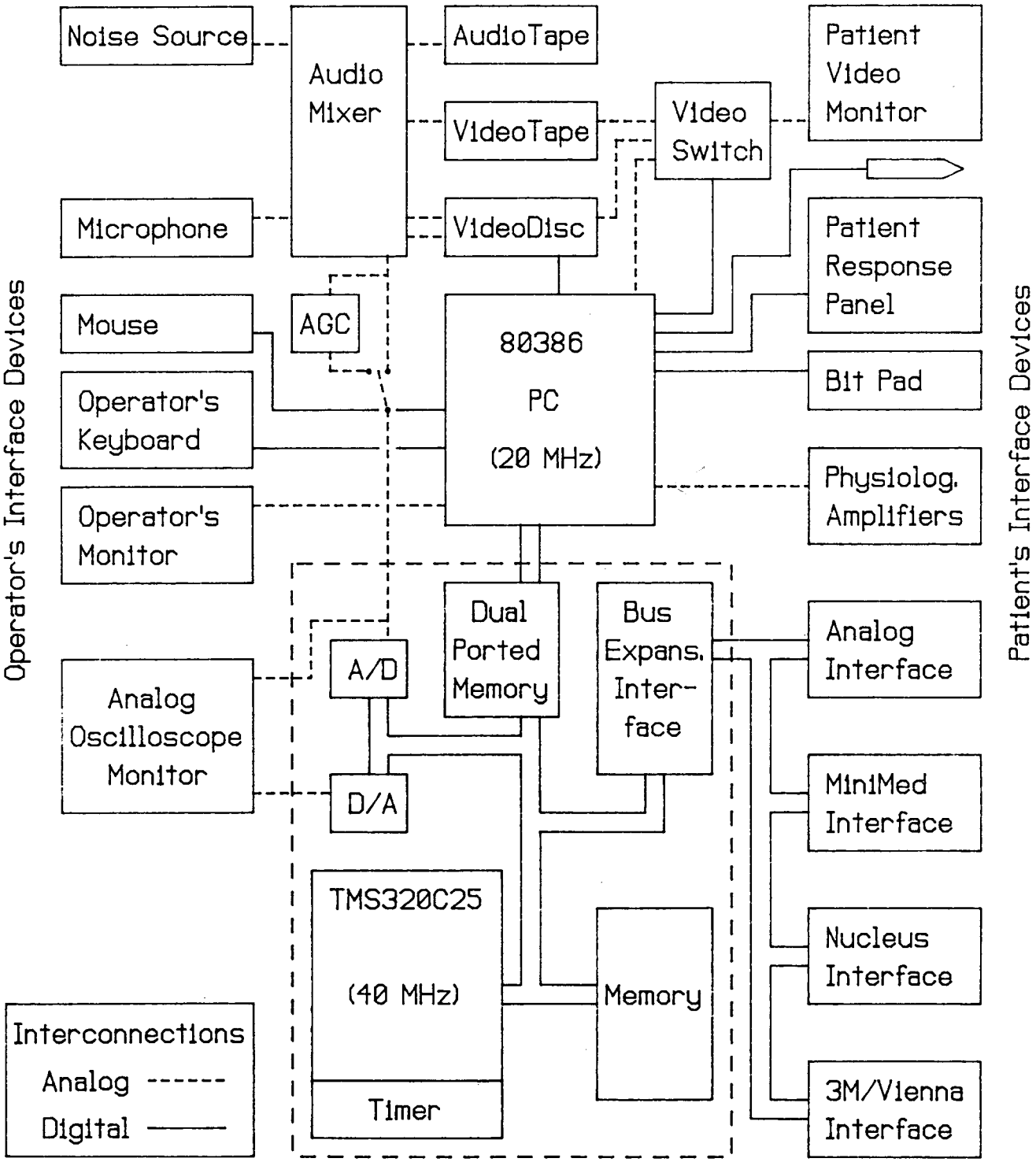



Fig. 1. Hardware configuration of the new laboratory system.

tape, video tape, and standard noise generators. All audio signals are controlled and conditioned by an audio mixer. An optional slow-acting automatic gain control (AGC) may be switched into the "front-end" signal path.

Output from the TMS320C25 may be directed to any of several memory-mapped patient interfaces. One is a standard analog interface featuring eight channels of optically-isolated current/voltage drivers. This interface will be used for studies with patients who have percutaneous cables. Our present stimulus isolation unit (Wilson and Finley, 1984) will form the basis for this interface. A second interface is provided for serial transmission of data to the transmitting coil of the new MiniMed prosthesis (see section III of this report). Additional interfaces will allow control of the implanted receivers in the Nucleus and 3M/Vienna auditory prostheses. A brief description of the Nucleus interface is presented below in the subsection on "Preparation for Studies with Nucleus Patients."

Patients will interact with the laboratory system in a variety of ways. The PC will monitor and control the peripheral equipment to implement tests of speech perception or psychophysical performance. Procedures for these tests will be a superset of those already developed for the Eclipse environment. Patients will be able to respond to speech or psychophysical stimuli using a light pen, a response panel with pushbuttons and knobs, or an x-y digital bit pad. Selection of the response modality and the interface(s) used for the presentation of stimuli will, of course, depend on the particulars of each test and prosthesis system. Finally, physiological amplifiers (and associated artifact-rejection circuitry) are interfaced to the PC for measurements of electrically-evoked brainstem and scalp potentials.

## Status of System Development

Most of the hardware shown in Fig. 1 already has been obtained from commercial sources or designed and built. Two Dell 20MHz, 80386 machines have been purchased using RTI capital equipment funds. One machine will soon be placed in the Cochlear Implant Laboratory at Duke and the other will remain at

RTI for development of software for the Duke machine. In addition, we have obtained a TMS320C25 coprocessor board for the Duke 80386 machine. This coprocessor has an on-board 16 bit A/D and D/A conversion system, along with 128k words of on-board memory. The PC and the TMS320C25 communicate via dual-ported memory, which allows a user to view and modify data and program memories directly, even during coprocessor program execution. A bi-directional interrupt/handshaking facility is available for synchronizing interactions and information transfers between the PC and TMS320 microprocessors. The particular coprocessor board selected for use in our laboratory system has a hardware expansion connector that buffers the TMS320C25 data, address, and control buses off the board for interfacing to additional hardware. This feature will facilitate the communication protocols for TMS320C25 control of the four prosthesis system interfaces shown in the lower-right corner of Fig. 1. A specifications sheet for the selected TMS320C25 coprocessor is presented in Appendix 2.

Additional elements of the laboratory system are in various stages of design and construction. A variety of equipment for patient responses is in place and functional. In addition, the necessary hardware interfaces and software have been developed for use with the new laser videodisc materials from the University of Iowa (Tyler et al., 1987) and from the City University of New York (Boothroyd, 1988).

Next, a prototype system has been designed and constructed for measurements of electrically-evoked brainstem and scalp potentials. The system includes circuitry for full isolation of several channels of input. In addition, circuitry is provided for artifact rejection for both pulsatile and sinusoidal stimulus waveforms. Development of averaging and analysis software is under way, and we expect that the entire system will be ready for use in studies with implant patients this September.

Finally, we are beginning the job of converting Eclipse software for use with the new 80386 and TMS320C25 processors. We have purchased Fortran and C-language compilers for the 80386 and a separate C-language compiler for the TMS320C25. Most of the existing Eclipse software for signal processing will

be converted from Fortran V to C or TMS320C25 assembler for real-time execution. Much of the remaining Fortran V software will be converted to Fortran 77 for execution on the 80386 machine. This last task is a modest undertaking and should be completed quickly. The task of converting the signal-processing software is much larger and therefore will require more time to complete. We expect that all hardware and software elements for the new laboratory system will be fully functional by mid-December, 1988. The new system will tremendously enhance our capabilities to evaluate alternative speech processing strategies for cochlear implants.

## Preparation for Studies with Nucleus Patients

Although the new laboratory system will not be fully functional until this winter, the development of certain elements of the system is being accelerated to allow planned studies with two Nucleus patients this September. Jim Patrick of Cochlear Pty. Ltd. (manufacturer of the Nucleus prosthesis) visited RTI at the end of this quarter to assist in the design of the interface to control the implanted receiver of the Nucleus device. Agreement was reached on a design using an additional TMS320C25 processor to provide timing signals for modulation of the 2.5 MHz carrier used in the Nucleus transcutaneous transmission system (TTS). Use of the TMS320C25 processor will provide much more flexible control over the implanted receiver than is now possible with the dedicated hardware of the transmitter in the clinical device.

The design of the hardware and software links for the Nucleus interface is under way and the additional TMS320C25 has been ordered. We expect to complete the interface in late August, 1988. Its operation will, of course, be fully validated with bench tests using a model of the implanted receiver before application in studies with patients. Mr. Patrick has graciously provided a model for this purpose.

## III. Development of a Next-Generation Auditory Prosthesis

We have been collaborating with UCSF in the development of a next-generation UCSF auditory prosthesis. In particular, we have played major roles in the specification and design of the speech processor and transcutaneous transmission system (TTS) for this new device. The design of these two elements of the system is based on the results from our studies comparing analog and pulsatile coding strategies in tests with individual implant patients. As indicated in detail elsewhere (QPRs 6 and 9, this project; Wilson et al, 1988a-c), the major conclusions from these studies are that

1. Different processing strategies can produce widely different outcomes for individual implant patients;

2. Interleaved pulses (IP) processors are far superior to the tested alternative processors for at least two patients with psychophysical findings consistent with poor nerve survival;

3. The performance of IP processors strongly depends on the selection of processor parameters;

4. Use of a TTS designed to support an IP processor (e.g., a TTS with eight channels of current-controlled outputs) is likely to produce results that are better than those obtained with the limited TTS of the present UCSF/Storz prosthesis;

5. Processors other than the IP processors can be superior for patients with psychophysical signs of good nerve survival and for whom an IP processor cannot be fully optimized;

6. One such processor is the compressed analog (CA) processor used in the UCSF/Storz prosthesis; and

7. Substantial gains in speech understanding can be made by (a) selecting the best type of speech processor for each patient and (b) using implanted and external hardware capable of supporting a range of different processing strategies.

The next-generation UCSF prosthesis, to be produced by MiniMed Technologies, will be capable of supporting both the CA and IP processing strategies and also will have a TTS that provides up to eight channels of current-controlled outputs for intracochlear stimulation. In fact, the TTS will have unprecedented flexibility for such a system. The current drivers in the system are fully isolated and can be individually programmed to provide outputs in 3 percent increments between 2 and 2000 μA. The drivers can also be instructed to provide a zero output or negative outputs (the direction of current flow is controlled by a switch matrix). All eight driver outputs can be simultaneously updated every 77 μsec (13kHz sampling rate) and a smaller number of driver outputs can be updated at higher rates. For example, one channel can be updated every 12.3 μsec (81 kHz sampling rate). This feature permits a mixture of sampling rates for the various stimulation channels which might be most useful for the generation of stimuli for CA processors. In particular, high frequency analog stimuli can be "reconstructed" at high sampling rates for basal electrode channels while low frequency stimuli can be reconstructed at low sampling rates for apical channels. Finally, the outputs of the current drivers can be connected (under external control) to form different electrode coupling configurations. Both the monopolar and radial bipolar configurations will be supported, as will "hybrid" mixtures of the two. In addition, a longitudinal bipolar configuration can be implemented if nonsimultaneous stimuli are used. All outputs from the current drivers are capacitively coupled to the selected intracochlear electrodes to ensure charge balancing of the stimuli.

The significance of the new UCSF device for the present project is that we will have access to patients with a highly-transparent TTS. This will allow us to evaluate an extremely wide range of processing strategies and electrode coupling configurations in tests with individual patients without

having to use a percutaneous cable. Thus, we will be able to retain most of the flexibility provided by the cable while eliminating the potential complications of cable use.

We expect that the new device will be available for implantation in the fall or winter of 1988.

## IV. Plans for the Next Quarter

Our plans for the next quarter include a visit from Dr. Sigfrid Soli on August 21-23. Dr. Soli will install at our site a sophisticated software package he has developed for various types of feature-transmission analysis of results from tests of vowel and consonant identification. Dr. Soli also will instruct us on the use of this software.

In addition to Dr. Soli's visit, we have the following plans for the next quarter:

1. Continue our work to upgrade the Cochlear Implant Laboratory at Duke, as indicated in section II of this report;

2. Conduct additional studies with implant patients, including studies with two patients implanted with the Nucleus device and two patients implanted with the UCSF/Storz device;

3. Present a report of project results in an invited paper for the World Congress on Medical Physics and Biomedical Engineering, to be held in San Antonio on August 6-12; and

4. Continue preparation of the four manuscripts listed in the Introduction of this report.

## V. References


Tyler, R.S.: Iowa audiovisual speech perception laser videodisc. University of Iowa, 1987.

Wilson, B.S. and C.C. Finley: Speech processors for auditory prostheses. Second Quarterly Progress Report, NIH project N01-NS-3-2356, 1984.

Wilson, B.S. and C.C. Finley: A computer-based simulator of speech processors for auditory prostheses. ARO Abstracts, 8th Midwinter Research Conference, p. 109, 1985.

Wilson, B.S., C.C. Finley, J.C. Farmer, Jr., D.T. Lawson, B.A. Weber, R.D. Wolford, P.D. Kenan, M.W. White, M.M. Merzenich and R.A. Schindler: Comparative studies of speech processing strategies for cochlear implants. Laryngoscope, Vol. 98: October, 1988a, in press.

Wilson, B.S., C.C. Finley, D.T. Lawson and R.D. Wolford: Speech processors for cochlear prostheses. In the special issue of Proc. IEEE on "Emerging Electromedical Systems," October, 1988b, in press.

Wilson, B.S., R.A. Schindler, C.C. Finley, D.K. Kessler, D.T. Lawson and R.D. Wolford: Present status and future enhancements of the UCSF cochlear prosthesis. In P. Banfai (Ed.), Cochlear Implants 1987, Springer-Verlag, 1988c, in press.

Appendix 1

Summary of Reporting Activity for the Period of
March 26 through June 27, 1988
NIH Contract N01-NS-5-2396

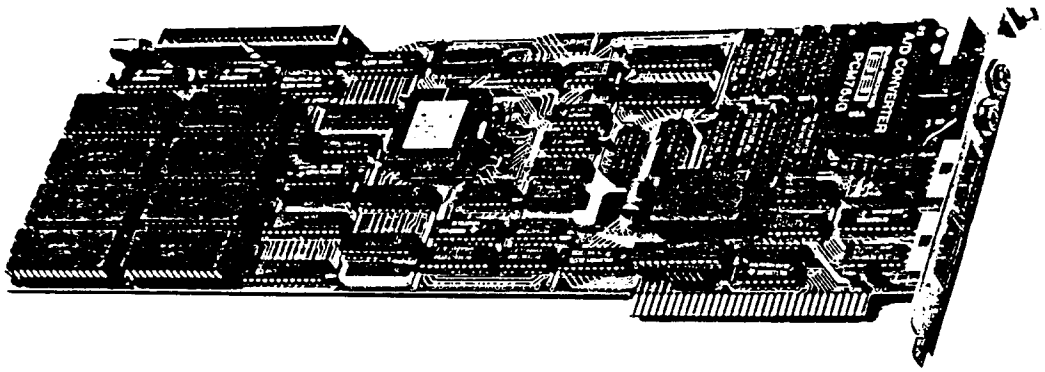
Reporting activity for the present quarter includes the following:

Wilson, B.S.: Various coding schemes used. Invited presentation at the Cochlear Implant Consensus Development Conference, National Institutes of Health, May 2-4, 1988.

Soli, S.D. and B.S. Wilson: Within-subject comparisons of analog and pulsatile speech processors for cochlear implants. Invited paper accepted for presentation in the special session on "Speech processing aids for the handicapped," at the Annual Meeting of the Acoustical Society of America, Honolulu, Hawaii, November 14-18, 1988 (Abstract in press).

SPECTRUM

# TMS320C25
## Development System




The TMS320C25 Development System is an IBM PC plug-in board offering full support for digital signal processing applications using the TMS320C25 from Texas Instruments.

### Features

- IBM PC, XT, AT plug-in board.
- TMS320C25 processor.
- High speed 16 bit A/D and D/A.
- Sample-and-hold on input.
- 128 Kwords on-board memory capacity.
- Monitor software including single step, breakpoint, and full speed operation.
- Hardware expansion connector.

The TMS320C25 Development Systems offers a general purpose solution to most DSP development needs.

The system runs at full speed (40 MHz) with 35ns on-board RAM and a general purpose on-board timer.

The PC board is configured to handle either analog, serial, or parallel I/O. The hardware expansion connector allows access to the address, control, and data busses of the TMS320C25. The system also supports multi-board configurations.

True dual-ported memory allows users to view and modify program or data memory while the TMS320C25 is running. The host processor and C25 processor can interrupt each other for efficient real time operation.

### Development Support

To assist the user in developing applications the system comes with a complete debug monitor which provides single step, breakpoint, and full speed operation. The debug monitor also allows the processor registers and memory to be examined and modified, and includes a disassembler.

Sample programs familiarize the user with program development and give good examples of how a TMS320C25 based system can be used in the PC environment. These sample programs include a 128 point FFT, a FIR filter, and a data logger. Source code for these programs is included as part of the system documentation. Spectrum also supplies TI's Macro Assembler/Linker for the TMS32020/C25 processors.

### Data Acquisition and Analysis Software

Spectrum offers **SignaLink320** which manages real-time data acquisition and display of signals for the TMS320C25 Development System.

SignaLink320 acquires and stores signals in the on-board memory of the system, where they can be displayed, reprocessed by the hardware, or loaded into a PC file. The software provides high speed pan and zoom, cursor display, peak detection, signal editing, and other functions which allow the user to quickly evaluate large data files.

SignaLink320 also provides an interface to the **DADISP** data analysis spreadsheet package from DSP Development Corp. For further information, please refer to the DSP Data Acquisition and Analysis Software data sheet. Demo disks are available.

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## SPECIFICATIONS

1. **Processor**
   TMS320C25 running at 40 MHz clock rate.
   16-bit processing including 16 x 16 hardware multiplier, and 32 bit ALU.
   544 words (16 bit) of internal RAM.
   8 auxiliary registers for address pointers and loop counters.
   Internal interval timer.

2. **Memory**
   System comes with 16 Kwords 35ns RAM.
   Supports up to 128K words (16 bit) of on-board memory, link programmable for RAM or EPROM.
   Fast access to memory from IBM PC via I/O ports inserting only one extra wait cycle to TMS320C25 operation for each transfer.
   Selectable wait state (0 or 1) to suit memory speed.

3. **Analog I/O Clocking Options**
   Main sample clock source is a 16 bit on-board interval timer, clocked at 10 MHz to provide precise time reference down to 153 Hz.
   Software generated sampling can be used.
   External clocking that can be easily linked to the internal clock of another board for synchronous sampling.
   Sample clock can be used as processor interrupt.

4. **Analog Input**
   16 bit A/D, conversion time 17 µs, or
   12 bit A/D, conversion time <10 µs.
   Voltage range ± 10V.
   Sample-and-hold on input.

5. **Analog Output**
   16 bit D/A, settling time 3µs.
   Voltage range ± 10V.

6. **Interface to PC Host**
   Option 1: Full handshaking16 bit bidirectional register as port to both processors, with status line signalling.
   Option 2: Block transfers through 1 of 8 selectable I/O spaces. (ports)

7. **Hardware Expansion Connector**
   TMS320C25 data, address, and control busses buffered to 50 pin expansion connector to facilitate addition of extra hardware by user.

8. **Serial Interface**
   Two separate 10 pin connectors for serial input and output data, clock and control.
   Cross-connection of cables possible for board linking.

9. **Physical**
   Full length IBM PC plug-in card.
   Dimensions: 13 3/8"l x 4 1/2"h x 5/8"d.

10. **Electrical**
    Power consumption: 5 volts @ 2 Amps from PC supply.

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**ORDERING INFORMATION:**

| | | Part No. |
|---|---|---|
| **Description:** | TMS320C25 Development System | 600-00103 |
| | Documentation Only | 601-00120 |
| | * TMS32020/C25 Macro Assembler/Linker from Texas Instruments | 100-00090 |
| | * SignaLink320 | 600-00121 |
| | * DADiSP | 100-00054 |

* These products are not included with the TMS320C25 Development System, and are available separately from Spectrum Signal Processing Inc.



D/S 601-00139-AB

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