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Speech Processors for Auditory Prostheses

NIH Contract N01-DC-2-1001

Wide-bandwidth Amplifier for Recording Scalp Potentials Generated by Cochlear Implants

submitted by

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A. Introduction to the QPR

Work performed with the support of this contract is directed at the design, development, and evaluation of sound-processing strategies for auditory prostheses implanted in deaf humans. The investigators, engineers, audiologists and students conducting this work are from four collaborating institutions: the Massachusetts Institute of Technology (MIT), the Massachusetts Eye and Ear Infirmary (MEEI), Boston University (BU) and the University of North Carolina at Chapel Hill (UNC-CH). Major research efforts are proceeding in four areas: (1) developing and maintaining a laboratory-based, software-controlled, real-time stimulation facility for making psychophysical measurements, recording field and evoked potentials and implementing/testing a wide range of monolateral and bilateral sound-processing strategies, (2) refining the sound processing algorithms used in current commercial and laboratory processors, (3) exploring new sound-processing strategies for implanted subjects, and (4) understanding factors contributing to the wide range of performance seen in the population of implantees through psychophysical, evoked-response and fMRI measures.

In this QPR, we describe the design of an amplifier system for recording stimulus artifact potentials from the scalp of cochlear implant subjects using transcutaneous radio-frequency linkage systems. The design is described in detail and includes fabrication information intended to facilitate the reproduction of the system in other laboratories. A fully functional amplifier system, demonstration software, and computer-aided design (CAD) files have been provided to the contract office of NIDCD.

B. Background for Amplifier Design

The amplifier system described in this quarterly report is designed specifically for the recording of stimulus artifact potentials from the scalp of cochlear implant patients. Most implant patients today have commercial medical devices, which employ transcutaneous transmission systems in order to convey power and command data across the skin into the implanted receiver/stimulator system. Such links typically employ radio-frequency (RF) transmissions at relatively high power levels, thus introducing significant high-magnitude, high-frequency (2-49 MHz) electromagnetic contamination on the scalp.

The presence of this RF contamination complicates the recording of scalp potentials on several accounts. First, the magnitude of this RF energy is much greater than the typical EEG/EMG activity observed on scalp electrodes with the implant device unpowered. These large signals thus force conventional biological amplifier systems to be operated at lower than desired gain levels in order to avoid saturation. This reduction in amplifier gain, combined with a higher noise floor, makes averaging of signals buried in the noise more difficult.

Low-pass filtering is often employed to reduce the size of the contaminating RF signals. Such filtering can produce several complications, including: (1) time smearing of stimulation artifact, which may subsequently overlap with and obscure longer latency biological responses which are of interest in the recording, and (2) significant amplitude distortion and ringing of electrical stimulation artifact that may be useful for monitoring device function, especially when pulses with short phase durations are used. If filtering is not employed, conventional amplifier systems are also susceptible to radio-frequency (>1 MHz) interference (RFI) which may produce spurious DC offset signals in precision integrated amplifiers due to RFI coupling to the input, output and supply leads of the amplifier. Placement of pi-section filter networks on the input of a differential amplifier to address this problem commonly results in reduction of input impedance due to shunting and loss of common-mode rejection ratio (CMRR) due to mismatching of symmetrical circuit component values.

An additional shortcoming of conventional biological recording amplifiers is their fairly long duration and often asymmetrical recovery from hard saturation depending on the polarity of the artifact inducing the saturation. These nonlinear behaviors of the active electronics arise principally from a combination of local on-chip heating and use of different circuit configurations for driving amplifier outputs toward either the positive or negative supply rails. Such saturation behavior is not limited to the output stages alone and can involve earlier gain stages within an individual op-amp. Similar cascading of active stages exists in full multistage amplifier systems, including both gain and filter stages. Saturation in such systems results in even more prolonged recovery as cascaded stages must recover sequentially beginning with the first saturated input stage, then intermediate stages, and finally progressing to the final output stage.

The amplifier system described here addresses these problems in a fairly conventional manner by using components with much greater signal bandwidths than are normally employed and by employing circuit design techniques to minimize problems commonly encountered in realistic recording environments. The result is a wide-bandwidth amplifier system suitable for use in the high RFI environment associated with a cochlear implant patient.

While the original objective of this quarterly project report was to provide design information on the latest implementation of our wideband recording system suitable for both artifact and biological potential recording, the present design has proven unsuitable for biological potential recording due to large baseline noise levels generated by power supply transients, computer bus noise, and a hardware amplifier instability at high gain. Each of these factors may be addressed through modification of the physical packing of one one board. The design is in revision and will be supplied to the contract officer at a future date. The present system performs well in the recording of short phase duration electrical artifacts in the predence of large RF fields.

C. General Description and Block Diagram

The general amplifier system consists of three components, including a headstage, a computer PCMCIA interface stage, and a multifunction data acquisition card (PCMCIA style) installed in a laptop computer. The data acquisition card (National Instruments NI-6062E) is discussed as part of the amplifier system because of its integrated programmable-gain stage that is used in conjunction with the other system components.

Overall the system design, summarized in the block diagram Figure 1, provides (1) wide bandwidth operation to prevent temporal smearing of electrical artifact, (2) variable gain control to allow maximization of dynamic range of various recording environments, (3) low-noise front-end design, (4) active guarding of input leads from the subject, (4) facilities to allow impedance measurement of subject electrodes, (5) fully-differential function of both input and output of the headstage to maintain high common mode rejection, (6) fast recovery from hard saturation of any gain stages, and (7) electrical isolation for subject safety and noise minization by battery operation.

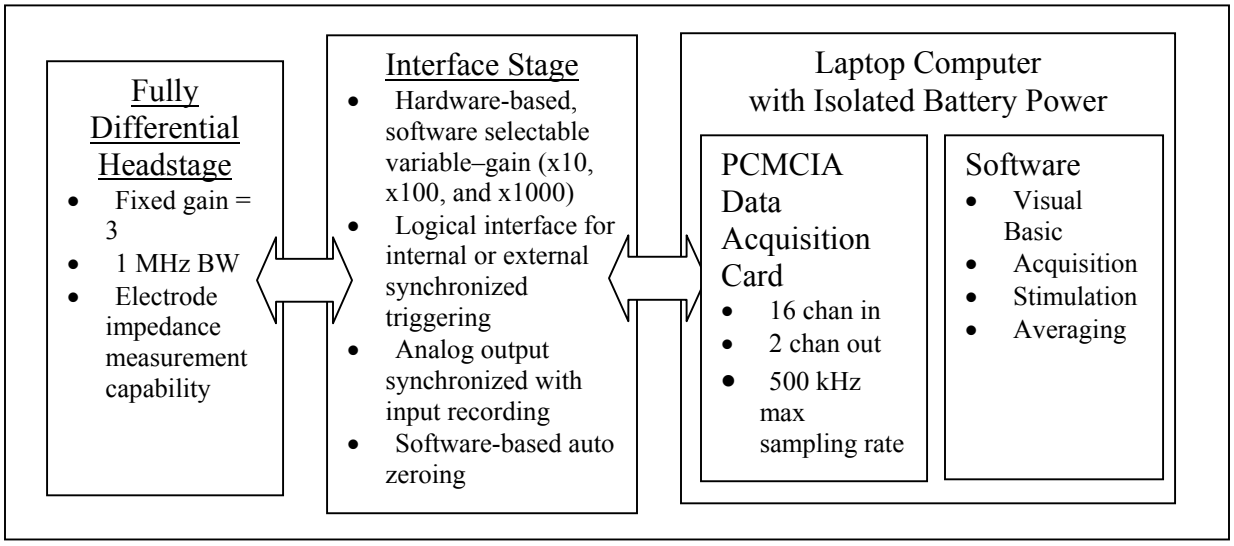


Figure 1. Block Diagram of the General Amplifier System

The subsequent paragraphs describe each section in general terms. Schematics for each are in Section II. The description begins with the headstage amplifier and proceeds to the data acquisition and processing stages.

The headstage amplifier described in the block diagram in Figure 2 features a classic three-op-amp instrumentation amplifier design with several enhancements. The two input buffer stages are very high-speed, low-noise BB OPA627 devices, which have signal gain-bandwidth ratings out to 16 MHz and input noise characteristics of 4.5nV/√Hz thus providing RF noise immunity and low input noise. Inputs to each of these buffers are electrostaticly protected by normally reversed-biased diode clamps to

the positive and negative supply rails. Each buffer output is also connected to a fully-differential, high-speed, low-noise TI THS4130 amplifier through an infinite-gain, multiple-feedback, low-pass filter network. The cut-off frequency of this two-pole network is adjusted to 1 MHz, thus limiting the passage of RF frequencies through the rest of the amplifier system. The outputs of the THS4130 drive two output lines in a differential manner in the cable leading to the PCMCIA interface board. A manually adjusted DC offset is also applied to the THS4130 output stage reference line so that the offset may be trimmed with input leads shorted. The headstage operates with ± 5volt supply rails. The instrumentation amp gain is set to a maximum of approximately 3 so that large electrical artifacts may be recorded by the system without saturation. This gain is later reduced to approximately 2.7 due to a resistive divider spanning the coupling cable between the headstage and the PCMCIA interface to reduce cable ringing, but reducing gain by 0.9.

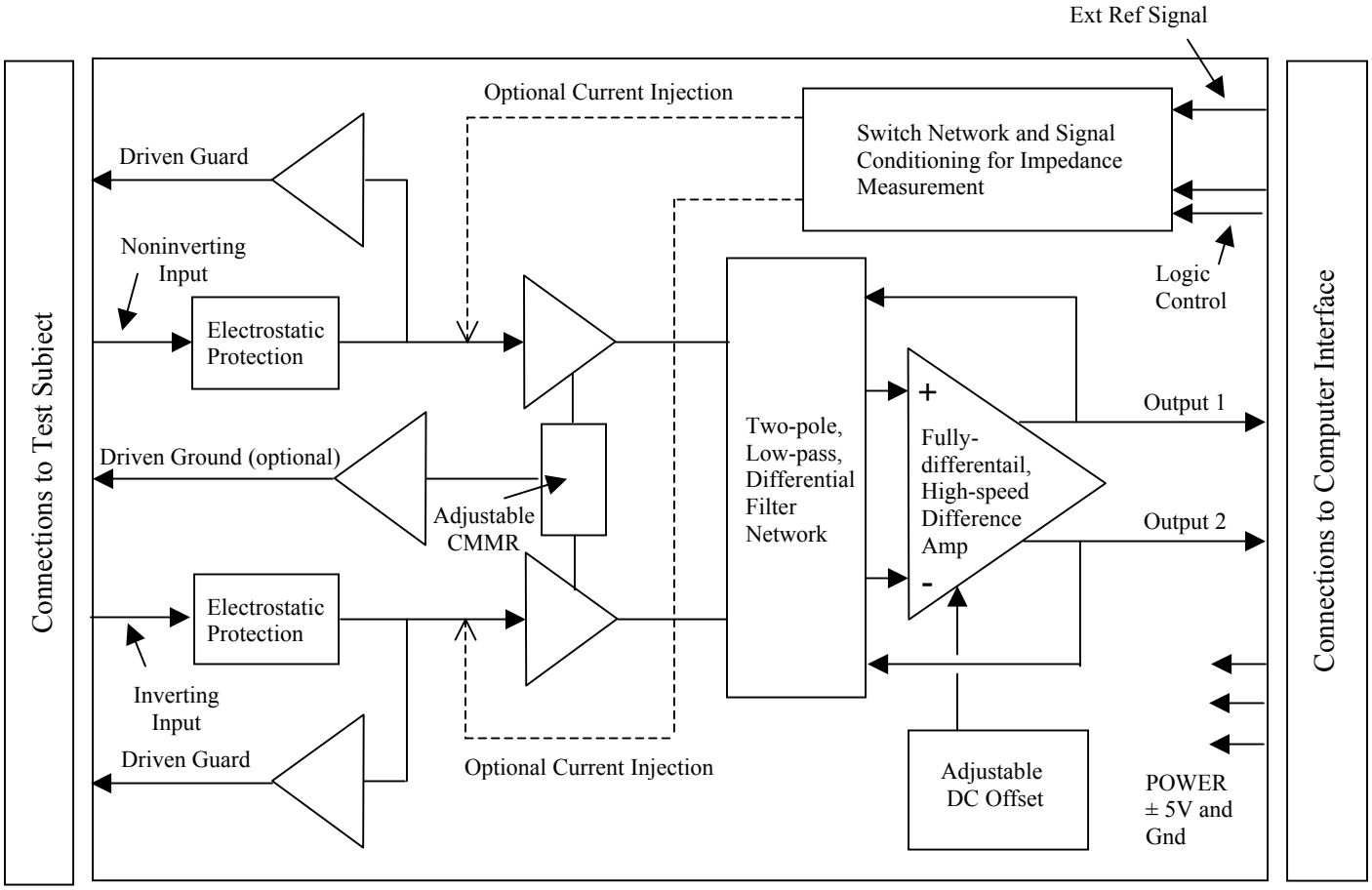


Figure 2. Block Diagram of the Headstage Design

In addition, the output from each of the OPA627 buffers in the headstage drives a separate unity-gain buffer (OPA627), which in turn is connected to the respective input lead shield to provide an active guard for the shielded electrode cables. A CMOS switching network is also configured on the inputs to the buffers so that recording electrode impedances may be measured under software control for each subject electrode. An optional (hardware-selected) active ground driver is also available to increase

common mode rejection of signals on the active electrodes from the test subject. The active ground feature, if used in normal recording, is disabled during electrode impedance measurements. The headstage is connected to the computer interface using a single, eight-lead, shielded CAT 5e network patch cable. Because the cable shield is actively used to convey supply ground to the headstage, unshielded patch cables cannot be substituted. Various lengths of this cable (1m, 2m, 3m) may be used depending on the physical recording situation. The cable carries power, differential output signals, logic control lines and a reference signal for impedance measurements.

The PCMCIA interface described in Figure 3 decodes the differential output of the headstage into a single-ended signal using a unity gain instrumentation amplifier to maintain common mode rejection. The resulting signal is then amplified through two cascaded gain stages, each with a gain of 10. Consequently, on the board are three simultaneous signals at gains of 1, 10 and 100, each of which is routed to a separate analog input on the data acquisition card. Combined with the net headstage gain of approximately 2.7x, available hardware gains are roughly 2.7x, 27x and 270x. Software selection of the gain of the PCMCIA interface is accomplished by selection of which analog input channel is used for data collection.

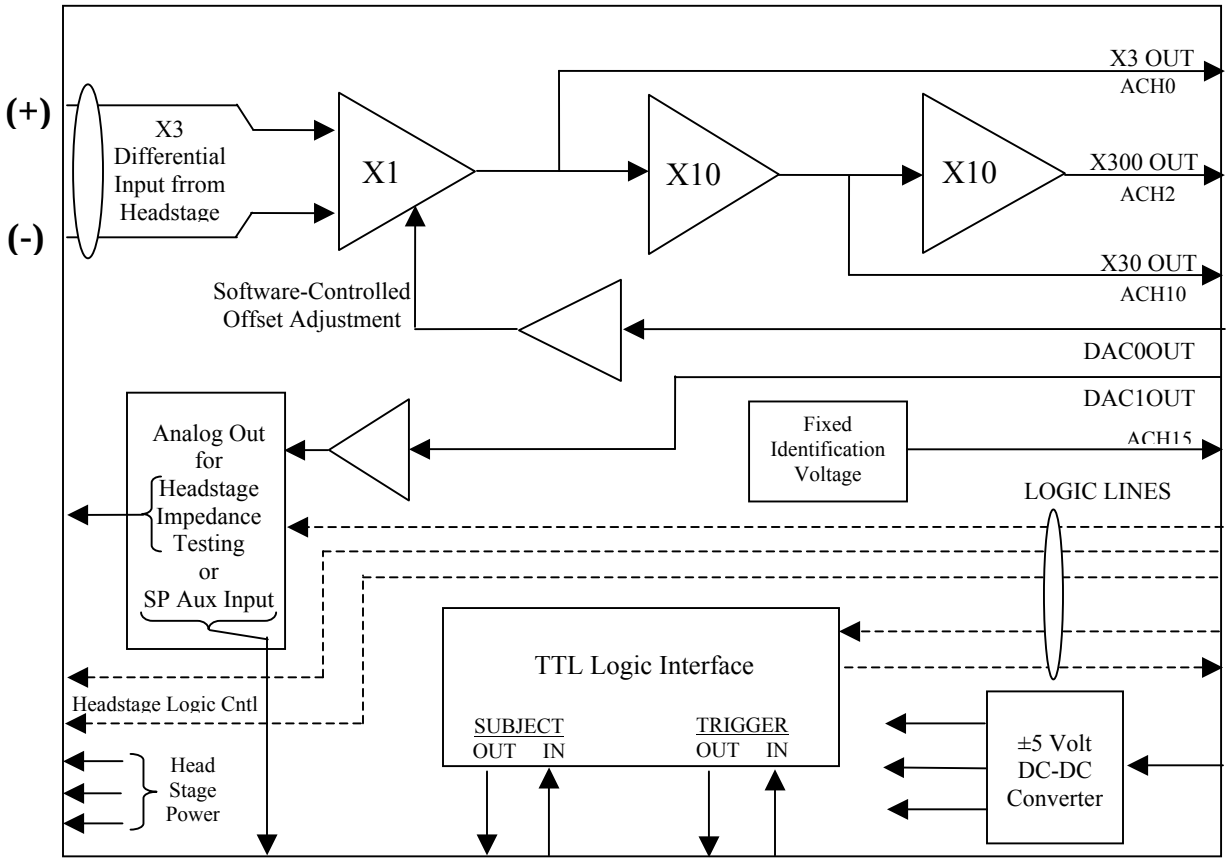


Figure 3. Block Diagram of PCMCIA Interface

Analog output channels for the data acquisition card are used for two purposes. One (DAC1OUT) is used as a general purpose output signal that may under software control of a relay be routed to a buffered AUX OUTPUT connector for stimulus delivery or may be directed internally to the headstage for use in impedance measurements. The other analog output (DAC0OUT) is connected through a resistive divider and buffer amp to the output reference of the initial 1x differential instrumentation amp stage. By adjusting the DAC0OUT level under software control, DC offsets may be removed from the analog input signal being monitored. By holding the DC reference level constant during data recording, the high-pass characteristic of the recording system extends effectively to DC or zero frequency.

The PCMCIA interface also contains two additional ports for internal or external synchronization of input and output data streams. The system may output a trigger pulse (TTL) to control external hardware or receive a trigger pulse (TTL) from external hardware. Another port provides two sets of logical lines, which may be independently configured as inputs or outputs for various experimental tasks such as controlling equipment or monitoring subject responses.

The National Instruments DAQCard 6062E data acquisition system is described in the block diagram shown in Figure 4. This system is a multifunction data acquisition system in a PCMCIA package. The 6062E features 16 single-ended or 8 differential analog input channels with 12-bit resolution. The maximum sampling rate is 500 kHz for one channel, 250 kHz for 2 channels, and 166.7 kHz for 3-channel operation assuming equivalent sampling duty cycles across channels. On-board amplification of 0.5, 1, 2, 5, 10, 20, 50, 100 operates under software control to scale the full-scale input range from ±0.05 to ±10.0 volt operation. There are two 12-bit analog output channels with maximum output rates of 850 kHz. Eight digital I/O lines and two 24-bit timers are also available. Input and output are buffered through separate FIFO's. Data transfers operate on an interrupt-driven basis using low-level drivers provided by the manufacturer.

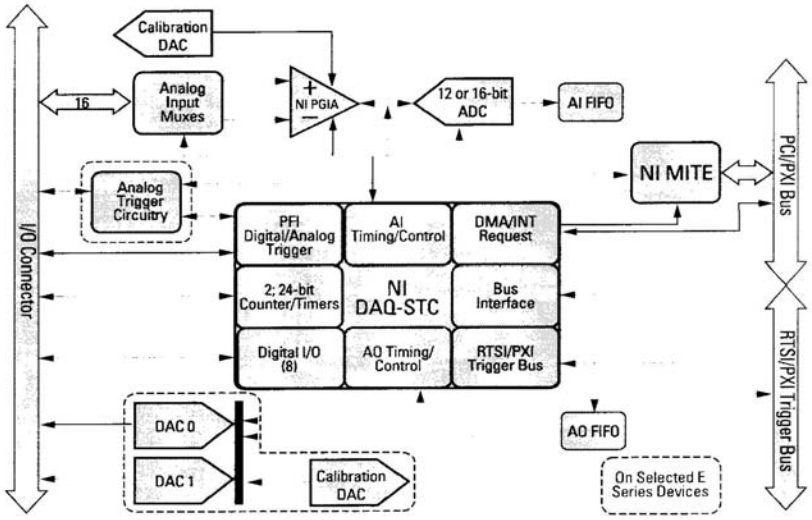


Figure 4. Block Diagram of the National Instruments 6062E Data Acquisition

D. Design Specifications

Note: For the present version of this report the following specifications are design specifications and are not performance specifications. Measured performance specifications will be included in a subsequent revision following anticipated board modifications to reduce supply noise, computer bus noise, and on board oscillations at high gain.

Gain Total gain is determined by the individual gains of three cascaded stages.

Headstage	Fixed gain of approximately 2.7x.
PCMCIA Interface	Software selectable hardware gains of 1, 10 and 100.
DAQCard	Software selectable hardware gains of 0.5, 1, 2, 5, 10, 20, 50, 100.

Consequently, under software control, gain may vary from approximately 1.35 to 27,000.

Bandwidth Approximately 700 kHz.

Slew Rate 4 V/μS

Saturation Recovery Approximately 20 usec from hard saturation.

Noise Approximately 6.2 nV/√Hz

Note: In the present design this targeted noise level is significantly compromised due to switching noise from a DC-DC converter. This issue is currently being addressed.

Input Impedance > 10 megohms

Common-Mode Rejection >90 dB at 1kHz.

E. System Installation and Operation of Demonstration Software

Recommended System Requirements:

Laptop PC with PCMCIA Port, CD Player, minimum 256 Mbytes of memory
Windows 2000 or XP
National Instruments DAQCard 6062E (provided in hardware kit to contract officer)

WARNING: The present hardware design draws 250mA continuously from the 5V supply lines available on the 6062E DAQCard. This is in addition to the specified current drain for the 6062E card itself (340 mA typical; 750 mA maximum). Experience has shown that not all laptop computers are capable of supporting this current drain from the internal bus of the machine. The present system has been developed on the Dell Inspiron 7500 platform and has been successfully installed and run on the IBM Thinkpad. Various models of the Dell Latitude series have behaved marginally, as have older generation laptop systems.

There are two hardware/software components that must be installed to operate the amplifier system. They should be installed in the following order:

1. National Instruments DAQCard 6062E and supporting software including (a) the NI Measurement and Automation environment which registers the data acquisition card in the Windows operating system and (b) the NI-DAQ Driver Software Revision 6.9.3. The software was developed on this platform and has not been evaluated or tested in later versions of the NI software. A CD containing the NI setup code is included in the folder at the end of this section. Insert the CD and execute the SETUP code contained in the top-most folder on the CD. Follow the software instructions to load the NI-DAQ Drivers. This is a protracted process, but continue to select the standard defaults.

At the completion of this process verify that the National Instruments software and hardware have been properly installed. Do this by selecting Start➔Programs➔NI Instruments➔Measurement & Automation. If the Measurement and Automation software is not found, first reboot the system. Then if Measurement & Automation is again not found, repeat the above installation process.

In addition to the Measurement and Automation system, a separate documentation module about the NI-DAQ driver software is also installed. This package may be accessed by the selection sequence Start➔Programs➔NI Instruments➔NI-DAQ. Although the NI-DAQ drivers are not the most current version of support software available from NI, they are the drivers used by the present demonstartion code.

After the NI Measurement and Automation Explorer opens, expand Devices and Interfaces under My System in the configuration panel. On expansion the DAQCard 6062E should be seen. For the demonstration software to operate properly, the 6062E

MUST be installed as Device 1. If other NI devices are installed as Device 1 in lieu of the 6062E, power the system down, physically remove the interferring NI card(s) from the system and reboot. Repeat the reboot process until the 6062E is registered as Device 1.

2. The next item to install is a simple demonstration program that utilizes the amplifier system for its input. This program is provided in executable form only and is intended to serve as a test platform for the amplifier hardware. A CD containing setup code for this demonstration program is also included in the folder at the end of this section. . Insert the CD and execute the SETUP code contained in the INSTALL folder on the CD. Follow the software instructions to load the IMPLANT_AMP code, version 1_1.

3. Finally, configure the amplifier hardware as follows:

- First, connect the HEADSTAGE to the PCMCIA INTERFACE with the blue, shielded network patch cable.
- Next plug the PCMCIA INTERFACE into the NI DAQ-Card in the computer. Please support the weight of the INTERFACE box on some object to reduce stress on the PCMCIA connector. A stack of Post-It Notes or index cards serves nicely for this task.
- Connect to the headstage the three long input leads (black insulation with red, green and black snap connectors) into the appropriate jacks of the same color on the side of the headstge amplifier.

The basic amplifier system is now configured and can be used to record signals applied to the input leads. The subsequent instructions guide the reader through several demonstrations intended to show the basic functionality of the amplifier system.

4. The demonstrations are implemented by applying known test signals to the input leads using a variety of coupling configurations. This process is facilitated by using the Demonstration Interface shown below in Figure 5. The schematic for the Demonstration Interface is also shown in Figure 5 and is comprised of a simple resistive divider network with two inputs and multiple outputs. The input test signals are supplied from the AUX OUT port on the PCMCIA Interface using the red cable to either phono connector, J1 or J2, depending in the desired test signal level to be applied to the amplifier system. The output voltage sensitivities for each input connector, J1 and J2, are

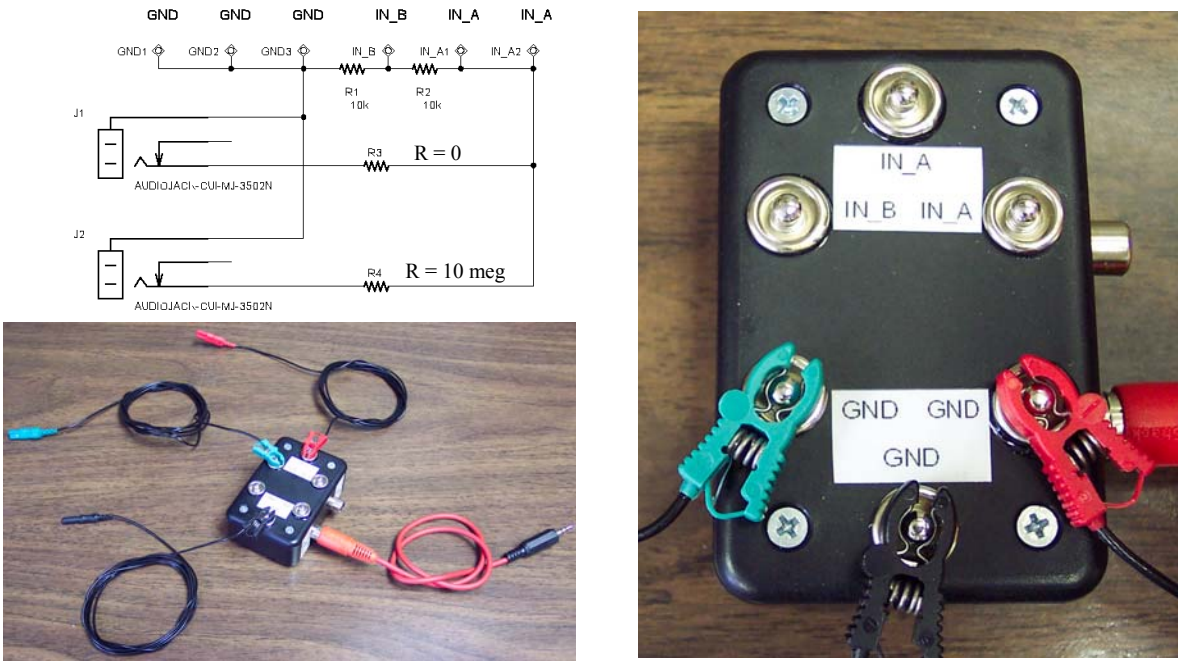


Figure 5. Demonstartion Interface schematic and two views showing connection of electrode leads from the headstage amplifier and test signals from AUX OUT connector. See text for explanation.

labeled on the case. The outputs are made available by six button-type snap terminals mounted on the surface of the plastic case. Of the six outputs there are two IN_A terminals, one IN_B terminal, and three GND terminals. Terminals with similar names are electrically-identical as indicated by the schematic. For instance, the electrode lead connections shown in the close-up view in the right side of Figure 5 short all three input leads to ground.

- First, short the input electrode leads from the headstage to ground by attaching them to the three GND terminals of the Demonstration Interface as described immediately above and as shown in the close-up view of Figure 5.
- Next, route the AUX OUT signal from the PCMCIA Interface to the J1 input on the Demonstration Interface.

4. Launch the demonstration software EVAL program located in the IMPLANT_AMP program group. This program opens with the screen shown in Figure 6.

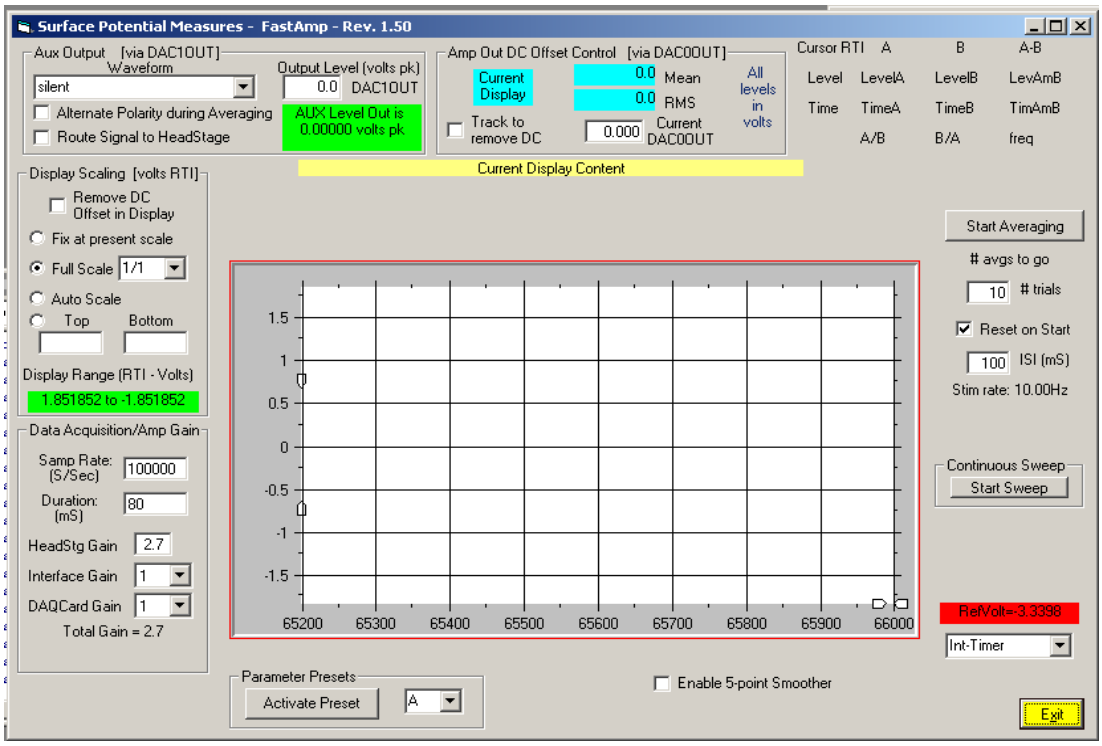


Figure 6. General Screen View of Demonstartion Software

As is evident by the large plotting grid in the middle of the user interface, the software functions primarily to acquire and display data recorded using the amplifier system. Output waveforms may also be presented simultaneously with data acquisition. Both processes are controlled and monitored by the operator by way of the screen controls and data summaries loacted in the perimeter of the screen. Most controls have cursor-activated hints available, which briefly describe the operation of the selected control. The following sections describe the general operation of key features.

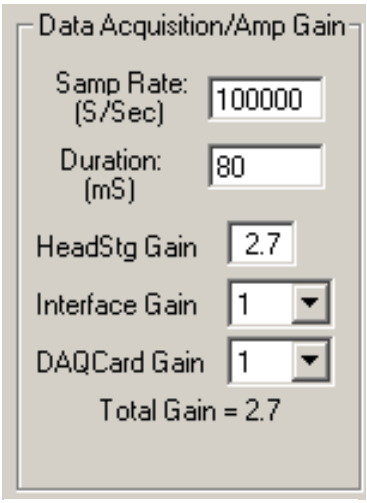


Figure 7. Controls for Data Buffer Duration, Sampling Rate, and System Gain

The controls shown in Figure 7 allow adjustment of the basic data acquisition parameters of sampling rate and time duration of the data acquisition window. These parameters define a floating-point data buffer into which integer data are sampled. The total number of samples in the buffer is the product of the sampling rate and time duration of acquisition. The maximum acquisition rate is 500,000 samples/sec for the NI DAQ-Card 6062E system. The length of the buffer is limited only by available memory.

Gain of the amplifier system is under software control to a large extent. Gains for the PCMCIA Interface may be selected in predetermined increments depending on how the hardware is configured. For the present demonstartion system the available interface gains are 1x, 10x and 100x. As described in the earlier block diagrams these selections are implemented by selecting the appropriate ADC input. The NI DAQCard 6062E also affords control of its on-board amplifier by selection of one of eight gain factors (0.5, 1, 2, 5, 10, 20, 50, 100). Selection of these parameters may also be viewed as modification of the effective full-scale input range from ±0.05 to ±10.0 volt operation of the DAQ-Card. The net gain of the headstage is fixed at approximately 2.7 in the present design. The total hardware gain of the system is the product of the individual gains of the headstage, the interface board, and the NI DAQ-Card. This total gain is computed and displayed in the panel when any one of the individual gains is changed. When a gain change is made on the user interface the new overall gain becomes effective immediately.

The display-scaling panel shown in Figure 8 controls the ordinal scale range and whether DC offsets are displayed. All displayed data are referred-to-the-input (RTI) meaning that measured values are divided by the current total system gain before display. Display scale units are in volts (RTI). The currently active scale range limits are displayed in the lower portion of the panel with green background. The scale range may be adjusted by one of four methods.

- Fix at present scale
- Full scale range equal to ± 5 Volts multiplied by a fractional scale factor set by the pulldown box.
- Autoscaling where by the ordinal scale is continually revised such that the most positive and most negative values in the current display buffer are displayed at 90% of full scale. While convenient for optimally displaying the current data buffer, operation in this display mode can be confusing due to sudden,unnoticed, large changes in scale and overemphasis of low-level and baseline noise signals.
- A final fixed range in which the range limits may be specified manually by keyboard entry in volts RTI.

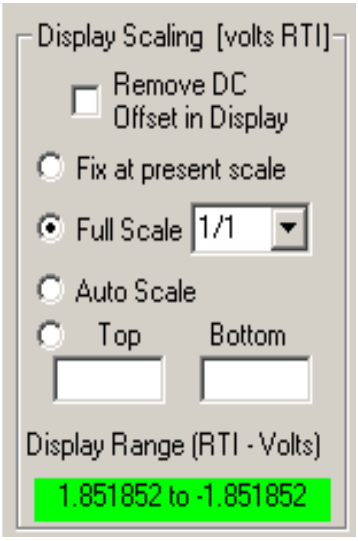


Figure 8. Control for Display Scaling and Offset Removal

The final feature of subtracting the mean value (removal of DC) from the display is selectable. *This process operates only in preparing the next display buffer values and has no influence on hardware operation.* It should not be confused with the *software/hardware tracking* feature described next.

One additional feature that influences processing and display of signals is the automatic tracking and removal of DC offsets by software adjustment of DAC0OUT. The screen controls shown in Figure 9 enable the operator to monitor and control this process. The mean and root-mean-square statistics of the current display buffer are displayed in volts RTI. Selection of "Track to remove DC" enables the adjustment of DAC0OUT to eliminate DC offset from the headstage. The current DAC0OUT level is displayed. Tracking adjustments are made only during periods between buffer acquisitions. The magnitude of single tracking adjustments in DAC0OUT level is variable and is based on the current residual DC offset and the current overall gain of the recording system. Unselection of the feature forces the DAC0OUT level immediately back to zero.

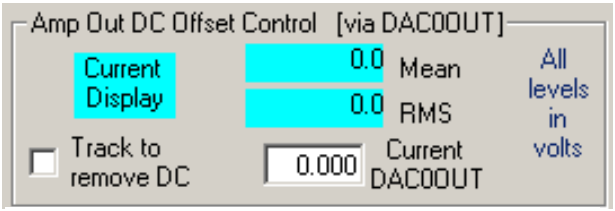


Figure 9. Controls for Removal of DC Offsets with Autotracking

Figue 10 shows the controls for starting and stopping data acquisition. Data acquisition may be made in a continuous sweep mode in which the display window is continually updated one buffer at a time. Selecting Start Sweep begins this process, whereas selection of the same control again stops the process and leaves the last buffer display on the screen. Data may also be acquired and averaged up to a total number of operator specified trials. Subsequent averaging sequences will be either added to the existing result or treated as a new result depending on the selection state of "Reset on Start". When averaging, an interstimulus interval (ISI in mSec) must be specified which is longer than the previously specified display buffer length.

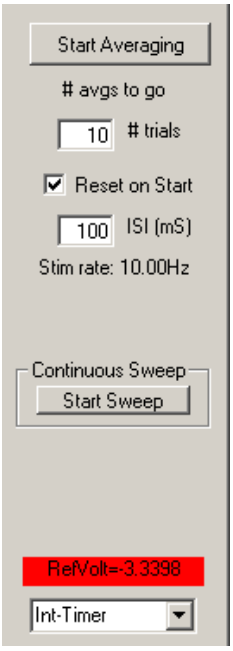


Figure 10. Controls for Data Acquisition using Continuous Sweeps and Averaging of Repeated Trials

The triggering method, either internal based on a timer or external based on an external TTL level signal may be specified by selecting various trigger modes listed in the combination box in the lower right part of the screen.

A reference voltage (RefVolt) is frequently read by the software from the interface module and may serve as indication if an interface module is plugged in, as well as identification of various interfaces which may have different hardware configurations.

As shown in Figure 11, the AUX OUTPUT of the interface module may be used to generate test signals under software control by use of DAC1OUT. The "Waveform" pull-down box provides selection of a number of self-described preprogrammed waveforms. The peak magnitude of the waveform appearing on DAC1OUT may be specified within a ±5.0 volt range. The signal from DAC1OUT may be directed by the operator to either the AUX OUTPUT connector or to the headstage amplifier for electrode impedance measurements. The gain along these alternative pathways differs, consequently the actual output level is calculated and displayed depending on the pathway currently selected. Selection of the "Alternate Polarity during Averaging" feature forces the polarity of subsequent output buffers to be inverted, thus providing in principle zero net stimulus residual for an even number of averaged records.

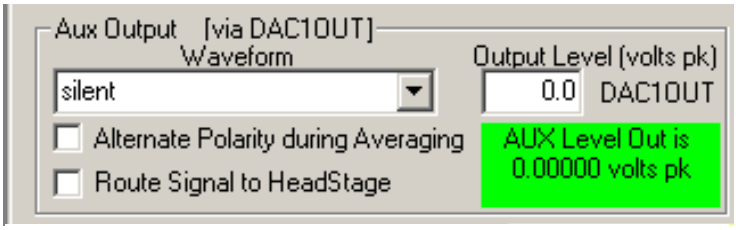


Figure 11. Controls for Specifying Outputs on DAC1OUT

5. At this point the reader will have sufficient information to be able to control the software and experiment with the operation of the amplifier system. To facilitate this process several preset operating conditions have been specified and may be selected and activated by the operator using the panel located at the bottom of the screen and reproduced in Figure 12. The operator may choose to set the parameters individually or use the presets. Once a preset condition is activated all parameters may be manipulated independently from that condition. Note: The default condition is always Preset A, which is the condition of the system on start up and which may be returned to by activating Preset A at any time when data acquisition is not in process.

Figure 12. Controls for Setting Preset Conditions

To begin exploring the operation of the system, use Preset A with the positive and negative input leads shorted to ground. Total gain is approximately 2.7 (2.7x in headstage, 1x in interface, and 1x in DAQCard). Select Start Sweep to begin sampling and then again to stop sampling. A display similar to Figure 13 should be observed. The abscissa is 80 msec in duration and the ordinal range is ± 1.85 volts RTI [±5.0 volts (full analog sampling scale) times 1/1(fractional display ratio) divided by 2.7 (total gain)]. The plotted data approximate a horizontal line at zero magnitude as would be expected for shorted inputs. A small amount of noise can be observed along this line.

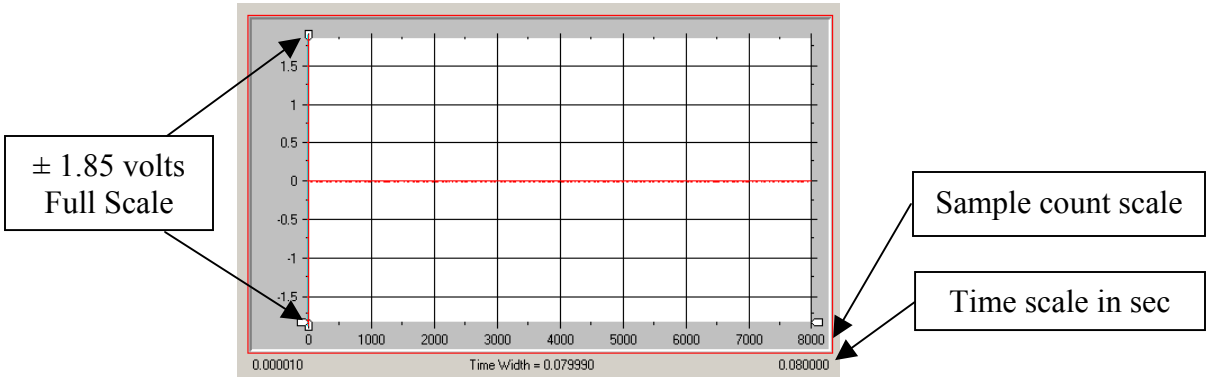


Figure 13. Display Panel for Currrent Data Buffer

This noise can be better visualized by expanding the ordinal range as shown in Figure 14. Change the fractional full-scale value to 1/128 and the display will approximate Panel A below. Selecting Auto Scale expands the ordinal axis further as shown in Panel B.

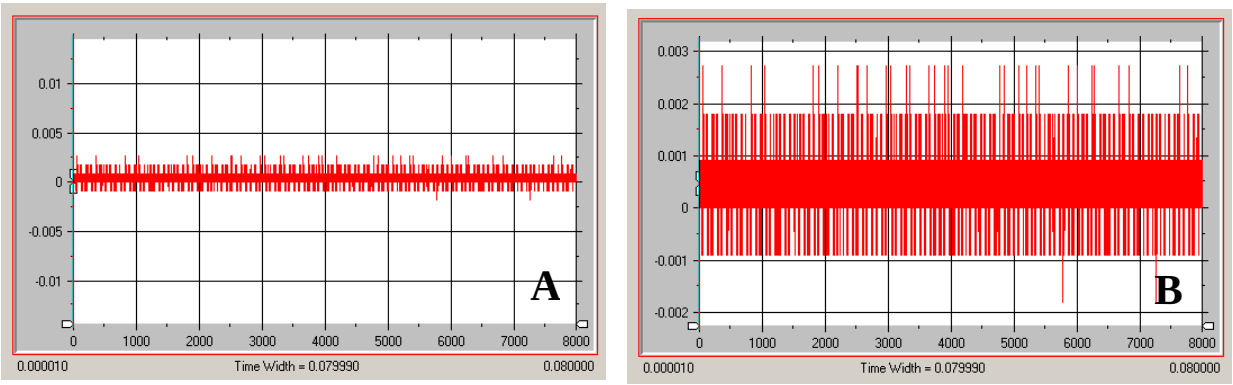


Figure 14. Two Displays of System Noise with Shorted Inputs
Panel A on the left is with fixed ordinal gain. Panel B is with autoscaling gain.

Note that there is a significant quantal content to this noise as seen by the sample data appearing only at six discrete amplitude levels in Figure 14B. This display condition occurs because the hardware gain is very small resulting in only two or three bits of sampled noise, hence only a few quantal levels, whereas the software display gain is maximal in scaling the display range to match the range of buffer data.

Employing Preset B and briefly collecting another continuous record provides a different perspective of the baseline noise as observed in Figure 15. In this case the ordinal display axis is *autoscaled* and the overall system gain has been increase from 2.7x to 27x by specifying an interface gain of 10x. All other parameters remain the same as with

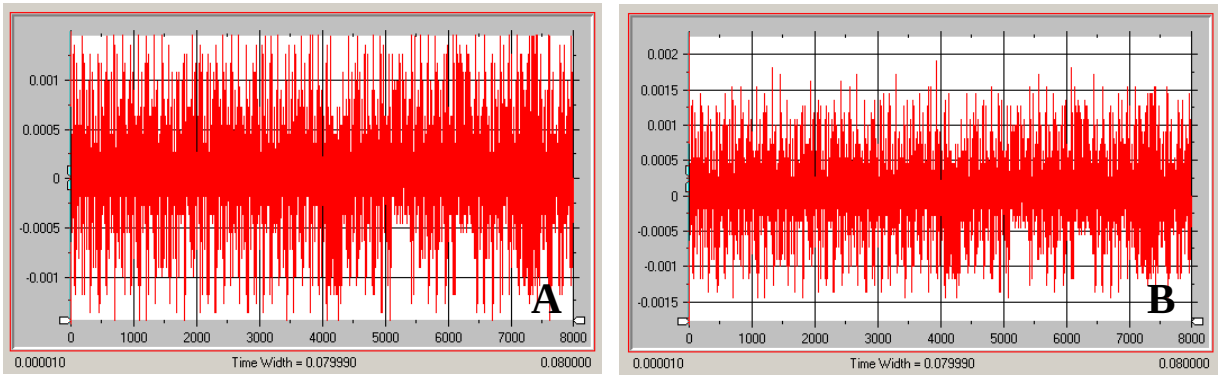


Figure 15. Two Displays of System Noise with Shorted Inputs and Increased Gain
This figure is similar to Figure 13 except that the amplifier gain is 10 times larger. Panel A on the left is with fixed ordinal gain. Panel B is with autoscaling gain.

Preset A. The baseline representation is much less quantal and appears more like gaussian noise. The display in Panel A is with the ordinal gain set to 0.00145 volts RTI which is 1/128 of the full scale ± 5.0 volts divided by total gain of 27, whereas Panel B is with autoscaling enabled.

Now continuing with the Preset B conditions while continually sampling sweeps, remove the red input cable from its GND snap button on the Demonstartion Interface. This will float one active input. Touching this input lead with a moistened finger should produce a 60 Hz noise signal in the display somewhat like that seen in Figure 16. Depending on the degree of offset, it may be necessary to touch another moistened finger to the input ground to provide an appropriate input leakage pathway, otherwise a very large magnitude 60 Hz. signal may be observed in which with only the steep transitions between phases are seen. The display time duration is 80 msec which is sufficient time for 4.8 cycles of 60 Hz as see in the display.

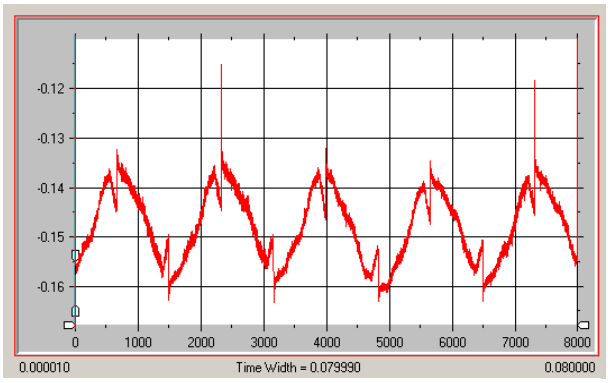


Figure 16. 60 Hz. Noise Contamination with a Single Input Lead Being Touched

Finally, to explore an example of averaging with the system it is necessary connect the input cables to the Demonstration Interface as shown in Figure 17, apply the AuxOut signal to J1, and activate Preset Condition C in the software. After activation the sampling rate has been increased to 400,000 and the buffer duration reduced to 4 msec with 5 msec ISI. The ordinal range is manually set to ± 0.015 volts. The Aux Out signal will be a 100 usec/phase biphasic pulse of 0.01 volt peak magnitude specified by a 0.1 volt peak output on DAC1OUT. Triggering is internal self-triggering using a software timer. Selection of Start Averaging will initiate averaging of 100 presentations of the cable attenuated Aux Out signal. The panel on the left below represents a typical display. By selecting Alternate Polarity during Averaging and repeating the averaging, no net residual stimulus remains in the averaged display as shown in the right panel.

Figure 17. Input connections for differential input.

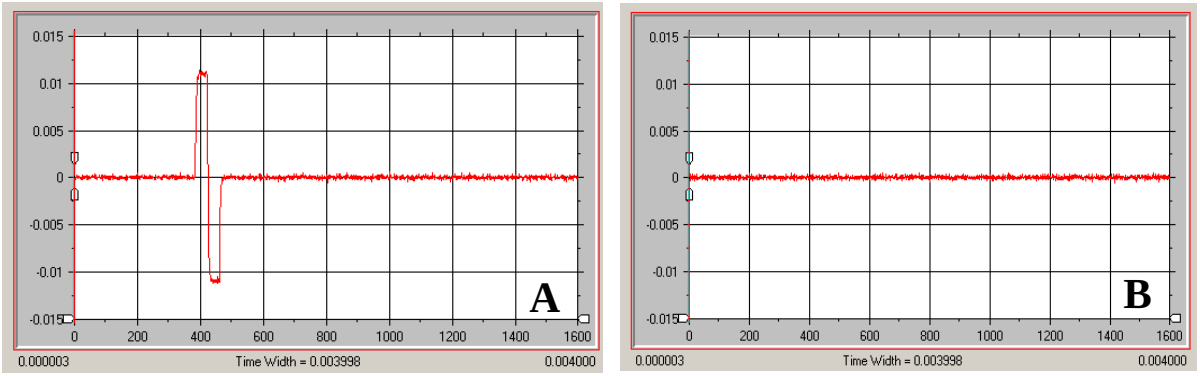


Figure 18. Final Averages of a 100 usec/sec Biphasic Pulse in which the Pulse Polarity was Constant (Panel A) and Alternated (Panel B) across 100 Trials

By changing the headstage input connection to that shown in Figure 19, the common mode rejection behavior of the system may be observed. Repeating the averaging as conducted in the previous step, zero magnituse averages similar to that shoul in Figure 18B are observed in all cases.

With this inroductory material illustrating the operation of the system, the reader may wish to perform additional evaluation of the system.

Figure 19. Input connections for common-mode input.

II. Specific Design Details

A. Gain Adjustments

There are multiple options available for modifying the operational gain of the amplifier system. While the gain of the headstage is fixed, three hardware gain options exist in the PCMCIA interface based on the cascaded string of INA129 instrumentation amps IC6-IC8. Currently, the individual gains of these stages are set to x1, x10 and x10 for IC6, IC7 and IC8, respectively, resulting in cascaded gains of x1, x10 and x100. The specific operational gain is selected under software control by sampling input data on a different analog input line of the NI 6062E data acquisition system.

Should an application require alternative gains for one, two or all of these three stages, a simple resistor swap may be made. Gain (G) for the INA129 instrumentation amplifier is set by the gain setting resistor R_G where $G = 1+(49{,}400\ \Omega\ /R_G)$, where R_G is in Ω. One percent precision resistors are sufficient.

Additional gain increments may be obtained by selecting different hardware gains for the input stages of the NI 6062E system using software control.

While it is possible to modify the gain of the headstage, it is best to handle this gain as part of the headstage bandwidth adjustment as described in the following section. The present low gain value of 3 is chosen to allow the recording of surface artifact potentials without encountering saturation of the headstage amplifiers operating with the small ±5 power rail voltages. The low ±5 voltage is used to maintain low power dissipation in the fully-differential, high-bandwidth op-amp THS4130 and to minimize overall system power. At ±5 volt rails the THS4130 may operate without requiring a heat sink. In principle the headstage could be operated with ±15 rails; however, the present device on this board will be destroyed by heating. In order to operate at ±15 volts the board will need to be modified to allow the use of the PowerPad version of the THS4130, which heatsinks the chip die directly to a special grid of board via located beneath the device package.

B. Bandwidth Adjustments

The headstage is configured basically as a three op-amp instrumentation amplifier. As part of this design, a fully balanced multiple feedback filter design is located just prior to the output op-amp of the system. The design characteristics of this filter may be determined using the FilterPro design tool available from Texas Instruments. The use of this tool is described in Application Report SBFA001A – November, 2001, titled FilterPro MFB and Sallen-Key Low-Pass Filter Design Program.

C. External and Internal Hardware Triggers for Synchronous Data Collection and Presentation

Simultaneously acquiring an analog signal into an input buffer while playing out a stored data buffer via an analog output in a synchronized manner is not a native mode of operation of the NI data acquisition system. However, this operation is possible and the PCMCIA interface has been specifically designed to support this capability.

The approach is simple and involves setting up both the analog input and analog output data transfer processes to each activate on an external trigger. To initiate synchronized data transfers, a common external trigger event is provided to start both of these processes. Each data transfer process may operate with its own clock frequency independent of the other process.

The external trigger event to start these processes may be provided in one of two ways.

(1) In the case of the existence of a logical TTL trigger source external to the software/hardware system, this external source may be applied as an external trigger to the PFI hardware input specified in software as the trigger source for each data transfer process as shown in Figure 20. In this case PFI_0 is used. The trigger signal to PFI_0 is conditioned through a D-type flipflop, which may be cleared and armed by a low-to-high transition on digital control line 6 (DIO_6). When a low-to-high transition occurs on the external trigger the Q output of the FF transitions high creating a trigger event on PFI_0 to begin data transfers. All subsequent events on the external trigger line are ignored until DIO_6 is cycled low and back to high again.

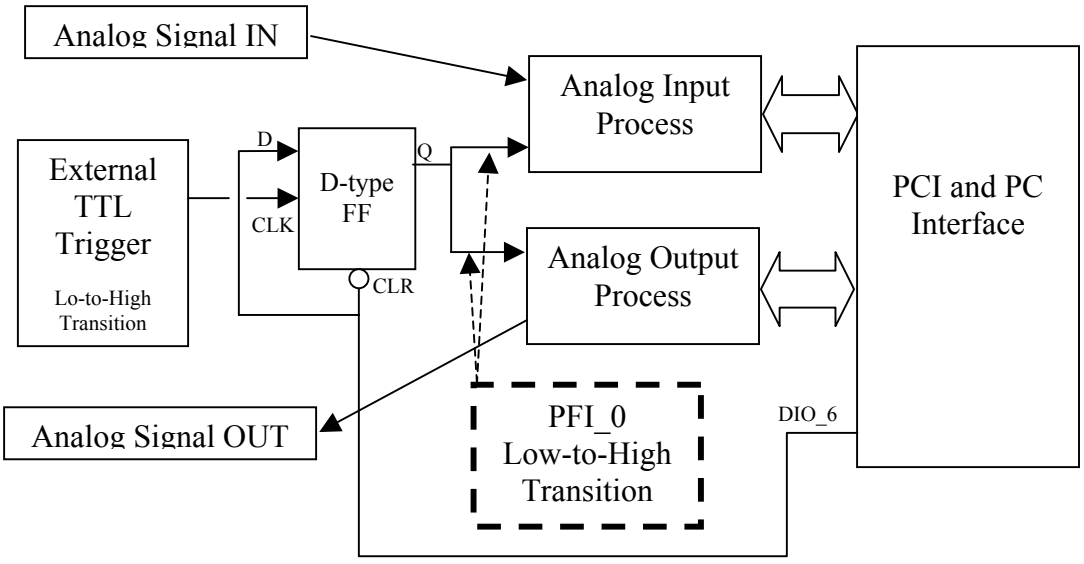


Figure 20. External trigger operation using and external TTL trigger source.

(2) In the case of no external signal, then a synchronizing hardware start pulse must be generated on a digital I/O line under software control as described in Figure 21. This signal is physically applied by an external jumper to another PFI hardware input as specified in software. Consequently, when the software generates a transition on the digital I/O line, the physical signal is detected by NI hardware as an externally applied trigger, thus initiating data transfer.

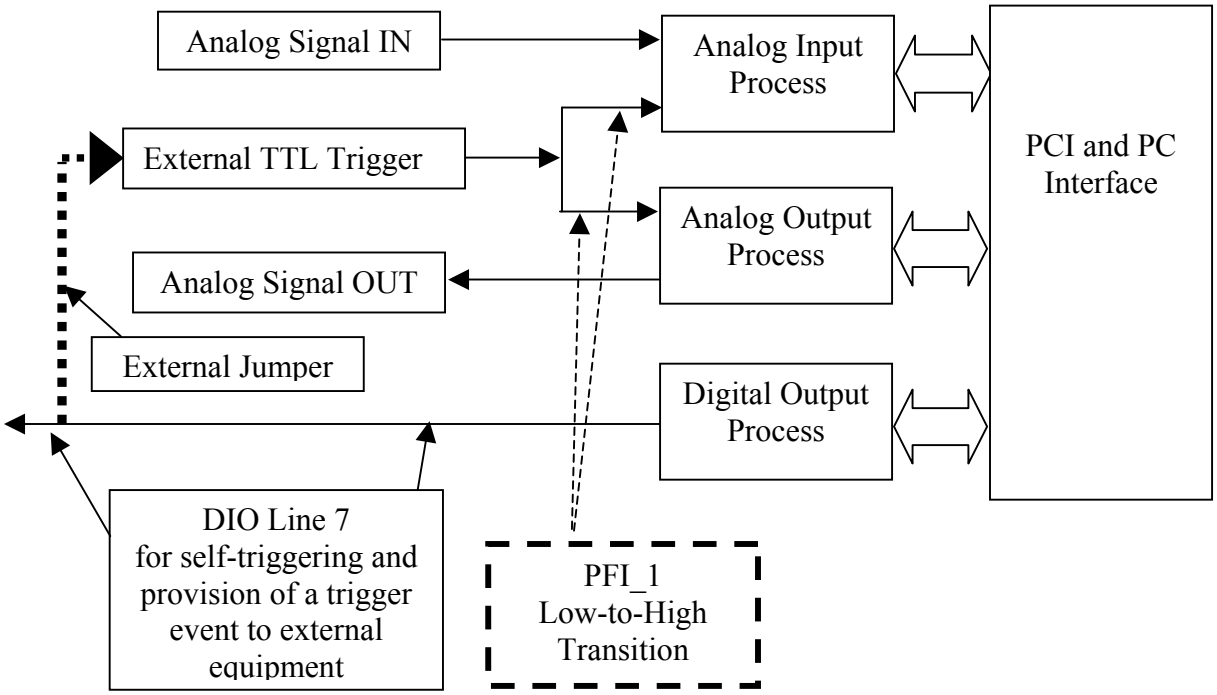


Figure 21. "Internal" triggering mode used in the case of no external trigger source. In this case, the system generates it's own trigger signal which is routed to the external trigger input so that input and output buffer transfer begin simultaneously.

D. Schematics

1. Headstage

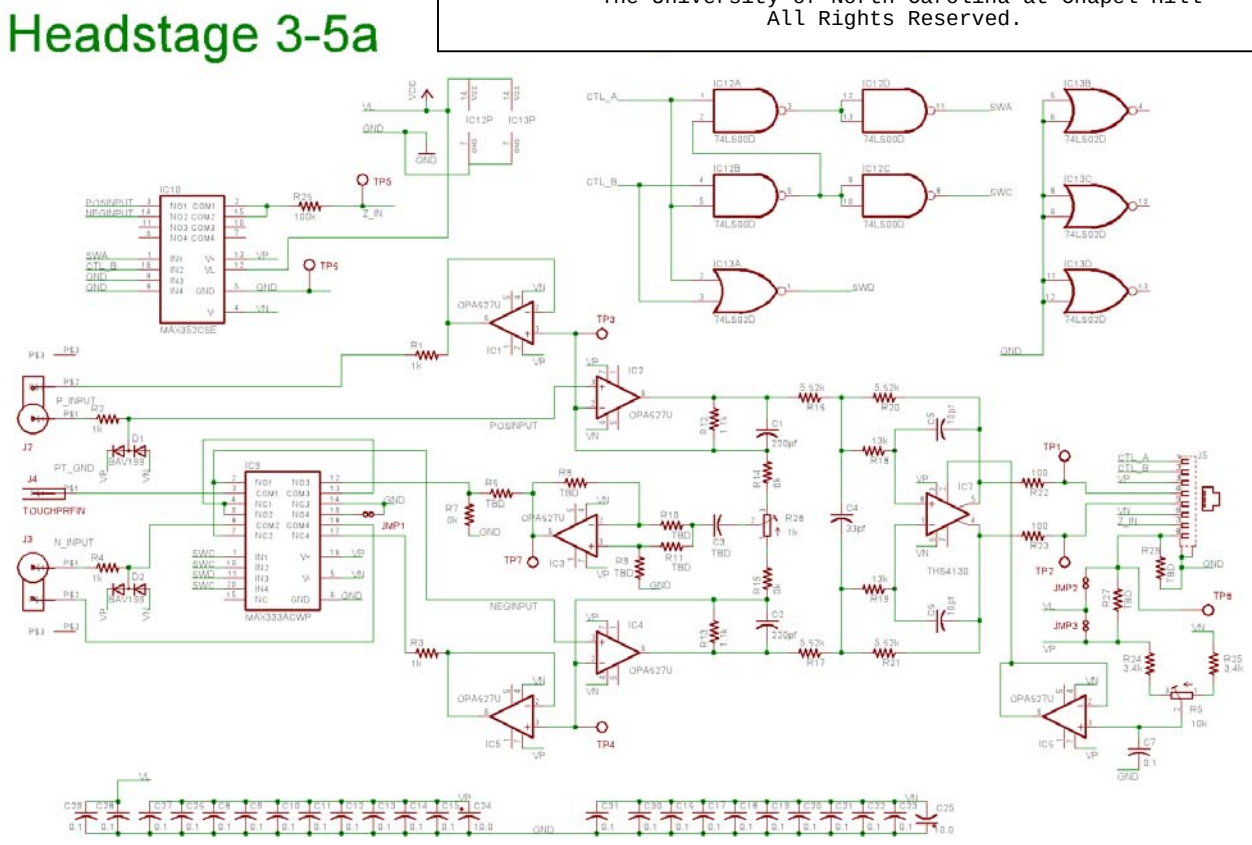


Figure 22. Schematic diagram of headstage amplifier.

2. PCMCIA Interface for Laptop Computer

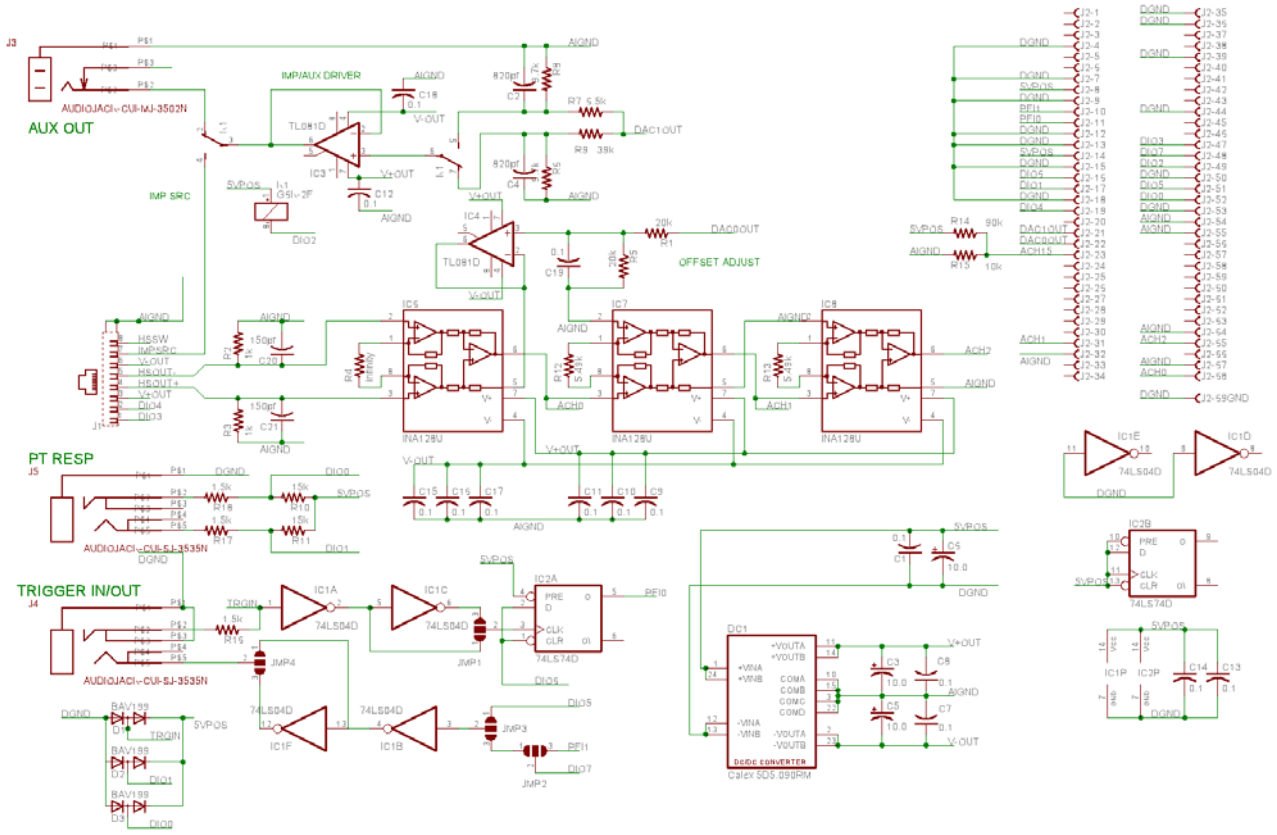


Figure 23. Schematic diagram of PCMCIA Interface.

III. Hardware Implementation

A. System Configuration and Equipment Photographs

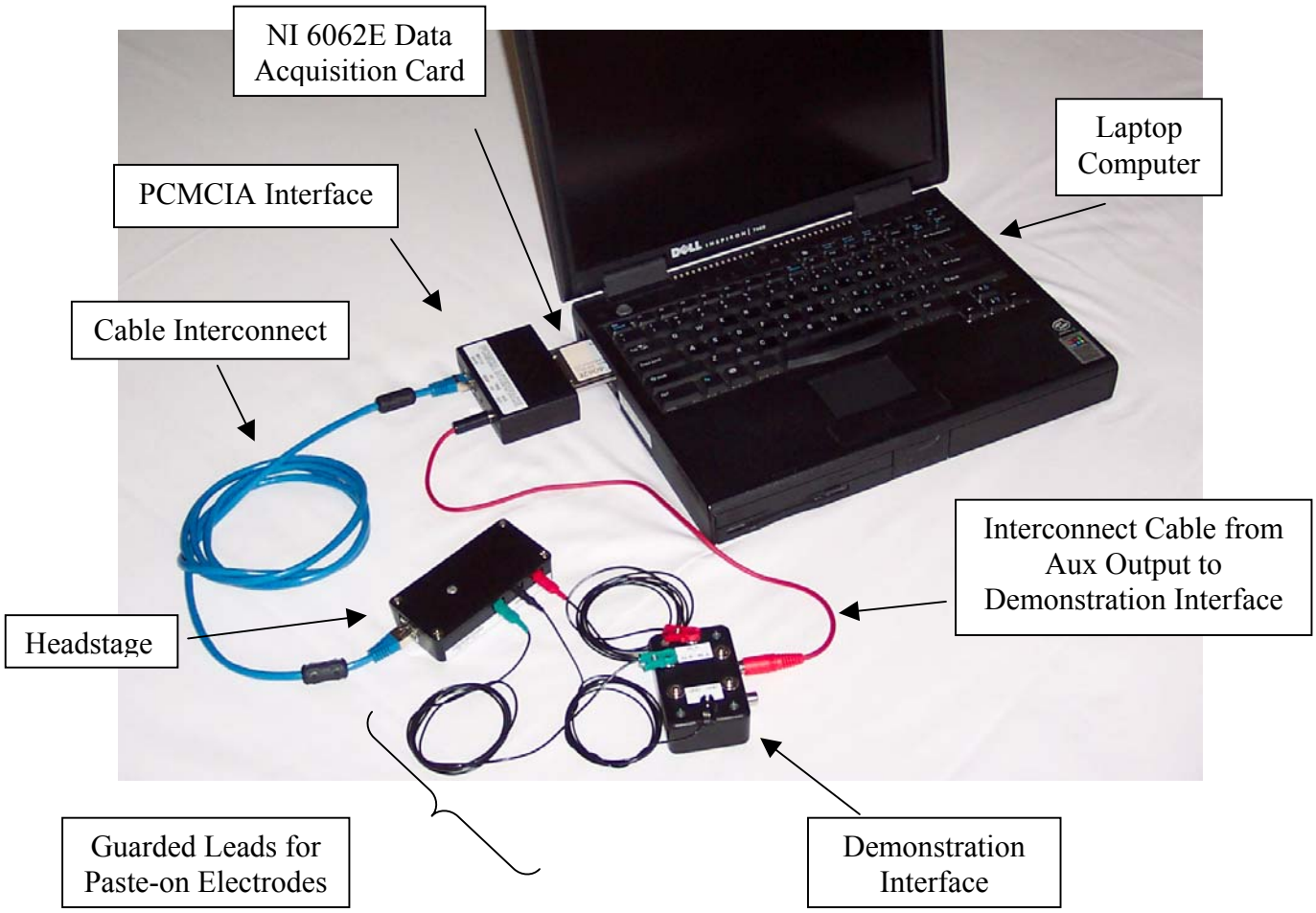


Figure 24. Photograph of basic system components illustrating the connectivity of the various elements.

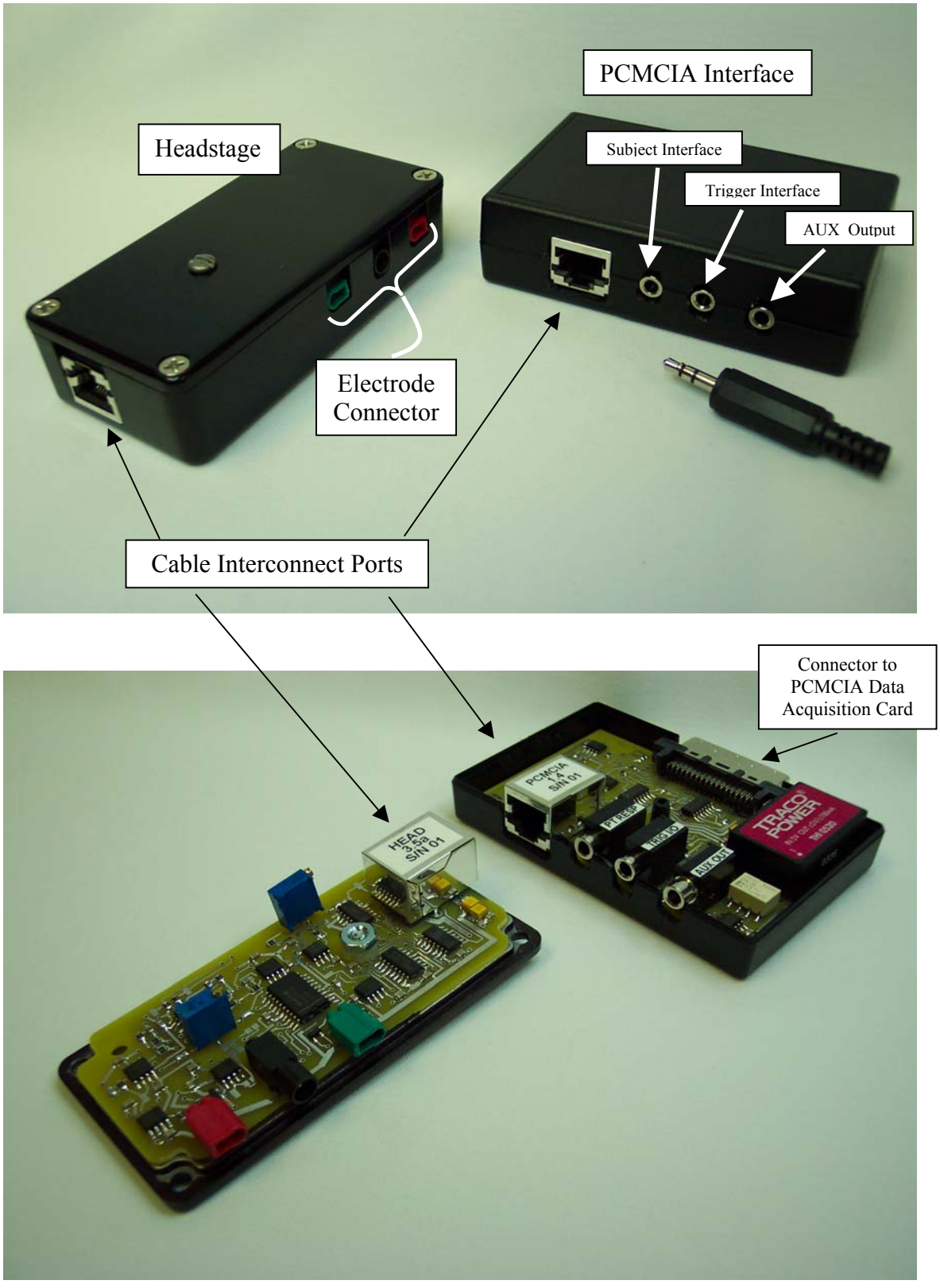
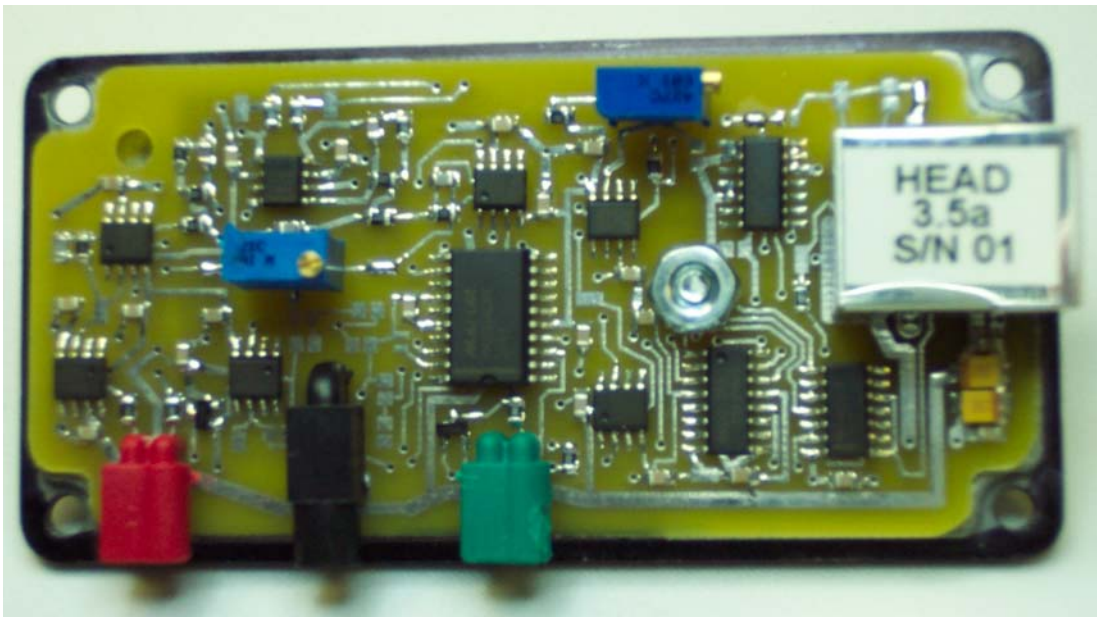
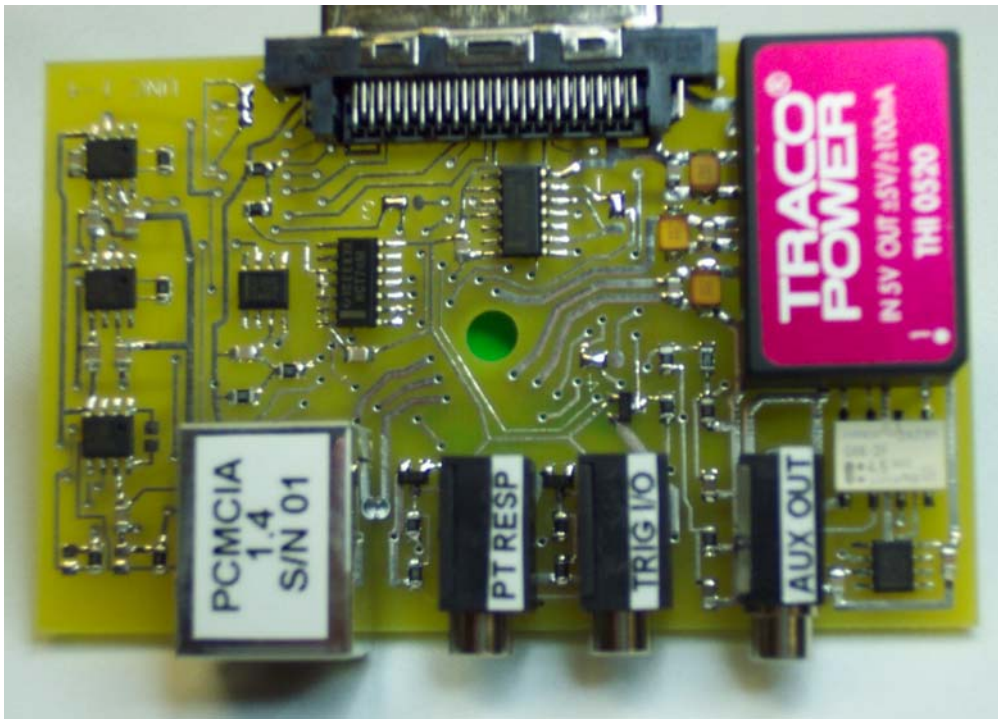


Figure 25. Close-up views of the exterior and interior of the headstage and the PCMCIA interface.



Headstage Amplifier



PCMCIA Interface

Figure 26. Expanded close-up photographs of the component sides of the headstage amplifier and the PCMCIA interface boards.

B. Board Layouts

1. Headstage

Figure 27. Headstage Component Layout (Top View)

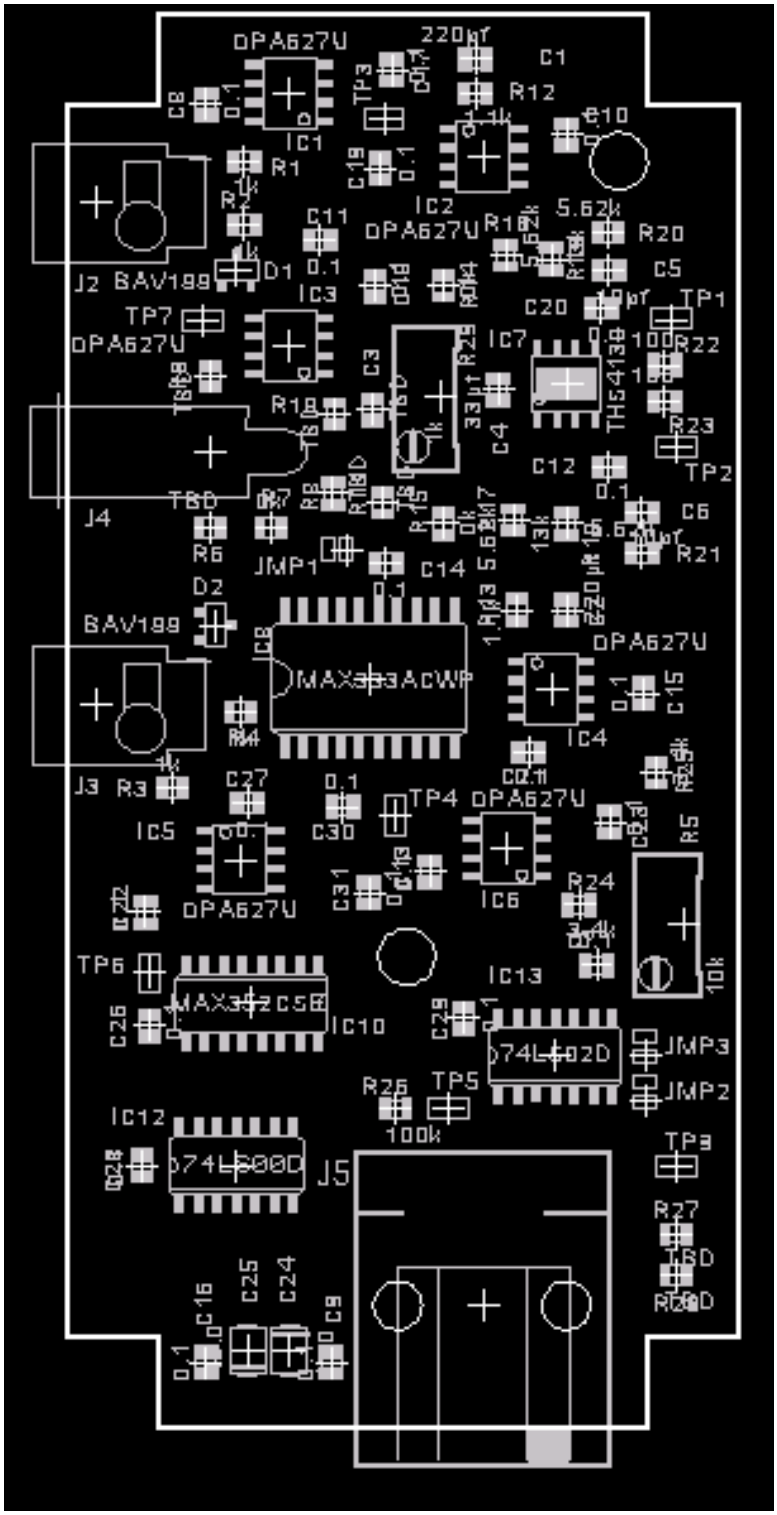


Figure 28. Headstage Board Top Layout

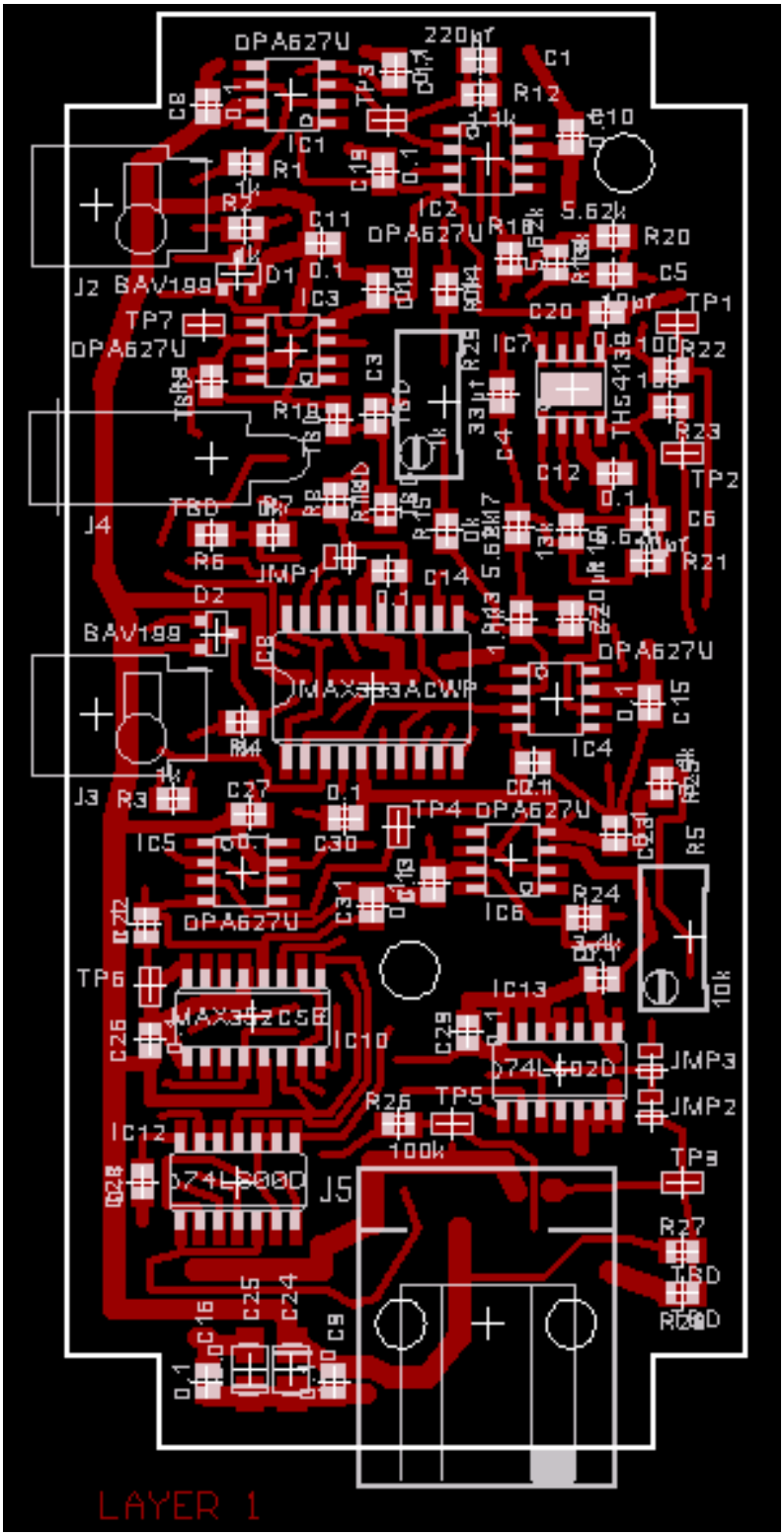
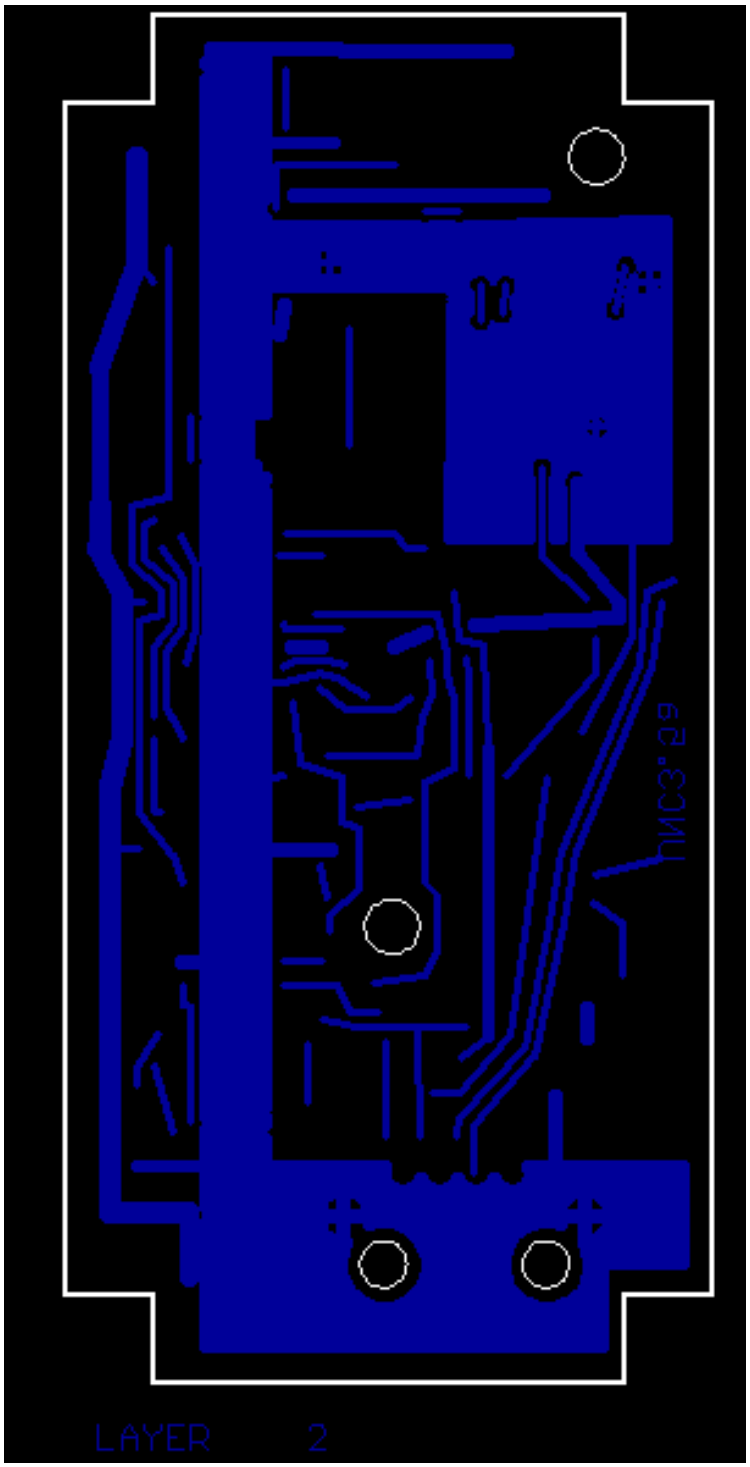


Figure 29. Headstage Board Bottom Layout



2. PCMCIA Interface for Laptop Computer

Figure 30. Component Layout (Top View)

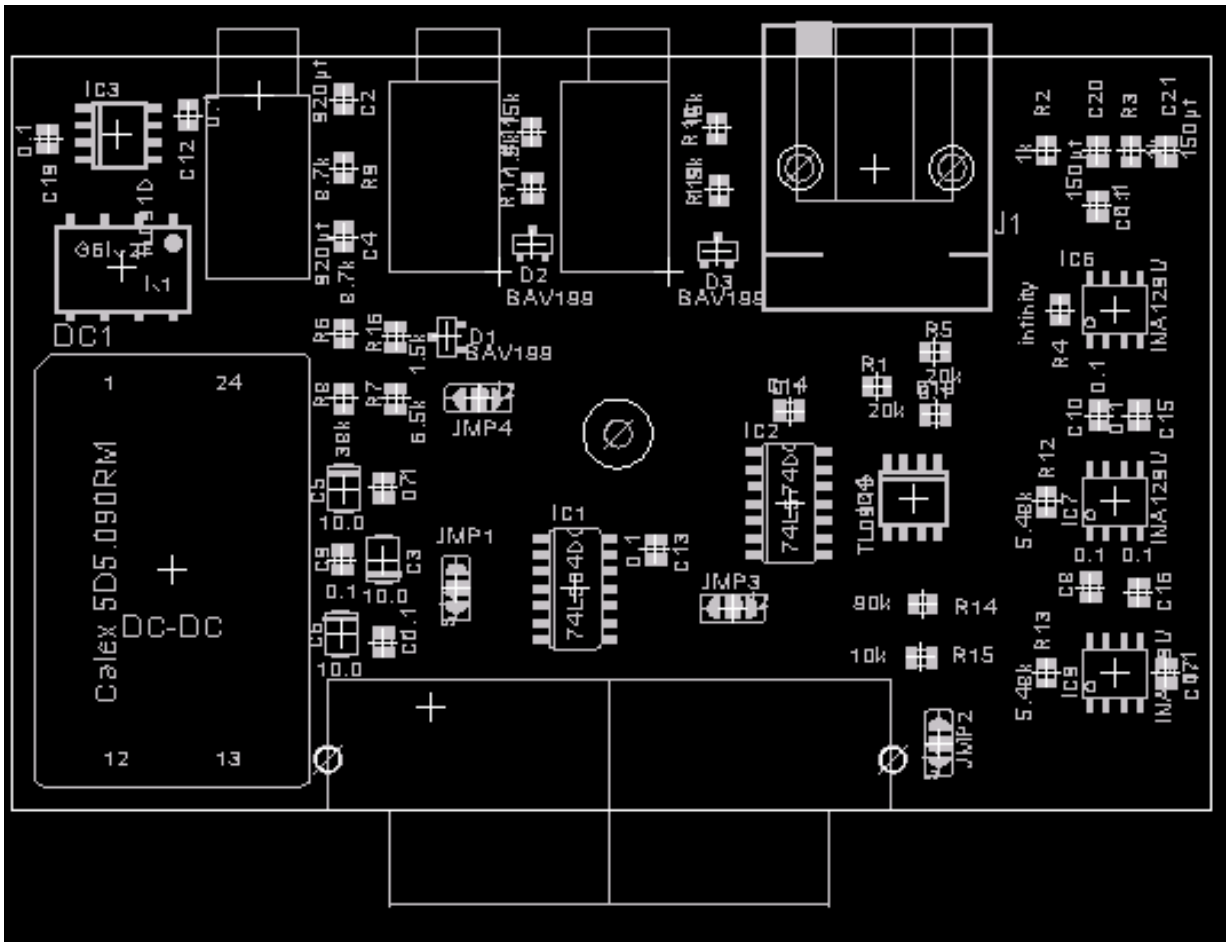


Figure 31. PCMCIA Interface Top Layout

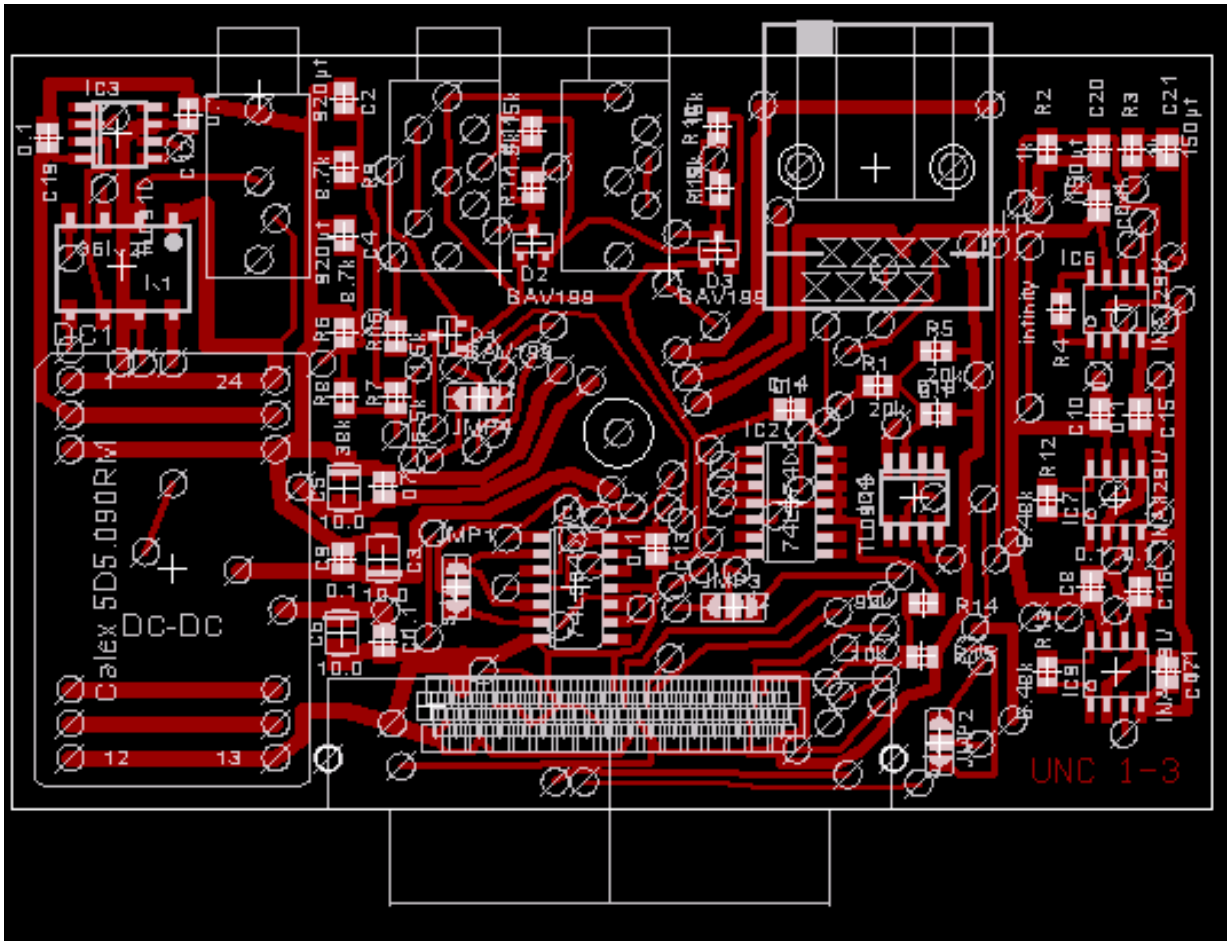
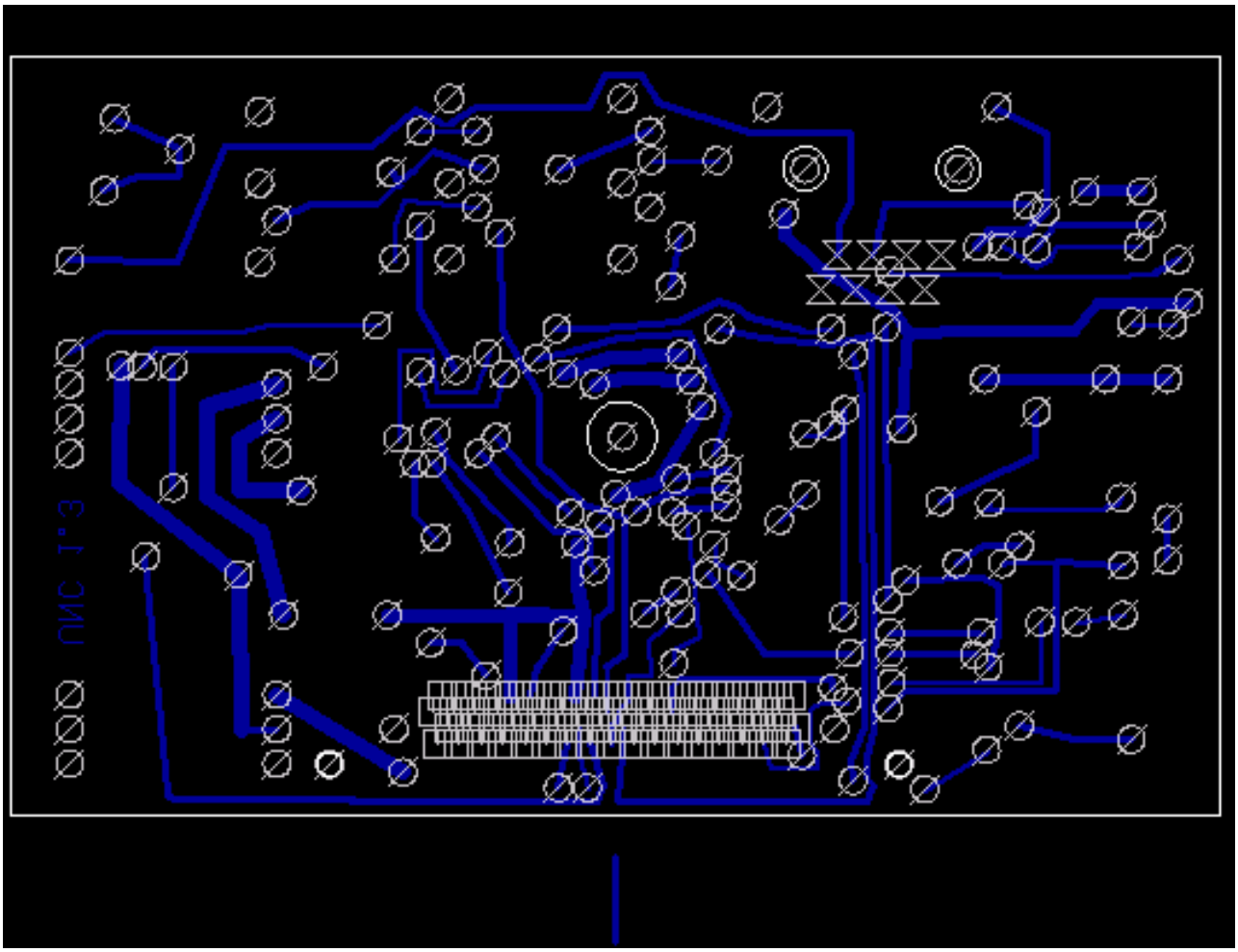


Figure 32. PCMCIA Interface Bottom Layout



C. Parts Lists

1. Headstage

Exported from headstage3_5a.sch at 12/23/2004 11:35:09a

EAGLE Version 4.11 Copyright (c) 1988-2003 CadSoft

Part	Value	Device	Package	Library	Sheet
C1	220pf	C-USC0805	C0805	rcl	1
C2	220pf	C-USC0805	C0805	rcl	1
C3	TBD	C-USC0805	C0805	rcl	1
C4	33pf	C-USC0805	C0805	rcl	1
C5	10pf	C-USC0805	C0805	rcl	1
C6	10pf	C-USC0805	C0805	rcl	1
C7	0.1	C-USC0805	C0805	rcl	1
C8	0.1	C-USC0805	C0805	rcl	1
C9	0.1	C-USC0805	C0805	rcl	1
C10	0.1	C-USC0805	C0805	rcl	1
C11	0.1	C-USC0805	C0805	rcl	1
C12	0.1	C-USC0805	C0805	rcl	1
C13	0.1	C-USC0805	C0805	rcl	1
C14	0.1	C-USC0805	C0805	rcl	1
C15	0.1	C-USC0805	C0805	rcl	1
C16	0.1	C-USC0805	C0805	rcl	1
C17	0.1	C-USC0805	C0805	rcl	1
C18	0.1	C-USC0805	C0805	rcl	1
C19	0.1	C-USC0805	C0805	rcl	1
C20	0.1	C-USC0805	C0805	rcl	1
C21	0.1	C-USC0805	C0805	rcl	1
C22	0.1	C-USC0805	C0805	rcl	1
C23	0.1	C-USC0805	C0805	rcl	1
C24	10.0	CPOL-USB/3528-21W	B/3528-21W	rcl	1
C25	10.0	CPOL-USB/3528-21W	B/3528-21W	rcl	1
C26	0.1	C-USC0805	C0805	rcl	1
C27	0.1	C-USC0805	C0805	rcl	1
C28	0.1	C-USC0805	C0805	rcl	1
C29	0.1	C-USC0805	C0805	rcl	1
C30	0.1	C-USC0805	C0805	rcl	1
C31	0.1	C-USC0805	C0805	rcl	1
D1	BAV199	BAV199	SOT23	diode	1
D2	BAV199	BAV199	SOT23	diode	1
IC1	OPA627U	OPA627U	SO08	burr-brown	1
IC2	OPA627U	OPA627U	SO08	burr-brown	1
IC3	OPA627U	OPA627U	SO08	burr-brown	1
IC4	OPA627U	OPA627U	SO08	burr-brown	1
IC5	OPA627U	OPA627U	SO08	burr-brown	1
IC6	OPA627U	OPA627U	SO08	burr-brown	1
IC7	THS4130	THS4130	SO08HS	ccf_parts1	1
IC9	MAX333ACWP	MAX333ACWP	SO20L	maxim	1
IC10	MAX352CSE	MAX352CSE	SO16	maxim	1
IC12	74LS00D	74LS00D	SO14	74xx-us	1
IC13	74LS02D	74LS02D	SO14	74xx-us	1
J2	DUALTOUCHPRF	DUALTOUCHPRF	DUALTCHPRFCON	ccf_parts2	1
J3	DUALTOUCHPRF	DUALTOUCHPRF	DUALTCHPRFCON	ccf_parts2	1
J4	TOUCHPRFIN	TOUCHPRFIN	TOUCHPROOFCONN	ccf_parts2	1
J5		558310-1	558310-1	con-amp	1
JMP1	SLDRJUMPER	SLDRJUMPER	SLDRJMPPADS	ccf_parts1	1
JMP2	SLDRJUMPER	SLDRJUMPER	SLDRJMPPADS	ccf_parts1	1
JMP3	SLDRJUMPER	SLDRJUMPER	SLDRJMPPADS	ccf_parts1	1
R1	1k	R-US_R0805	R0805	rcl	1

R2	1k	R-US_R0805	R0805	rcl	1
R3	1k	R-US_R0805	R0805	rcl	1
R4	1k	R-US_R0805	R0805	rcl	1
R5	10k	R-TRIMM64Y	RTRIM64Y	rcl	1
R6	TBD	R-US_R0805	R0805	rcl	1
R7	0k	R-US_R0805	R0805	rcl	1
R8	TBD	R-US_R0805	R0805	rcl	1
R9	TBD	R-US_R0805	R0805	rcl	1
R10	TBD	R-US_R0805	R0805	rcl	1
R11	TBD	R-US_R0805	R0805	rcl	1
R12	1.1k	R-US_R0805	R0805	rcl	1
R13	1.1k	R-US_R0805	R0805	rcl	1
R14	0k	R-US_R0805	R0805	rcl	1
R15	0k	R-US_R0805	R0805	rcl	1
R16	5.62k	R-US_R0805	R0805	rcl	1
R17	5.62k	R-US_R0805	R0805	rcl	1
R18	13k	R-US_R0805	R0805	rcl	1
R19	13k	R-US_R0805	R0805	rcl	1
R20	5.62k	R-US_R0805	R0805	rcl	1
R21	5.62k	R-US_R0805	R0805	rcl	1
R22	100	R-US_R0805	R0805	rcl	1
R23	100	R-US_R0805	R0805	rcl	1
R24	3.4k	R-US_R0805	R0805	rcl	1
R25	3.4k	R-US_R0805	R0805	rcl	1
R26	100k	R-US_R0805	R0805	rcl	1
R27	TBD	R-US_R0805	R0805	rcl	1
R28	1k	R-TRIMM64Y	RTRIM64Y	rcl	1
R29	TBD	R-US_R0805	R0805	rcl	1
TP1	SMTESTPT	SMTESTPT	SMTESTPAD	ccf_parts1	1
TP2	SMTESTPT	SMTESTPT	SMTESTPAD	ccf_parts1	1
TP3	SMTESTPT	SMTESTPT	SMTESTPAD	ccf_parts1	1
TP4	SMTESTPT	SMTESTPT	SMTESTPAD	ccf_parts1	1
TP5	SMTESTPT	SMTESTPT	SMTESTPAD	ccf_parts1	1
TP6	SMTESTPT	SMTESTPT	SMTESTPAD	ccf_parts1	1
TP7	SMTESTPT	SMTESTPT	SMTESTPAD	ccf_parts1	1
TP8	SMTESTPT	SMTESTPT	SMTESTPAD	ccf_parts1	1

Parts List (continued)

2. PCMCIA Interface for Laptop Computer

```
Exported from PCMCIA_1-3.sch at 12/23/2004 11:33:13a

EAGLE Version 4.11 Copyright (c) 1988-2003 CadSoft

Part     Value       Device         Package            Library         Sheet

C1       0.1            C-USC0805              C0805              rcl         1
C2       820pf          C-USC0805              C0805              rcl         1
C3       10.0           CPOL-USB/3528-21W      B/3528-21W         rcl         1
C4       820pf          C-USC0805              C0805              rcl         1
C5       10.0           CPOL-USB/3528-21W      B/3528-21W         rcl         1
C6       10.0           CPOL-USB/3528-21W      B/3528-21W         rcl         1
C7       0.1            C-USC0805              C0805              rcl         1
C8       0.1            C-USC0805              C0805              rcl         1
C9       0.1             C-USC0805              C0805              rcl        1
C10      0.1             C-USC0805              C0805              rcl        1
C11      0.1             C-USC0805              C0805              rcl        1
C12      0.1             C-USC0805              C0805              rcl        1
C13      0.1             C-USC0805              C0805              rcl        1
C14      0.1             C-USC0805              C0805              rcl        1
C15      0.1             C-USC0805              C0805              rcl        1
C16      0.1             C-USC0805              C0805              rcl        1
C17      0.1             C-USC0805              C0805              rcl        1
C18      0.1             C-USC0805              C0805              rcl        1
C19      0.1             C-USC0805              C0805              rcl        1
C20      150pf           C-USC0805              C0805              rcl        1
C21      150pf           C-USC0805              C0805              rcl        1
D1       BAV199          BAV199                 SOT23              diode      1
D2       BAV199          BAV199                 SOT23              diode      1
D3       BAV199          BAV199                 SOT23              diode      1
DC1      Calex 5D5.090RM DCW2C                  DCW                dc-dc-
onverter 1
IC1      74LS04D         74LS04D                SO14               74xx-us    1
IC2      74LS74D         74LS74D                SO14               74xx-us    1
IC3      TL081D          TL081D                 SO08               linear     1
IC4      TL081D          TL081D                 SO08               linear     1
IC6      INA128U         INA128U                SO08               burr-brown 1
IC7      INA128U         INA128U                SO08               burr-brown 1
IC8      INA128U         INA128U                SO08               burr-brown 1
J1                       558310-1               558310-1           con-amp    1
J2                       HONDA68                HONDA68RA          ccf_parts1 1
J3       AUDIOJACK-CUI-MJ-3502N AUDIOJACK-CUI-MJ-3502N AUDIO-CUI-MJ-3502N
ccf_parts1      1
J4       AUDIOJACK-CUI-SJ-3535N AUDIOJACK-CUI-SJ-3535N AUDIO-CUI-SJ-35
ccf_parts1      1
J5       AUDIOJACK-CUI-SJ-3535N AUDIOJACK-CUI-SJ-3535N AUDIO-CUI-SJ-35
ccf_parts1      1
JMP1     SJ2             SJ2                    SJ_2               jumper     1
JMP2     SJ2             SJ2                    SJ_2               jumper     1
JMP3     SJ2             SJ2                    SJ_2               jumper     1
JMP4     SJ2             SJ2                    SJ_2               jumper     1
K1       G6K-2F          G6K-2F                 G6K-2F             relay      1
R1       20k             R-US_R0805             R0805              rcl        1
R2       1k              R-US_R0805             R0805              rcl        1
R3       1k              R-US_R0805             R0805              rcl        1
R4       infinity        R-US_R0805             R0805              rcl        1
R5       20k             R-US_R0805             R0805              rcl        1
R6       9.7k            R-US_R0805             R0805              rcl        1
```

R7	6.5k	R-US_R0805	R0805	rcl	1
R8	9.7k	R-US_R0805	R0805	rcl	1
R9	39k	R-US_R0805	R0805	rcl	1
R10	15k	R-US_R0805	R0805	rcl	1
R11	15k	R-US_R0805	R0805	rcl	1
R12	5.49k	R-US_R0805	R0805	rcl	1
R13	5.49k	R-US_R0805	R0805	rcl	1
R14	90k	R-US_R0805	R0805	rcl	1
R15	10k	R-US_R0805	R0805	rcl	1
R16	1.5k	R-US_R0805	R0805	rcl	1
R17	1.5k	R-US_R0805	R0805	rcl	1
R18	1.5k	R-US_R0805	R0805	rcl	1

D. Board Design Information

1. Schematic and Board Layout Software

The schematics and printed circuit boards described in this report were prepared using the CadSoft EAGLE PCB–Design Package (Version 4.1). Details on this software CAD system for schematic entry, board layout and autorouting may be obtained at http://www.cadsoft.com. This system is a moderately priced, functionally capable system with large component libraries available.

On the accompanying CD are the schematic (*.sch) and board layout (*.brd) files for both the headstage and the PCMCIA boards. A library file (*.lib) is also included and contains custom components developed for this project.

2. Board Design and Fabrication Files

Boards used in this project were manufactured by PCB Express using Internet submission of the Eagle board (*.brd) files described above. The boards are two-layer boards with surface mount components and plated through holes. The board material is industry standard 0.062" FR-4 laminate with standard 1oz. finished copper weight.

The basic PCBExpress #1 service was used, which does not include solder masks or silk screening, although the board layout will support these features. If a board with silk screening is desired, the user is encouraged to carefully examine the contents of the silk layer in the *.brd files for desired content and positioning of labels. Information about the PCBExpress #1 service can be obtained at http://www.pcbexpress.com. Other pc board houses should be able to process the Eagle board files as well. To date only the PCBExpress services have been employed.

IV. Availability of Present System and Future Design Improvements

A complete working set of the equipment and software described in this report has been provided to the Neural Prosthesis Development Office of the National Institute on Deafness and Commuication Disorders (NIDCD). Contact Roger Miller, Ph.D.[1] of NIDCD at millerr@nidcd.nih.gov to obtain the supporting documents in electronic form.

Contact Charles Finley, Ph.D.[2] at the University of North Carolina at Chapel Hill at ccf@med.unc.edu for information on current design improvements, known problems, errata, and limited technical support. The present report describes the general features and design details of the amplifier as it is best configured for the recording of short duration electrical artifact potentials in the presence of large RF fields. A second configuration optimized for the recording of biological potentials elicited by similar electrical stimulation is presently being prepared. The reason for the second amplifier version for recording low-level biological signals is due to excessive power supply noise from the DC-DC converter, injection of bus noise from the laptop computer, and the occurrence of a board oscillation at high gains in the present configuration of the amplifier system. These problems are currently being addressed and the revised configuration, including full documentation and functioning hardware, will be provided subsequently to the NIDCD Neural Prosthesis Development Office. The new documentation will be made available as an appendix to this present document. The current version of this document, including additional appendices when available, may be obtained electronically at http://www.nidcd.nih.gov/funding/programs/npp/index.asp or by contacting Roger Miller[1] millerr@nidcd.nih.gov.

All users of this equipment and software must obtain indemnification agreements with the Massachusetts Institute of Technology (MIT) and the University of North Carolina at Chapel Hill (UNC-CH) for applications involving human subjects. Contact Charles Finley[2] to initiate the process to make such arrangements.

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V. Appendices

A. Errata

There is one know board error on the PCMCIA board. On the top, component-side layer of the board the trace leading to the pad for IC6 pin 5 ends before reaching the pad for this pin. The error is easily observed on close visual inspection of the top side of the board. The gap must be filled by soldering a small wire from the pad to the trace. If this defect is not corrected, the software-controlled offset adjustment system will not function.

B. List of Supporting Materials on Accompanying CD

Data Files

Custom Component Libraries for Eagle Schematic/Board Design Package

Schematic and Board Layout Files for Headstage Amplifier

Schematic and Board Layout Files for PCMCIA Interface

Device Specifications

INA 129 Precision, Low Power Instrumentation Amplifier - TI/BurrBrown

DAQCard 6062E PCMCIA Multifunction Data Acquisition System - National Instruments

OPA627 Precision, High-Speed Operational Amplifier – TI/Burr Brown

THI 0520 DC/DC Converter – Traco Power

Software

NI-DAQ Driver Software for PC Compatibles, version 6.9.3, for Windows 2000/NT/XP/Me/9*x* - National Instruments

Custom VB Project Software for Data Acquisition and System Testing not including Strip VB-Active-X Component for Graphical Waveform Display

Executable Version of above project VB file

Evaluation Version of CadSoft Eagle Schematic Capture and Board Layout Software
(Note: This *evaluation version* of the Eagle software is not capable of supporting the included schematic and board files due to limitations by CadSoft on maximum board size.)

VI. Notes

- End of Document -