Oct 5, 2004

Emerging Devices and Materials for Beyond CMOS

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NIST

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Semiconductor Electronics Division
Gaithersburg, MD 20899

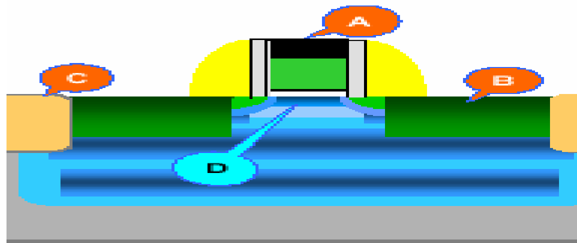
The Semiconductor Electronics Division

Emerging Devices and Materials for Beyond CMOS

CMOS and Novel Devices Group

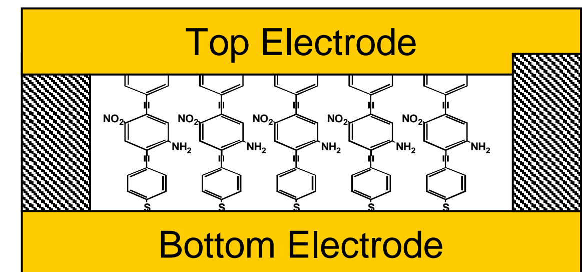
Performs research and development for the metrology, test structures, and reference materials required for CMOS and Beyond devices and their constituent materials.

MOS Device Characterization and Reliability Project

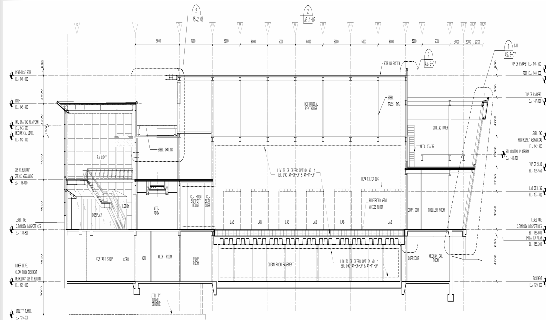


~20 Staff and Associates

Nanoelectronic Device Metrology Project

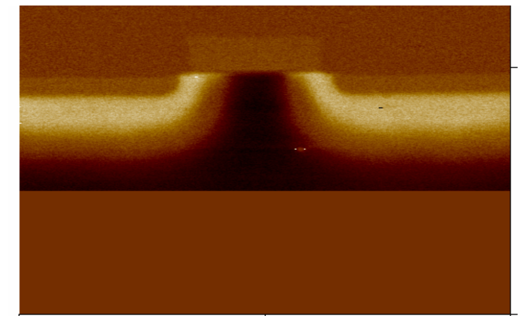


AML Nanofabrication Facility



The CND Group collaborates with numerous internal & external partners to leverage expertise

Electronic Materials Characterization Project



International Technology Roadmap for Semiconductors

- The ITRS serves as a guideline for the global semiconductor industry for a 15-year on projected technology needs and opportunities for innovation.

- The ITRS is devised and intended for technology assessment only and is without regard to any commercial considerations pertaining to individual products or equipment

- The ITRS consists of 15 chapters dealing with details of projected technology trends.

1. System Drivers, 2. Design, 3. Test & Test Equipment, 4. Process Integration, Devices, & Structures, 5. RF and A/MS Technologies for Wireless Communications, **6. Emerging Research Devices**, **7. Front End Processes**, 8. Lithography, 9. Interconnect, 10. Factory Integration, 11. Assembly & Packaging, 12. Environment, Safety, & Health, 13. Yield Enhancement, **14. Metrology**, 15. Modeling & Simulation

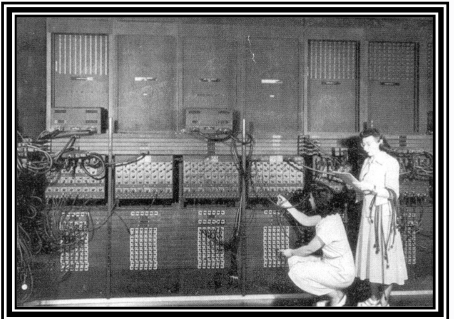
Outline

- The Future of Electronics
- The End of CMOS?
- Architectures, Devices, and Materials for Beyond CMOS
- Characterization Needs for Beyond CMOS
- Modeling/Simulation Needs for Beyond CMOS

Moore’s Law

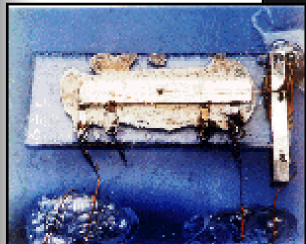
~2 cm

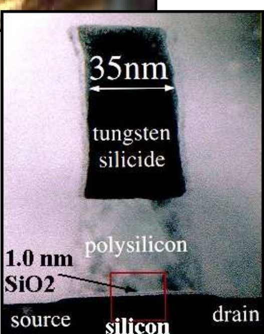
1945



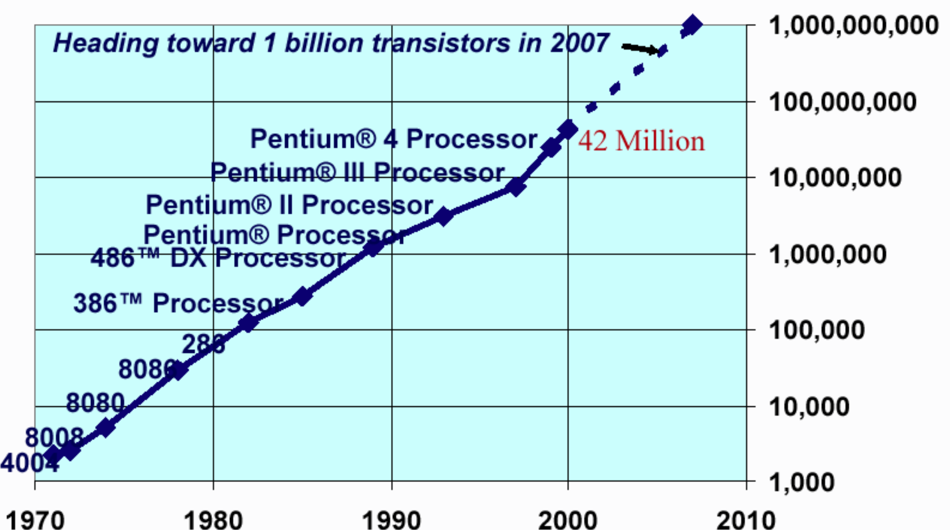
1948

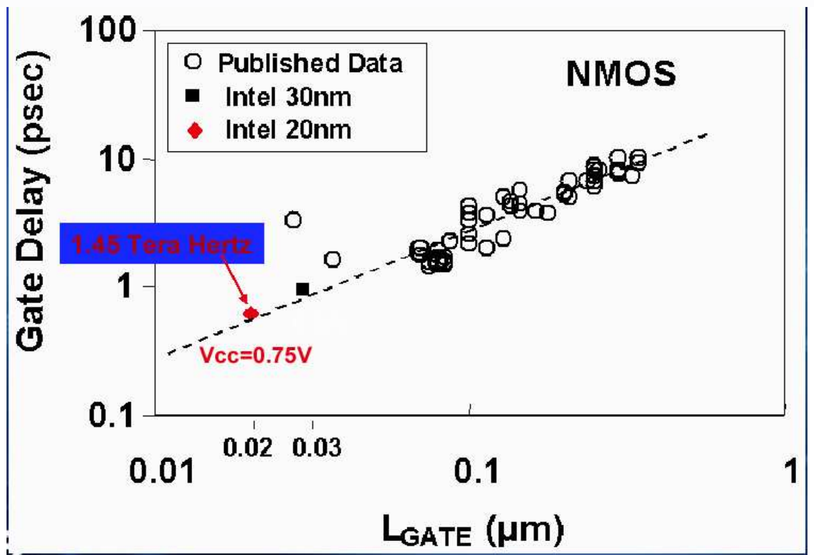
1959



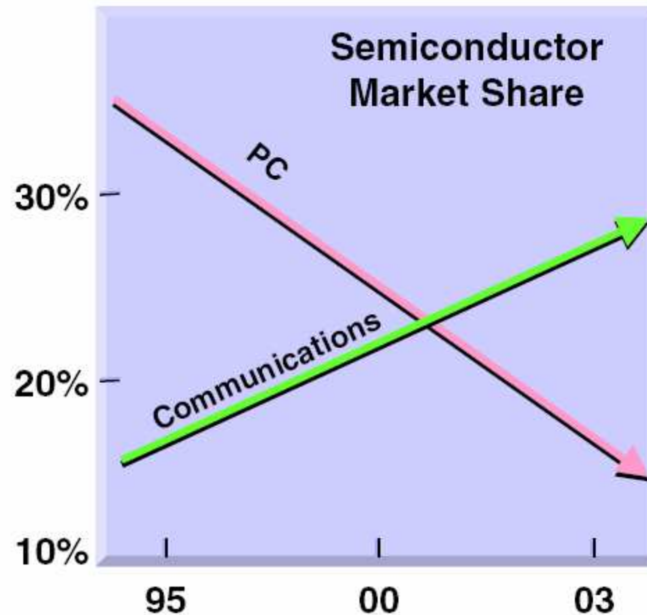


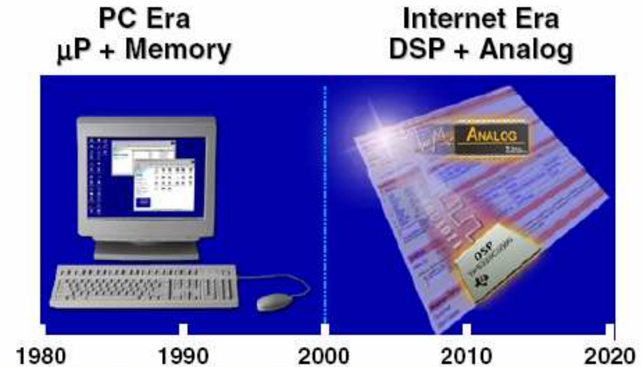
2014

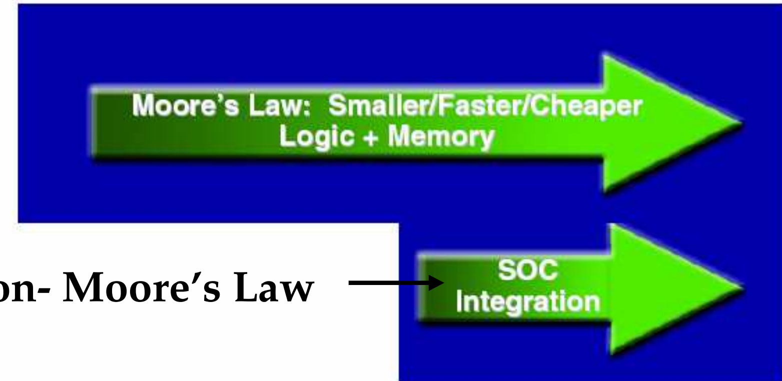




The Future of Electronics







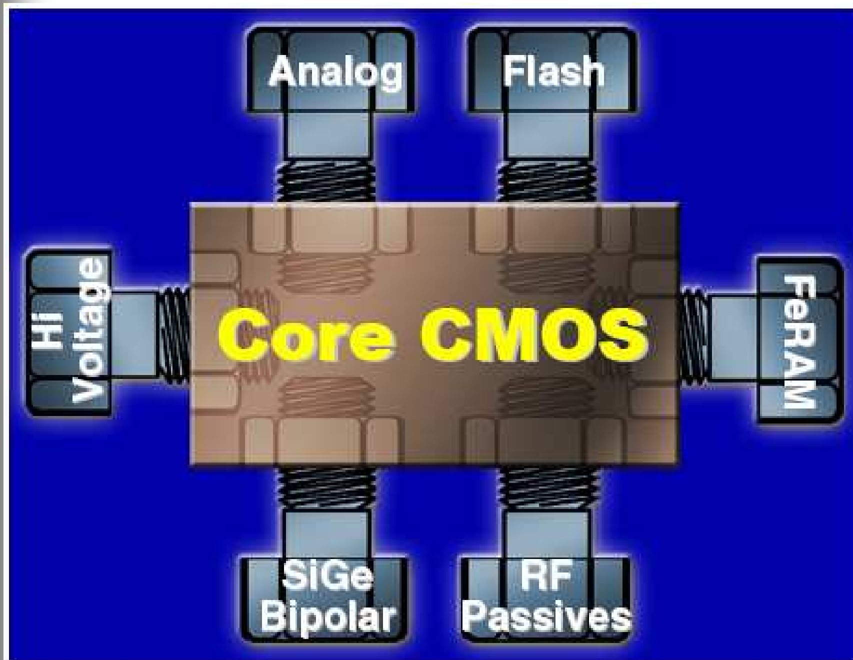
Non- Moore's Law

Transistor Scaling will continue to be an important Technology Driver in the Internet Era. But it will no longer be the sole driver: SOC Integration will be increasingly important.

Non-Moore's Law:

Adding Additional Functionality to CMOS

On-chip power, optical, memory, RF for communications applications



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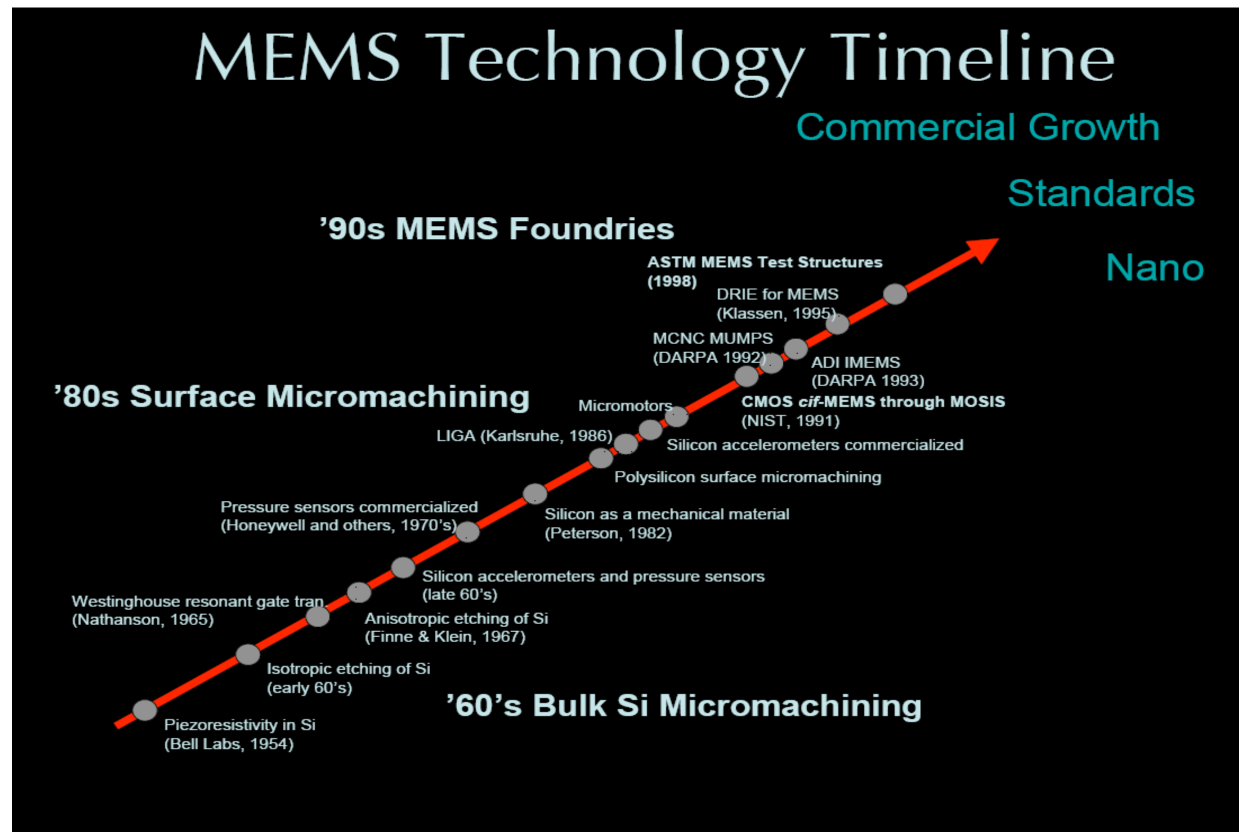
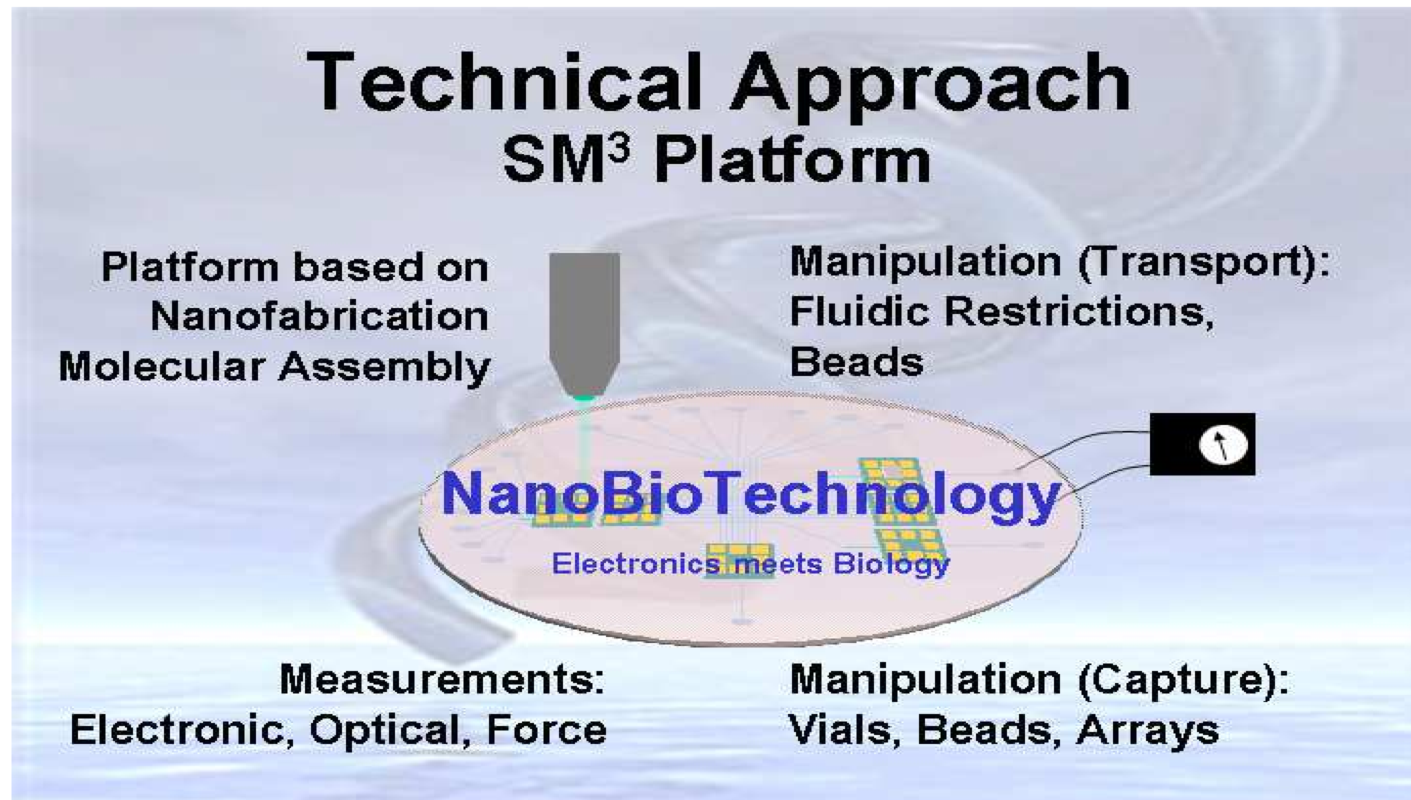
Non-Moore's Law:
Adding Additional Functionality to CMOS

On-chip MEMS (micromotors, accelerometers, pressure and gas sensors)



Non-Moore's Law:
Adding Additional Functionality to CMOS

On-chip molecular/biological manipulation and characterization



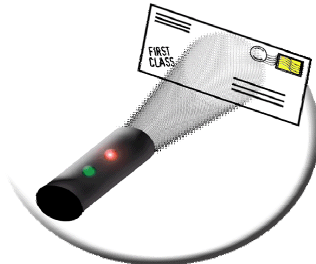
Non-Moore's Law:
Electronics Everywhere

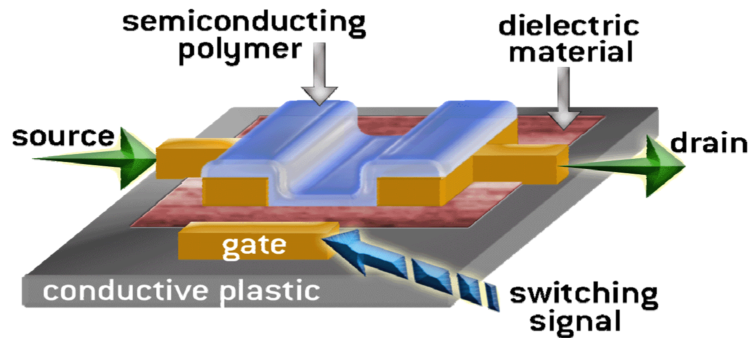
Organic Electronics

cheap dynamic signs

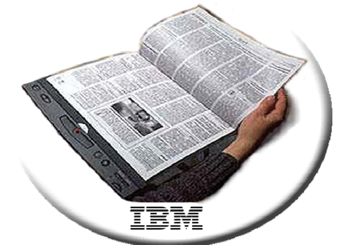
wearable electronics

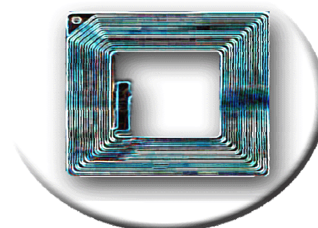
sensors



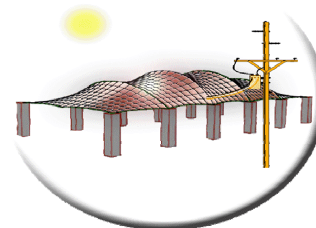


electronic paper





RFID tags



flexible solar cells

Non-Moore's Law:
Electronics Everywhere

Interactive Electronics

U. Of Rochester Center for Future Health

The Semiconductor Electronics Division

Emerging Devices and Materials for Beyond CMOS

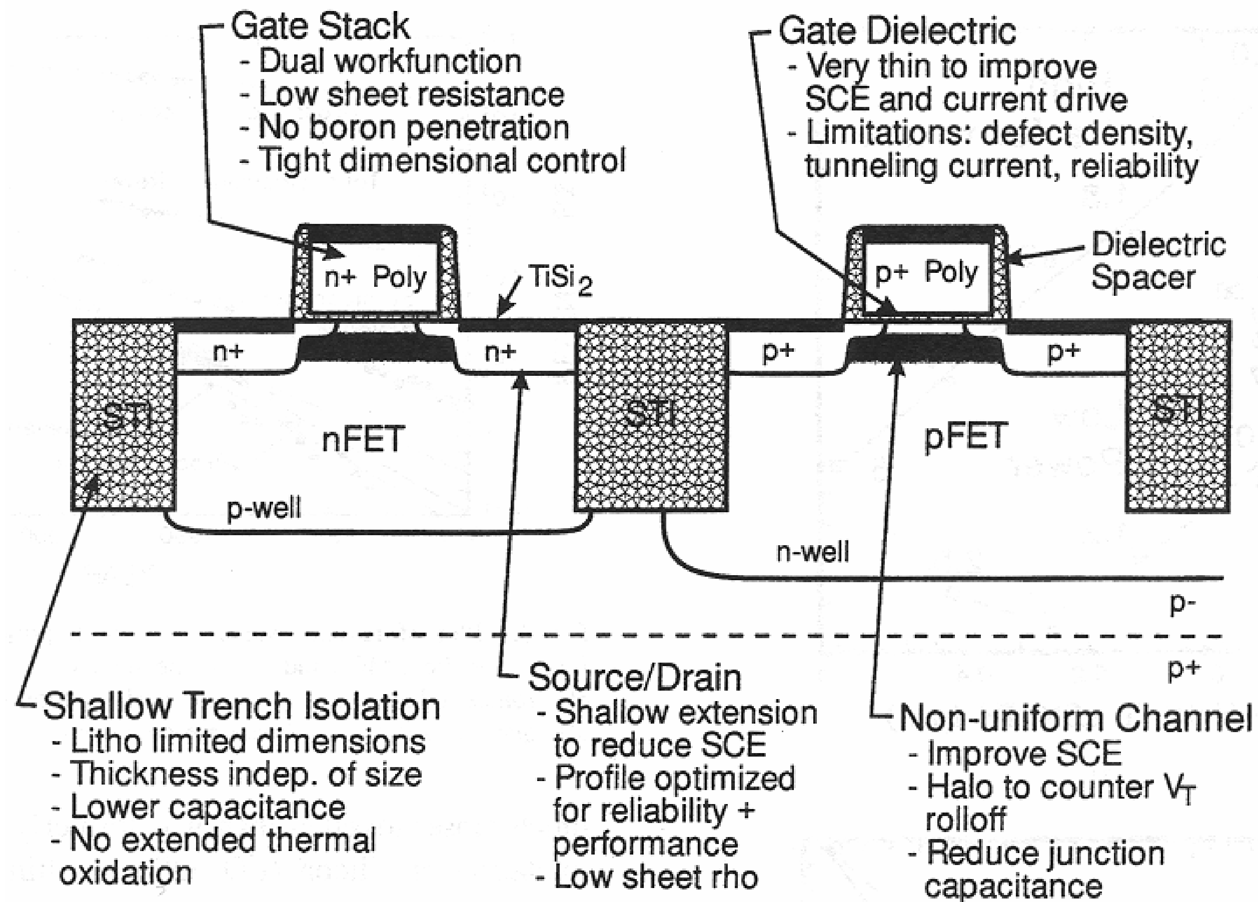
Accelerating the Rate of Technical Change

Moore's Law: Smaller, faster and cheaper logic and memory

Non-Moore's Law: 1) Adding functionality to logic and memory, 2) Electronics everywhere

What is CMOS?

CMOS = Complementary Metal Oxide Semiconductor
FET = Field Effect Transistor



Emerging Devices and Materials for Beyond CMOS

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ITRS International Technology Roadmap for Semiconductors

Possible "Red Brick Walls"

- Gate dielectric thickness <1nm
- Random dopant fluctuation
- Depletion of the polysilicon gate electrode
- Resistance of contact to devices too high

....

Table 71a Thermal and Thin Film, Doping and Etching Technology Requirements—Near-term

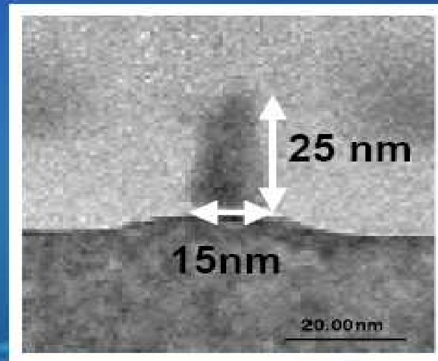
Year of Production	2003	2004	2005	2006	2007	2008	2009	Driver
Technology Node		hp90			hp65			
DRAM ½ Pitch (nm)	100	90	80	70	65	57	50	DRAM
MPU/ASIC ½ Pitch (nm)	107	90	80	70	65	57	50	MPU
MPU Printed Gate Length (nm)	65	53	45	40	35	32	28	MPU
MPU Physical Gate Length (nm)	45	37	32	28	25	22	20	MPU
Equivalent physical oxide thickness for MPU/ASIC T_{ox} (nm) [A, A1]	1.3	1.2	1.1	1.0	0.9	0.8	0.8	MPU
Gate dielectric leakage at 100°C (nA/μm) High-performance [B, B1, B2]	100	170	170	170	230	230	230	MPU

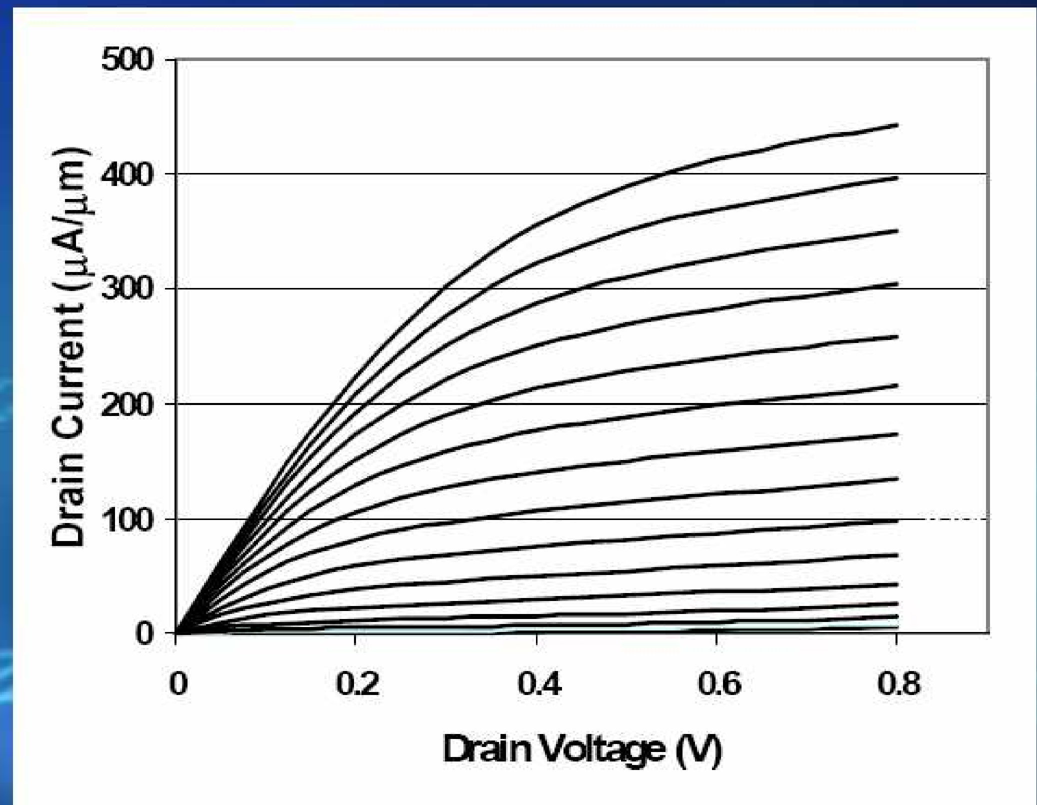
Table 71b Thermal and Thin Film, Doping and Etching Technology Requirements—Long-term

Year of Production	2010	2012	2013	2015	2016	2018	Driver
Technology Node	hp45		hp32		hp22		
DRAM ½ Pitch (nm)	45	35	32	25	22	18	DRAM
MPU/ASIC ½ Pitch (nm)	45	35	32	25	22	18	MPU
MPU Printed Gate Length (nm)	25	20	18	14	13	10	MPU
MPU Physical Gate Length (nm)	18	14	13	10	9	7	MPU
Equivalent physical oxide thickness for MPU/ASIC T_{ox} (nm) [A, A1]	0.7	0.7	0.6	0.6	0.5	0.5	MPU/ASIC
Gate dielectric leakage at 100°C (μA/μm) high-performance [B, B1, B2]	0.33	0.33	1	1.00	1.67	1.67	MPU/ASIC

But, CMOS keeps going and going and going and…

Yet another record: Intel's 15nm NMOS Transistor

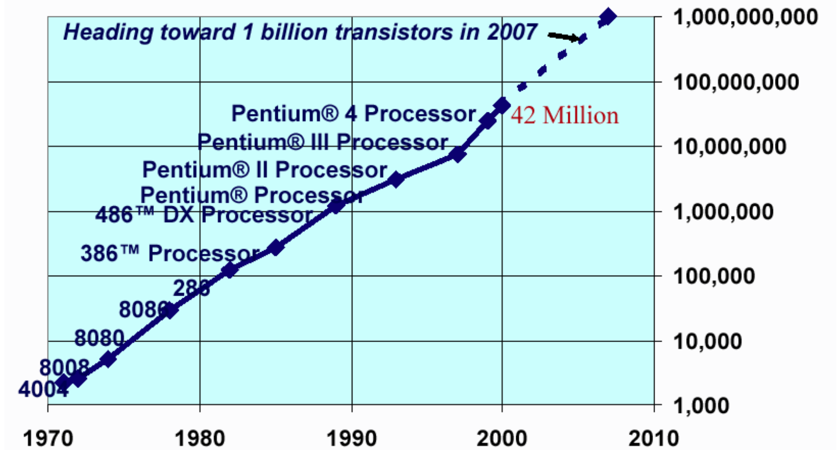


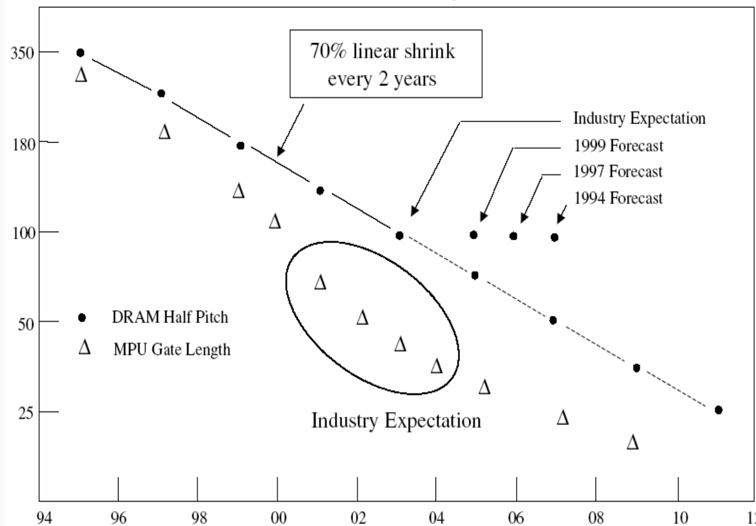


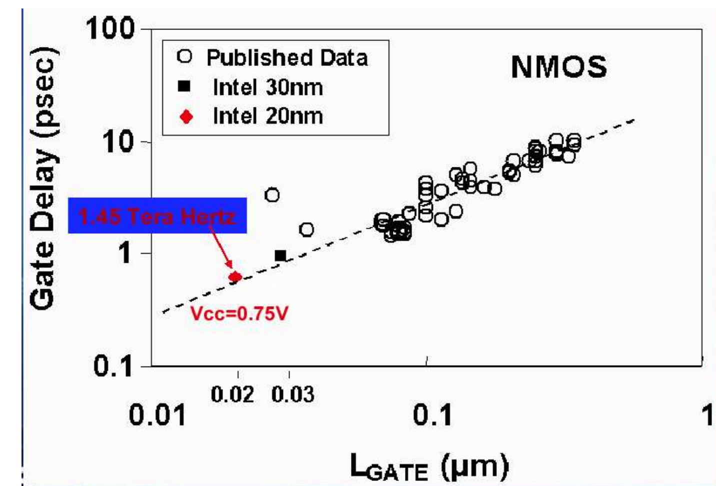
2.63 THz @ 0.8V!

What does a Beyond CMOS technology have to do to replace CMOS?

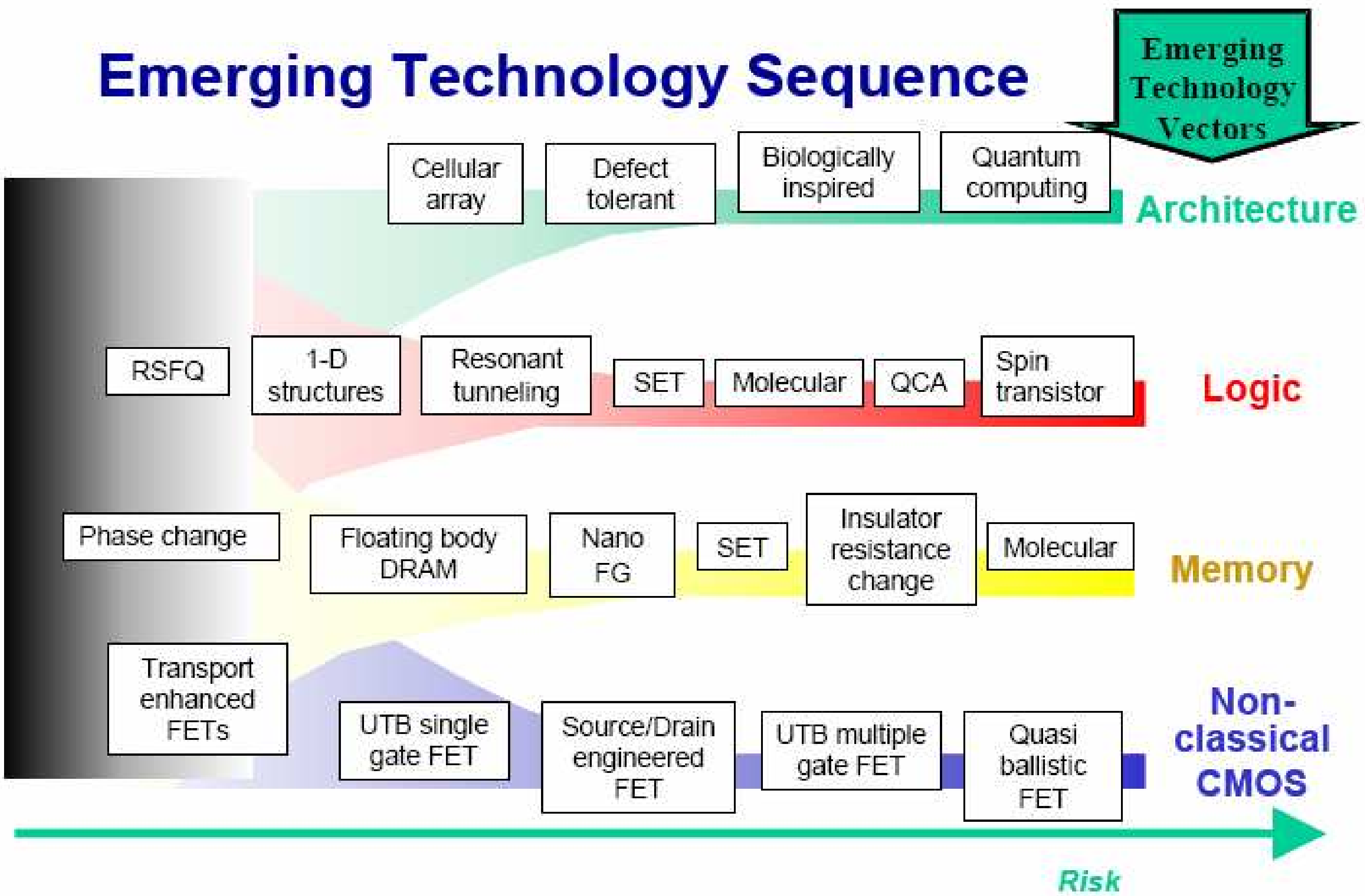
- >> 10^9 devices
- << 10 nm feature size
- << 1 psec gate delay
- <~ $4B fab
- ~ 10 year reliability



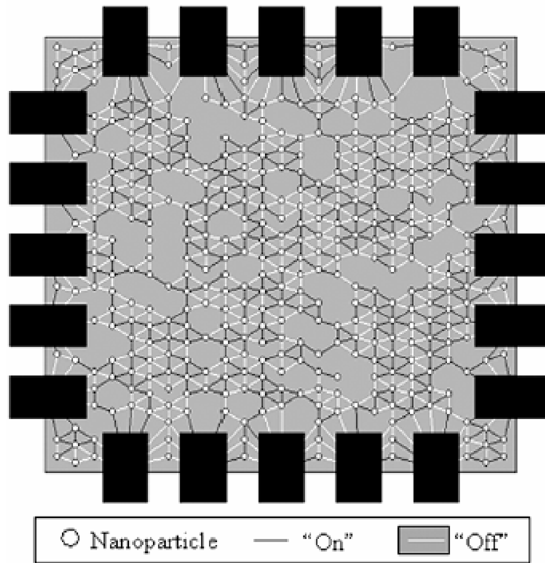




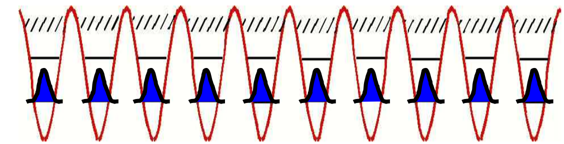
Possible Beyond CMOS Technologies



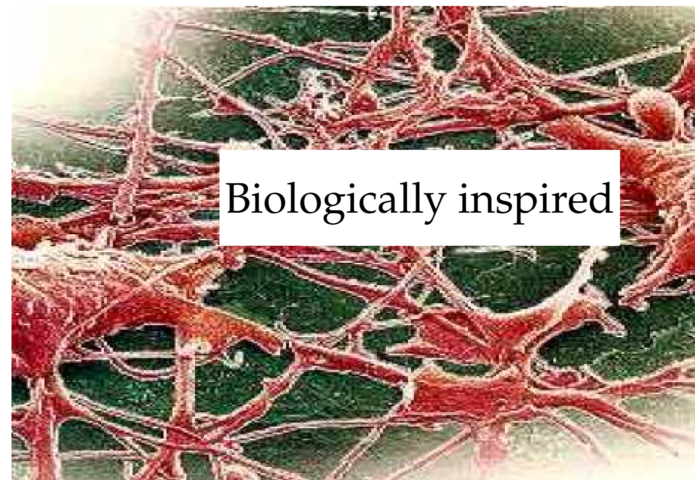
Emerging Architectures



Nanocell



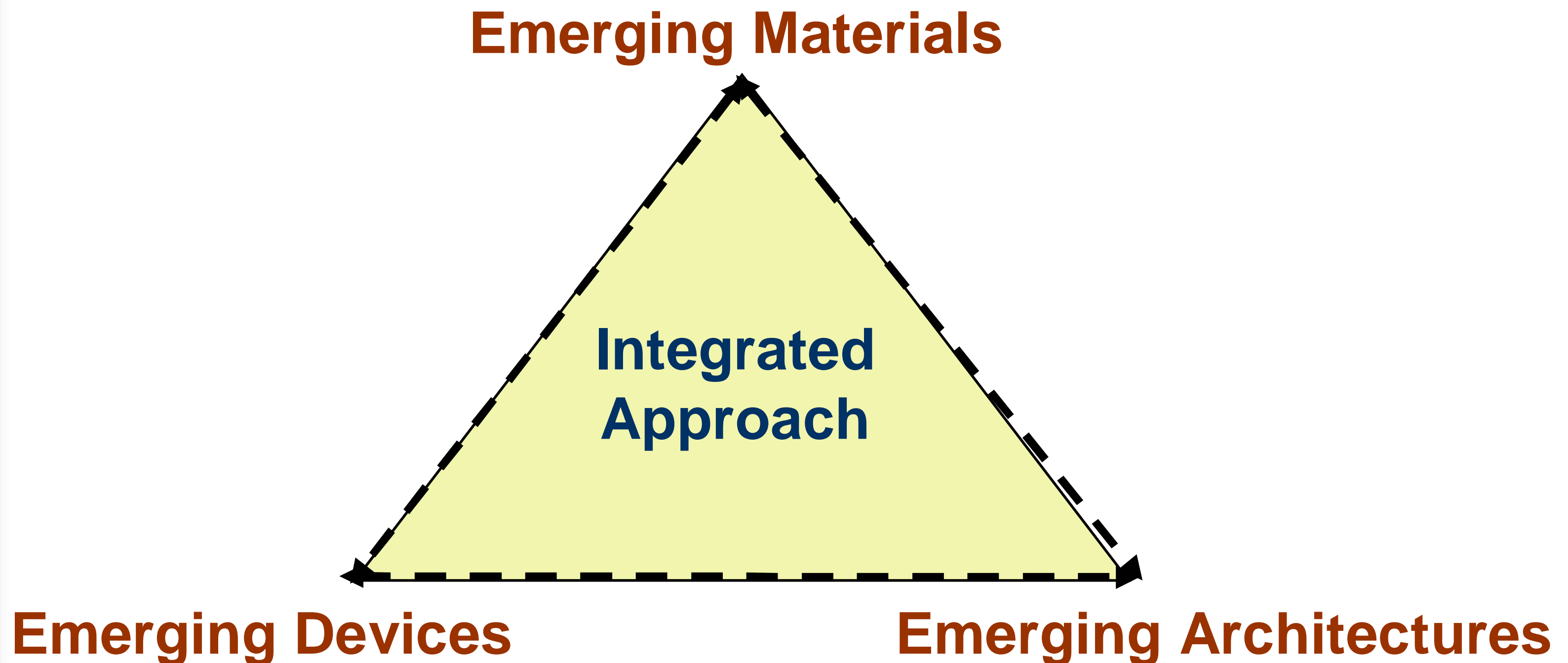
Quantum Computing



Biologically inspired

Materials, Devices, and Architectures

- There is a paradigm shift taking place in future information processing technologies.



The Missing Plateau

What Will Fill the Plateau?

- Carbon NanoTubes
- Self Assembly
- Single Molecule / Electron Devices

Missing Plateau

Quantum Computing

intel

Extracted from a talk by Dr. David Tennenhouse (V.P. for Research, Intel Corporation) entitled "Three Challenges" at a joint CIA/DARPA conference on The Global Computer Industry Beyond Moore's Law

Emerging Logic Devices

Availability Sequence		1	2	2–3	2–3	4	5	6
Device	*FET*	*RSFQ*[A,B,C]	*1D structures*	*Resonant Tunneling Devices*	*SET*	*Molecular*	*QCA*[D]	*Spin transistor*
Types	▪ Si CMOS	▪ JJ	▪ CNT FET ▪ NW FET ▪ NW hetero-structures ▪ Crossbar nanostructure	▪ RTD-FET ▪ RTT	▪ SET	▪ 2-terminal ▪ 3-terminal FET ▪ 3-terminal bipolar transistor ▪ NEMS ▪ Molecular QCA	▪ E: QCA** ▪ M: QCA**	▪ Spin FET (SFET) ▪ Spin-valve transistor (SVT)
Supported Architectures	▪ Conventional	▪ Pulse	▪ Conventional ▪ Cross-bar	▪ Conventional ▪ CNN	▪ CNN	▪ Memory-based ▪ QCA	▪ QCA	▪ Quantum ▪ Programmable logic
Cell Size (spatial pitch)	100 nm*	0.3 µm	100 nm*	100 nm*	40 nm	Not known	60 nm	100 nm*
Density (device/cm^2)	3E9	1E6	3E9	3E9	6E10	1E12	3E10	3E9
Switch Speed	700 GHz	1.2 THz	Not known	1 THz	1 GHz	Not known	30 MHz	700 GHz
Circuit Speed	30 GHz	250–800 GHz	30 GHz	30 GHz	1 GHz	<1 MHz (NEMS)	1 MHz	30 GHz
*Switching Energy, J****	2×10^{-18}	2×10^{-19}(Nb) [$>1.4\times10^{-17}$]	2×10^{-18}	$>2\times10^{-18}$	1×10^{-18} [$>1.5\times10^{-17}$][C]	1.3×10^{-16} (NEMS)	[E:$>1\times10^{-18}$][E] M:$>4\times10^{-17}$	2×10^{-18}
Binary Throughput, GBit/ns/cm^2	86	0.4	86	86	10	N/A	0.06	86
Gain	Must be >>1 for all devices. See Table 63b for experimental values							
Operational Temperature	RT	▪ 4 K (Nb) ▪ 77 K (HTS) ▪ 20 K(MgB$_2$)	RT	RT	20 K	RT	E:QCA Cryogenic M:QCA RT	▪ Cryogenic (SFET) ▪ RT (SVT)
CD Tolerance	Critical	Not critical	Not critical	Very critical	Very critical	Not critical	Very critical <2% (M: QCA)	Critical
Materials System	Si	Nb HTS	CNT Si III-V	III-V Si-Ge	III-V Si	C-60	Al/Al$_2$O$_3$ (E: QCA)	▪ III-V (SFET) ▪ Si/FM (SVT)
Most Complex Circuit Demonstrated	See Table 63b							

Emerging Memory Devices

Table 62a Emerging Research Memory Devices—Projected Parameters

	Present Day Baseline Technologies		*Phase Change Memory**	*Floating Body DRAM*	*Nano-floating Gate Memory***	*Single/Few Electron Memories***	*Insulator Resistance Change Memory***	*Molecular Memories***
Storage Mechanism								
Device Types	DRAM	NOR Flash	OUM	1TDRAM	Engineered tunnel barrier or nanocrystal	SET	MIM	Bi-stable switch
Availability	2004	2004	~2006	~2006	>2006	>2007	~2010	>2010
Cell Elements	1T1C	1T	1T1R	1T	1T	1T	1T1R	1T1R
Initial F	90 nm	90 nm	100 nm	70 nm	80 nm	65 nm	65 nm	45 nm
Cell Size	$8F^2$ 0.065 μm^2	$12.5F^2$ 0.101 μm^2	~$6F^2$ 0.06 μm^2	~$4F^2$ [A] 0.0049 μm^2	~$6F^2$ 0.038 μm^2	~$6F^2$ 0.025 μm^2	~$6F^2$ 0.025 μm^2	Not known
Access Time	<15 ns	~80 ns	<100 ns	<10 ns [A,B]	<10 ns	<10 ns	Slow	~10 ns
Store Time	<15 ns	~1 ms	<100 ns	<10 ns [A,B]	<10 ns	<100 ns	<100 ns	~10 ns
Retention Time	64 ms	10–20 yrs	>10 yrs	<10 ms [A]	>10 yrs	~100 sec	~1 year	~1 month
E/W Cycles	Infinite	1E5	>1E13	>1E15 [A]	>1E6	>1E9	>1E3	>1E15
General Advantages	▪ Density ▪ Economy	▪ Non-volatile ▪ Multi-bit cells	▪ Non-volatile ▪ Low power ▪ Rad hard ▪ Multi-bit cells	▪ Density ▪ Economy	▪ Non-volatile ▪ Fast read and write ▪ Multi-bit cells	▪ Density ▪ Low power	▪ Low voltage ▪ Multi-bit cells	▪ Density ▪ Low power ▪ 3D potential ▪ Defect tolerant
Challenges	▪ Scaling	▪ Scaling	▪ Large E/W current ▪ New materials and integration	▪ Need SOI ▪ Retention versus scaling ▪ Dopant fluctuation ▪ Endurance	▪ Material quality	▪ Dimension control for RT operation ▪ Background charge disturb	▪ New materials and integration ▪ Slow access ▪ Speed versus R trade-off	▪ Volatile ▪ Thermal stability
Maturity	Production	Production	Development	Demonstrated	Research	Research	Research	Research
*Research Activity*****			3***	3	61	40	3	43

Emerging Devices and Materials for Beyond CMOS

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NanoElectronic Device Metrology Project (Curt Richter)

Goal: Develop metrology that will enable emerging information processing technologies to extend electronic device performance improvements beyond the incremental scaling of CMOS

Molecular Electronic Test Structures (METS): Developing test structures and accompanying measurement methods that enable reliable, reproducible electrical measurements of molecules to investigate molecular conduction mechanisms.

Self-assembly based fabrication paradigm

Si-Based NanoElectronics: Developing the precise metrology required for Si-based nanoelectronics. Focus on the electrical and physical metrology of the basic building blocks of confined-silicon devices (e.g., quantum layers, wires, and quantum-dots).

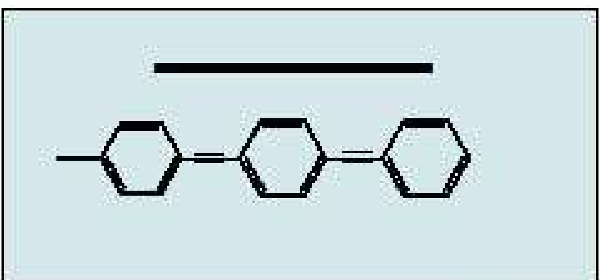
Extrapolation of CMOS top-down fabrication.

Molecular Electronics

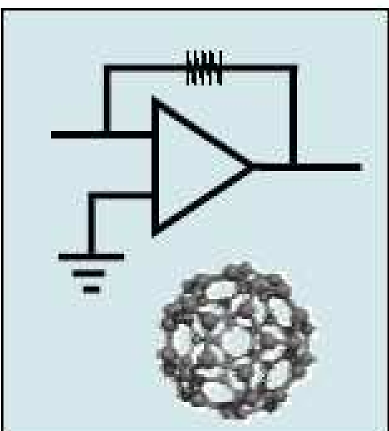
"moletronics"

Moletronics: A new technology that uses molecules to perform the function of electronic components.

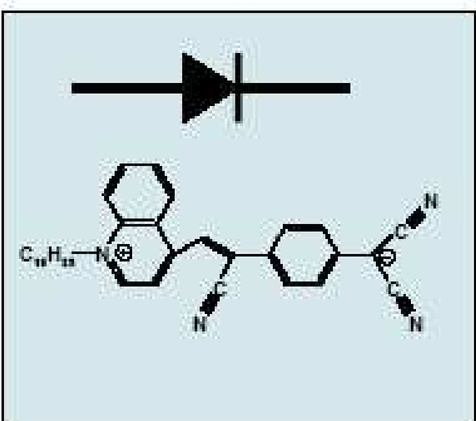
wire



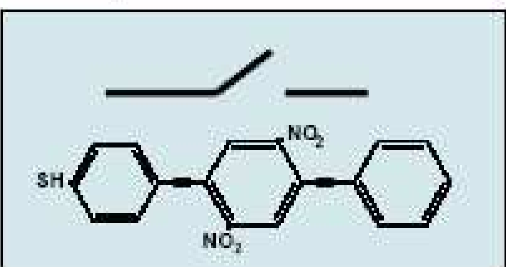
amplifier



diode

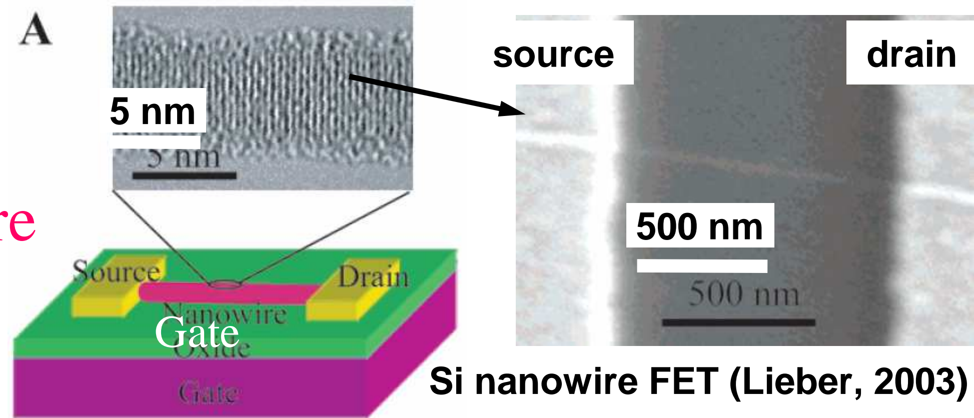


switch

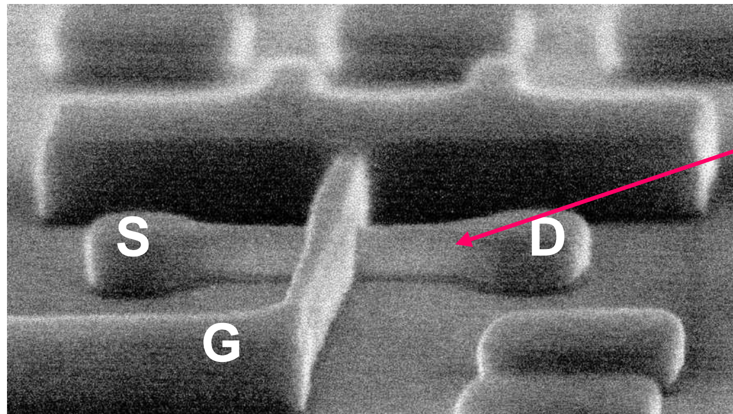


Silicon Nanowires

Bottom-up silicon nanowire



Si nanowire FET (Lieber, 2003)



Top-down Silicon nanowire

Intel

2 Primary Characterization Needs for Emerging Devices and Materials

- **2D/3D** resolved, non-destructive, timely characterization of chemical, structural, electrical (e.g. spin, DOS), and atomic bonding at the nano-/atomic- scale.
  - We are "blind" at the nanoscale.
  - Should include need of subsurface characterization of interfaces (specifically organic/inorganic).
  - Include target spatial resolution and atomic sensitivity.

- **Electrical metrology and test structures**/vehicles for timely characterization of electronic properties of nanoscale components (e.g. molecules, nanotubes, nanowires) independent of the contacts

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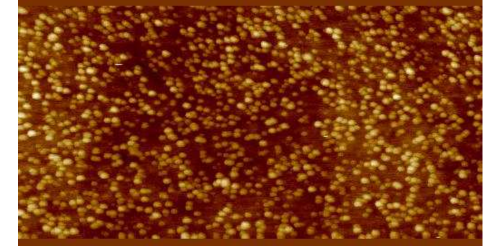
3D Physical Characterization

Defining and developing metrology for future nanoelectronics

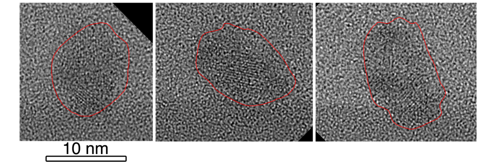
- The measured size of the quantum dots determined using AFM is larger than that determined using TEM.

- Quantum dot memories generally show large retention time that is strongly dependent on the size and distribution of the dots.

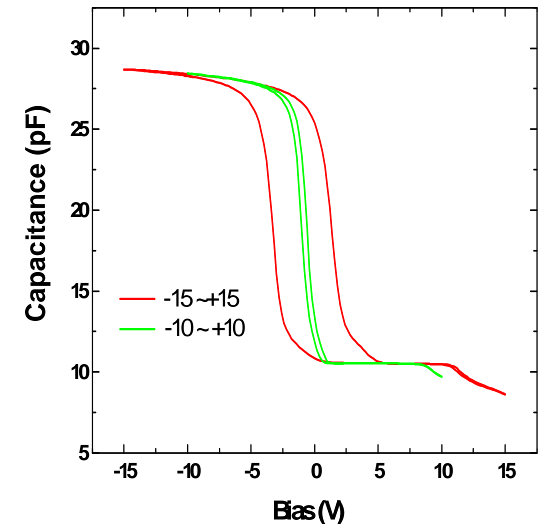
AFM



TEM



C-V



†J. Park, C. A. Richter, J. Y. Kim, N. V. Nguyen, J. E. Bor
'Characterization of ultrathin amorphous silicon and correlation with crystalline evolution after thermal annealing,' 2003 MRS Spring Meeting.

3D Physical Characterization

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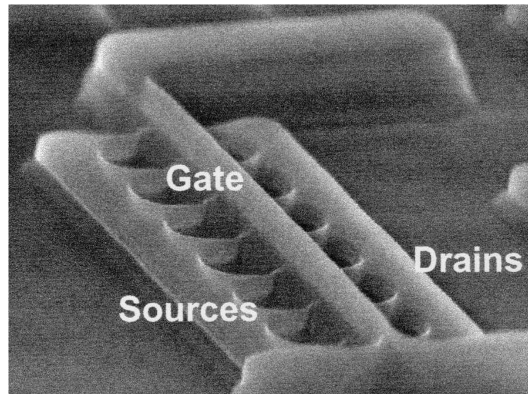
Emerging Devices and Materials for Beyond CMOS

FIN/Tri-gate FETs are based upon Si-nanowires

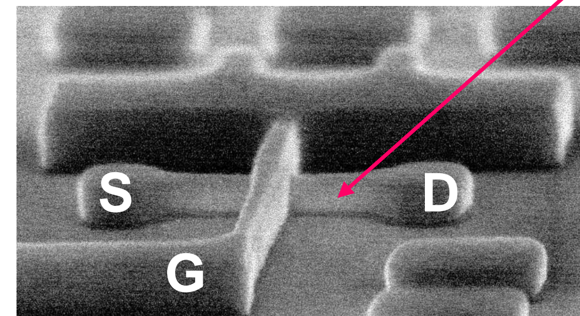
Need to monitor:

- 3D properties…
  - Accurate size of wire (is it critical to performance?)
  - Film thicknesses (ie, gate dielectric) on a 3D structure
- 3D Processing parameters (example):
  Pattern/orientation dependent oxidation?



Multiple Si-nanowire FET

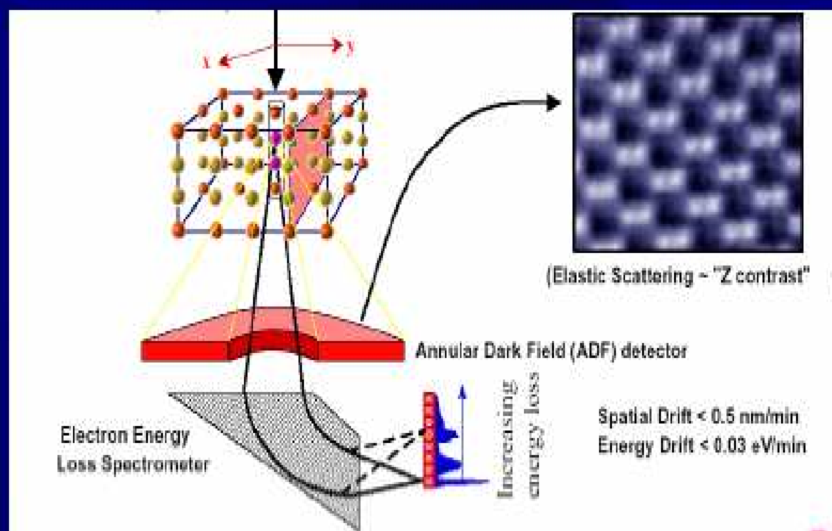
Silicon nanowire



Intel

3D Chemical Imaging

- The holy grail of characterization and chemical measurement:
  - Know each atom and relationship to all others
  - Where one or more atoms well placed or misplaced can make or break a nanodevice



Courtesy David Muller, Cornell

NIST

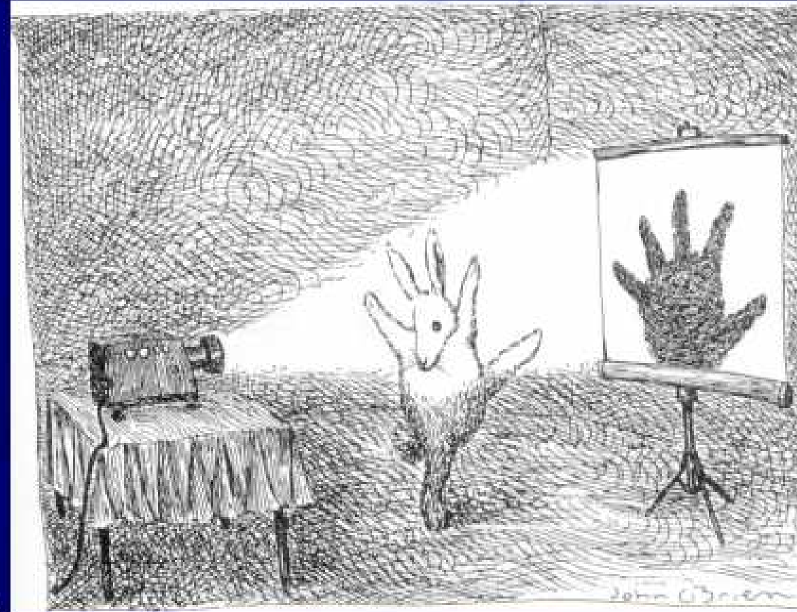
NIST/NNI Workshop – J. H. Scott (NIST, CSTL)

3D Chemical Imaging

Need for 3D Chemical Reconstruction

Projection and Surface Images are Limiting

- **Currently most used approach is 2D projection or surface morphologic imaging with limited chemical mapping**
- **This approach can easily lead to misinterpretation**
- **Chemical 3D information is now often required to determine true nature of working nanodevices and their failure modes**



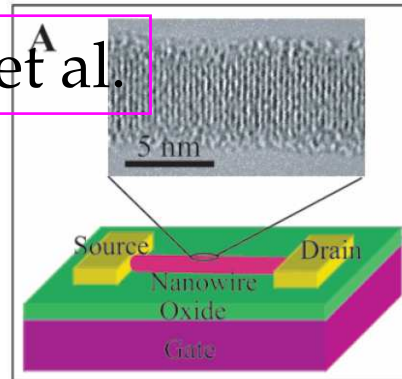
Drawing by John O'Brien, The New Yorker Magazine (1991)

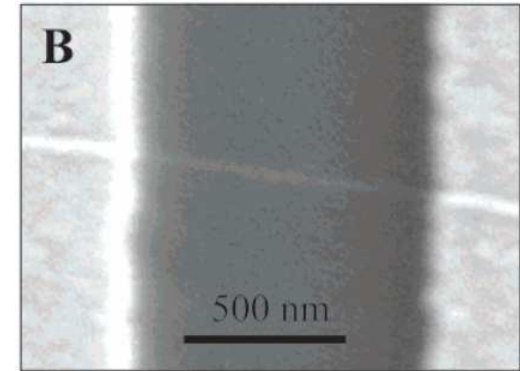
NIST

NIST/NNI Workshop – J. H. Scott (NIST, CSTL)

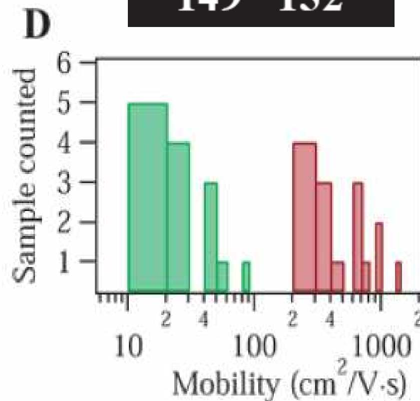
Test Structures for Electrical Characterization

SiNW FETs – Lieber et al.





NANO LETTERS
2003
Vol. 3, No. 2
149−152



Hole mobility extracted using simple measurements and very approximate models was as high as $1350cm^2/Vs$

Recent results by Lieber et al. suggest that silicon nanowires may have hole mobility much greater than that of bulk silicon => this result was in question.

Emerging Devices and Materials for Beyond CMOS

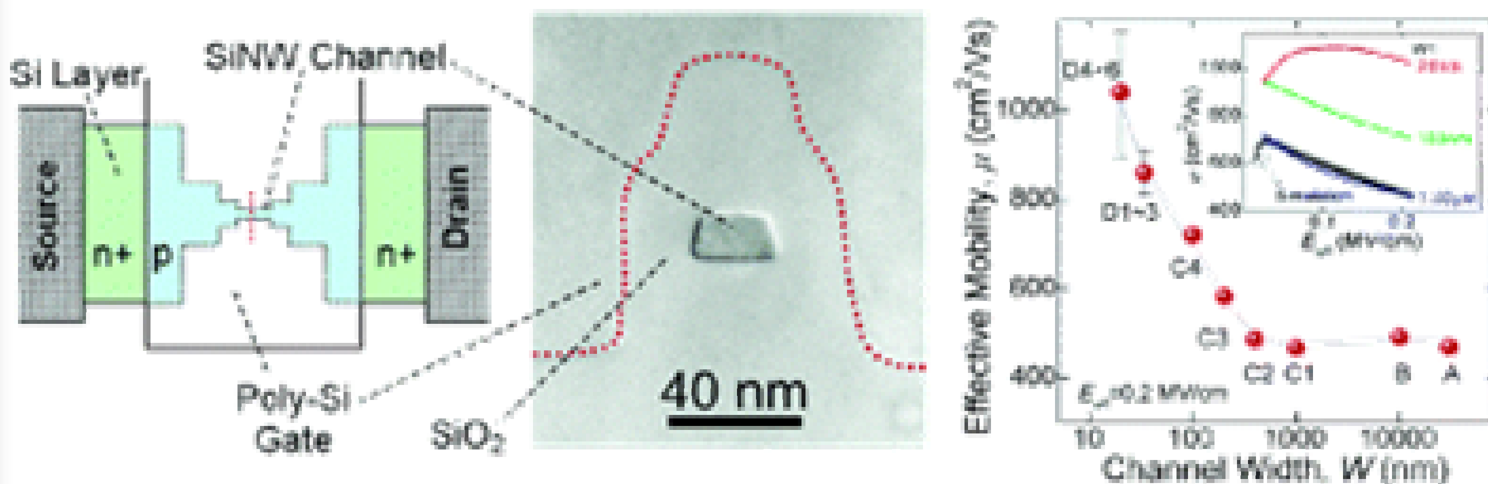
The Semiconductor Electronics Division

Test Structures for Electrical Characterization

High Inversion Current in Silicon Nanowire Field Effect Transistors

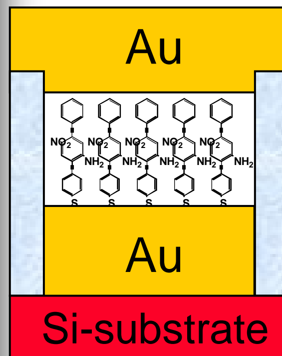
Sang-Mo Koo, Akira Fujiwara, Jin-Ping Han, Eric M. Vogel,
Curt A. Richter, and John E. Bonevich

Web Release Date: 30-Sep-2004; *NanoLetters*



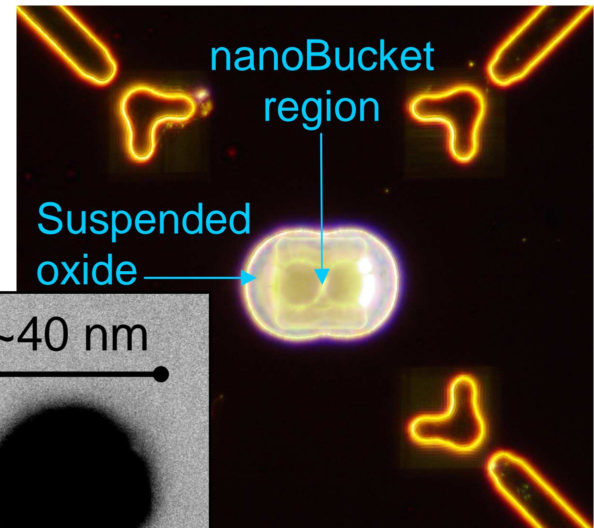
Test Structures for Electrical Characterization

A Device prototype that enables robust electrical measurements of molecules



Schematic of planar nanoBucket

Criteria:
- Characterizes Molecules
- Tunable to fit Molecules
- Prototypical Device Structure
- "Makeable" (i.e., transferable)



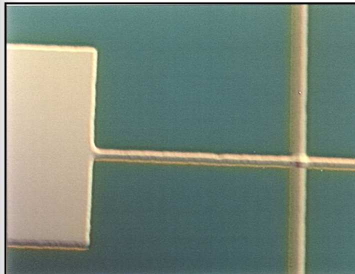
Fully suspended nanoBucket: one example

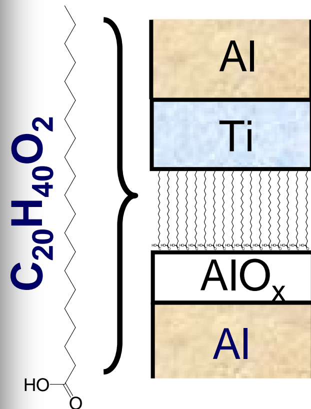
Major Objective:
- **A NIST suite of robust molecular electronics test structures.**

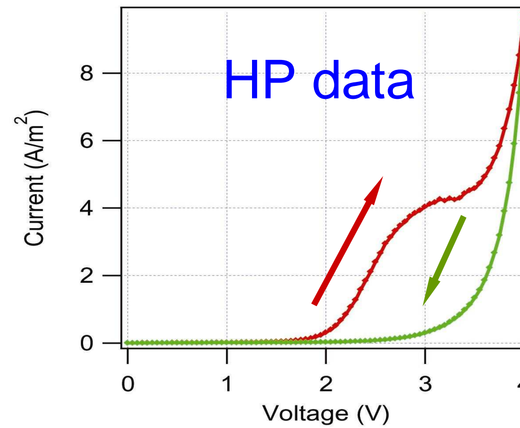
NanoBuckets allow control:
- Variety (contacts & molecules)
- Depth (molecular length)
- Area (no. of molecules)

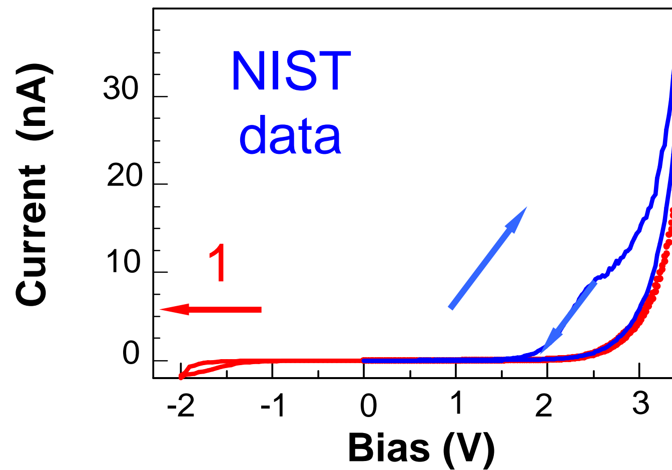
Measure the molecules, not artifacts of the METS

Test Structures for Electrical Characterization



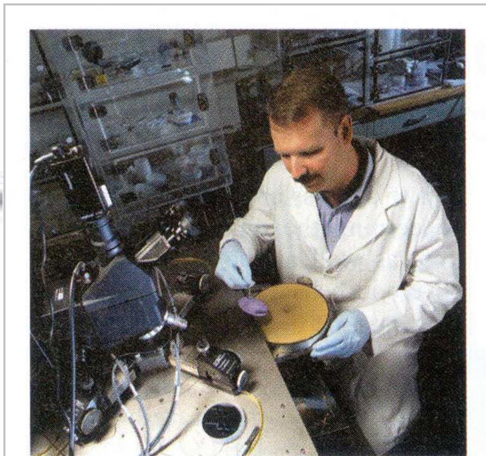






CA Richter (NIST) & DR Stewart (HP)

- **First independent confirmation of molecular device behavior. (Switching observed at both NIST and HP.)**



NIST researchers are developing meth-
ods for testing the electrical properties

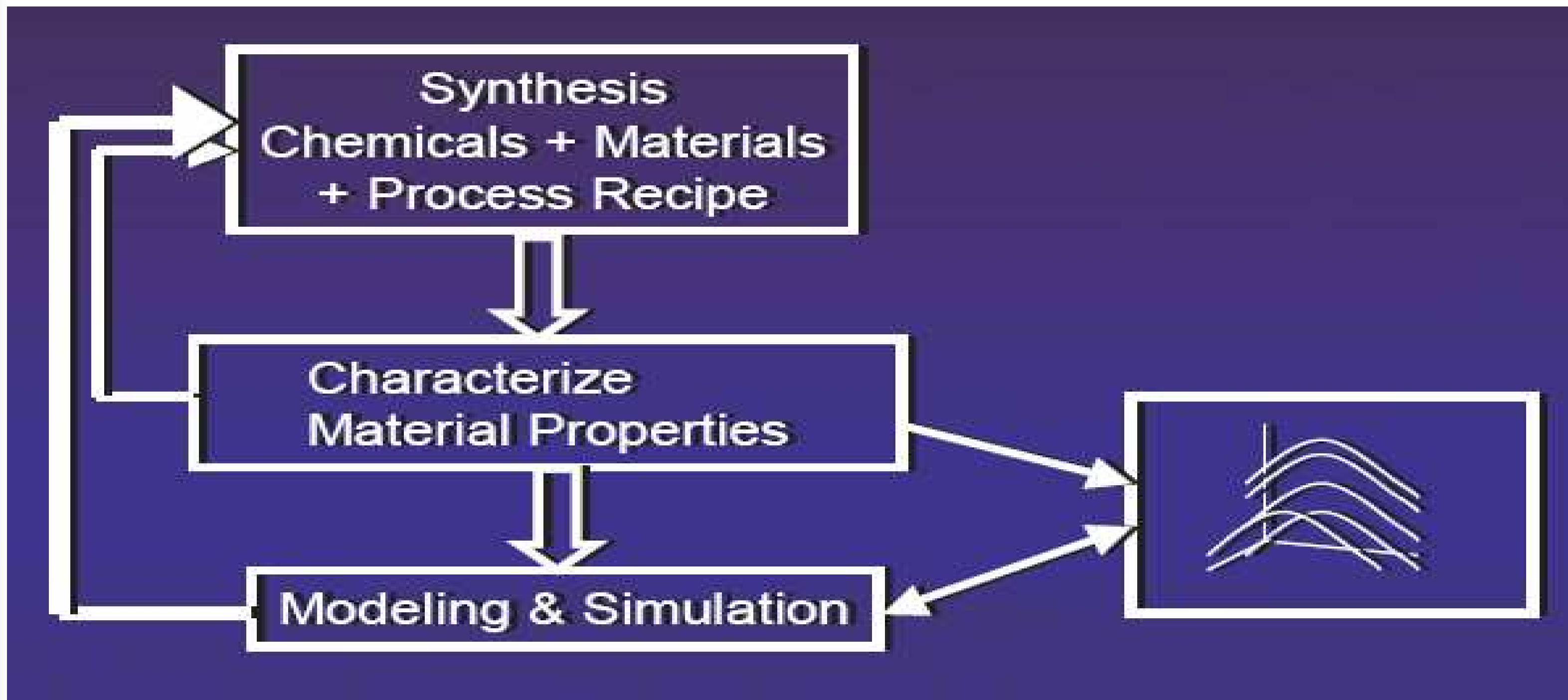
Device = Molecules + Electrodes

Critical Interplay between Modeling/Sim. & Characterization

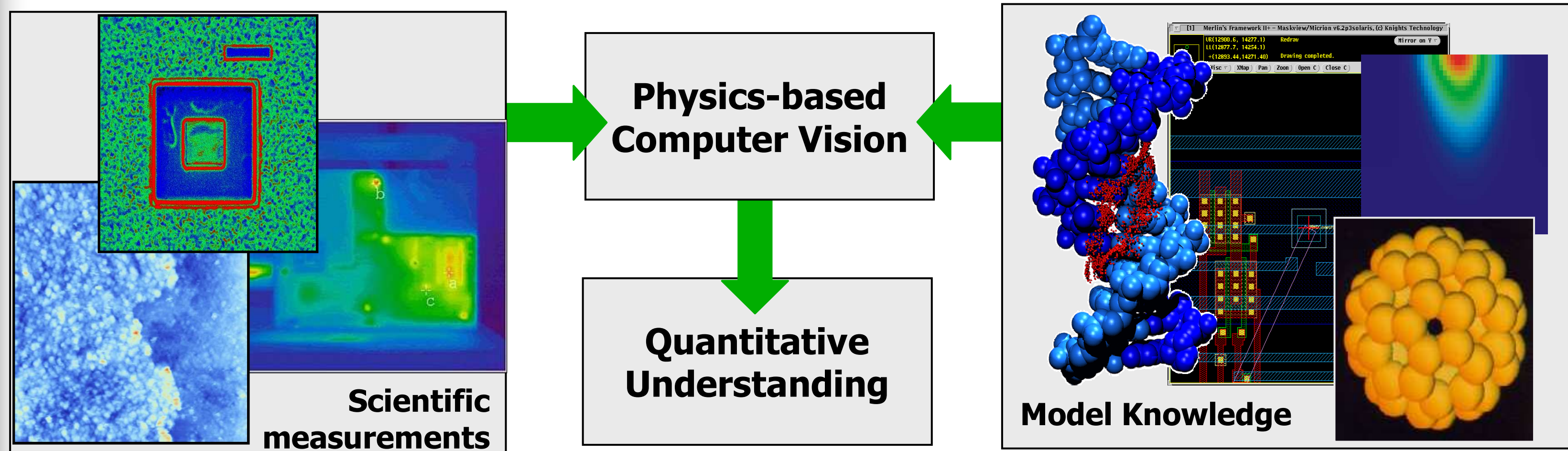
<u>**Two categories of modeling/characterization interactions**</u>:

• Models and simulations necessary to interpret a physical or electrical measurement.

• Physical or electrical characterization necessary to confirm a model or simulation of a novel material, device structure, or process.



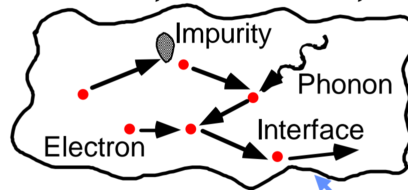
Modeling/Simulation to Interpret Characterization



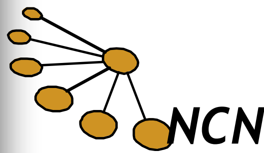
- Metrology interacts with with nanoscale properties, and confounds the measured properties
- Need to decouple metrology interaction with material
- Interpret images in conjunction with physical models.

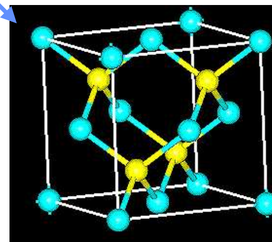
NEMO (Nanoelectronic Modeling)

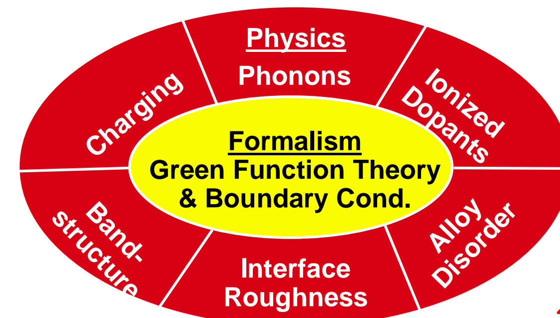
- NEMO 1-D was developed under a NSA/NRO contract to Texas Instruments and Raytheon from ‘93-’98 (>50,000 person hours, 250,000 lines of code).
- NEMO 1-D maintained and NEMO 3-D developed at JPL ‘98-’03 (>14000 person hours) under JPL, NASA funding. Since ‘02 NSA and ONR funding.
- NEMO is THE state-of-the-art quantum device design tool.
  - First target: transport through resonant tunneling diodes (high speed electronics).
  - Second target: electronic structure in realistically large nano devices (detectors).
  - Newly set target: qbit device simulation.
- Bridges the gap between device engineering and quantum physics.
- Based on Non-Equilibrium Green function formalism NEGF - Datta, Lake, and Klimeck.
- Used at Intel, Motorola, HP, Texas Instruments, and >10 Universities.



G. Klimeck, Purdue



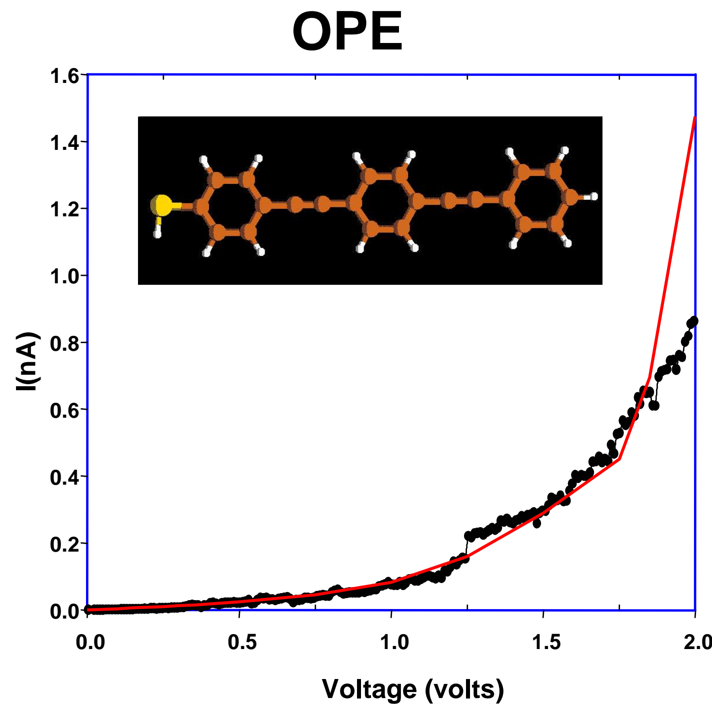


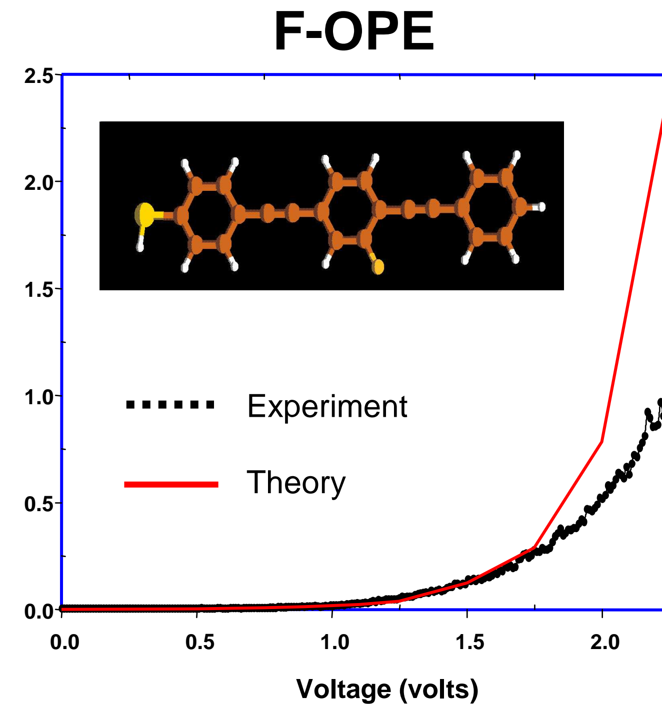


Morgan State University - Northwestern University - Purdue University - Stanford University - University of Florida - University of Illinois - University of Texas at El Paso

Rapid Modeling and Simulation

Validation of new theoretical methods for rapid assessment of charge transport . . .





"A Quasi-molecular Approach to the Conductance of Molecule-Metal Junctions: Theory and Application to Voltage-Induced Conductance Switching," C. Gonzalez, Y. Simón-Manso, J.D. Batteas, M. Marquez, M. Ratner and V. Mujica, *J. Phys. Chem.* (2004) in press.

Div. 838: Carlos Gonzalez

Summary

- The future of electronics (accelerating the rate of technical change): Moore's Law (faster, smaller, cheaper), Non-Moore's Law #1 (adding functionality to CMOS), Non-Moore's Law #2 (electronics everywhere).
- There are many "red brick walls" for CMOS technology but it will likely continue for ~15 years (10^9 devices, 10 nm feature size,sub-ps gate delay).
- There are numerous emerging architectures, logic & memory devices, and materials that are being researched for Beyond CMOS.
- There are 2 primary characterization needs for Beyond CMOS: 1) 3D physical characterization, 2) reliable electrical test structures.
- There are 2 primary modeling/simulation needs for Beyond CMOS: 1) interpretation of measurements, 2) both fundamental and fast modeling/simulation of nano-devices and –materials.

The Semiconductor Electronics Division

Emerging Devices and Materials for Beyond CMOS

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- ITRS Emerging Research Devices and Materials Technical Working Groups
- NIST/NNI Instrumentation and Metrology for Nanotechnology Grand Challenge Workshop, January 27-29, 2004.
- CMOS and Novel Devices Group, Semiconductor Electronics Division:
- Dr. Curt Richter, Leader, Nanoelectronic Device Metrology Project
- Dr. Michael Gaitan, Leader, MEMS Project