The CDF Silicon Vertex Trigger

Beauty 2005

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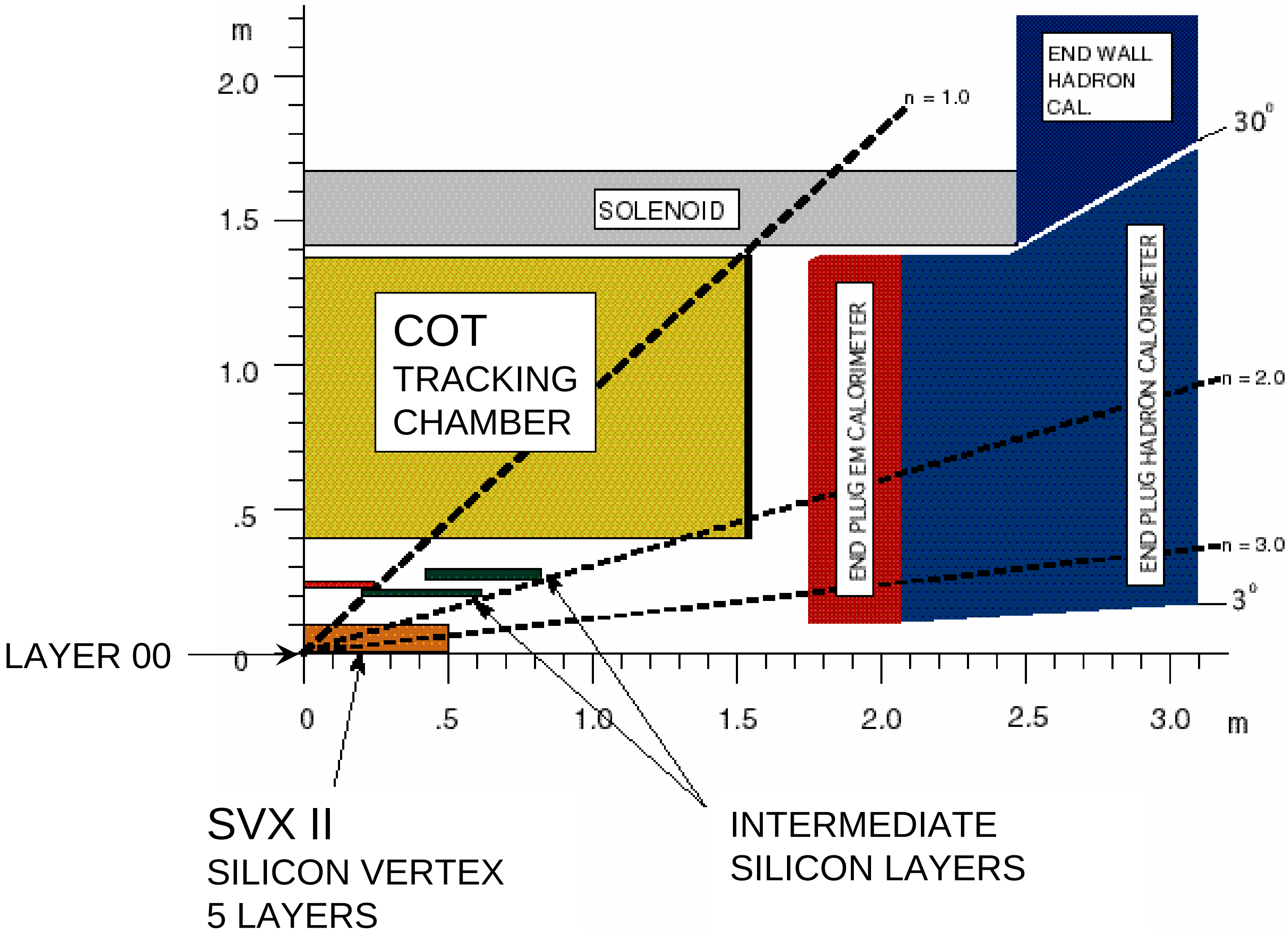
Outline

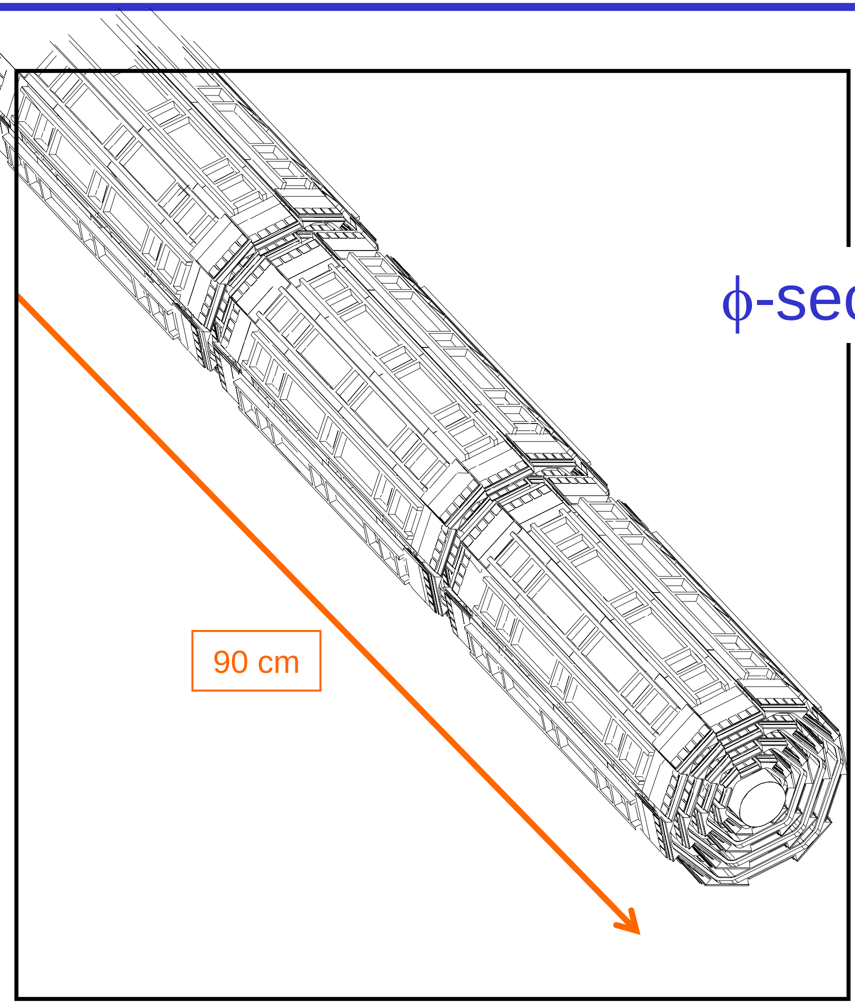
- CDF and the Silicon Vertex Trigger (SVT)
- Motivations
- Design
- Performance
- Upgrade
- Conclusions

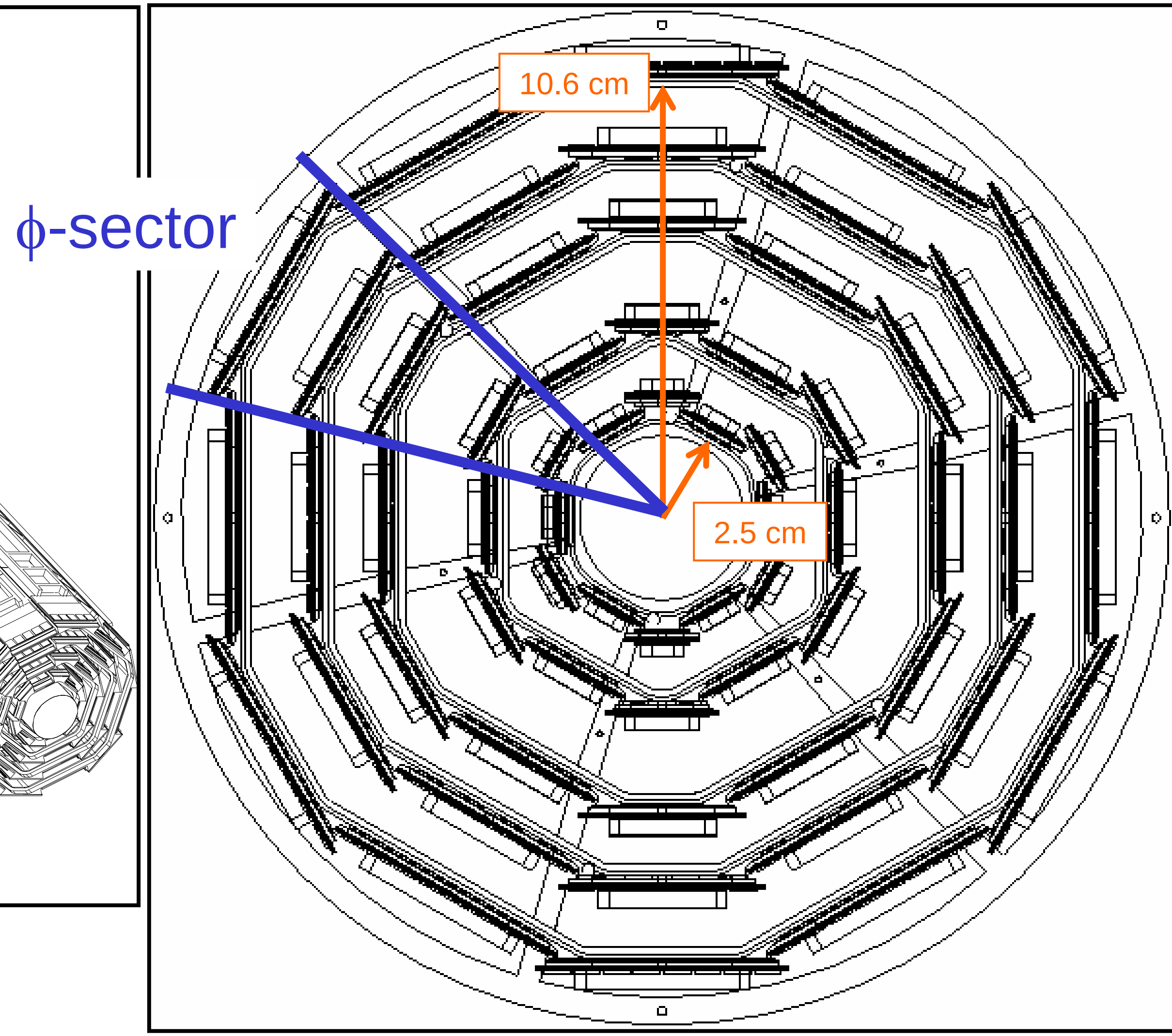
CDF r-z view

SVT



SVX II





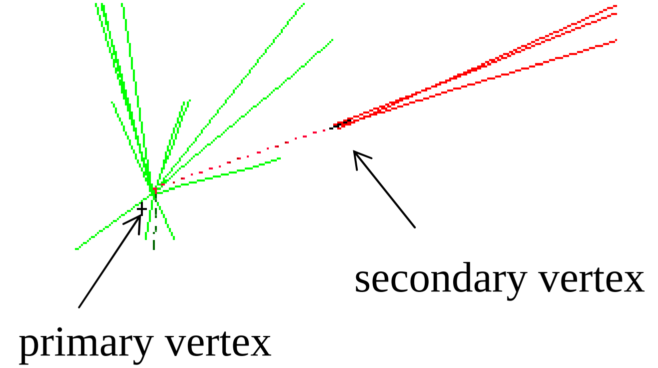
Why and how?

- Trigger on B hadronic decays
  - B physics studies, eg. CP violation in B decays, Bs mixing
  - new particle searches, eg. Higgs, Supersymmetry

- A b-trigger is particularly important at hadron colliders
  - large B production cross section for B physics
  - high energy available to produce new particles decaying to b quarks
  - overwhelming QCD background O(10^3)
    - need to improve S/B at trigger level

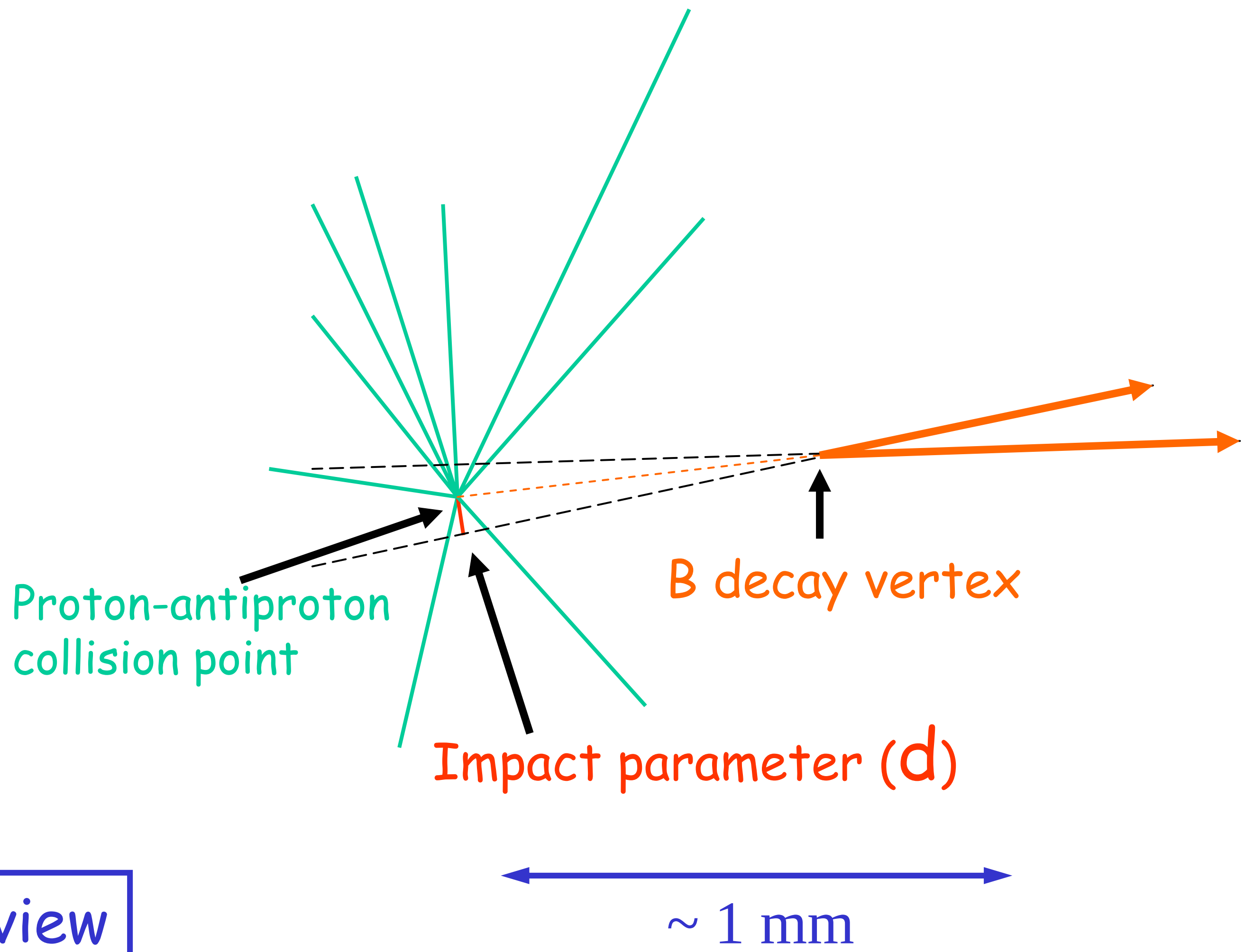
- Detect large impact parameter tracks from B decays using the fact that τ(B)$\approx$1.5 ps

Technical challenge!



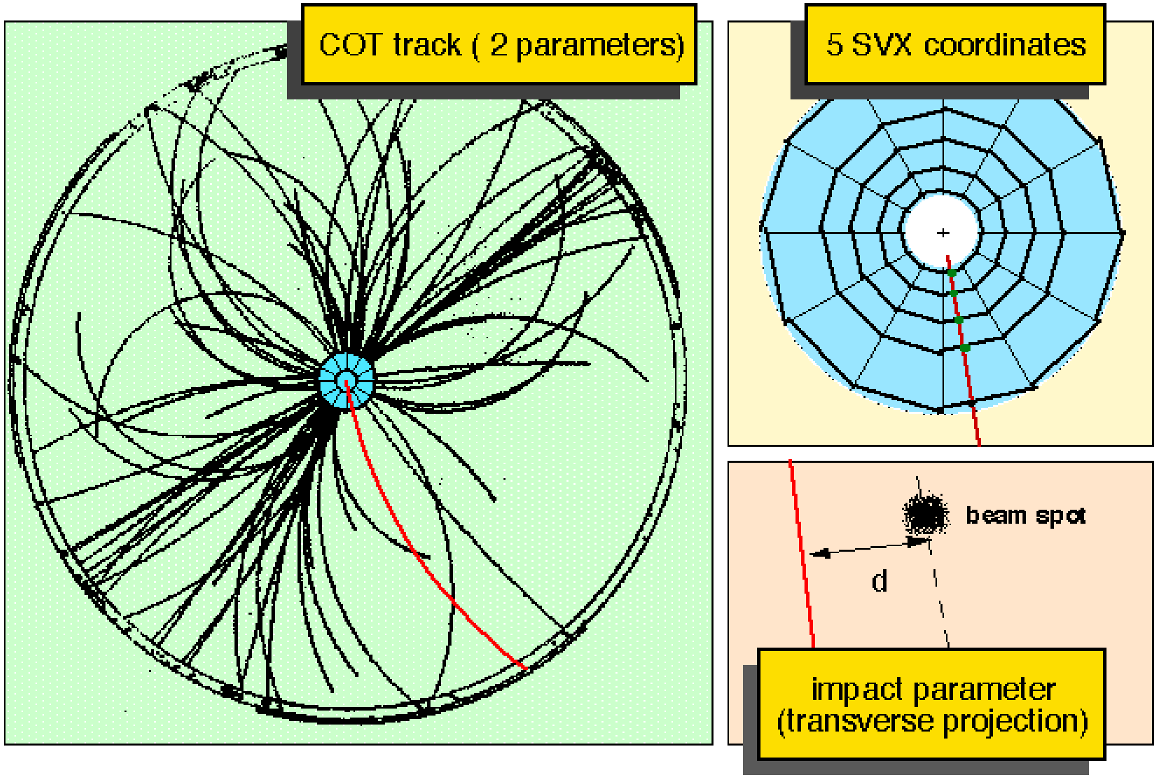
Exploit lifetime to select b,c

SVT



Transverse view

SVT: Input & Output



Inputs:

- **L1 tracks from XFT (ϕ, p_T)**
- **digitized pulse heights from SVX II**

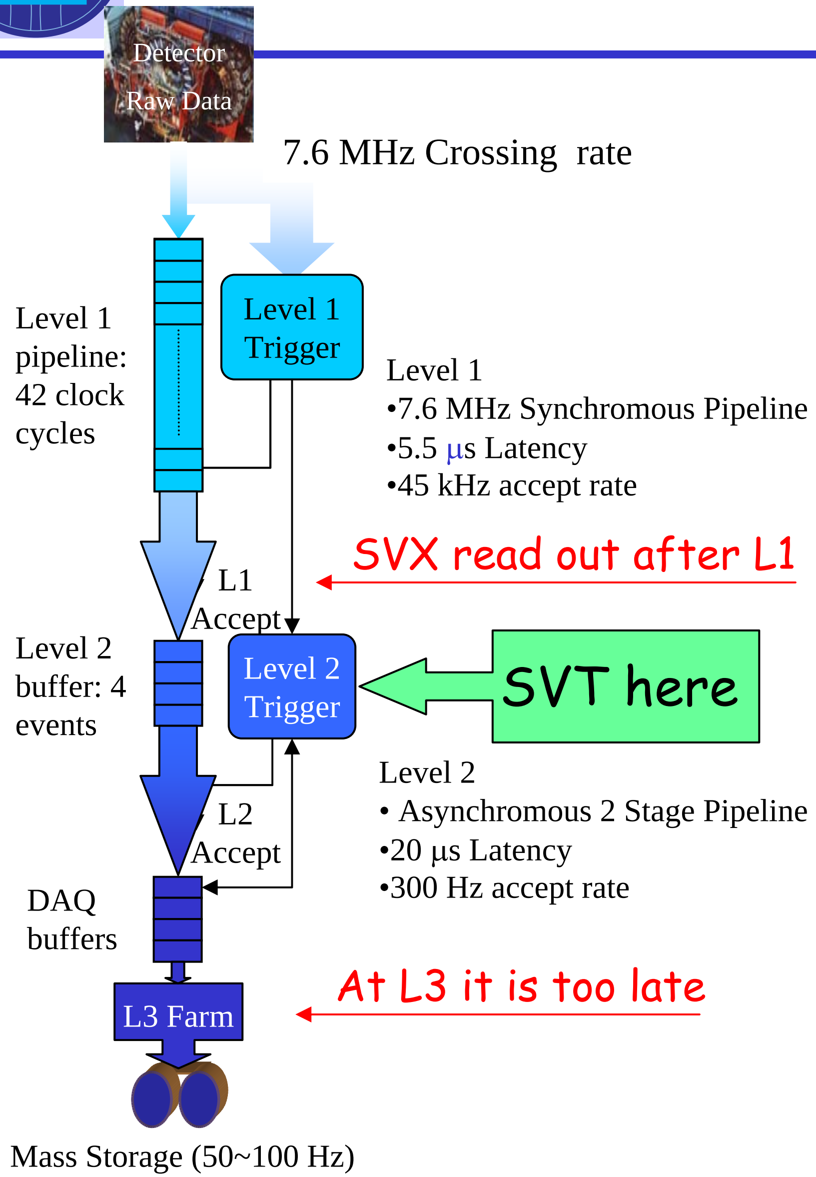
Functionalities:

- **hit cluster finding**
- **pattern recognition**
- **track fitting**

Outputs:

- **reconstructed tracks (d, ϕ, p_T)**

SVT Design Constraints

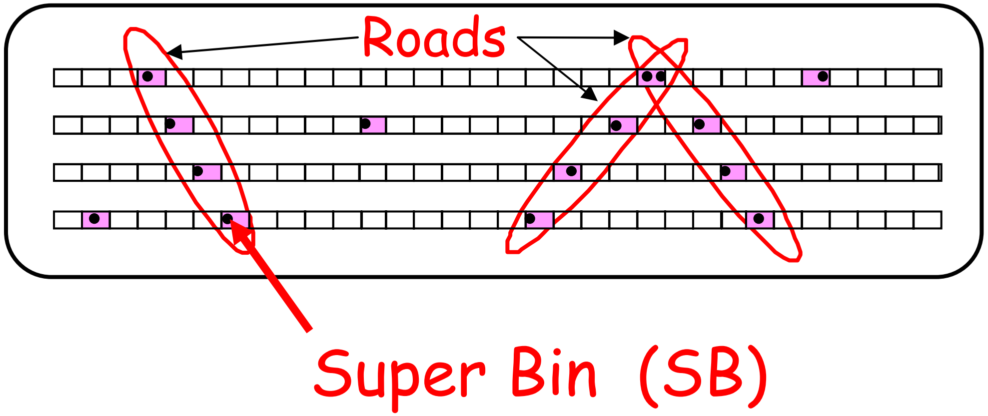


- **45 kHz input rate**
- **O(10^3) SVX strips/event**
- **2-D low-res COT tracks**

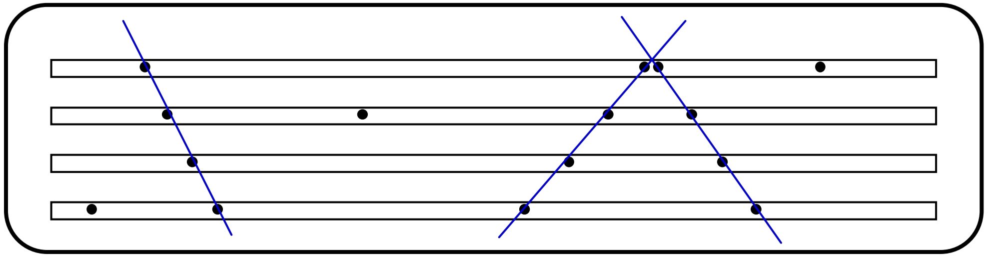
- **Latency O(10) μsec**
- **No Dead Time**
- **Resolution ≈offline**

Tracking in 2 steps

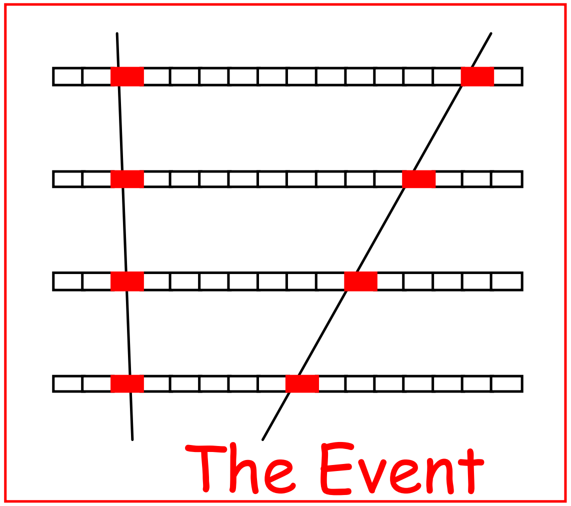
1. Find low resolution track candidates called "roads".
   Solve most of the pattern recognition

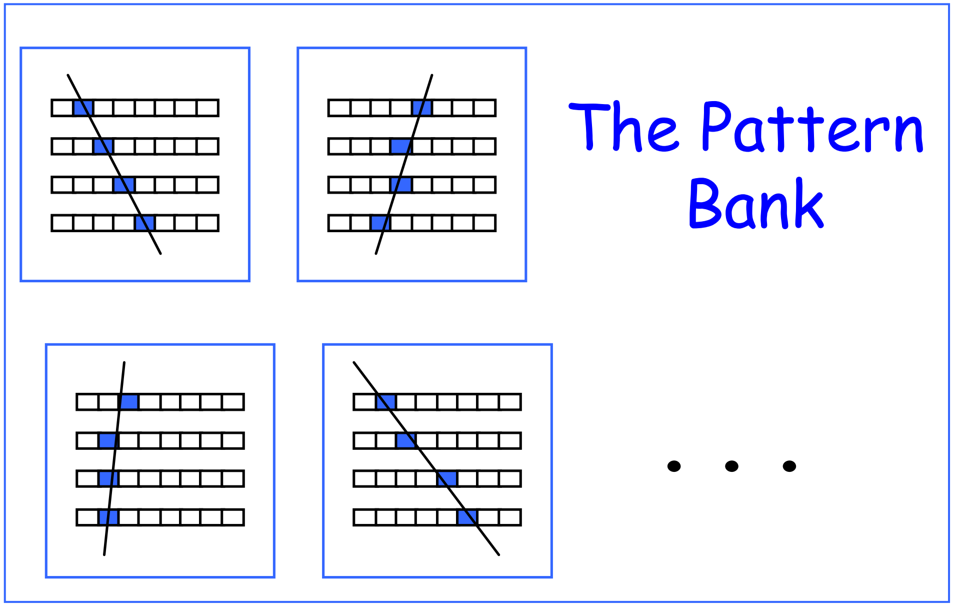


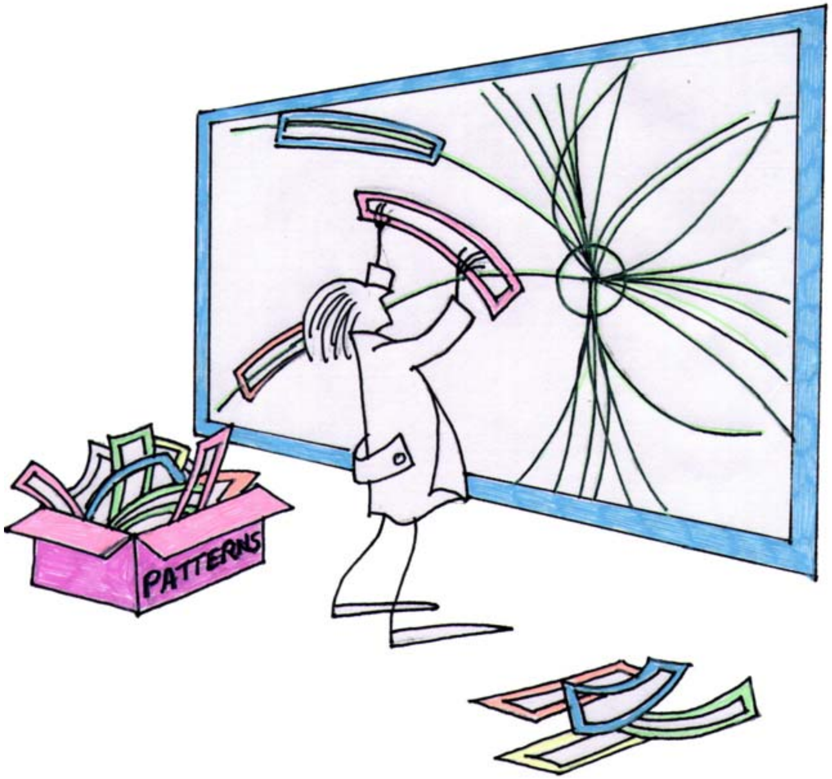
2. Then fit tracks inside roads.
   Thanks to 1st step it is much easier



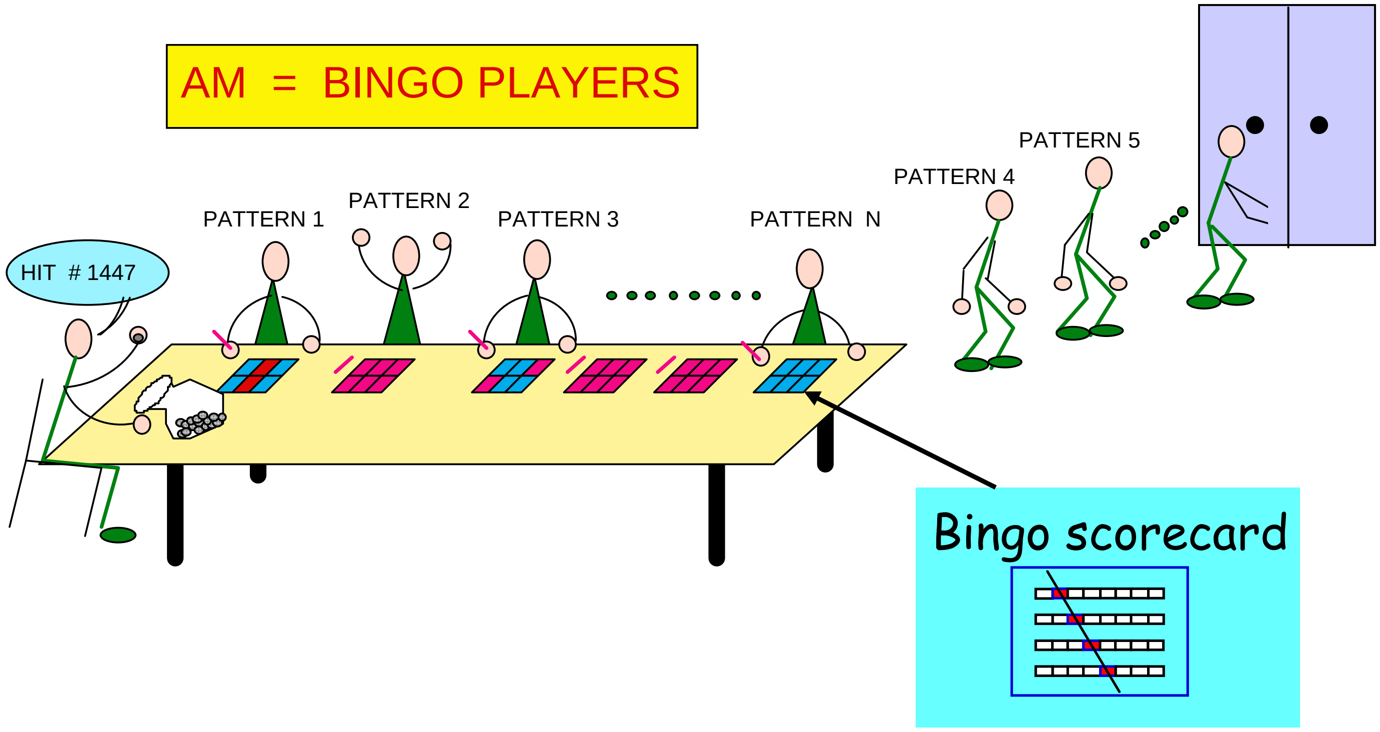
Pattern matching







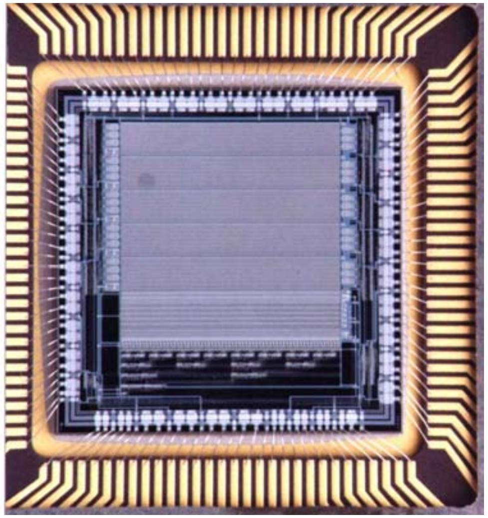
AM: Associative Memory



- **Dedicated device: maximum parallelism**
- **Each pattern with private comparator**
- **Track search during detector readout**

AM chip & system

SVT



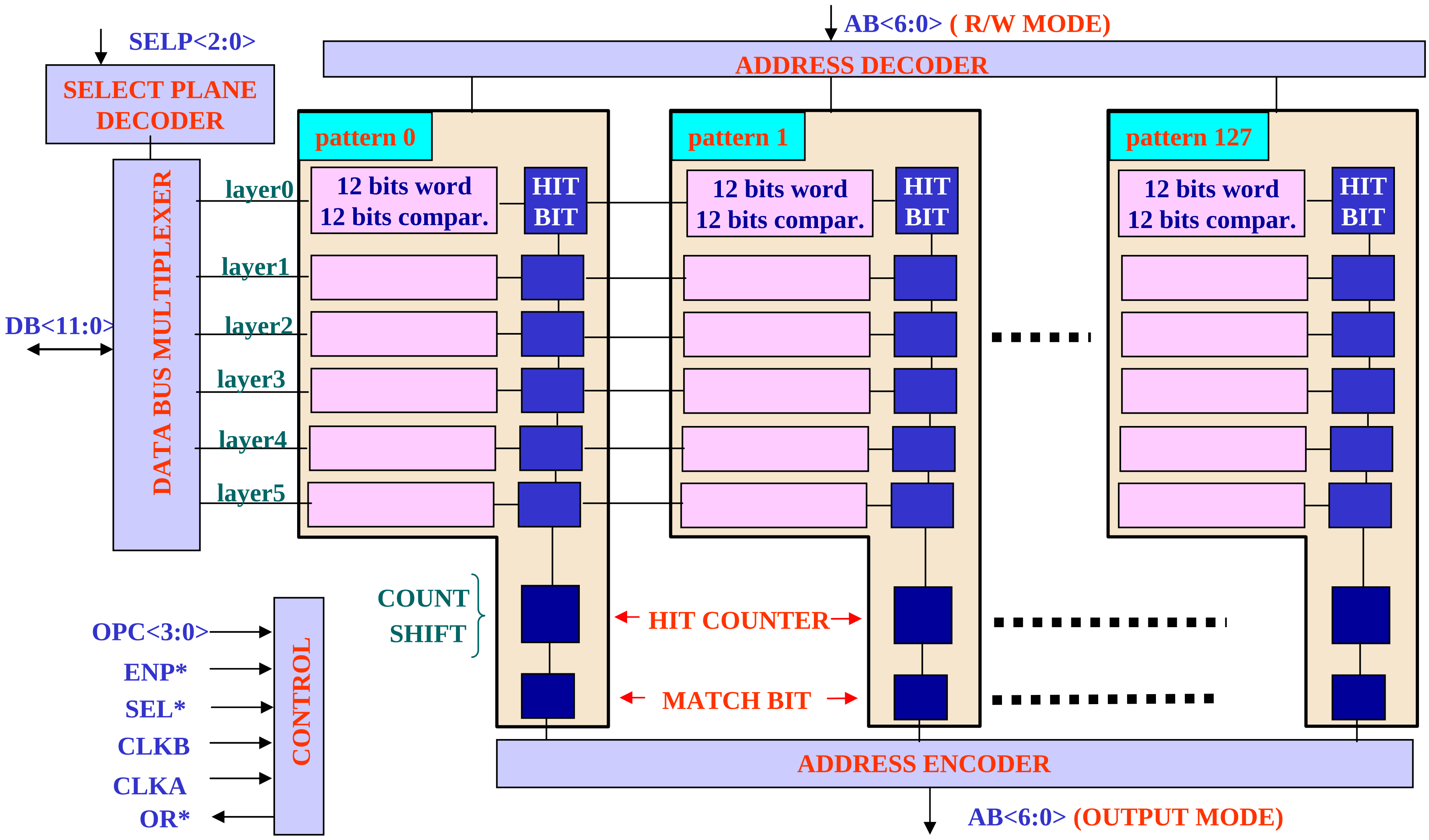
- **Undoable with standard electronics** (90's)

$\Rightarrow$ **Full custom VLSI chip -** 0.7μm (INFN-Pisa)

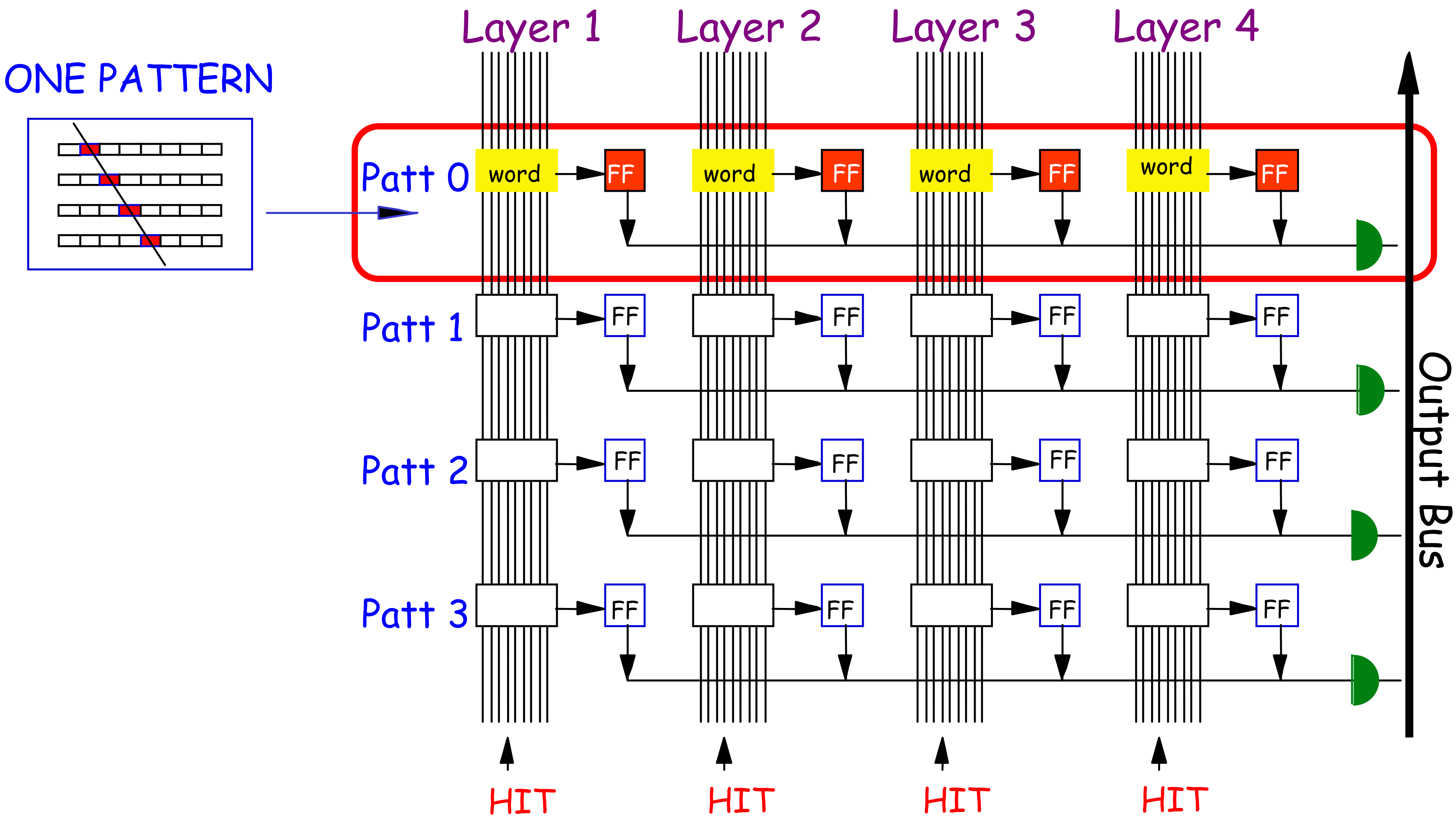
- **128 patterns, 6x12bit words each**
- **Working up to 40 MHz**

- **Limit to 2-D**
- **6 layers: 5 SVX + 1 COT**
- **~250 micron bins $\Rightarrow$ 32k roads / 30^0 φ sector**
- **>95% coverage for P_t > 2 GeV**

AM chip internal structure



AM chip working principle



Track Fitting

- Track confined to a road: fitting becomes easy

- Linear expansion in the hit positions x_i:
  - Chi2 = Sum_k ((c_{ik} x_i)^2)
  - $d = d_0 + a_i\, x_i$; $phi = phi_0 + b_i\, x_i$; Pt = ...

- Fit reduces to a few scalar products: fast evaluation
  - (DSP, FPGA …)

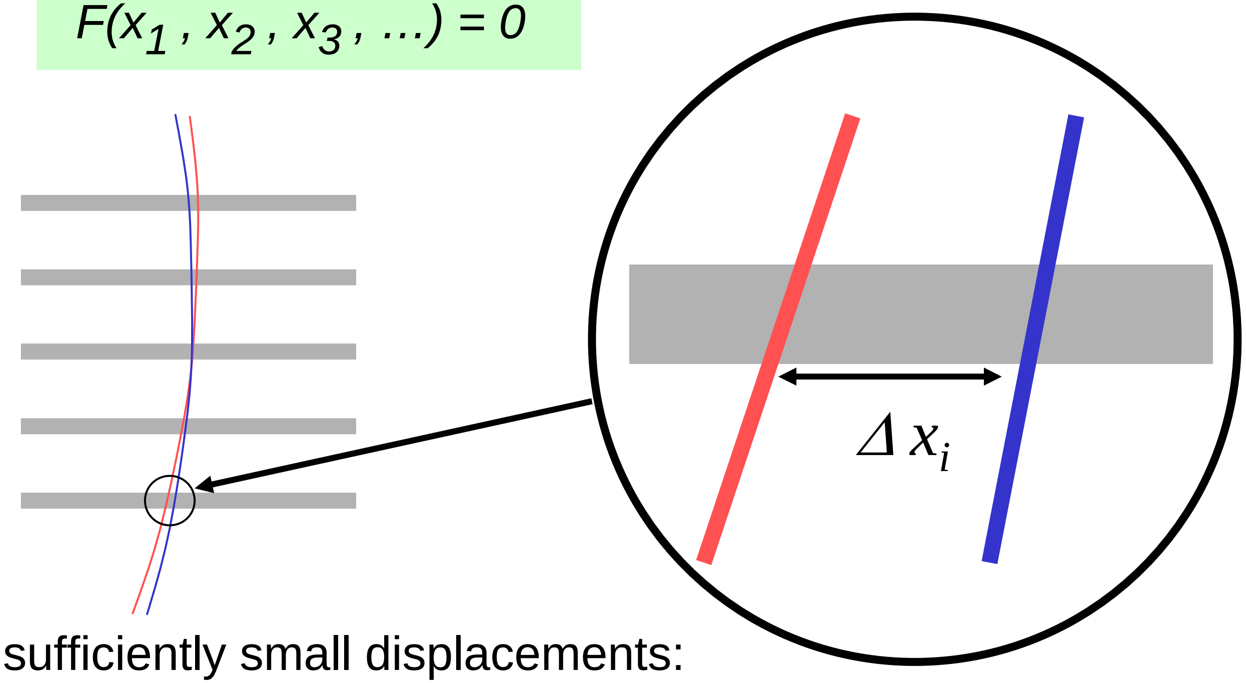
- Constants from detector geometry
  - Calculate in advance
  - Correction of mechanical alignments via linear algorithm
    - fast and stable
    - A tough problem made easy !

From non-linear to linear constraints

SVT

Non-linear geometrical constraint for a circle:

$$F(x_1, x_2, x_3, \ldots) = 0$$



But for sufficiently small displacements:

$$F(x_1, x_2, x_3, \ldots) \sim a_0 + a_1\Delta x_1 + a_2\Delta x_2 + a_3\Delta x_3 + \ldots = 0$$

with constant a_i (first order expansion of F)

Constraint surface

6 coordinates: x_1, x_2, x_3, x_4, x_5 (P_T), x_6 (ϕ)

3 parameters to fit: P_T , ϕ , d

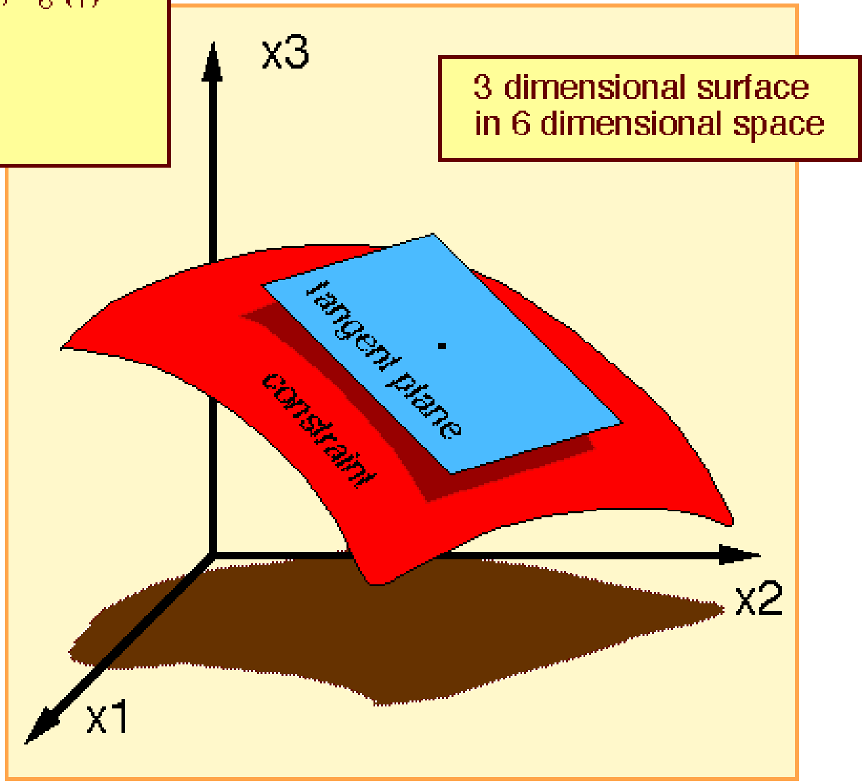
3 constraints

tangent plane:

$$\sum_{1}^{6} a_i x_i = b$$

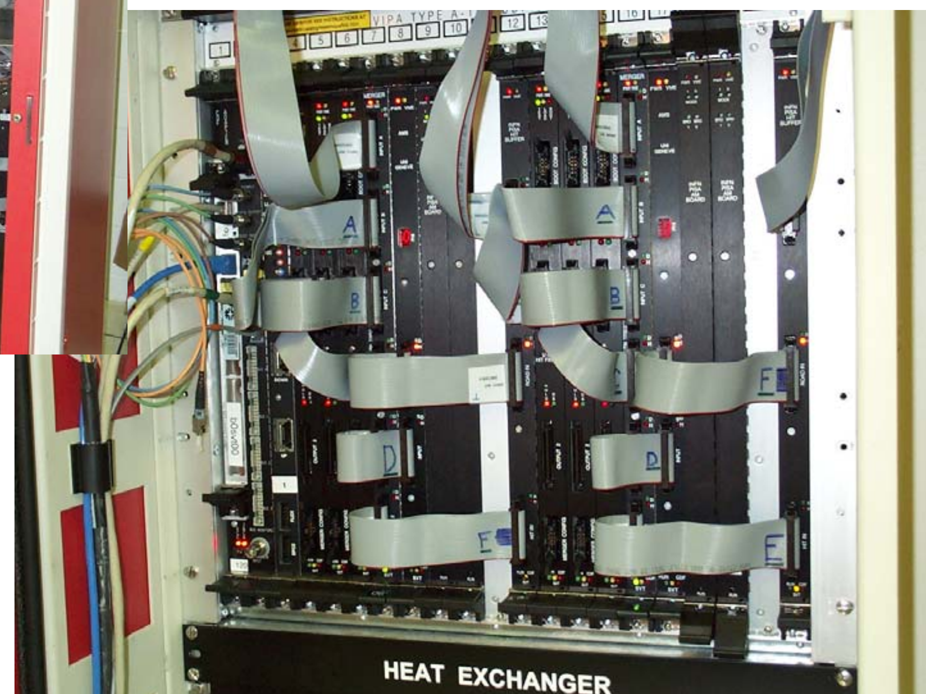
track parameters:

$$d \approx c_0 + \sum_{1}^{6} c_i x_i$$

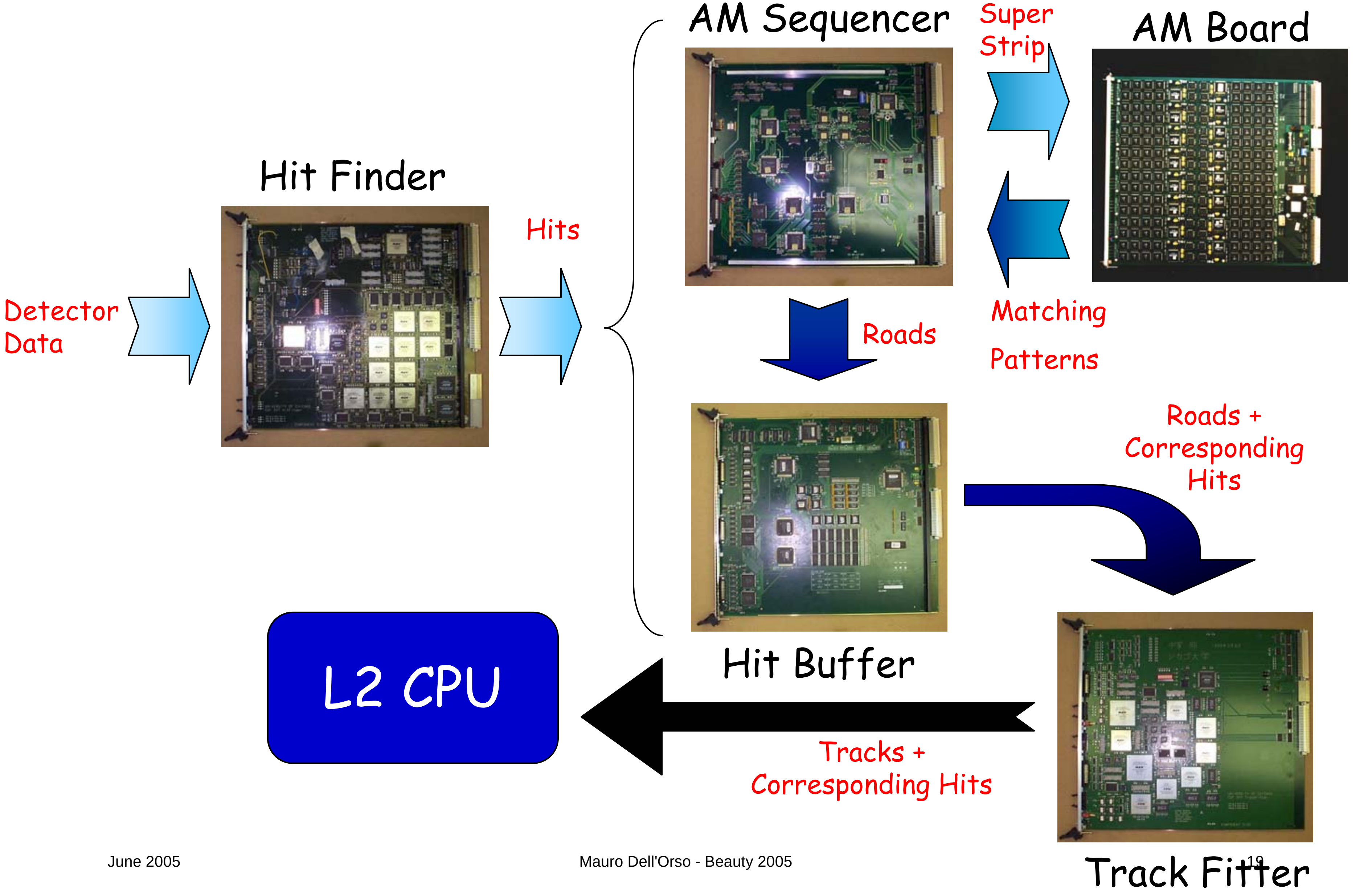


Linear approximation is so good that a single set of constants is sufficient for a whole detector wedge (30° in ϕ)

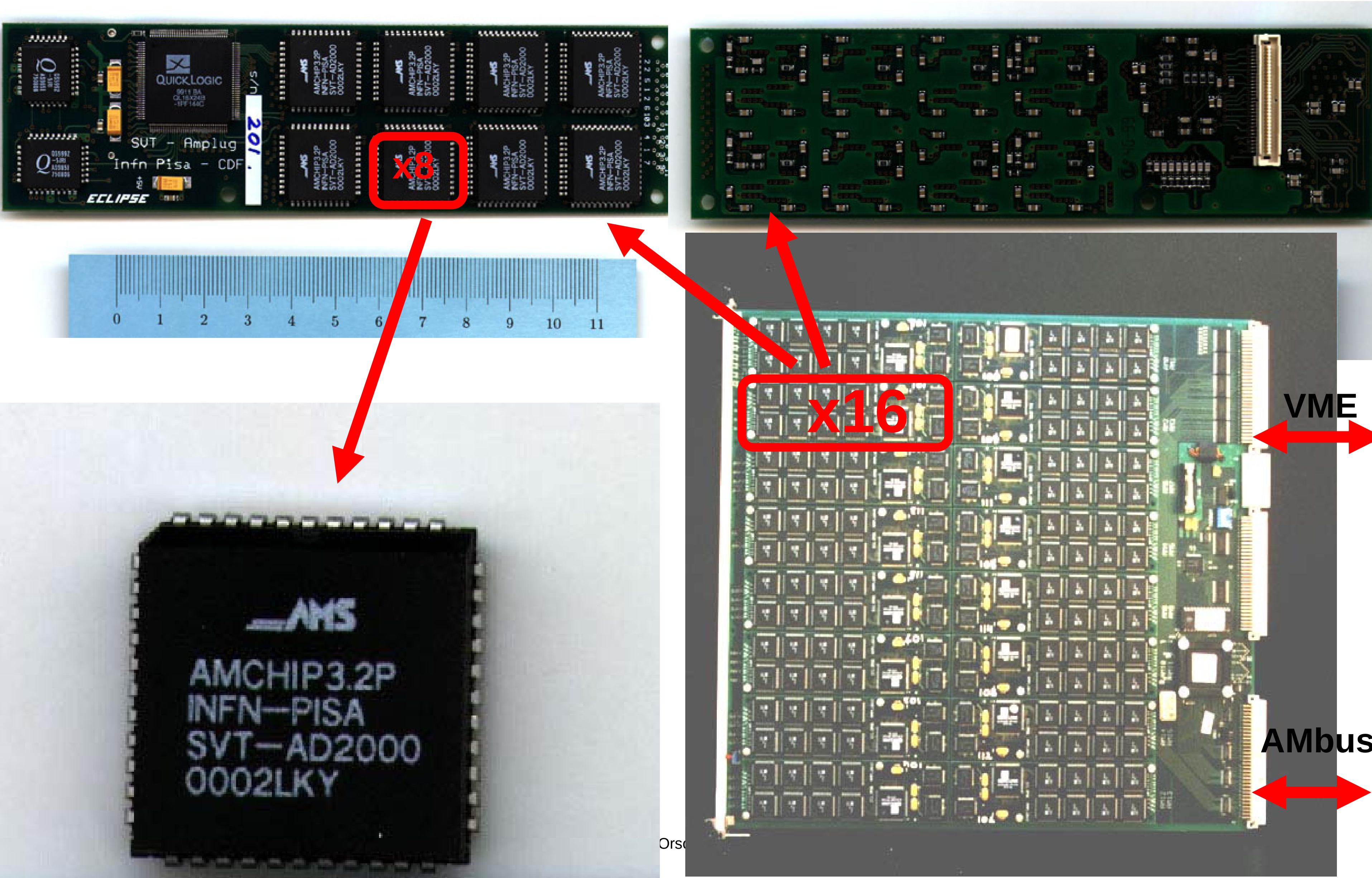
SVT crates in CDF counting room



The Device


AM Sequencer
Super Strip
AM Board
Hit Finder
Hits
Detector Data
Matching Patterns
Roads
Roads + Corresponding Hits
L2 CPU
Hit Buffer
Tracks + Corresponding Hits
Track Fitter

AM Board


QUICKLOGIC
SVT - Amplug
Infn Pisa - CDF
ECLIPSE
x8
0 1 2 3 4 5 6 7 8 9 10 11
x16
VME
AMbus
AMS
AMCHIP3.2P
INFN–PISA
SVT–AD2000
0002LKY

Hadronic B decays with SVT

SVT

Two paths

@ 3 x 10^{31} cm^{-2} s^{-1}

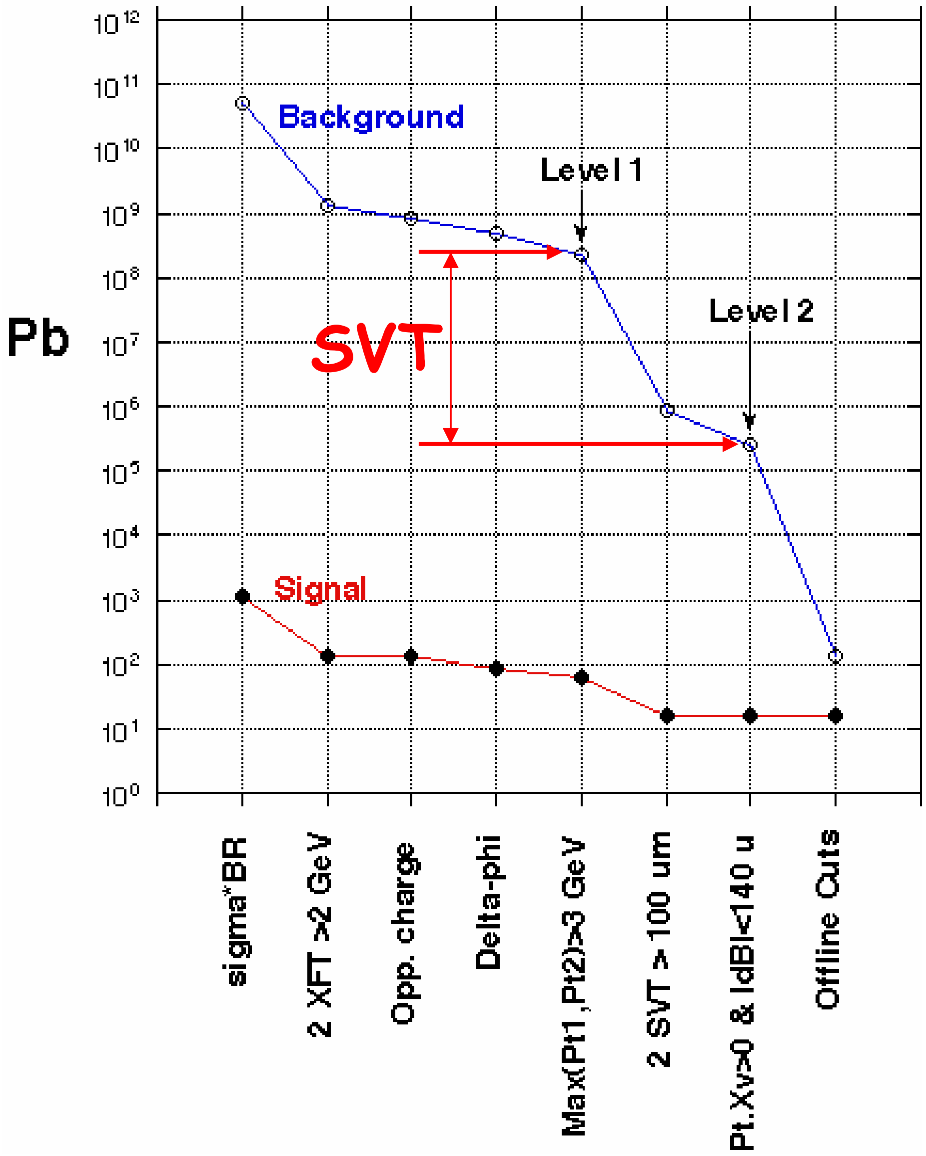
- **L1**:
  - Two XFT tracks
  - P_t > 2 GeV; $P_{t1} + P_{t2}$ > 5.5 GeV
  - $\Delta\phi$ < 135°
- **L2**:
  - d_0>100 μm for both tracks
  - Validation of L1 cuts with $\Delta\phi$>20°
  - Lxy > 200 μm
  - d_0(B)<140 μm

Two body decays

- **L1**:
  - Two XFT tracks
  - P_t > 2 GeV; $P_{t1} + P_{t2}$ > 5.5 GeV
  - $\Delta\phi$ < 135°
- **L2**:
  - d_0>120 μm for both tracks
  - Validation of L1 cuts with $\Delta\phi$>2°
  - Lxy > 200 μm
  - ~~d_0(B)<140 μm~~

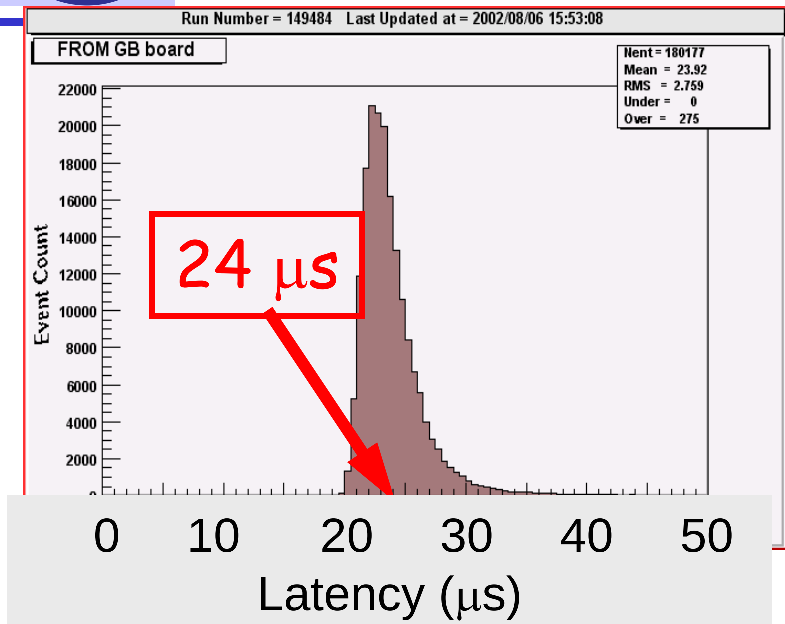
Many body decays

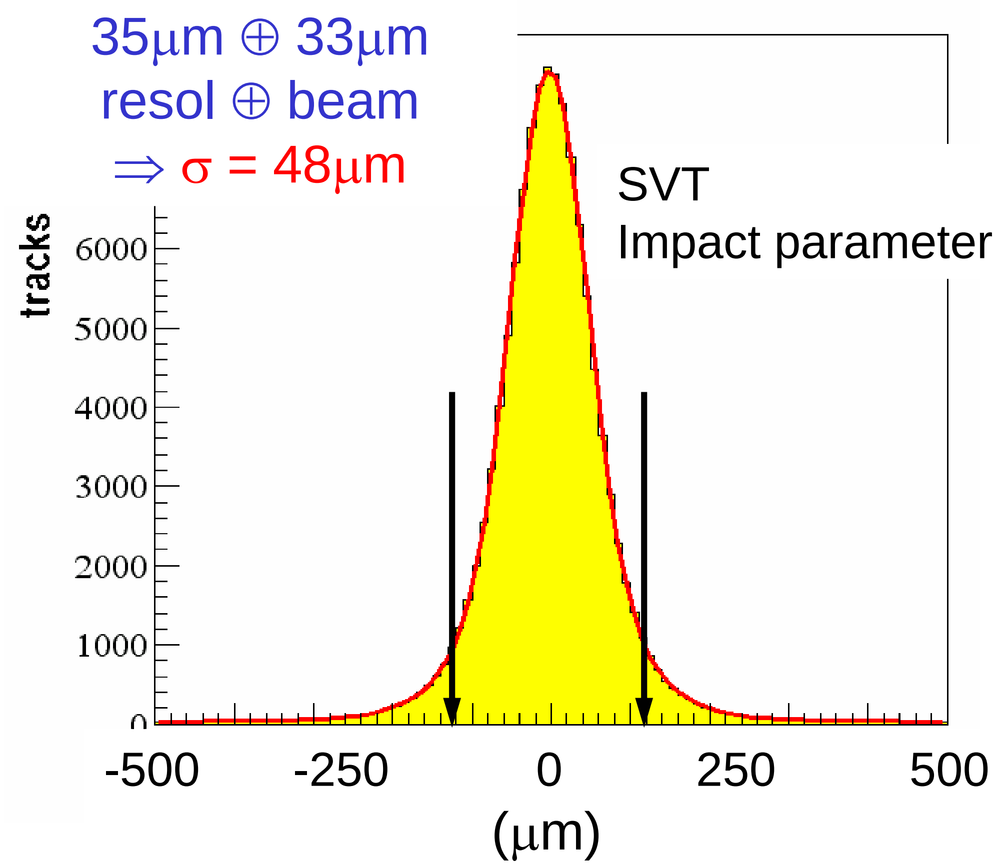
$B^0 \rightarrow$ had + had Trigger

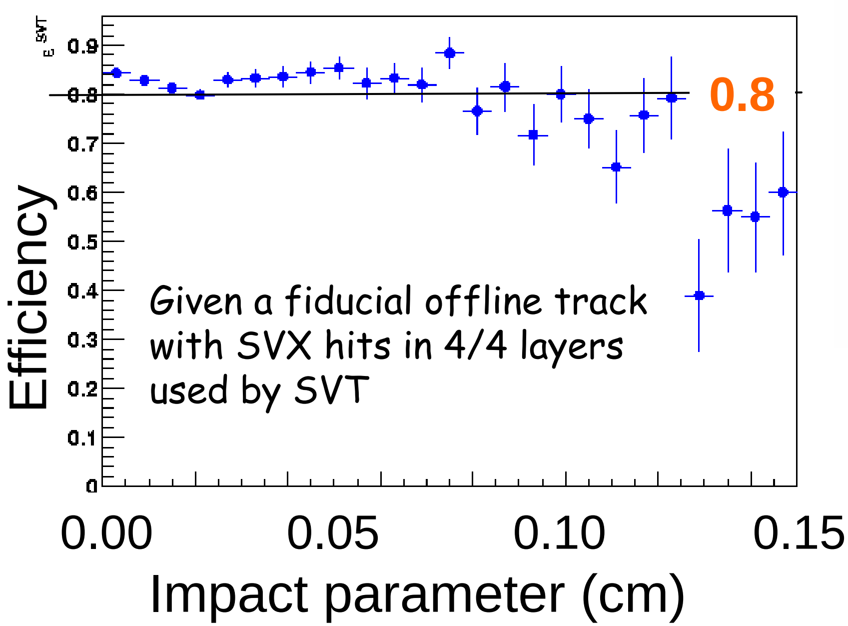


The SVT advantage:
3 orders of magnitude

Performance @ 5×10^{31}





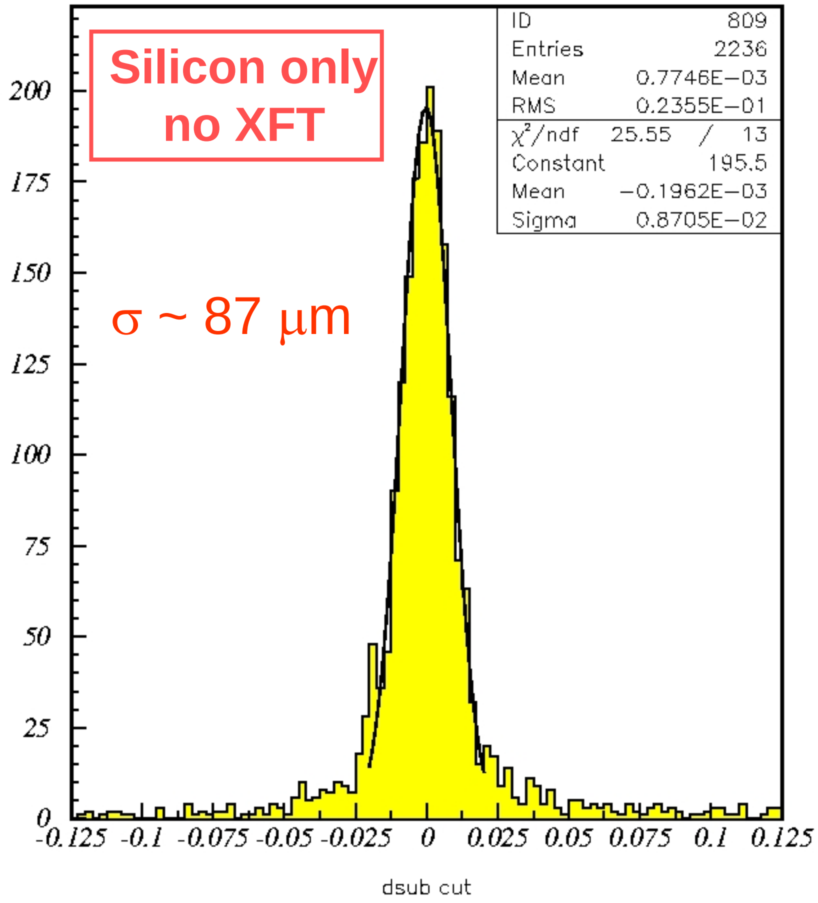


SVX only

SVT

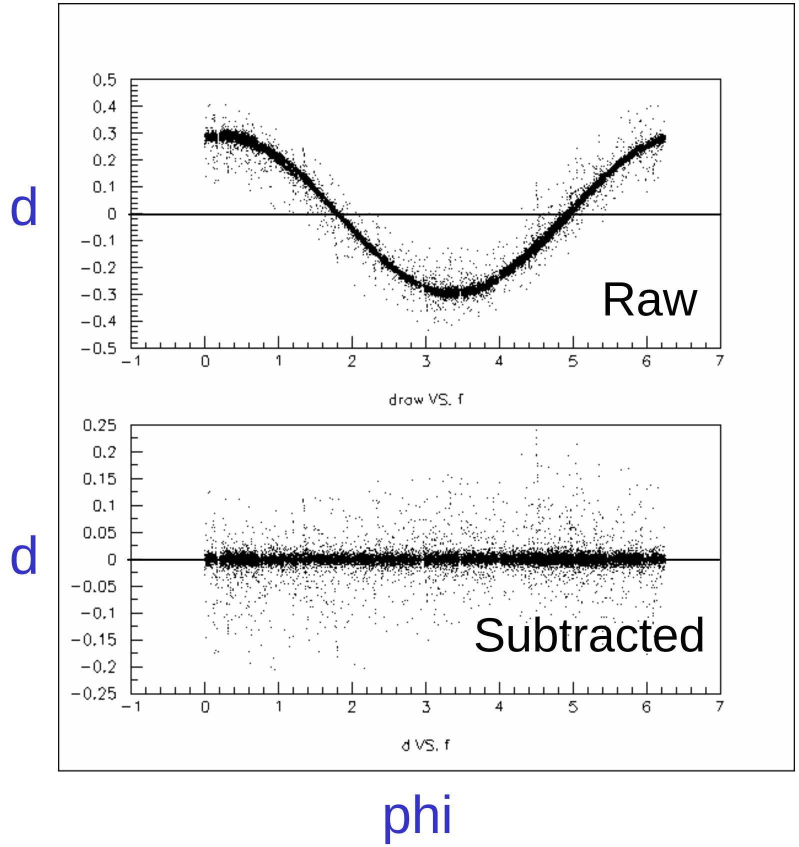
- Good tracks from just 4 closely spaced silicon layers
- I.p. as expected due to the lack of curvature information

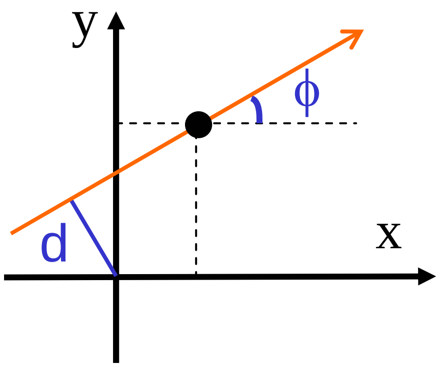
impact parameter distribution



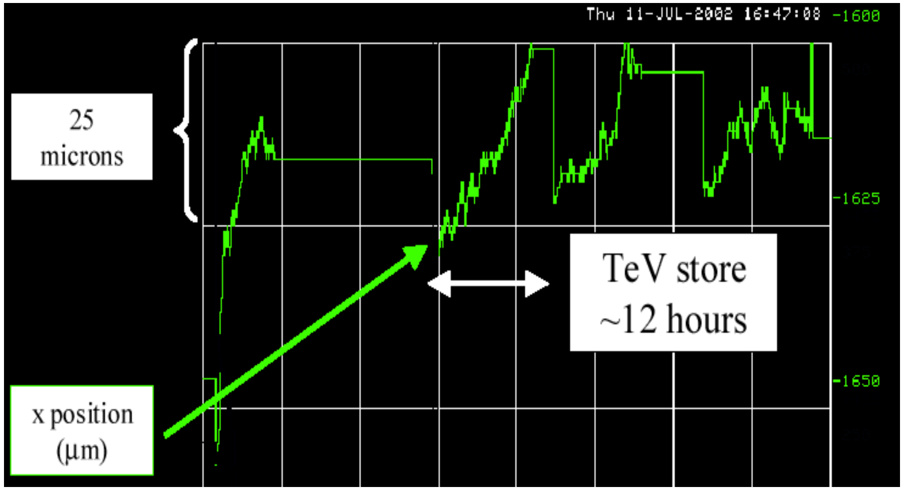
Online beamline fit & correction

SVT

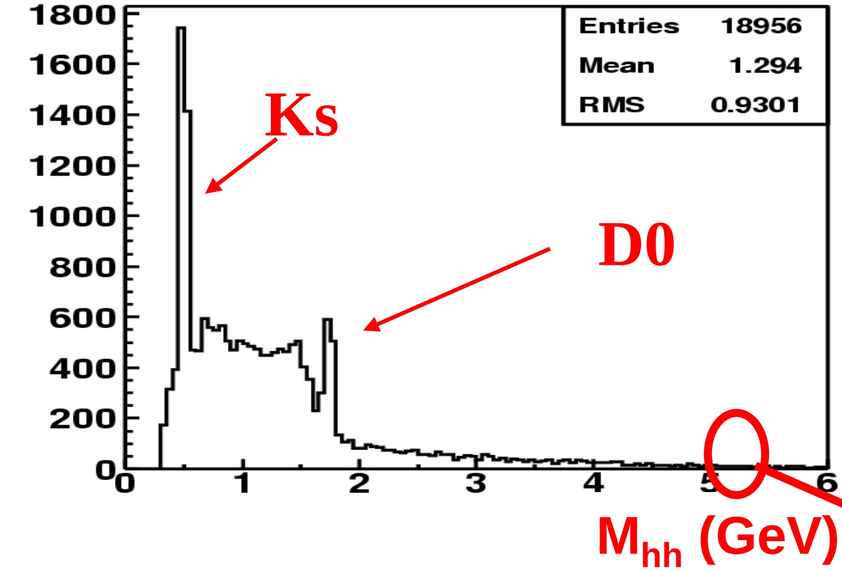


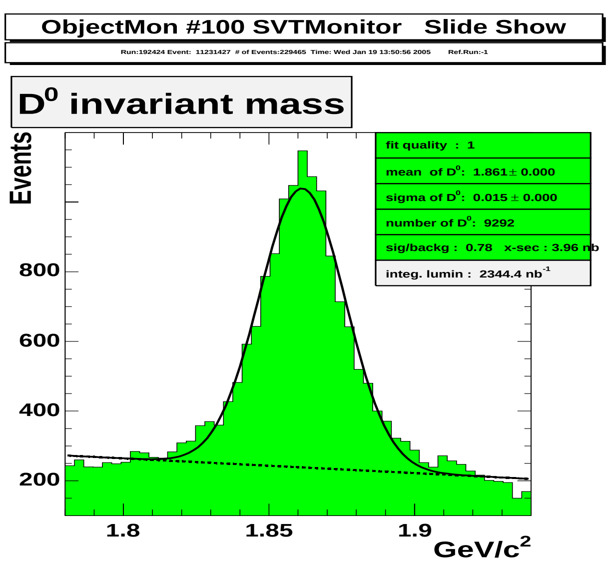


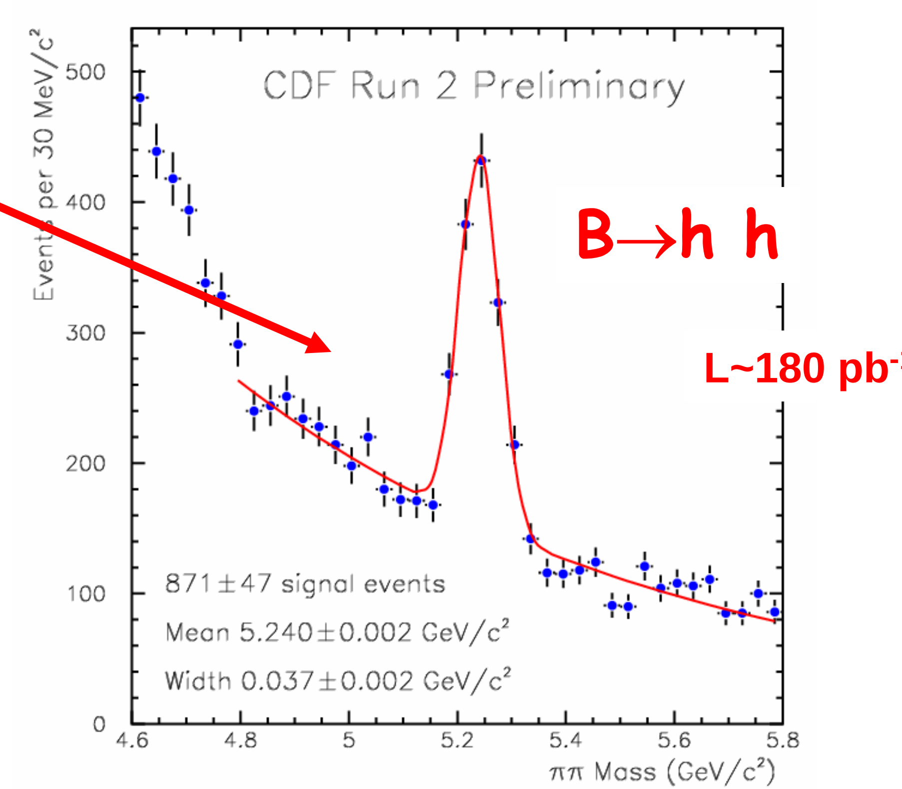
$$\langle d \rangle = Y_{beam} \cos\phi - X_{beam} \sin\phi$$



Hadron-hadron mass distribution

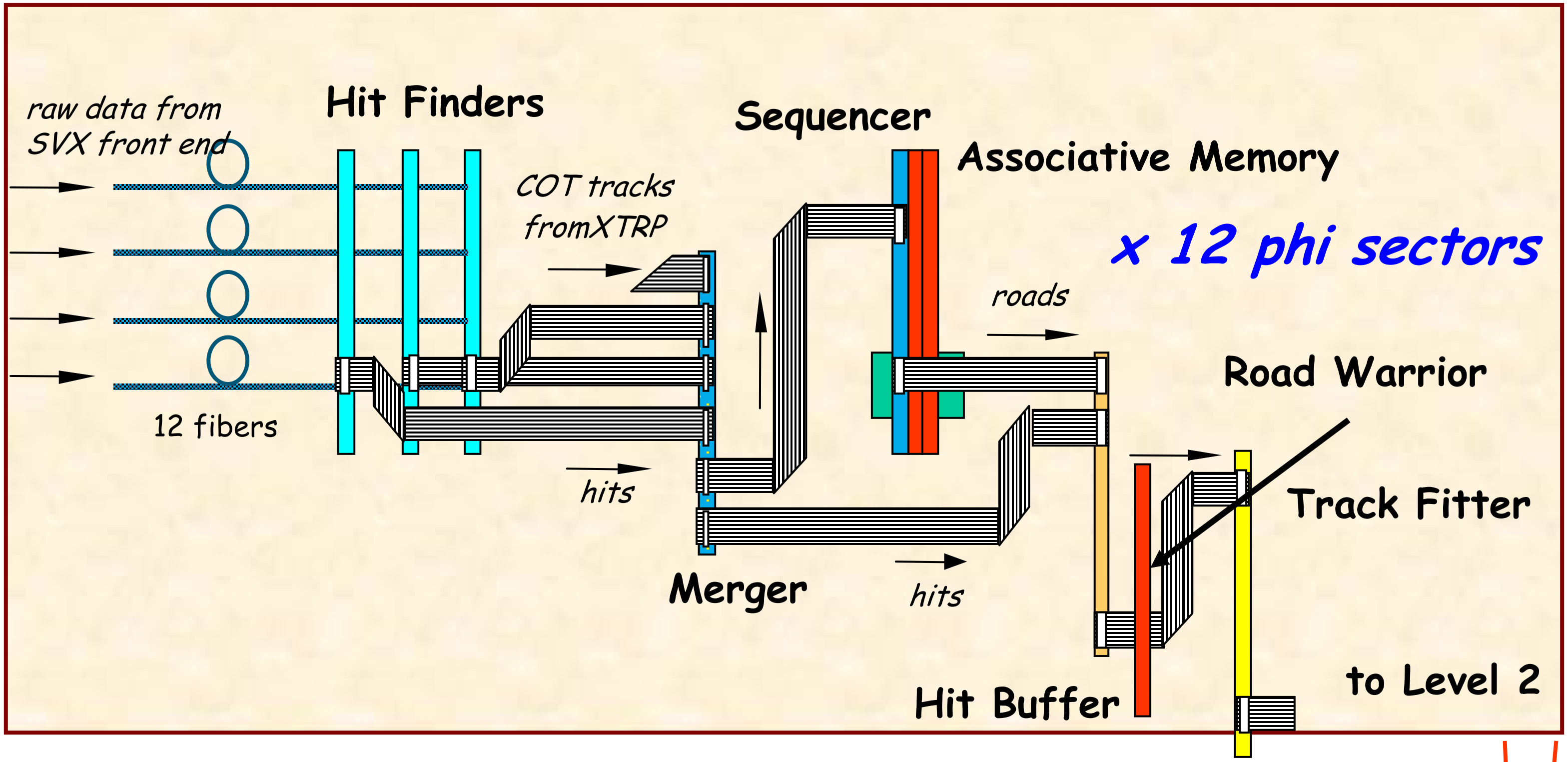






Upgrading SVT

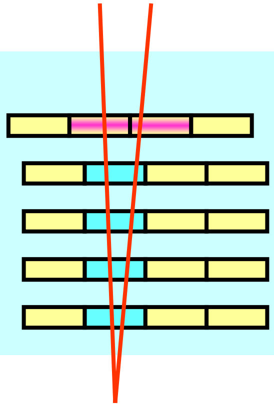
SVT



Reduce SVT processing time: c_1+c_2*N(Hit) $+c_3$*N(Comb.)

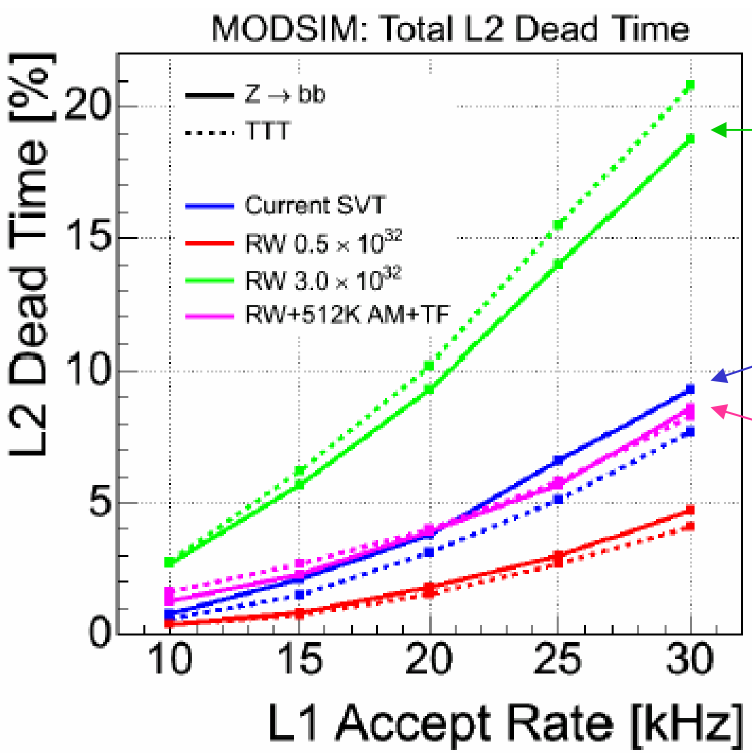
1. More patterns → thinner roads
2. Move Road Warrior before the HB
3. New TF++, HB++, AMS++, AM++ @ > 40MHz

RW:
Remove
ghosts



Dead Time vs. L1 Accept Rate

SVT



SVT @ 3 x 10^{32}

SVT @ 0.5 x 10^{32}

UPGRADE @ 3 x 10^{32}

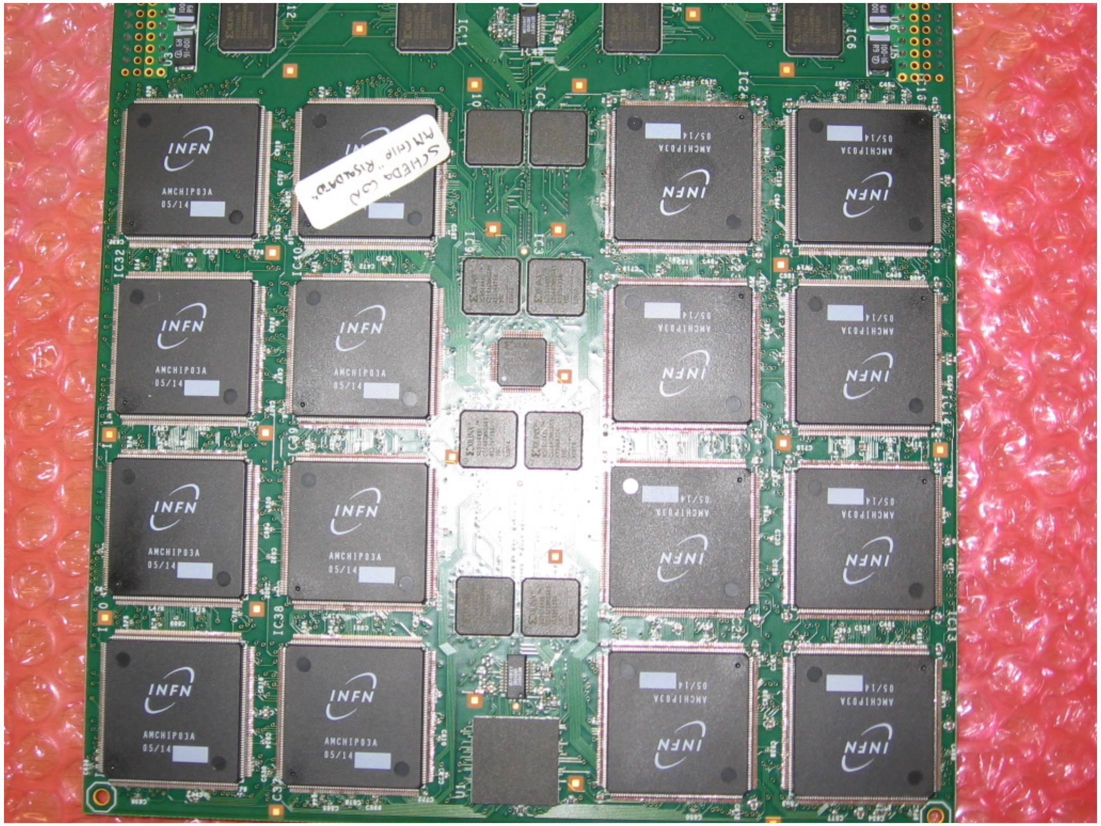
New AM chip

- Standard Cell UMC 0.18 μm
  10x10 mm die - 5000 patterns
  6 input hit buses
  tested up to 40 MHz, simulated up to 50 MHz

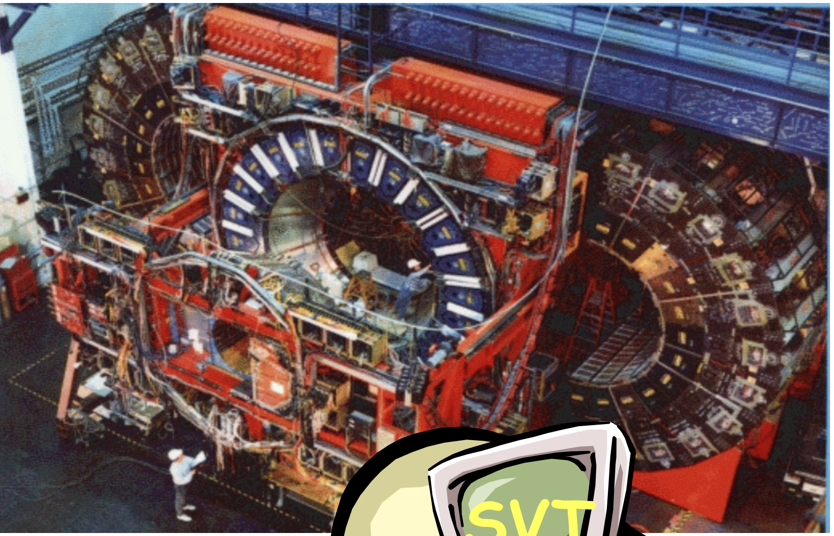
- 116 prototype chips on September 2004
  MPW run – low yield 37%

- 3000 production chips on April 2005
  good yield 70%
  private masks → better process parameter tuning for dense memory

LAMB++



What next ?



Next challenge is silicon tracking at both Level 1 & Level 2

Fast Track (FTK)

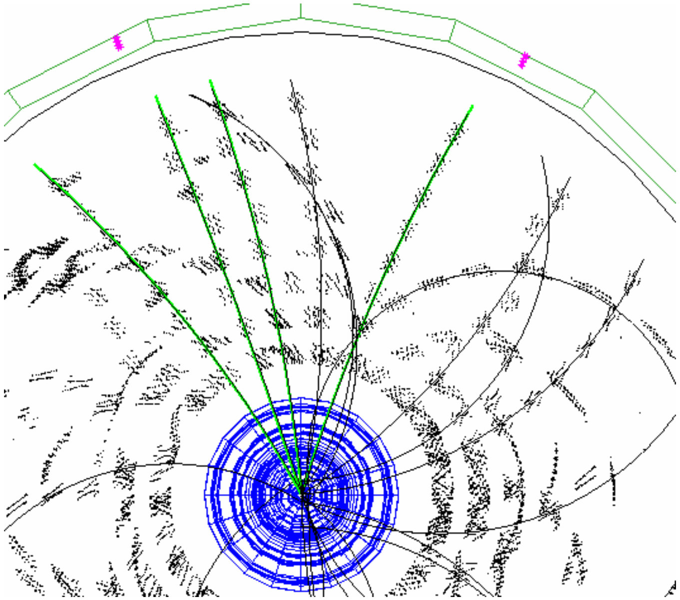
SUMMARY

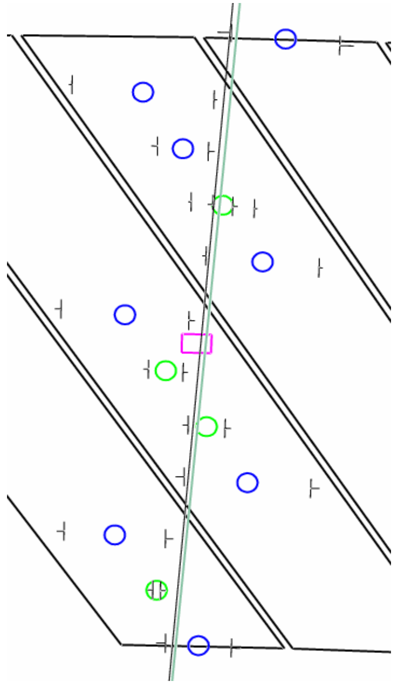
- The design and construction of SVT was a significant step forward in the technology of fast track finding
- We use a massively parallel/pipelined architecture combined with some innovative techniques such as the associative memory and linearized track fitting
- Performance of SVT is as expected
- CDF is triggering on impact parameter and collecting data leading to significant physics results
- B-physics, and not only, at hadron colliders substantially benefits of on-line tracking with off-line quality

BACKUP SLIDES

Level 1 drift chamber trigger (XFT)

SVT





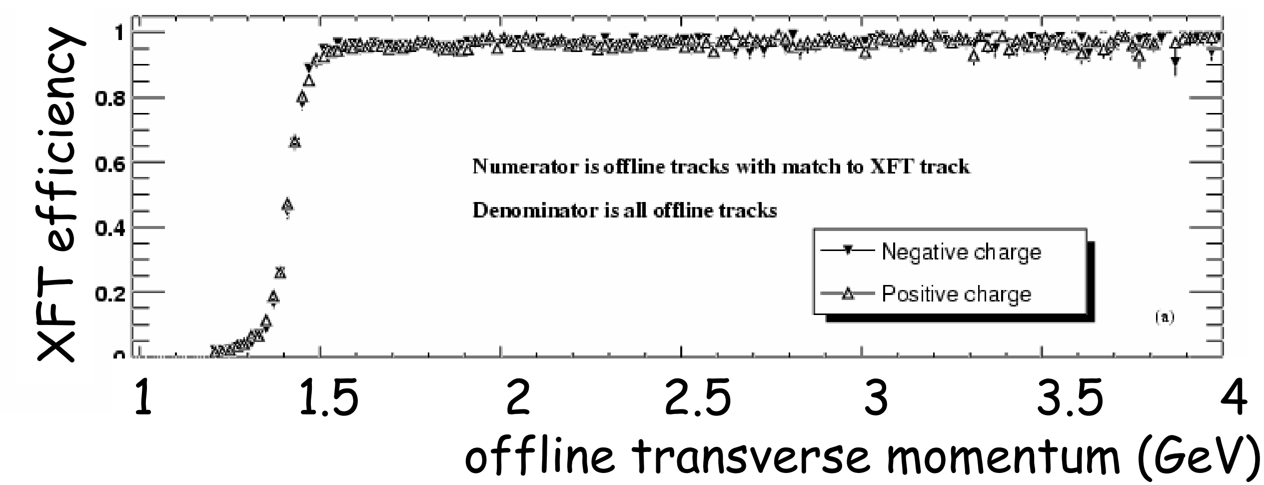
Finds p_T>1.5 GeV tracks in 1.9 μs

For every bunch crossing (132 ns)!

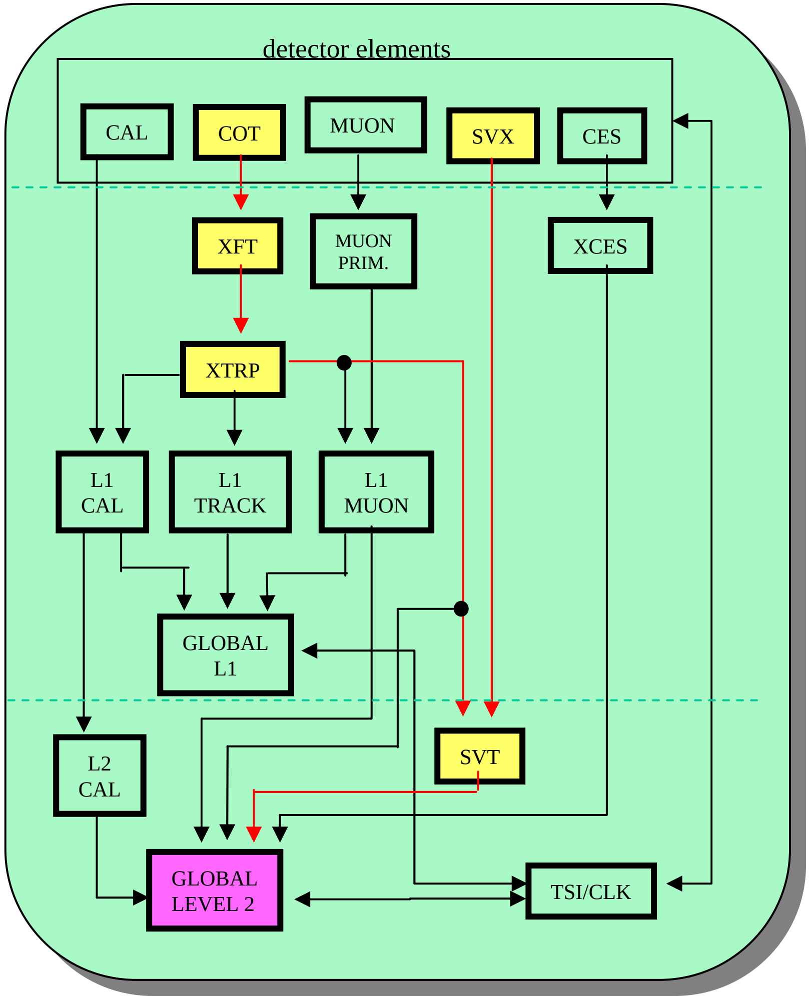
$\sigma(1/p_T)$ = 1.7%/GeV

$\sigma(\phi_0)$ = 5 mrad

96% efficiency



CDF Run II trigger architecture



- Tracking system
  - central outer tracking (COT)
  - silicon tracking (SVX II & ISL)
- three-level trigger
  - L1: 5.5 μs pipeline
    - XFT: L1 2D COT track
  - L2: ~20 μs processing time
    - two stages of 10 μs
- SVT at stage 1 of L2
  - SVX II readout
  - hit cluster finding
  - pattern recognition
  - track fitting

2005 Trigger Performance & Limitations

SVT

Level	Input rate	Output rate	Potential limitations Current limitation	Future upgrades	2006 Output rate
1	~1MHz	25kHz (spec 45kHz)	•Silicon readout •SVT processing time •L2 processing time	•XFT upgrade •SVT upgrade •L2 Pulsar DONE	25kHz (higher at low lum)
2	25kHz	400Hz (spec 300Hz)	•Readout (non Si) •Event builder •L3 processing	•TDC modification •Event builder •Faster L3 nodes	1kHz
3	380Hz	85Hz (spec 75Hz)	•CSL/data logging	•Parallel logger 45 MB/s •CSL upgrade >60MB/s	100Hz

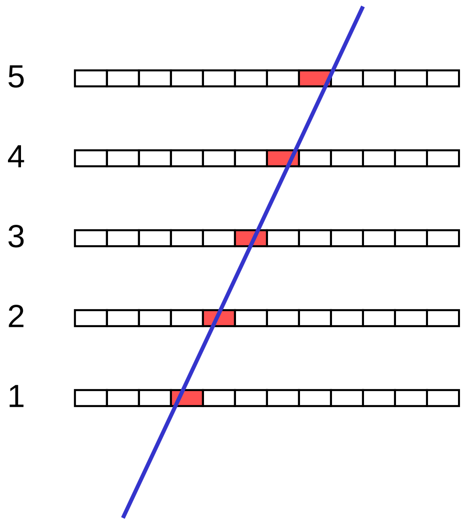
Rates are "peak rates that we can achieve with good livetime."

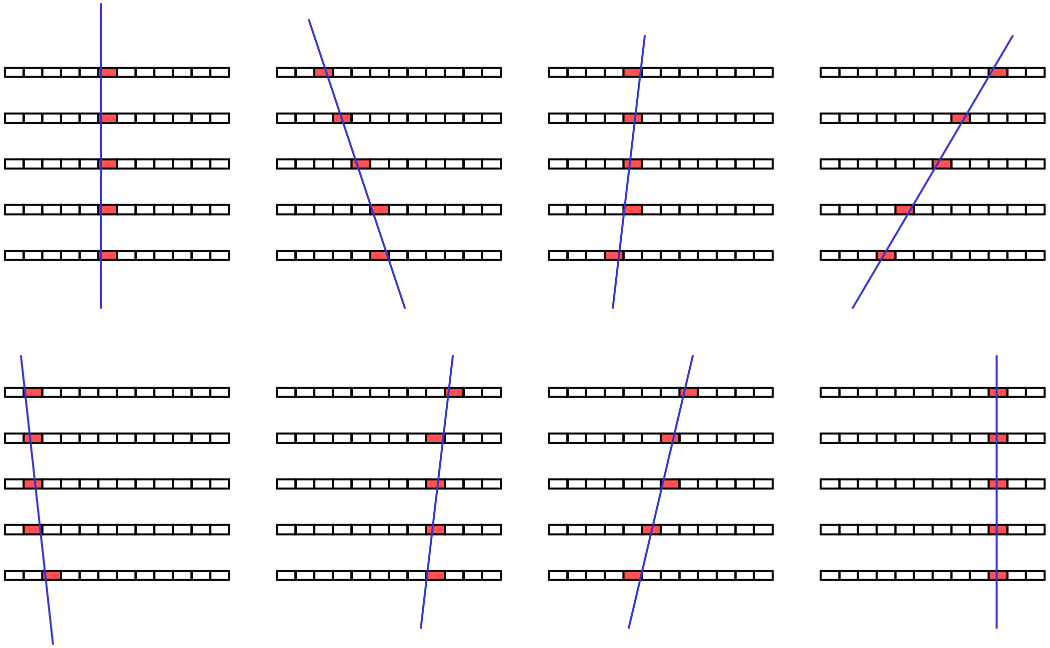
Building the "Pattern Bank"

SVT

Instead of looking for hit combinations such that *f(x1,x2,x3,…) = 0*

1. Build a database with all patterns corresponding to "good" tracks
2. Compare hits in each event with all patterns to find track candidates





In this example:
Straight lines, 5 layers, 12 bins/layer

⇒ Total number of patterns ~ $(12)^2*(5-1) = 576$

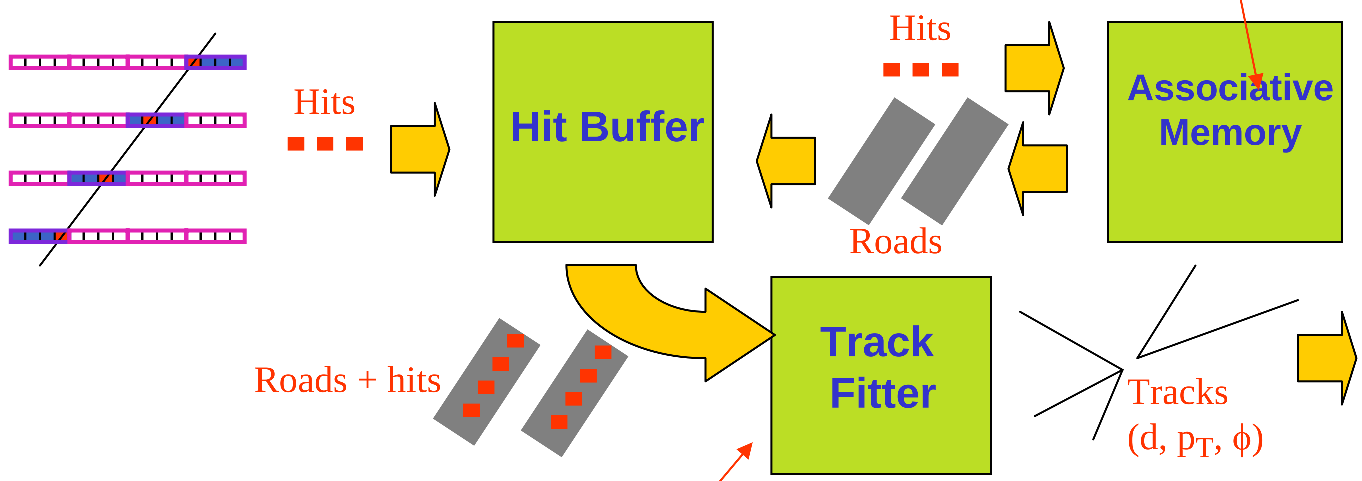
SVT basic architecture

- Pattern recognition and track fitting done separately and pipelined

Pattern recognition with Associative Memory (AM)

highly parallel algorithm

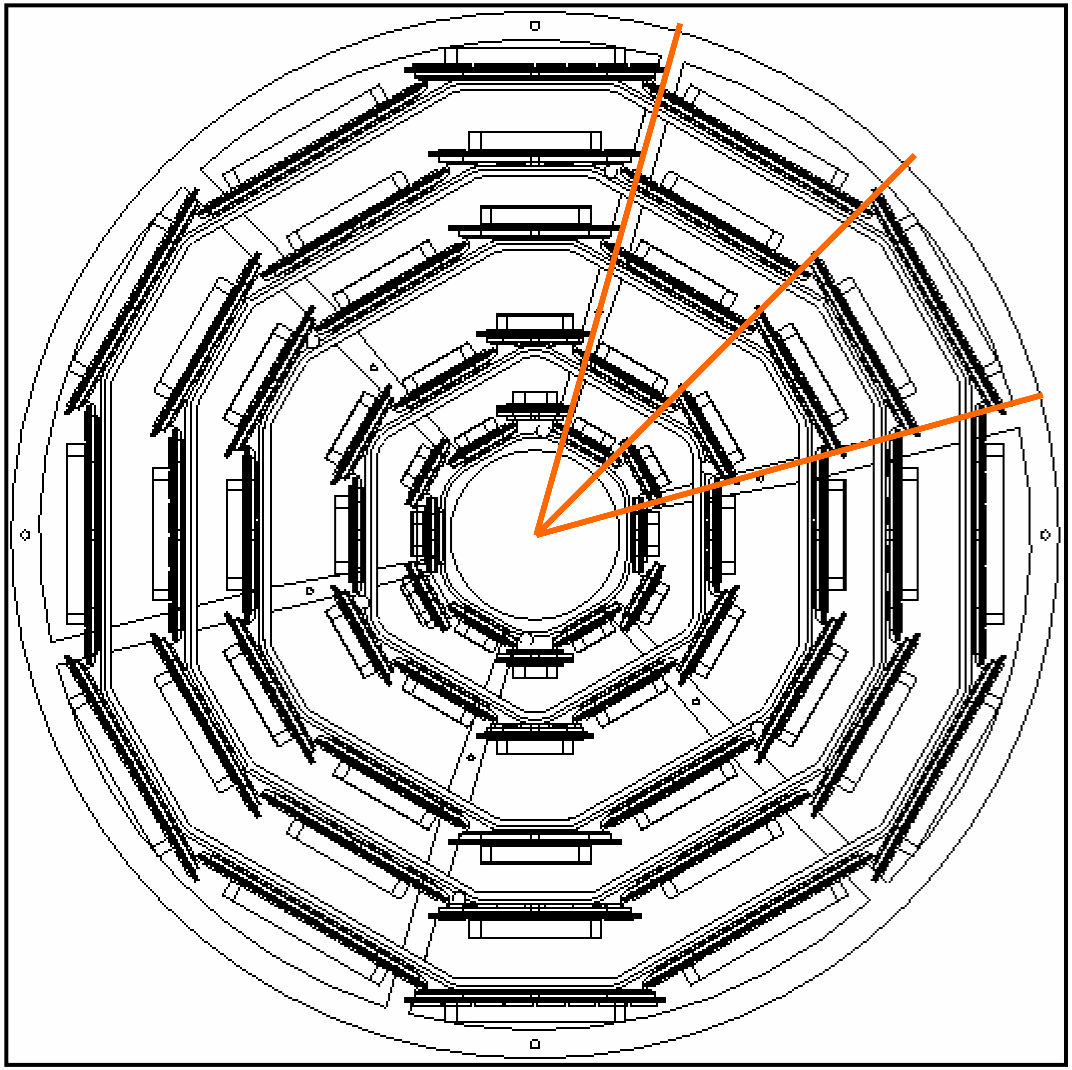
using coarser resolution to reduce memory size



Fast track fitting with linear approximation

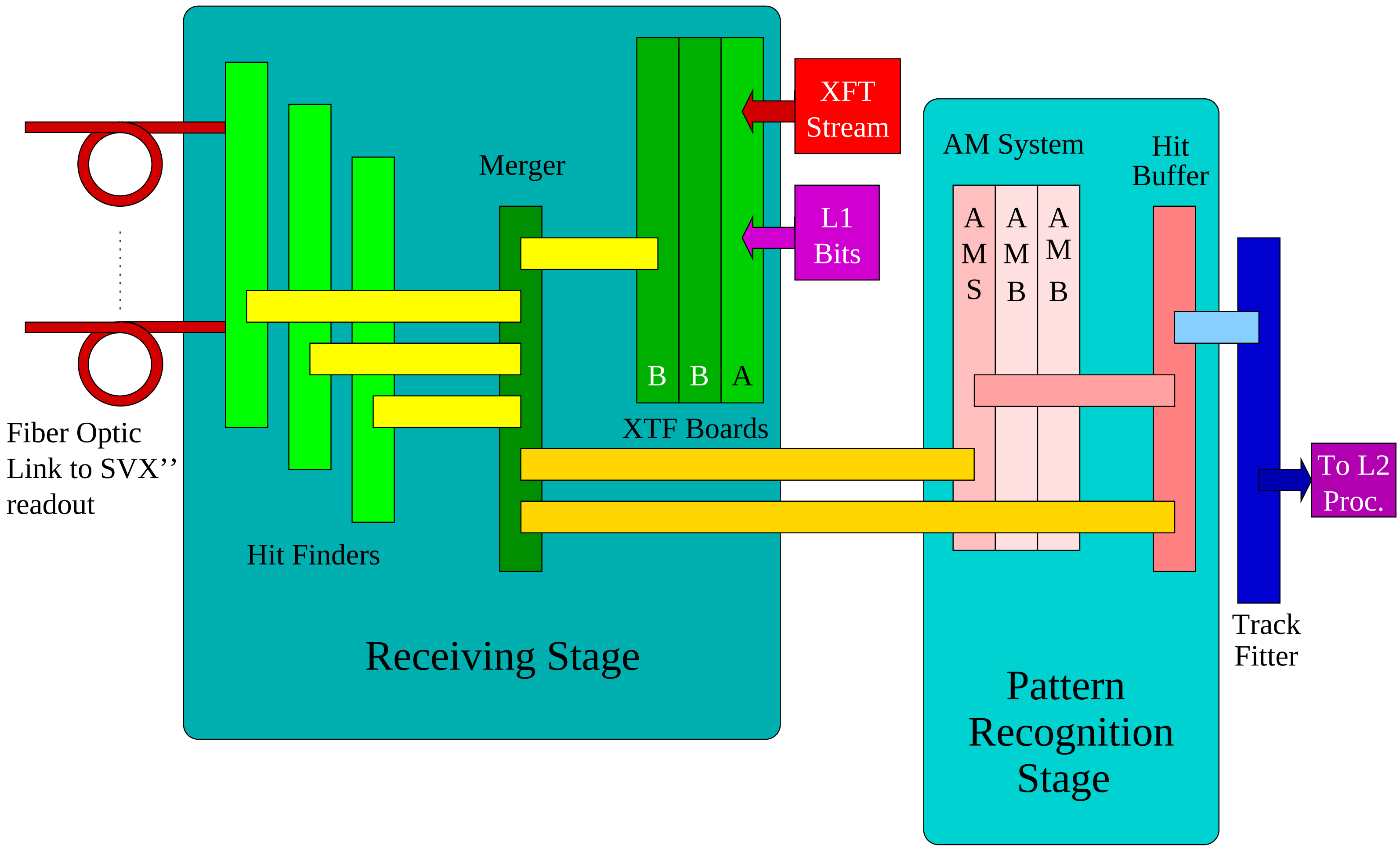
using full resolution of the silicon vertex detector

SVT Wedges



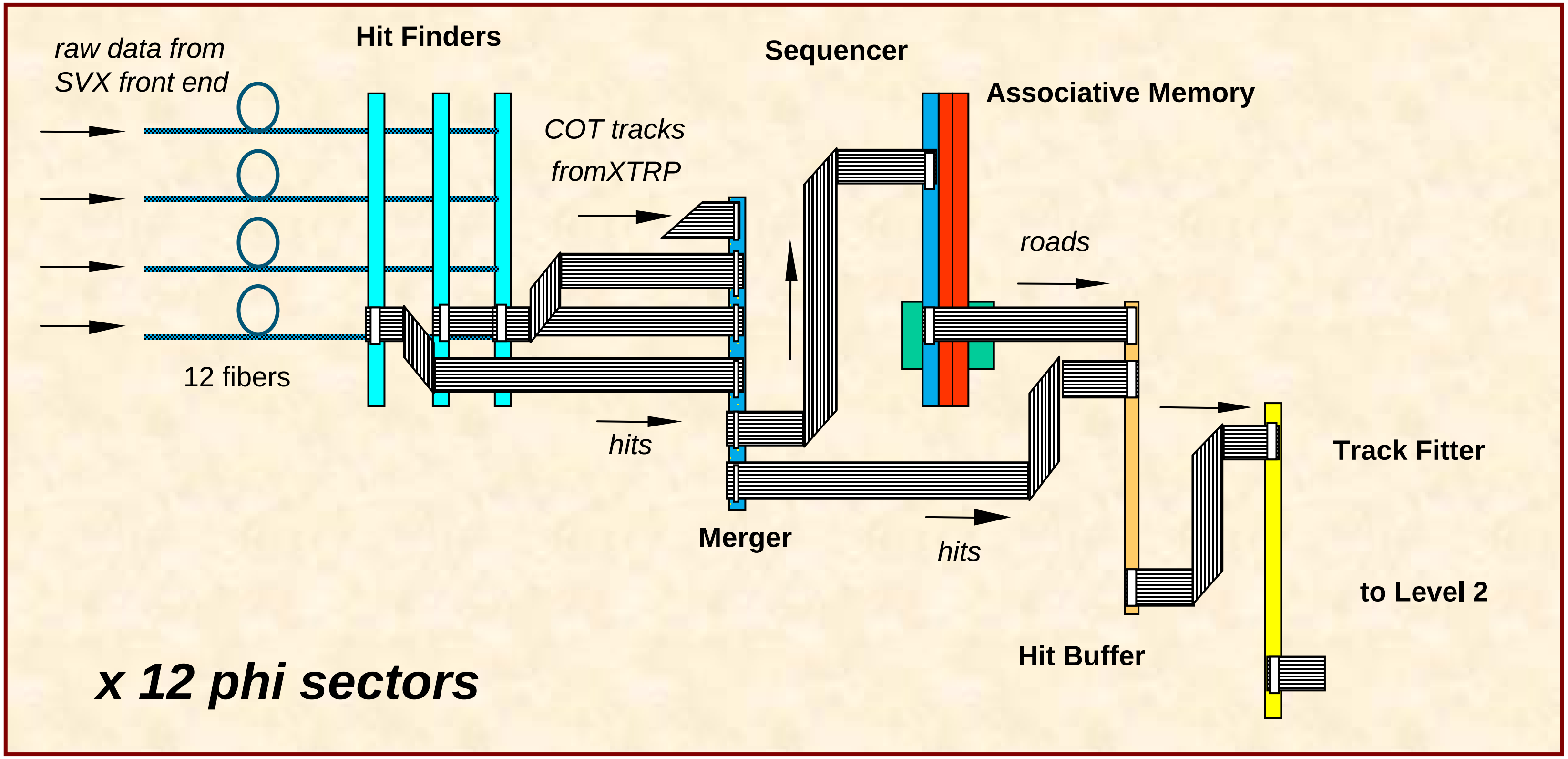
An SVT Slice

SVT



SVT system architecture

SVT



SVT: board count

• Hit Finders	42
• Mergers	16
• Sequencers	12
• AMboards	24
• Hit Buffers	12
• Track Fitters	12
• Spy Controls	8
• XTFA	1
• XTFB	2
• XTFC	6
• Ghostbuster	1
TOTAL	**136**

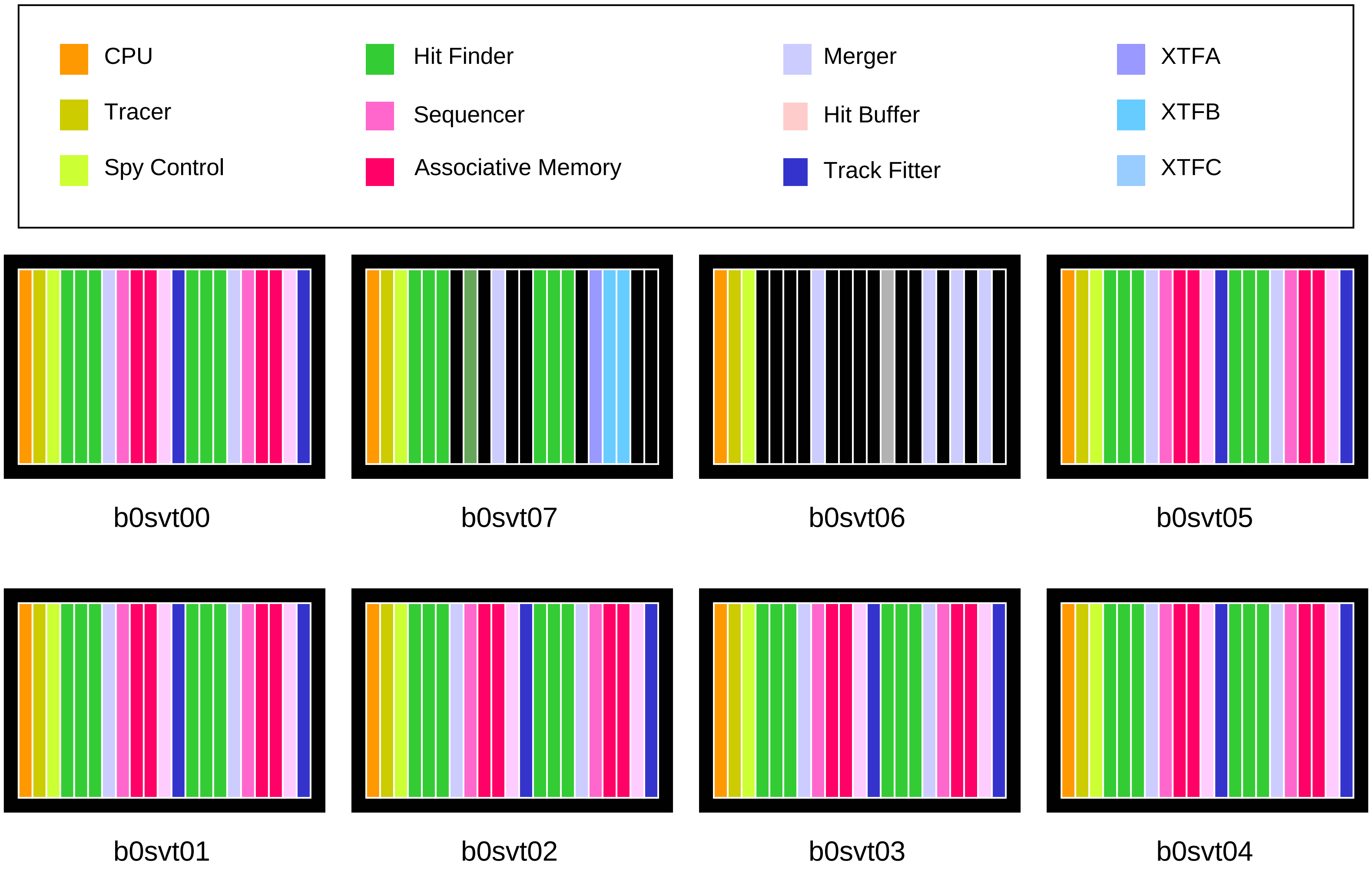
+ spares

■ INFN

■ INFN & Geneva

■ University of Chicago

SVT: board and crate layout



SVT data volume requires parallelism

2 meters

Reduces gigabytes/second to megabytes/second

Peak (avg): 20 (0.5) GB/s ⟶ 100 (1.5) MB/s

Expectations for runII

Rates within bandwidth @ 0.7×10^{32}

- **Level 1: 20 kHz (bw 50 kHz)**
- **Level 2: 39 Hz (bw 300 Hz)**
- **Level 3: negligible**

Expected yields in run II (2 fb^{-1})

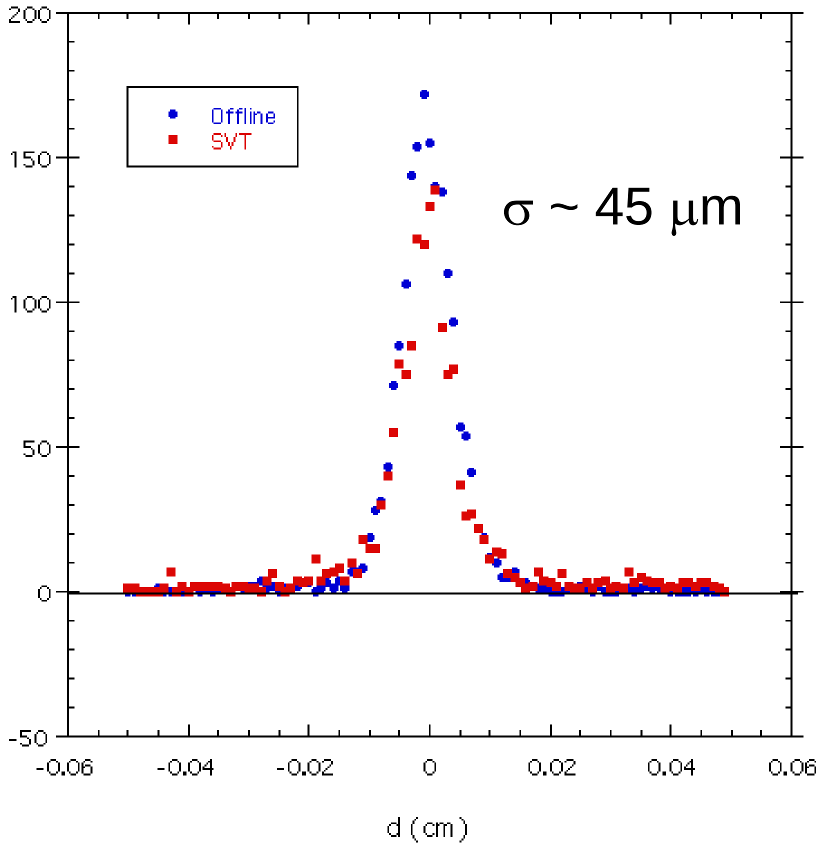
Mode	Events
$B_d \to \pi^+\pi^-$	15,200
$B_s \to D_s\, \pi$	10,600
$B_s \to D_s\, \pi\pi\pi$	12,800
$B_s \to D^*_s\, \pi$	9,400
$D^*\, \pi$	300,000
$Z \to$ b-bbar	32,000

angle γ at few degrees level

5σ sensitivity up to $x_s \sim 40$

N.B. : yields without SVT $\Rightarrow$ O(1) event !

Promise is promise

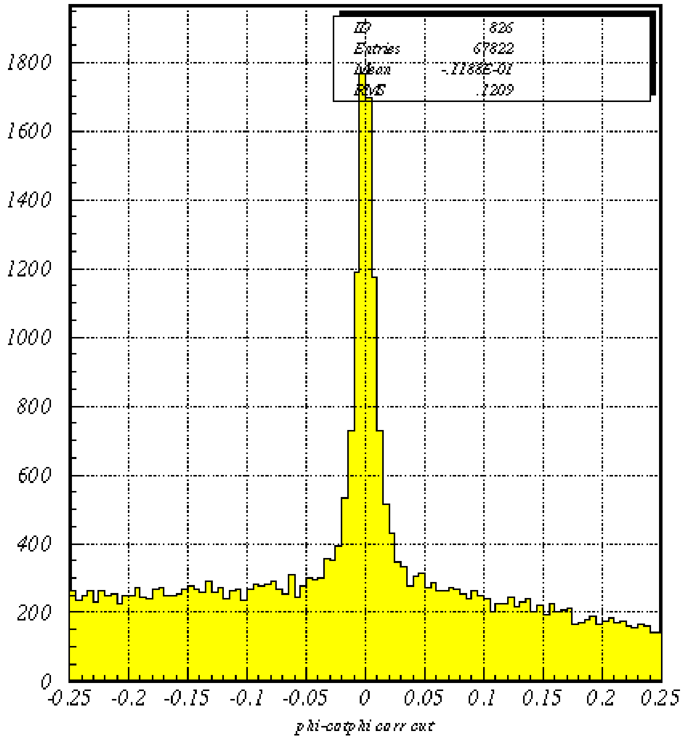


What we promised…. From SVT TDR ('96) using offline silicon hits and offline CTC tracks

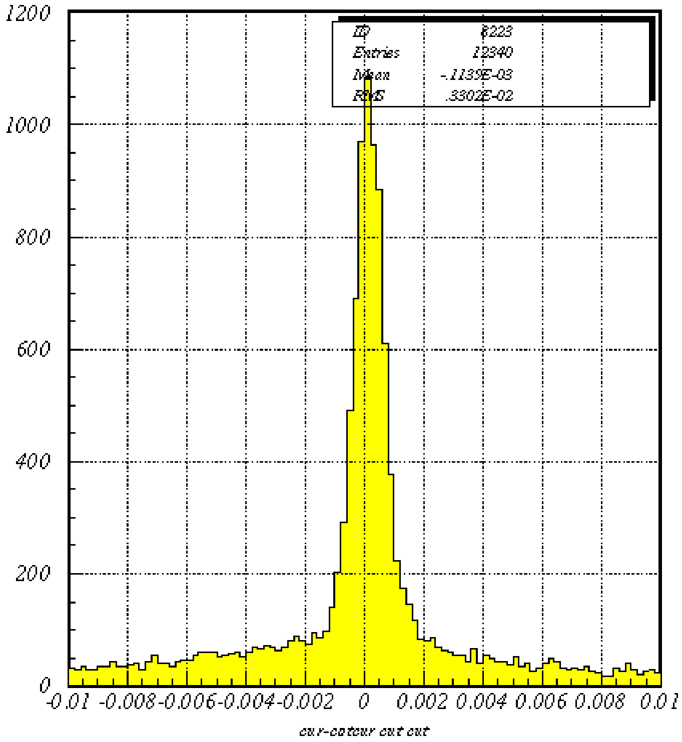
SVT performance
Not just impact parameter

Loop on all SVT-COT track pairs and compare parameters

φ: SVT – COT



Curvature: SVT - COT



Level 1 @Lum=40x10^{30} cm^{-2} sec^{-1}

- Two Major Components
  - Calorimeter Triggers: Jets, electrons, photons, etc. ~4-5 kHz

In SVT:

L1_JET10_&_ΣET90 (Higgs multijet)
L1_TWO_TRK2_&_TWO_CJET5 ($Z \rightarrow bb$)
L1_MET15_&_TWO_TRK2 (Higgs $Z \rightarrow \nu\nu$) ~2 kHz
L1_TWO_TRK10_DPHI20 (Di TAU exotic)
L1_EM8 (Gamma + bjet)
L1_CEM4_PT4 (B electron)
L1_CMUP6_PT4 (B muon)

  - Hadronic B Decays: Two XFT tracks ~11-12 kHz
- Using three classes of B triggers
  - Scenario A
    - p_T>2, $p_{T,1}+p_{T,2}$>5.5, opp. charge, $\Delta\phi$<135°; DPS
  - Scenario C
    - p_T>2.5, $p_{T,1}+p_{T,2}$>6.5, opp. charge, $\Delta\phi$<135°; PS by 2
  - Low PT
    - p_T>2, $\Delta\phi$<90°; Heavy DPS, saturate bandwidth
    - Not considered for long-term

Physics Prospects: All-Hadronic B decay Trigger

SVT

Impact parameter from the SVT → **Trigger on secondary vertices (B hadrons)**

$B^0_d \rightarrow \pi\pi$ (CP Violation)

$B^0_s \rightarrow D_s\ n\pi$ (B_s mixing)

$Z^0 \rightarrow b\bar{b}$ (b-jet calibration / top mass)

$H \rightarrow b\bar{b}$

Trigger Strategy

Level 1: **2D COT tracks (XFT)**

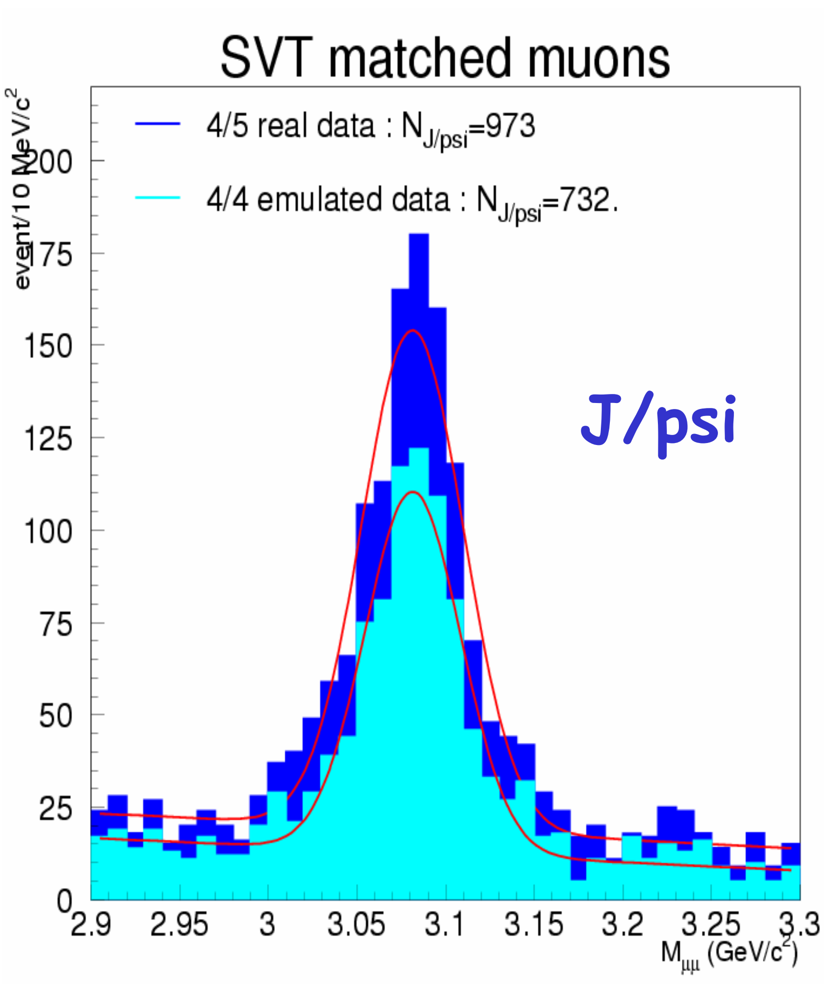
- **Two stiff tracks (P_t > 2.0 GeV/c)**
- **Remove back-to-back pairs ($\delta \phi < 135^{0}$)**
- **Opposite charge**

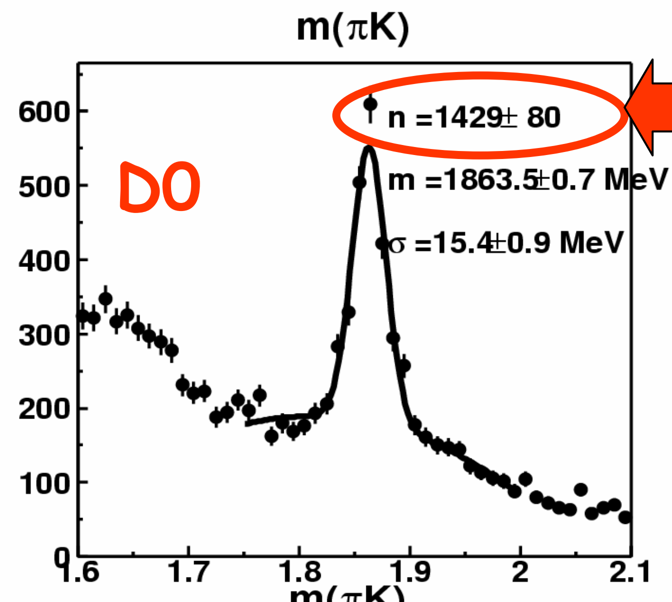
Level 2: **SVT tracks**

- **Two tracks with large impact parameter**
- **Vertex tracks - require positive decay length**

Level 3: **full event reconstruction**

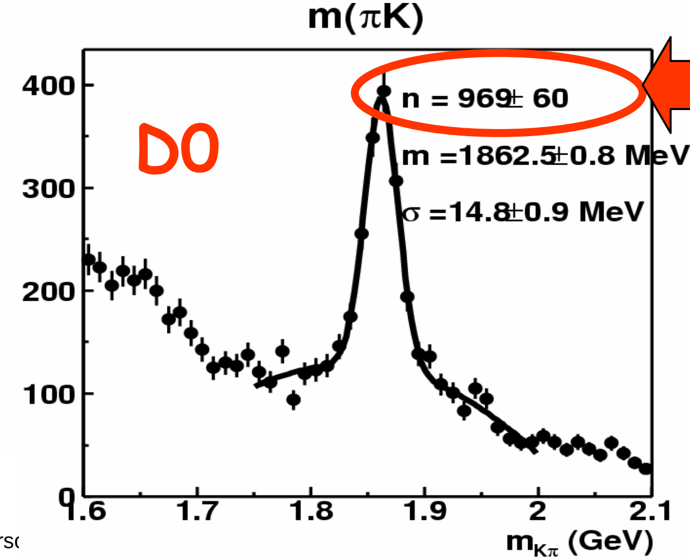
WHY 4/5? Signal Yields with 4/5





1430

4/5



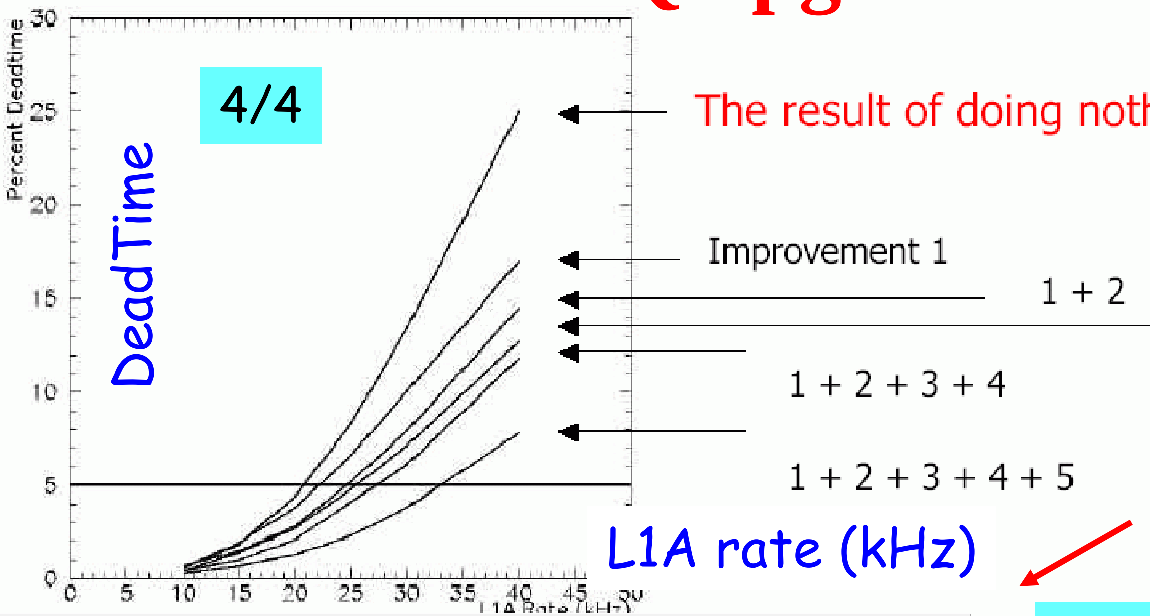
970

4/4

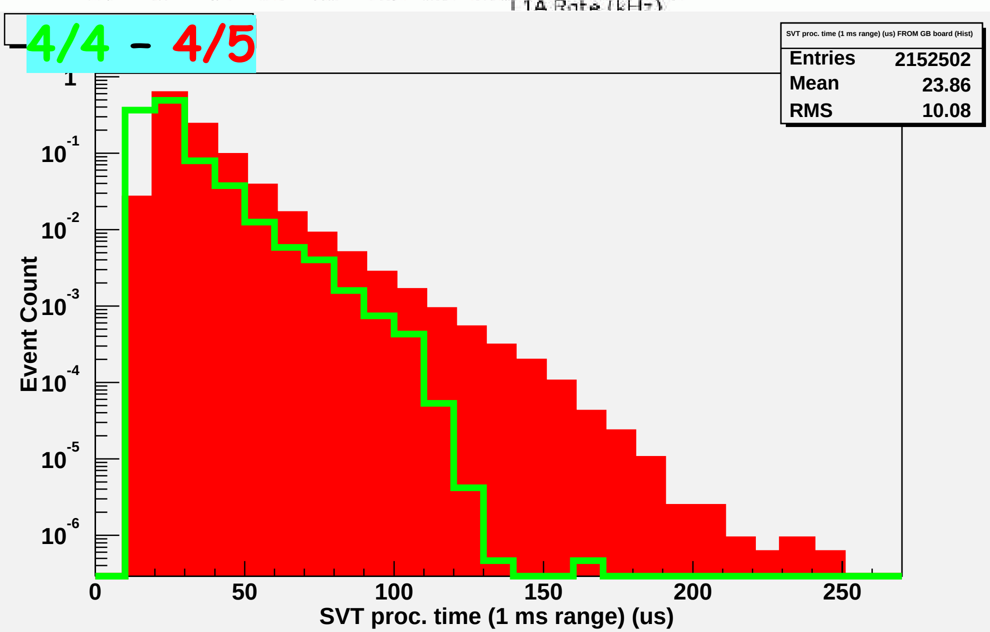
Accurate deadtime model (ModSim) to understand DAQ upgrades

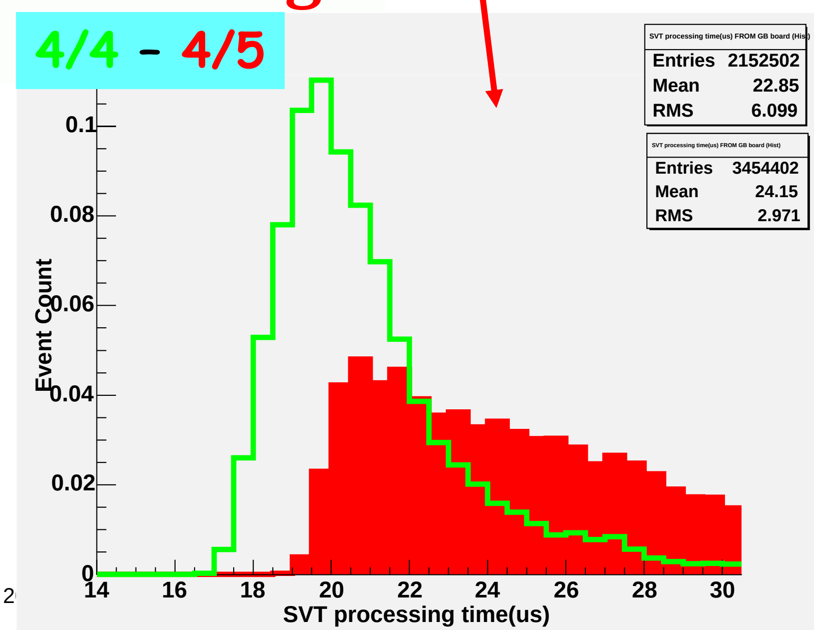
SVT

1. Two SRCs in parallel
2. L2 processor upgrade
3. 8→7 bit SVX digit.
4. - 3 μsec in SVT proc.time
5. cut SVT tails above 27 μsec



BUT the recent use of 4/5 in SVT changes the conditions!





7.6 MHz Crossing rate

CDF DAQ & Trigger

Detector

Raw Data

Level 1 pipeline: 42 clock cycles

Level 1 Trigger

L1 Accept

Level 2 buffer: 4 events

Level 2 Trigger

L2 Accept

DAQ buffers

L3 Farm

To Mass Storage (50~100 Hz)

Design goals

Level 1
- 7.6 MHz Synchromous Pipeline
- 5544 ns Latency
- **50 kHz accept rate**

~20 kHz actual

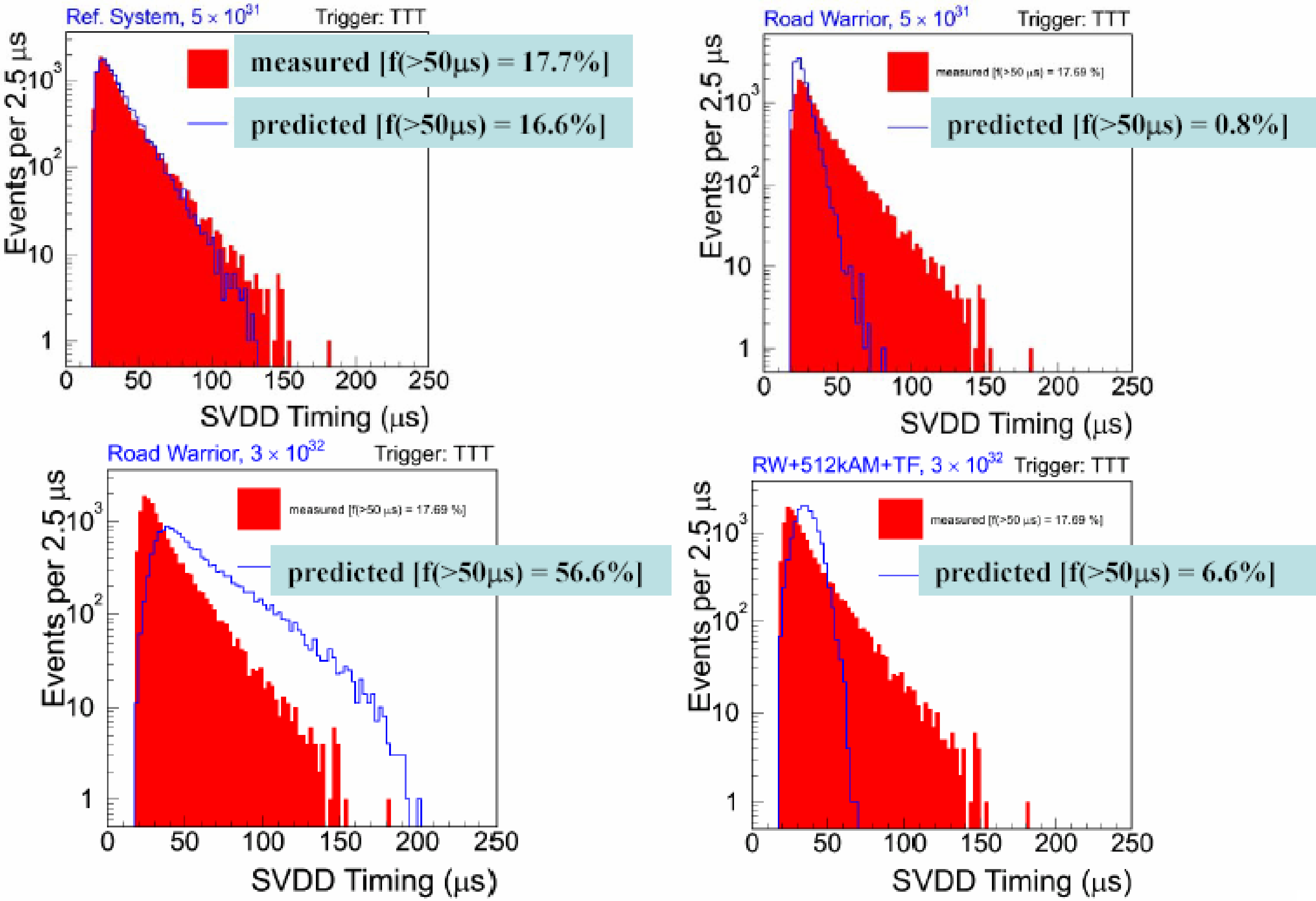
Level 2
- Asynchronous 3 Stage Pipeline
- **20 μs average Latency**
- 300 Hz accept rate

SVT here

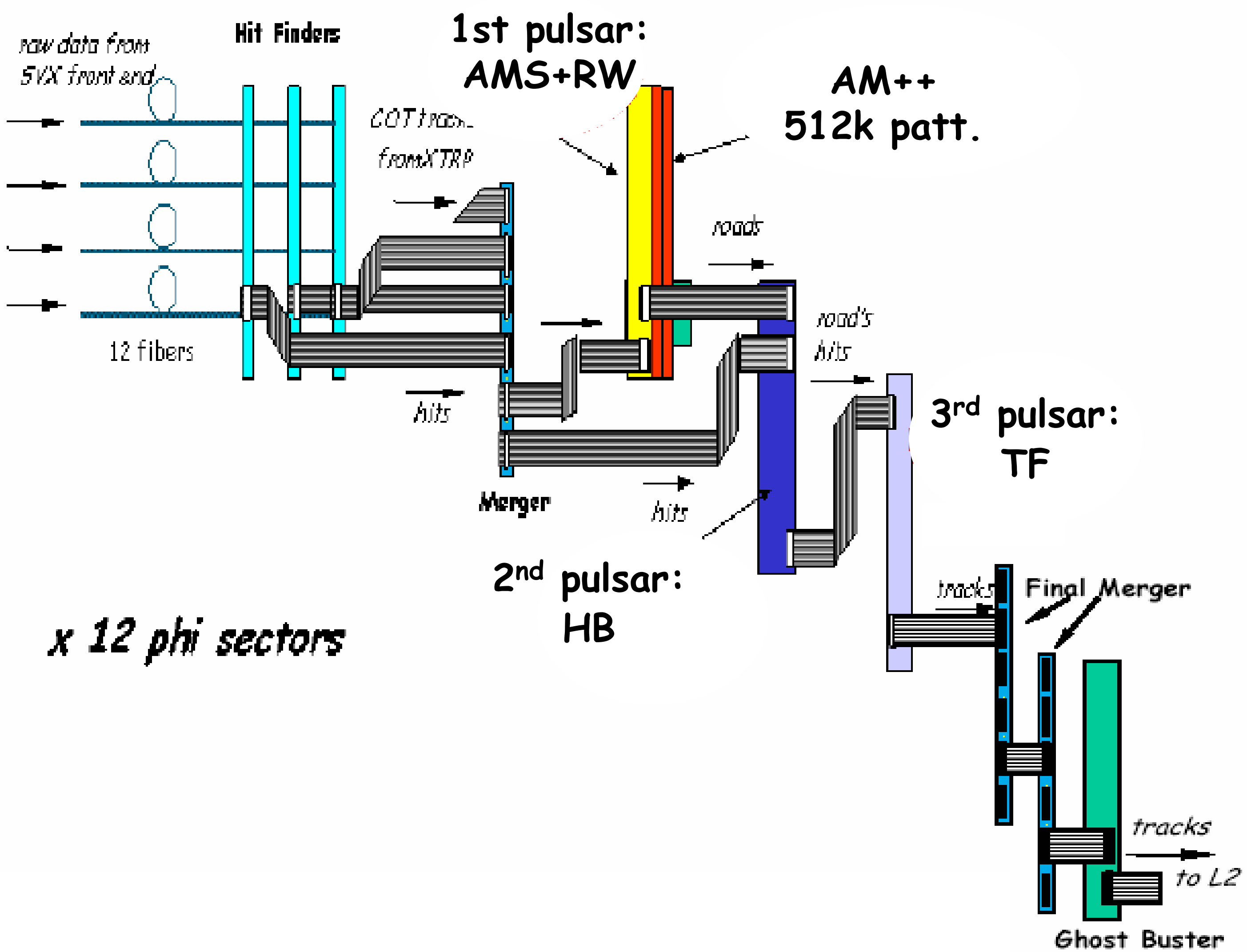
~35 μs actual

Tails are important

Extrapolate to high $\mathcal{L}$ with & without upgrades



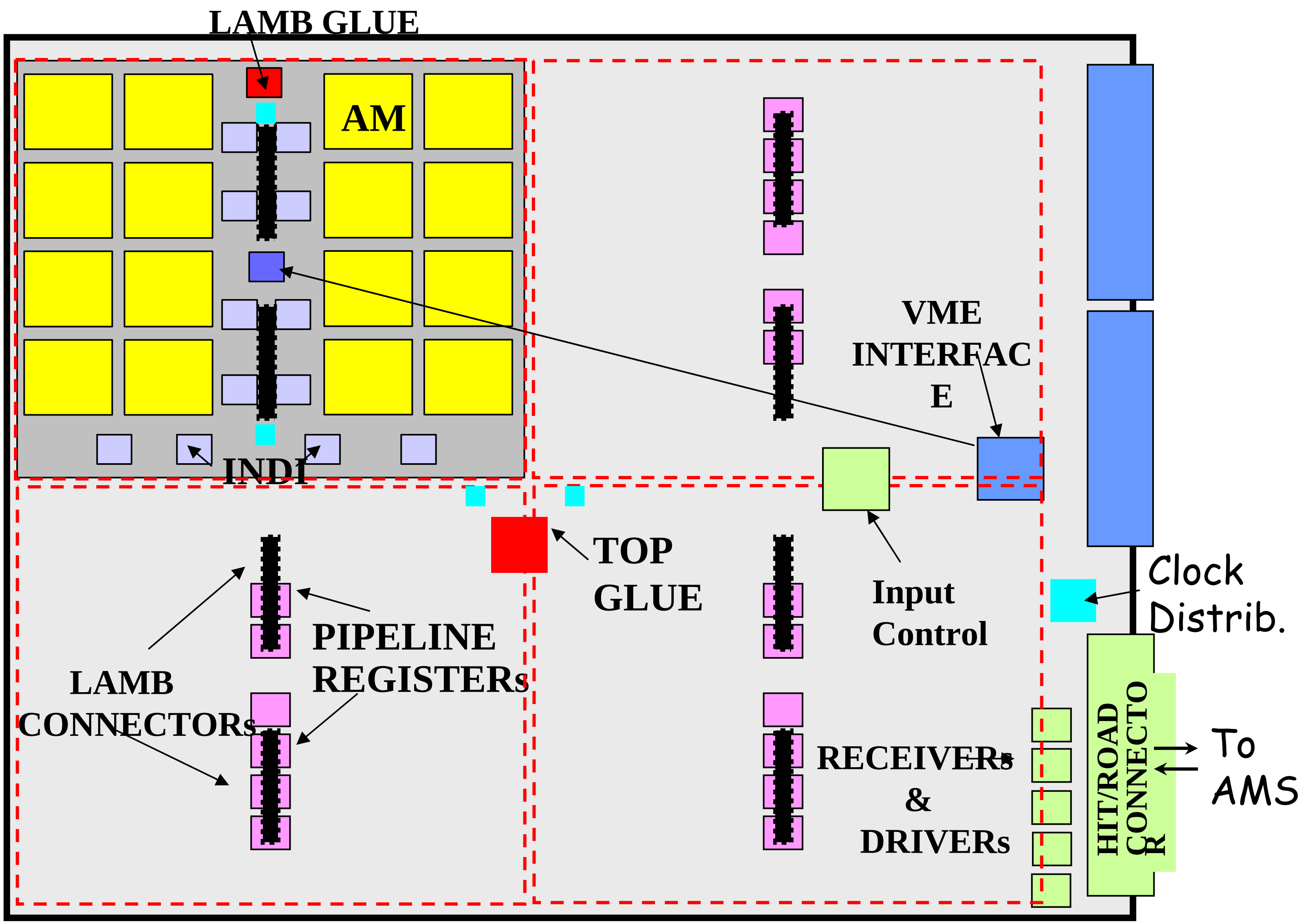
Upgrading SVT



x 12 phi sectors

512 Kpattern / phi sector

SVT

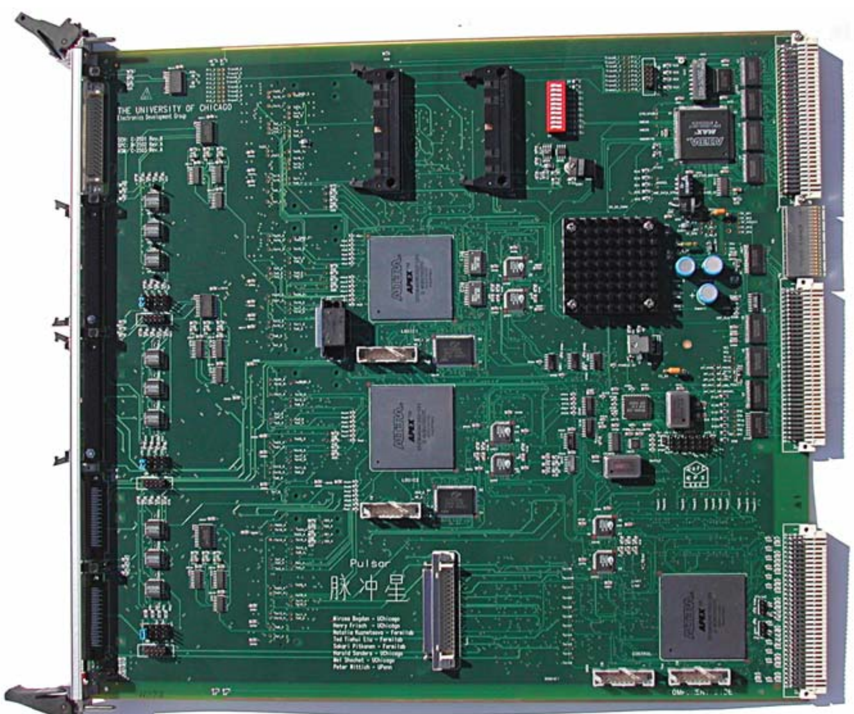


Pulsar in SVT++

SVT

Large memory cannot be handled by old SVT boards.
The new ones are developed using Pulsar

- Fast enough to handle the new amount of data
- SVT interface built in
- Developers can concentrate on firmware (= board functionalities)



Pulsar PCB, top side

Sequencer + RW

RW remove redundant roads as soon as they are returned by AM sensitively reducing the amount of data handled by the Hit Buffer

Hit Buffer and Track Fitter

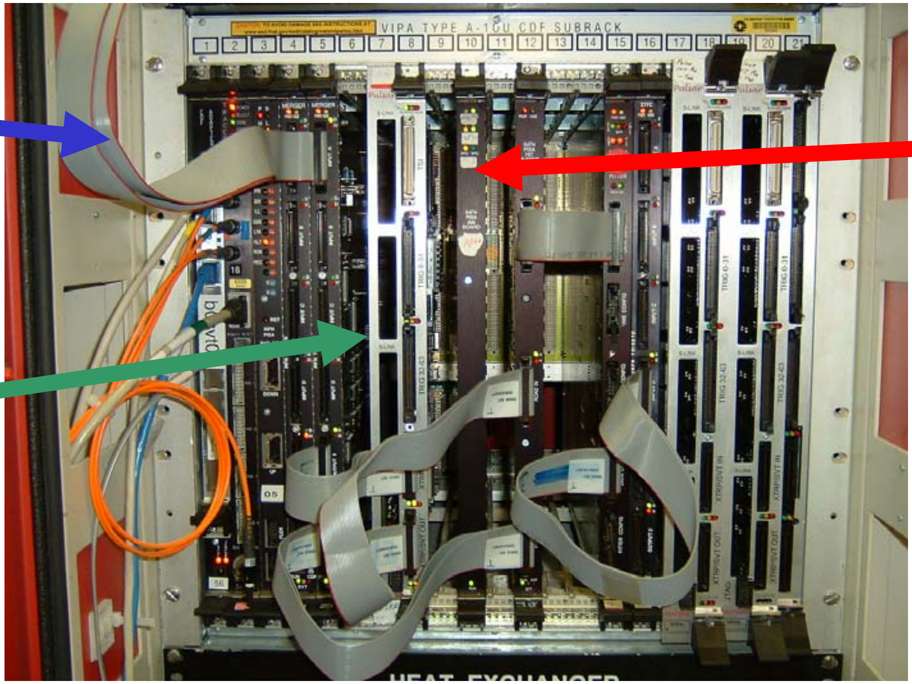
- They need to handle larger amount of roads and hits
- Fully exploit the fast logic of the Pulsar

Upgrade is on schedule

SVT

Real data

AM++



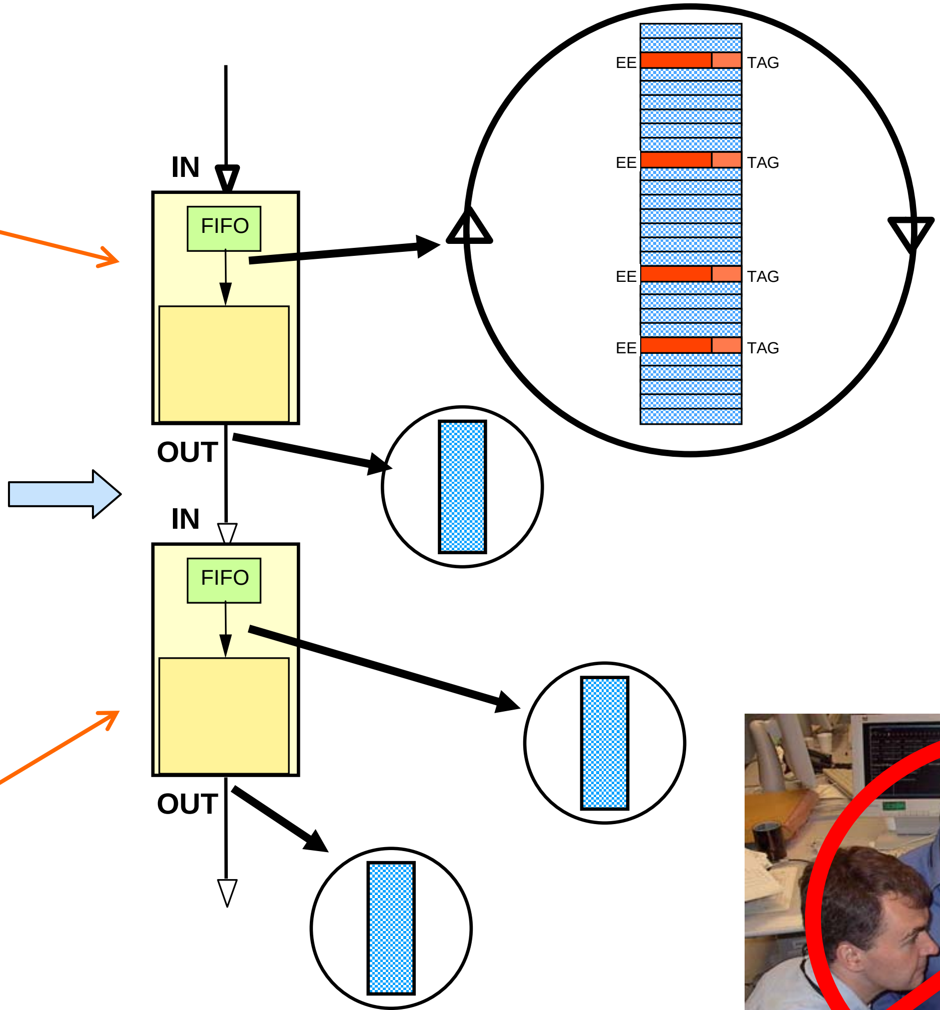
AMS/RW

- AM++ and RW with 32k patterns have been already used in test runs for data tacking
- Plan to install AM++ with 32k pattern in July
- Studies of 128k patterns coverage and efficiency are underway
- Plan to install TF++ as soon as it will be ready (August) then move to 128k
- HB++ expected to be installed during fall with 512k pattern memory

Circular buffers monitor every data link: like a built-in logic analyzer

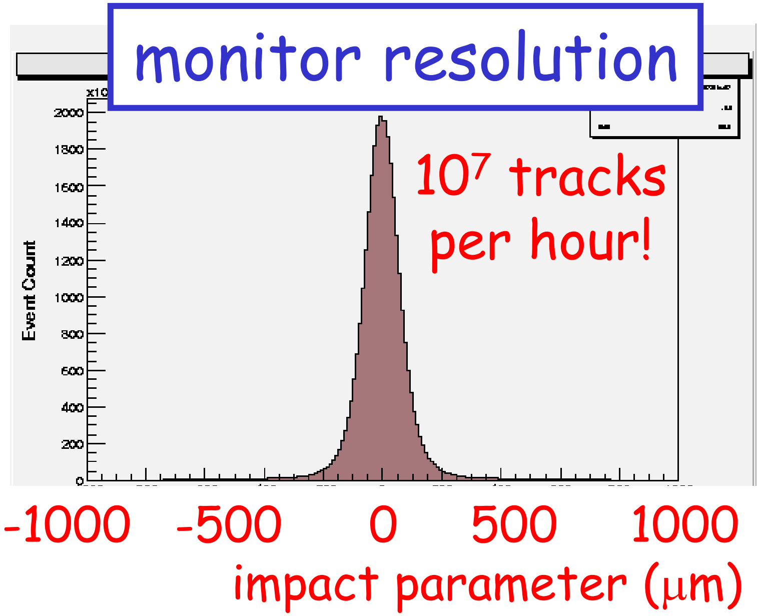
SVT board 1

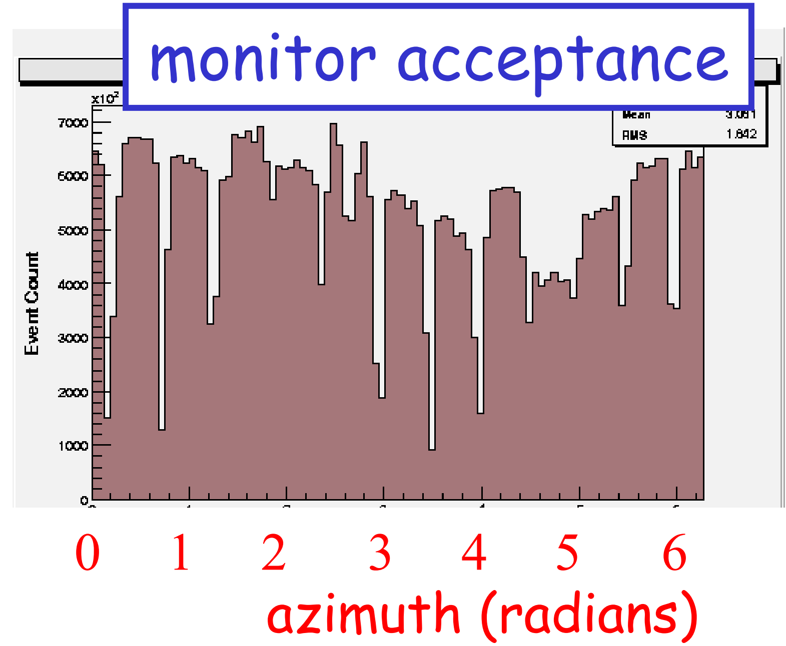
System wide uniform inter-board communication protocol

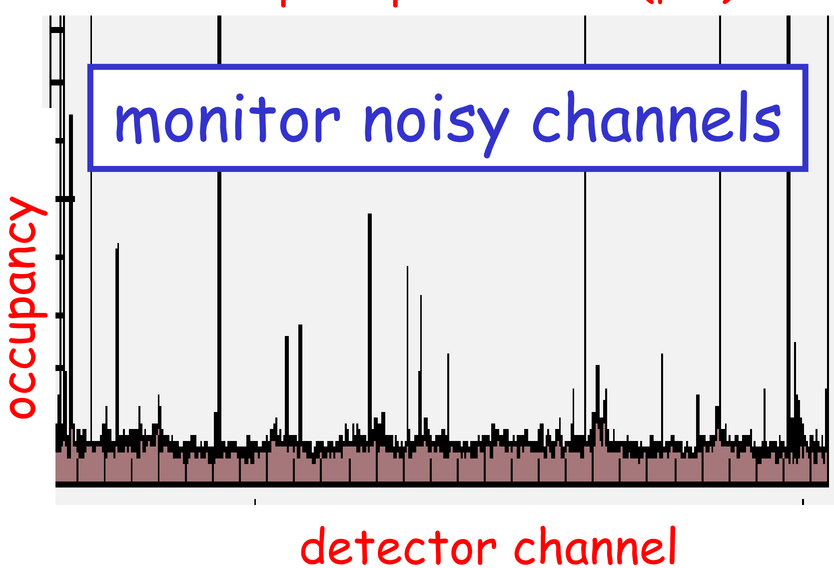


SVT board 2

On-crate monitoring of circular buffers







Sample hits, roads, tracks at high rate

Check boards against emulation software

Fit for beam position …

Why SVT succeeded

- Performance:
  - Parallel/pipelined architecture
  - Custom VLSI pattern recognition
  - Linear track fit in fast FPGAs

- Reliability:
  - Easy to sink/source test data (many boards can self-test)
  - Modular design; universal, well-tested data link & fan-in/out
  - Extensive on-crate monitoring during beam running
  - Detailed CAD simulation before prototyping
    - See poster by Mircea Bogdan

- Flexibility:
  - System can operate with some (or all) inputs disabled
  - Building-block design: can add/replace processing steps
  - Modern FPGAs permit unforeseen algorithm changes

- Key: design system for easy testing/commissioning

Doing silicon tracking quickly

- Three key features of SVT allow us to do in tens of microseconds what typically takes software hundreds of milliseconds:
  - Parallel/pipelined architecture
  - Custom VLSI pattern recognition
  - Linear track fit in fast FPGAs