

1	<b>ADDRESSING COMBINED WITH SPECIFIC MEMORY CONFIGURATION OR SYSTEM</b>	134	....Combined replacement modes
2	.Addressing extended or expanded memory	135	....Cache flushing
3	.Addressing cache memories	136	....Least recently used
4	.Dynamic-type storage device (e.g., disk, tape, drum)	137	...Look-ahead
5	.For multiple memory modules (e.g., banks, interleaved memory)	138	...Cache bypassing
6	.Virtual machine memory addressing	139	....No-cache flags
100	<b>STORAGE ACCESSING AND CONTROL</b>	140	...Cache pipelining
101	.Specific memory composition	141	...Coherency
102	..Solid-state read only memory (ROM)	142	....Write-through
103	...Programmable read only memory (PROM, EEPROM, etc.)	143	....Write-back
104	..Solid-state random access memory (RAM)	144	....Cache status data bit
105	...Dynamic random access memory	145	....Access control bit
106	....Refresh scheduling	146	....Snooping
107	..Ferrite core	147	.Shared memory area
108	..Content addressable memory (CAM)	148	..Plural shared memories
109	..Shift register memory	149	..Multiport memory
110	..Circulating memory	150	..Simultaneous access regulation
111	..Accessing dynamic storage device	151	..Prioritized access regulation
112	...Direct access storage device (DASD)	152	..Memory access blocking
113	....Caching	153	..Shared memory partitioning
114	....Arrayed (e.g., RAIDs)	154	.Control technique
115	..Detachable memory	155	..Read-modify-write (RMW)
116	..Bubble memory	156	..Status storage
117	.Hierarchical memories	157	..Interleaving
118	..Caching	158	..Prioritizing
119	...Multiple caches	159	..Entry replacement strategy
120	....Parallel caches	160	...Least recently used (LRU)
121	....Private caches	161	..Archiving
122	....Hierarchical caches	162	...Backup
123	....User data cache and instruction data cache	163	..Access limiting
124	....Cross-interrogating	164	...With password or key
125	...Instruction data cache	165	..Internal relocation
126	..User data cache	166	..Resetting
127	...Interleaved	167	.Access timing
128	...Associative	168	..Concurrent accessing
129	...Partitioned cache	169	..Memory access pipelining
130	...Shared cache	170	.Memory configuring
131	..Multiport cache	171	..Based on data size
132	...Stack cache	172	..Based on component size
133	...Entry replacement strategy	173	..Memory partitioning
		200	<b>ADDRESS FORMATION</b>
		201	.Slip control, misaligning, boundary alignment
		202	.Address mapping (e.g., conversion, translation)
		203	..Virtual addressing
		204	...Predicting, look-ahead
		205	....Directories and tables (e.g., DLAT, TLB)
		206	...Translation tables (e.g., segment and page table or map)
		207	....Directory tables (e.g., DLAT, TLB)

208	....Segment or page table descriptor	E12.001	<b>ACCESSING, ADDRESSING OR ALLOCATING WITHIN MEMORY SYSTEMS OR ARCHITECTURES (EPO)</b>
209	...Including plural logical address spaces, pages, segments, blocks	E12.002	..Addressing or allocation; relocation (EPO)
210	..Resolving conflict, coherency, or synonym problem	E12.003	..With multidimensional access, e.g., row/column, matrix, etc. (EPO)
211	.Address multiplexing or address bus manipulation	E12.004	..With look-ahead addressing means (EPO)
212	.Varying address bit-length or size	E12.005	..User address space allocation, e.g., contiguous or noncontiguous base addressing, etc. (EPO)
213	.Generating prefetch, look-ahead, jump, or predictive address	E12.006	...Free address space management (EPO)
214	.Operand address generation	E12.007	...In block-addressed memory (EPO)
215	.In response to microinstruction	E12.008	....In block-erasable memory, e.g., flash memory, etc. (EPO)
216	.Hashing	E12.009	...Garbage collection, i.e., reclamation of unreferenced memory (EPO)
217	.Generating a particular pattern/sequence of addresses	E12.01	....Using reference counting (EPO)
218	..Sequential addresses generation	E12.011	....Incremental or concurrent garbage collection, e.g., in real-time systems, etc. (EPO)
219	.Incrementing, decrementing, or shifting circuitry	E12.012	....Generational garbage collection (EPO)
220	.Combining two or more values to create address	E12.013	...Multiple users address space allocation, e.g., using different base addresses, etc. (EPO)
221	.Using table	E12.014	...Using tables or multilevel address translation means (EPO)

**E-SUBCLASSES**

The following subclasses beginning with the letter E are E-subclasses. Each E-subclass corresponds in scope to a classification in a foreign classification system, for example, the European Classification system (ECLA). The foreign classification equivalent to an E-subclass is identified in the subclass definition. In addition to US documents classified in E-subclasses by US examiners, documents are regularly classified in E-subclasses according to the classification practices of any foreign Offices identified in parentheses at the end of the title. For example, "(EPO)" at the end of a title indicates both European and US patent documents, as classified by the EPO, are regularly added to the subclass. E-subclasses may contain subject matter outside the scope of this class. Consult their definitions, or the documents themselves to clarify or interpret titles.

E12.015	..Addressing variable-length words or parts of words (EPO)
E12.016	..In hierarchically structured memory systems, e.g., virtual memory systems, etc. (EPO)
E12.017	...Addressing of memory level in which access to desired data or data block requires associative addressing means, e.g., cache, etc. (EPO)
E12.018	...Using pseudo-associative means, e.g., set-associative, hashing, etc. (EPO)
E12.019	...For peripheral storage systems, e.g., disc cache, etc. (EPO)

- E12.02 ....With dedicated cache, e.g., instruction or stack, etc. (EPO)
- E12.021 ....Using selective caching, e.g., bypass, partial write, etc. (EPO)
- E12.022 ....Using clearing, invalidating, or resetting means (EPO)
- E12.023 ....Multi-user, multiprocessor, multiprocessing cache systems (EPO)
- E12.024 .....With multilevel cache hierarchies (EPO)
- E12.025 .....With a network or matrix configuration (EPO)
- E12.026 .....Cache consistency protocols (EPO)
- E12.027 .....Using directory methods (EPO)
- E12.028 .....Copy directories (EPO)
- E12.029 .....Associative directories (EPO)
- E12.03 .....Distributed directories, e.g., linked lists of caches, etc. (EPO)
- E12.031 .....Limited pointers directories; state-only directories without pointers (EPO)
- E12.032 .....With concurrent directory accessing, i.e., handling multiple concurrent coherency transactions (EPO)
- E12.033 .....Using a bus scheme, e.g., with bus monitoring or watching means, etc. (EPO)
- E12.034 .....In combination with broadcast means, e.g., for invalidation or updating, etc. (EPO)
- E12.035 .....For main memory peripheral accesses, e.g., I/O or DMA, etc. (EPO)
- E12.036 .....With software control, e.g., non-cacheable data, etc. (EPO)
- E12.037 ....With cache invalidating means (EPO)
- E12.038 ....With shared cache (EPO)
- E12.039 ....For multiprocessing or multitasking (EPO)
- E12.04 ....With main memory updating (EPO)
- E12.041 ....Organization and technology of caches (EPO)
- E12.042 .....Of parts of caches, e.g., directory or tag array, etc. (EPO)
- E12.043 .....With plurality of cache hierarchy levels (EPO)
- E12.044 ....Multiple simultaneous or quasi-simultaneous cache accessing (EPO)
- E12.045 ....Cache with multiple tag or data arrays being simultaneously accessible (EPO)
- E12.046 .....Partitioned cache, e.g., separate instruction and operand caches, etc. (EPO)
- E12.047 .....Cache with interleaved addressing (EPO)
- E12.048 ....Cache with multi-port tag or data arrays (EPO)
- E12.049 ....Overlapped cache accessing, e.g., pipeline, etc. (EPO)
- E12.05 .....By multiple requestors (EPO)
- E12.051 .....With reload from main memory (EPO)
- E12.052 ....Cache access modes (EPO)
- E12.053 ....Burst mode (EPO)
- E12.054 ....Page mode (EPO)
- E12.055 ....Parallel mode, e.g., in parallel with main memory or CPU, etc. (EPO)
- E12.056 ....Variable-length word access (EPO)
- E12.057 ....With pre-fetch (EPO)
- E12.058 ...Address translation (EPO)
- E12.059 ....Using page tables, e.g., page table structures, etc. (EPO)
- E12.06 .....Involving hashing techniques, e.g., inverted page tables, etc. (EPO)
- E12.061 ...Using associative or pseudo-associative address translation means, e.g., translation look-aside buffer (TLB), address translation buffer (ATB), address cache, etc. (EPO)
- E12.062 ....Associated with data cache (EPO)
- E12.063 .....Data cache being concurrently physically addressed (EPO)
- E12.064 .....Data cache being concurrently virtually addressed (EPO)

- E12.065 .....For multiple virtual address spaces, e.g., segmentation, etc. (EPO)
- E12.066 ....Decentralized address translation, e.g., in distributed shared memory systems, etc. (EPO)
- E12.067 ....For peripheral accesses to main memory, e.g., DMA, etc. (EPO)
- E12.068 ....For multiple virtual address spaces, e.g., segmentation, etc. (EPO)
- E12.069 ...Replacement control (EPO)
- E12.07 ....Using a replacement algorithm (EPO)
- E12.071 .....Of the least frequently used type, e.g., with individual count value, etc. (EPO)
- E12.072 .....With age list, e.g., queue, MRU-LRU list, etc. (EPO)
- E12.073 .....Being minimized, e.g., nonMRU, etc. (EPO)
- E12.074 .....Being generated by decoding array or storage (EPO)
- E12.075 .....With special data handling, e.g., priority of data or instructions, pinning, errors, etc. (EPO)
- E12.076 .....Using additional replacement algorithm (EPO)
- E12.077 .....Adapted to multidimensional cache systems, e.g., set-associative, multi-cache, multi-set, or multilevel, etc. (EPO)
- E12.078 ..Addressing physical block of locations, e.g., base addressing, module addressing, memory dedication, etc. (EPO)
- E12.079 ...Interleaved addressing (EPO)
- E12.08 ...Address space extension (EPO)
- E12.081 ....For memory modules (EPO)
- E12.082 ....For I/O modules, e.g., memory mapped I/O, etc. (EPO)
- E12.083 ...Combination of memories, e.g., ROM and RAM, etc., to permit replacement or supplementing of words in one module by words in another module (EPO)
- E12.084 ...Configuration or reconfiguration (EPO)
- E12.085 ....With centralized address assignment (EPO)
- E12.086 .....And decentralized selection (EPO)
- E12.087 ....With decentralized address assignment (EPO)
- E12.088 .....Address being position dependent (EPO)
- E12.089 ....With feedback, e.g., presence or absence of unit detected by addressing, overflow detection, etc. (EPO)
- E12.09 ....Multi-configuration, e.g., local and global addressing, etc. (EPO)
- E12.091 .Protection against unauthorized use of memory (EPO)
- E12.092 ..By using cryptography (EPO)
- E12.093 ..By checking subject access rights (EPO)
- E12.094 ...Key-lock mechanism (EPO)
- E12.095 ....In virtual system, e.g., with translation means, etc. (EPO)
- E12.096 ...Using access table, e.g., matrix or list, etc. (EPO)
- E12.097 ...In hierarchical protection system, e.g., privilege levels, memory rings, etc. (EPO)
- E12.098 ..By checking object accessibility, e.g., type of access defined by the memory independently of subject rights, etc. (EPO)
- E12.099 ...Protection being physical, e.g., cell, word, block, etc. (EPO)
- E12.1 ....For module or part of module (EPO)
- E12.101 ....For range (EPO)
- E12.102 ...Protection being virtual, e.g., for virtual blocks or segments before translation mechanism, etc. (EPO)
- E12.103 .Protection against loss of memory contents (EPO)

**FOREIGN ART COLLECTIONS**FOR 000 **CLASS-RELATED FOREIGN DOCUMENTS**