PUBLIC

UNITED STATES OF AMERICA
BEFORE THE FEDERAL TRADE COMMISSION

In the Matter of **RAMBUS INC.,** **a corporation.**	**Docket No. 9302**

RAMBUS'S OBJECTIONS TO ATTACHMENT 1 AND APPENDIX A SUBMITTED BY COMPLAINT COUNSEL

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I. INTRODUCTION

In support of their Appeal Brief, Complaint Counsel have filed two "attachments" and three "appendices." Contrary to Complaint Counsel's representation, neither Attachment 1, which purports to analyze the differences between SDRAM and RDRAM, nor Appendix A, which purports to provide a glossary of technical terms, consists of "objective information." Rather, they contain argument regarding issues in dispute and take positions contrary to the findings of the Initial Decision in this matter. The rules require that argument of counsel be contained in a brief that is governed by a word limitation. Because Attachment 1 and Appendix A consist of improper argument, they should not be considered by the Commission.

II. RAMBUS'S OBJECTIONS TO ATTACHMENT 1

Attachment 1 to the Appeal Brief, headed "Comparison of RDRAM and SDRAM Architectures," is inaccurate and misleading in at least three respects.

A. Complaint Counsel's Attachment 1 Exaggerates The Differences Between The RDRAM And SDRAM Architecture – And Ignores Their Similarities

Attachment 1 exaggerates the differences between RDRAM and SDRAM, while ignoring the many similarities. Complaint Counsel's desire to avoid reference to those aspects of RDRAM technology that Rambus has patented and that are used in SDRAM and/or DDR SDRAM is understandable, but that does not render Attachment 1 any less objectionable. Moreover, in their zeal, Complaint Counsel overstate the differences that do exist between RDRAM and SDRAM.

Complaint Counsel assert that "RDRAM was a narrow bus, multiplexed, packetized system," while SDRAM did not share any of these attributes. In fact, the bright line that Complaint Counsel would like to draw between RDRAM and SDRAM does not exist. To distinguish it from the purportedly "narrow bus" RDRAM, Complaint Counsel describe SDRAM as a "wide-bus system, with up to 200 bus lines, in a typical

arrangement." Attachment 1 at 2. The number of bus lines has grown significantly since Complaint Counsel proposed findings last fall, where they stated that "[a] typical synchronous DRAM bus contains 100-120 parallel lines." CCPF 718. As Rambus pointed out in response, even that number was a gross exaggeration, since the first published SDRAM standard showed *no* configuration of an SDRAM chip with more than *26* bus lines connecting to it. RRPF 718. Certain configurations of RDRAM use 24 bus lines, in the same range as the 21 to 26 bus lines shown in the first published SDRAM standard. RRPF 719.

Complaint Counsel go on to say that, unlike RDRAM, SDRAM "bus lines were not multiplexed." Attachment 1 at 2. This is false. First, as Complaint Counsel's technical expert admitted, certain lines *were* multiplexed in the SDRAM bus architecture. RRPF 1268. While it is true that not all SDRAM bus lines are multiplexed, this is also the case for certain configurations of RDRAM. RRPF 721. Attachment 1 is also misleading in referring to "RDRAM" as if it were a single well-defined technology when, in fact, there were different generations of RDRAM with different numbers of bus lines and different degrees of multiplexing. *Id.*

Finally, Complaint Counsel assert that in an RDRAM system information was sent in "sequential waves of signals," while in an SDRAM system "signals were sent as a simultaneous wave." Attachment 1 at 2-3. In fact, it is not true that all the signals relevant to a given operation were sent simultaneously in an SDRAM system. For example, as Complaint Counsel themselves explain, the row address and column address related to a given read or write operation are sent sequentially in SDRAM systems. CCPF 1306.

B. Complaint Counsel's Attachment 1 Exaggerates SDRAM's Supposed Advantages

The Attachment also confuses the time lines and relative advantages and disadvantages of RDRAM as opposed to SDRAM and DDR SDRAM. Complaint

Counsel refer to SDRAM and DDR SDRAM architecture as "traditional," as though they predated RDRAM. Attachment 1 at 4. In fact, RDRAM came first. JEDEC did not even arguably begin consideration of a synchronous DRAM device until May 1991, CCPF 513, over a year after Rambus had filed its patent application. The first RDRAM was produced by Toshiba in the 1991-92 time frame, RPF 643, at a time when the features of SDRAM were still being debated at JEDEC.

Complaint Counsel go on to assert that it was "the majority view during the early to mid-1990s" that SDRAM and DDR SDRAM "would dominate the mainstream memory market." Attachment 1 at 4. But, as Judge McGuire found, discussions about DDR SDRAM did not even begin until 1996. IDC at 277-79. While SDRAM did become the dominant memory technology in the late 1990s, there is no evidence to support Complaint Counsel's assertion that DDR SDRAM, technology that was not yet even under discussion, was seen as SDRAM's successor in the "early to mid-1990s." The testimony of Howard Sussman and Gordon Kelley cited by Complaint Counsel relates only to the personal views of those gentlemen about SDRAM and RDRAM in the early 1990s and certainly does not support Complaint Counsel's assertion.

C. Complaint Counsel's Attachment 1 Ignores The True Reasons For The Unsuccessful Marketplace Introduction Of The RDRAM Device

Complaint Counsel assert that, after Intel chose Direct RDRAM as the next generation of main memory, "technical problems . . . [led] Intel to change its position and launch a chipset supporting SDRAM and DDR SDRAM." Attachment 1 at 4. However, the evidence showed that it was not "technical problems" that ultimately forced Intel to abandon its choice of RDRAM as the next generation of main memory. Rather, several major DRAM manufacturers, including Infineon, Micron and Hynix, became alarmed by the possibility that Intel's selection of RDRAM technology would lower their profits and cause them to lose control of future DRAM design and implementation, and engaged in collusive conduct that resulted in lower production and higher prices of RDRAM, which

limited and ultimately prevented RDRAM's successful market launch. IDF 526-559; RPF 1548-1602.[1]

RDRAM's lack of success caused substantial consumer harm, since it represented the best solution from a cost/performance perspective. As one of Complaint Counsel's own witnesses -- an Intel executive closely involved in the RDRAM launch -- testified at trial:

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MacWilliams, Tr. 5075 (*in camera*), *quoted* and afforded *in camera* treatment in IDF 557.

III. RAMBUS'S OBJECTIONS TO APPENDIX A

Complaint Counsel's "Glossary of Terms" is not only riddled with errors, but also, under the guise of "objectivity," takes positions on issues in dispute in this matter, without bothering to tell the Commission that the issues are disputed and without bothering to cite to record evidence in support of their position. Some examples of the errors and disputed facts in Appendix A follow; this is not, however, meant to be an exhaustive list of all the errors in Appendix A and does not signify agreement with

[1] Judge McGuire found, for example, that Hynix executive Farhad Tabrizi had "admitted at trial that he had told Sang Park, then the President and Chief Operating Officer of [Hynix], that he wanted to 'kill' Rambus and force RDRAM from the market." IDF 553. Judge McGuire also found that Tabrizi had urged other manufacturers to "stick together" and say "NO TO RAMBUS AND NO TO INTEL DOMINATION." IDF 526, 529 (*quoting* RX 778 at 1 and RX 802 at 3). Similarly, Judge McGuire found that Micron had in October 1998 proposed to other DRAM manufacturers that they agree to a "common roadmap" that the manufacturers would then present to customers. IDF 512. A "main target" of the common roadmap was to remove the "currrent uncertainty about the supply situation" among chipset companies and PC OEMs. *Id*. Not surprisingly, the "common roadmap" did not show any market share for Rambus. RX 2191 at 2.

particular "definitions" that are not addressed below.

A. Auto Precharge

Complaint Counsel provide a nonsensical definition of "auto precharge," stating that precharging "eliminates the data stored in the DRAM in order to prepare for the next operation." Of course, if the next operation were intended, for example, to read data from the DRAM, eliminating all the data beforehand would be ill-advised. In fact, precharging only eliminates the data temporarily stored in one part of the DRAM, the "sense amplifiers," as part of a read or write operation, while retaining all of the data in the memory cells. Moreover, while mentioning that auto precharge is included on both SDRAM and DDR SDRAM, Complaint Counsel neglect to mention that the feature was invented by Rambus and first included on RDRAM.

B. DDR SDRAM Standard

Complaint Counsel's definition suggests that the DDR SDRAM standard consisted simply of adding features to the previous SDRAM standard. This is not based on any evidence in the record and is incorrect; some features of SDRAM were changed or removed by the DDR standard. For example, while a burst stop command could be used during read or write operations in SDRAMs, the command could only be used during read operations in DDR SDRAMs. Likewise, unlike SDRAMs, DDR SDRAMs were not capable of "full page" bursts of data.

Moreover, the statement that DDR SDRAM "was developed during the mid to late 1990s at JEDEC" is contrary to Judge McGuire's findings. First, DDR SDRAM development began outside JEDEC. IDF 372-74, 376-78. Second, DDR development at JEDEC did not begin until December 1996. IDF 371-74, 376-78.

C. Dual Bank Design/Multibank Design

Complaint Counsel's definition suggests that SDRAM and DDR only have two banks. In fact, they generally have four banks.

D. Externally Supplied Reference Voltage

Complaint Counsel state that this technology is included on SDRAM. This is contrary to the Initial Decision which found that "Complaint Counsel did not present evidence sufficient to find that [externally supplied reference voltage] was ever balloted or incorporated into the SDRAM standard." IDF 350.

E. IEEE

The statement that "IEEE working groups sometimes work in conjunction with JEDEC subcommittees in developing certain standards" is not based on any evidence.

F. Multiplexed Bus

The proposed definition is vague and unhelpful. As the Federal Circuit explained, "[m]ultiplexing refers to the sharing of a single set of lines to send multiple types of information." *Rambus Inc. v. Infineon Technologies AG*, 318 F.3d 1081, 1094 (Fed. Cir. 2003). A "multiplexed bus" would simply be a bus that uses multiplexing.

G. Narrow/Wide Bus

The definition is unhelpful. As discussed above in connection with Attachment 1, the various memory devices at issue can be used with varying numbers of bus lines, and all multiplex the bus lines to varying degrees.

H. Packetized/Packet-Based Operation

The definition is vague and unhelpful. Moreover, contrary to Complaint Counsel's statement, the broad definition of "packet" given applies to SDRAMs and DDR SDRAMs in which row address information and column address information in connection with a particular read or write operation is transmitted over multiple clock cycles.

I. Phase Lock Loops/Delay Lock Loops

Contrary to the statement in the definition, DDR SDRAM and RDRAM use DLLs in similar ways. Furthermore, the statement that the original version of SyncLink's

DRAM did not use PLLs or DLLs is highly misleading. In fact, the SyncLink Consortium tried to design a high-speed DRAM without using PLLs or DLLs, but ultimately had to include the technology in order to meet timing constraints. IDF 1374-75.

J. RDRAM

Complaint Counsel's definition of RDRAM is replete with inaccuracies and misleading statements. Perhaps most egregious is the attempt to describe the host of inventions made by Drs. Farmwald and Horowitz in 1989-90 as "characterized by," or whose "basic notion" was nothing more than, a "narrow bus" – i.e. using relatively few bus lines. The breadth of the Rambus inventions, many of which are used in SDRAMs and DDR SDRAMs, is described in Rambus's appeal brief.

K. SDRAM

As discussed above in connection with Attachment 1, the statement that the number of bus lines in an SDRAM system "often rang[es] from 100 to 200 parallel bus lines" is not supported by the evidence. Although Complaint Counsel assert that "SDRAM memory is often referred to as having a wide-bus architecture," Rambus is unaware of any instance in which SDRAM was referred to in that way outside the context of this case and related patent litigation.

L. SDRAM Lite

It is not true that in some SDRAM Lite proposals both burst length and CAS latency were to be fixed. Complaint Counsel did propose a finding to that effect, CCPF 572; however, the evidence did not support the finding and Judge McGuire found that, in fact, the proposal involved multiple burst lengths. IDF 365. Complaint Counsel also neglect to mention that the SDRAM Lite proposal lost support at JEDEC and was abandoned. IDF 369.

M. SyncLink

Complaint Counsel's definition of SyncLink is highly misleading in what it chooses to omit. For example, Judge McGuire found that "the SyncLink Consortium was well aware that that their work could or would violate [Rambus intellectual property]." IDC at 308. Complaint Counsel's definition also ignores the findings of fact suggesting that the purpose of the SyncLink Consortium was to block RDRAM by presenting a purported alternative. *See* IDF 484-85. The statement that "SyncLink never achieved significant market penetration," which suggests that there was actually a SyncLink product, is misleading. In fact, SyncLink's chip never went into volume production. IDF 486.

N. System Clock

The statement that a clock signal resembles a sine wave is incorrect. Clock signals are approximations of square waves.

O. Source Synchronous Clocking

The definition states that, in source synchronous clocking, "a clock signal travels with the data," and that this technology is used in DDR SDRAM. This is incorrect. In DDR SDRAM, a strobe signal travels with the data. CCPF 648. The data strobe in DDR SDRAMs is *not* a clock signal. IDF 410.

IV. CONCLUSION

For all of the foregoing reasons, the Commission should decline to consider Complaint Counsel's Attachment 1 and Appendix A.

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CERTIFICATE OF SERVICE

I, Rebecca A. Williams, hereby certify that June 14, 2004, I caused a true and correct copy of the public version of *Rambus's Objections to Attachment 1 and Appendix A Submitted by Complaint Counsel* to be served on the following persons by hand delivery:

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CERTIFICATION

I, Rebecca A. Williams, hereby certify that the electronic copy of the public version of *Rambus's Objections to Attachment 1 and Appendix A Submitted by Complaint Counsel* accompanying this certification is a true and correct copy of the paper version that is being filed with the Secretary of the Commission on June 14, 2004 by other means.

Rebecca A. Williams
June 14, 2004