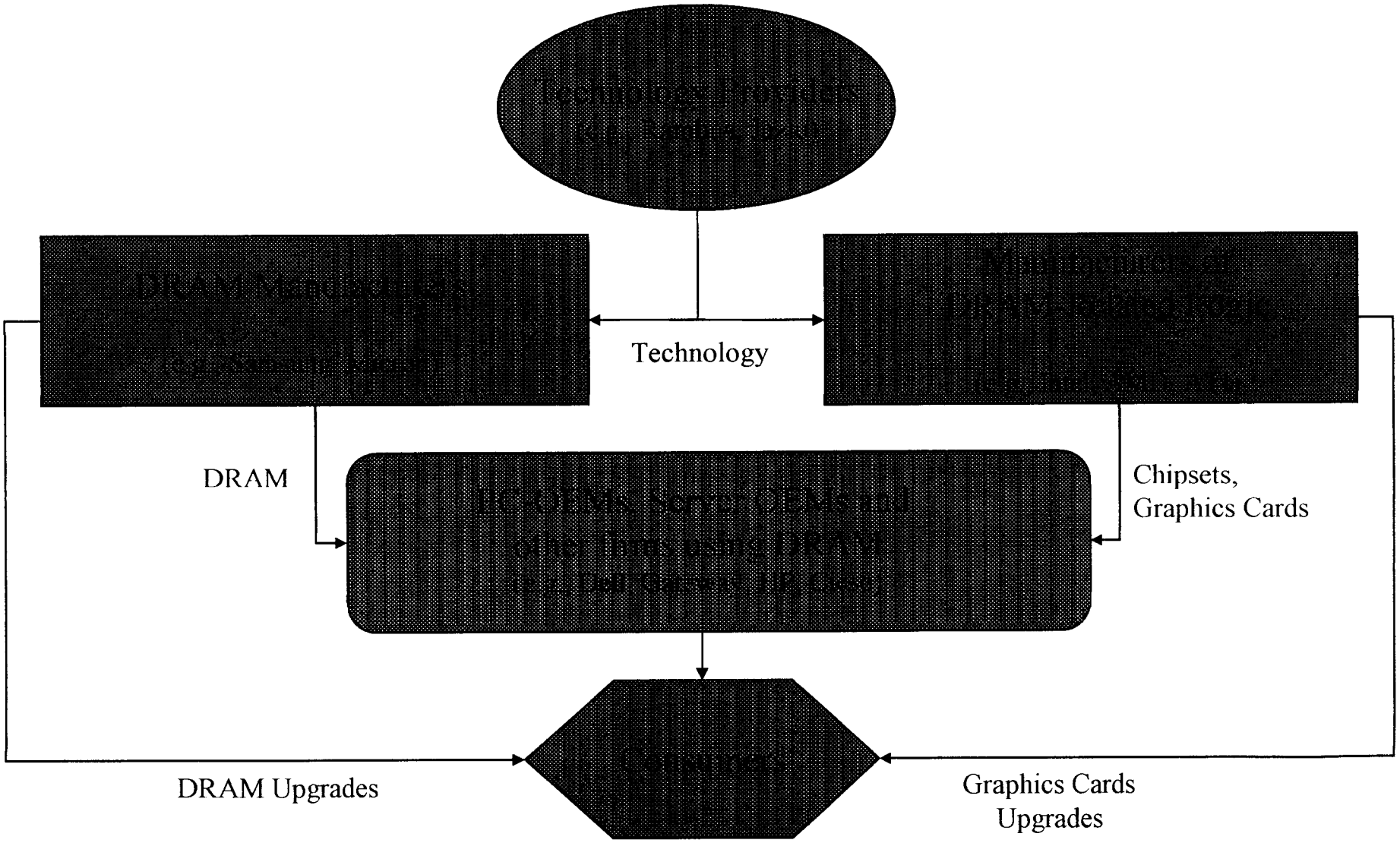
Interviews Conducted

- DRAM engineers
- DRAM plant managers
- JEDEC participants
- DRAM users

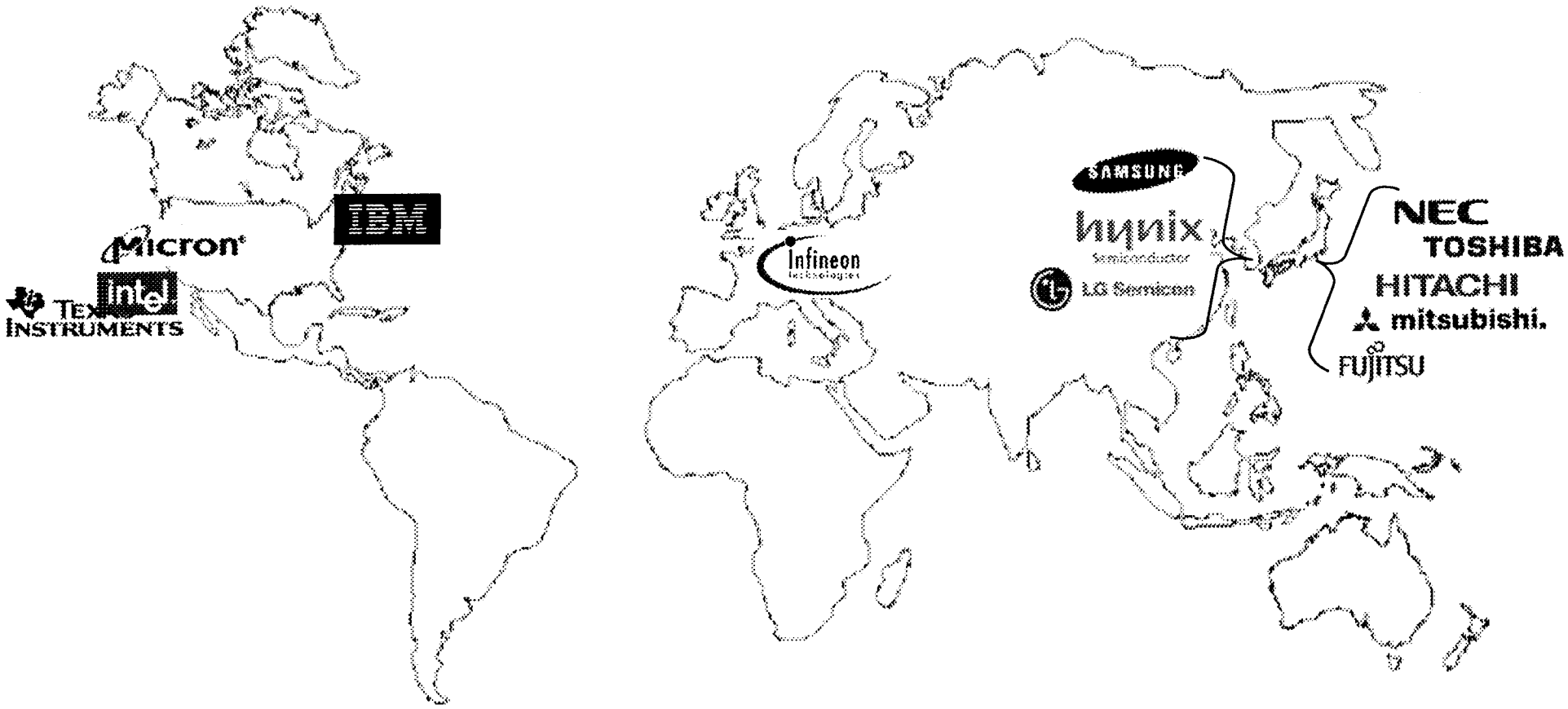
Case Study

- Methodology: Comprehensive review of public / private reports and information
- Focus: evolution of DRAM standards / technologies
- Time period: 1990 to present
- Information sources: publicly available materials, trade press, analyst reports, discovery materials
- Purpose: assessing economic factors influencing choices among alternative DRAM technologies / standards

DRAM Industry Overview



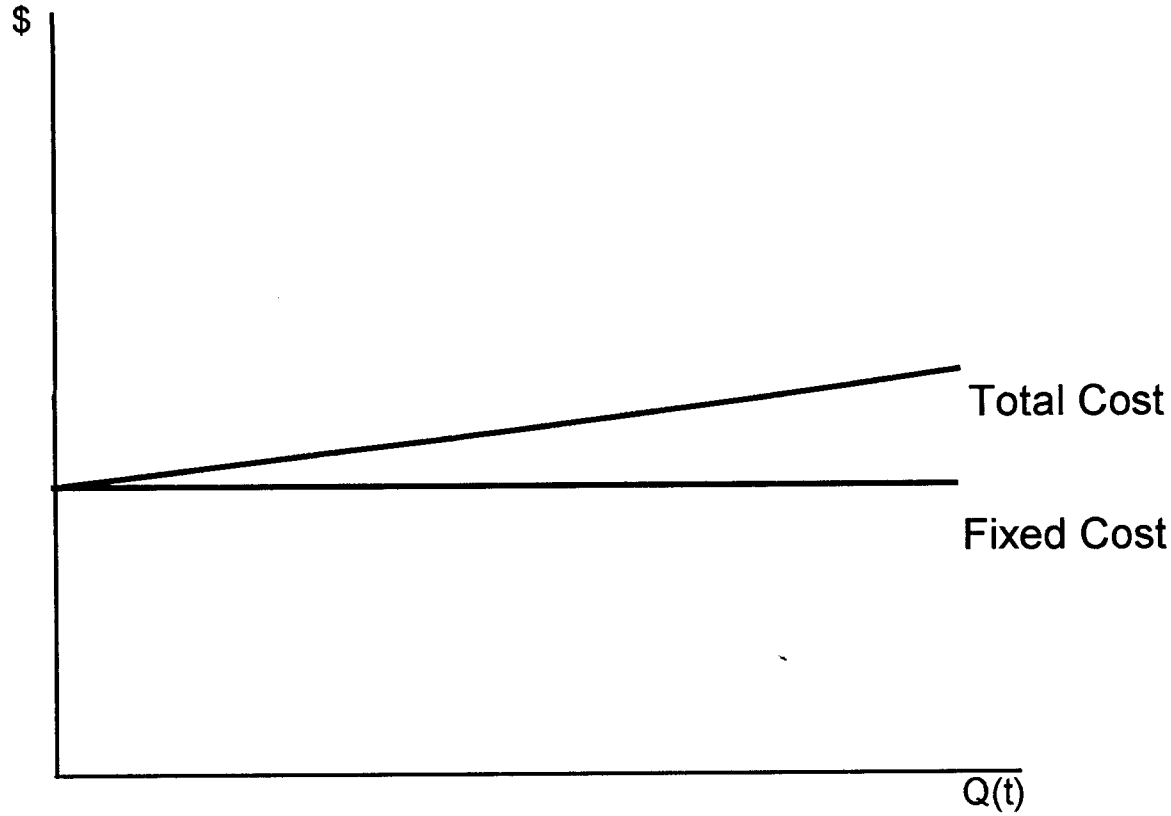
DRAM Chip Manufacturers in the Past



Economics of DRAM Production

- High fixed costs
- Volatility / cyclicality
- Intense price competition
- Maximize capacity utilization / yield
- Intense cost cutting

Total Cost and Fixed Cost



Reducing DRAM Production Costs / Increasing Yields

- 24/7 operation
- Clean rooms
- Extended equipment life
- Optimized production process
- Die shrinks
- Larger wafer size

Economic Factors Influencing Success of DRAM Standards

- Open, consensus-based process
- Open availability of standard
- Royalties
- Implementation costs
- Manufacturing costs
- Evolutionary / revolutionary

JEDEC: IP Disclosure

- Preference to avoid patents
- Early disclosure / good faith
- Disclosure applies to patents / patent applications relevant to JEDEC standards / work
- RAND: mandatory for JEDEC; voluntary for members
- Valid technical justification

Latency Technology Market

- Fixed CAS latency
  - Presented at JEDEC
    - NEC Presentation at 42.3 Committee Meeting 76 (9/95)
  - Cost impact
    - "A fixed DRAM is easier to test. Every time you add a new feature to the DRAM, you have to test it. So, from a test cost point of view, there would have been an advantage to fixing every function in the DRAM, including programmable CAS and burst length." *Macri Trial Testimony at 4773*
    - Potentially higher inventory costs to DRAM manufacturers – *Macri Trial Testimony at 4763-64*

Latency Technology Market

- Programmable by pin strapping
  - Presented at JEDEC
    - Micron Presentation at Special 42.3 Committee Meeting (7/00)
  - Cost impact
    - "Q. So, one of the costs of these -- of this alternative would have been to add extra pins on the DRAM? A. Yes, but if you're smart, you do it in a way where the cost is exceedingly minimal, and that's what, you know, we try to build the products on, being smart." *Macri Trial Testimony at 4767*

Latency Technology Market

- Programmable in read command
  - Not presented at JEDEC
    - Mitsubishi Presentation at 42.3 Committee Meeting 60 (12/91) (Programming Burst Length)
  - Cost impact
    - "The advantage would be that you would eliminate the mode register and the circuitry required to decode special commands and put that information into the mode register, so it would make the part potentially smaller and simpler." *Jacob Trial Testimony at 5391-92*

Latency Technology Market

- Set by fuses
  - Presented at JEDEC
    - Cray Presentation at 42.3 Committee Meeting 62 (5/92)
  - Cost impact
    - "It would be potentially a simpler design. You would eliminate the mode register. It would be potentially a smaller design and therefore a cheaper design. After blowing the fuse, you would only need to test one CAS latency value instead of having to test all possible CAS latency values, so it would be a cheaper alternative potentially." *Jacob Trial Testimony at 5382*

Burst Length Technology Market

- Fixed burst length
  - Presented at JEDEC
    - NEC Presentation at 42.3 Committee Meeting 76 (9/95)
  - Cost impact
    - "A fixed DRAM is easier to test. Every time you add a new feature to the DRAM, you have to test it. So, from a test cost point of view, there would have been an advantage to fixing every function in the DRAM, including programmable CAS and burst length." *Macri Trial Testimony at 4773*

Burst Length Technology Market

- Programmable by pin strapping
  - Not presented at JEDEC
    - Micron Presentation at Special 42.3 Committee Meeting (7/00) (Programming CAS latency)
  - Cost impact
    - "The cost associated with each of those was relatively similar in the large scheme of things, so I would say from a cost standpoint, that was a large factor in our decision." *Kellogg Trial Testimony at 5132*

Burst Length Technology Market

- Programmable in read command
  - Presented at JEDEC
    - Mitsubishi Presentation at 42.3 Committee Meeting 60 (12/91)
  - Cost impact
    - "Well, again, you would get rid of the mode register and therefore the circuitry required to initialize it, which would make the part simpler to design and test and potentially cheaper to manufacture." *Jacob Trial Testimony at 5407-408*

Burst Length Technology Market

- Burst interrupt
  - In SDRAM and DDR SDRAM standards and proposed for DDR-2
  - Cost impact
    - "I mean, for DDR2, the DDR2 SDRAM standard, we do have burst interrupt, and it is fixed, and it's not a burden to the DRAM designers. The DRAM designers, if I recall their words, they said this is easy." *Macri Trial Testimony at 4775*

Data Acceleration Technology Market

- Double the clock frequency
  - Presented at JEDEC
    - VLSI Presentation at 42.3 Committee Meeting 78 (3/96)
  - Cost impact
    - "Well, a faster single edge clock has some enormous benefits in that we don't have to pay attention to this concept called duty cycle. Duty cycle -- you know, a clock has a pulse that is high and a pulse that is low, and the duty cycle is the length of the high pulse versus the length of the low pulse, and managing that is very difficult across real world conditions. It sounds simple; very complicated. Single edge clocking doesn't have that issue at all. So, that's a huge benefit to single edge clocking." *Macri Trial Testimony at 4779-4780*

Clock Synch Technology Market

- Put the DLL on the memory controller
  - Presented at JEDEC
    - Samsung Presentation at 42.3 Committee Meeting 78 (3/96)
  - Cost impact
    - "You would eliminate the on-chip DLL, which would reduce the power consumption of the DRAM. It would reduce the die size of the DRAM, which would reduce the manufacturing cost of the DRAM. You would reduce the testing costs of the DRAM because you don't have this PLL or, rather, this DLL that would be part of the DRAM. It would be a simpler design because it would not include a DLL and therefore cheaper, take less time. And it would cancel out more timing uncertainty than simply putting the DLL out on the DRAM itself, so you could potentially reach higher rates of speed than just using an on-chip DLL alone." *Jacob Trial Testimony* at 5446-5447

Clock Synch Technology Market

- PLL/DLL on module
  - PLL on DIMM in registered DIMMs and in Kentron QBM DIMM
  - Cost impact
    - "You eliminate the on-chip DLL from the DRAM, thereby reducing its power consumption, reducing its cost, reducing the design time. … [Y]ou then move that design complexity onto a special DLL chip that goes onto the module, so you would be trading one for the other." *Jacob Trial Testimony* at 5450

Clock Synch Technology Market

- Vernier
  - Presented at JEDEC
    - Synclink Presentation at 42.3 Committee Meeting 75 (5/95)
  - Cost impact
    - "It's simpler to design than a DLL and it would cancel out potentially more skew than a DLL so you could potentially achieve higher data rates using it. And burn less power." *Jacob Trial Testimony at 5452*

Clock Synch Technology Market

- No DLL at all
  - Presented at JEDEC
    - SGI Presentation at 42.3 Interim Committee Meeting (7/97)
  - Cost impact
    - "Q. Now, what, if any, would be the advantages of relying on a DQS data strobe to provide timing rather than using on-chip DLLs?
    - A. Well, you would eliminate your DLL, which would make your design simpler. It would consume less power. The design would be smaller, cheaper to manufacture, and so forth."
    - *Jacob Trial Testimony at 5457*

Asynchronous – Burst EDO

- Alternative to both programmable CAS latency and burst length in SDRAM
- Often presented at JEDEC
  - NEC Presentation at 42.3 Committee Meeting (3/95)
- Cost impact
  - "It would have been a simpler transition because the technology existed at the time. This was a technology that the engineers of the time were more familiar with. Asynchronous DRAM tended to have smaller die sizes like burst EDO at the time had a smaller die size than SDRAM and had better performance at the same speeds. So asynchronous potentially had better performance and cheaper implementation." *Jacob Trial Testimony at 5395-96*

Reasons Why Rambus's Challenged Conduct Is Exclusionary

- Distorted JEDEC's standard setting process by concealing (or misrepresenting) material information
- Excluded alternative commercially viable DRAM technologies
- Entailed a conscious choice to jeopardize the enforceability of patented intellectual property

If Rambus Had Disclosed IP to JEDEC: No RAND Letter

- Rambus documents state RAND not consistent with business model
- Rambus wanted flexibility to charge different royalty rates
- Rambus wanted RDRAM to succeed
- Not issuing RAND letter could have helped RDRAM
- Without RAND letter, JEDEC could not include IP in standard

Exclusionary Conduct: Rambus's Costly Investment

- By not disclosing IP *ex ante*, Rambus knowingly incurred risk of having patents found unenforceable
- Implication is that Rambus expected compensating benefits from non-disclosure
- Like predatory pricing, this conduct is irrational absent expected benefits from excluding competition