PUBLIC

UNITED STATES OF AMERICA

BEFORE THE FEDERAL TRADE COMMISSION

In the Matter of **RAMBUS INC.,** **a corporation.**	**Docket No. 9302**

RESPONDENT RAMBUS INC.'S SUPPLEMENTAL RESPONSES TO COMPLAINT COUNSEL'S FIRST REQUEST FOR ADMISSIONS

Pursuant to section 3.32 of the Federal Trade Commission's Rules of Practice, Respondent Rambus Inc. ("Rambus") hereby supplements and/or revises its responses to certain requests in the First Request for Admissions propounded by Complainant. Rambus incorporates by reference the General Objections in its Responses to Complaint Counsel's First Request for Admissions filed on February 7, 2003.

REQUEST FOR ADMISSION NO. 1:

Admit that, to comply with JEDEC Standard No. 21-C, an SDRAM device must contain a mode register to store a value to determine CAS latency, where that value can be changed by programming the mode register.

RESPONSE TO REQUEST FOR ADMISSION NO. 1:

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JEDEC Standard No. 21-C is the subject of the request, which part of JEDEC Standard No. 21-C is the subject of the request, and the terms "mode register," "to determine CAS latency," and "programming." Rambus further objects to this request on the

grounds that it is compound.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Section 3.11.5.1.3 of certain versions of JEDEC Standard No. 21-C did or does purport to relate, *inter alia*, to certain SDRAM devices and shows a representation of a "Mode Register" that is "located on the Synchronous DRAM (SDRAM or SGRAM) chip." Rambus further admits that Section 3.11.5.1.3 states that the purpose of the "Mode Register" is "to store the mode-of-operation data," that this data contains, *inter alia*, "the /CAS Latency," and that "[d]uring operation, this register (and therefore operation of the chip) may be changed." Rambus further admits that these versions of JEDEC Standard No. 21-C do not state that these features are optional.

Rambus otherwise denies the request.

REQUEST FOR ADMISSION NO. 2:

Admit that, to comply with JEDEC Standard No. 21-C, a DDR SDRAM device must contain a mode register to store a value to determine CAS latency, where that value can be changed by programming the mode register.

RESPONSE TO REQUEST FOR ADMISSION NO. 2:

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JEDEC Standard No. 21-C is the subject of the request, which part of JEDEC Standard No. 21-C is the subject of the request, and the terms "mode register," "to determine CAS latency," and "programming." Rambus further objects to this request on the grounds that it is compound.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Section 3.11.5.1.3 of certain versions of JEDEC Standard No. 21-C did or does purport to relate, *inter alia*, to certain DDR SDRAM devices and shows a representation of a "Mode Register" that is "located on the Synchronous DRAM (SDRAM or SGRAM) chip." Rambus further admits that Section 3.11.5.1.3 states that the purpose of the

"Mode Register" is "to store the mode-of-operation data," that this data contains, *inter alia*, "the /CAS Latency," and that "[d]uring operation, this register (and therefore operation of the chip) may be changed." Rambus further admits that these versions of JEDEC Standard No. 21-C do not state that these features are optional.

Rambus otherwise denies the request.

REQUEST FOR ADMISSION NO. 3:

Admit that, to comply with JEDEC Standard No. 21-C, an SDRAM device must contain a mode register to store a value to determine burst length, where that value can be changed by programming the mode register.

RESPONSE TO REQUEST FOR ADMISSION NO. 3:

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JEDEC Standard No. 21-C is the subject of the request, which part of JEDEC Standard No. 21-C is the subject of the request, and the terms "mode register," "to determine burst length," and "programming." Rambus further objects to this request on the grounds that it is compound.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Section 3.11.5.1.3 of certain versions of JEDEC Standard No. 21-C did or does purport to relate, *inter alia*, to certain SDRAM devices and shows a representation of a "Mode Register" that is "located on the Synchronous DRAM (SDRAM or SGRAM) chip." Rambus further admits that Section 3.11.5.1.3 states that the purpose of the "Mode Register" is "to store the mode-of-operation data," that this data contains, *inter alia*, "the Burst Length," and that "[d]uring operation, this register (and therefore operation of the chip) may be changed." Rambus further admits that these versions of JEDEC Standard No. 21-C do not state that these features are optional.

Rambus otherwise denies the request.

REQUEST FOR ADMISSION NO. 4:

Admit that, to comply with JEDEC Standard No. 21-C, a DDR SDRAM device must contain a mode register to store a value to determine burst length, where that value can be changed by programming the mode register.

RESPONSE TO REQUEST FOR ADMISSION NO. 4:

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JEDEC Standard No. 21-C is the subject of the request, which part of JEDEC Standard No. 21-C is the subject of the request, and the terms "mode register," "to determine burst length," and "programming." Rambus further objects to this request on the grounds that it is compound.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Section 3.11.5.1.3 of certain versions of JEDEC Standard No. 21-C did or does purport to relate, *inter alia*, to certain DDR SDRAM devices and shows a representation of a "Mode Register" that is "located on the Synchronous DRAM (SDRAM or SGRAM) chip." Rambus further admits that Section 3.11.5.1.3 states that the purpose of the "Mode Register" is "to store the mode-of-operation data," that this data contains, *inter alia*, "the Burst Length," and that "[d]uring operation, this register (and therefore operation of the chip) may be changed." Rambus further admits that these versions of JEDEC Standard No. 21-C do not state that these features are optional.

Rambus otherwise denies the request.

REQUEST FOR ADMISSION NO. 5:

Admit that, to comply with JEDEC Standard No. 21-C, an SDRAM device must contain a mode register to store a value to determine block size, where that value can be changed by programming the mode register.

RESPONSE TO REQUEST FOR ADMISSION NO. 5:

Rambus objects to this request on the grounds that it is vague and ambiguous, at least

with respect to which version of JEDEC Standard No. 21-C is the subject of the request, which part of JEDEC Standard No. 21-C is the subject of the request, and the terms "mode register," "to determine block size," and "programming." Rambus further objects to this request on the grounds that it is compound.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Section 3.11.5.1.3 of certain versions of JEDEC Standard No. 21-C did or does purport to relate, *inter alia*, to certain SDRAM devices and shows a representation of a "Mode Register" that is "located on the Synchronous DRAM (SDRAM or SGRAM) chip." Rambus further admits that Section 3.11.5.1.3 states that the purpose of the "Mode Register" is "to store the mode-of-operation data," that this data contains, *inter alia*, "the Burst Length," and that "[d]uring operation, this register (and therefore operation of the chip) may be changed." Rambus further admits that these versions of JEDEC Standard No. 21-C do not state that these features are optional.

Rambus otherwise denies the request.

REQUEST FOR ADMISSION NO. 6:

Admit that, to comply with JEDEC Standard No. 21-C, a DDR SDRAM device must contain a mode register to store a value to determine block size, where that value can be changed by programming the mode register.

RESPONSE TO REQUEST FOR ADMISSION NO. 6:

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JEDEC Standard No. 21-C is the subject of the request, which part of JEDEC Standard No. 21-C is the subject of the request, and the terms "mode register," "to determine block size," and "programming." Rambus further objects to this request on the grounds that it is compound.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Section 3.11.5.1.3 of certain versions of JEDEC Standard No. 21-C

did or does purport to relate, *inter alia*, to certain DDR SDRAM devices and shows a representation of a "Mode Register" that is "located on the Synchronous DRAM (SDRAM or SGRAM) chip." Rambus further admits that Section 3.11.5.1.3 states that the purpose of the "Mode Register" is "to store the mode-of-operation data," that this data contains, *inter alia*, "the Burst Length," and that "[d]uring operation, this register (and therefore operation of the chip) may be changed." Rambus further admits that these versions of JEDEC Standard No. 21-C do not state that these features are optional.

Rambus otherwise denies the request.

REQUEST FOR ADMISSION NO. 25:

Admit that, to comply with JEDEC Standard No. 21-C, an SDRAM device must contain a mode register as described in section 3.11.5.3 (page 3.11.5 –8) of Release 4.

RESPONSE TO REQUEST FOR ADMISSION NO. 25:

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JEDEC Standard No. 21-C is the subject of the request, which part of JEDEC Standard No. 21-C is the subject of the request.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Section 3.11.5.3 of JEDEC Standard No. 21-C, Release 4, did purport to relate, *inter alia*, to certain SDRAM devices and shows a representation of a "Mode Register" that is "located on the Synchronous DRAM (SDRAM) chip." Rambus further admits that JEDEC Standard No. 21-C, Release 4, does not state that this feature is optional.

Rambus otherwise denies the request.

REQUEST FOR ADMISSION NO. 26:

Admit that, to comply with JEDEC Standard No. 21-C, an SDRAM device must contain a mode register as described in section 3.11.5.1.3 of Release 9.

RESPONSE TO REQUEST FOR ADMISSION NO. 26:

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JEDEC Standard No. 21-C is the subject of the request, which part of JEDEC Standard No. 21-C is the subject of the request.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Section 3.11.5.1.3 of JEDEC Standard No. 21-C, Release 9, did purport to relate, *inter alia*, to certain SDRAM devices and shows a representation of a "Mode Register" that is "located on the Synchronous DRAM (SDRAM or SGRAM) chip." Rambus further admits that JEDEC Standard No. 21-C, Release 9, does not state that this feature is optional.

Rambus otherwise denies the request.

REQUEST FOR ADMISSION NO. 44:

Admit that, to comply with the JEDEC Double Data Rate (DDR) SDRAM Specification, JESD79, a DDR SDRAM device must contain a mode register to store a value to determine CAS latency, where that value can be changed by programming the mode register.

RESPONSE TO REQUEST FOR ADMISSION NO. 44:

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JESD79 is the subject of the request and the terms "mode register," "to determine CAS latency" and "programming." Rambus further objects to this request on the grounds that it is compound.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that JESD79, Release 1, purports to relate to certain DDR SDRAM devices. Rambus further admits that JESD79, Release 1, states in part:

"The Mode Register is used to define the specific mode of operation of the DDR SDRAM. This definition includes the selection of . . . a CAS latency . . . . The Mode Register is programmed via the MODE REGISTER SET command . . . and will retain the stored

information until it is programmed again or the device loses power (except for bit A8, which is self-clearing).

"Mode Register bits . . . A4-A6 specify the CAS latency . . . . "

Rambus further admits that JESD79, Release 1, does not state that these features are optional.

Rambus otherwise denies the request.

REQUEST FOR ADMISSION NO. 45:

Admit that, to comply with the JEDEC Double Data Rate (DDR) SDRAM Specification, JESD79, a DDR SDRAM device must contain a mode register to store a value to determine burst length, where that value can be changed by programming the mode register.

RESPONSE TO REQUEST FOR ADMISSION NO. 45:

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JESD79 is the subject of the request and the terms "mode register," "to determine burst length" and "programming." Rambus further objects to this request on the grounds that it is compound.

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that JESD79, Release 1, purports to relate to certain DDR SDRAM devices. Rambus further admits that JESD79, Release 1, states in part:

"The Mode Register is used to define the specific mode of operation of the DDR SDRAM. This definition includes the selection of a burst length . . . . The Mode Register is programmed via the MODE REGISTER SET command . . . and will retain the stored information until it is programmed again or the device loses power (except for bit A8, which is self-clearing).

"Mode Register bits A0-A2 specify the burst length . . . . "

Rambus further admits that JESD79, Release 1, does not state that these features are optional.

Rambus otherwise denies the request.

REQUEST FOR ADMISSION NO. 63:

Admit that, to comply with JEDEC Standard No. 21-C, an SDRAM device must be able to respond to information sent along with a read request instructing it to automatically precharge bank(s) after each read request.

RESPONSE TO REQUEST FOR ADMISSION NO. 63:

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JEDEC Standard No. 21-C is the subject of the request, which part of JEDEC Standard No. 21-C is the subject of the request, and the terms "able to respond," "automatically precharge bank(s)," and "after each read request."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Section 3.11.5.1.5 of JEDEC Standard No. 21-C, Release 9, headed "Auto Precharge" did purport to relate to, *inter alia*, certain SDRAM devices and states, in part: "The user may specify that the bank currently being accessed precharge itself as soon as the burst is completed. This is done using the address bit AP during the column address cycle."

Rambus further admits that JEDEC Standard No. 21-C, Release 9, does not state that this feature is optional.

Rambus otherwise denies the request.

REQUEST FOR ADMISSION NO. 64:

Admit that, to comply with JEDEC Standard No. 21-C, an SDRAM device must have the ability to internally precharge a bank without first receiving a separate precharge command.

RESPONSE TO REQUEST FOR ADMISSION NO. 64:

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JEDEC Standard No. 21-C is the subject of the request, which part of JEDEC Standard No. 21-C is the subject of the request, and the terms "internally

precharge a bank" and "separate precharge command."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Section 3.11.5.1.5 of JEDEC Standard No. 21-C, Release 9, headed "Auto Precharge" did purport to relate to, *inter alia*, certain SDRAM devices and states, in part: "The user may specify that the bank currently being accessed precharge itself as soon as the burst is completed. This is done using the address bit AP during the column address cycle."

Rambus further admits that JEDEC Standard No. 21-C, Release 9, does not state that this feature is optional.

Rambus otherwise denies the request.

REQUEST FOR ADMISSION NO. 69:

Admit that, to comply with the JEDEC Double Data Rate (DDR) SDRAM Specification, JESD79, an SDRAM device must contain the auto precharge feature described at page 14.

RESPONSE TO REQUEST FOR ADMISSION NO. 69:

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JESD79 is the subject of the request and the term "SDRAM device."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that JESD79, Release 1, purports to relate to certain DDR SDRAM devices. Rambus further admits that page 8 of JESD79, Release 1, contains a section headed "Auto Precharge" on page 14 which purports to describe an "auto precharge" feature.

Rambus further admits that JESD79, Release 1, does not state that this feature is optional.

Rambus otherwise denies the request.

REQUEST FOR ADMISSION NO. 70:

Admit that, to comply with the JEDEC Double Data Rate (DDR) SDRAM Specification, JESD79, a DDR SDRAM device must permit the user to use A10 to enable auto precharge in

conjunction with a specific read or write command.

RESPONSE TO REQUEST FOR ADMISSION NO. 70:

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JESD79 is the subject of the request and the terms "user," "auto precharge," and "read or write command."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that JESD79, Release 1, purports to relate to certain DDR SDRAM devices. Rambus further admits that page 8 of JESD79, Release 1, contains a section headed "Auto Precharge" on page 14 which states in part:

"AUTO PRECHARGE is a feature which performs the same individual-bank precharge function described above, but without requiring an explicit command. This is accomplished by using A10 to enable AUTO PRECHARGE in conjunction with a specific READ or WRITE command."

Rambus further admits that JESD79, Release 1, does not state that this feature is optional.

Rambus otherwise denies the request.

REQUEST FOR ADMISSION NO. 71:

Admit that, to comply with the JEDEC Double Data Rate (DDR) SDRAM Specification, JESD79, a DDR SDRAM device must permit the user to perform automatically, upon completion of the read or write burst, a precharge of the bank/row that is addressed with the read or write command.

RESPONSE TO REQUEST FOR ADMISSION NO. 71:

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which version of JESD79 is the subject of the request and the terms "user," "automatically," "bank/row," "the read or write burst," and "the read or write command."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that JESD79, Release 1, purports to relate to certain DDR SDRAM

devices. Rambus further admits that page 8 of JESD79, Release 1, contains a section headed "Auto Precharge" on page 14 which states in part:

"AUTO PRECHARGE is a feature which performs the same individual-bank precharge function described above, but without requiring an explicit command. This is accomplished by using A10 to enable AUTO PRECHARGE in conjunction with a specific READ or WRITE command. A precharge of the bank/row that is addressed with the READ or WRITE command is automatically performed upon completion of the READ or WRITE burst."

Rambus further admits that JESD79, Release 1, does not state that this feature is optional.

Rambus otherwise denies the request.

REQUEST FOR ADMISSION NO. 114:

Admit that, to comply with JEDEC Standard No. 21-C, Release 9, a DDR SDRAM device must contain an extended mode register definition containing a DLL enable/disable bit.

RESPONSE TO REQUEST FOR ADMISSION NO. 114:

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which part of JEDEC Standard No. 21-C is the subject of the request and the terms "extended mode register definition" and "DLL enable/disable bit."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Section 3.11.5.2.11 of JEDEC Standard No. 21-C, Release 9, purports to relate, *inter alia*, to certain DDR SDRAM devices. Rambus further admits that that section refers to an extended mode register and purports to define "the DLL disable/enable bit in the Extended Mode Register." Rambus further admits that JEDEC Standard No. 21-C, Release 9, does not state that these features are optional.

Rambus otherwise denies the request.

REQUEST FOR ADMISSION NO. 115:

Admit that, to comply with JEDEC Standard No. 21-C, Release 9, a DDR SDRAM

device must contain a bit in the mode register that operates to enable and disable an on-chip DLL.

RESPONSE TO REQUEST FOR ADMISSION NO. 115:

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which part of JEDEC Standard No. 21-C is the subject of the request and the terms "mode register," "operates," and "on-chip DLL."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Section 3.11.5.2.11 of JEDEC Standard No. 21-C, Release 9, purports to relate, *inter alia*, to certain DDR SDRAM devices. Rambus further admits that this section refers to an extended mode register and purports to define "the DLL disable/enable bit in the Extended Mode Register." The Section indicates that if this bit set to 0 corresponds to "DLL enable," and this bit set to 1 corresponds to "DLL disable." Rambus further admits that JEDEC Standard No. 21-C, Release 9, does not state that these features are optional.

Rambus otherwise denies the request.

REQUEST FOR ADMISSION NO. 116:

Admit that, to comply with JEDEC Standard No. 21-C, Release 9, a DDR SDRAM device must contain an extended mode register definition containing an enable/disable bit for delay locked loop circuitry to generate an internal clock signal using an external clock signal.

RESPONSE TO REQUEST FOR ADMISSION NO. 116:

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which part of JEDEC Standard No. 21-C is the subject of the request and the terms "extended mode register definition," "enable/disable bit," "delay locked loop circuitry" and "generate an internal clock signal using an external clock signal."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Section 3.11.5.2.11 of JEDEC Standard No. 21-C, Release 9, purports to relate, *inter alia*, to certain DDR SDRAM devices. Rambus further admits that this

section refers to an extended mode register and purports to define "the DLL disable/enable bit in the Extended Mode Register." Rambus further admits that JEDEC Standard No. 21-C, Release 9, does not state that these features are optional. Rambus further admits that "DLL" is often used as an acronym for "delay locked loop."

Rambus otherwise denies the request.

REQUEST FOR ADMISSION NO. 117:

Admit that, to comply with JEDEC Standard No. 21-C, Release 9, a DDR SDRAM device must contain a bit in the mode register that operates to enable and disable delay locked loop circuitry to generate an internal clock signal using an external clock signal.

RESPONSE TO REQUEST FOR ADMISSION NO. 117:

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to which part of JEDEC Standard No. 21-C is the subject of the request and the terms "mode register," "operates," "delay locked loop circuitry" and "generate an internal clock signal using an external clock signal."

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that Section 3.11.5.2.11 of JEDEC Standard No. 21-C, Release 9, refers to an extended mode register and purports to define "the DLL disable/enable bit in the Extended Mode Register." Rambus further admits that JEDEC Standard No. 21-C, Release 9, does not state that these features are optional. Rambus further admits that "DLL" is often used as an acronym for "delay locked loop."

Rambus otherwise denies the request.

REQUEST FOR ADMISSION NO. 281:

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus had claims in pending patent applications that, if included in an issued patent, would cover the use of programmable CAS

latency in a non-compatible DRAM device.

RESPONSE TO REQUEST FOR ADMISSION NO. 281:

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "believed," "programmable CAS latency," "cover" and "non-compatible DRAM device." Rambus further objects to this request on the ground that the beliefs of Rambus's directors, officers or employees as to the scope, or potential scope, of Rambus's patents and patent applications are irrelevant to any issue raised by this matter. *See Rambus Inc. v. Infineon Technologies AG*, 318 F.3d 1081, 1104 (Fed. Cir. 2003) ("The JEDEC policy, though vague, does not create a duty premised on subjective beliefs. JEDEC's disclosure duty erects an objective standard. It does not depend on a member's subjective belief that its patents do or do not read on the proposed standard.").

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at various times between December 1991 and June 1996, various directors, officers or employees of Rambus incorrectly assumed that Rambus had claims in pending patent applications that, if included in an issued patent, would be infringed by certain non-compatible DRAM devices. For example, in 1992, Geoffrey Tate assumed that Rambus's pending patent claims would, if issued, be infringed by certain synchronous DRAM products that were being developed outside of JEDEC at that time; however, his assumption was not founded on any review or analysis of the claims. Rambus later attempted to determine the exact claims that would protect Rambus's inventions from competitive use in synchronous DRAMs. Sometime in late 1992 or early 1993, Mr. Tate learned that his assumption about the scope of Rambus's patent protection was incorrect, and that Rambus did not have pending claims that would protect Rambus's inventions from competitive use in synchronous DRAMs.

As another example, Fred Ware reported in a June 1993 email that Rambus's patent counsel had filed claims that were purportedly "directed against SDRAMs." Mr. Ware's statement was not, however, based on a review or analysis of the pending claims in comparison

to an actual product. In fact, the pending claims referenced in Mr. Ware's e-mail as being "directed at SDRAMs" contained limitations that made clear that they were unrelated to SDRAMs.

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus had any claims in pending patent applications that, if included in an issued patent, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

REQUEST FOR ADMISSION NO. 282:

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus could amend pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would cover the use of programmable CAS latency in a non-compatible DRAM device.

RESPONSE TO REQUEST FOR ADMISSION NO. 282:

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "could amend its pending patent applications, or file continuation or divisional applications, to add claims," and the terms "believed," "programmable CAS latency," "cover" and "non-compatible DRAM device." Rambus further objects to this request on the ground that the beliefs of Rambus's directors, officers or employees as to the scope, or potential scope, of Rambus's patents and patent applications are irrelevant to any issue raised by this matter. *See Rambus Inc. v. Infineon Technologies AG*, 318 F.3d 1081, 1104 (Fed. Cir. 2003)

("The JEDEC policy, though vague, does not create a duty premised on subjective beliefs. JEDEC's disclosure duty erects an objective standard. It does not depend on a member's subjective belief that its patents do or do not read on the proposed standard.").

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at various times between December 1991 and June 1996, various directors, officers or employees of Rambus assumed that Rambus could amend its pending patent applications or file continuation or divisional applications to add claims that, if included in an issued patent application, would be infringed by certain non-compatible DRAM devices. For example, in 1992, Geoffrey Tate assumed that pending patent claims in Rambus's continuation and divisional applications would, if issued, be infringed by certain synchronous DRAM products that were being developed outside of JEDEC at that time; however, his assumption was not founded on any review or analysis of the claims. Rambus later attempted to determine the exact claims that would protect Rambus's inventions from competitive use in synchronous DRAMs. Sometime in late 1992 or early 1993, Mr. Tate learned that his assumption about the scope of Rambus's patent protection was incorrect, and that Rambus did not have pending claims that would protect Rambus's inventions from competitive use in synchronous DRAMs.

As another example, Fred Ware reported in a June 1993 email that Rambus's patent counsel had filed claims that were purportedly "directed against SDRAMs." Mr. Ware's statement was not, however, based on an analysis of the pending claims in comparison to an actual product. In fact, the pending claims referenced in Mr. Ware's e-mail as being "directed at SDRAMs" contained limitations that made clear that they were unrelated to SDRAMs.

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus could amend its pending patent applications or file continuation or divisional applications to add valid claims that, if included in an issued patent application, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered

belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

REQUEST FOR ADMISSION NO. 283:

Admit that, at one or more times between December 1991 and June 1996, Rambus attempted to amend pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would cover the use of programmable CAS latency in a non-compatible DRAM device.

RESPONSE TO REQUEST FOR ADMISSION NO. 283:

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "attempted to amend pending patent applications, or file continuation or divisional applications, to add claims" and the terms "programmable CAS latency," "cover" and "non-compatible DRAM device." Rambus further objects to the request as compound. Rambus further objects that the request calls for a legal conclusion. Rambus further objects to this request on the grounds that Rambus is not familiar, and cannot through reasonable inquiry become familiar, with the operation of all non-compatible DRAM devices. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature. Rambus further objects to this request on the ground that the beliefs of Rambus's directors, officers or employees as to the scope, or potential scope, of Rambus's patents and patent applications are irrelevant to any issue raised by this matter. *See Rambus Inc. v. Infineon Technologies AG*, 318 F.3d 1081, 1104 (Fed. Cir. 2003) ("The JEDEC policy, though vague, does not create a duty premised on subjective

beliefs. JEDEC's disclosure duty erects an objective standard. It does not depend on a member's subjective belief that its patents do or do not read on the proposed standard.").

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at one or more times between December 1991 and June 1996, Rambus amended its pending U.S. patent applications, filed continuation applications, and filed divisional applications. Rambus further admits that at various times between December 1991 and June 1996, various directors, officers or employees of Rambus directed Rambus's patent counsel to consider whether claims could be filed that might be infringed by certain non-compatible DRAM devices.

Rambus is not presently aware of any non-compatible devices that would infringe claims that were amended in or added to its U.S. Patent applications between December 1991 and June 1996 if such claims were included in an issued patent, with the exception of MDRAM devices designed by MoSys. By preliminary amendment dated September 6, 1994, Rambus properly added claims in its patent application with serial number 08/222,646 that were fully supported by the specification and that Rambus intended would read on MoSys MDRAM. *See, e.g.*, *Kingsdown Medical Consultants, Ltd. v. Hollister, Inc.*, 863 F.2d 867, 874 (Fed. Cir. 1988), *cert. denied*, 490 U.S. 1067 (1989) ("nor is it in any manner improper to amend or insert claims intended to cover a competitor's product the applicant's attorney has learned about during the prosecution of a patent application"). After the application issued as U.S. Patent No. 5,513,327 and the MoSys device was closely examined, Rambus informed MoSys of Rambus's belief that MoSys was infringing the patent. The parties settled their dispute and no infringement ruling was ultimately obtained.

Rambus otherwise denies the request.

REQUEST FOR ADMISSION NO. 287:

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus had claims in pending patent

applications that, if included in an issued patent, would cover the use of a programmable register to store a value that is representative of a delay time after which the device responds to a read request in a non-compatible DRAM device.

RESPONSE TO REQUEST FOR ADMISSION NO. 287:

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "believed," "programmable register," "representative of a delay time," "responds to a read request," "cover" and "non-compatible DRAM device." Rambus further objects to this request on the ground that the beliefs of Rambus's directors, officers or employees as to the scope, or potential scope, of Rambus's patents and patent applications are irrelevant to any issue raised by this matter. *See Rambus Inc. v. Infineon Technologies AG*, 318 F.3d 1081, 1104 (Fed. Cir. 2003) ("The JEDEC policy, though vague, does not create a duty premised on subjective beliefs. JEDEC's disclosure duty erects an objective standard. It does not depend on a member's subjective belief that its patents do or do not read on the proposed standard.").

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at various times between December 1991 and June 1996, various directors, officers or employees of Rambus incorrectly assumed that Rambus had claims in pending patent applications that, if included in an issued patent, would be infringed by certain non-compatible DRAM devices. For example, in 1992, Geoffrey Tate assumed that Rambus's pending patent claims would, if issued, be infringed by certain synchronous DRAM products that were being developed outside of JEDEC at that time; however, his assumption was not founded on any review or analysis of the claims. Rambus later attempted to determine the exact claims that would protect Rambus's inventions from competitive use in synchronous DRAMs. Sometime in late 1992 or early 1993, Mr. Tate learned that his assumption about the scope of Rambus's patent protection was incorrect, and that Rambus did not have pending claims that would protect Rambus's inventions from competitive use in synchronous DRAMs.

As another example, Fred Ware reported in a June 1993 email that Rambus's patent counsel had filed claims that were purportedly "directed against SDRAMs." Mr. Ware's

statement was not, however, based on a review or analysis of the pending claims in comparison to an actual product. In fact, the pending claims referenced in Mr. Ware's e-mail as being "directed at SDRAMs" contained limitations that made clear that they were unrelated to SDRAMs.

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus had any claims in pending patent applications that, if included in an issued patent, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

REQUEST FOR ADMISSION NO. 290:

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus had claims in pending patent applications that, if included in an issued patent, would be infringed by a non-compatible DRAM device using programmable CAS latency.

RESPONSE TO REQUEST FOR ADMISSION NO. 290:

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "believed," "programmable CAS latency," and "non-compatible DRAM device." Rambus further objects to this request on the ground that the beliefs of Rambus's directors, officers or employees as to the scope, or potential scope, of Rambus's patents and patent applications are irrelevant to any issue raised by this matter. *See Rambus Inc. v. Infineon Technologies AG*, 318 F.3d 1081, 1104 (Fed. Cir. 2003) ("The JEDEC policy, though vague, does not create a duty premised on subjective beliefs. JEDEC's disclosure duty erects an

objective standard. It does not depend on a member's subjective belief that its patents do or do not read on the proposed standard.").

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at various times between December 1991 and June 1996, various directors, officers or employees of Rambus incorrectly assumed that Rambus had claims in pending patent applications that, if included in an issued patent, would be infringed by certain non-compatible DRAM devices. For example, in 1992, Geoffrey Tate assumed that Rambus's pending patent claims would, if issued, be infringed by certain synchronous DRAM products that were being developed outside of JEDEC at that time; however, his assumption was not founded on any review or analysis of the claims. Rambus later attempted to determine the exact claims that would protect Rambus's inventions from competitive use in synchronous DRAMs. Sometime in late 1992 or early 1993, Mr. Tate learned that his assumption about the scope of Rambus's patent protection was incorrect, and that Rambus did not have pending claims that would protect Rambus's inventions from competitive use in synchronous DRAMs.

As another example, Fred Ware reported in a June 1993 email that Rambus's patent counsel had filed claims that were purportedly "directed against SDRAMs." Mr. Ware's statement was not, however, based on a review or analysis of the pending claims in comparison to an actual product. In fact, the pending claims referenced in Mr. Ware's e-mail as being "directed at SDRAMs" contained limitations that made clear that they were unrelated to SDRAMs.

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus had any claims in pending patent applications that, if included in an issued patent, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated

September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

REQUEST FOR ADMISSION NO. 305:

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus had claims in pending patent applications that, if included in an issued patent, would cover the use of programmable burst length in a non-compatible DRAM device.

RESPONSE TO REQUEST FOR ADMISSION NO. 305:

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "believed," "programmable burst length," "cover," and "non-compatible DRAM device." Rambus further objects to this request on the ground that the beliefs of Rambus's directors, officers or employees as to the scope, or potential scope, of Rambus's patents and patent applications are irrelevant to any issue raised by this matter. *See Rambus Inc. v. Infineon Technologies AG*, 318 F.3d 1081, 1104 (Fed. Cir. 2003) ("The JEDEC policy, though vague, does not create a duty premised on subjective beliefs. JEDEC's disclosure duty erects an objective standard. It does not depend on a member's subjective belief that its patents do or do not read on the proposed standard.").

Subject to and without waiving any objections, Rambus responds as follows: Rambus admits that at various times between December 1991 and June 1996, various directors, officers or employees of Rambus incorrectly assumed that Rambus had claims in pending patent applications that, if included in an issued patent, would be infringed by certain non-compatible DRAM devices. For example, in 1992, Geoffrey Tate assumed that Rambus's pending patent claims would, if issued, be infringed by certain synchronous DRAM products that were being developed outside of JEDEC at that time; however, his assumption was not founded on any review or analysis of the claims. Rambus later attempted to determine the exact claims that would protect Rambus's inventions from competitive use in synchronous DRAMs. Sometime in

late 1992 or early 1993, Mr. Tate learned that his assumption about the scope of Rambus's patent protection was incorrect, and that Rambus did not have pending claims that would protect Rambus's inventions from competitive use in synchronous DRAMs.

As another example, Fred Ware reported in a June 1993 email that Rambus's patent counsel had filed claims that were purportedly "directed against SDRAMs." Mr. Ware's statement was not, however, based on a review or analysis of the pending claims in comparison to an actual product. In fact, the pending claims referenced in Mr. Ware's e-mail as being "directed at SDRAMs" contained limitations that made clear that they were unrelated to SDRAMs.

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus had any claims in pending patent applications that, if included in an issued patent, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

REQUEST FOR ADMISSION NO. 306:

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus could amend pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would cover the use of programmable burst length in a non-compatible DRAM device.

RESPONSE TO REQUEST FOR ADMISSION NO. 306:

Rambus objects to this request on the grounds that it is vague and ambiguous, at least

with respect to the phrase "could amend its pending patent applications, or file continuation or divisional applications, to add claims," and the terms "believed," "programmable burst length," "cover," and "non-compatible DRAM device." Rambus further objects to this request on the ground that the beliefs of Rambus's directors, officers or employees as to the scope, or potential scope, of Rambus's patents and patent applications are irrelevant to any issue raised by this matter. *See Rambus Inc. v. Infineon Technologies AG*, 318 F.3d 1081, 1104 (Fed. Cir. 2003) ("The JEDEC policy, though vague, does not create a duty premised on subjective beliefs. JEDEC's disclosure duty erects an objective standard. It does not depend on a member's subjective belief that its patents do or do not read on the proposed standard.").

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at various times between December 1991 and June 1996, various directors, officers or employees of Rambus assumed that Rambus could amend its pending patent applications or file continuation or divisional applications to add claims that, if included in an issued patent application, would be infringed by certain non-compatible DRAM devices. For example, in 1992, Geoffrey Tate assumed that pending patent claims in Rambus's continuation and divisional applications would, if issued, be infringed by certain synchronous DRAM products that were being developed outside of JEDEC at that time; however, his assumption was not founded on any review or analysis of the claims. Rambus later attempted to determine the exact claims that would protect Rambus's inventions from competitive use in synchronous DRAMs. Sometime in late 1992 or early 1993, Mr. Tate learned that his assumption about the scope of Rambus's patent protection was incorrect, and that Rambus did not have pending claims that would protect Rambus's inventions from competitive use in synchronous DRAMs.

As another example, Fred Ware reported in a June 1993 email that Rambus's patent counsel had filed claims that were purportedly "directed against SDRAMs." Mr. Ware's statement was not, however, based on an analysis of the pending claims in comparison to an actual product. In fact, the pending claims referenced in Mr. Ware's e-mail as being "directed at SDRAMs" contained limitations that made clear that they were unrelated to SDRAMs.

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus could amend its pending patent applications or file continuation or divisional applications to add valid claims that, if included in an issued patent application, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

REQUEST FOR ADMISSION NO. 307:

Admit that, at one or more times between December 1991 and June 1996, Rambus attempted to amend pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would cover the use of programmable burst length in a non-compatible DRAM device.

RESPONSE TO REQUEST FOR ADMISSION NO. 307:

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "attempted to amend pending patent applications, or file continuation or divisional applications, to add claims" and the terms "programmable burst length," "cover," and "non-compatible DRAM device." Rambus further objects to the request as compound. Rambus further objects that the request calls for a legal conclusion. Rambus further objects to this request on the grounds that Rambus is not familiar, and cannot through reasonable inquiry become familiar, with the operation of all non-compatible DRAM devices. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the

doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be determined by whether the DRAM device contains a single feature. Rambus further objects to this request on the ground that the beliefs of Rambus's directors, officers or employees as to the scope, or potential scope, of Rambus's patents and patent applications are irrelevant to any issue raised by this matter. *See Rambus Inc. v. Infineon Technologies AG*, 318 F.3d 1081, 1104 (Fed. Cir. 2003) ("The JEDEC policy, though vague, does not create a duty premised on subjective beliefs. JEDEC's disclosure duty erects an objective standard. It does not depend on a member's subjective belief that its patents do or do not read on the proposed standard.").

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at one or more times between December 1991 and June 1996, Rambus amended its pending U.S. patent applications, filed continuation applications, and filed divisional applications. Rambus further admits that at various times between December 1991 and June 1996, various directors, officers or employees of Rambus directed Rambus's patent counsel to consider whether claims could be filed that might be infringed by certain non-compatible DRAM devices.

Rambus is not presently aware of any non-compatible devices that would infringe claims that were amended in or added to its U.S. Patent applications between December 1991 and June 1996 if such claims were included in an issued patent, with the exception of MDRAM devices designed by MoSys. By preliminary amendment dated September 6, 1994, Rambus properly added claims in its patent application with serial number 08/222,646 that were fully supported by the specification and that Rambus intended would read on MoSys MDRAM. *See, e.g., Kingsdown Medical Consultants, Ltd. v. Hollister, Inc.*, 863 F.2d 867, 874 (Fed. Cir. 1988), *cert. denied*, 490 U.S. 1067 (1989) ("nor is it in any manner improper to amend or insert claims intended to cover a competitor's product the applicant's attorney has learned about during the prosecution of a patent application"). After the application issued as U.S. Patent No. 5,513,327 and the MoSys device was closely examined, Rambus informed MoSys of Rambus's belief that MoSys was infringing the patent. The parties settled their dispute and no infringement ruling

was ultimately obtained.

Rambus otherwise denies the request.

REQUEST FOR ADMISSION NO. 317:

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus had claims in pending patent applications that, if included in an issued patent, would be infringed by a non-compatible DRAM device using programmable burst length.

RESPONSE TO REQUEST FOR ADMISSION NO. 317:

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "believed," "programmable burst length" and "non-compatible DRAM device." Rambus further objects to this request on the ground that the beliefs of Rambus's directors, officers or employees as to the scope, or potential scope, of Rambus's patents and patent applications are irrelevant to any issue raised by this matter. *See Rambus Inc. v. Infineon Technologies AG*, 318 F.3d 1081, 1104 (Fed. Cir. 2003) ("The JEDEC policy, though vague, does not create a duty premised on subjective beliefs. JEDEC's disclosure duty erects an objective standard. It does not depend on a member's subjective belief that its patents do or do not read on the proposed standard.").

Subject to and without waiving any objections, Rambus responds as follows: Rambus admits that at various times between December 1991 and June 1996, various directors, officers or employees of Rambus incorrectly assumed that Rambus had claims in pending patent applications that, if included in an issued patent, would be infringed by certain non-compatible DRAM devices. For example, in 1992, Geoffrey Tate assumed that Rambus's pending patent claims would, if issued, be infringed by certain synchronous DRAM products that were being developed outside of JEDEC at that time; however, his assumption was not founded on any review or analysis of the claims. Rambus later attempted to determine the exact claims that would protect Rambus's inventions from competitive use in synchronous DRAMs. Sometime in

late 1992 or early 1993, Mr. Tate learned that his assumption about the scope of Rambus's patent protection was incorrect, and that Rambus did not have pending claims that would protect Rambus's inventions from competitive use in synchronous DRAMs.

As another example, Fred Ware reported in a June 1993 email that Rambus's patent counsel had filed claims that were purportedly "directed against SDRAMs." Mr. Ware's statement was not, however, based on a review or analysis of the pending claims in comparison to an actual product. In fact, the pending claims referenced in Mr. Ware's e-mail as being "directed at SDRAMs" contained limitations that made clear that they were unrelated to SDRAMs.

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus had any claims in pending patent applications that, if included in an issued patent, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

REQUEST FOR ADMISSION NO. 332:

Admit that between December 1991 and June 1996, Rambus, through any one of its directors, officers or employees, believed that it had claims in pending patent applications or issued patents that would cover a synchronous DRAM device that output data on the rising and the falling edge of a clock signal.

RESPONSE TO REQUEST FOR ADMISSION NO. 332:

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "through any one of its directors, officers or employees," "believed,"

"the rising and the falling edge," "a clock signal," "cover," and "synchronous DRAM device." Rambus further objects to this request on the ground that the beliefs of Rambus's directors, officers or employees as to the scope, or potential scope, of Rambus's patents and patent applications are irrelevant to any issue raised by this matter. *See Rambus Inc. v. Infineon Technologies AG*, 318 F.3d 1081, 1104 (Fed. Cir. 2003) ("The JEDEC policy, though vague, does not create a duty premised on subjective beliefs. JEDEC's disclosure duty erects an objective standard. It does not depend on a member's subjective belief that its patents do or do not read on the proposed standard.").

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at various times between December 1991 and June 1996, various directors, officers or employees of Rambus incorrectly assumed that Rambus had claims in pending patent applications that, if included in an issued patent, would be infringed by certain synchronous DRAM devices. For example, in 1992, Geoffrey Tate assumed that Rambus's pending patent claims would, if issued, be infringed by certain synchronous DRAM products that were being developed outside of JEDEC at that time; however, his assumption was not founded on any review or analysis of the claims. Rambus later attempted to determine the exact claims that would protect Rambus's inventions from competitive use in synchronous DRAMs. Sometime in late 1992 or early 1993, Mr. Tate learned that his assumption about the scope of Rambus's patent protection was incorrect, and that Rambus did not have pending claims that would protect Rambus's inventions from competitive use in synchronous DRAMs.

As another example, Fred Ware reported in a June 1993 email that Rambus's patent counsel had filed claims that were purportedly "directed against SDRAMs." Mr. Ware's statement was not, however, based on a review or analysis of the pending claims in comparison to an actual product. In fact, the pending claims referenced in Mr. Ware's e-mail as being "directed at SDRAMs" contained limitations that made clear that they were unrelated to SDRAMs.

Rambus is not aware of any Rambus director, officer or employee who had a reasoned

and considered belief, between December 1991 and June 1996, that Rambus had any claims in pending patent applications that, if included in an issued patent, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

REQUEST FOR ADMISSION NO. 333:

Admit that between December 1991 and June 1996, Rambus, through any one of its directors, officers or employees, believed that it had claims in pending patent applications or issued patents that would cover a synchronous DRAM device that input data on the rising and the falling edge of a clock signal.

RESPONSE TO REQUEST FOR ADMISSION NO. 333:

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "through any one of its directors, officers or employees," "believed," "the rising and the falling edge," "a clock signal," "cover," and "synchronous DRAM device." Rambus further objects to this request on the ground that the beliefs of Rambus's directors, officers or employees as to the scope, or potential scope, of Rambus's patents and patent applications are irrelevant to any issue raised by this matter. *See Rambus Inc. v. Infineon Technologies AG*, 318 F.3d 1081, 1104 (Fed. Cir. 2003) ("The JEDEC policy, though vague, does not create a duty premised on subjective beliefs. JEDEC's disclosure duty erects an objective standard. It does not depend on a member's subjective belief that its patents do or do not read on the proposed standard.").

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at various times between December 1991 and June 1996, various directors, officers or employees of Rambus incorrectly assumed that Rambus had claims in pending patent applications that, if included in an issued patent, would be infringed by certain synchronous DRAM devices. For example, in 1992, Geoffrey Tate assumed that Rambus's pending patent claims would, if issued, be infringed by certain synchronous DRAM products that were being developed outside of JEDEC at that time; however, his assumption was not founded on any review or analysis of the claims. Rambus later attempted to determine the exact claims that would protect Rambus's inventions from competitive use in synchronous DRAMs. Sometime in late 1992 or early 1993, Mr. Tate learned that his assumption about the scope of Rambus's patent protection was incorrect, and that Rambus did not have pending claims that would protect Rambus's inventions from competitive use in synchronous DRAMs.

As another example, Fred Ware reported in a June 1993 email that Rambus's patent counsel had filed claims that were purportedly "directed against SDRAMs." Mr. Ware's statement was not, however, based on a review or analysis of the pending claims in comparison to an actual product. In fact, the pending claims referenced in Mr. Ware's e-mail as being "directed at SDRAMs" contained limitations that made clear that they were unrelated to SDRAMs.

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus had any claims in pending patent applications that, if included in an issued patent, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

REQUEST FOR ADMISSION NO. 334:

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus had claims in pending patent applications that, if included in an issued patent, would cover the output a first portion of data in response to a rising edge of a clock signal and a second portion of data in response to a falling edge of a clock signal in a non-compatible DRAM device.

RESPONSE TO REQUEST FOR ADMISSION NO. 334:

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "believed," "first portion of data," "second portion of data," "in response to," "a clock signal," "cover," and "non-compatible DRAM device." Rambus further objects to this request on the ground that the beliefs of Rambus's directors, officers or employees as to the scope, or potential scope, of Rambus's patents and patent applications are irrelevant to any issue raised by this matter. *See Rambus Inc. v. Infineon Technologies AG*, 318 F.3d 1081, 1104 (Fed. Cir. 2003) ("The JEDEC policy, though vague, does not create a duty premised on subjective beliefs. JEDEC's disclosure duty erects an objective standard. It does not depend on a member's subjective belief that its patents do or do not read on the proposed standard.").

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at various times between December 1991 and June 1996, various directors, officers or employees of Rambus incorrectly assumed that Rambus had claims in pending patent applications that, if included in an issued patent, would be infringed by certain non-compatible DRAM devices. For example, in 1992, Geoffrey Tate assumed that Rambus's pending patent claims would, if issued, be infringed by certain synchronous DRAM products that were being developed outside of JEDEC at that time; however, his assumption was not founded on any review or analysis of the claims. Rambus later attempted to determine the exact claims that would protect Rambus's inventions from competitive use in synchronous DRAMs. Sometime in late 1992 or early 1993, Mr. Tate learned that his assumption about the scope of

Rambus's patent protection was incorrect, and that Rambus did not have pending claims that would protect Rambus's inventions from competitive use in synchronous DRAMs.

As another example, Fred Ware reported in a June 1993 email that Rambus's patent counsel had filed claims that were purportedly "directed against SDRAMs." Mr. Ware's statement was not, however, based on a review or analysis of the pending claims in comparison to an actual product. In fact, the pending claims referenced in Mr. Ware's e-mail as being "directed at SDRAMs" contained limitations that made clear that they were unrelated to SDRAMs.

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus had any claims in pending patent applications that, if included in an issued patent, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

REQUEST FOR ADMISSION NO. 335:

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus could amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would cover the output a first portion of data in response to a rising edge of a clock signal and a second portion of data in response to a falling edge of a clock signal in a non-compatible DRAM device.

RESPONSE TO REQUEST FOR ADMISSION NO. 335:

Rambus objects to this request on the grounds that it is vague and ambiguous, at least

with respect to the phrase "could amend its pending patent applications, or file continuation or divisional applications, to add claims," and the terms "believed," "first portion of data," "second portion of data," "in response to," "a clock signal," "cover," and "non-compatible DRAM device." Rambus further objects to this request on the ground that the beliefs of Rambus's directors, officers or employees as to the scope, or potential scope, of Rambus's patents and patent applications are irrelevant to any issue raised by this matter. *See Rambus Inc. v. Infineon Technologies AG*, 318 F.3d 1081, 1104 (Fed. Cir. 2003) ("The JEDEC policy, though vague, does not create a duty premised on subjective beliefs. JEDEC's disclosure duty erects an objective standard. It does not depend on a member's subjective belief that its patents do or do not read on the proposed standard.").

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at various times between December 1991 and June 1996, various directors, officers or employees of Rambus assumed that Rambus could amend its pending patent applications or file continuation or divisional applications to add claims that, if included in an issued patent application, would be infringed by certain non-compatible DRAM devices. For example, in 1992, Geoffrey Tate assumed that pending patent claims in Rambus's continuation and divisional applications would, if issued, be infringed by certain synchronous DRAM products that were being developed outside of JEDEC at that time; however, his assumption was not founded on any review or analysis of the claims. Rambus later attempted to determine the exact claims that would protect Rambus's inventions from competitive use in synchronous DRAMs. Sometime in late 1992 or early 1993, Mr. Tate learned that his assumption about the scope of Rambus's patent protection was incorrect, and that Rambus did not have pending claims that would protect Rambus's inventions from competitive use in synchronous DRAMs.

As another example, Fred Ware reported in a June 1993 email that Rambus's patent counsel had filed claims that were purportedly "directed against SDRAMs." Mr. Ware's statement was not, however, based on an analysis of the pending claims in comparison to an actual product. In fact, the pending claims referenced in Mr. Ware's e-mail as being "directed at

SDRAMs" contained limitations that made clear that they were unrelated to SDRAMs.

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus could amend its pending patent applications or file continuation or divisional applications to add valid claims that, if included in an issued patent application, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

REQUEST FOR ADMISSION NO. 370:

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus had claims in pending patent applications that, if included in an issued patent, would be infringed by a non-compatible DRAM device that output a first portion of data in response to a rising edge of a clock signal and a second portion of data in response to a falling edge of a clock signal.

RESPONSE TO REQUEST FOR ADMISSION NO. 370:

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "believed," "first portion of data," "second portion of data," "in response to," "a clock signal," and "non-compatible DRAM device." Rambus further objects to this request on the ground that the beliefs of Rambus's directors, officers or employees as to the scope, or potential scope, of Rambus's patents and patent applications are irrelevant to any issue raised by this matter. *See Rambus Inc. v. Infineon Technologies AG*, 318 F.3d 1081, 1104 (Fed. Cir. 2003) ("The JEDEC policy, though vague, does not create a duty premised on subjective beliefs. JEDEC's disclosure duty erects an objective standard. It does not depend on a

member's subjective belief that its patents do or do not read on the proposed standard.").

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at various times between December 1991 and June 1996, various directors, officers or employees of Rambus incorrectly assumed that Rambus had claims in pending patent applications that, if included in an issued patent, would be infringed by certain non-compatible DRAM devices. For example, in 1992, Geoffrey Tate assumed that Rambus's pending patent claims would, if issued, be infringed by certain synchronous DRAM products that were being developed outside of JEDEC at that time; however, his assumption was not founded on any review or analysis of the claims. Rambus later attempted to determine the exact claims that would protect Rambus's inventions from competitive use in synchronous DRAMs. Sometime in late 1992 or early 1993, Mr. Tate learned that his assumption about the scope of Rambus's patent protection was incorrect, and that Rambus did not have pending claims that would protect Rambus's inventions from competitive use in synchronous DRAMs.

As another example, Fred Ware reported in a June 1993 email that Rambus's patent counsel had filed claims that were purportedly "directed against SDRAMs." Mr. Ware's statement was not, however, based on a review or analysis of the pending claims in comparison to an actual product. In fact, the pending claims referenced in Mr. Ware's e-mail as being "directed at SDRAMs" contained limitations that made clear that they were unrelated to SDRAMs.

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus had any claims in pending patent applications that, if included in an issued patent, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

REQUEST FOR ADMISSION NO. 406:

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus had claims in pending patent applications that, if included in an issued patent, would cover on-chip PLL or on-chip DLL circuitry in a non-compatible DRAM device.

RESPONSE TO REQUEST FOR ADMISSION NO. 406:

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the terms "believed," "on-chip PLL" "on-chip DLL" "cover," and "non-compatible DRAM device." Rambus further objects to this request on the ground that the beliefs of Rambus's directors, officers or employees as to the scope, or potential scope, of Rambus's patents and patent applications are irrelevant to any issue raised by this matter. *See Rambus Inc. v. Infineon Technologies AG*, 318 F.3d 1081, 1104 (Fed. Cir. 2003) ("The JEDEC policy, though vague, does not create a duty premised on subjective beliefs. JEDEC's disclosure duty erects an objective standard. It does not depend on a member's subjective belief that its patents do or do not read on the proposed standard.").

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at various times between December 1991 and June 1996, various directors, officers or employees of Rambus incorrectly assumed that Rambus had claims in pending patent applications that, if included in an issued patent, would be infringed by certain non-compatible DRAM devices. For example, in 1992, Geoffrey Tate assumed that Rambus's pending patent claims would, if issued, be infringed by certain synchronous DRAM products that were being developed outside of JEDEC at that time; however, his assumption was not founded on any review or analysis of the claims. Rambus later attempted to determine the exact claims that would protect Rambus's inventions from competitive use in synchronous DRAMs. Sometime in late 1992 or early 1993, Mr. Tate learned that his assumption about the scope of

Rambus's patent protection was incorrect, and that Rambus did not have pending claims that would protect Rambus's inventions from competitive use in synchronous DRAMs.

As another example, Fred Ware reported in a June 1993 email that Rambus's patent counsel had filed claims that were purportedly "directed against SDRAMs." Mr. Ware's statement was not, however, based on a review or analysis of the pending claims in comparison to an actual product. In fact, the pending claims referenced in Mr. Ware's e-mail as being "directed at SDRAMs" contained limitations that made clear that they were unrelated to SDRAMs.

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus had any claims in pending patent applications that, if included in an issued patent, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

REQUEST FOR ADMISSION NO. 407:

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus could amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would cover on-chip PLL or on-chip DLL circuitry in a non-compatible DRAM device.

RESPONSE TO REQUEST FOR ADMISSION NO. 407:

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "could amend its pending patent applications, or file continuation or

divisional applications, to add claims," and the terms "believed," "on-chip PLL" "on-chip DLL" "cover," and "non-compatible DRAM device." Rambus further objects to this request on the ground that the beliefs of Rambus's directors, officers or employees as to the scope, or potential scope, of Rambus's patents and patent applications are irrelevant to any issue raised by this matter. *See Rambus Inc. v. Infineon Technologies AG*, 318 F.3d 1081, 1104 (Fed. Cir. 2003) ("The JEDEC policy, though vague, does not create a duty premised on subjective beliefs. JEDEC's disclosure duty erects an objective standard. It does not depend on a member's subjective belief that its patents do or do not read on the proposed standard.").

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at various times between December 1991 and June 1996, various directors, officers or employees of Rambus assumed that Rambus could amend its pending patent applications or file continuation or divisional applications to add claims that, if included in an issued patent application, would be infringed by certain non-compatible DRAM devices. For example, in 1992, Geoffrey Tate assumed that pending patent claims in Rambus's continuation and divisional applications would, if issued, be infringed by certain synchronous DRAM products that were being developed outside of JEDEC at that time; however, his assumption was not founded on any review or analysis of the claims. Rambus later attempted to determine the exact claims that would protect Rambus's inventions from competitive use in synchronous DRAMs. Sometime in late 1992 or early 1993, Mr. Tate learned that his assumption about the scope of Rambus's patent protection was incorrect, and that Rambus did not have pending claims that would protect Rambus's inventions from competitive use in synchronous DRAMs.

As another example, Fred Ware reported in a June 1993 email that Rambus's patent counsel had filed claims that were purportedly "directed against SDRAMs." Mr. Ware's statement was not, however, based on an analysis of the pending claims in comparison to an actual product. In fact, the pending claims referenced in Mr. Ware's e-mail as being "directed at SDRAMs" contained limitations that made clear that they were unrelated to SDRAMs.

Rambus is not aware of any Rambus director, officer or employee who had a reasoned

and considered belief, between December 1991 and June 1996, that Rambus could amend its pending patent applications or file continuation or divisional applications to add valid claims that, if included in an issued patent application, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

REQUEST FOR ADMISSION NO. 408:

Admit that, at various times between December 1991 and June 1996, Rambus attempted to amend pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would cover on-chip PLL or on-chip DLL circuitry in a non-compatible DRAM device.

RESPONSE TO REQUEST FOR ADMISSION NO. 408:

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "attempted to amend pending patent applications, or file continuation or divisional applications, to add claims" and the terms "on-chip PLL" "on-chip DLL" "cover," and "non-compatible DRAM device." Rambus further objects to the request as compound. Rambus further objects that the request calls for a legal conclusion. Rambus further objects to this request on the grounds that Rambus is not familiar, and cannot through reasonable inquiry become familiar, with the operation of all non-compatible DRAM devices. Rambus further objects that, to the extent that "cover" is to be interpreted as "infringed by," whether any particular claim is, in fact, infringed by any given DRAM device will depend on whether the DRAM device contains each and every limitation of the claim, either literally or under the doctrine of equivalents, as those limitations are ultimately construed by the courts, and cannot be

determined by whether the DRAM device contains a single feature. Rambus further objects to this request on the ground that the beliefs of Rambus's directors, officers or employees as to the scope, or potential scope, of Rambus's patents and patent applications are irrelevant to any issue raised by this matter. *See Rambus Inc. v. Infineon Technologies AG*, 318 F.3d 1081, 1104 (Fed. Cir. 2003) ("The JEDEC policy, though vague, does not create a duty premised on subjective beliefs. JEDEC's disclosure duty erects an objective standard. It does not depend on a member's subjective belief that its patents do or do not read on the proposed standard.").

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at one or more times between December 1991 and June 1996, Rambus amended its pending U.S. patent applications, filed continuation applications, and filed divisional applications. Rambus further admits that at various times between December 1991 and June 1996, various directors, officers or employees of Rambus directed Rambus's patent counsel to consider whether claims could be filed that might be infringed by certain non-compatible DRAM devices.

Rambus is not presently aware of any non-compatible devices that would infringe claims that were amended in or added to its U.S. Patent applications between December 1991 and June 1996 if such claims were included in an issued patent, with the exception of MDRAM devices designed by MoSys. By preliminary amendment dated September 6, 1994, Rambus properly added claims in its patent application with serial number 08/222,646 that were fully supported by the specification and that Rambus intended would read on MoSys MDRAM. *See, e.g.*, *Kingsdown Medical Consultants, Ltd. v. Hollister, Inc.*, 863 F.2d 867, 874 (Fed. Cir. 1988), *cert. denied*, 490 U.S. 1067 (1989) ("nor is it in any manner improper to amend or insert claims intended to cover a competitor's product the applicant's attorney has learned about during the prosecution of a patent application"). After the application issued as U.S. Patent No. 5,513,327 and the MoSys device was closely examined, Rambus informed MoSys of Rambus's belief that MoSys was infringing the patent. The parties settled their dispute and no infringement ruling was ultimately obtained.

Rambus otherwise denies the request.

REQUEST FOR ADMISSION NO. 452:

Admit that, at various times between December 1991 and June 1996, various directors, officers or employees of Rambus believed that Rambus could amend its pending patent applications, or file continuation or divisional applications, to add claims that, if included in an issued patent, would be infringed by a non-compatible DRAM device using a PLL.

RESPONSE TO REQUEST FOR ADMISSION NO. 452:

Rambus objects to this request on the grounds that it is vague and ambiguous, at least with respect to the phrase "could amend its pending patent applications, or file continuation or divisional applications, to add claims," and the terms "believed," "using a PLL" and "non-compatible DRAM device." Rambus further objects to this request on the ground that the beliefs of Rambus's directors, officers or employees as to the scope, or potential scope, of Rambus's patents and patent applications are irrelevant to any issue raised by this matter. *See Rambus Inc. v. Infineon Technologies AG*, 318 F.3d 1081, 1104 (Fed. Cir. 2003) ("The JEDEC policy, though vague, does not create a duty premised on subjective beliefs. JEDEC's disclosure duty erects an objective standard. It does not depend on a member's subjective belief that its patents do or do not read on the proposed standard.").

Subject to and without waiving any objections, Rambus responds as follows:

Rambus admits that at various times between December 1991 and June 1996, various directors, officers or employees of Rambus assumed that Rambus could amend its pending patent applications or file continuation or divisional applications to add claims that, if included in an issued patent application, would be infringed by certain non-compatible DRAM devices. For example, in 1992, Geoffrey Tate assumed that pending patent claims in Rambus's continuation and divisional applications would, if issued, be infringed by certain synchronous DRAM products that were being developed outside of JEDEC at that time; however, his assumption was not founded on any review or analysis of the claims. Rambus later attempted to determine the

exact claims that would protect Rambus's inventions from competitive use in synchronous DRAMs. Sometime in late 1992 or early 1993, Mr. Tate learned that his assumption about the scope of Rambus's patent protection was incorrect, and that Rambus did not have pending claims that would protect Rambus's inventions from competitive use in synchronous DRAMs.

As another example, Fred Ware reported in a June 1993 email that Rambus's patent counsel had filed claims that were purportedly "directed against SDRAMs." Mr. Ware's statement was not, however, based on an analysis of the pending claims in comparison to an actual product. In fact, the pending claims referenced in Mr. Ware's e-mail as being "directed at SDRAMs" contained limitations that made clear that they were unrelated to SDRAMs.

Rambus is not aware of any Rambus director, officer or employee who had a reasoned and considered belief, between December 1991 and June 1996, that Rambus could amend its pending patent applications or file continuation or divisional applications to add valid claims that, if included in an issued patent application, would be infringed by non-compatible DRAM devices existing during that period, with the exception of MDRAM devices designed by MoSys. Various directors, officers and employees of Rambus did come to a reasoned and considered belief that MoSys MDRAM devices might infringe claims added to the Rambus patent application with serial number 08/222,646 by preliminary amendment dated September 6, 1994 and as further amended, if those claims were included in an issued patent.

Rambus otherwise denies the request.

REQUEST FOR ADMISSION NO. 651:

Admit that Rambus's ability to increase the price that its licensees must pay to incorporate some technologies into synchronous DRAM, over what those licensees were paying prior to their license with Rambus, is the result of patents claiming priority back to the '898 patent application filed by Rambus in April of 1990.

RESPONSE TO REQUEST FOR ADMISSION NO. 651:

Rambus incorporates its response to Request No. 650 and otherwise denies this request,

except that Rambus admits that Rambus licensees were not paying any licensing fees to Rambus prior to entering into license agreements with Rambus, but did begin paying licensing fees to Rambus after entering into license agreements, and that a portion of the licensing fee paid by certain Rambus licensees for the use of Rambus intellectual property in SDRAMs and DDR SDRAMs results from licensing rights to patents that claim priority back to Rambus's '898 patent application, which was filed in April of 1990.

REQUEST FOR ADMISSION NO. 652:

Admit that Rambus has been able to increase the price that its licensees must pay to incorporate programmable CAS latency into synchronous DRAM, over what those licensees were paying prior to their license with Rambus.

RESPONSE TO REQUEST FOR ADMISSION NO. 652:

Rambus objects to this request as vague and ambiguous at least with respect to the terms "the price that its licensees must pay to incorporate programmable CAS latency," "programmable CAS latency," "synchronous DRAM," and "what those licensees were paying prior to their license with Rambus." The request is also unintelligible. For example, the phrase "the price that its licensees must pay to incorporate programmable CAS latency" could refer to licensing fees paid to Rambus. This interpretation renders the request unintelligible, however, because the request later compares this "price" to "what those licensees were paying prior to their license with Rambus" and therefore, apparently, cannot refer to licensing fees. Rambus does admit that its licensees were not paying any licensing fees to Rambus prior to entering into license agreements with Rambus, but did begin paying licensing fees to Rambus after entering into license agreements. To the extent "the price that its licensees must pay to incorporate programmable CAS latency" is meant to refer to design, implementation, or manufacturing costs, there is no reason to believe an increase in such costs would be related to a change in status due to entering into a license with Rambus. To the contrary, the cost of incorporation of certain technology could be reduced due to the transfer of Rambus know-how. In any event, to

the extent that the request is referring to design, implementation, or manufacturing costs, Rambus does not possess, and would be unable to obtain after reasonable inquiry, data concerning DRAM manufacturers' costs before and after some of those manufacturers began paying a licensing fee to Rambus that would be sufficient for Rambus to admit or deny the request.

REQUEST FOR ADMISSION NO. 653:

Admit that Rambus's ability to increase the price that its licensees must pay to incorporate programmable CAS latency into synchronous DRAM, over what those licensees were paying prior to their license with Rambus, is the result of patents claiming priority back to the '898 patent application filed by Rambus in April of 1990.

RESPONSE TO REQUEST FOR ADMISSION NO. 653:

Rambus incorporates its response to Request No. 652 and otherwise denies this request, except that Rambus admits that Rambus licensees were not paying any licensing fees to Rambus prior to entering into license agreements with Rambus, but did begin paying licensing fees to Rambus after entering into license agreements, and that a portion of the licensing fee paid by certain Rambus licensees for the use of Rambus intellectual property in SDRAMs and DDR SDRAMs results from licensing rights to patents that claim priority back to Rambus's '898 patent application, which was filed in April of 1990.

DATED: March 12, 2003

Respectfully submitted,

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