UNITED STATES OF AMERICA
BEFORE THE FEDERAL TRADE COMMISSION

In the Matter of **RAMBUS INC.,** **a corporation.**	**Docket No. 9302**

RULE 3.22(f) DECLARATION OF STEVEN M. PERRY IN SUPPORT OF RAMBUS INC.'S MOTION TO COMPEL NEC ELECTRONICS, INC. TO PRODUCE DOCUMENTS IN ITS PARENT COMPANY'S POSSESSION RESPONSIVE TO THE SUBPOENA SERVED BY RAMBUS INC.

I, Steven M. Perry, declare:

1. I am a member of the State Bar of California and a member of the law firm of Munger, Tolles & Olson LLP, co-counsel for respondent Rambus Inc. ("Rambus") in this matter. I submit this declaration in support of Rambus Inc.'s Motion To Compel NEC Electronics, Inc. To Produce Documents In Its Parent Company's Possession Responsive To The Subpoena Served By Rambus Inc. I have personal knowledge of the facts set forth in this declaration. I make this Declaration pursuant to Rule 3.22(f) of the Rules of Practice.

2. On September 9, 2002, Rambus served a subpoena duces tecum on NEC Electronics, Inc. ("NEC USA") that required, among other things, that NEC USA produce responsive documents that were in the possession of its corporate parent, NEC Corporation. On September 23, 2002, NEC USA served objections to Rambus's

subpoena and objected in particular to the requirement that it produce documents from its parent company's files. At about the same time, Mitsubishi Electric & Electronics USA, Inc. ("Mitsubishi") filed a motion to quash that raised the same issue. Rambus's subpoenas to Mitsubishi and to NEC USA involved the same basic document categories and subject matters.

3. On November 12, 2002, Your Honor denied Mitsubishi's motion to quash and ordered Mitsubishi to comply with Rambus's subpoena within ten days (*i.e.*, by November 22, 2002). Among other things, Your Honor ordered Mitsubishi to produce responsive documents in the possession of Mitsubishi's corporate parent.

4. On November 19, 2002, I forwarded Your Honor's November 18, 2002 opinion in support of the November 12, 2002 order to counsel for NEC USA. I requested that counsel meet and confer with me regarding NEC USA's objections. I did not receive any response from counsel. On December 5, 2002, I again wrote to counsel to request a meet-and-confer, and I served a subpoena requiring that NEC produce a witness to testify about the relationship between NEC USA and its parent company. Counsel for NEC subsequently informed me that the witness in question was unavailable on the date set out in the subpoena, but did not respond to my request that we meet and confer on the issue.

5. At about the same time, we received documents in response to a subpoena to a former NEC USA JEDEC representative, Howard Sussman, that demonstrated conclusively that NEC USA and NEC Corp. had a very close relationship with respect to both JEDEC activities and the design of DRAM technologies. A few of

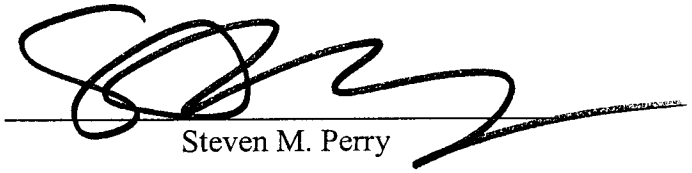
the documents in question are attached as exhibit A. The documents all relate to presentations at JEDEC meetings about the design and performance of various kinds of DRAM modules and related devices. All of the documents reflect communications between NEC USA employees and NEC Corp. employees. I have also reviewed various official JEDEC meeting minutes and have confirmed that personnel from both NEC USA and NEC Corp. attended such meetings.

6. We also recently received Samsung's privilege log, which contains entries involving ADT-related communications with some of the same NEC Corp. employees as are listed in the documents attached as exhibit A.

7. Finally, an Internet search done at my direction revealed that there is an overlap and exchange of officers between NEC USA and NEC Corp. For example, an official biography of NEC USA's president shows that for the 30 years prior to his recent appointment to that position, he served in various "high-level management positions" at NEC Corp. *See* exhibit B.

I declare under penalty of perjury that the foregoing is true and correct.

Executed on December 20, 2002 at Los Angeles, California.



Steven M. Perry

EXHIBIT A

NEC

NEC LSI MEMORY DIVISION

3-1-35 MINAMIHASHIMOTO SAGAMIHARA
KANAGAWA 229 JAPAN

TEL (0427)72-7727
FAX (0427)72-7733

TO: H. Sussman (NT1095) Received 4/29 via Forman. ( )
S. Forman (NT1035) request to present it @ JEDEC ( )
( ) ( )

CC: C. Conkle (MV4572) H. Ogawa (10-242Po)
T. Nishimura (MV4570)
O. Kimura, Y. Nishimura
H. Ikeda, M. Hayashi (24-66170)

FM: Y. Hoshino (24-66120)

Total No. of Pages: ____
(INCLUDING THIS PAGE)

DATE: 3 / 5 / 1990

YOUR REF: ____ OUR REF: ASM-

(IF THE FOLLOWING MESSAGE IS RECEIVED POORLY OR INCOMPLETELY PLS CALL 72-7727)

MESSAGE

RE: 256k x 8 VRAM PINLAYOUT (Re-send)

Attached sheet are new version of pin layout figures.

(Changes are only Typo's are corrected)
pich → pitch

Because those materials will be shown during JEDEC meeting, we've desided to resend. Sorry for bothering you by our careless misses.

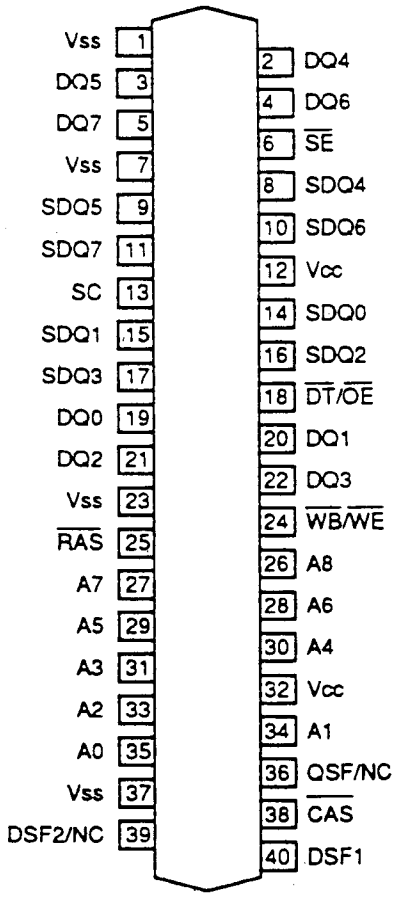
Best regards,

Y. Hoshino

C&C COMPUTERS AND COMMUNICATIONS

JEDEC-P-0291-1
Feb. 1991

256K x 8 VRAM
Pin Layout



475mil ZIP (35mil Lead Pitch)

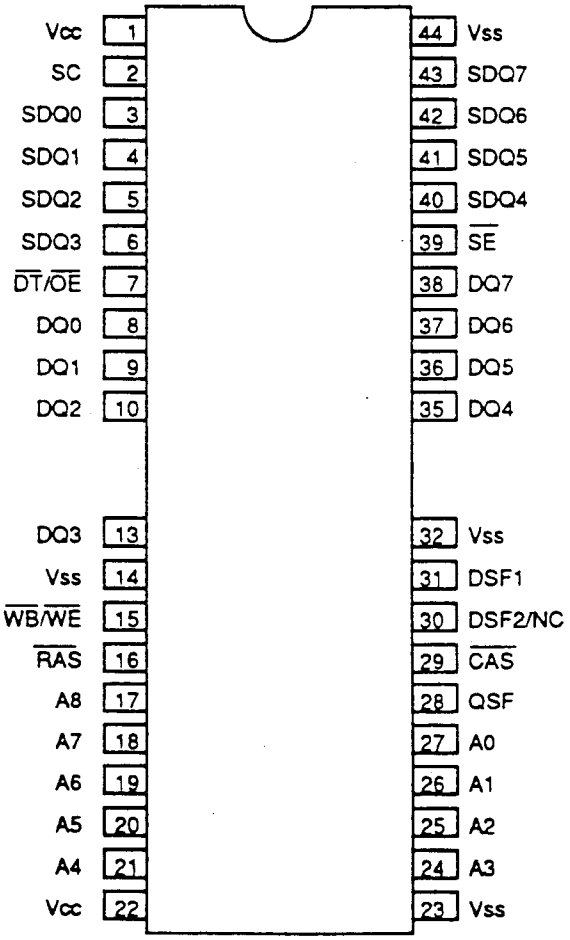
SUS-FTC 004370

NEC LSI MEMORY DIV.

C&C COMPUTERS AND COMMUNICATIONS

JEDEC-P-0291-2
Feb. 1991

256K x 8 VRAM
Pin Layout



400mil TSOP II

(0.8mm Lead Pitch)

NEC LSI MEMORY DIV.

Pin Identification

Symbol	I/O	Description
SC	Input	Serial Clock
SDQ0 - SDQ7	Input/Output	Serial Data Inputs and Outputs
QSF	Output	Special Function Output
$\overline{DT}/\overline{OE}$	Input	Data Transfer/Output Enable
DQ0 - DQ7	Input/Output	Data Inputs and Outputs
$\overline{WB}/\overline{WE}$	Input	Write-Per-Bit/Write Enable
$\overline{RAS}$	Input	Row Address Strobe
A0 - A8	Input	Address Inputs
Vcc1 - 2		+5V Power Supply
Vss1 - 4		Ground
$\overline{CAS}$	Input	Column Address Strobe
$\overline{SE}$	Input	Serial Input/Output Enable
DSF1,2	Input	Special Function Enable
N.C.		No Connection

***** FAX *****
***** FAX *****
***** FAX *****

NEC Electronics Inc.
Natick Memory Design Center
1 Natick Executive Park
Natick, Ma. 01720

tel: (508) 655-8833 x4261
fax: (508) 872-8692

November 19, 1991

TO: Z. Matsuda 24-66140

CC: T. Watamabe 24-66140
Y. Kobayashi 24-66140
A. Nagami 24-66150
FM: H. Sussman EU3150

RE: SRAM / JEDEC

Attached are copies of three faxes that were received during the time I was at NEC.

The first one is Motorola promoting their concept to NEC Systems. The additional two are proposals from Toshiba and Motorola that will be discussed at the next meeting. Please review and give me your thoughts. With the many SRAM items, should someone from your department also attend the next JEDEC meeting ?

Best regards,

Toshiba made a presentation at the September 1991 meeting on 4M Slow SRAM.

At the December meeting ,we would like to pursue that discussion. Attached are some questions to focus that discussion:

1. Should the committee establish a slow 4M SRAM standard?_____

2. Should there be a standard for X16 organization?_____

3. If there should be a standard, what package types should be included in the standard? Comments or reasons for/against? Rank importance - 5 is most important; 1 is least important.

DIP	_____	_____
SOJ	_____	_____
PLCC	_____	_____
Flatpack	_____	_____
TSOP I	_____	_____
TSOP II	_____	_____
Other	_____	_____

4. What pinout philosophy should be followed? Why?

Evolutionary	_____	_____
Revolutionary	_____	_____ _____
Other?	_____	_____ _____
Identical to HSRAM?	_____	_____
New Power/Ground Scheme?	_____	_____

5. What densities should be defined?

4M	_____
16M	_____
64M	_____

6. Who else should be surveyed?

_____

_____

7. What other issues are key to further resolution?

_____

8. What other concepts should be included in the slow pinout?

Burst	_____
Boundry Scan	_____
JTAG	_____
Other (specify)	_____

Please fax your comments to:
Jim Townsend (Mark, please note the spelling) Toshiba 714-859-3963
Thanks and regards. Hope to hear back before the meeting.

To:HIROYUKI MATSUO - NEC
CC:SHIGEMI KAWAI - NML, YOSHIYUKI KAYASHIMA - MOT/TKY, Roger Kung, Howard Su
BCC:
Priority: Normal
Date sent: 11/12/91

MOTOROLA
MOS Memory Products Division
P. O. Box 6000, MD-K5
Austin, Texas 78762

David Chapman,
Strategic Product Planning Manager
(512) 928-7184 Office
(512) 928-6809 Fax
(512) 928-5114 MacFax

Date: 11/12/91

Subject: FOLLOW-UP FROM OUR 11/12/91 MEETING

TO: HITOYUKI MATSUO, SR MGR - 1ST CKT ENG DEPT
COMPUTER ENG DIV NEC - TOKYO
011-81-42-3-33-1015 OFF, 011-81-42-3-33-1890 FAX

DEAR MATSUO-SAN,

THANK YOU SO MUCH FOR YOUR KIND ATTENTION AT OUR MEETING IN AUSTIN. I AM LOOKING FORWARD TO A VISIT WITH YOUR ENGINEERING STAFF AS SOON AS IS PRACTICAL. WE ARE LOOKING AT MID-JANUARY AS A POSSIBILITY.

YOUR ENTHUSIASM FOR OUR 64KX16/18 TSOP PINOUT AND LV-HP INTERFACE PROPOSALS CAN BE COMMUNICATED TO JEDEC THROUGH YOUR JEDEC REPRESENTATIVE, HOWARD SUSSMAN, IN BOSTON. HIS OFFICE PHONE NUMBER IS (508) 685-8833 Ext. 4261, AND FAX NUMBER: (508) 870-6691. JEDEC ENCOURAGES THE DIRECT PARTICIPATION OF MEMORY USERS AT ITS MEETINGS. HP, IBM, DEC, APPLE, COMPAQ AND UNISYS ARE REGULARLY REPRESENTED AND SOMETIMES MAKE THEIR OWN PROPOSALS.

THE NEXT MEETING WILL BE HELD AT THE INTERCONTINENTAL HOTEL MAUI. CALL 808-879-1922 FOR RESERVATIONS AT THE DIA RATE:$120/NIGHT. THE SCHEDULE FOLLOWS:

DEC 2 - JC-42.1 (PLD)
JC-42.4 (NON-VOLATILE MEMORY)
JC-42.5 (MODULES & MEMORY CARDS)
DEC 3 - JC-16 (LOW VOLTAGE INTERFACE)
DEC 4 - JC-16 (CONTINUED)
JC-42.3 TASK GROUP (RAM)
DEC 5 - JC-42.3 TASK GROUP (CONTINUED)
DEC 6 - JC-42.3 COMMITTEE MEETING (RAM BALLOTING)

I HAVE ENCLOSED THE PLCC PINOUT FOR THE 64KX16/18-10ns 0.8u BiCMOS PSRAM THAT WE HAVE IN DESIGN AT THIS TIME. AS YOU CAN SEE, SEVERAL VENDORS HAVE MADE PROPOSALS AT JEDEC TO EXTEND THIS PINOUT TO SOME SPECIAL FUNCTION RAMS. WE EXPECT THE DIE E T FOR THE PLCC

- more -

To:HIROYUKI MATSUO - NEC

CC:SHIGEMI KAWAI - NML, YOSHIYUKI KAYASHIMA - MOT/TKY, Roger Kung, Howard Su

BCC:

Priority: Normal

Date sent: 11/12/91

TO BE AVAILABLE FROM SEVERAL SUPPLIERS. WE ALSO EXPECT THE PLCC DIE WILL BE FASTER AND HAVE BETTER INPUT NOISE MARGINS THAN THE 44 PIN SOJ DEVICES. THIS IS THE DEVICE THAT I BELIEVE WOULD BE WELL SUITED FOR YOUR 3.3V R4000 PROGRAM. ALTHOUGH WE DO NOT HAVE ANY SPECIFIC TAB PLANS FOR THIS DEVICE YET, WE LOOK FORWARD TO EXPLORING THE POSSIBILITIES WITH YOU. NEC IS OUR MOST IMPORTANT JAPANESE FSRAM CUSTOMER. WE INTEND TO DO WHATEVER WE CAN TO MEET YOUR NEEDS FOR THIS IMPORTANT PROJECT.

BEST REGARDS,

DC

A	A	/E	/UW	/LW	VCC	VSS	DL	C, K, CK	/G	A	A	A	SYNC w/ DLE (ITEM 389.4)	
A	A	/E	/UW	/LW	/AC	/AP	/ADV	C, K, CK	/G	A	A	A	BURST RAM (ITEM 389.3)	
A	A	/E	/UW	/LW	VCC	VSS	DL	AL	/G	A	A	A	ASYNC w/ DLE (ITEM 389.2)	
A	A	/E	/UB	/LB	VCC	VSS	/W	C, K, CK	/G	A	A	A	SYNC (ITEM 389.1)	
A	A	/E	/UB	/LB	VCC	VSS	/W	AL	/G	A	A	A	ASYNC 64KX18	STD 21-C
A	A	/E	/UB	/LB	VCC	VSS	/W	AL	/G	A	A	**NC**	ASYNC 16KX18	FIG 3.7.7-5

	7	6	5	4	3	2	1	52	51	50	49	48	47	
DQ9	8												46	**DQ8, NC**
DQ10	9												45	DQ7
VCCQ, VCC	10												44	DQ6
VSSQ, VSS	11												43	VCCQ, VCC
DQ11	12												42	VSSQ, VSS
DQ12	13						52 Pin PLCC						41	DQ5
DQ13	14						750 x 750 mils						40	DQ4
DQ14	15												39	DQ3
VSSQ, VSS	16												38	DQ2
VCCQ, VCC	17												37	VSSQ, VSS
DQ15	18												36	VCCQ, VCC
DQ16	19												35	DQ1
DQ17, NC	20												34	DQ0
	21	22	23	24	25	26	27	28	29	30	31	32	33	

NC	A	A	A	A	A	A	VSS	VCC	A	A	A	A	A	16Kx16/18
A	A	A	A	A	A	A	VSS	VCC	A	A	A	A	A	64KX16/18

CURRENT JEDEC 64KX16/18 ASYNC STANDARD
and ASYNC w/ DLE, SYNC & BURST FSRAM PROPOSALS

COMPILED BY: DAVID CHAPMAN, MGR., MOTOROLA MEMORY PRODUCT PLAN
512-928-7184 OFF. 512-928-6809

To: Howard Sussman - NEC, Farhad Tabrizi - Hit, JIM TOWNSEND - TOSHIBA
CC: JEFF CHRITZ - EDI, PATRICK CHUANG - SONY, CARL COOK - HP, DAVID FORD - CYP
BCC:
Priority: Urgent
Date sent: 11/7/91

MOTOROLA
MOS Memory Products Division
P. O. Box 6000, MD-K5
Austin, Texas 78762

David Chapman,
Strategic Product Planning Manager
(512) 928-7184 Office
(512) 928-6809 Fax
(512) 928-5114 MacFax

Date: 11/7/91

Subject: Wide Revo Pinout Proposals

Gents,

It is clear to all of us that wider RAMs and finer package pitches are on the way and we need to get ready for them. Moderately wide FSRAMs will comprise the bulk of the market's next wave. RAMS in x16 and x18 organizations can and often will be implemented on the same mask sets as x4's and x8/9's. These two factors combined make development of a two sided fine pitch pinout standard imperative.

It is also clear that these wide RAMS must perform as well as their x8 cousins, so the performance principles observed in the development of the x8 pinouts have been followed in the development of this proposal. No output is any further than two pins away from a power pin (except x18's). There are no more that four outputs per ground pin (except x18's). Control pins are located as close to the center as possible and the Byte Control pins are located close to the bytes they control. NC's are bubbled to the ends.

We hope you find these ideas stimulating and invite your comments.

Best regards,

DC

Fine Pitch
Two Sided
Revo FSRAM
Pinout
Proposal

Pins 1–26 (left side of the 52-pin outline):

Pin	1Mx18 Sync	1Mx18 Async	1Mx16 Sync	1Mx16 Async	256kx18 Sync	256kx18 Async
1	A	A	A	A	NC	NC
2	A	A	A	A	A	A
3	A	A	A	A	A	A
4	A	A	A	A	A	A
5	A	A	A	A	A	A
6	UB\	UB\	UB\	UB\	UB\	UB\
7	E\	E\	E\	E\	E\	E\
8	DQU	DQU	DQU	DQU	DQU	DQU
9	DQU	DQU	DQU	DQU	DQU	DQU
10	Vcc	Vcc	Vcc	Vcc	Vcc	Vcc
11	Vss	Vss	Vss	Vss	Vss	Vss
12	DQU	DQU	DQU	DQU	DQU	DQU
13	DQU	DQU	DQU	DQU	DQU	DQU
14	DQU	DQU	DQU	DQU	DQU	DQU
15	DQU	DQU	DQU	DQU	DQU	DQU
16	Vss	Vss	Vss	Vss	Vss	Vss
17	Vcc	Vcc	Vcc	Vcc	Vcc	Vcc
18	DQU	DQU	DQU	DQU	DQU	DQU
19	DQU	DQU	DQU	DQU	DQU	DQU
20	DQU	DQU	W\	W\	DQU	DQU
21	W\	W\	A	A	W\	W\
22	[illegible]	A	A	A	A	A
23	[illegible]	A	A	A	A	A
24	A	A	A	A	A	A
25	A	A	A	A	A	A
26	A	A	NC	NC	A	A

Pins 52–27 (right side of the 52-pin outline):

Pin	256kx18 Async	256kx18 Sync	1Mx16 Async	1Mx16 Sync	1Mx18 Async	1Mx18 Sync
52	A	A	NC	NC	A	A
51	A	A	A	A	A	A
50	A	A	A	A	A	A
49	A	A	A	A	A	A
48	LB\	LB\	A	A	LB\	LB\
47	G\	G\	LB\	LB\	G\	G\
46	DQL	DQL	G\	G\	DQL	DQL
45	DQL	DQL	DQL	DQL	DQL	DQL
44	DQL	DQL	DQL	DQL	DQL	DQL
43	Vcc	Vcc	Vcc	Vcc	Vcc	Vcc
42	Vss	Vss	Vss	Vss	Vss	Vss
41	DQL	DQL	DQL	DQL	DQL	DQL
40	DQL	DQL	DQL	DQL	DQL	DQL
39	DQL	DQL	DQL	DQL	DQL	DQL
38	DQL	DQL	DQL	DQL	DQL	DQL
37	Vss	Vss	Vss	Vss	Vss	Vss
36	Vcc	Vcc	Vcc	Vcc	Vcc	Vcc
35	DQL	DQL	DQL	DQL	DQL	DQL
34	DQL	DQL	DQL	DQL	DQL	DQL
33	A	CK\	A	CK\	A	CK\
32	A	A	A	A	A	[illegible]
31	A	A	A	A	A	A
30	A	A	A	A	A	A
29	A	A	A	A	A	A
28	A	A	A	A	A	A
27	NC	A	NC	A	NC	A

Pins 1–24 (left side of the 48-pin outline):

Pin	256kx16 Sync	256kx16 Async	64kx18 Sync	64kx18 Async	64kx16 Sync	64kx16 Async
1	A	A	A	A	A	A
2	A	A	A	A	A	A
3	A	A	A	A	A	A
4	A	A	A	A	A	A
5	UB\	UB\	UB\	UB\	UB\	UB\
6	E\	E\	E\	E\	E\	E\
7	DQU	DQU	DQU	DQU	DQU	DQU
8	DQU	DQU	DQU	DQU	DQU	DQU
9	Vcc	Vcc	Vcc	Vcc	Vcc	Vcc
10	Vss	Vss	Vss	Vss	Vss	Vss
11	DQU	DQU	DQU	DQU	DQU	DQU
12	DQU	DQU	DQU	DQU	DQU	DQU
13	DQU	DQU	DQU	DQU	DQU	DQU
14	DQU	DQU	DQU	DQU	DQU	DQU
15	Vss	Vss	Vss	Vss	Vss	Vss
16	Vcc	Vcc	Vcc	Vcc	Vcc	Vcc
17	DQU	DQU	DQU	DQU	DQU	DQU
18	DQU	DQU	DQU	DQU	DQU	DQU
19	W\	W\	DQU	DQU	W\	W\
20	A	A	W\	W\	A	A
21	A	A	A	A	A	A
22	A	A	A	A	A	A
23	A	A	A	A	A	A
24	A	A	A	A	NC	NC

Pins 48–25 (right side of the 48-pin outline):

Pin	64kx16 Async	64kx16 Sync	64kx18 Async	64kx18 Sync	256kx16 Async	256kx16 Sync
48	NC	NC	A	A	A	A
47	A	A	A	A	A	A
46	A	A	A	A	A	A
45	A	A	LB\	LB\	A	A
44	LB\	LB\	G\	G\	LB\	LB\
43	G\	G\	DQL	DQL	G\	G\
42	DQL	DQL	DQL	DQL	DQL	DQL
41	DQL	DQL	DQL	DQL	DQL	DQL
40	Vcc	Vcc	Vcc	Vcc	Vcc	Vcc
39	Vss	Vss	Vss	Vss	Vss	Vss
38	DQL	DQL	DQL	DQL	DQL	DQL
37	DQL	DQL	DQL	DQL	DQL	DQL
36	DQL	DQL	DQL	DQL	DQL	DQL
35	DQL	DQL	DQL	DQL	DQL	DQL
34	Vss	Vss	Vss	Vss	Vss	Vss
33	Vcc	Vcc	Vcc	Vcc	Vcc	Vcc
32	DQL	DQL	DQL	DQL	DQL	DQL
31	DQL	DQL	DQL	DQL	DQL	DQL
30	A	CK\	A	CK\	A	CK\
29	A	A	A	A	A	A
28	A	A	A	A	A	A
27	A	A	A	A	A	A
26	A	A	A	A	A	A
25	NC	A	NC	A	A	A

NOTES:
NC's are always moved to ends.
UB\ and LB\ are located for best possible speed.
Nom. Pkg Dim.: 1M-400x775, 4M-400x825, 16M-500x975
Fin Pitch: 1M - 0.8mm, 4M - 0.8mm, 16M - 0.8mm

David Chapman FSRAM Applications & Product Planning Mgr.
Motorola Memory Products Div., Offi : 512-928-7184
email: david_chapman@ausgtr.sps.mot m, Fax: 512-928-

SUS-FTC 000790

FAX TRANSMITTAL

DATE:APR.22.1992
RN:SPX-042201
PAGE: 1/2

TO: [redacted] MV4570
T.NISHIMURA MV4571
S.FORMAN NT0800
P.WESTERDORF SE2001
FM: M.SHIRAKABE 10-24280

RE: PPM FOR APPLICATION SPECIFIC MEMORY

CC: J.MARCK, G.HULSE, R.SOGA, E.TANABE MV4570
S.KOBAYASHI, C.FURNWEGER MV4572
C.CONKLE, B.LADD MV4570
O.DELOLLIS, R.LUCIER NT0800
Y.TAKASUKA, G.SCHAUSS, K.HARDT SE2001
M.YAMAMOTO 24-88101
K.TOKUSHIGE, T.SATO, H.IKEDA 24-88120
H.INUKAI, Y.FUKUZO 24-88130
H.MYAUMI, A.HANAI 22-84051
J.YAMAGUCHI, T.IIDA, K.YAKABE 10-28550
H.HARA, T.MURATA, M.YAMADA 10-24280
A.FURUSAWA, M.TANAKA, M.FURUSAWA 10-24300
S.MURAKAMI, T.NAMIMATSU 10-24310
A.YUKAWA, H.OGAWA 10-24280

9

AS WE HAVE DISCUSSED SO FAR, I WOULD LIKE TO SET ROUGH OUTLINE FOR THE PPM AS FOLOWS:

PLEASE START YOUR PREPARATION FOR ATTENDING THE MEETING WITH YOUR PRESENTATION.
IN CASE YOU HAVE ANY QUESTION OR COMMENT ON THE AGENDA, ALSO PLEASE LET US KNOW.

PLEASE GIVE YOUR FINAL CONFIRMATION ABOUT WHO ARE GOING TO ATTEND THE MEETING FROM EACH AREA AND WHEN. (AS SOON AS IT IS AVAILABLE)

BASED ON THE PROPOSAL BY T.NISHIMURA-SAN AND FORMAN-SAN, WE ASKED H.YAMAMOTO-SAN(AGM, MEMORY LSI DIV) TO JOIN THE WRAP UP SESSION OF THIS PPM TO AUTHORIZE THE DISCUSSION THERE.
(HIS SCHEDULE IS OPEN FOR THE MOMENT)

(AA) PURPOSE OF THE MEETING

WE WOULD LIKE TO FOCUS ON FOLLOWING 8 PRODUCT CATEGORIES THIS TIME.
- VRAMs & GRAPHICS MEMORIES
- SYNCHRONOUS DRAM
- RAMBUS

(FOR 'OTHER ASMs', WE WILL DISCUSS JUST HOW TO PROMOTE, IF NECESSARY)

<VRAM>
2MVRAM : TO MAKE SOME ANALYSIS OVER THE MARKET ITSELF.
x8 IS DEFINED ALREADY, x16 ON THE WAY.
-- MARKET TREND, APPLICATION TREND, COMPETITION
-- ANY ADDITIONAL FEATURES TO BE CONSIDERED?

4MVRAM : FEATURES ARE DEFINED ALREADY.
MARKET TREND, APPLICATION TREND, COMPETITION

GRAPHICS DRAM : MARKET SURVEY , MARKET STATUS UPDATE
-- POTENTIAL DESIGN-INs
-- PROMOTION PLANS

NEXT GENERATION VRAM : FRAMEBUFFER ON CHIP
-- JEDEC ACTIVITIES UPDATE

<SYNCHRONOUS DRAMs>
-- MAY JEDEC RESULT
-- POTENTIAL DESIGN-INs
-- PROMOTION PLAN

<RAMBUS>
-- POTENTIAL DESIGN-INs
-- PROMOTION STATUS (by RAMBUS), FOLLOW-UP BY NEC-EL

ALL THOSE DISCUSSION WILL START WITH DEVELOPMENT STATUS FROM DESIGN SIDE.

(BB) TIME, PLACE AND ATTENDANCE

TIME : MAY 19(TUE) AND 20(WED) [HOPEFULLY 1.5DAYS]
PLACE: HASHIMOTO TECH. CENTER
ATTENDANCE: NEC-EL [ENGINEERING AND MARKETING]
NEC-EE
MR.YAMAMOTO (AGM)
MEMORY APPLICATION ENG. DEPT, KTC
CENTRAL MARKETING (A PART OF MEETING)
NAEDD/EEDD/(AEDD)/IBPD

(CC) AGENDA

IN MY VIEW, THE TIMETABLE LOOKS LIKE FOLLOWING:
1ST DAY(19TH) : VRAM + GRAPHIC MEMORY + RAMBUS
2ND DAY(20TH) : SYNCHRONOUS DRAM + PROMOTION PLAN + WRAP UP

SINCE WE HAVE TOO MANY ITEMS TO COVER, I WOULD LIKE TO ASK YOU TO FOCUS ON FOLLOWING:
GRAPHICS DRAM - MARKET POTENTIAL, PROMOTION IDEA
4MVRAM & NEXT GENERATION - FEATURES NEEDED BY MARKET, PROMOTION IDEA
SYNCHRONOUS & RAMBUS - MARKET PROMOTION IDEA
2MVRAM - MARKET GROWTH, NEC'S SALES PREDICTION

IN ADDITION TO THOSE FOCUSED ITEMS OF ABOVE, WE WOULD LIKE TO COVER FOLLOWING AGENDA IF POSSIBLE (I DO NOT THINK IT'S POSSIBLE TO COER EVERYTHING, THOUGH).

<< GRAPHICS APPLICATION SESSION >>

- OVERALL BUSINESS OUTLOOK (BL&EB)
- PRODUCT DEVELOPMENT STATUS UPDATE (TOKYO ENGINEERING)
- 2MVRAM * COMPETITION STATUS (BL&EB)
  * PENETRATION STATUS AND PLAN IN EACH MARKET (INCLUDING TECHNICAL PROMO.STATUS -BL&EB&KIC)
  * PROBLEM AREA IN PROMOTION (DISCUSSION)
- 4MVRAM/NEXT GENERATION VRAM
  * MARKET REQUIREMENT (BL&EB)
- GRAPHICS DRAM:

* DEFINE PROMOTION STRATEGY (DISCUSSION)

<< CACHE-FILL SESSION >>

- SYCHRONOUS DRAMs
  * DEVELOPMENT STATUS (1ST DESIGN)
  * PROMOTION STATUS (BLAZER&KTC) --- NOTE 1
  * DEFINE TARGET ACCOUNTS/PROMOTION PLAN
- RAMBUS
  * INTRODUCTION PLAN (SYSTEM DEPT)
  * MARKET RESPONCE (BLAZE) --- NOTE 2
  * DEFINE TARGET ACCOUNTS/PROMOTION PLAN

NOTE 1 : PLEASE DEFINE FOLLOWING IN YOUR PRESENTATION:
POTENTIAL ACCOUNTS, THEIR DESIGN STATUS AND PLAN INCLUDING VOLUME. IF POSSIBLE, THEIR PLAN OF MIXED USAGE OF 'S-DRAM', 'DRAM' AND 'VRAM'.

NOTE 2 : PLEASE DEFINE FOLLOWING IN YOUR PRESENTATION:
THE SAME INFORMATION AS ABOVE.
ALSO, HOW TO WORK WITH RAMBUS

THE DISCUSSION ABOUT 'SYNCHRONOUS' AND 'RAMBUS' MIGHT NOT GO DEEP ENOUGH TO SHOW YOU HOW THOSE TWO NEW PRODUCTS ARE GOING TO EMERGE IN THE MARKET. SO, PLEASE ADVISE HOW MUCH INFORMATION YOU CAN PROVIDE IN THE MEETING. THE CONTENTS AND AMOUNT OF YOUR PRESENTATION ABOUT THOSE TWO PRODUCTS ARE SUFFICIENT? WE HAVE NOT PROPOSED ANY FORMAL SURVEY TO YOUR SIDE.

ANYWAY, PLEASE LET US KNOW WHAT YOU HAVE IN YOUR MIND ABOUT WHAT TO DISCUSS FOR ABOVE TWO PRODUCTS.

<< OTHERS >>

- HOW TO WORK WITH KEY CUSTOMERS (HP/SUN/IBM/DEC/COMPAQ...)
- AD. PLAN/DOCUMENTATION
- PROMOTION TRIP PLAN

IF YOU FIND ANY QUESTIONS, PLEASE TLE US KNOW.
WE WILL BE WAITING FOR YOUR CONFIRMATION ON AGENDA, AND YOUR ATTENDANCE.

REGARDS

TO: T.Watanabe 24-66140 Sept 25, 1991
CC: T.Akashi 24-66410
CC: T.Takahashi 24-66410
CC: M.Arimura 24-66410
CC: A.Nagami 24-66150
CC: H.Sussman NT0145 ✓
CC: J.Kelley NT0105
CC: T.Matsuda 24-66140
CC: Y.Hachiya 24-66140
FM: P.Barratt NT0145
RN: NMDC9109251

RE: JEDEC SRAM Pinout standards activity

Summary

Task group meeting on Sept 17., main meeting on Sept. 18.
Significant industry activity in wide SRAMs.
-Toshiba 1M wide SRAM pinout will be balloted.
383 -PLCC vs SOJ/TSOP II controversy remains unsolved.
306 -Mitsubishi proposal for fast address option.
387 -AT&T x36 proposal.
388 -Toshiba 256K x 16 proposal.
384 -AT&T 64K x 16/18 PLCC proposal.
— -IDT responds to patent issue on burst mode.
— -Motorola proposes JTAG for SRAMs.
— -Motorola proposes fine pitch packaging for fast SRAM.

Task Group Meeting

Toshiba.In december 1990, Toshiba made a first showing of a proposed pinout family for wide SRAMs from 16K x 16/18 to 4M x 16/18 in both synchronous and asynchronous versions. These are shown as attachments 1a through 1j. At that time, there was considerable concern that only two pair of power/ground pins are provided for 18 I/Os and the logic core. At the next meeting in San Diego, Toshiba presented data taken from silicon that showed adequate performance. The committee noted that this data was only taken at room temperature and requested data taken at worst case corners. At the next meeting in Anchorage, Toshiba showed data taken at temperature to support their claims. The rest of the members appear to remain unconvinced.

Additionally, the topic of PLCC versus SOJ was debated. As shown in attachment 2, Toshiba demonstrated that the lead lengths for the power/ground pins are shorter for the SOJ.

After showing the proposal for 9 months, Toshiba wanted to go to ballot. A compromise position was worked out where only the 1M synchronous in SOJ, x8/9 and x16/18 would be balloted (1c and 1d).

Attachment 3a through 3e shows Motorola suggested pinouts that would strike a compromise between the Toshiba proposal and the need for more power pins. The committee felt, however, that it was not desirable to violate the standard 21-C for the 52 pin PLCC (attachment 4). Motorola and AT&T admitted that their choice of PLCC over SOJ was based on near term package availability and that future devices would be in SOJ. It was brought out that there is a standard TSOP II package for the 16M DRAM with 50 pins and a 400 x 825 outline. This package, however would not be as readily available to SRAM houses. Note that the Motorola PLCC proposal provides two power/ground pairs for the logic core. This item was discussed at the Pheonix meeting and some companies such as Cypress felt that only one would be required. At the Philadelphia meeting, the general consensus appeared to be that two will be needed.

Attachment 5a, 5b, and 5c are a Cypress PLCC proposal for the x16, x18, and burst mode parts. Note that the core logic power is provided at top and bottom, not from the sides as in the Motorola proposal. Cypress backed away from this proposal in favour of staying closer to the existing standard.

Mitsubishi. Attachment 6a and 6b is the Mitsubishi proposal to make the lowest order address pin (A0) an optional 'fast address' pin where the access time is 75% or less of the standard acess time. Sheet 6b is intended to show the implementation and is not meant to suggest an actual pinout.

AT&T. Attachments 7a and 7b are an AT&T proposal for x36 devices in 132 pin PQFP. There was little discussion on this item.

Toshiba. Attachment 8a through d is the Toshiba proposal for a 'slow' 256K x 16 SRAM in DIP and SOJ. By defining the part as 'slow', the issue of the number of power/ground pins was hopefully avoided. This device was not intended to contradict Toshiba's agreement to consider more pins for fast SRAMs over 1M.

Main Meeting

Toshiba. It was agreed to ballot the Toshiba 64K x 16/18 proposal as outlined above.

AT&T. Attachment 9 shows the results of the task group's discussions on 52 pin PLCC pinout. This was redrawn from the meeting notes for the purposes of clarity. Note that at this time, the SRAM group does not have a proposal to make for the 52 pin PLCC standard.

IDT. Attachment 10 is the letter from IDT regarding their position on their patent application. It is a requirement of JEDEC that companies holding a patent of a JEDEC standard feature will offer a license for a 'reasonable' fee or royalty. The committee will rewrite IDT's letter to reflect these requirements.

Motorola. Motorola introduced a proposal for implementing JTAG on SRAMs by providing 4 additional pins on the bottom of a dual in line package. They committed to provide more details at the next meeting. Motorola also introduced the concept of using fine pitch TSOP packages at the 16 M level. Since the die are becoming larger, the use of a fine pitch package could proved additional pins without a board are penalty. It was further suggested that such devices all have the same pin count since the package size will be dictated by die size, not pin count.

Conclusions

The pinouts and packages for the wide SRAMs are in a state of flux but appear to be settling on the 52 pin PLCC for the near term. It is evident that many more companies are now considering this area compared with 9 months ago. Toshiba has the lead and will probably be in the market this year. Sharp may be a close second.

The burst SRAM, a subset, is under consideration by at least Motorola, Cypress, AT&T, and NEC. It is imperative that this be followed up on. At the moment, the NECEL proposal for a two way set associative device has not been surveyed by other vendors with their customers but has evoked interest.

Thank you and Best Regards

9/91

INTERNAL MEMO
NEC ELECTRONICS INC
NATICK MEMORY DESIGN CENTER
NATICK, MA. 01760

TO: A. Nagami 24-66150

FM: H. Sussman EU3150

Attached are the presentations on low voltage from the last JEDEC JC35 meeting. I have also enclosed the presentation material from my task group. We reviewed the responses from survey ballot JC35-91-104 and arrived at a consensus for the DC characteristics. The consensus position was approved for formal ballot by a vote of 34:0. (There were 27 companies that submitted the survey ballot. NEC did not choose to respond to the survey ballot. You have previously received a copy of all of the ballot responses.) Note that there was considerable interest in the addition of AC characteristics and undershoot, but there was not any agreement on what the values should be.

Standard 8.1 task group
Charter proposal to JEDEC Council
Survey Ballot 91-52 and 91-104 results

xxx	Definition of an "Interface" Standard
Motorola	Equal Center Supply Std (Low Voltage Battery Operated and Low Voltage CMOS)
Siemens	Low Voltage I/O Spec.
Hitachi	Internal division's Low Voltage requests
Toshiba	Proposed 3.3V I/O Spec.
IBM	Proposed 3.3V I/O Spec.
MosAid	Comments on IBM's proposal
TI	Proposed 3.3V I/O Spec.
TI	4M DRAM Output characteristics.
Mitsubishi	Proposed 3.3V DRAM I/O Spec.
Sony	Comments on 3.3V Input levels
Samsung	Proposed output load
Motorola	Proposed output load
Intel	Proposed output load
Atmel	Industry Data Sheets
IDT	Logic Device Data Sheet and Low Voltage Proposal
XEROX	GTL Interface
MosAid	Active feedback Output Buffer

TO: H. Sussman EU3150 (NTO200) 1/2

FM: K. Tokushige 24-66130

RE: JEDEC (May, 1991) Report from you

you reported that DRAM Self Refresh Mode and Gophers DRAM were all approved for ballot.

But I didn't see your presentation material.

(1) pls send your presentation materials

(2) pls keep in your mind that I have a responsibility for those devices, So I have to manage all of Information,

Pls send your presentation Material 2/2

before JEDEC Meeting for discussion

and My approval.

Best Regards

FAX

To: H. Sussman (NT0145) 9/13/90 1 of 4
From: H. Ikeda (24-66120)
Re: x16 VRAM; two $\overline{WE}$, two $\overline{CAS}$ control
Rn: ASM-D-091390-1
cc: C. Conkle (MV4572)
S. Forman (NT0145)
O. Kimura, M. Hayashi, Y. Hoshino (24-66120)

Attatched are our proposal conserning two $\overline{WE}$ and two $\overline{CAS}$ control on x16 VRAM.
Key points are follows.

1. Data latch timing is common for both bytes.
2. For block write, "MASK DATA" will be latched respectively to upper-byte and lower-byte.
   For DQ0-7, column mask data wil be latched by DQ0-3.
   For DQ8-15, column mask data will be latched by DQ8-11.

The reason why we propose these way is to eliminate too complicated write/read operation, I also attached several examples to show complexity (difficulty). Please make use these materials for the discussion that will be held in next JEDEC meeting. And I also ask you to send this information to Tony Balistreri and get his opinion. I believe these proposal may be supported by TI/Toshiba/Hitachi. After JEDEC discussion, please let me know the results A.S.A.P.
If you need more detailed information, please contact me.

Best regards,

Hiroaki Ikeda

TO: Mr. H. Sussman (EU3150)

CC: Z. MATSUDA, T. WATANABE (24-66140)

FM: Y. KOBAYASHI (24-66140)

Attached are copies of 1M density x8/x9/x16/x18 Sync. SRAM JEDEC proposals.

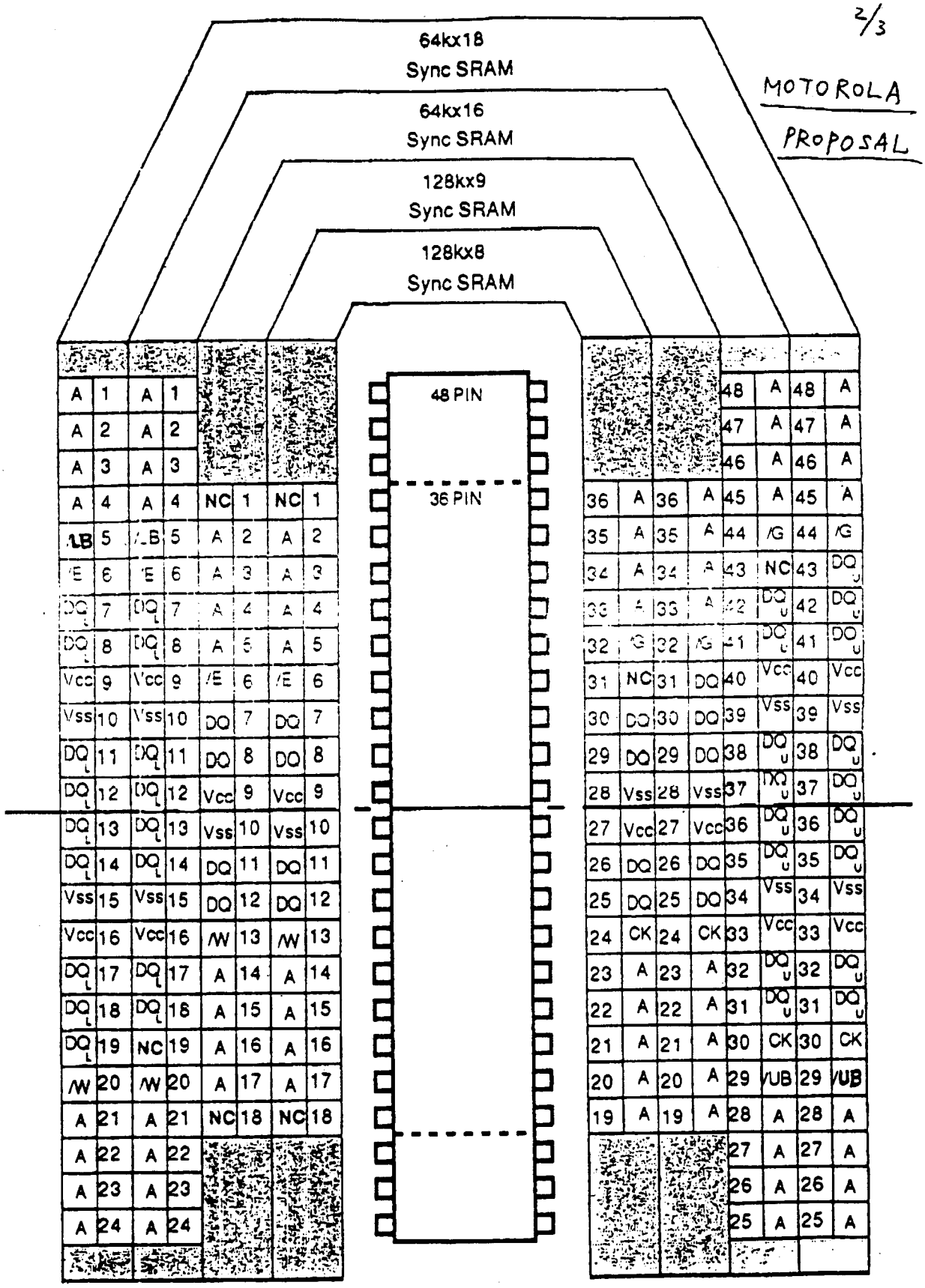
We will soon start the design of 1M density x8/x9/x16 /x18 SRAMs. But standard pinouts is not yet fixed at present. We would like to know which proposal of Motorola or Toshiba will be standardized. Recently we have heard that the Toshiba proposal becomes major.

So, please let us know the latest information which you have. If possible, please inform us by May 8th (Fax machine will stop on April 27th to May 6th (golden week)).

Best Regards

MOTOROLA

PROPOSAL



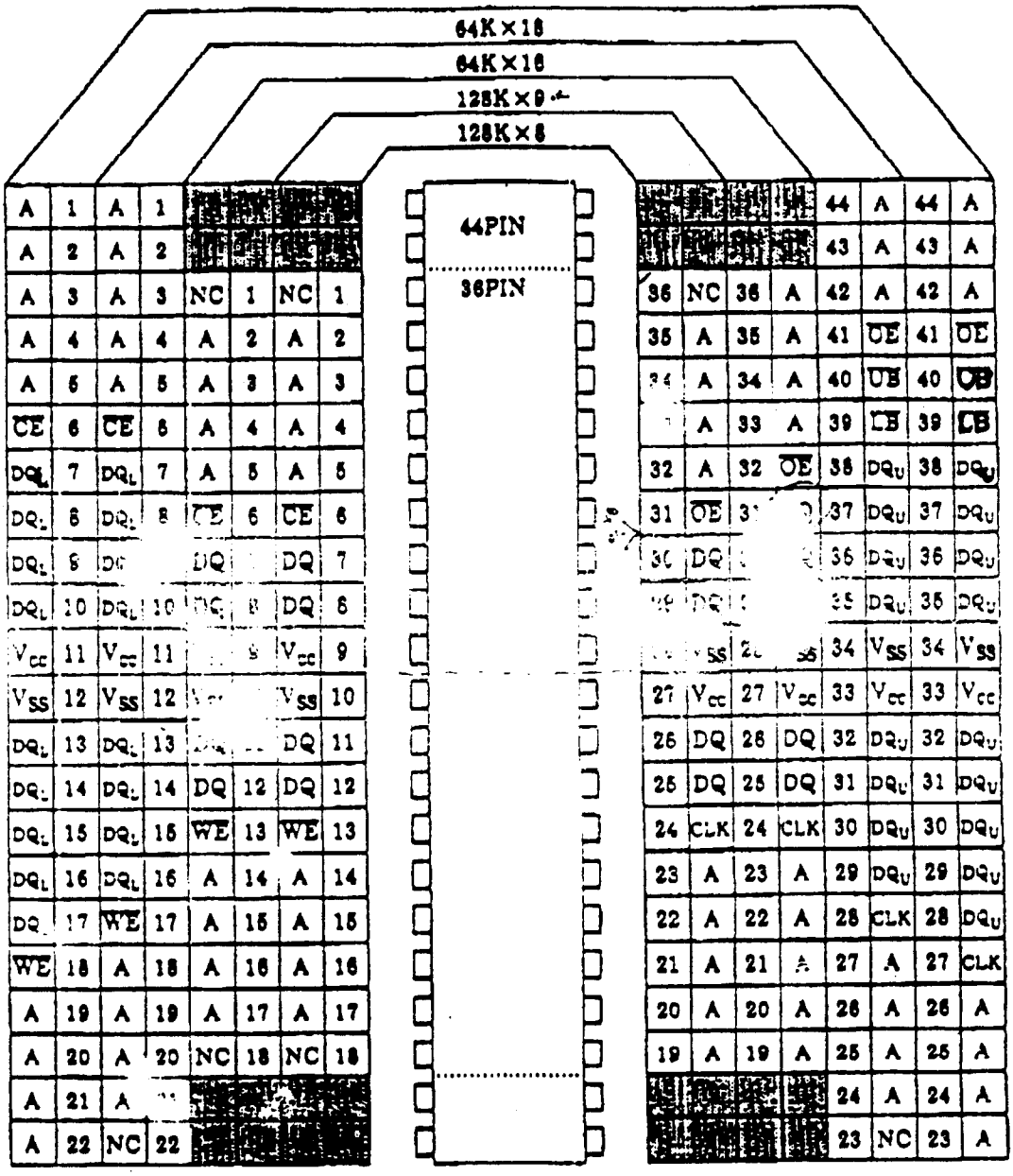
WIDE 1M TTL COMMON I/O SYNCHRONOUS SRAM FAMILY

Rev 4

1990. Nov.

WIDE 1M TTL COMMON I/O SRAM FAMILY
(SYNCHRONOUS)

TOSHIBA PROPOSAL

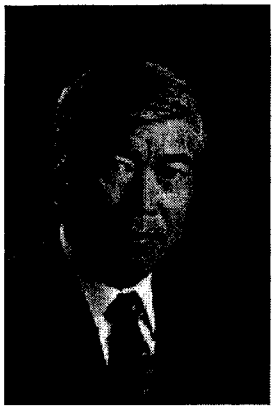


A	1	A	1							44	A	44	A
A	2	A	2							43	A	43	A
A	3	A	3	NC	1	NC	1	36	NC	36	A	42	A	42	A
A	4	A	4	A	2	A	2	35	A	35	A	41	$\overline{OE}$	41	$\overline{OE}$
A	5	A	5	A	3	A	3	34	A	34	A	40	$\overline{UB}$	40	$\overline{UB}$
$\overline{CE}$	6	$\overline{CE}$	6	A	4	A	4	33	A	33	A	39	$\overline{LB}$	39	$\overline{LB}$
DQ_L	7	DQ_L	7	A	5	A	5	32	A	32	$\overline{OE}$	38	DQ_U	38	DQ_U
DQ_L	8	DQ_L	8	$\overline{CE}$	6	$\overline{CE}$	6	31	$\overline{OE}$	31	[illegible]	37	DQ_U	37	DQ_U
DQ_L	9	DQ_L	9	DQ	7	DQ	7	30	DQ	[illegible]		36	DQ_U	36	DQ_U
DQ_L	10	DQ_L	10	DQ	8	DQ	8	[illegible]	DQ	[illegible]		35	DQ_U	35	DQ_U
V_{CC}	11	V_{CC}	11	[illegible]		V_{CC}	9	[illegible]	V_{SS}	[illegible]		34	V_{SS}	34	V_{SS}
V_{SS}	12	V_{SS}	12	[illegible]		V_{SS}	10	27	V_{CC}	27	V_{CC}	33	V_{CC}	33	V_{CC}
DQ_L	13	DQ_L	13	[illegible]		DQ	11	26	DQ	26	DQ	32	DQ_U	32	DQ_U
DQ_L	14	DQ_L	14	DQ	12	DQ	12	25	DQ	25	DQ	31	DQ_U	31	DQ_U
DQ_L	15	DQ_L	15	$\overline{WE}$	13	$\overline{WE}$	13	24	CLK	24	CLK	30	DQ_U	30	DQ_U
DQ_L	16	DQ_L	16	A	14	A	14	23	A	23	A	29	DQ_U	29	DQ_U
DQ	17	$\overline{WE}$	17	A	15	A	15	22	A	22	A	28	CLK	28	DQ_U
$\overline{WE}$	18	A	18	A	16	A	16	21	A	21	A	27	A	27	CLK
A	19	A	19	A	17	A	17	20	A	20	A	26	A	26	A
A	20	A	20	NC	18	NC	18	19	A	19	A	25	A	25	A
A	21	A	[illegible]									24	A	24	A
A	22	NC	22									23	NC	23	A

DQ_L : Lower Byte
DQ_U : Upper Byte

Package Width	SOJ / DIP	JEDEC status
128K×8	TBD/TBD	proposal by another vendor
28K×9	TBD/TBD	proposal by another vendor
64K×16	400 / –	proposal (1st showing) by TSB
64K×18	400 / –	proposal (1st showing) by TSB

EXHIBIT B



Toshio Nakajima
President and Chief Operations Officer
NEC Electronics America, Inc.

Mr. Toshio Nakajima is president and chief operations officer of NEC Electronics Inc. He is responsible for overseeing day-to-day operations and delivering company strategies and goals as set forth by the chairman and chief executive officer and the board of directors. With Mr. Nakajima's wide-ranging experience and talents, he will continue promoting NEC's presence as a strong supplier of both LSI solutions and electronic products to its broad range of customers.

Mr. Nakajima has held a variety of high-level management positions in his more than 30 years with NEC Corporation. He recently served as the general manager of NEC Corporation's 1st System LSI and System Microdivisions, and also held the positions of chief manager of development and department manager in the System Micro division.

Mr. Nakajima additionally has played an active role in assisting other companies to realize their goals, and he has served on DataPath's board of directors.

Mr. Nakajima holds a bachelor's degree in engineering from Kyoto University in Japan. He is based in NEC Electronics' headquarters facility in Santa Clara, California.

NEWS 2001

NEC Electronics Inc. Appoints New President and Chief Operations Officer

SANTA CLARA, Calif.- August 22nd, 2001 _ NEC Electronics Inc. today announced the appointment of Toshio Nakajima as president and chief operations officer (COO). In his new role, Nakajima will oversee day-to-day operations at NEC Electronics and will be responsible for delivering on the company's strategies and goals as set forth by the chairman and CEO and board of directors. Nakajima, who has held a variety of high-level management positions in his more than 30 years at NEC Corporation, will report directly to Hirokazu Hashimoto, who will remain as chairman and CEO of NEC Electronics.

"We are extremely fortunate to have a new president with the breadth of experience and knowledge that Mr. Nakajima brings with him," said Hashimoto. "We plan to utilize his talents to continue promoting NEC's presence as a strong supplier of both System LSI solutions and electronic products, in turn enabling us to provide a broader range of solutions to our customers."

Nakajima has most recently served as the general manager of NEC Corporation's 1st System LSI and System Micro divisions. He also held the positions of chief manager of development and department manager in the System Micro division. Nakajima holds a bachelor of engineering degree from Kyoto University in Japan.

About NEC Electronics Inc. NEC Electronics Inc., headquartered in Santa Clara, Calif., is one of the leading developers, manufacturers and suppliers of semiconductor products in the United States. Committed to meeting customers' cost, performance and time-to-market requirements, the company offers solutions ranging from standard products to system-on-a-chip (SOC) solutions, as well as customized products for next-generation designs. NEC Electronics also offers customers the benefits of a local manufacturing facility in Roseville, Calif., and the global manufacturing capabilities of its parent company, NEC Corporation (NASDAQ: NIPNY). For more information about products offered by NEC Electronics Inc., please visit the NEC Electronics web site at http://necelam.com.

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#10808

UNITED STATES OF AMERICA
BEFORE THE FEDERAL TRADE COMMISSION

In the Matter of	)	
	)	Docket No. 9302
RAMBUS INCORPORATED,	)	
a corporation.	)	

CERTIFICATE OF SERVICE

I, IJay Palansky, hereby certify that on December 23, 2002, I caused a true and correct copy of the *Rule 3.22(f) Declaration of Steven M. Perry in Support of Rambus Inc.'s Motion to Compel NEC Electronics, Inc. to Produce Documents in its Parent Company's Possession Responsive to the Subpoena Served by Rambus Inc.* to be served by facsimile at 415-371-1211, to be followed by overnight delivery, to Thelen, Reid & Priest LLP, counsel for NEC, at 101 Second Street, Suite 1800, San Francisco, California 94105, and the following persons by hand delivery:

Hon. James P. Timony
Administrative Law Judge
Federal Trade Commission
Room H-112
600 Pennsylvania Avenue, N.W.
Washington, D.C. 20580

Donald S. Clark, Secretary
Federal Trade Commission
Room H-159
600 Pennsylvania Avenue, N.W.
Washington, D.C. 20580

Richard B. Dagen
Assistant Director
Bureau of Competition
Federal Trade Commission
601 Pennsylvania Avenue, N.W.
Room 6223
Washington, D.C. 20580

M. Sean Royall
Deputy Director, Bureau of Competition
Federal Trade Commission
Room H-378
600 Pennsylvania Avenue, N.W.
Washington, D.C. 20580

Malcolm L. Catt
Attorney
Federal Trade Commission
Room 3035
601 Pennsylvania Avenue, N.W.
Washington, D.C. 20580

IJay Palansky

PUBLIC

UNITED STATES OF AMERICA
BEFORE THE FEDERAL TRADE COMMISSION

In the Matter of	)	
	)	Docket No. 9302
RAMBUS INC.,	)	
a corporation,	)	
	)	

CERTIFICATION

I, Steven M. Perry, hereby certify that the electronic copy of RULE 3.22(f) DECLARATION OF STEVEN M. PERRY IN SUPPORT OF RAMBUS INC.'S MOTION TO COMPEL NEC ELECTRONICS, INC. TO PRODUCE DOCUMENTS IN ITS PARENT COMPANY'S POSSESSION RESPONSIVE TO THE SUBPOENA SERVED BY RAMBUS INC. accompanying this certification is a true and correct copy of the paper original and that a paper copy with an original signature is being filed with the Secretary of the Commission on December 23, 2002 by other means.

Dated: December 23, 2002

/s/
Steven M. Perry