A New Concept in Computing

BY [redacted]

Unclassified

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A new computing scheme was proposed by von Neumann in a patent[1] submitted in 1954 and granted posthumously last December. This paper is an explanatory statement of the ideas embodied in the patent, with other related topics.

INTRODUCTION

Von Neumann recognized the limitations of computing speeds inherent in the existing technology due to device operation times, signal propagation delays, and transmission distortion of information video pulses. Of course we cannot reconstruct the thinking that led him to the proposed solution, but the attractiveness of large bandwidths which could be obtained at microwave frequencies and of representation of digital information by distinct phases of an RF signal (neither of which had been exploited in computer technology) no doubt seemed fertile ground for investigation. Whatever the prompting force was, von Neumann proposed a computing scheme using RF techniques which is potentially faster if employed at microwave frequencies than present conventional methods. The same methods will also work at lower frequencies.

The availability of an element of the following nature was assumed:

a. An element is available that has both L and C, one of which is nonlinear.

b. The dissipation in the element is not great in comparison to the nonlinearity. This dissipation may be resistive loss or a hysteresis.

c. The element has approximately linear operation for small signals and has a resonant frequency (which is later referred to as f_0).

NONLINEAR REACTANCE ANALYSIS

To see that such an element can exist, consider the nonlinear capacitor that has no loss and no hysteresis[2], and is mounted in multiply-tuned circuits. The bare outline of the analysis will be presented.

[1] "Non-linear Capacitance or Inductance Switching, Amplifying, and Memory Organs", John von Neumann, U. S. Patent No. 2,815,488, issued 3 December 1957.

[2] These restrictions may be relaxed somewhat in the practical case, but are assumed here to make explanation simpler.

Full discussion of it has been published by Manley and Rowe[4]. As pointed out in that reference, consideration of nonlinear reactances as elements to transfer power from one frequency to another is not a new subject, having been discussed by Hartley in 1916.

Consider the circuit in Fig. 1.

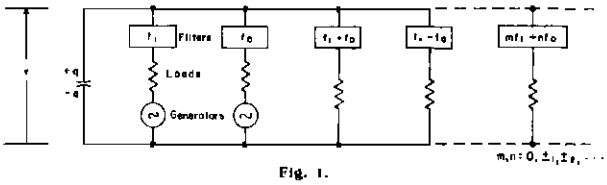


Fig. 1.

$v = f(q)$ is an arbitrary, single-valued function, being in general nonlinear.

The filters have zero impedance at the labeled frequency and infinite impedance otherwise.

Such a circuit might be a number of tuned circuits in parallel with the nonlinear reactance (which also may be inductance rather than capacitance). Two of the tuned circuits contain RF generators.

The charge on the capacitor, the current into it, and the voltage across it may all be expressed as double Fourier series in the frequencies $mf_1 + nf_0$ for $m, = 0, \pm 1, \pm 2, \cdots$. By manipulation of these expressions[4] one may derive others giving the summation of real power at all frequencies into the nonlinear element in terms of double integrals over complete cycles of f_1 and f_0 wherein the integrand is $v = f(q)$.

The variable q, hence $f(q)$, is periodic in f_1 and f_0 and thus for an element without hysteresis these double integrals are identically zero. From this are obtained the Manley-Rowe conditions, namely:

$$\sum_{m=0}^{\infty}\sum_{n=-\infty}^{\infty}\frac{mW_{m,n}}{mf_1+nf_0}=0 \qquad m,\ n\ =\ \text{integers}$$

$$\sum_{m=-\infty}^{\infty}\sum_{n=0}^{\infty}\frac{nW_{m,n}}{mf_1+nf_0}=0,$$

where $W_{m,n}$ is the real power at frequency $mf_1 + nf_0$ *into* the nonlinear reactance.

[4] "Some General Properties of Nonlinear Elements—Part I. General Energy Relations", J. M. Manley and R. E. Rowe, *Proc. of IRE*, Vol. 44, No. 7, pp. 904–918, July 1966.

[4] Complete discussion is given in reference 3.

Of course, a reactance without hysteresis, whether linear or nonlinear, can dissipate no energy. Therefore, as must be true and as can be obtained from the above conditions, the summation of energy at all frequencies into the reactance is zero, and power supplied from one source at a given frequency will show up in another branch of the circuit at another frequency. The exact manner in which this takes place is controlled by the above conditions.

The circuit initially pictured was a general circuit; variations of it may lead to modulators, demodulators, amplifiers, oscillators, or combinations of them. Of interest to this discussion is a sub-harmonic generator as shown in the circuit of Fig. 2.

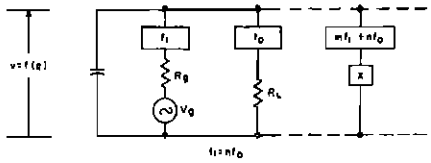


Fig. 2.

V_G is an RF generator, essentially an AC power supply. The f_1 filter and R_G correspond to the resonant tank of the RF generator. The f_0 filter and R_L are the load tank at the sub-harmonic frequency desired. The filters at all other frequencies are terminated in pure reactances, X, which for simplicity may be open or short circuits. There will be no power loss at these other frequencies.

The only terms of interest in the Manley-Rowe conditions are for $(m, n) = (0, 1)$ and $(0, n)$. The rest of the $W_{m,n}$ are zero. This gives:

$$\frac{W_{0,1}}{f_0}+\frac{nW_{0,n}}{nf_0}=0,$$

or simply

$$W_{0,1} = -W_{0,n}.$$

The minus sign indicates that all the energy put into the nonlinear reactance at the $f_1 = nf_0$ frequency is transferred to the load tuned to the f_0 frequency. This is a harmonic generator with an ideal efficiency of 100%, assuming no losses in the reactive termination of the other frequencies. Of course with real elements some losses, and resultant reduction of efficiency, will occur, but the basic (sub-)harmonic generation process, unlike that of Class C multipliers or crystal multipliers, is not limited in efficiency.

NATURE OF NONLINEARITY REQUIRED

It remains to show that an element with a threshold of sub-harmonic generation is possible. The transfer function for such an element is shown in Fig. 3.

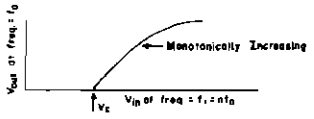


Fig. 3.

The reactance function shown in Fig. 4 is, of course, idealized. In the actual case only a smoothly varying reactance would be obtainable which could be approximated by the straight lines of Fig. 4. At V_c, the nonlinearity produces a negative resistance great enough to overcome passive circuit losses. At this level of the RF power supply, the circuit would break into oscillation at the sub-harmonic frequency and the threshold action is obtained. For $V_{in} > V_c$, the amount of signal $V_{in} - V_c$ will be effective in producing sub-harmonic voltage.

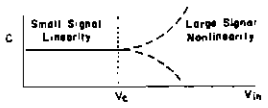


Fig. 4.

DEVICES

Various solid-state elements have been proposed to perform the function of the nonlinear reactance.[5] An equivalent circuit for a nonlinear capacitance, as realized with a semiconductor diode, is shown in Fig. 5.

[5] "Two-Terminal P–N Junction Devices for Frequency Conversion and Computation", by Arthur Uhlir, Jr., *Proc of IRE*, Vol. 44, No. 9, pp. 1188–1191, Sept. 1956.
"The Theory of the Ferromagnetic Microwave Amplifier", H. Suhl, *Journal of Applied Physics*, pp. 1225–1236, Nov. 1957.
"Semiconductor Capacitance Amplifier", Frederick Dill, Jr. and Louis Depian, *IRE Convention Record*, Part 3, pp. 172–174, 1956.
"Small-Signal Measurements on Planar P–N Junction Diodes". A. E. Bakenowski, *Task 8 Report on Crystal Rectifiers*, Bell Telephone Laboratories, 15 April 1955.
"Frequency Conversion in P–N Junction Devices", A. Uhlir, *Task 8 Report on Crystal Rectifiers*, Bell Telephone Laboratories, 15 January 1955.

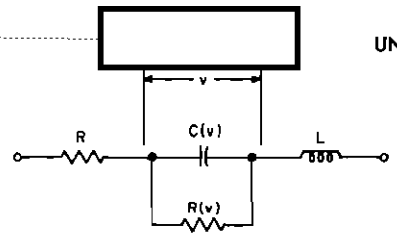


Fig. 5.

v = Barrier voltage
R = Bulk resistance
$R(v)$ = Barrier resistance (which may be nonlinear)
L = Lead inductance
$C(v)$ = Barrier capacity (nonlinear)

The barrier capacity is the primary nonlinearity of the device. Among these components the following relationships are assumed:

(1) $R(v) \gg R$
(2) $R_0 = \sqrt{L/C_s} \gg R, C_s$ = small signal $C(v)$ } (The element has a reasonable Q.)
(3) $f_0 = 1/(2\pi\sqrt{LC_s})$ (Tuned to the sub-harmonic frequency desired.)

This equivalent circuit as drawn includes both linear and nonlinear reactances. These may be physically separated in real devices. Research is being done on other practical means of achieving sub-harmonic response.

INFORMATION IN TERMS OF PHASE

The phase of the f_0 signal is determined by the phase of the f_1 signal. Qualitatively, this may be understood by observing, that the oscillations in the f_0 circuit are not like the oscillations in an ordinary negative resistance oscillator, in which the power supply is d-c and the phase of the oscillation is determined by noise when the oscillator is turned on. The nonlinear-reactance sub-harmonic generator is more akin to a crystal harmonic generator in which power is transferred from one frequency to another by a nonlinear element. This is true even though the action of the nonlinear reactance device in general may be explained in terms of the apparent negative resistance reflected into each appropriate branch of the circuit.

Eliminating any constant phase shift between the fundamental and the nth harmonic, the phase relationships are examined more closely in Fig. 6.

In the example in which $n = 3$, the two signals are assumed in phase at $t = 0$. (The $n = 3$ example is chosen deliberately to point out im-

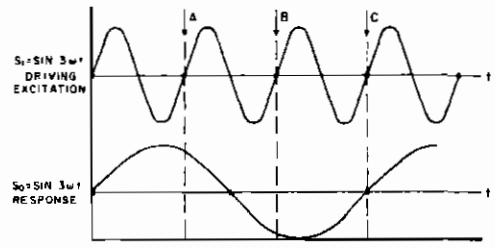


Fig. 6.

portant relationships and to avoid the $n = 2$ case, in which simplicity may cause some essential points to be overlooked.) One full cycle of S_1 later, at point A, S_1 is the same as it was at $t = 0$, but S_0 has a relative phase shift of $2\pi/3$. Similarly, at point B, S_1 is the same again, but S_0 now has a phase shift of $4\pi/3$. At point C, S_0 has a phase shift of $6\pi/3 = 2\pi$ or, like S_1, the same relative phase as when $t = 0$. Thus there are, for $n = 3$, three indeterminate phase relationships between S_0 and S_1, because in the continuous wave, S_1, one cycle is just like another. In the general case there are n such indeterminate relationships between the RF power supply (S_1) and the induced sub-harmonic response (S_0), each of which can represent a logical state.

PHASE SELECTION AND CONTROL

If the power supply (S_1) is increased from zero amplitude past the critical amplitude, V_c, a sub-harmonic response S_0 will appear when the amplitude of S_1 is V_c. Since which of the n possible phases of S_0 will result is indeterminate, noise, or—indifferently—a small S_0 signal from another element, will dictate which phase will appear. Once the harmonic response has started, however, no external signal of less magnitude than $|S_0|$ can change the phase of the response. A simple cycle can be diagrammed (Fig. 7), plotting envelope amplitudes only. The S'_0 signal would have no effect if present at any other time than when $|S_1| = V_c$ and is increasing. Note that:

$\lvert S_0 \rvert$	$>$	S'_0	(Amplification)
Duration of S_0	$>$	Duration of S'_0	(Memory)
Phase of S_0	$=$	Phase of S'_0	(Control or Toggle Action)

For practical realization of any computing scheme the electrical process must have natural or built-in margins. Noise, stray-signal pickup, slight misadjustment of circuits, component changes with age, all can cause a certain malfunctioning of the equipment, if the parameters which determine the action of the machine must have precise

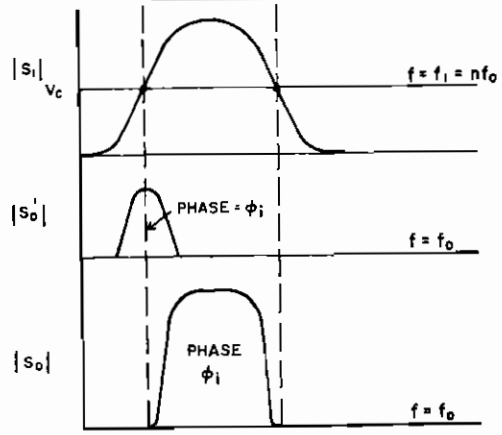


Fig. 7.

values to cause action. For, in practice, action must occur if the appropriate parameter falls within a certain region, or margin, about the ideal value.

The controlling signal, S'_0, has up to now been assumed to coincide exactly with one of the n possible phases, Φ_i, of the response, S_0, and to cause S_0 to respond with that phase, Φ_i.

In Fig. 8, the phase of S'_0 is shown as being closer to the phase Φ_0 than either Φ_1 or Φ_2. The system will stabilize with S_0 at phase Φ_0, since this requires the minimum amount of energy in the presence of the S'_0 signal to respond at the Φ_0 phase as compared with the other possible phases. The figure is not intended to illustrate the exact duration (in terms of number of cycles) of the transient condition, but is only a qualitative picture. The duration of the transient will depend on the rate of build-up of the S_1 envelope and the ratio of the response S_0 to the control S'_0 during and after the start of the response. The magnitude of $\Delta\Phi$ and the effective damping constant of the transient condition will also be important.

One may conclude from this that the phase-locking property of the sub-harmonic generator has natural margins, and hence is a practical method.

AGGREGATES OF ELEMENTS

In order to control the flow of information in a logical machine, ways

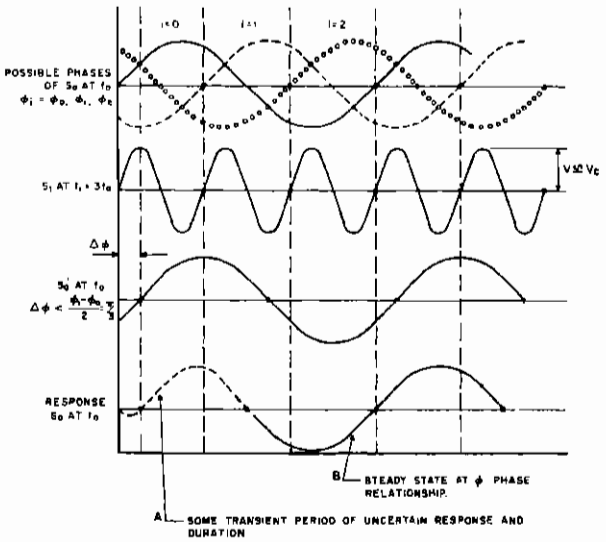


Fig. 8.

must be devised to establish an order of control. For example, if information is to flow from A to B, then A must control B but B must not control A. Ordinarily this is no problem, because the non-reciprocal devices normally used in a logical circuit to provide gain or gating perform this function automatically, but in this case one must consider the control problem separately.

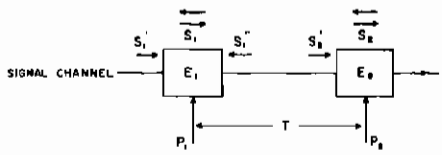


Fig. 9.

It is now necessary to devise a diagrammatic model of devices and their interconnection (see Fig. 9). The following symbolism and nomenclature will be used:

E_1, E_2 are elements such as have been described.
P_1, P_2 are amplitude-modulated AC power supplies.
S_1, S_2 are the output signals of E_1, E_2, respectively.
S'_1, S'_2 are the controlling signals for E_1, E_2, respectively.
S''_1 is the signal reaching E_1 from E_2.

The signal channel is an electromagnetic propagation path which permits propagation in either direction. The response S_1, from E_1, travels in both directions on the signal channel. The problem is to make E_1

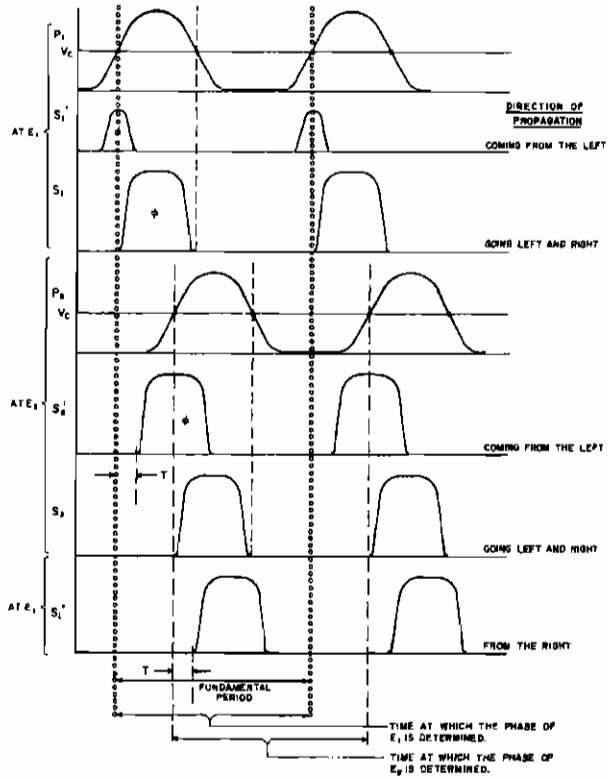


Fig. 10.

control E_2 and not the reverse. Let T be the time delay of the signal between elements E_1 and E_2. Consider next the timing sequence in Fig. 10.

With the timing cycle as pictured, E_1 can control E_2 but E_2 cannot control E_1. If the relative timing (i. e., the order of occurrence) of the P_1 and P_2 modulation is reversed, the direction of control is reversed.

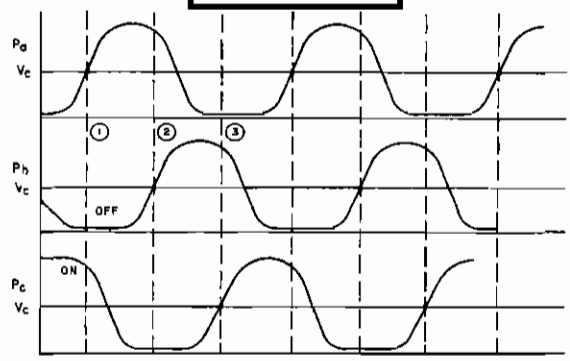
To prevent signals other than those from next neighbors from forcing synchronization with the wrong phase, an attenuator is placed in the signal path between each element. Stray signals will have had to pass through at least two attenuators, instead of only one, so that unwanted signals will not have a major influence in determining the phase of the sub-harmonic response. The natural margins of the process enable this to work properly.

With the simple combination of elements described above, not much can be done. If, however, three classes of elements are used as shown in Fig. 11, and the timing principles discussed above are employed, all logical operations can be realized. Classes of elements are defined by the timing of the modulation of the AC power supply, as shown in the figure.

The elements of classes A, B, and C are shown interconnected by signal paths. Their respective power supplies have modulation as illustrated. The delay between elements is assumed to be negligible with respect to the power-supply modulation period. *Recalling that the phase of the response is determined by the phase of signals from other elements present when the power supply passes the critical level (the heavy dots in the diagram), observe at each dot which other element is ON.* For example, at (1) in the diagram P_a is passing the critical level, element B is off, and element C is on. Therefore, C controls A. Similarly, at (2), A controls B, and at (3), B controls C. Putting a delay between elements equal to one third of the period of the power-supply modulation, as in Fig. 12, inverts the order of control. The exact fraction of a cycle needed to do this is related to the number of different types of elements (i. e., A, B, C, . . .). Three is the minimum number of types required, and results in the simplest hierarchy of control.

This order of control is independent of which phase is induced in the controlled element by the controlling element. Similarly the number of classes of elements is independent of the number of possible phase states.

The delays referred to above are in terms of *group velocity* with respect to the power-supply modulation period. This period has been assumed to be long compared to the period of the sinusoidal signals involved, so that adjustments of delay to fractional cycles of the sinus-



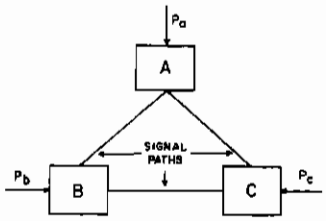


Fig. 11.

oidal voltage in the signal channel will not affect appreciably the delays previously discussed. Consider now the *phase velocity* of the signal channel. The phase induced in the controlled element will depend on the phase delay between it and its controlling element. A phase Φ_i in the controlling element after a phase delay K would put the controlled element into phase state $\Phi_i + K$. For the binary case, the phase shift K would be either an even or an odd multiple of π.

Up to this point all discussion has admitted the possibility of n phase states, or equivalently that $f_1 = nf_0$, where n is any integer. The elements can thus be used to implement n-state logic. At this point complete generality will be dropped, and we shall proceed to illustrate how these principles can be applied to build up binary logic with $n = 2$. With minor changes in the illustrations an n-state logic can also be realized.

Collecting nomenclature and graphical conventions which have been used, a lexicon of terminology for $n = 2$ is shown in Fig. 13.

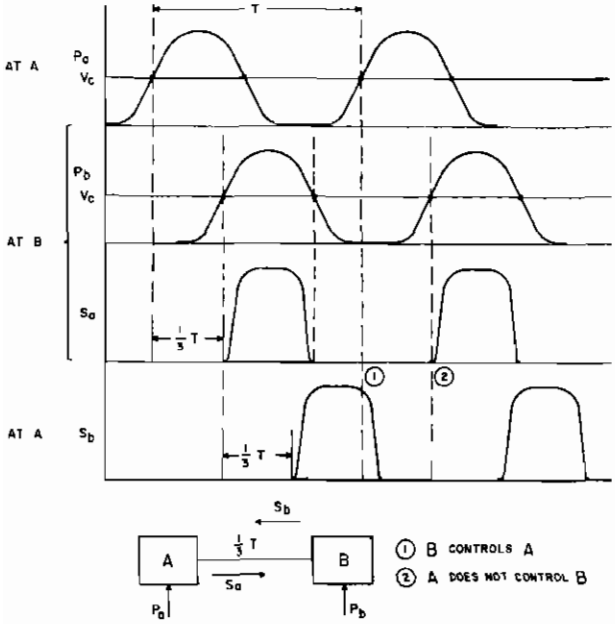


Fig. 12.

MAJORITY LOGIC

The chief value of the aggregates of sub-harmonic generators is that they can be used to perform majority logic. By definition, a majority organ is a device or circuit which has multiple inputs and a single output. The value of the output is the value of the majority of the inputs. To avoid the indeterminate case, there must be an odd number of inputs.

In Fig. 14 the linear addition of signals from three A elements is applied to a B element.

$$\begin{aligned} \text{Let } S_{a1} &= E\cos(\omega_0 t + \Phi_1) \\ S_{a2} &= E\cos(\omega_0 t + \Phi_2) \\ S_{a3} &= E\cos(\omega_0 t + \Phi_3) \end{aligned}$$

where $\Phi_1, \Phi_2, \Phi_3 = 0, \pi$, depending on the state of each A element, and $\omega_0 = 2\pi f_0$, the angular frequency of the sub-harmonic response. Possible results for S_a are:

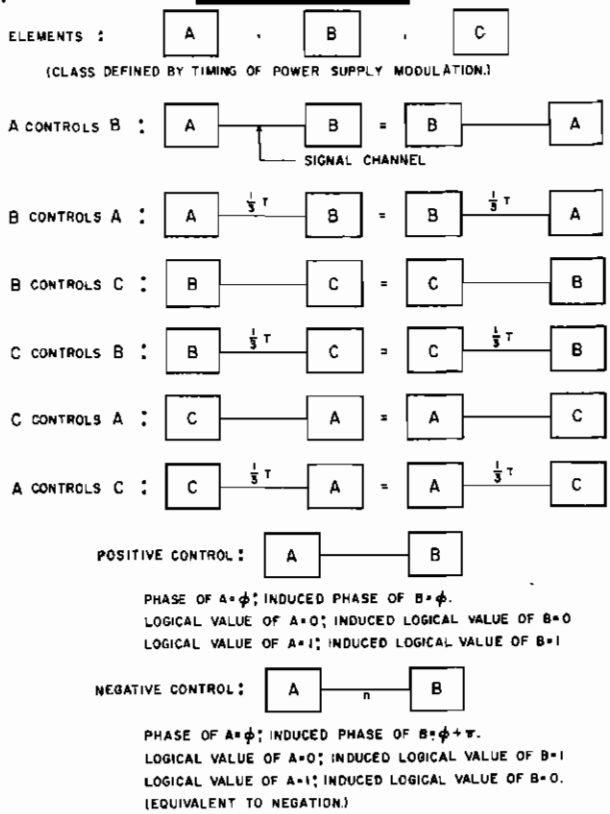


Fig. 13.

$E\cos(\omega_0 t + 0)$	two $\Phi_i = 0$, one $\Phi_i = \pi$
$E\cos(\omega_0 t + \pi)$	two $\Phi_i = \pi$, one $\Phi_i = 0$
$3E\cos(\omega_0 t + 0)$	$\Phi_1 = \Phi_2 = \Phi_3 = 0$
$3E\cos(\omega_0 t + \pi)$	$\Phi_1 = \Phi_2 = \Phi_3 = \pi$.

Since the information is carried in the phase, S'_a has either 0 or π phase depending on the majority of the phases of S_{a1}, S_{a2}, and S_{a3}, and since the phase of S_b is determined by the phase of S'_a, then

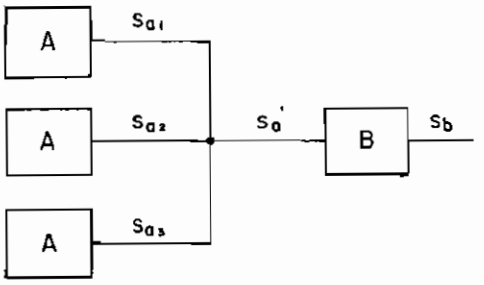


Fig. 14.

$B = \mathrm{Maj}(A_1, A_2, A_3)$. The amplitude variation has no importance. The truth table and equivalent logical expression are as follows, arbitrarily letting $\Phi = 0$ be state "0" and $\Phi = \pi$ be state "1".

A_1	A_2	A_3	B
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

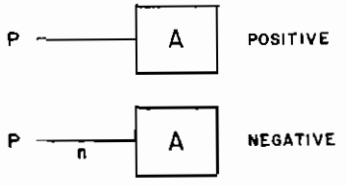
$B = A_1 \cdot A_2 \cdot A_3 + (A_1 \cdot A_4 + A_1 \cdot A_5 + A_1 \cdot A_6)$

WHERE "$\cdot$" IS INTERSECTION,

AND "+" IS CONJUCTION

The majority organ and a negation operation (as shown in Fig. 13) are sufficient to build all logic.

The only thing lacking at this point is a method for putting information into such a system. Permanent sources at the f_0 frequency which are gated on when desired by external controls, fill this need. A permanent source can control any class (A, B, C) of element. There are two possible types of permanent sources:



The reference permanent source p is assumed to have state "1".

By using majority organs, negation, and permanent sources, the elementary logical operations shown in Fig. 15 can be performed. (At this point the separate designation of S_a as being a response of an element, A, will be dropped. The logical state represented by S_a will be called simply the *state* or *binary value* of A.)

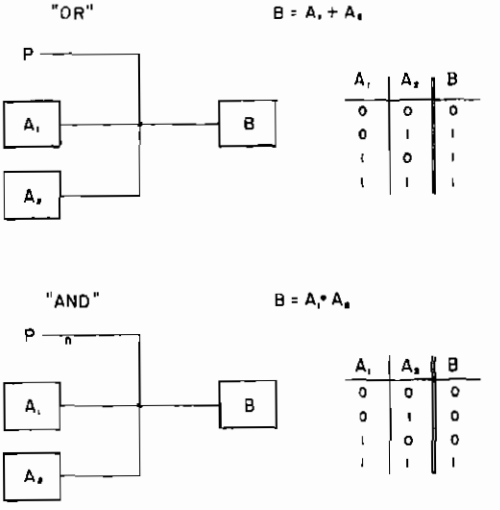


Fig. 15.

The use of the majority organ also allows realization of other non-elementary logical functions. One of its great values is that a single organ can be used to realize many logical operations by what might be called logical biasing. This is shown in Fig. 16.

The above may be generalized in an obvious way to n elements. Also, an n-element "or" circuit differs from the "and" circuit only in having a positive rather than a negative relationship for the permanent sources. One other important aggregate is the "parity" circuit (Fig. 17).

$$B_1 = \mathrm{Maj}(A_1, A_2, A_3) \qquad C = B'_1 \cdot B'_2$$
$$B_2 = A'_1 \cdot A'_2 \cdot A'_3 \qquad A_4 = B_3 + C$$
$$B_3 = A_1 \cdot A_2 \cdot A_3$$
$$\therefore A_4 = A_1 \cdot A_2 \cdot A_3 + \{[\mathrm{Maj}\ (A_1, A_2, A_3)]' \cdot (A'_1 \cdot A'_2 \cdot A'_3)'\}$$
$$= A_1 \cdot A_2 \cdot A_3 + [(A_1 \cdot A_2 \cdot A_3) \cdot (A'_1 \cdot A'_2 \cdot A'_3) + (A_1 \cdot A_2) + (A_2 \cdot A_3) + (A_1 \cdot A_3)]'$$

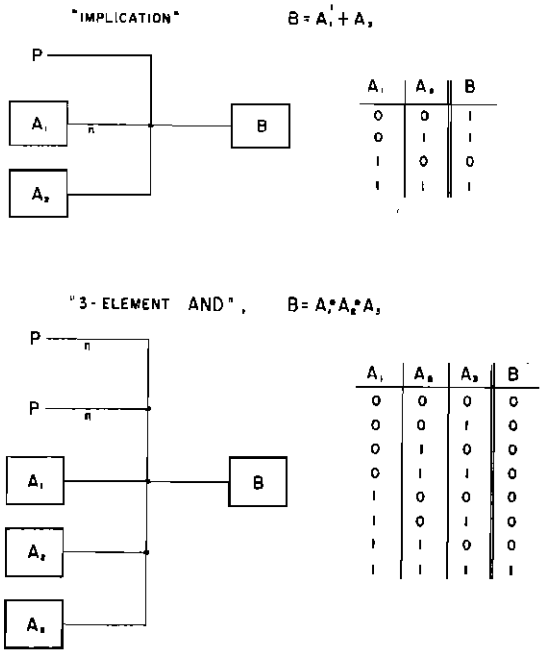


Fig. 16.

As an example of the performance of a specific non-elementary logical operation, we show the majority organ and the parity circuit combined to make one stage of an adder (Fig. 18).

Reviewing what has been discussed: after establishing that the phase of the sub-harmonic response of a "tuned" nonlinear reactance can be used to represent logical states, the processes of negation and majority were shown to arise naturally. From these two operations the basic logical elements "and" and "or" were shown to be possible, along with other more complex logical functions from which can be built all logical operation. The entire discussion was in terms of binary computation, although it can be generalized to n-valued logic. An added attraction of majority logic is that the function of an aggregate of elements can be changed by processes implicit in the programming. For example, an "or" circuit becomes an "and" circuit by shifting the

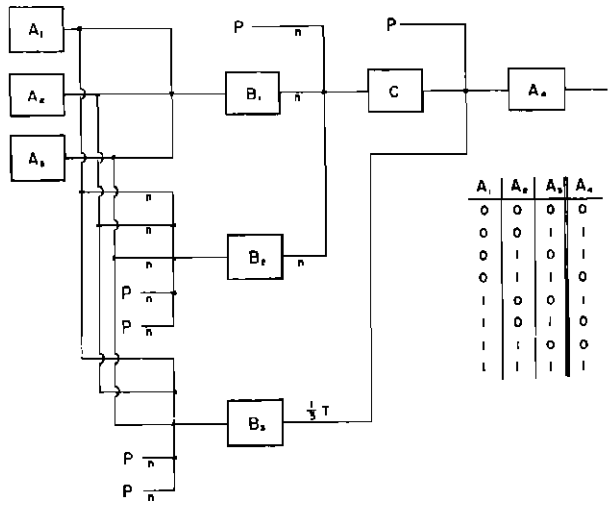


Fig. 17.

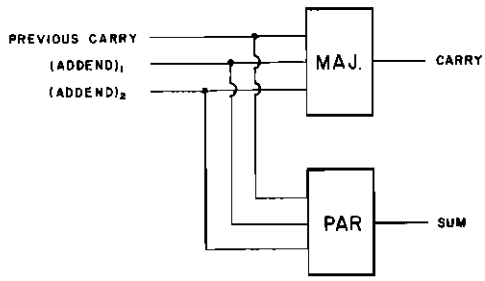


Fig. 18.

phase of the permanent source or, equally, by biasing the specific majority circuit with the output of another element involved in the computation. This provides great flexibility.

SOME PRACTICAL CONSIDERATIONS

A typical sequence of events in a signal channel is illustrated in Fig. 19.

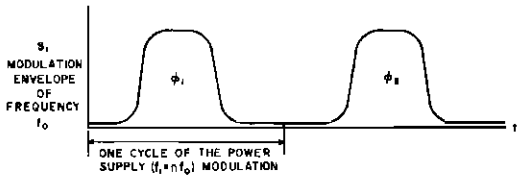


Fig. 19.

This shows a peculiar type of AM-phase-modulated sine wave. Information is represented by phase states Φ_1 and Φ_2, which may be the same or different. The AM has no purpose in the logical processing, and so may be used to monitor the operation of the machine and, in servo-control circuits, to maintain signal levels at the proper average. The phase reference of the entire machine is the phase of the master oscillator supplying or controlling the power-supply signals for each element. The modulation of the power supply determines the basic logical time-cycle.

The modulation envelope of the power supply has been assumed to have time variations that are slow compared to the periods of both f_0 and f_1. To give a numerical example, let the period of the power supply modulation be 50 cycles of f_1 (25 cycles of f_0) in a binary circuit. Reasonable values of f_1 and f_0 are 20 Kmc and 10 Kmc, respectively. The basic computing cycle has therefore, a period of 2.5 mμsec or a clock rate of 400 Mc. The envelope of the modulation of both frequencies is not sinusoidal, but good rectangular pulses are not required. Three harmonics would be sufficient. Thus the modulation envelope would involve frequencies of 400–1200 Mc.

To achieve a computing period of 1 mμsec (a "clock rate" of 1000 Mc) with the above time ratios would require $f_0 = 25$ Kmc and $f_1 = 50$ Kmc. The modulation envelopes would contain frequency components between 1000 and 3000 Mc. For an absolute bandwidth of 2000 Mc, this would be 4% and 8% relative bandwidth at f_1 and f_0, respectively.

Hardware realization of this scheme may well seem outrageous to computer-systems engineers who now are in the transistor age. And it would truly be outrageous in size, cost, and power, with conventional waveguide components at X-band (8.6–12.4 Kmc) and below. The techniques worked out with these conventional, readily available components can be applied to more practical geometries at higher frequencies. Higher frequencies of course have bad characteristics, such as high transmission attenuation, extreme precision requirements, and the lack, at present, of a complete line of components. These are things that must be overcome.

Von Neumann, who played the leading role in the birth of the modern electronic computing machine, has, in these ideas, made another great contribution to the field. Whether this contribution will have as much importance as his original efforts can be decided only after the technology for implementing the sub-harmonic response scheme has been more fully worked out. At this point the prospects look good.

Author's note—The Japanese have developed a sub-harmonic oscillator computer based on nonlinear inductance which uses the same phase script for information representation and majority logic schemes as represented in the von Neumann ideas described in this paper[6]. The basic circuit, called the Parametron, uses RF frequencies of 1 and 2 Mc and has a computing rate of 10 Kc. These two efforts are almost identical in concept, although far different in the speed of the suggested implementation, and from available records they seem to have been proposed in the same year, namely 1954, but there is no known direct connection between them.

[6] Saburo Muroga, "Elementary Principle of Parametron and Its Application to Digital Computers," *Datamation*, Vol. 4, No. 5, pp 31-34; Sept/Oct 1958.