A8: Metrology for Interconnects and Packaging in High Speed Electronics

Accurate Experimental Characterization of On-Chip Interconnects

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In this paper we examine different approaches to the extraction of frequency dependent line parameters from broadband S-parameter measurements. We fabricated several test structures with a geometry typical of high-speed digital interconnects on wafers with substrate resistivities in the range of 0.015 .. 1.5 Ω-cm.

The cross-section of the test structures consists of a signal line with typical widths of 2 µm, 10 µm and 50 µm and two 20 µm wide ground rails. These grounds are connected through a 0.5 µm thick oxide layer to the silicon substrate by a continuous 10 µm wide ohmic contact. The signal line as well as the grounds are connected to 50 µm by 50 µm pads suitable for on-chip measurements in the frequency range up to 40 Ghz.

The geometry of the structures made it possible to apply the methods described in the references [1]-[3]. The method of [1] determines the characteristic impedance Z_0 and the propagation constant γ by comparing the S-parameters measured by probe tip calibration to those of an ideal transmission line. A separate measurement of the contact-pads is necessary to account for the pad parasitics. The experimental results show that the method of [1] is very sensitive to errors in the measurement of the particular line under consideration. Another drawback is that additional open pad structures have to be designed for the deembedding of the pad parasitics.

In contrast to [1] the method of [2] employs a calibration comparison technique for reducing the sensitivity of the measured characteristic impedance to the electrical parasitics of the contact pad. First a multiline TRL probe tip calibration with a reference impedance of 50 Ω is performed in a set of easily characterized reference lines. Then a second-tier multiline TRL calibration in the transmission lines of interest determines "error boxes" which contain the pad parasitics as well as an impedance transformation from 50 Ω to Z_0, the reference impedance of the second-tier calibration. Since the measurement data from different line lengths are used the method of [2] is much less sensitive to errors than the method of [1]. Additionally, there are no separate structures required in order to account for the pad parasitics. This method yields accurate results on substrates with low conductivity. However, it is not very well suited for highly conductive substrates.

Reference [3] suggests a different treatment of the error boxes determined by [2]. This newly developed approach works well in the presence of very large contact pad parasitics as long as pad capacitance and conductance are the dominant sources of error. The experimental results show that this method is well suited for transmission lines built on substrates with very different conductivities. It clearly outperforms the methods of [1] and [2] and is thus applicable to transmission line characterization in CMOS technology as well as in RF industry.

References

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