

# On-Wafer Impedance Measurement on Lossy Substrates

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## Abstract

This paper introduces a new method for measuring impedance parameters in transmission lines fabricated on lossy or dispersive dielectrics. The method, which uses an independent calibration to provide an impedance reference, compares well with conventional techniques when applied to lossless substrates. The effectiveness of the technique is illustrated for resistors fabricated on lossy silicon substrates.

## Introduction

In this letter, we introduce a new on-wafer calibration procedure that measures impedance parameters in transmission lines fabricated on lossy or dispersive dielectrics. Until now, such measurements have been limited to lossless, dispersionless dielectrics. Regardless of substrate, the TRL method provides an accurate calibration for measuring on-wafer scattering parameters at a reference plane in the transmission line. It cannot, however, provide impedance parameters unless the reference impedance, which is equal to the characteristic impedance  $Z_0$  of the line standard, is known [1]. A method for the measurement of  $Z_0$  on lossy, dispersive dielectrics is introduced in [2]. In this paper we apply the method of [2] to the construction of a calibration suitable for the measurement of impedance parameters on lossy dielectric substrates. We illustrate the calibration on low-loss sapphire and quartz substrates and on lossy semiconducting silicon substrates.

Alternative calibrations, such as open-short-load-thru (OSLT) and line-reflect-match (LRM), require a knowledge of the impedance parameters of lumped-element standards. The accuracy with which these parameters are known is questionable, even on lossless dielectrics [3]. On lossy dielectrics, the electrical properties of lumped-element standards are even more difficult to calculate. As shown in this letter, the impedance of a “simple” lumped resistor on silicon may be complicated. As a result, calibrations based on a known resistive “match” are unreliable.

The new lossy-line calibration begins with a determination of  $Z_0$  of coplanar waveguide (CPW) lines using the method we described in [2] and [4]. In this method  $Z_0$  is determined by comparing a TRL calibration in the lossy lines to a reference calibration of known reference

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impedance. Subsequently we can move the reference plane of the lossy-line calibration to any desired location and reset its reference impedance to  $50 \Omega$ . We can also use  $Z_0$  to determine impedance parameters of devices embedded in the lines [1].

In principle, a comparison to any probe-tip calibration with known reference impedance will approximate  $Z_0$ . In our experiments, we compared to a TRL calibration based on lines fabricated on a low-loss gallium arsenide (GaAs) substrate. In this case, the reference impedance can be accurately and straightforwardly determined by the method of [5]. The geometry of these lines was identical to that of the lossy lines. We determined the capacitance of the lines required by [5] from a resistor [6]. For the comparison, we reset the reference impedance of the GaAs calibration to  $50 \Omega$  and moved both calibration reference planes to a location  $25 \mu\text{m}$  from the physical beginning of the CPW lines.

### Comparison to the Conventional Method

The conventional method of [5] is applicable to nondispersive low-loss substrates. We tested the lossy-line calibration by comparing it to the conventional method on sapphire and quartz, where the conventional method is applicable. Figure 1 plots the upper bound [4] on  $|S_{ij} - S'_{ij}|$  for  $ij \in \{11, 21, 12, 22\}$ , where  $S_{ij}$  is the S-parameter of any passive device measured by the conventional calibration [5] and  $S'_{ij}$  is the S-parameter of the same device measured by the lossy-line calibration. Plotted in dashed lines is this upper bound for two nominally identical GaAs calibrations performed at the beginning and the end of the experiment. These two GaAs calibrations differ primarily due to instrument drift and contact errors. The figure shows that, at least in these experiments on quartz and sapphire, the differences between the lossy-line calibration and the conventional calibration are on the order of the instrument drift and contact errors.

### Measurements of Resistor Impedance

We applied the lossy-line calibration to the measurement of resistors embedded in CPW lines fabricated on sapphire, quartz, and silicon substrates. We chose resistors because their measured impedance is sensitive to errors in the calibration reference impedance and because we could compare the measurements to predictions from a simple model [3].

The real and imaginary parts of the resistor impedances measured by the lossy-line calibration are plotted in Fig. 2 and Fig. 3, respectively, and are identified by solid lines with hollow markers. For comparison, their measured dc resistances are marked with arrows on the left edge of Fig. 2. On the sapphire and quartz substrates, we were able to compare these results to measurements using a convention calibration. These measurements are indicated by solid lines with solid markers in the figures. In these two cases, the results are nearly identical.

The figures also plot, in dashed lines, the predictions from the model of [3], which includes a series inductance and a shunt capacitance. We assumed that the series inductance of the resistor is independent of the substrate. We anticipated that the substrate would affect the shunt capacitance

just as it affected the capacitance and conductance of the CPW lines. Therefore we calculated the shunt capacitance  $C$  of the resistor from  $C = (C_\ell / C_\ell^G) C_r^G$  and its shunt conductance  $G$  from  $G = (G_\ell / C_\ell) C$ , where  $C_\ell$  and  $G_\ell$  are the capacitance and conductance per unit length of the CPW line determined from the method of [2],  $C_\ell^G$  is the capacitance per unit length of the GaAs CPW line [6], and  $C_r^G$  is the capacitance used in the model [3] for a resistor of the same geometry fabricated on a GaAs substrate. Although there are some discrepancies, the resistor measurements from the lossy-line calibration agree fairly closely with the model, even for the resistor on the silicon line of highest conductivity.

## Conclusion

The measured resistance of the resistor fabricated on the silicon substrate of highest conductivity drops sharply with frequency to a value about  $6 \Omega$  lower than its dc resistance. Its measured reactance also attains a surprisingly large negative value of about  $-3 \Omega$  at about 500 MHz before increasing again and approaching the linear behavior of the other resistors. An examination of the resistor model indicated that these unexpected results were related to substrate effects.

The complicated electrical behavior of our resistor illustrates the importance of careful measurement on lossy semiconducting substrates and the difficulty of developing accurate lumped-element LRM and OSLT calibrations. The surprisingly large effect of the substrate on the electrical characteristics of the resistor also suggests that even the small contact pads we use for our wafer probes might significantly affect the calibration.

## References

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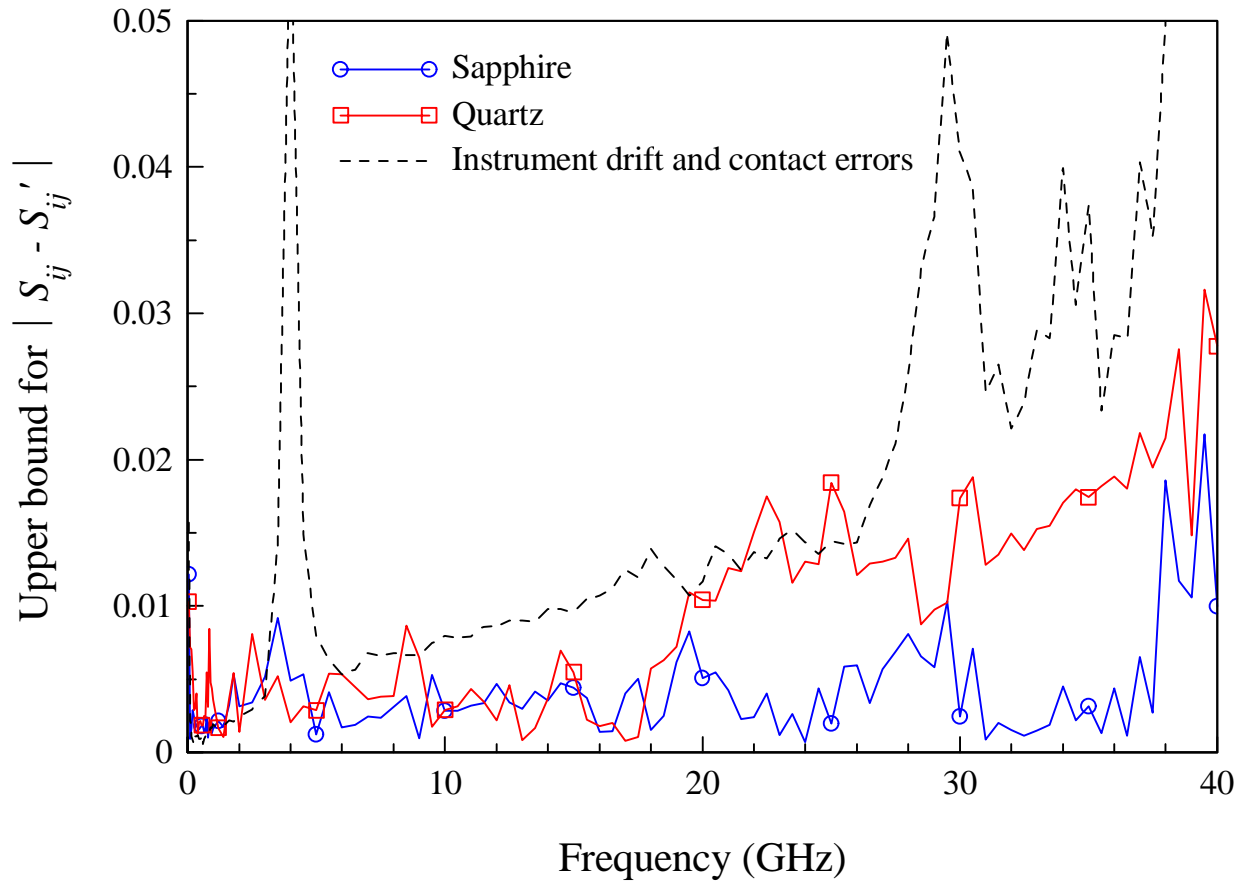


Figure 1. The upper bounds on measurement differences between the lossy-line calibration and conventional calibration (solid lines) are compared to the upper bound on instrument drift and contact errors (dashed line) during the experiment. c:\ep\silicon\ver.plt

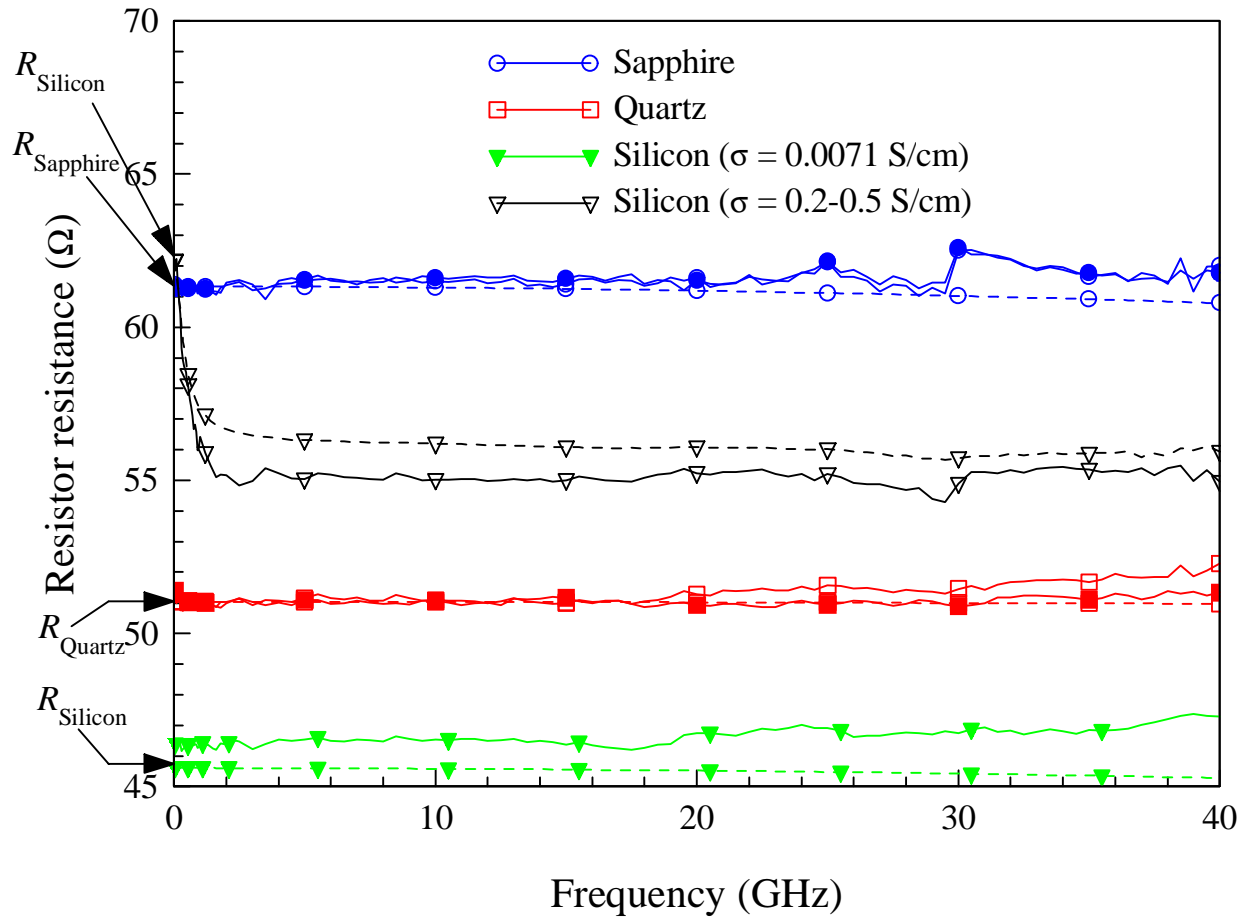


Figure 2. The resistance of small thin-film resistors embedded in CPW lines fabricated on quartz, sapphire, and silicon substrates. Measurements from the lossy-line calibration are indicated by solid lines with hollow markers. Measurements from the convention calibration, when that calibration was applicable, are indicated by solid lines with filled markers. Predictions from the model are indicated by dashed lines. The dc resistances of the resistors are indicated by the arrows on the left side of the plot. For the silicon substrate marked by diamonds, we measured the substrate conductivity  $\sigma$  at dc. For the most lossy silicon substrate marked by triangles, the  $\sigma$  listed in the legend was quoted by the manufacturer. c:\ep\silicon\real.plt

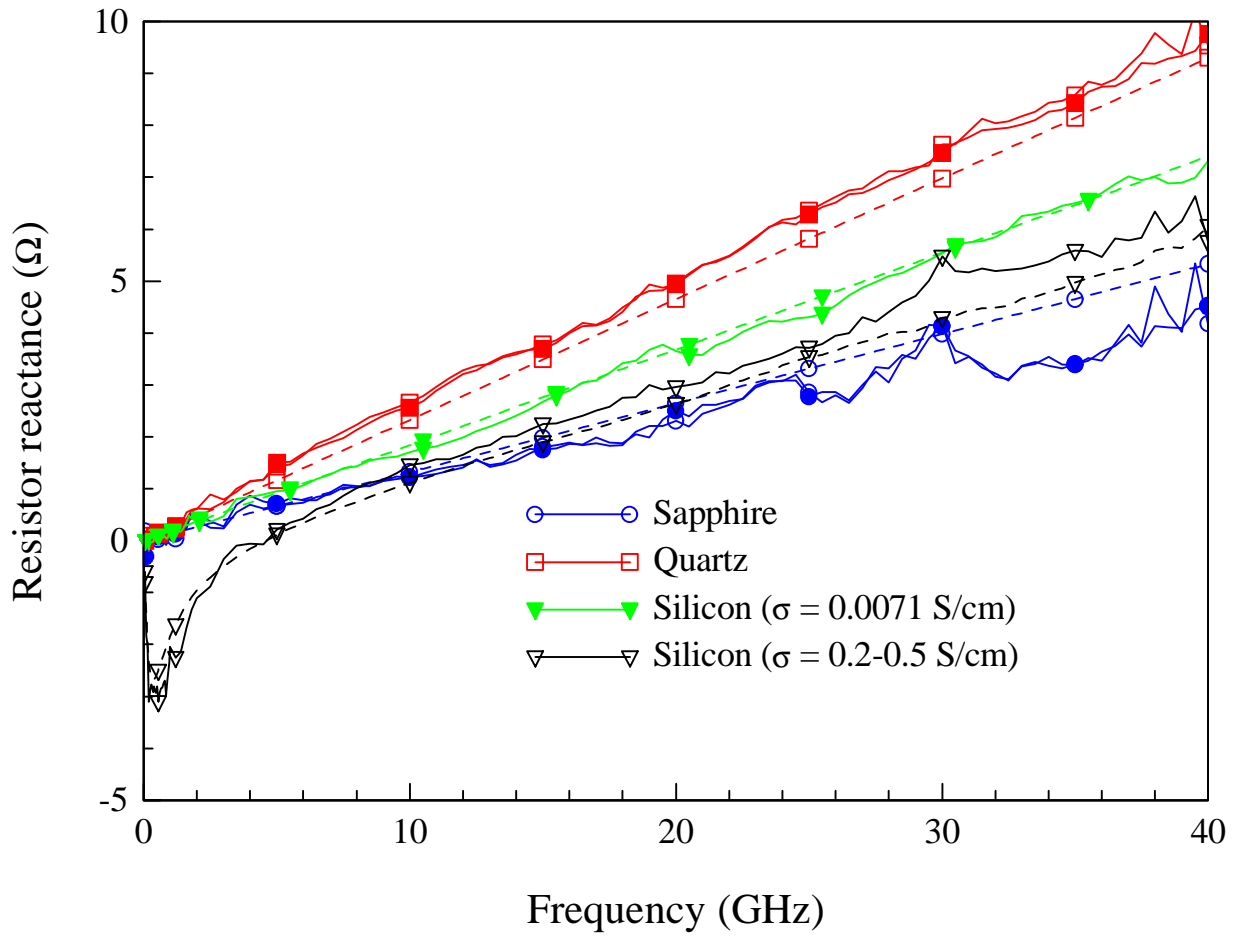


Figure 3. The reactances of the resistors of Fig. 2. c:\ep\silicon\imag.plt