Contact-Pad Design for High-Frequency Silicon Measurements

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***Abstract*- We measure and compare the electrical parasitics of contact pads of different designs fabricated on silicon integrated circuits and develop a strategy for reducing the parasitics.**

INTRODUCTION

We used an on-wafer probe system calibrated with the multiline thru-reflect-line (TRL) probe-tip calibration [1] to measure the capacitance and conductance of contact pads fabricated on silicon integrated circuits. A comparison of the pad's electrical parasitics suggests a design strategy for reducing pad capacitance and conductance, and thereby improving the accuracy of high-frequency on-wafer silicon device measurements. We will show that this strategy, which consists of maximizing the thickness of the oxide layer under the pads, breaking design rules to minimize pad area, and blocking the "field implant" below the signal contact, can reduce pad parasitics by over a factor of two.

CALIBRATION PROCEDURE

We calibrated our on-wafer measurement system with the multiline TRL algorithm of [1]. The standards consisted of a 550 µm long coplanar waveguide (CPW) thru line, five longer lines of lengths 2.685 mm, 3.75 mm, 7.115 mm, 20.245 mm, and 40.55 mm, and two shorts offset 225 µm from the beginning of the line, all fabricated on a semi-insulating gallium arsenide substrate. The CPW had a center conductor width of 64 µm separated from two 261.5 µm wide ground planes by two 42 µm gaps. We set the calibration reference plane to a position 25 µm in front of the physical beginning of the lines and set the reference impedance to 50 Ω using the method of [2].

We began by investigating some of our contact pads, which we fabricated on a silicon wafer, using a two-tier measurement procedure. In this procedure, the reference plane of the first-tier calibration was placed in the CPW transmission lines, as described above. The reference plane of the second-tier calibration was located in a 6 µm wide microstrip line attached to the contact pads fabricated on the silicon substrate. The signal line of this microstrip line was fabricated in the second level of metal

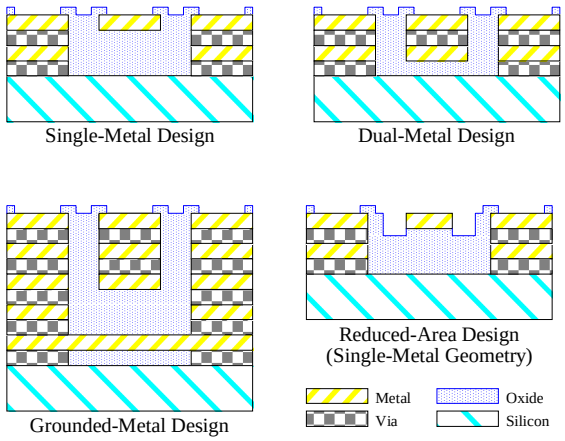

Fig. 1. Cross sections of the designs investigated in this work.

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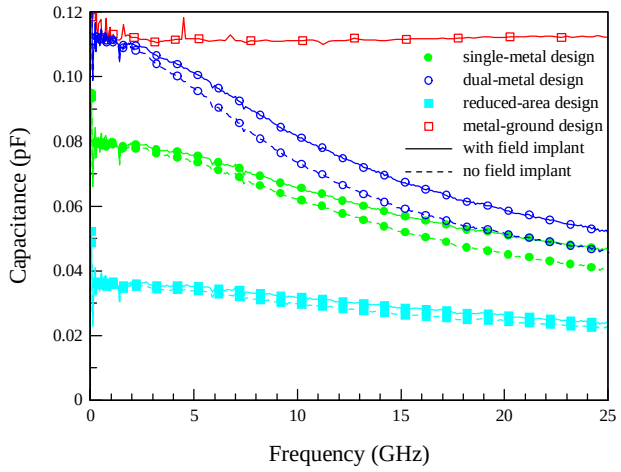

Fig. 2. Pad capacitance.

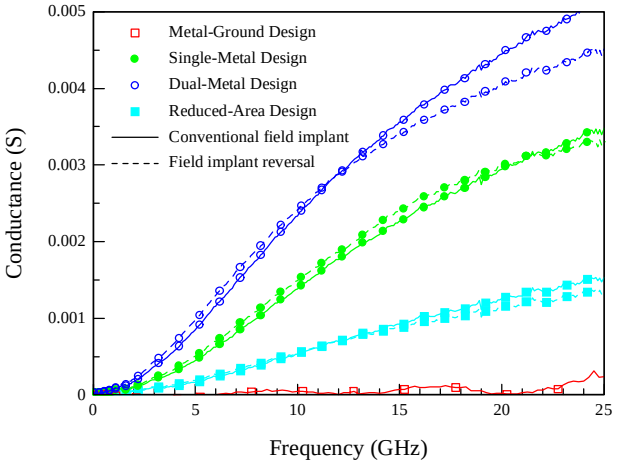

Fig. 3. Pad conductance.

(metal 2), and its ground plane was fabricated in the first level of metal (metal 1). This allowed us to directly measure the scattering parameters of the contact pads we had fabricated on the silicon wafer. This investigation showed that the electrical parasitics of the contact pads fabricated on the silicon wafer were dominated by their shunt capacitance and conductance.

After determining that inductance and resistance could be neglected in our study, we focused on determining the admittance of our silicon contact pads. We found that we could measure that admittance more accurately by directly contacting open pads that were not connected to a microstrip line. Then we calculated the capacitance C and shunt conductance G of the pads from their open-circuit admittances.

CONTACT-PAD MEASUREMENTS

Figure 1 contains cross sectional views of our contact pads. The single-metal, dual-metal, and reduced-area designs were fabricated in a commercial 2-metal-level CMOS process. The grounded-metal design was fabricated in a 5-metal-level CMOS process at a different foundry. Figures 2 and 3 compare our measurements of the capacitance C and conductance G of our contact pads, while Fig. 4 compares their total admittances.

SINGLE- AND DUAL-METAL DESIGNS

We fabricated our single-metal and dual-metal designs with a standard 60 µm by 60 µm contact pad recommended by the manufacturer of the microwave probes we used, and observed that the capacitances of our single- and dual-metal pad designs were nearly equal to the capacitance through the oxide layer at the low frequencies. This is because the doped substrate acts as a ground at low frequencies.

However, as the frequency increases, the capacitances of our single- and dual-metal pad designs dropped off. This is because, at high frequencies, the substrate acts as a lossy dielectric, rather than as a ground. This increases the effective distance to the ground, reducing the overall pad capacitance.

As expected, the pad capacitance and conductance of our single-metal design is much lower than that of the dual-metal designs. This is a consequence of the greater thickness of the oxide separating the contact pad from the substrate in the single-metal design. From this we conclude that the best pad designs use only the top level metal for the signal contact.

REDUCED-AREA DESIGN

We also fabricated pads in the 2-metal-level process with a "reduced area" of 50 µm by 30 µm. The width of these pads was significantly smaller than that recommended by the probe manufacturer. However, we opened large holes in the passivation layer around the pad, as illustrated in Fig. 1. While this large opening in the passivation broke foundry design rules and allowed the passivation etch to attack other oxide layers below it, the large opening also prevented the passivation from interfering with the probe tips. As a result, we were able to reduce the area of the pad well below the 60 µm by 60 µm contact area recommended by the probe manufacturer to obtain repeatable contacts.

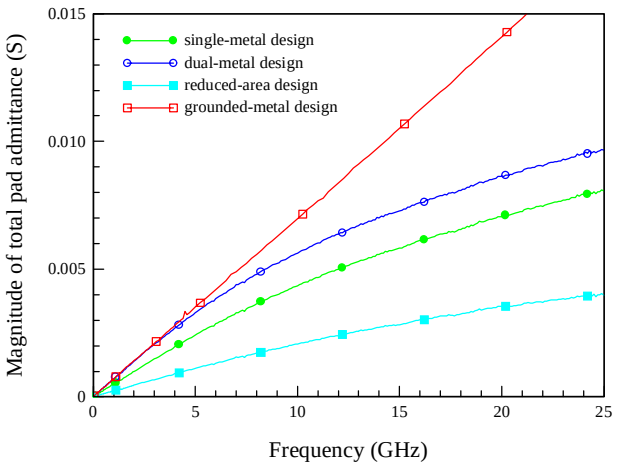

Fig. 4. Total pad admittance (with field implant).

The figures also show that the reduced-area designs have much lower capacitance and conductance than the standard designs. This is not surprising, given the smaller pad area, and is a strong motivation for breaking foundry rules.

FIELD IMPLANT

The two-metal-level foundry process we used employs a field implant between transistors to prevent inversion at the silicon surface. However, it is possible to suppress the field implant with a "block-field-implant" layer. Suppressing this field implant below the signal contact lowers the doping level there, and we speculated that that would decrease the capacitance of our contact pads slightly.

The dashed curves in Figs. 2 and 3 show the pad capacitance and conductance when we used the block-field-implant layer under the signal contact. The data do indicate a slight reduction in pad capacitance and conductance when we suppressed the field implant under the pad.

GROUNDED-METAL DESIGN

We also tested the grounded-metal pad design illustrated in Fig. 1. This structure was fabricated in a different foundry using a five-metal-level process. The signal contact was formed from the top three metal layers (metal 3, metal 4, and metal 5), and had an area of 80 µm by 80 µm. In this design, the lowest level of metal (metal 1) acted as a shield to prevent field penetration into the substrate.

Figures 2 shows that the capacitance of the grounded-metal pad is nearly flat, while Fig. 3 shows that its conductance is nearly 0. This is not surprising, as the pad's capacitance is due entirely to the oxide between the metal 1 and metal 3 layers.

At high frequencies, it is the pad's capacitance, not its conductance, that dominates the pad's parasitics. Figure 4 confirms this, showing that the total admittance of the grounded-metal design is larger than that of any of our other designs. Thus we see that the grounded-metal design is not suitable for high-frequency measurements. This is because the oxide layer between the signal pad and ground is thinner than it need be, and we cannot take advantage of the decrease in capacitance at the high frequencies typical of the single-metal designs. In fact, we estimate that we could have reduced the total admittance of our grounded-metal design by a factor of over 10 at the

low frequencies, and an even greater amount at the high frequencies, if we had used a single-metal reduced-area design in the same technology.

CONCLUSIONS

This work shows that contact-pad capacitance and conductance can be reduced significantly by using a single-metal reduced-area design in which the field implant has been blocked. These designs minimize pad capacitance by minimizing the area of the signal contact and maximizing the oxide thickness under the signal contact. However, the reduced-area design requires breaking the design rules of both the probe manufacturer and the foundry.

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