Line-Reflect-Match Calibrations with Nonideal Microstrip Standards[1]

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***Abstract*- We apply a previously developed Line-Reflect-Match (LRM) calibration that compensates for the nonideal electrical behavior of the match standard to microstrip transmission lines and investigate impedance definitions, standard parasitics, and calibration accuracy.**

INTRODUCTION

This paper applies the line-reflect-match (LRM) calibration method of [1] for nonideal calibration standards to microstrip lines. That method was developed to reduce the size of the calibration set without sacrificing measurement accuracy and was subsequently demonstrated in coplanar waveguide. The method uses a compact thru-reflect-line (TRL) calibration set consisting of a short line, a line of moderately longer length, and a symmetric reflect to determine the transmission-line characteristic impedance and propagation constant, and also to measure the impedance of an embedded resistor. This information corrects the inherent reference impedance error of an LRM calibration based on the short line, symmetric reflect, and embedded resistor, and translates its reference plane accurately.

Here the method, which is applied to the microstrip line of Figure 1, is used to eliminate the need for probe movement during the calibration and to simplify the calibration from the user's point of view while maintaining high measurement accuracy. The calibration set is fabricated on a calibration substrate with the same process used to fabricate large numbers of small adaptor substrates, which are typically wirebonded to discrete devices to allow direct testing with wafer probes, and duplicate accurately the electrical environment of the device embedded in the circuit. The calibration sets are assumed to contain probe-tip to microstrip transitions electrically identical to those on the adaptor substrates, and

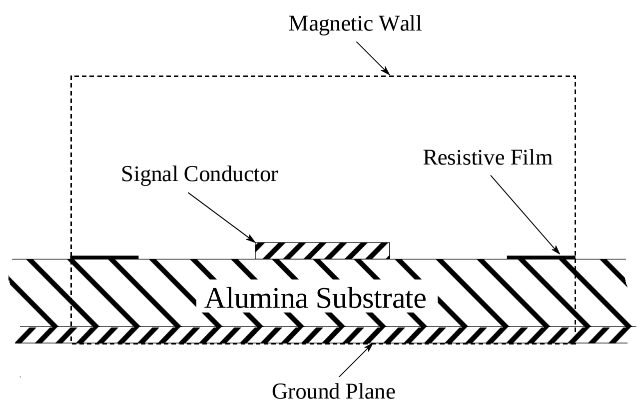

Fig. 1. A cross-sectional view of the microstrip line. The manufacturer specified the gold signal conductor to be nominally 246 μm wide, the polished alumina substrate to be 254 μm thick, and the 180 μm wide 45 $\Omega/\square$ resistive film to be placed 368 μm from the edge of the signal conductor. We measured the thickness of the gold signal line to be 6.3 μm and its dc resistance to be 16.2 Ω/m ($\sim 1.02 \times 10^{-4}$ $\Omega/\square$). We used the values listed above for the calculation of line parameters, assuming in addition a relative substrate dielectric constant of 10 and that the ground plane thickness and conductivity were equal to those of the signal line. For the purposes of the simulation we also surrounded the microstrip line with the 2254 μm high and 1338 μm wide magnetic wall shown in the figure.

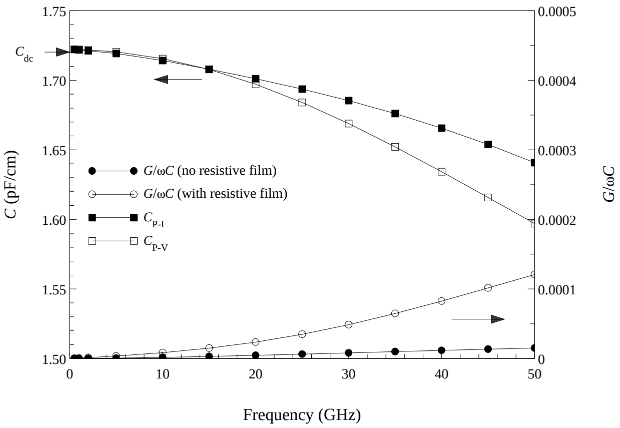

Fig. 2. The microstrip per-unit-length line capacitance C and normalized conductance $G/\omega C$. The arrow on the left marks the measured capacitance of the line at dc.

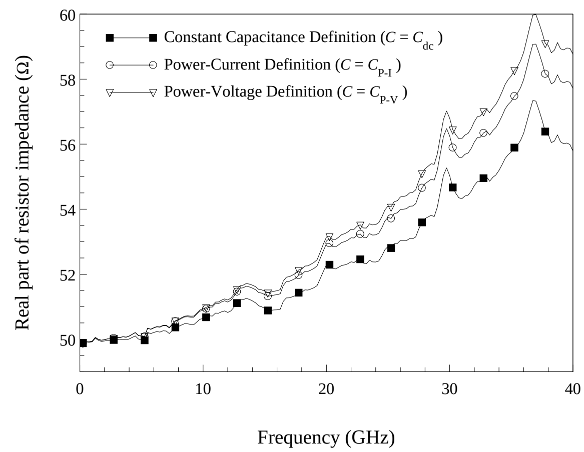

Fig. 3. The resistance of our embedded resistor with respect to three common impedance definitions.

are intended to remove that transition from the measurement, characterizing any parasitics at the end of the microstrip line, any wirebonds that may connect the line on the adaptor substrate to the device, and the device itself.

To apply the method of [1] to the microstrip lines of Figure 1 we will use a 50 Ω multiline TRL calibration [2] to characterize the reactance and frequency dependent resistance of a microstrip match standard. Using this characterization we will translate the reference impedance of an LRM calibration based on this match to 50 Ω and verify its accuracy. Although the method of [1] also allows the reference plane to be translated, that will not be required in the application described here.

TRL CALIBRATION

We performed the initial TRL calibration using the multiline method of [2]. The calibration elements consisted of a 1.219 mm long thru line, three additional microstrip lines with lengths of 1.829 mm, 2.438 mm, and 5.512 mm, and a pair of symmetric opens positioned at the center of the thru line. These lengths, like most of the dimensions given in Figure 1, are the nominal dimensions specified by the manufacturer.

We applied the method of [3] to determine the complex characteristic impedance of the lines, which is also the reference impedance of the TRL calibration [4], from the line's per-unit-length capacitance C and conductance G. The quantity $G/\omega C$ determines its phase, which is a unique property of the line, while C determines its definition dependent magnitude [4].

Figure 2 shows C and $G/\omega C$ calculated for our microstrip lines from the full-wave method of [5]. To calculate these results we first verified that the conductor thickness only has a negligible effect on C and G when both the metal thickness and metal resistivity are scaled by the same factor. We then scaled the conductor and resistor metalization thicknesses to 0.63 nm, scaling the film resistivities appropriately. This was required so that we could incorporate the resistive metal into the calculation, whose high resistivity at greater thicknesses resulted in estimates of the metal mode decay constants of insufficient accuracy for the method of [5].

Figure 2 shows that $G/\omega C$ is small, despite the additional loss due to the resistive film nearby the line, and justifies the assumption $G/\omega C \approx 0$ used by [3] to determine the phase angle of reference impedance. The method of [3] determines the definition dependent magnitude of the reference impedance of the TRL calibration from C: setting $C=C_{P-V}$, the line capacitance in the power-voltage definition, or $C=C_{P-I}$, the line capacitance in the power-current definition, results in impedance measurements with respect to the power-voltage or power-current definitions, respectively. Setting $C=C_{dc}$, its dc value of 1.72 pF/cm measured from a load by the method of [6], results in yet a third definition, which we will call the constant capacitance definition. The figure plots C_{P-V} and C_{P-I}, and compares them to C_{dc}; the variation of C_{P-V} and C_{P-I} with frequency is considerably larger than that for the coplanar

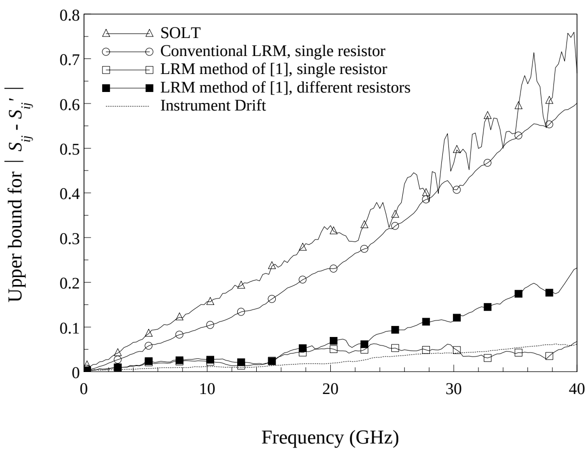

Fig. 4. Bounds for calibration errors.

waveguides discussed in [3]. To obtain what we hoped would be the best approximation for $C_{\text{P-V}}$ and $C_{\text{P-I}}$, we fitted the calculated capacitances of Figure 2 to a quadratic, and then fixed the constant term to correspond to the measured value C_{dc} marked at the left of Figure 2, with the result $C_{\text{P-V}} \approx C_{\text{dc}}\,(1\text{-}3.47{\times}10^{-4} f\text{-}2.3{\times}10^{-5} f^2)$ and $C_{\text{P-I}} \approx C_{\text{dc}}\,(1\text{-}3.9{\times}10^{-4} f\text{-}1.11{\times}10^{-5} f^2)$, where f is the frequency in GHz.

Figure 3 plots the real part of the impedance of our embedded resistor measured with respect to the three impedance definitions; its quadratic dependence on frequency is consistent with that predicted by the planar resistor model of [7]. While this impedance is sensitive to differences in the three definitions, the figure shows that these differences are in fact not large when compared to the overall precision of the measurements. For this reason, we chose the simplest choice, the constant capacitance definition, which is also the choice of [3], in what follows. Impedances with respect to any other definition are calculated from those of the constant capacitance definition by multiplying by C_{dc}/C, where C is the line capacitance with respect to the desired definition.

SOLT AND LRM CALIBRATIONS

We used the calibration comparison method of [8] to test the accuracy of a short-open-load-thru (SOLT) and a conventional LRM calibration [9], both based on the microstrip thru line and embedded opens, shorts, and resistors. The SOLT calibration used standard definitions provided by the supplier of the calibration substrates. The LRM calibration assumed that the resistor was ideal (that is, that its impedance was equal to its dc resistance) and used the embedded opens as the reflect standard. We compared these calibrations to the multiline TRL calibration with 50 Ω reference impedance described above which, based on the theoretical and experimental results of [3] and [4], we believe to be accurate. The comparison determines an upper bound for $|S_{ij}'\text{-}S_{ij}|$ for measurements of any passive device, where S_{ij} is its S-parameter measured with respect to one calibration and S_{ij}' is its S-parameter measured with respect to the other: the bound is obtained from a linearization which assumes that the two calibrations are similar to first order.

Figure 4 plots the bounds, which are large at high frequencies. We also compared two consecutive multiline TRL calibrations using identical standards performed before and after the experiment in order to assess the limitations on calibration repeatability due to contact error and instrument drift. The result, plotted as a dashed line in Figure 4, roughly indicates the minimum deviation between any pair of calibrations. This result is much smaller than the same bound for the SOLT and conventional LRM calibrations, showing that they may introduce large systematic errors into the measurement.

LRM CALIBRATION WITH REFERENCE IMPEDANCE CORRECTION

The reference impedance of a conventional LRM calibration is equal to the impedance of the resistor standard, usually assumed to be equal to its dc resistance. The method of [1] uses the TRL measurements of the impedance of the resistor standard, which is also the reference impedance of the LRM calibration [4], to reset the LRM reference impedance to the desired value, and thus improve its accuracy. We measured our resistor twice with the TRL calibration, once on each port, and fitted the average of the two measurements to a quadratic, fixing the constant term of the fitted impedance equal to that of the resistor's measured dc resistance. We then used the method of [1] with these fits to reset the LRM reference impedance to 50 Ω. Figure 4 compares the bound on the measurement error of this corrected LRM calibration, labeled with hollow squares, to that bound for the SOLT and conventional LRM calibrations, showing that it is significantly more accurate. In fact, the figure shows that the error of the method of [1] is comparable to that due to contact error and instrument drift in the experiment, at least when the same resistor is used on both ports, indicating that little further improvement in accuracy is possible.

We also applied the method of [1] with a different resistor on port two. This eliminated the need to rotate the calibration substrate to connect the same resistor to each port. Figure 4 shows that this LRM calibration is nearly as accurate as the calibration based on a single resistor. An investigation showed that the additional error was caused primarily by the difference in reactance of the two resistors, and that this difference was in large part due to inaccurate placement of the resistors' via-hole grounds.

CONCLUSIONS

We successfully applied the method of [1] to microstrip lines. While the method requires a prior characterization of the match standard with a TRL calibration, the calibration is considerably simplified from the perspective of the user: only three standards, all of which may be of the same length, are required to obtain accurate broadband calibrations. While the method accommodates different choices of impedance definition, the data showed that the differences were small, despite the relatively thick, high dielectric-constant substrate and high frequency.

We noted that improving the accuracy of via-hole placement would improve the electrical uniformity of the resistors, and that eliminating the resistive film in close proximity to the microstrip line would simplify and render more accurate its electromagnetic model.

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