High Frequency Limitations of the JEDEC 123 Guideline

Dylan F. Williams, *Senior Member, IEEE*
National Institute of Standards and Technology, 325 Broadway, Boulder, CO 80303
Ph: [+1] (303)497-3138 Fax: [+1] (303)497-3122 E-mail: dylan@boulder.nist.gov

***Abstract*- This paper assesses certain systematic high frequency measurement errors inherent in the procedures described in the JEDEC 123 Guideline for Measurement of Electronic Package Inductance and Capacitance Model Parameters.**

INTRODUCTION

This paper uses a circuit simulator to assess some of the systematic high frequency measurement errors inherent in the JEDEC 123 Guideline for Measurement of Electronic Package Inductance and Capacitance Model Parameters [1], which outlines procedures for developing lumped-element circuit models for electronic packaging and was primarily intended for use at lower frequencies. The assessment assumes that the impedance analyzer is perfectly calibrated for each package port and uses a circuit simulator to simulate the JEDEC procedure. The simulation compares the responses of the actual circuit model to the those of the JEDEC model. The assessment method not only reveals the nature of the high frequency limitations of the JEDEC Guideline, but can be used to estimate measurement error from approximate electrical models of the package under test, better defining the range of applicability of the Guideline.

The JEDEC Guideline describes the determination of self and mutual inductances and capacitances of electronic package pins with one or two-port measurements performed at the package periphery. The guideline is quite general, and describes a number of possible procedures.

The most basic of these procedures determines the self and mutual inductances of two pins from two-port impedance measurements at the ends of the pins at the package periphery, while the interior ends of the package pins are wire-bonded to the package paddle, and all other pins are left open. The self and mutual inductances are determined from the elements of the measured impedance matrix; the inductance of the wire-bonds is accounted for by subtracting its impedance from the measured values of self impedance. A similar procedure determines the self and mutual capacitances of two pins from admittance measurements performed with the ends of the pins in the package interior left open, and all other pins wire-bonded to ground. Here the stray capacitance of the open circuits is subtracted from the raw measured self capacitances.

When applied to a single pin, the JEDEC procedure measures only its self inductance and capacitance. A single pin is sufficient to illustrate the high frequency error mechanism inherent in the JEDEC procedure.

In the single pin configuration, the self inductance is determined by measuring the impedance at the near end of the pin with its interior end wire-bonded to the package paddle (ground). Subtracting the wirebond inductance from this measurement yields an approximate value of the pin's resistance and inductance. The pin's self capacitance is determined in a similar way from an admittance measurement.

If we think of the pin as a distributed L-C circuit, or transmission line, we see an immediate high frequency limitation of the method. Once the pin reaches a quarter of a wavelength long, the impedance measured in the shorted configuration becomes infinite, and the impedance measured in the open configuration becomes zero. As a result, the JEDEC measurements predict no transmission, when, in fact, the magnitude of the transmission coefficient is one.

While the JEDEC Guideline warns that the procedure should not be applied for circuits more than a tenth of a wavelength long, it does not discuss how to assess the measurement error, or to apply this tenth-wavelength criteria to lumped connections. This paper will investigate the basic JEDEC procedure outlined above and show how a circuit simulator can be used to estimate its high frequency measurement errors. It will first illustrate ideas by investigating extraction of

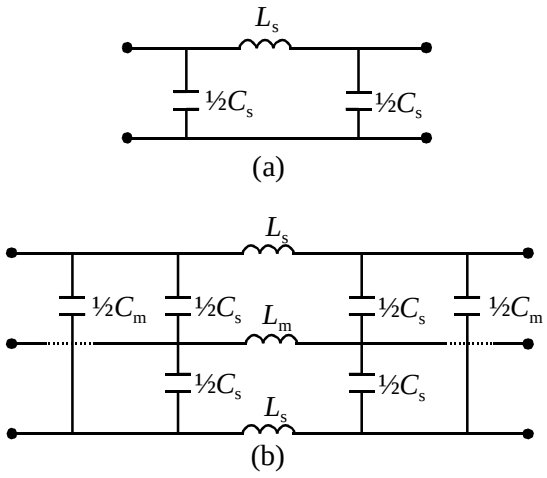

Fig. 1. The one and two pin circuits used to demonstrate the high frequency limitations of the JEDEC procedure. The circuit parameters are from [2].

parameters for a single pin, and then describe how to assess errors with two or greater pins.

SINGLE PIN

We used a commercial circuit simulator to simulate the application of the JEDEC procedure to the characterization of a pin with the equivalent circuit of Fig. 1a with L_s = 6 nH and C_s = 0.6 pF, parameters derived from data presented in [2] and representative of typical packaging parasitics. The JEDEC procedure does not specify how the total inductance and capacitance it measures should be distributed in the JEDEC model, so we also distributed these parameters as indicated in Fig. 1a, placing the entire inductance between two shunt capacitors, each of which had one half of the total capacitance measured by the JEDEC procedure.

Figure 2 compares the reflection and transmission of the JEDEC model to the pin model it is supposed to reproduce. In each case, we assumed different values of wirebond inductances L_w and open circuit capacitances C_o, and subtracted these values from the raw measured self inductance and capacitance, as suggested in the JEDEC Guideline.

The figure shows that the JEDEC model reproduces the circuit response accurately below 500 MHz, but diverges quickly above 1 GHz, even when L_w and C_o are 0. This error arises because the JEDEC procedure ignores the effect of the pin's capacitance on the measurements used to determine its

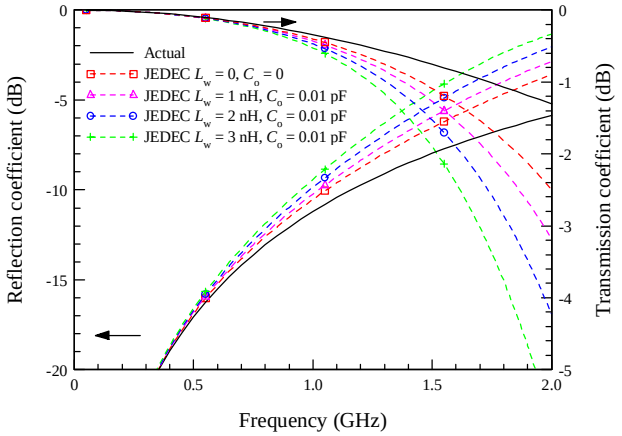

Fig. 2. A comparison of the JEDEC models to the single pin model of Fig. 1a they attempt to emulate.

inductance, and visa versa.

The figure also shows that, even though the JEDEC procedure subtracts L_w and C_o from the measurements, the JEDEC results are sensitive to the actual value of L_w. This suggests a useful rule of thumb: wire bond inductance and open circuit capacitance should be kept to a minimum, even when if they are characterized perfectly and subtracted from the raw measurements.

TWO PINS

Figure 3 illustrates the application of the JEDEC Guideline to the two package pins of Fig. 1b, with L_s = 6 nH, C_s = 0.6 pF, L_m = 2.5 nH, C_m = 0.5 pF, L_w = 2 nH, and C_o = 0.01 pF, realistic parameters from [2]. Figure 4 illustrates the method used to simulate the circuit, which begins with a determination of Z_{ij} and Y_{ij} from measurements at the package exterior, and then assembles the package model from these values. The simulation shows that the errors in the JEDEC results become significant at 1 GHz, and that the JEDEC model extracted from the measurements significantly underestimate the frequency range to which this package might be used.

This simulation approach can be applied to any approximate package model to estimate the frequency range over which the JEDEC procedure is valid. The appendix contains a suitable netlist for analyzing a two-pin circuit. The netlist allows the effects of wirebond inductance and capacitance to be studied, and extension to more pins is straight forward. The netlist may also be used to extract circuit models from JEDEC measurements.

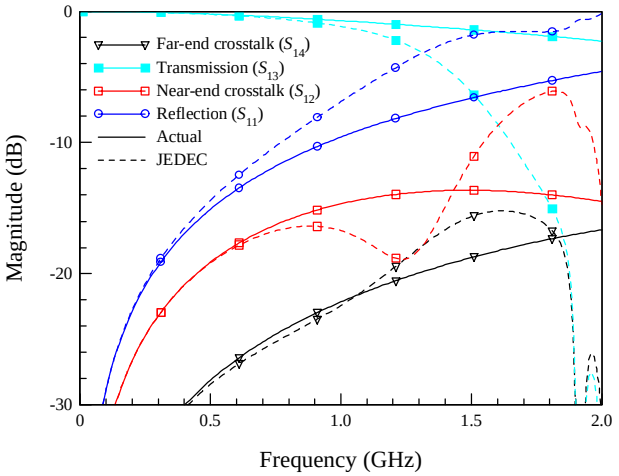

Fig. 3. A comparison between the JEDEC model and the two-pin circuit of Fig. 1b it tries to emulate.

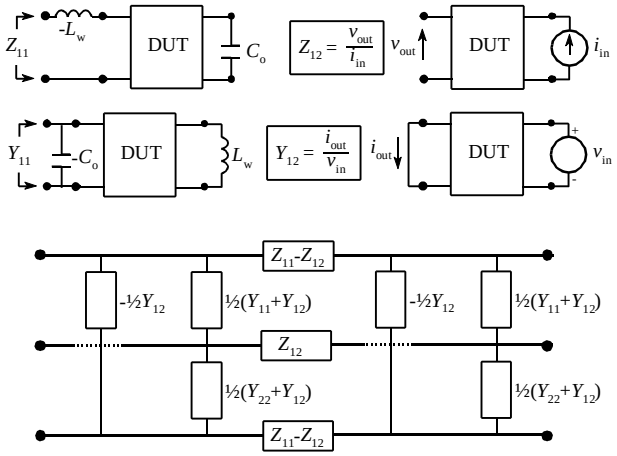

Fig. 4. An illustration of the JEDEC procedure.

DISCUSSION

The basic high frequency limitation of the JEDEC procedure arises because it tries to solve an under-determined system. For example, to describe a single pin requires three complex scattering, impedance, or admittance parameters. However, the JEDEC Guideline only specifies two measurements, which do not contain enough information to determine the three parameters required to describe the circuit.

When enough is understood about the circuit topology, this additional information could be used to reduce the number of required measurements. In this approach a circuit simulator could be used to fit the reduced set of model parameters to the measurements prescribed in the JEDEC Guideline. However, this is a risky proposition: choosing the wrong circuit topology can actually increase measurement error, and independent verification of the accuracy of the topology is difficult.

An better alternative is to perform enough additional measurements to determine all of the electrical parameters describing the circuit. For example, the impedance matrix of a single pin can be determined uniquely by terminating its interior end with an open, short, and resistor, or any other three known impedances using classic two-tier de-embedding methods [3]. Furthermore, it is possible to construct general multiport procedures based on three possible interior terminations [4].

Multiport measurement systems [5] offer another attractive alternative to the JEDEC procedure. These systems are not difficult or expensive to construct, although they may add parallel paths to the ground return that could complicate the measurement of large ground return inductances.

APPENDIX

A Super-Compact [6] netlist for analyzing the JEDEC measurement procedure applied to two package pins. ACTUAL is the approximate two-pin model, WIRE is the wirebond model, and OPEN is the model for the fringing fields at an open pin. This netlist produced Fig. 3. Straightforward modifications extend it to additional ports. The netlist can also be used to extract JEDEC models by reading the raw JEDEC measurements into OPENED and BONDED.

```
*Approximate pin model ACTUAL.
BLK
*Approximate pin model from Fig. 1b.
IND 1 3 L=6NH
IND 2 4 L=6NH
CAP 1 0 C=0.3PF
CAP 3 5 C=0.3PF
CAP 2 0 C=0.3PF
CAP 4 5 C=0.3PF
CAP 1 2 C=0.25PF
CAP 3 4 C=0.25PF
IND 5 0 L=2.5NH
TRF 3 8 5 0 N=1
TRF 4 9 5 0 N=1
ACTUAL: 4POR 1 2 8 9
END
*Open circuit fringe capacitance
BLK
CAP 1 C=0.01PF
OPEN: 1POR 1
*The capacitance subtracted from the raw meas.
*Modify to simulate effect of poor open circuit model
CAP 2 C=-0.01PF
MOPEN: 1POR 2
END
```

```
*Wire bond inductance
BLK
IND 1 L=2NH
WIRE: 1POR 1
*The inductance subtracted from the raw meas.
*Modify to simulate effect of poor wirebond model
IND 2 L=-2NH
MWIRE: 1POR 2
END
*To use netlist to extract JEDEC model from measurements,
*read measurements directly into BONDED and OPENED
*
*Wire-bonded circuit used to find inductances
BLK
ACTUAL 1 2 3 4
WIRE 3
WIRE 4
BONDED: 2POR 1 2
END
*Open circuit used to find capacitances
BLK
ACTUAL 1 2 3 4
OPEN 3
OPEN 4
OPENED: 2POR 1 2
END
*Inverter used to negate impedances
BLK
CCG 3 1 4 0 B=1 R1=1E-10 R2=1E10
VVG 1 3 0 5 M=1 R1=1E10 R2=1E-10
TRF 4 7 5 0 N=1
INVERT: 2POR 1 7
END
*Circuit used to find Y11
BLK
MOPEN 1
OPENED 1 2
WIRE 2
Y11: 1POR 1
END
*Circuit used to find Y22
BLK
MOPEN 1
OPENED 2 1
WIRE 2
Y22: 1POR 1
END
*Circuit used to find Z11
BLK
MWIRE 1 2
BONDED 2 3
OPEN 3
Z11: 1POR 1
END
*Circuit used to find Z22
BLK
MWIRE 1 2
BONDED 3 2
OPEN 3
Z22: 1POR 1
END
*Circuit used to find Y12
BLK
CCG 3 1 0 0 B=1 R1=1E-10 R2=1E10
VVG 1 4 0 0 M=1 R1=1E10 R2=1E-10
OPENED 3 4
Y12: 1POR 1
END
*Circuit used to find Z12
BLK
CCG 1 4 2 0 B=1 R1=1E-10 R2=1E10
VVG 3 2 0 0 M=1 R1=1E10 R2=1E-10
BONDED 3 4
Z12: 1POR 1
END
*Circuit used to find -Z12
BLK
INVERT 1 2
Z12 2
MZ12: 1POR 1
END
*Circuit used to find -(Y12)/2
BLK
INVERT 1 2
Y12 2 3
Y12 3
HMY12: 1POR 1
END
*Create 4-port JEDEC circuit from Zij and Yij
BLK
Y11  1 2
Y12  1 2
Y11  2 0
Y12  2 0
HY11: 1POR 1
END
BLK
Y22  1 2
Y12  1 2
Y22  2 0
Y12  2 0
HY22: 1POR 1
END
BLK
Z11   1 2
MZ12  2 3
Z12   0 4
Z22   7 6
MZ12  6 5
HY11  1 0
HMY12 1 7
HY22  7 0
HY11  3 4
HMY12 3 5
HY22  4 5
TRF   3 8 4 0 N=1
TRF   5 9 4 0 N=1
JEDEC:4POR 1 7 8 9
END
```

REFERENCES

[1] "Guideline for Measurement of Electronic Package Inductance and Capacitance Model Parameters," Electronic Industries Association, EIA/JEDEC Publication no. 123, October 1995.

[2] Y. Qiu, M.K. Iyer, K.C. Chong, T.C. Wong, E. Chong, "Effect of material and interconnect parameters on leaded package parasitics," 2nd IEEE Workshop on Signal Propagation on Interconnects, May 13-15, 1998, Travemunde, Germany.

[3] R.F. Bouer and P. Penfield, "De-embedding and unterminating," IEEE Trans. Microwave Theory and Tech., vol. 22, no. 3, pp. 282-288, March 1974.

[4] J.C. Tippet and R.A. Speciale, "A rigorous technique for measuring the scattering matrix of a multiport device with a 2-port network analyzer," *IEEE Trans. Microwave Theory Tech.*, vol. 30, no. 5, pp. 661-666, May 1982.

[5] D. F. Williams and D. K. Walker, "4-port measurement system," *51st ARFTG Conference Digest*, pp. 88-90, June 12, 1998.

[6] We use trade names to specify the experimental procedure adequately and do not imply endorsement by NIST. Similar products may work as well or better.