Compensation for Geometrical Variations in Coplanar Waveguide Probe-Tip Calibration

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Abstract— **We show how coplanar-waveguide probe-tip scattering parameter calibrations performed in one coplanar waveguide conductor geometry may be adjusted for measurement in another. The method models the difference between the two probe-tip-to-coplanar-waveguide transitions as a change in shunt capacitance and applies previously developed techniques for its determination and compensation. Comparison to accurate multiline Thru-Reflect-Line calibrations verifies the accuracy of the method. Differences in both conductor geometry and substrate permittivity are considered in the comparison. The method requires only a single, compact open stub or thru line fabricated on the measurement wafer.**

Index Terms— **Automatic network analyzers, coplanar waveguide, on-wafer calibration.**

I. Introduction

THIS letter extends the coplanar-waveguide (CPW) scattering parameter (S-parameter) calibration method of Williams and Marks [1], which accounts for differences between the substrate permittivity of calibration and measurement wafers, to account for changes in conductor geometry as well.

The most accurate CPW measurements use an "on-wafer" calibration: the devices under test are embedded in the CPW lines used for the calibration. The on-wafer multiline Thru-Reflect-Line (TRL) calibration [2] is an example. On-wafer calibrations accurately measure S-parameters, however, only when the devices under test are embedded in transmission lines with properties similar to those used in the calibration, limiting their range of applicability.

In practice, many measurements rely on an "off-wafer" calibration: the calibrations standards are *not* constructed on the same wafer as the device under test. The objective of the off-wafer calibration is to perform accurate measurements in the line in which the devices under test are embedded; this requires that it reproduce the on-wafer calibration accurately.

Williams and Marks demonstrate in [1] that differences in substrate permittivity between the calibration and measurement wafers significantly deteriorates measurement accuracy. They show that in CPW lines, the effects of this difference can be modeled electrically by a change in a shunt capacitance at the probe tip. They present methods for determining and compensating for this change, extending the calibration to a wide range of measurement substrates. They also demonstrate that these methods allow the off-wafer calibration to reproduce the on-wafer multiline TRL calibration accurately when the conductor geometries on the two wafers are identical.

Here, we demonstrate that differences in CPW geometry between the calibration and measurement wafers result in similar measurement errors. As was true for a change of substrate permittivity, the effect of these geometrical differences on the probe-tip-to-CPW transition can be modeled electrically by a change in shunt capacitance at the probe tip; the same measurement and correction methods used in [1] apply. We demonstrate that the method accounts accurately for simultaneous changes in both CPW conductor geometry and substrate permittivity. The *only* calibration structure required on the measurement wafer is a single compact open stub or thru line. The method of [3], which demonstrates the characteristic impedance and propagation constant CPW lines, could be used to translate the measurement reference plane, if desired. This requires a thru line, a short length of transmission line, and a symmetrical reflect on the measurement wafer; this is not demonstrated here.

II. Compensation for CPW Geometry

To demonstrate the method we fabricated nine TRL calibration sets on a semi-insulating gallium arsenide substrate. The lines differed only in conductor geometry, as listed in Table I. Each calibration set consisted of a thru line of length 550 μm, four lines of additional lengths 2.135, 3.200, 6.565, and 19.695 mm, and symmetrical shorts offset 225 μm from the beginning of the line.

We performed multiline TRL probe-tip calibrations with each calibration set in the table. We set the reference plane of each calibration to a position 25 μm beyond the physical beginning of the lines and the reference impedance to 50 Ω with the method of [4], determining the capacitance per unit length of each line from physical measurements of the geometries and the CPW model of Heinrich [5].

We will call the calibration based on the first set listed in the table the "reference" calibration, and call the other eight "target" calibrations. Ideally, the reference calibration will reproduce the target calibration in each case; if so, we could use it for accurate off-wafer calibration. As a measure of how well the reference calibration replicates the target calibration, we calculate the upper bound for $|S'_{ij} - S_{ij}|$ using the method of [6], where S'_{ij} are the S-parameters of any passive device measured by the 50-Ω reference calibration, and S_{ij} are the S-parameters measured by the 50-Ω target calibration. The

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TABLE I
CPW CONDUCTOR AND GAP WIDTHS

Calibration set	Center-conductor width (μm)	Gap width (μm)	Ground-plane width (μm)
1*	103*	19*	265*
2	93	29	260
3	83	39	255
4	73	49	250
5	73	49	200
6	73	49	150
7	63	59	245
8	53	69	240
9	43	79	235

*Indicates reference calibration set.

bounds are valid when $|S_{11}| \leq 1$, $|S_{22}| \leq 1$, and $|S_{12}S_{21}| \leq 1$ for $ij \in \{11, 21, 12, 22\}$.

We found a trend toward greater error bound as the geometrical deviation increases. Fig. 1 shows in solid lines the upper bounds for three representative cases (calibration sets 4, 5, and 8 of Table I), chosen so as to have varying degrees of geometrical deviation from the lines of the reference calibration. The figure compares these bounds to the same bound for a calibration performed at the beginning and the end of the experiment, shown as a solid line marked with large dots; it bounds the measurement errors due to drift in the instrument during the course of the experiment [1]. The figure shows that the error made when the reference calibration is used to test devices embedded in lines of the target geometries can significantly exceed those due to instrument drift. We conclude that the uncompensated reference calibration does not reproduce the target calibrations within the precision possible with the instrument, even though their reference impedances are equal.

We examined various electrical models for this residual difference between the reference and target calibrations; as with a change in substrate permittivity, the effects of changes in conductor geometry were best described by a change in capacitance at the probe tip attributable to the change in end-effect and per-unit-length capacitance of the short section of CPW behind the calibration reference plane. Also, using the procedure of [1], we were able to determine the size of these capacitances accurately from measurements of an open stub or thru line in the target geometry, corrected with respect to the reference calibration. Fig. 1 shows in dashed lines the bound on the measurement errors of the reference calibration when used to measure devices embedded in the target geometries of the same three calibration sets, after it has been compensated for the change in shunt probe-tip capacitance in each case. The figure shows that the method of [1] adjusts the reference calibration to reproduce accurately the measurements of the target calibrations. In addition, the

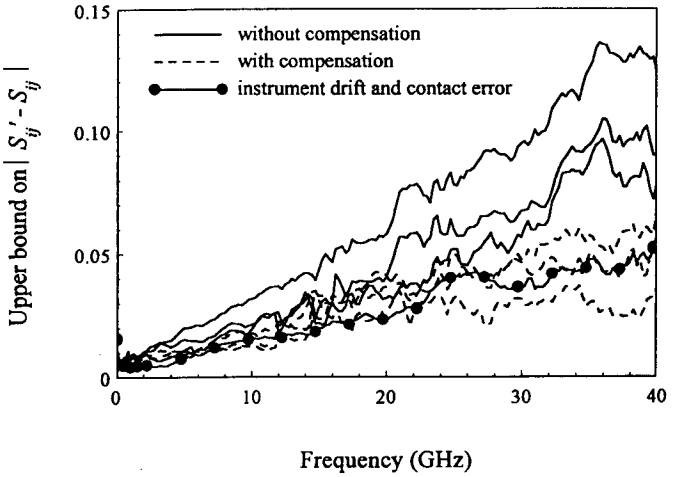

Fig. 1. Comparison between representative upper bounds on measurement differences of the reference and target calibrations, before and after probe-tip capacitance compensation. The bound on errors due to instrument drift is shown for reference.

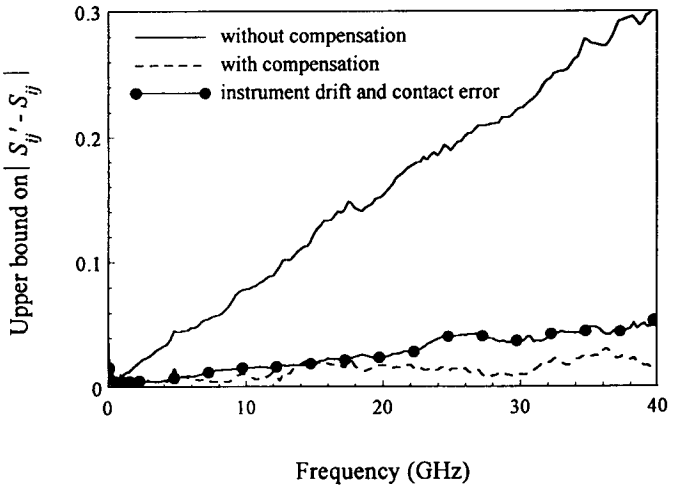

Fig. 2. The upper bound on measurement differences for the reference calibration and a fused silica calibration with differing CPW geometries, before and after probe-tip capacitance compensation. The bound on instrument drift error is shown for comparison.

compensated error bound is independent of the initial, uncompensated bound, indicating that the technique is equally effective for large or small geometrical differences between the lines.

III. CHANGE IN GEOMETRY AND SUBSTRATE

We tested the method on CPW in which both the geometry and substrate permittivity on the calibration and the measurement wafers differed. We used the same 50-Ω reference calibration as before, fabricated on a gallium arsenide substrate ($\epsilon_r \sim 13$), and compared it to a 50-Ω target calibration performed on a fused silica substrate ($\epsilon_r \sim 3.8$) with geometry 4 of Table I (center conductor width of 73 μm, gap width of 49 μm, and ground-plane width of 250 μm). Fig. 2 shows the error bounds for measurements using the reference calibration to test devices embedded in lines fabricated on the fused silica

substrate, with and without probe-tip capacitance compensation. Again, the figure shows that the method of [1] accurately adjusts the reference calibration to measure devices embedded in target lines.

IV. Conclusion

The method of [1] corrects for measurement error caused by differences in either permittivity or conductor geometry between the calibration and measurement substrates. The method comprises an impedance transformation to correct for the change in CPW line characteristic impedance, followed by an adjustment for the change in the shunt capacitance at the probe tip between the two substrates. The method could be used to measure accurately devices embedded in CPW lines on different substrates even when the conductor geometries have been adjusted so that the CPW lines have roughly the same characteristic impedance. The method requires a calibration substrate and only a single, compact open stub or thru line fabricated on the measurement wafer.

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