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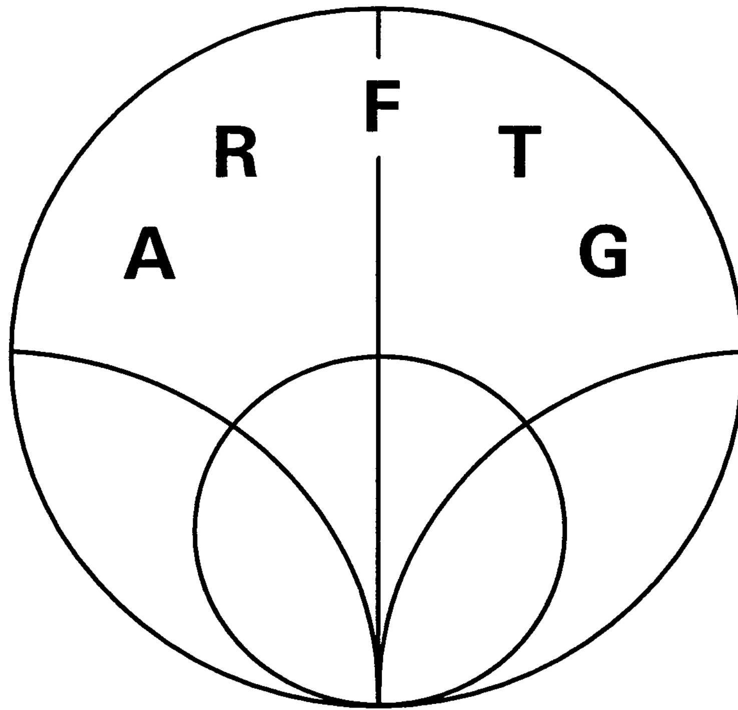

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Compensation for Substrate Permittivity in Probe-Tip Calibration[1]

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Abstract- **We demonstrate a method of compensation for the effect of substrate permittivity on coplanar waveguide probe-tip scattering parameter calibrations, modeling the effect as a capacitance at the probe tip. Comparison to on-wafer multiline TRL calibration verifies its accuracy. The method allows calibration to the probe tip using generic off-wafer standards with accuracy comparable to that of on-wafer calibration.**

INTRODUCTION

This paper develops a simple model accounting for the effect of substrate permittivity on coplanar waveguide (CPW) thru-reflect-line (TRL) probe-tip scattering parameter (S-parameter) calibrations. We model the effect as a small capacitance at the probe tip and apply the model to the prediction and correction of systematic variations between TRL calibrations performed using coplanar waveguide fabricated on different substrates.

The most accurate on-wafer measurements use an on-wafer calibration, in which the calibration standards are constructed on the same wafer and with the same contact structure as the device under test. Since this requires custom standards, many users prefer off-wafer calibration standards, typically using a generic calibration wafer supplied by an outside source. The resulting error depends in detail on the differences between the off-wafer standards and their on-wafer counterparts. Unless this error can be corrected, or at least assessed, off-wafer calibration will be severely limited as an accurate tool and traceability will be impossible.

A previous study addressing this problem [1] demonstrated that the differences between on-wafer and off-wafer calibrations can be moderated by ensuring that, in both cases, the reference plane is located near the probe tip and the reference impedance is adjusted to 50 Ω. These corrections will eliminate virtually all calibration discrepancy due to differences in metal thickness and conductivity, as would be present due to inevitable process variations. However, these same studies showed that differences in *substrate*, even moderate ones, can affect the calibration drastically in a way that cannot be explained by differences in reference plane or reference impedance. As a result, generic probe-tip calibration standards are of limited accuracy for measurements on wafers whose permittivity is dissimilar to that of the standards.

The procedure developed here addresses the problem for coplanar waveguide by accounting for the effect of substrate permittivity on the calibration. The procedure is based on a model of the transition between the analyzer and CPW as a complex but fixed electrical network followed by a small shunt capacitance at the probe tip. The model leads to a description of the error in the measurements of the off-wafer calibration in terms of a residual capacitance; it is similar to that suggested in [2], [3], and [4] to model pad capacitance and to that suggested in [5] to describe the interconnection of coaxial lines of different diameters.

Here we show that, at least for identical CPW line and launch geometries, a capacitance at the probe tip describes well the difference between calibrations performed on substrates of different permittivities. We show that capacitance is, to a good approximation, just that due to the short section of CPW behind the on-wafer reference plane. We develop expressions for accurately estimating that capacitance from either a knowledge of the substrate permittivities or from

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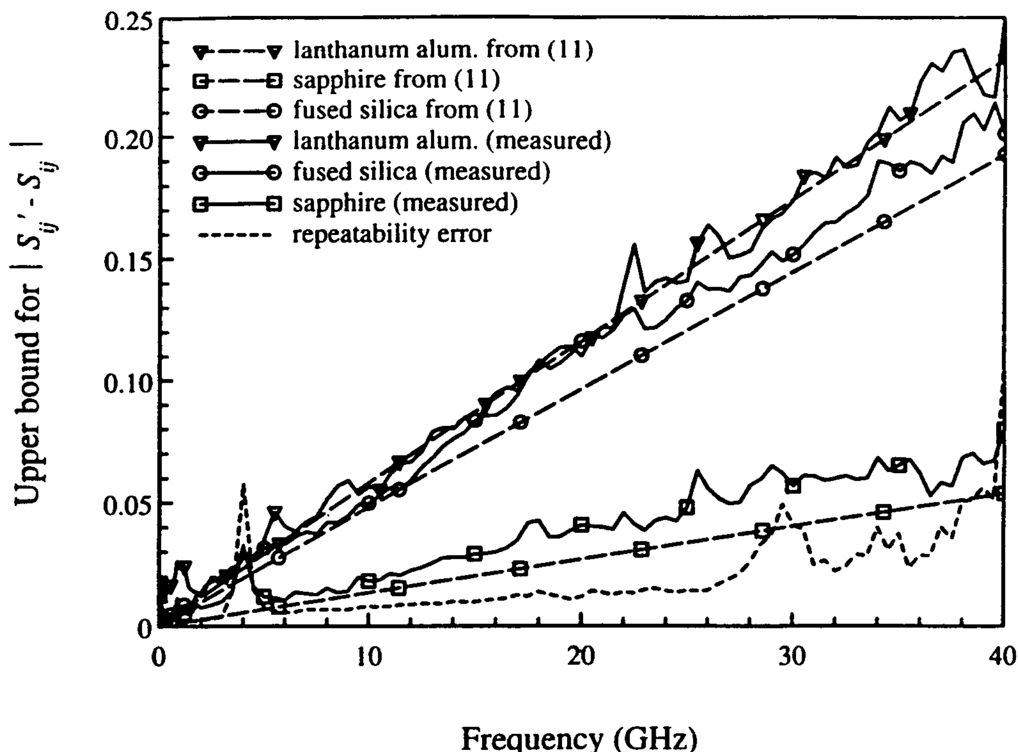

Figure 1. The bounds for differences between measurements of passive devices using the off-wafer GaAs calibrations and the on-wafer fused silica, sapphire, and lanthanum aluminate multiline TRL probe-tip calibrations. The dotted curve corresponds to repeated calibrations with identical artifacts. The dashed curve is the prediction from (11).

measurement. Finally we show how off-wafer calibrations can be modified to accurately characterize on-wafer devices, and we quantify the residual error of the modified off-wafer calibration by comparison to an accurate on-wafer TRL calibration.

Calibration Errors

We used the method of [1] to quantify the differences between on-wafer and off-wafer CPW probe-tip calibrations performed on different substrates. The method measures upper bounds for $|S'_{ij} - S_{ij}|$, where S_{ij} and S'_{ij} are the S-parameters of any passive device measured by the on-wafer and off-wafer calibrations respectively. The off-wafer calibrations use GaAs substrates while the on-wafer calibrations use fused silica, sapphire, and lanthanum aluminate substrates. Otherwise the calibrations are identical. All of the calibrations were performed with the multiline TRL method [6] using calibration artifacts of virtually identical geometry: a CPW thru line 550 μm long, four longer lines of length 2.685 mm, 3.75 mm, 7.115 mm, and 20.245 mm, and two shorts offset 225 μm from the beginning of the line. The lines had a center conductor of width 73 μm separated from two 250 μm ground planes by 49 μm gaps. The calibrations are probe-tip calibrations; that is, the reference planes were set to a position just beyond the physical beginning of the CPW lines (in our case, 25 μm beyond) and the reference impedance was adjusted to 50 Ω. In order to adjust the reference impedance, we determined the characteristic impedance of each line by the method of [7] and the dc capacitance per unit length of each line from a resistor, as in [8]. The bounds, plotted in solid lines in Figure 1, are valid for $ij \in \{11, 21, 12, 22\}$ when $|S_{11}| \leq 1$, $|S_{22}| \leq 1$, and $|S_{12}S_{21}| \leq 1$. Plotted in dotted lines is the bound for two nominally identical GaAs calibrations performed at the beginning and the end of the fused silica and sapphire experiments; these differ primarily due to repeatability limitations such as instrument drift and contact errors. The figure shows that the differences between the off-wafer GaAs and the on-wafer calibrations, plotted in solid lines, are significantly larger than this repeatability error.

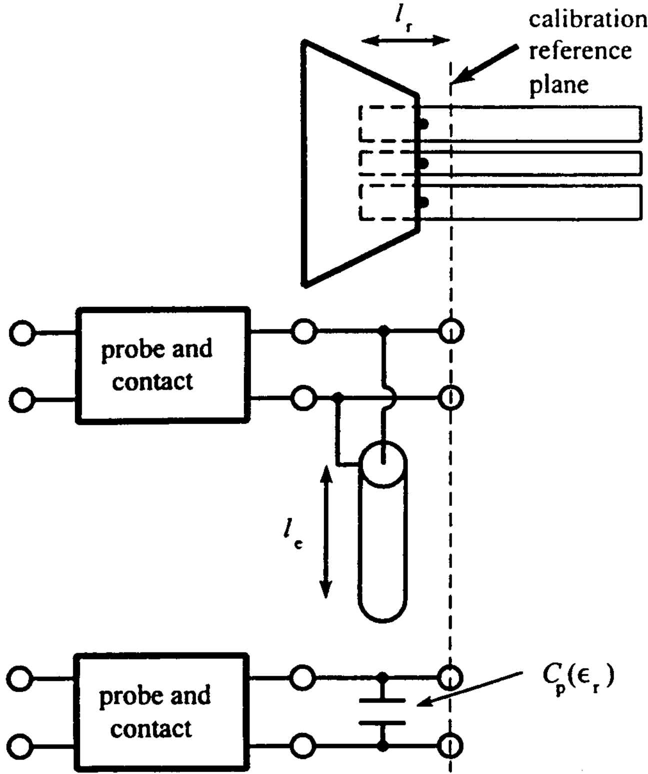

Figure 2. The measurement configuration and two equivalent circuits for the probe and transition to the CPW line.

CAPACITANCE MODEL

Figure 2 shows a simplified diagram of our model of the connection between the analyzer and a coplanar line. The model consists of two elements. The first is a general two-port network, which includes the complicated electrical behavior of the analyzer and probe as well as its interaction with the CPW line, except for that due to a shunt capacitance $C_p(\epsilon_r)$. The second is the shunt capacitance $C_p(\epsilon_r)$. In our model, the network is fixed while the value of $C_p(\epsilon_r)$ depends on the substrate.

In the model, the vector network analyzer measures a transmission matrix M which is expressible as the product

$$M = \left[X_1 \;\; Y(C_p(\epsilon_r))\right] \; T \; \left[Y(C_p(\epsilon_r)) \;\; X_2\right]. \qquad (1)$$

Here T is the cascade matrix of the device under test, $X_1 Y(C_p(\epsilon_r))$ and $Y(C_p(\epsilon_r)) X_2$ are transmission matrices describing the instrument, probe, and interaction with the line, and $Y(C_p(\epsilon_r))$ is the transmission matrix of a capacitor with capacitance $C_p(\epsilon_r)$. The on-wafer calibration yields the measured result

$$T = \left[X_1 \;\; Y(C_p(\epsilon_r))\right]^{-1} \; M \; \left[Y(C_p(\epsilon_r)) \;\; X_2\right]^{-1}, \qquad (2)$$

whereas the off-wafer calibration yields

$$T' = \left[X_1 \;\; Y(C_p(\epsilon_{ro}))\right]^{-1} \; M \; \left[Y(C_p(\epsilon_{ro})) \;\; X_2\right]^{-1}. \qquad (3)$$

T′ is not the actual transmission matrix T of the device under test, but rather

$$T' = \left[Y(C_p(\epsilon_{ro}))^{-1} Y(C_p(\epsilon_r))\right] T \left[Y(C_p(\epsilon_r)) \, Y(C_p(\epsilon_{ro}))^{-1}\right] \qquad (4)$$

or equivalently

$$T' = Y(\Delta C_p)) \;\; T \;\; Y(\Delta C_p)) \qquad (5)$$

where

$$\Delta C_p = C_p(\epsilon_r) - C_p(\epsilon_{ro}). \qquad (6)$$

The method of [1] directly measures the two transmission matrices relating T′ to T in (4) and (5). Figures 3 and 4 show these matrices in S-parameter form for an off-wafer GaAs calibration used to measure on a lanthanum aluminate substrate. Figures 3 and 4 also show the calculated S-parameters of a shunt capacitance of value 7.555 fF. We determined these values using a circuit simulator to optimize the match between the measurements and the calculations. In spite of some residual differences, the figures show generally good agreement, an indication that the two transmission matrices in (4) and (5) are indeed modeled to a good approximation by a small capacitance ΔC_p. Similar agreement was found for an off-wafer GaAs calibration used to measure on fused silica and a capacitance of -6.562 fF.

We presumed that $C_p(\epsilon_r)$ includes both the end-effect capacitance and the capacitance of the short section of line before the on-wafer reference plane, as illustrated in Figure 2. We measured the capacitance $C_p(\epsilon_{ro})$ on our off-wafer GaAs substrate directly. We accomplished this by performing a TRL calibration on our GaAs substrate and contacting a short line at one of its ends as illustrated in Figure 5; we did not contact the other end with a probe. We numerically moved the measurement

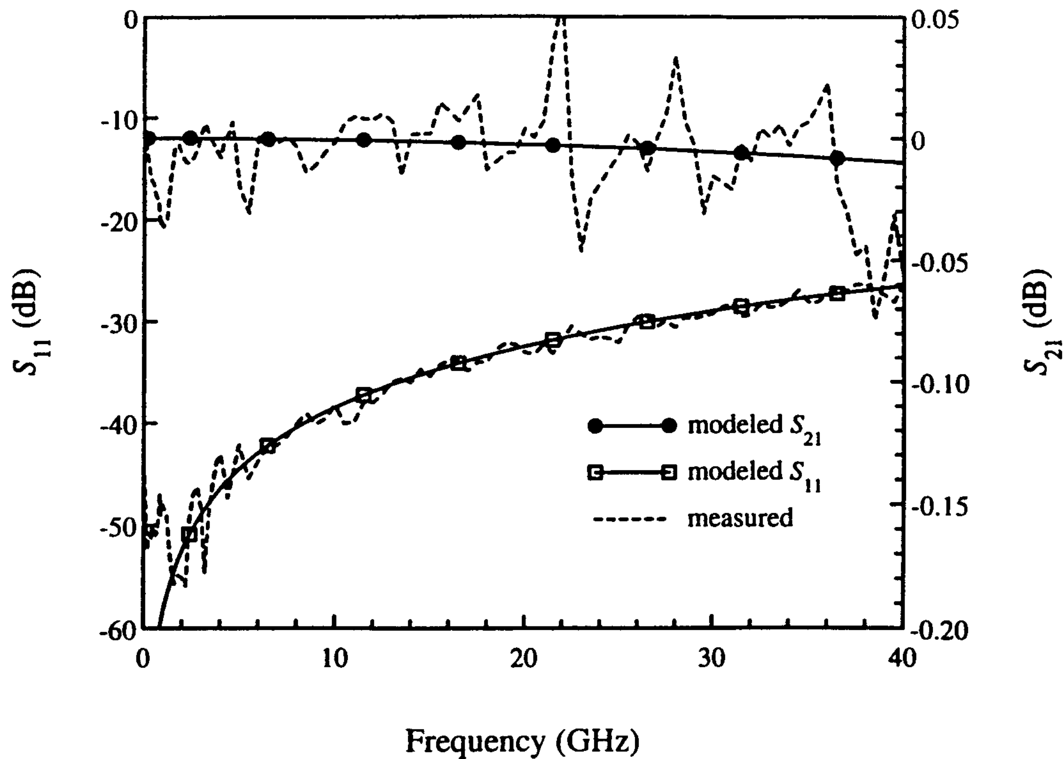

Figure 3. The magnitude of the S-parameters of the error box relating an off-wafer GaAs probe-tip calibration to an on-wafer calibration on a lanthanum aluminate substrate are shown in dotted lines. The S-parameters of a shunt 7.555 fF capacitor are shown in solid lines for comparison. The value of this capacitance was optimized by a circuit simulator so as to best match the measured S-parameters.

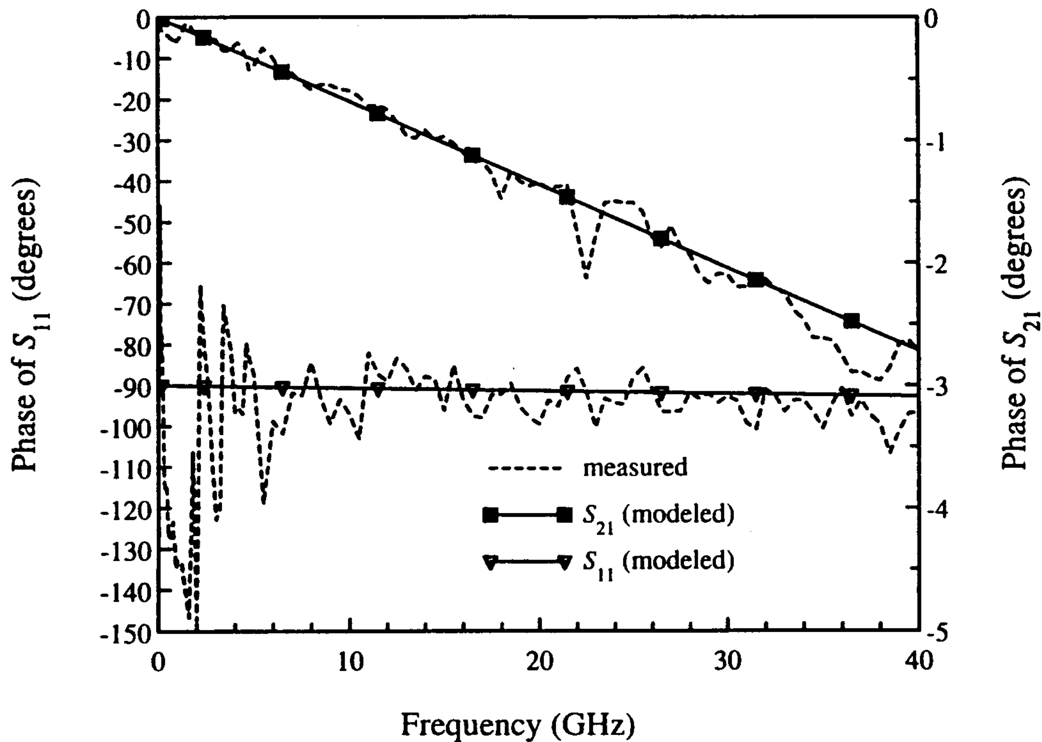

Figure 4. The phases of the quantities of Figure 3.

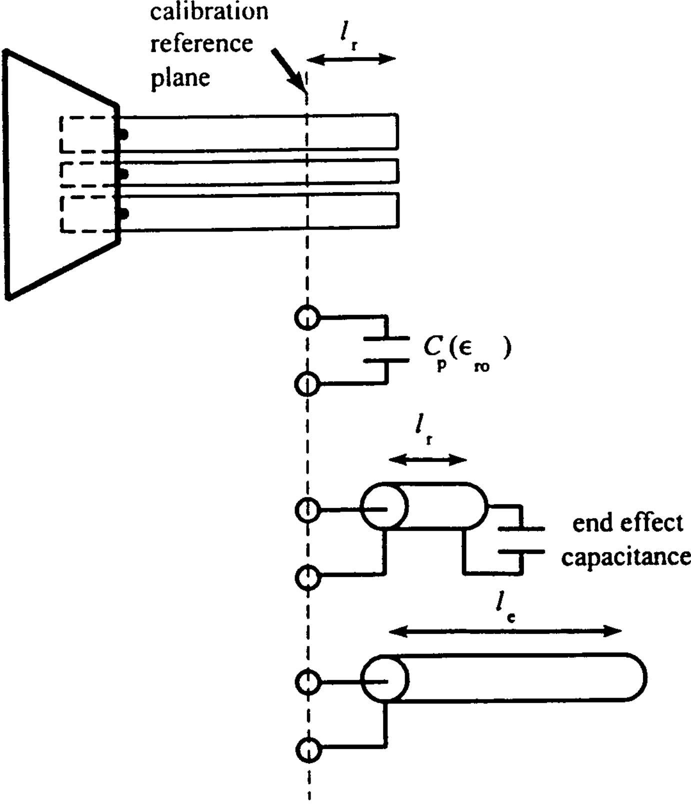

Figure 5. An illustration of the measurement of $C_p(\epsilon_{ro})$ and three equivalent circuits.

reference plane to a location l_r from the physical end of the short line, thus directly measuring the impedance of the open stub of length l_r. We defined the stub's electrical length to be $l_e \equiv C_p(\epsilon_{ro})/C_l(\epsilon_{ro})$ where C_l is the capacitance per unit length of the line (see Figures 2 and 5). The line's electrical length l_e is greater than l_r because it includes both the physical length and the added electrical length due to the end-effect capacitance.

We assumed that l_e is independent of the substrate relative dielectric constant ϵ_r, which leads to the approximation $C_p(\epsilon_r) \approx l_e\, C_l(\epsilon_r) \approx C_p(\epsilon_{ro})\, C_l(\epsilon_r)/C_l(\epsilon_{ro})$. For CPW line capacitance, we used the quasi-TEM approximation $C_l(\epsilon_r) \approx 2(\epsilon_r+1)\epsilon_o\, K(k)/K((1\text{-}k^2)^{1/2})$ where ϵ_o is the permittivity of free space, K is the complete elliptic integral of the first kind, and k is the ratio of the center conductor width to the distance between the ground planes [9]. This approximation assumes infinitely thin, perfectly conducting metal, a semi-infinite substrate, and semi-infinite ground planes. For lines of identical geometry, these two assumptions yield

$$C_p(\epsilon_r) \approx \frac{\epsilon_r + 1}{\epsilon_{ro} + 1}\, C_p(\epsilon_{ro}), \tag{7}$$

which results in

$$\Delta C_p = C_p(\epsilon_r) - C_p(\epsilon_{ro}) \approx \frac{\epsilon_r - \epsilon_{ro}}{\epsilon_{ro} + 1}\, C_p(\epsilon_{ro}). \tag{8}$$

The first and second lines of Table I compare the fitted values of ΔC_p with the values predicted by **(8)**. The predicted values are based on a measured value of $C_p(\epsilon_{ro})$ = 9.37 fF and the reported relative dielectric constants ϵ_{ro}=12.95 of GaAs [10], ϵ_r=3.825 of fused silica [11], ϵ_r=23.95 of lanthanum aluminate [12], and ϵ_r=10.4 of sapphire, the average of its vertical and horizontal dielectric constants [12]. The table shows that the fitted values of ΔC_p are reasonably consistent with the values predicted by our approximate model.

Error Bound Prediction

The capacitance model developed above predicts that the bounds on $|S'_{ij} - S_{ij}|$ of [1] will be

$$|S_{ii}' - S_{ii}| \lesssim (1 + 2|S_{ii}| + |S_{ii}|^2 + |S_{12}S_{21}|)\, |B/2| \tag{9}$$

and

$$\frac{|S_{ij}' - S_{ij}|}{|S_{ij}|} \lesssim (2 + |S_{11}| + |S_{22}|)\, |B/2| \qquad (i \neq j) \tag{10}$$

where $B \equiv \omega\, \Delta C_p\, Z_r$, Z_r is the reference impedance of the calibration and the symbol $\lesssim$ indicates that the inequality is strictly valid only when $|B| \ll 1$. If $|S_{11}| \leq 1$, $|S_{22}| \leq 1$, and $|S_{12}S_{21}| \leq 1$, then we can simplify **(9)** and **(10)** to obtain the bound

$$|S_{ij}' - S_{ij}| \lesssim 5\,|B/2|. \tag{11}$$

The estimated bounds from **(11)** using the estimates for ΔC_p from **(8)** and the published dielectric constants are plotted in dashed lines and labeled with markers in Figure 1. The figure also shows that, at least when the systematic component of the measurement error is large compared to the repeatability error, the estimates from **(11)** and **(8)** predict well the measured bounds.

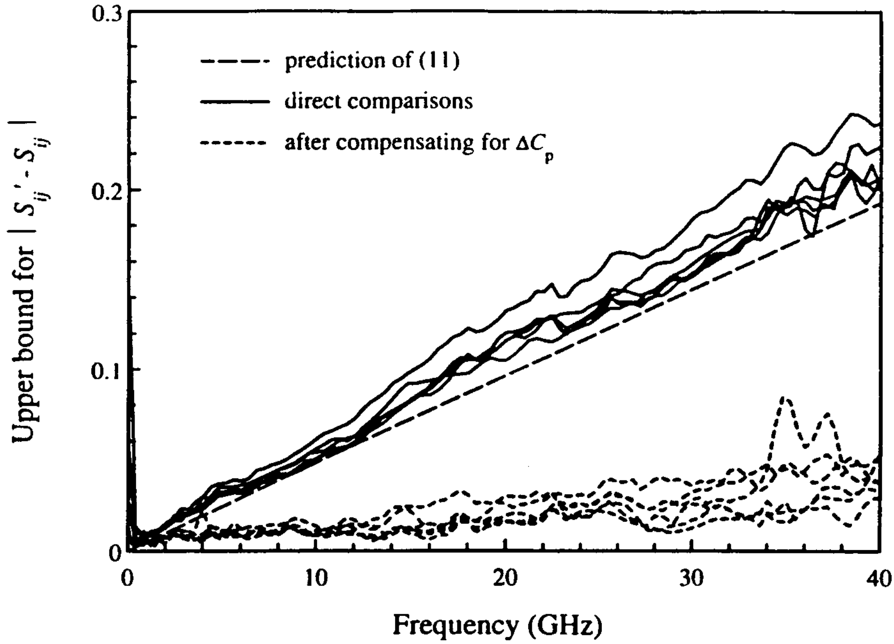

Figure 6. The bounds for differences between measurements of passive devices, comparing an off-wafer GaAs calibration to an on-wafer fused silica calibration. Results from different probe configurations are shown both before and after compensation for the capacitance ΔC_p at the probe tips. The dashed curve is the prediction from **(11)**.

TABLE I

Values of ΔC_p determined by various methods. Data for the 550 μm open stub was available only for fused silica.

	ΔC_p		
Method	fused silica	sapphire	lanthanum aluminate
From error boxes	-6.562 fF	-2.331 fF	+7.555 fF
From ϵ_r reported in [10-12] and **(8)**	-6.129 fF	-1.713 fF	+7.388 fF
From 550 μm line and **(12)**	-6.365 fF	-2.132 fF	+7.532 fF
From 550 μm stub and **(12)**	-6.448 fF	-----	-----

PROBE-INDEPENDENCE OF THE RESULTS

Figure 6 illustrates the difference between the GaAs and fused silica CPW probe-tip calibrations for various probe configurations. We used an alumina probe of 150 μm pitch at angles of approximately 11°, 25°, and 45° with the substrate. We also performed the experiment with this same probe at an angle of 11° but with the position of the probe-tip contact displaced from our nominal position of approximately 35 μm from the beginning of the line to positions approximately 10 μm and 45 μm from the beginning of the lines. In addition, we performed the experiment with a probe of coaxial construction. The figure shows that the estimated bounds from equation **(11)** are applicable to probes of different construction and geometry and to different contact positions. This result is consistent with our model's assumption that the residual capacitance is due strictly to the substrate, not to the probe.

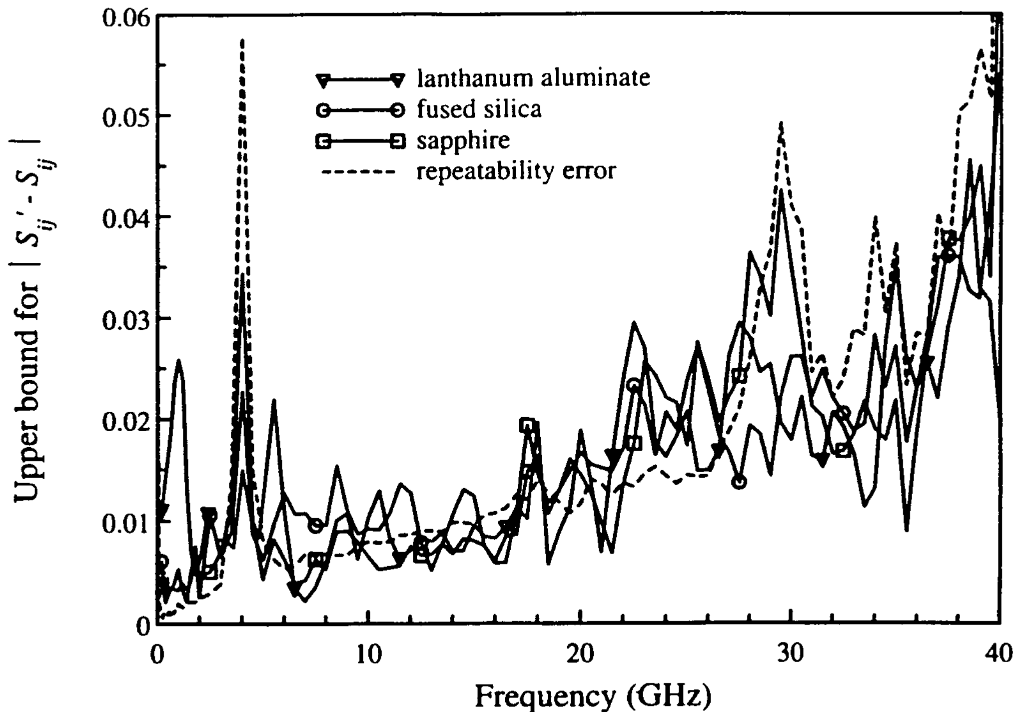

Figure 7. The bounds of Figure 1 after compensation of the off-wafer calibrations for the capacitance ΔC_p at the probe tips.

COMPENSATION FOR A CHANGE IN SUBSTRATE

Once these systematic errors have been evaluated, the calibration can be modified to correct them, as has been done for coaxial measurements [5]. To accomplish the correction, we modified the GaAs calibrations of Figure 1 by cascading the transmission parameters of the capacitances ΔC_p to the calibration error boxes. Figure 7 plots the differences between these modified GaAs calibrations and the on-wafer probe-tip calibrations. The figure shows that the upper bounds on measurement differences are comparable to the instrument drift and contact errors, demonstrating that the accuracy of the modified off-wafer calibration is comparable to the accuracy of the on-wafer calibration.

Figure 6 also shows a comparison of modified off-wafer calibrations to the fused silica on-wafer calibrations for various probe configurations. The compensation method works well for all of the probe configurations we tested.

DETERMINING ΔC_p FROM ON-WAFER STRUCTURES

For measurement on fused silica, Figure 8 plots bounds on the off-wafer calibration as modified using several values of ΔC_p. The figure shows that, in this case, ΔC_p need not be known to much better than about 1 fF for the compensation to be effective. The insensitivity of the correction allows a number of approximate methods for estimating ΔC_p. For example, the values of ΔC_p from (6) and the published dielectric constants are, in this case, sufficiently accurate.

ΔC_p can also be estimated with good accuracy from measurements of simple capacitive on-wafer test structures, such as open stubs, with the off-wafer calibration. The estimate is based on relating ΔC_p to the capacitance of the test structure. The method differs from [2-4] in that the capacitance ΔC_p is not measured directly but is inferred from the larger change in $C_s(\epsilon_r)$, the total capacitance of the test structure, due to a change of substrate dielectric constant.

Figure 9 shows a simplified measurement model for an open stub. The model neglects any inductance and resistance in the stub. While the analyzer measures X_1 and $C_s(\epsilon_r)$, the off-wafer calibration removes X_1 and a capacitance of value $C_p(\epsilon_{ro})$ from this measurement, measuring a capacitance $C_s(\epsilon_r) - C_p(\epsilon_{ro})$. We determined this capacitance from the low-frequency limit of $\mathrm{Im}(1/\omega Z_s)$ where Z_s is the impedance of the open stub measured by the off-wafer calibration. Subtracting the

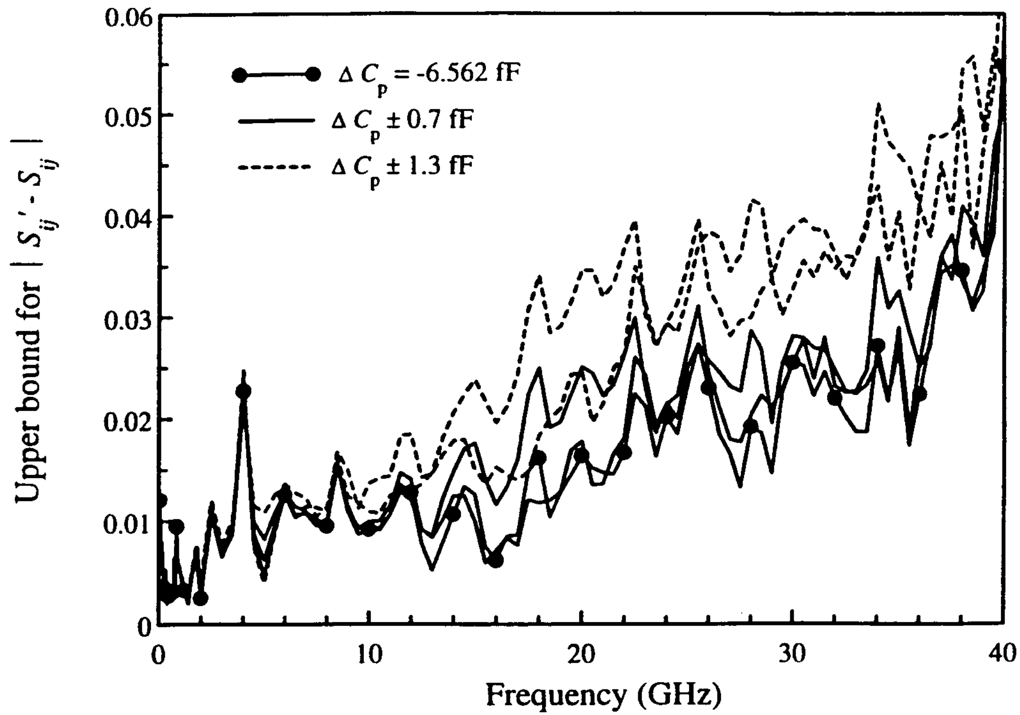

Figure 8. The sensitivity of the modified off-wafer GaAs calibrations to the capacitance used for the correction.

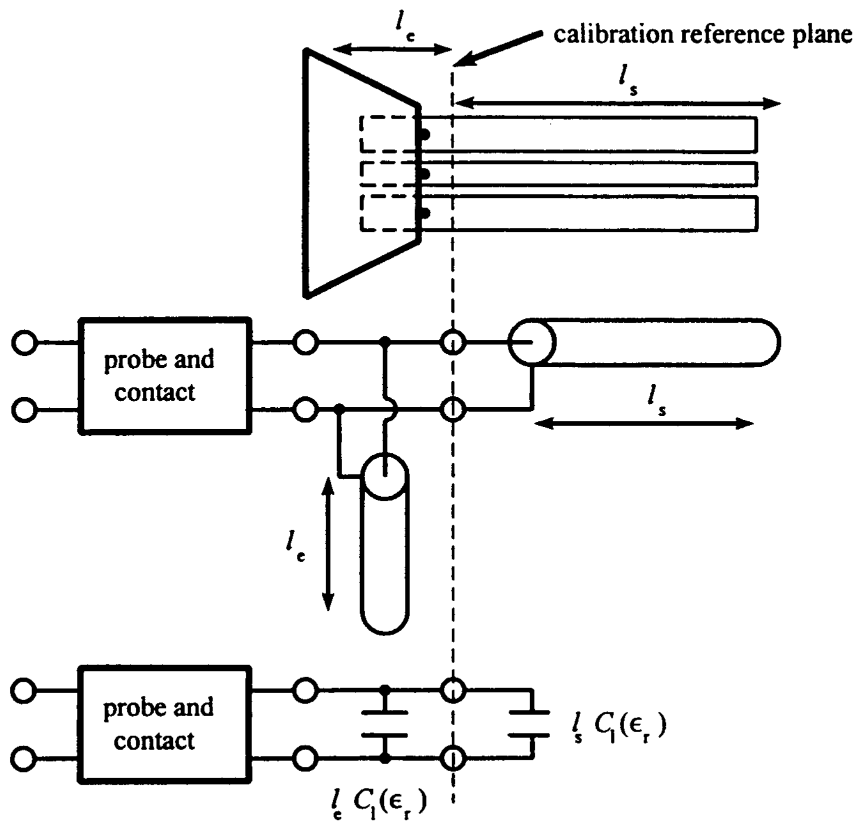

Figure 9. The measurement of an open stub and two equivalent circuits for the probe and transition to the CPW line.

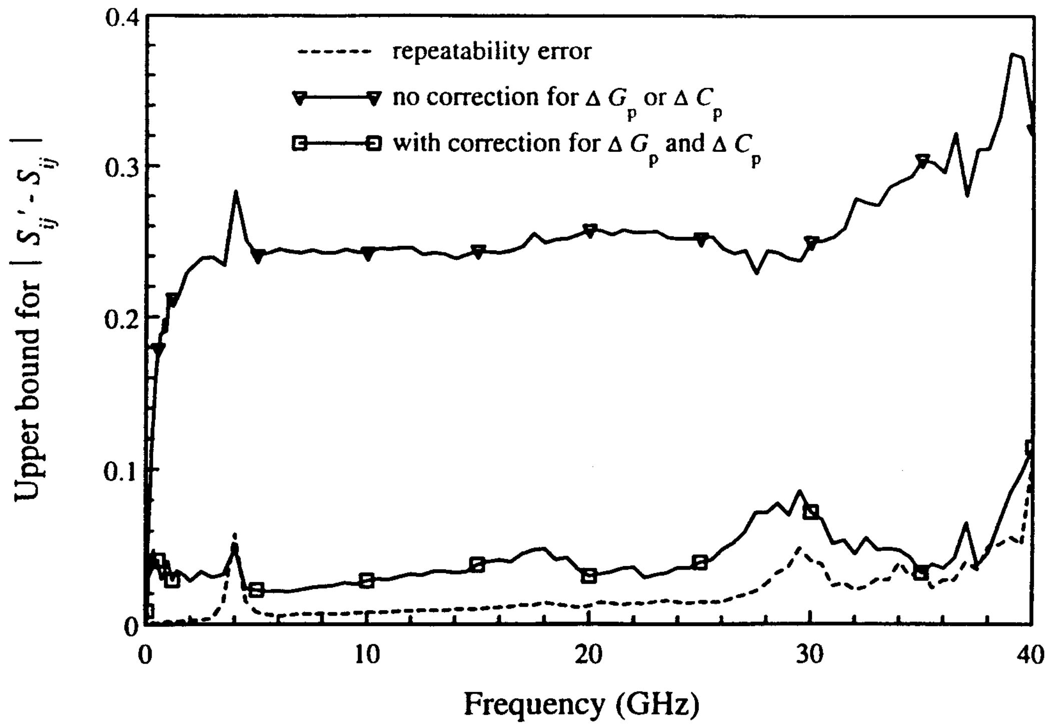

Figure 10. The bounds for differences between measurements of passive devices, comparing an off-wafer GaAs calibration to an on-wafer silicon calibration [13] before and after compensation for the frequency-dependent capacitance ΔC_p and conductance ΔG_p at the probe tips.

measured capacitances of open stubs fabricated on and off the wafer yields the quantity $C_s(\epsilon_r)$ - $C_s(\epsilon_{ro})$. For stubs of identical geometry this is approximately the change in capacitance of a section of transmission line of length $l_s + l_e$ where l_e is the electrical length of the line behind the measurement reference plane and l_s is the electrical length of the open stub in front of the measurement reference plane. Both l_s and l_e include the electrical length of the end-effect capacitance (29 μm in our case). The capacitance ΔC_p required to correct the off-wafer calibration, however, is only that due to a transmission line of length l_e. Thus ΔC_p can be determined approximately from

$$\Delta C_p \approx (C_s(\epsilon_r) - C_s(\epsilon_{ro})) \frac{l_e}{l_s + l_e} \qquad (12)$$

where the term $C_s(\epsilon_r)$ - $C_s(\epsilon_{ro})$ is simply the difference in the measured capacitances of the two open stubs on the two substrates, typically much larger than ΔC_p, and the term $l_e/(l_s+l_e)$ on the right is the ratio of the electrical length of the open stub behind the reference plane to the total electrical length of the open stub. To demonstrate this method for the measurement of ΔC_p, we used two open stubs of physical length 550 μm on our fused silica and GaAs substrates measured with the off-wafer GaAs calibration. Line 4 of Table I shows the estimate for ΔC_p from (12). This estimate is adequate for an accurate correction.

ΔC_p can also be determined from two-port measurements of lines fabricated on the two wafers. This procedure uses the fact that the impedance Z_s of a one-port stub of length l terminated with an ideal open circuit can be synthesized from the impedance parameters Z_{ij} of a line of length $2l$ from $Z_s = Z_{11}+Z_{12}$. In this case the electrical length of line l_s in front of the reference plane, is just the distance from the reference plane to the center of the line. The results, listed in line 3 of Table I, are close to the measured values of ΔC_p and thus would also effectively correct the off-wafer GaAs calibration.

Lossy Silicon Substrate

We also applied the method to a lossy silicon substrate, for which the manufacturer specified a conductivity in the range of 0.2-0.5 S/cm. Figure 10 compares the off-wafer GaAs probe-tip calibration to a silicon probe-tip calibration based on the calibration

comparison technique of [13] and shows large systematic differences.

To account for the substrate loss, we added a conductance ΔG_p in shunt with ΔC_p at the probe tip. Both ΔG_p and ΔC_p were calculated at each frequency from the thru measurement of a 550 μm line, ΔC_p using (12) with $C_s(\epsilon_r) \equiv \mathrm{Im}(1/\omega Z_s)$ and ΔG_p from

$$\Delta G_p = G_s \frac{l_e}{l_s + l_e} \tag{13}$$

where $G_s \equiv \mathrm{Re}(1/Z_s)$. The correction, marked with squares in Figure 10, improves the accuracy of the off-wafer calibration significantly. Nevertheless, the differences between the modified GaAs calibration and the silicon calibration from [13] are still somewhat greater than the repeatability error for the experiment, which is plotted as a dotted line in the figure.

Microstrip Calibration

All of the experiments reported here involved coplanar waveguide. Although some generalization may be possible, the model is not universal. For example, commercial users frequently apply off-wafer CPW calibrations to measurements of devices embedded in microstrip. Obviously, the CPW calibration does not account for the electromagnetic behavior, typically modeled as a series inductance, of the "vias" connecting the microstrip ground plane to the probe contact pads. Since this behavior cannot be corrected by a shunt admittance, we would not expect the method presented here to apply. In experiments, we found that we were indeed unable to model the differences between off-wafer CPW and on-wafer microstrip calibrations with a shunt admittance at the probe tip; at a minimum, a series inductance was required to obtain a reasonable fit. Further study is required to confirm the utility of a generalized method.

Conclusions

The correction for a fixed shunt capacitance at the probe tip proved extremely effective on the fused silica, sapphire, and lanthanum aluminate substrates for reference plane positions near the probe tips, reducing systematic error to the level of the repeatability error in the experiments. On these substrates, ΔC_p could be estimated from published values of dielectric constant with adequate accuracy. On the silicon substrate, the correction for a frequency-dependent shunt capacitance and conductance at the probe tip also offered a large improvement in calibration accuracy. In this case, however, the correction did not reduce the difference between the off-wafer and on-wafer calibrations quite to the repeatability error in the experiment. Additional systematic error is apparently present, either in the modified off-wafer calibration or in the approximate on-wafer calibration to which we were comparing.

The model makes restrictive assumptions concerning the differences between the on-wafer and off-wafer calibrations. A specific CPW launch geometry was used throughout the experiments and the calibration reference planes were located near the probe tip. Many of the relations between line capacitance, end-effect capacitance, and substrate relative dielectric constant were specific to CPW with thin, highly conducting metal. Inductive and resistive behavior of the line behind the reference plane was ignored. Serious violation of any of the assumptions might invalidate the method. In the one such case we investigated, a microstrip calibration, the differences between calibrations was not modeled well by a shunt admittance, and the method failed.

Despite some limitations, the method provides a simple means of measuring S-parameters at the probe tip with high accuracy in CPW of standard dimensions using an off-wafer calibration. While the contact and launch geometry of the devices under test must conform to the standard, on-wafer calibration structures are minimized or eliminated.

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