

Comparison of On-Wafer Calibrations¹

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Abstract

A powerful new verification technique determines the measurement accuracy of scattering parameter calibrations. The technique determines the relative reference impedance, reference plane offset, and the worst-case measurement deviations of any calibration from a benchmark calibration. The technique is applied to several popular on-wafer scattering parameter calibrations, and the deviations between those calibrations and the thru-reflect line calibration are quantified.

Introduction

Although the microwave scattering parameters (S-parameters) of a device embedded in a transmission line may be measured accurately with the thru-reflect-line (TRL) calibration the bandwidth limitations associated with TRL and the difficulty of fabricating and measuring precision TRL standards make its use inconvenient in some production environments. As a result, other calibration methods, such as open-short-load-thru (OSLT), line-reflect-match (LRM) [1,2], or line-reflect-reflect-match (LRRM) [3], are commonly used, especially for on-wafer testing.

The TRL calibration requires a thru line long enough that only a single mode propagates at its center, a longer line, and two identical reflects. To ensure a consistent calibration, the probe-

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tip transition and the lines are fabricated to be nearly identical to those in which the device is embedded. In contrast to a consistent TRL calibration, many of the commonly used on-wafer calibrations are based on lumped elements and transmission lines fabricated on different substrates. Since these calibrations do not involve the actual probe-tip transitions and transmission lines used in the measurement, they might not accurately measure the actual scattering parameters of the device.

In this paper, we develop a technique for quantifying the differences between S-parameter measurements made with respect to any two vector network analyzer (VNA) calibrations. We apply the technique to the comparison of LRM, LRRM, and OSLT calibrations to a benchmark TRL calibration. In the experiments, the benchmark TRL calibration is based on a set of coplanar waveguide (CPW) transmission lines with measured characteristic impedance and well-controlled dimensions.

In one experiment, we show how actual measured deviations of passive microstrip circuits compare to the worst case bounds developed in the paper.

Verification Technique

A two-port VNA in which the switching and isolation errors are either negligible or have been completely accounted for by some correction algorithm provides a measurement M_i of the product of three matrices [4]

$$M_i = XT_i\bar{Y}, \quad (1)$$

where the reverse cascade matrix of Y is

$$\bar{Y} = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix} Y^{-1} \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix}, \quad (2)$$

and T_i is the cascade matrix of device i . The calibration procedure consists of connecting a number of devices whose cascade matrices T_i are assumed to be known. When enough measurements M_i are available, approximations to the matrices X and Y are determined.

Let T^M be the cascade matrix of a device measured with respect to a calibration M , T^B its cascade matrix measured with respect to a benchmark calibration, and T^o its actual cascade matrix. Then (1) shows that T^M , T^B and T^o must be related by

$$T^M = X^B T^B \overline{Y^B} = X^O T^O \overline{Y^O} . \quad (3)$$

The matrices X^O , Y^O , X^B , and Y^B in (3) are independent of the device under test and are determined by the calibrations. The verification is based on determining these matrices.

The verification begins with a VNA calibrated with initial calibration M. Subsequently, a benchmark calibration based on precise transmission lines is performed with respect to calibration M using the two-tier multi-line TRL calibration of Marks [5]. This procedure determines X^B and Y^B .

Marks and Williams [4] show that the TRL calibration provides a direct measurement of the cascade matrix T^O when the same lines and transitions connected to the device under test are used in the calibration and when there are no random measurement errors or unaccounted-for switching and isolation errors. They also show that those cascade parameters are measured with respect to a reference plane in the center of the thru line, whose length we designate $2l_o$, and a reference impedance which is equal to the characteristic impedance Z_o of the line. Since this is true for all devices embedded in the line, $T^B=T^O$ for all matrices T^O , and therefore $X^B=X^O$ and $Y^B=Y^O$.

From the preceding argument we see that X^B and Y^B are good approximations to the matrices X^O and Y^O . This is true only when the same transitions and lines connected to the device are employed in the TRL calibration procedure, however. Thus the "correct" benchmark is the TRL calibration using the same lines and transitions as are actually connected to the device.

The matrices X^O and Y^O describe the differences between measurements performed with respect to the initial calibration M and the actual S-parameters of the device. If the calibration M measures the actual S-parameters, then $X^O=Y^O=I$, the identity matrix. Deviations from the identity matrix may occur for a number of reasons. For instance, a TRL calibration may not be perfect due to random connector and other measurement error. In that case, X^O and Y^O represent these random errors.

Two calibrations may also differ systematically due to differences in reference plane or reference impedance. Then, we may find it more informative to compare measurements performed with respect to calibration M not to the actual cascade matrix but instead to a transformed version in which the reference plane and reference impedance have been adjusted. Of particular interest are fixed reference planes and real and constant reference impedances [4].

Let $T(Z,l)$ be the result of a transformation of T^O to refer-

ence planes l and to reference impedance Z . Then

$$T^o = R(Z, l) T(Z, l) \overline{R(Z, l)}, \quad (4)$$

and

$$T^M = X^o T^o \overline{Y^o} = [X^o R(Z, l)] T(Z, l) \overline{Y^o R(Z, l)}, \quad (5)$$

where

$$\begin{aligned} R(Z, l) &\equiv \frac{1}{\sqrt{1-\Gamma^2}} \begin{bmatrix} e^{-\gamma(l-l_o)} & 0 \\ 0 & e^{\gamma(l-l_o)} \end{bmatrix} \begin{bmatrix} 1 & \Gamma \\ \Gamma & 1 \end{bmatrix} \\ &= \frac{1}{\sqrt{1-\Gamma^2}} \begin{bmatrix} e^{-\gamma(l-l_o)} & \Gamma e^{-\gamma(l-l_o)} \\ \Gamma e^{\gamma(l-l_o)} & e^{\gamma(l-l_o)} \end{bmatrix}, \end{aligned} \quad (7)$$

$$\Gamma \equiv \frac{Z-Z_o}{Z+Z_o}, \quad (8)$$

and γ is the propagation constant in the transmission line. The reference plane positions have been defined so that an increasingly positive position is farther from the analyzer.

Estimates of Reference Impedance and Reference Plane Position

We have derived estimates for the reference impedance Z_M and reference plane position l_M of calibration M from X^o or Y^o . The estimates for the reference impedance and reference plane from X^o are

$$\hat{\Gamma}_X = \sqrt{\frac{X_{11}^o X_{22}^o - 1}{X_{11}^o X_{22}^o}} = \sqrt{\frac{X_{21}^o X_{12}^o}{1 + X_{21}^o X_{12}^o}}, \quad (9)$$

and

$$\hat{l}_X = l_o + \frac{Im(\ln(X_{11}^o/X_{22}^o))}{2Im(\gamma)}, \quad (10)$$

where the estimate of Z_M is related to the estimate (9) by (8). The estimates for the second port are identical except that the elements of X° in (9) and (10) are replaced by the corresponding elements of Y° .

For many calibrations, we expect the reference impedances and reference plane offsets at each port to be identical. Then the estimates

$$\hat{\Gamma} = \frac{\hat{\Gamma}_X + \hat{\Gamma}_Y}{2}, \quad (11)$$

and

$$\hat{I} = \frac{\hat{I}_X + \hat{I}_Y}{2}, \quad (12)$$

are most appropriate. In many cases the reference plane is also expected to remain constant as a function of frequency, so it is appropriate to consider the estimate

$$I_M = \frac{\sum_i |Im(\gamma_i)| \cdot \hat{I}_i}{\sum_i |Im(\gamma_i)|}, \quad (13)$$

where i spans the set of measurements over which X° and Y° are known.

Worst-case Deviations

We have also derived worst-case deviations of the measured S-parameters S_{ij}^M (corresponding to the cascade matrix T^M) and the impedance and reference plane transformed S-parameters S_{ij} (corresponding to the cascade matrix $T(Z, l)$) in terms of the elements of

$$\delta^X = X^\circ R(Z, l) - I; \quad \delta^Y = Y^\circ R(Z, l) - I. \quad (14)$$

The derivation assumes that $|S_{ij}| \leq 1$, which is true for passive devices when the reference impedance is real at each port. The worst-case deviations are

$$|S_{11}^M - S_{11}| \leq \epsilon_{11} \equiv |\delta_{11}^X - \delta_{22}^X| + |\delta_{21}^X| + |\delta_{12}^X| + |\delta_{21}^Y|, \quad (15)$$

$$\frac{|S_{21}^M - S_{21}|}{|S_{21}|} \leq \epsilon_{21} \equiv |\delta_{11}^Y - \delta_{22}^X| + |\delta_{21}^X| + |\delta_{21}^Y|, \quad (16)$$

$$\frac{|S_{12}^M - S_{12}|}{|S_{12}|} \leq \epsilon_{12} \equiv |\delta_{11}^X - \delta_{22}^Y| + |\delta_{21}^Y| + |\delta_{21}^X|, \quad (17)$$

and

$$|S_{22}^M - S_{22}| \leq \epsilon_{22} \equiv |\delta_{11}^Y - \delta_{22}^Y| + |\delta_{21}^Y| + |\delta_{12}^Y| + |\delta_{21}^X|, \quad (18)$$

where we have used the symbol \leq to indicate that the inequalities are strictly valid only when $|\delta_{ij}^X| \ll 1$ and $|\delta_{ij}^Y| \ll 1$. We will also use the bound

$$|S_{ij}^M - S_{ij}| \leq \epsilon(Z, l) \equiv \max_{mn}(\epsilon_{mn}). \quad (19)$$

In (19) we have added the arguments Z and l to explicitly reflect the dependence, through R , of ϵ on the reference impedance and reference plane position of the transformed benchmark calibration.

Experimental Results

We have applied the verification technique to a number of different on-wafer calibrations, which we denote as the LRM_{GaAs}, LRM_{sapphire}, OSLT, LRRM, and TRL calibrations. The calibrations were compared to benchmark TRL calibrations based on a CPW thru line of 550 μm length, five lines of additional length 2.135 mm, 3.2 mm, 6.565 mm, 19.695 mm, and 40 mm, and two shorts offset 0.225 mm from the beginning of the line. These calibration standards were all fabricated on a 500 μm thick GaAs wafer and had a center conductor of width 73 μm separated from two 250 μm ground planes by 49 μm gaps in the 1.5 μm thick gold metallization. The benchmark calibrations were performed using the multi-line TRL calibration algorithm of Marks [5]. The capacitance of the lines was found from the resistance per unit length of the lines, as explained in [6]. The characteristic impedance Z_0 of the CPW lines was found from the capacitance and propagation constant of the lines as explained in [7].

LRM calibrations always transform the thru used in the calibration into a perfect thru and the match (resistor) used in the calibration into a reflectionless load. Thus the shift of reference impedance cannot be detected by remeasuring the calibration standards with respect to the LRM_{GaAs} calibration. This makes

these shifts in reference impedance difficult to detect except by comparison to another calibration or by the measurement of other artifacts. The LRM_{GaAs} calibration demonstrates this clearly.

The LRM_{GaAs} calibration used the same CPW thru line and CPW short as the TRL benchmark. In addition, a single small resistor embedded in CPW line on the same wafer was used as the match standard and served to set the reference impedance for the calibration, as explained in [4]. The resistor consisted of a single $73 \mu\text{m}$ -by- $73 \mu\text{m}$ square of resistive material placed at the end of the line. In Figure 1, the estimates of the reference impedance of the LRM_{GaAs} calibration are plotted.

The shift in the real part of the reference impedance shown in the figure is caused by the resistor, which has a variable resistance as a function of frequency. The variation is caused by photoresist residue left between the gold conductor and the thin-film resistor by the lift-off process used to pattern the gold conductor. Although only the small amount of photoresist residue typical of lift-off processing was present, its effect on the electrical properties of the resistor is large. In this experiment, so little photoresist residue was present that it could not be detected with conventional optical microscopy.

Since the LRM_{GaAs} calibration used the same thru and reflect as the benchmark calibration, its reference impedance must, in the absence of measurement errors, be equal to the load impedance of the resistor [4,8]. We measured the impedance of the resistor and plotted its real part in the same figure for comparison. The difference between these measurements is negligible. The imaginary parts showed similar agreement.

The OSLT and $LRM_{sapphire}$ calibrations were performed using a sapphire substrate. In the OSLT calibration, metallized bars were used for the shorts, probe tips suspended in the air for the opens, precise 50Ω resistors for the loads, and a short section of nominally 50Ω line for the thru. The OSLT calibration was performed following the procedure and standards definitions of the manufacturer. In the $LRM_{sapphire}$ calibration, metallized bars were used for the reflects, a precision 50Ω resistor for the match, and a short section of nominally 50Ω CPW for the thru.

The LRRM calibration was performed on an alumina substrate. The reflects consisted of shorts (short metallized bars) and opens (probe tips raised in the air). The match was a precise 50Ω resistor measured only on port 1 and the thru a short section of nominally 50Ω CPW. As explained in [3], the inductance of the resistor was determined from the measurement of the open. The experiment was performed on a different instrument, by a different operator, using a different set of lines on the GaAs wafer than in

the other experiments. The 40 mm line was also omitted from the benchmark calibration in this case, degrading its low frequency accuracy.

The OSLT and LRRM calibrations are designed so that the reference planes are near the probe tips. The probe tips were placed so that they were located at a position approximately $25 \mu\text{m}$ in front of the physical beginning of the benchmark standards. Using the beginning of the benchmark standards as a reference, we have plotted the estimates of \hat{l} in Figure 2 for the LRRM and OSLT calibrations. Figure 2 shows that the reference planes for the OSLT and LRRM calibrations lie approximately 30 and 18 μm in front of that point, respectively, a position very near the physical tip of the probe.

In Figure 3 we have plotted $\epsilon(50 \Omega, l_M)$ for the $\text{LRM}_{\text{sapphire}}$, OSLT, LRRM, and TRL calibrations. In the absence of measurement error, the plotted values represent the maximum deviation between measurements of a passive device and the actual S-parameters of the device measured with respect to a 50Ω calibration at the reference plane l_M .

The maximum deviation between the TRL calibration and its nominally identical benchmark, labeled "TRL" in the figure, is plotted to give an indication of the random measurement errors in our test setup and of errors arising from an incomplete correction for the switching or isolation errors of the VNA and probe station. Neither the LRRM nor the TRL calibrations deviate greatly from the benchmark calibration. Thus, some lumped-element calibrations can be nearly identical to the TRL calibration.

In contrast, the $\text{LRM}_{\text{sapphire}}$ and OSLT calibrations deviate significantly from the benchmark calibration, especially at the high frequencies. In Figure 4 we have plotted $\epsilon(\hat{Z}, \hat{l})$ for the OSLT and $\text{LRM}_{\text{sapphire}}$ calibrations. This shows that the deviations of the OSLT and $\text{LRM}_{\text{sapphire}}$ calibrations from the benchmark calibration remain even when the reference impedance \hat{Z} and reference plane \hat{l} are optimally chosen at each frequency. Since the calibrations are not related by an impedance transform to the benchmark, the cause of the deviations cannot be due to a neglect of the load reactance. The cause of these deviations has not yet been determined, but could be due to the use of a sapphire rather than an alumina substrate, to inaccurate probe placement, or to some unidentified factor affecting the accuracy of these calibrations.

Error Bounds

We also performed a study to determine how actual measured deviations compared with the worst-case bounds given in (15) and (16). The test wafer fabricated for the Software Validation

Project described in [9], which contained a large number of passive structures typical of those commonly used on MMICs, provided the test vehicle for the study.

We began the experiment by performing two TRL calibrations. The first was a TRL calibration in CPW. This calibration is not expected to account for the effect of the via-holes which comprise part of the probe tip-to-microstrip transition. The second was microstrip TRL calibration performed in the lines fabricated on the wafer containing the test structures. This calibration served as benchmark for the experiment. In contrast to the CPW calibration, the benchmark calibration does correct for the via-hole transition and measures the actual S-parameters of the devices in the microstrip lines. In both cases we transformed the reference planes to a position near the probe tips and transformed the reference impedances to 50Ω .

We then measured the S-parameters of the passive and primarily two-port test structures with respect to these two calibrations and plotted the differences in solid lines in Figures 5 and 6. We also determined the worst-case error bounds ϵ_{11} and ϵ_{21} , which we have plotted on the same graph for comparison. The figure shows that the actual deviations are indeed bounded by ϵ_{11} and ϵ_{21} . In many cases, the measured deviations approach the bounds ϵ_{11} and ϵ_{21} , showing that they are representative of actual measured deviations for typical passive MMIC structures.

Conclusion

In this work we have explored a powerful new technique for verifying calibrations. The technique determines the reference impedance, reference plane position, and worst-case deviations of measurements. Furthermore, these worst-case bounds on the deviations are representative of actual deviations for typical passive microwave circuits.

A number of on-wafer calibrations based on lumped elements on different media were compared to a benchmark TRL calibration performed in CPW. These calibrations give similar results below 10 GHz. The data indicate that, even above 10 GHz, lumped-element calibrations may agree closely with the CPW calibration. A comparison of a CPW calibration to a microstrip calibration, however, showed significantly larger measurement discrepancies even though the reference plane positions were moved to a location near the probe tips and the reference impedances were both set equal. These large discrepancies suggest that the CPW calibration did not accurately account for the effects of the via-hole transitions used in our experiment.

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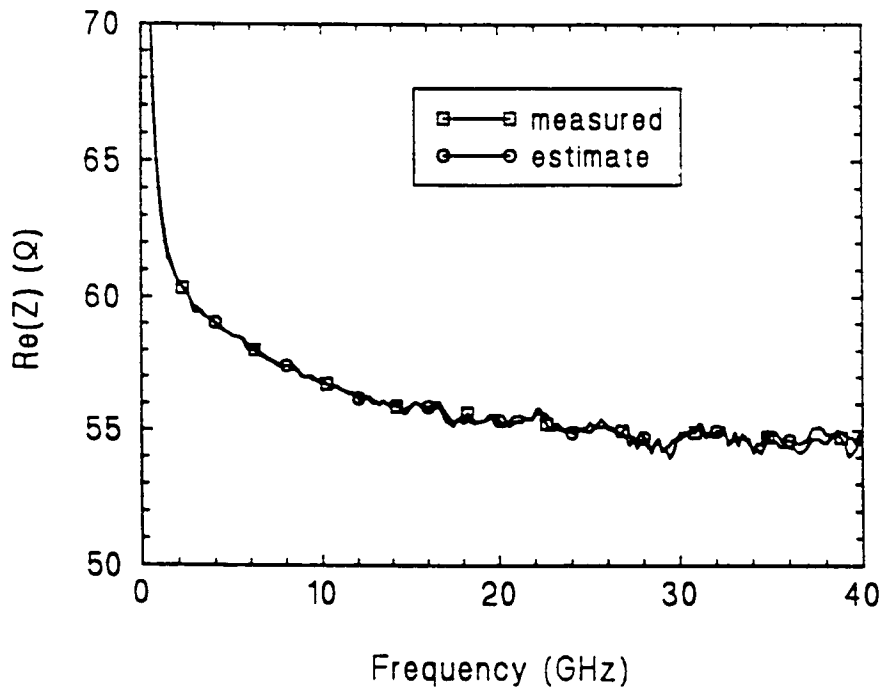


Figure 1. The real part of the estimated reference impedance of the LRM_{GaAs} calibration and the measured real part of the impedance of the match used in that calibration are compared. Due to its method of fabrication, the small resistor used as a match displays a complicated behavior as a function of frequency.

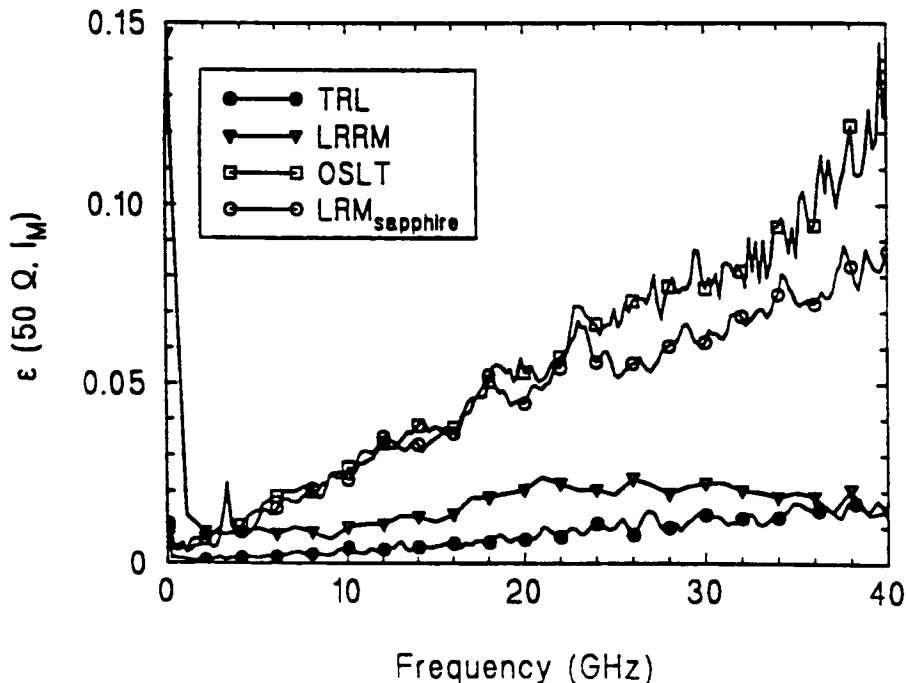


Figure 2. Estimates of the reference plane position of an LRRM and an OSLT calibration are plotted as a function of frequency. The reference plane position plotted corresponds to the distance in front of the physical beginning of the benchmark calibration standards, as indicated in the sketch in the upper right hand portion of the plot.

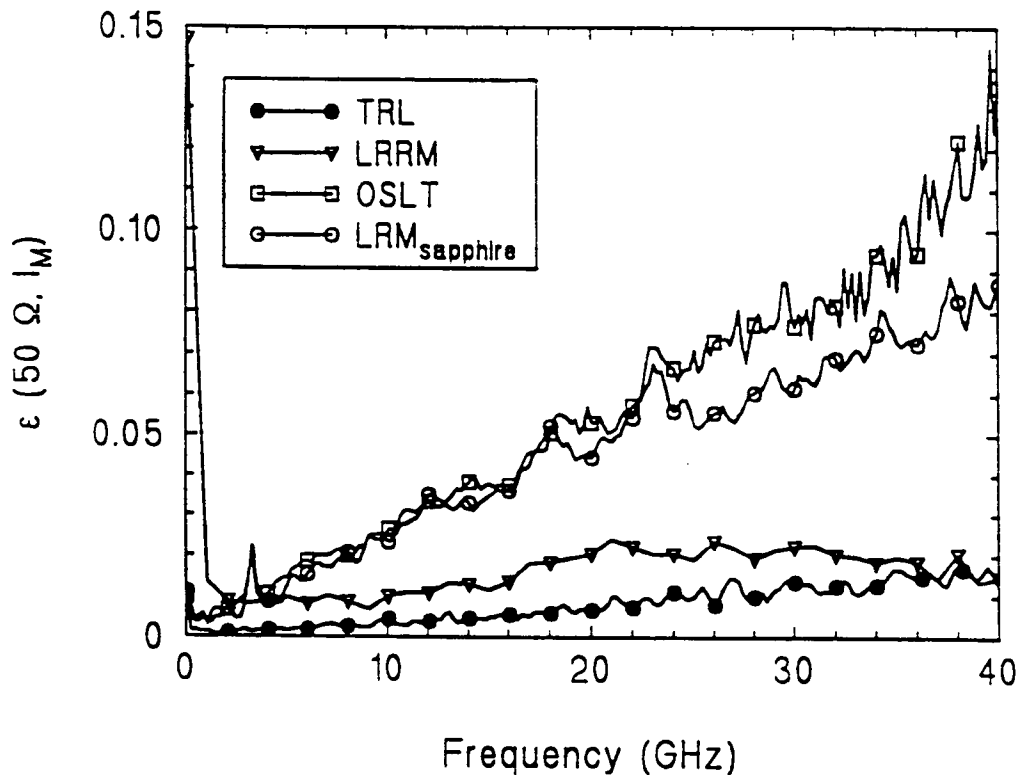


Figure 3. $\epsilon(50 \Omega, l_M)$ for the LRM_{sapphire} , OSLT, LRRM, and TRL calibrations. The calibrations are compared to a 50Ω benchmark calibration whose reference plane has been set at the estimated reference plane position l_M . The deviations depend both on frequency and calibration type.

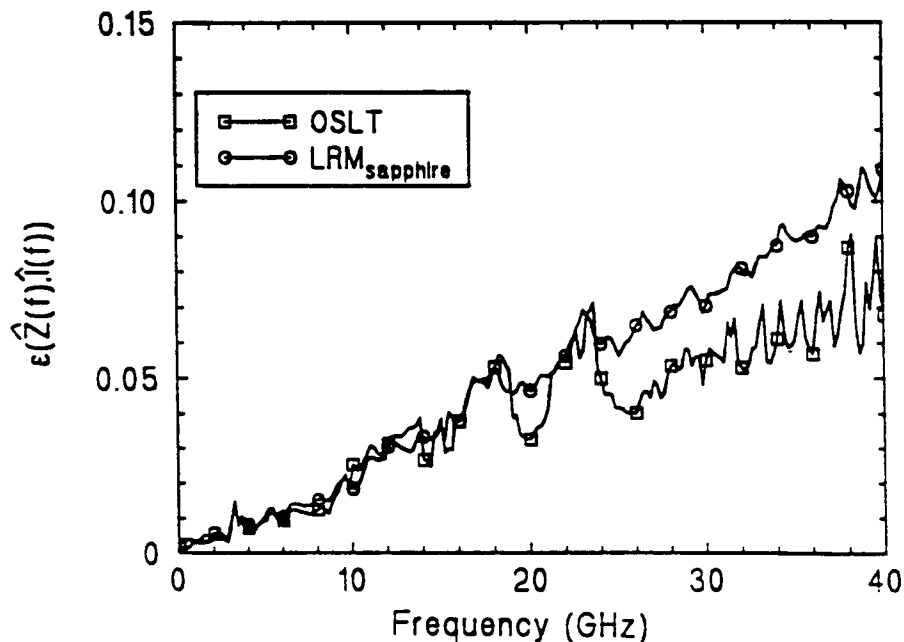


Figure 4. $\epsilon(\hat{z}, \hat{i})$ for the OSLT and LRM_{sapphire} calibrations. Comparison to Figure 3 shows that the deviations in these calibrations cannot be ascribed to a simple shift of reference plane and impedance.

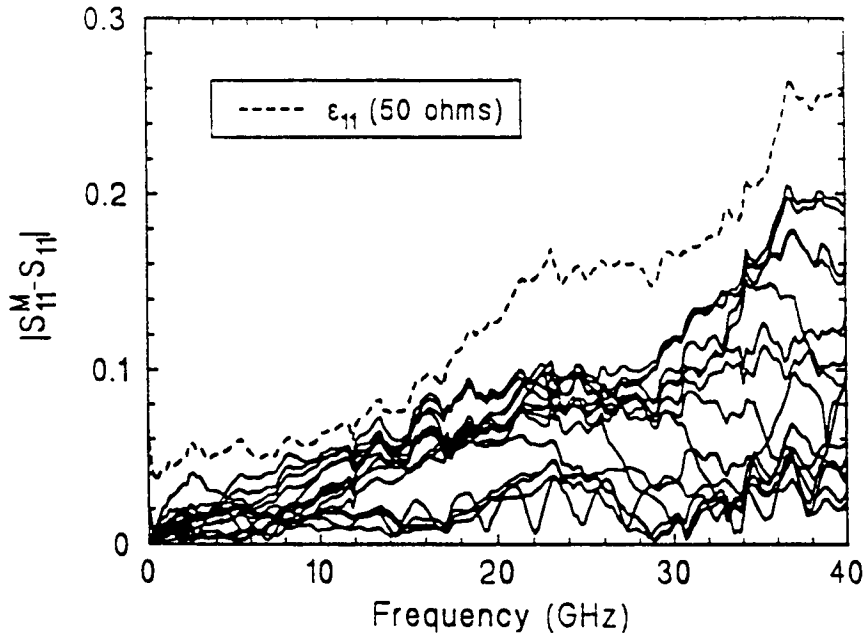


Figure 5. Measured deviations in the reflection coefficient of the passive test structures employed in the Software Validation Project [9]. For comparison, the worst case error bound ϵ_{11} for the calibration is shown as a dashed curve.

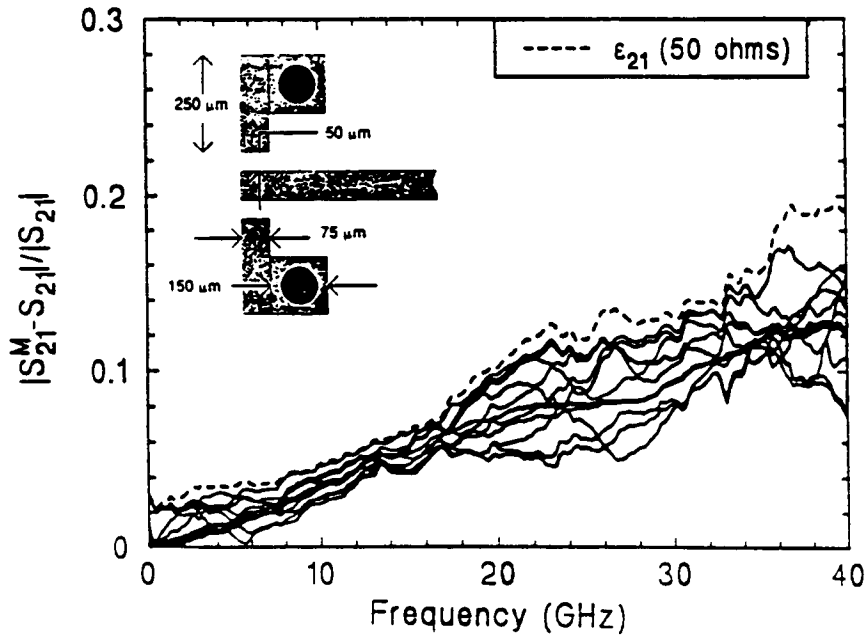


Figure 6. Measured relative deviations in the transmission coefficient of the passive test structures employed in the Software Validation Project [9]. For comparison, the worst case error bound ϵ_{21} for the calibration is shown as a dashed curve. The via-hole transition is sketched in the upper right hand corner of the plot.