Characterization of Broad-Band Transmission for Coplanar Waveguides on CMOS Silicon Substrates

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***Abstract*— This paper presents characteristics of microwave transmission in coplanar waveguides (CPW's) on silicon (Si) substrates fabricated through commercial CMOS foundries. Due to the CMOS fabrication, the metal strips of the CPW are encapsulated in thin films of Si dioxide. Many test sets were fabricated with different line dimensions, all on p-type substrates with resistivities in the range from 0.4 $\Omega\cdot$cm to 12.5 $\Omega\cdot$cm. Propagation constant and characteristic impedance measurements were performed at frequencies from 0.1 to 40 GHz, using a vector-network analyzer and the through-reflect-line (TRL) deembeding technique. A quasi-TEM equivalent circuit model was developed from the available process parameters, which accounts for the effects of the electromagnetic fields in the CPW structure over a broad frequency range. The analysis was based on the conformal mapping of the CPW multilayer dielectric cross section to obtain accurate circuit representation for the effects of the transverse fields.**

***Index Terms*—CMOS, coplanar waveguide, deembedding, microwave propagation on silicon substrate, on-wafer measurement.**

I. Introduction

PLANAR microwave transmission lines on lossy substrates such as silicon (Si) can exhibit a wide range of propagation characteristics in different frequency regimes and with different resistivities. Although transmission lines on Si substrates have been explored both experimentally and theoretically [1]–[6], in most cases, the lines were fabricated on high-resistivity Si and by special processes. With constantly increasing frequencies in digital circuits, downscaling of semiconductor processes, and increasing demand for integrated RF components in CMOS, it is necessary to characterize propagation behavior on lossy Si substrates with resistivities in the range of 1 $\Omega\cdot$ cm.

Substrates with resistivities on the order of 1 $\Omega\cdot$ cm, as commonly used in today's commercial CMOS processes, present a difficult problem for analysis and modeling. Accurate characterization of signal propagation behavior of transmission lines in CMOS integrated circuits was traditionally unessential because the circuits operated at relatively low frequencies and could be modeled sufficiently and accurately by simple lumped-element *RC* models. Today, the interest for more accurate modeling has grown significantly, due to high operating frequencies, with harmonics well into the microwave region.

Many of the proposed models for integrated circuit transmission lines refer to the different "modes" or mechanisms of propagation [2]–[6]. The "modes" were identified by Hasegawa *et al.* [2] using the values of loss tangent $(\sigma/\omega\varepsilon)$. They identified a "slow-wave" mechanism for large losses when the signal frequency was less than the Si relaxation frequency, and a "quasi-TEM" mechanism for low losses when the frequency exceeded the Si relaxation frequency. Kwon *et al.* [6] showed the so-called slow-wave "mode" to be a quasi-TEM waveguide mode by adequately describing their transmission lines with a single distributed resistance, inductance, conductance, and capacitance (RLGC) model. Marks and Williams also examined lossy transmission lines in their general theory of waveguides [7]. Their direct expressions for RLGC values, based on the quasi-TEM fields, show the distributed frequency-dependent circuit parameters to be an exact description of a quasi-TEM transmission line. They also examined phase velocity on transmission lines and showed it to increase in general for increasing losses. While the current literature describes the high-loss regime as a slow-wave "mode" distinct from quasi-TEM propagation, it appears that transmission lines on lossy Si actually support a true quasi-TEM waveguide mode over very broad bandwidths, and can be adequately described with an appropriate RLGC model for certain ranges of substrate resistivity.

In this paper, we characterized the properties of coplanar waveguides (CPW's) on Si substrates with resistivites in the range of 1 $\Omega\cdot$ cm, fabricated by commercial CMOS foundries through MOSIS [8]. These CPW's are shown schematically in Fig. 1. As described in Section III, we applied accurate on-wafer measurement and calibration techniques to acquire frequency-dependent propagation constant and characteristic impedance data for our CPW's. Using these measured data, we calculated RLGC parameters as functions of frequency.

Further, in Section IV, we propose a general quasi-TEM model based on the physical parameters of the mentioned CMOS process to account for the two loss mechanisms on

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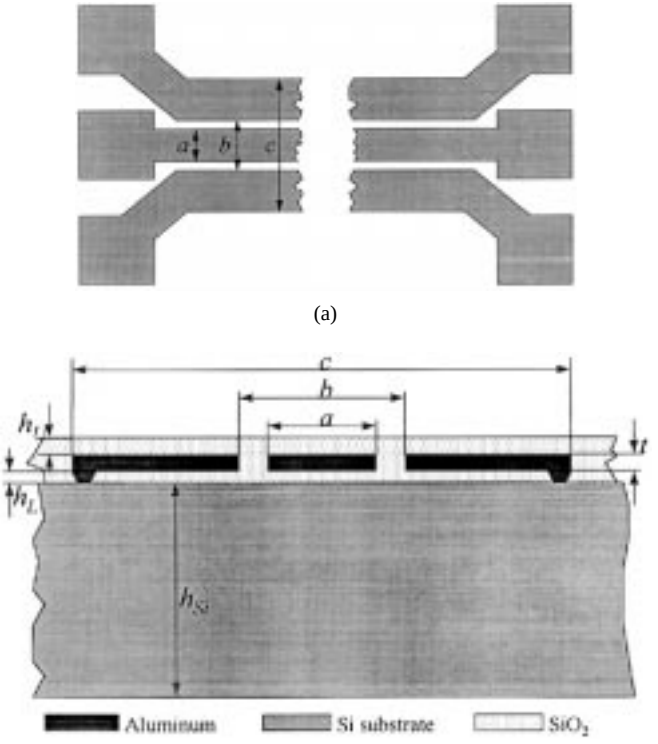


Fig. 1. CPW test structure. (a) Layout. (b) Cross-sectional view with pertinent dimensions.

TABLE I
DIMENSIONS AND PARAMETERS OF EXPERIMENTAL LINES

CPW Set	a [μm]	b [μm]	c [μm]	t [μm]	h_U [μm]	h_L [μm]	ρ_{Si} [Ω/cm]	ρ_{Al} [x10^{-6} Ω/cm]
1	24	30	130	0.6	1.65	1.45	12.5	3.0
2	60	68	300	0.6	1.65	1.45	11.5	3.0
3	60	68	300	1.15	1	2.1	11.5	3.0
4	60	68	300	1.75	1	1.45	11.5	3.0
5	60.9	69	364.2	1.35	1.4	1.03	0.434	3.0

either side of the Si relaxation frequency, and then compare this model to the measured RLGC parameters. The model is presented in terms of quasi-TEM equivalent circuits, shown in Fig. 2. The result is a model which circuit designers can use to estimate loss and phase factors as well as the characteristic impedance of their CMOS transmission lines given the starting process parameters.

II. DESIGN AND FABRICATION

For the experimental characterization, five test sets of CPW's with different dimensions were fabricated through three different standard CMOS processes available through the MOSIS service. The test sets differ in transverse line dimensions and in substrate resistivities to give a wider range of data for a better understanding of the propagation characteristics. The line dimensions and other parameters, as outlined in Fig. 1, are listed in Table I for all the sets. The layouts for the transmission lines were created using standard computer-aided design (CAD) graphics-layout editors. The conductor strips were designed using, in some cases, the first layer metal (aluminum), in some cases, the second layer metal, and in some cases, both metals, to provide less series

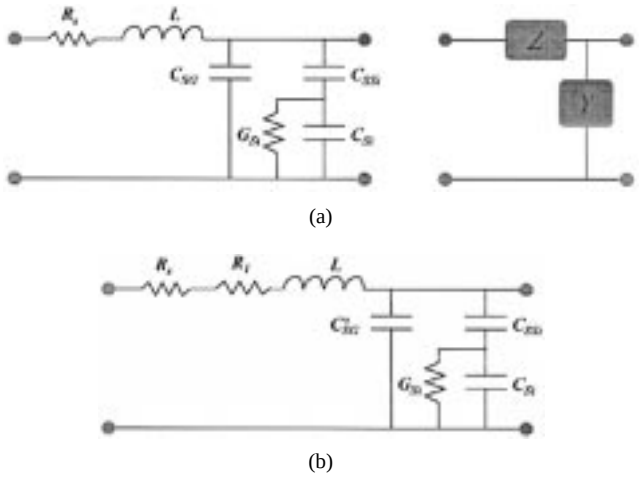


Fig. 2. Quasi-TEM equivalent circuit. (a) Theoretical model (Model A). (b) Empirical model (Model B).

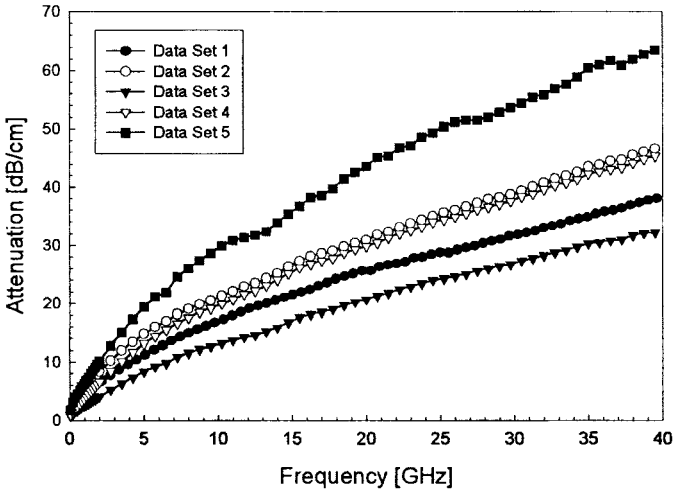
resistance. All of the structures were fabricated on p-substrates in analog n-well processes. Due to standard CMOS processing, the center conductor is fully encapsulated in layers of glass, while the ground planes make ohmic contacts to the underlying substrate, as illustrated in Fig. 1. The waveguides connect with electrical probing pads in the ground–signal–ground (GSG) configuration with 100-μm pitch, and in some cases, 150-μm pitch. The pads consist of both first- and second-layer metal connected by many vias. As shown in Table I, test sets 1–4 were fabricated in a 2-μm CMOS n-well process; test-set 5 was fabricated in a 1.2-μm n-well process. For accurate measurement characterization, all of the necessary TRL components were designed in the same transverse geometry: lines of different lengths and reflection standards (short and/or open).

III. MICROWAVE MEASUREMENT SETUP AND PROCEDURE

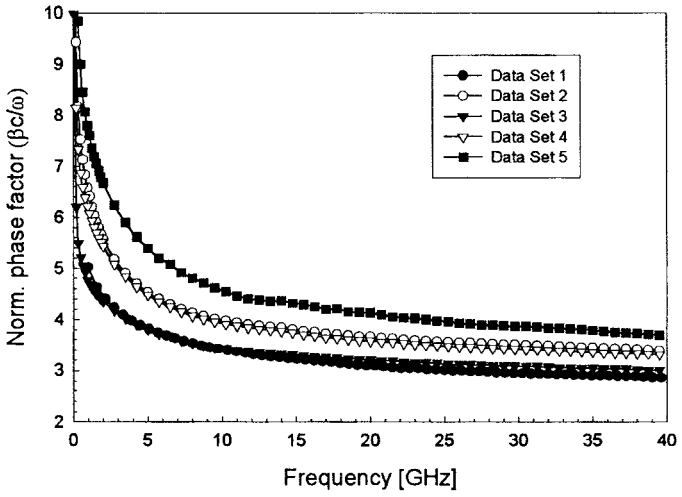
We characterized the CMOS transmission lines at frequencies from 100 MHz to 40 GHz using a commercial automatic network analyzer, microwave probing station, and the multiline through-reflect-line (TRL) calibration technique [9], [10]. We measured the propagation constant (attenuation and phase factors of the lines), and by implementing the calibration comparison method [11], determined the characteristic impedance of the lines. Finally, knowing the propagation constant and characteristic impedance of the lines, we calculated the total resistance R, inductance L, capacitance C, and conductance G per unit length of the transmission lines [7].

Measurements were made on five separate calibration sets located on three distinct chips. These sets varied in metal thickness, conductivity, and geometry. The longest delay line for all of the layouts was approximately 4.0 mm in length, while the through lines were close to 0.8-mm-long. Probe placement on the contact pads had to be performed with micron scale precision in order to ensure accurate measurements.

The multiline TRL calibration method provides an exact solution for the propagation constant accounting for all the transmission and reflection parameters (S_{ij}) from two or more lines of varying lengths. In contrast to other propagation-constant measurement techniques, multiline does not make any port–match assumptions. As shown in previous work, it



(a)



(b)

Fig. 3. Measured complex propagation constant for data sets listed in Table I. (a) Attenuation. (b) Normalized phase factor.

provides accurate frequency-dependent propagation constants even when the characteristic impedance of the lines significantly differs from the reference impedance of the system [12].

To determine the propagation constant in this study of CMOS transmission lines, we measured two lines of different lengths. Then, using the NIST MultiCal software with an estimate of the effective dielectric constant, we solved for the propagation constant according to the multiline TRL equations [10]. The propagation constant is determined irrespective of the system calibration, so the accuracy is limited only by the random errors encountered in measuring the two lines and by the accuracy of the length difference. For S-parameter measurements with our system, the magnitude of the worst-case repeatability bound is typically less than 0.01 over the frequency range studied here [11]. The propagation constant data are shown in Fig. 3 as the attenuation factor (α) and normalized phase factor $(\beta c/\omega)$.

We made use of the calibration comparison technique [11] to determine the characteristic impedance of our lines. This method was chosen over conventional techniques since it has been shown to generate more accurate results over broad bandwidths [11]. By measuring the S-parameters of our transmission lines with respect to a reference multiline calibration (GaAs CPW referenced to the probe tips), we could apply this method to directly determine the characteristic impedance of our unknown lines. Finally, with the propagation constant and characteristic impedance known, we could calculate the frequency-dependent equivalent-circuit parameters per unit length of line (R, L, C, and G) by

$$j\omega C + G \equiv \frac{\gamma}{Z_0} \tag{1}$$

and

$$j\omega L + R \equiv \gamma \cdot Z_0 \tag{2}$$

where γ is the complex propagation constant, and Z_0 is the complex characteristic impedance of the CPW.

While the propagation constant measurements are limited only by system repeatability, the RLGC parameters are limited to two sources of uncertainty. The first is the valid range of calibration based on the multiline TRL standards. We designed our lines to have a minimum error at 20 GHz, with increasing errors at low frequencies due to the short line length, and increasing errors around 40 GHz due to the half-wavelength approaching that of the differences in line length [10]. From our measurements, we determined the range of valid calibration to extend from 3 to 40 GHz. For frequencies decreasing below 3 GHz, the data will be susceptible to increasing calibration errors.

The lack of probe pad compensation is the second major source of uncertainty in the RLGC measurements. The calibration comparison method of determining Z_0 [11] requires the pads of the test lines to exactly match that of the reference calibration structures, or to be symmetrical. If not, a separate measurement of the pads must be made to compensate for the differences. In our test wafers, we did not have access to an isolated pad, and could not compensate our Z_0 measurements accordingly [24]. Consequently, in comparing models to measurement, we consider the probe pad contribution as uncertainty in the data. This source far exceeds the calibration and repeatability limits over our frequency range.

The measurements of attenuation for each line are shown in Fig. 3(a). As seen in this figure, the attenuation becomes very high for frequencies above 10 GHz, and exceeds 20 dB/cm at 20 GHz. This is mainly due to the currents in the relatively highly conductive Si substrate, as will be shown in the following analysis. Though some of the attenuation is due to losses in the thin metal conductors, this contribution is substantially less than the substrate contribution at high frequencies, as demonstrated in our previous work on fully suspended CPW's where Si substrate is etched away [13]. Fig. 4 shows the real and imaginary parts of the measured complex characteristic impedance for set 2, Fig. 5 shows real and imaginary parts of the measured propagation constant for the same set, and Fig. 6 shows the RLGC parameters for the same set as computed from these with (1) and (2).

IV. Quasi-TEM Model

At higher frequencies, modeling of transmission lines in VLSI circuits in terms of the simple *RC* model is

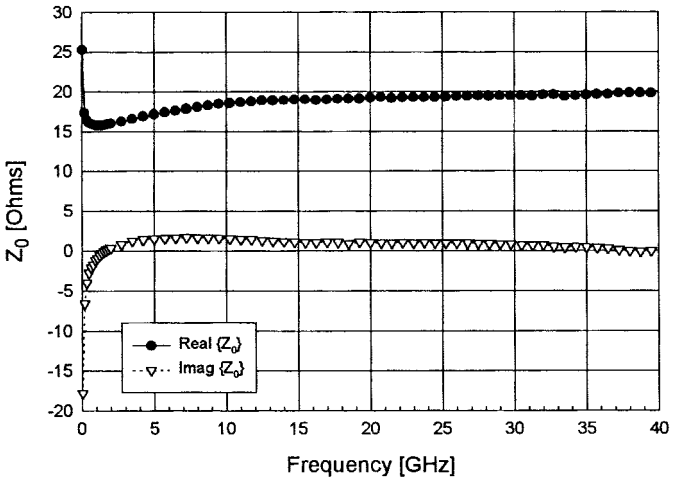
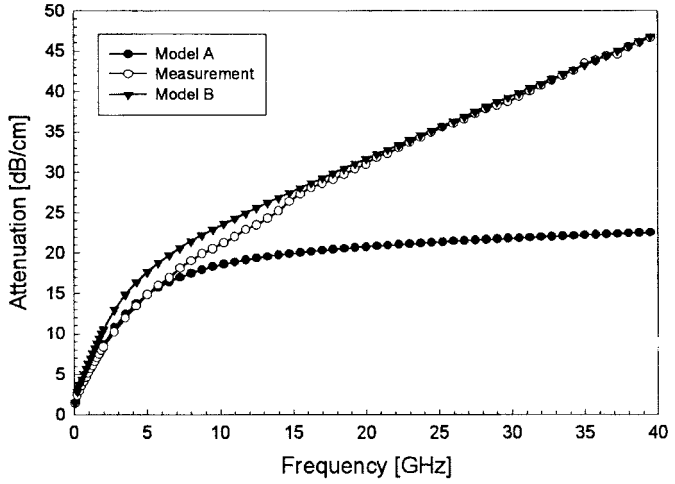
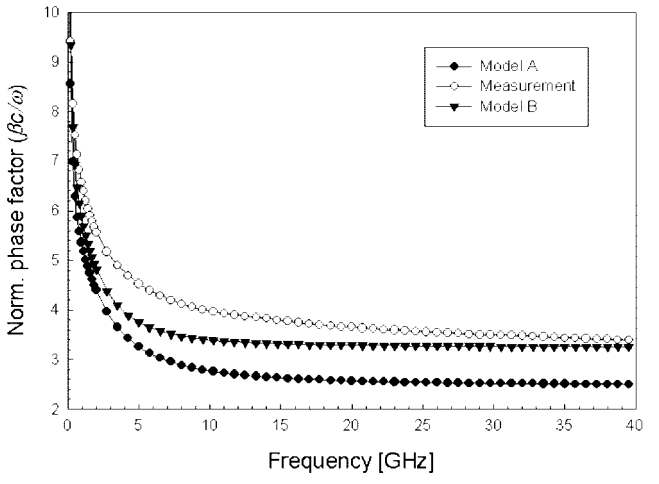


Fig. 4. Measured complex characteristic impedance for data-set 2.



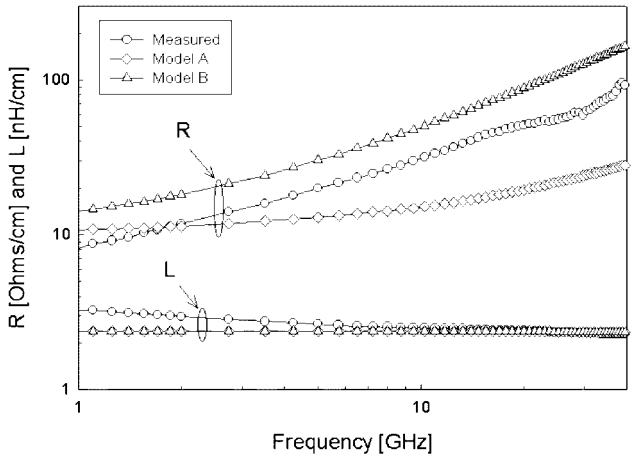
(a)



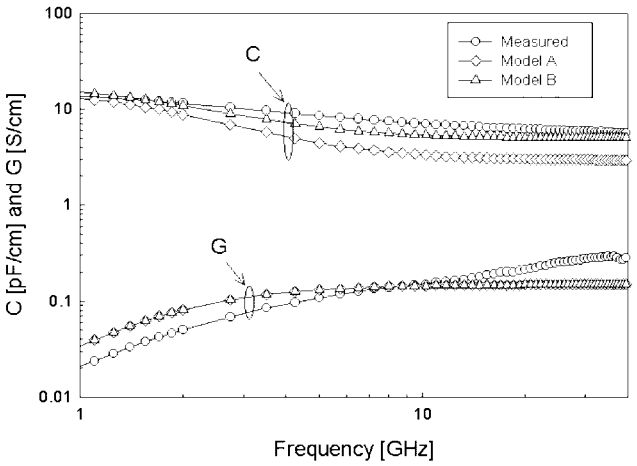
(b)

Fig. 5. Comparison of measured and modeled (a) attenuation and (b) normalized phase factor for data-set 2.

insufficient. To account for the propagation effects in the CPW structures, we use a physical equivalent circuit of a differential line length dz, which models the effects of the transverse electric and magnetic fields. From the equivalent



(a)



(b)

Fig. 6. Comparison of measured and modeled RLGC parameters for data-set 2.

circuit, we obtain the four transmission-line components of a corresponding RLCG transmission-line model. The components are expressed as real and imaginary parts of the series impedance per unit length, and shunt admittance per unit length of the transmission line. Such lumped-element models have been widely used in transmission-line design and theory and, although approximate, are simple and computationally efficient. However, they are only accurate for quasi-TEM mode analysis. The main assumption of the analysis is that the transverse fields carry the majority of the electromagnetic energy. This assumption is valid as long as the transverse CPW dimensions are much smaller than the shortest wavelength of the applied signals, and the losses are not excessive. In our experimental test sets, the largest transverse dimension is nearly 400 μm, satisfying the former criteria well throughout the experimental frequency range.

To analyze the CPW of Fig. 1, we developed the equivalent circuits in Fig. 2. The circuit in Fig. 2(a) includes elements from the model of Shibata and Sano [4], which was derived from a full-wave computer analysis of a similar metal–insulator–semiconductor (MIS) structure. The results of

the full-wave analysis in [4] show that two different regimes of propagation take place, thereby leading to the model as shown in Fig. 2(a), where the relaxation between two modes is taken into account in terms of circuit elements $C_{\rm Si}$ and $G_{\rm Si}$. Capacitors $C_{\rm SSi}$ and $C_{\rm SG}$ represent the signal-to-Si substrate and signal-to-ground plane capacitances, respectively. The conductance $G_{\rm Si}$ is due to transverse currents induced in the Si substrate by the electric field, while $C_{\rm Si}$ similarly represents transverse displacement currents. Both $C_{\rm Si}$ and $G_{\rm Si}$ are given by the electrical energy stored in the substrate, and can be combined in a complex element $Y_{\rm Si}$ by introducing complex permittivity or complex conductivity of the substrate.

The effects of the longitudinal currents and transverse magnetic field are modeled in terms of components R_s and L. Elements L and R_s are the inductance and resistance of the aluminum conductors, respectively. However, the longitudinal losses cannot be adequately described by considering only the conductor losses. We used an additional resistance R_l in series with R_s to represent longitudinal current losses in the Si beneath the signal strip.

The shunt capacitors $C_{\rm Si}$, $C_{\rm SSi}$, and $C_{\rm SG}$ model the transition from the slow-wave "mode" at lower frequencies to the dielectric quasi-TEM "mode" at higher microwave frequencies. Namely, in the low-frequency limit, the conductance $G_{\rm Si}$ effectively shunts $C_{\rm Si}$, and the total capacitance is mainly the glass capacitance $C_{\rm SSi}$. In the limit of frequency equal to infinity, the capacitances make up the total dielectric quasi-TEM limit capacitance C_d.

The CPW cross section with multilayer dielectrics, as shown in Fig. 1, can be analyzed by conformal mapping [14], [15]. The method allows us to compute geometry factors from which we can compute the capacitance per unit length C_0 of an equivalent air-filled line, and in general, allows us to compute the stored electric energy in any of the surrounding dielectrics. The accuracy of the computation depends on the validity of the approximation to the solution of the ratio of the elliptic integrals of first order. For CPW's with finite-thickness metals and finite-extent ground planes, even in the case of air dielectric, three sequential conformal transformations would be required to obtain simple expressions for capacitance [16], [17]. In general, it is very difficult to obtain closed-form expressions for all three stages of the transformation, and various approximations are often employed [17]. In this paper, we use a simple approximation for the finite-thickness metal contribution to the capacitance by adding the capacitance between the metal sidewalls to the zero-thickness capacitance. This gives better results than simply assuming a zero-thickness case, and does not require additional computation. Hence, the capacitance per unit length C_0 of an equivalent air-filled transmission line can be found from the following expression:

$$C_0 = 4 \cdot \varepsilon_0 \cdot \left[F + \frac{t}{(b-a)} \right]. \tag{3}$$

In (3), F is the geometry factor for a conformally mapped air-filled zero-thickness CPW of finite-extent ground planes, which was derived by Veyres and Hanna [15] as follows:

$$F = \frac{K(k')}{K(k)} \tag{4}$$

where $K(k)$ is the complete elliptic integral of the first kind, and k is the argument of the integral, expressed in terms of the CPW dimensions as

$$k = \frac{c}{b}\sqrt{\frac{b^2-a^2}{c^2-a^2}}$$
$$k' = \sqrt{1-k^2}. \tag{5}$$

The ratio of elliptic integrals in (4) can be obtained by computation or approximated by the following expressions [18]:

$$\frac{K(k)}{K(k')} \cong \begin{cases} \frac{1}{2.0\cdot\pi} \cdot \ln\left(2 \cdot \frac{\sqrt{1+k}+\sqrt[4]{4.0\cdot k}}{\sqrt{1+k}-\sqrt[4]{4.0\cdot k}}\right), & 0.707 \le k \le 1.0 \\ \dfrac{2.0\cdot\pi}{\ln\left(2 \cdot \frac{\sqrt{1+k}+\sqrt[4]{4.0\cdot k}}{\sqrt{1+k}-\sqrt[4]{4.0\cdot k}}\right)}, & 0.0 \le k \le 0.707. \end{cases} \tag{6}$$

While we found the above approximate expressions of (3)–(6) sufficiently accurate for our application, there are other proposed expressions for CPW's with finite-extent ground planes available in the literature [19], [20]. Also, simpler expressions are often found which use only the two parameters a and b [6], [16]. In those cases, infinite ground planes on both sides are assumed, which is often an adequate assumption. In the case of our experimental CPW's, the ground planes extend for a limited distance. Therefore, all three parameters a, b, and c are included in the computation of F.

The equivalent air capacitance is employed to obtain per-unit-length inductance L_∞ of a lossless perfectly conducting line with the same dimensions as follows:

$$L = \frac{1}{c^2 \cdot C_0}. \tag{7}$$

The presented structures have very small dimensions and have very thin conducting layers (less than 1.5-μm thickness) $t_{\rm Al}$; therefore, the sheet resistance of the metal cannot be neglected. The series resistance in the metal conductor is normally not a function of frequency, and the value could actually be looked up from MOSIS parameters which are provided after fabrication (included in Table I). However, as frequency increases, the skin depth in the metal becomes less than the metal thickness, so the resistance becomes a function of frequency. In order to find the frequency dependence of R_s, we first calculated the internal impedance for each conductor by using the phenomenological loss equivalence method (PEM) introduced in [21]

$$Z_i = (1+j) \cdot R_{\rm surface} \cdot g \cdot \coth\left[\frac{(1+j)\cdot g \cdot A}{\delta_{\rm Al}}\right] \tag{8}$$

where $R_{\rm surface}$ is the surface resistance of the aluminum conductors ($R_{\rm surface} = 1/(\sigma_{\rm Al} \cdot \delta_{\rm Al})$), parameter A is the cross-sectional area of the conductors (for center conductor $A = a \cdot t_{\rm Al}$, and each ground conductor $A = (c-b)\cdot t_{\rm Al}/2$), $\delta_{\rm Al}$ is the skin depth in the aluminum conductor defined as

$$\delta_{\rm Al} = \sqrt{\frac{2}{\omega \cdot \mu \cdot \sigma_{\rm Al}}}. \tag{9}$$

The geometrical factor g in (8) is shown in [21] to be the derivative of external inductance with respect to the incremental recession in conductor walls as a function of

frequency. Namely, due to the finite conductivity of the metal, the inductance and resistance contribution from the currents within the conductors is represented by the factor g as follows. At each frequency, the skin depth is computed by (9), and (3)–(7) are applied on the resulting equivalent perfectly conducting CPW, with the dimensions of all three conductors recessed by $\delta_{\mathrm{Al}}/2$ from each side. As a result, we obtain frequency-dependent external inductance L_δ. Lastly, we compute the factor g as

$$g = \frac{1}{\mu}\frac{\partial L_\delta}{\partial \delta}. \tag{10}$$

Then R_s is given by the real part of the total impedance in the metal conductors

$$R_s = \Re\left(Z_{i,\mathrm{center}} + \frac{1}{2}Z_{i,\mathrm{ground}}\right) \tag{11}$$

while L is given by the sum of L_∞ and the imaginary part of the same impedance

$$L = L_\infty + \Im\left(Z_{i,\mathrm{center}} + \frac{1}{2}Z_{i,\mathrm{ground}}\right). \tag{12}$$

In order to take into account the longitudinal losses in the substrate, Kwon *et al.* [6] proposed a parallel resistor R_l, which is calculated in terms of the skin depth inside the substrate, linewidths, and substrate resistivity. Seguinot *et al.* [22] used a series resistor in their model to account for the same losses. But for the skin effect to become significant, the conductivity of the substrate must be much higher than 1 S/cm for the substrate thicknesses from the commercial processes. On the other hand, the measurements indicate that the resistance in the longitudinal circuit increases with larger slope than R_s does [see Fig. 6(a)]. The skin-effect resistors both for conductor and substrate give $\sqrt{f}$-type increase with frequency [17]. In this paper, we added a series resistor R_l, which changes linearly with frequency and gives almost the same slope as the measurement. The results for data-set 2 are shown in Figs. 5 and 6. The empirical R_l is given in (13) and the resulting circuit is illustrated in Fig. 2(b).

$$R_l = \frac{1}{2}\sigma_{\mathrm{Si}} \cdot \omega \cdot \mu_0. \tag{13}$$

This expression approximately corresponds to two-sided skin effect in the substrate. Therefore, the total impedance per unit length of the longitudinal circuit is given by

$$Z = \frac{1}{\frac{1}{R_l} + \frac{1}{j\cdot\omega\cdot L + R_s}}. \tag{14}$$

Capacitance C_{SSi} is the capacitance found between the center conductor and the underlying substrate, which is simply found from the linewidth a and the oxide permittivity. However, due to the relatively small widths of the lines, the effects of the fringing fields should not be neglected. To obtain a more accurate value for the capacitance C_{SSi}, we computed it numerically by using commercial finite-element two-dimensional electrostatic simulations. From numerically obtained results for C_{SSi}, and by using several linewidths a, we arrived at an approximate equation which accounts for the extra capacitance from the conductor edges. Capacitance C_{SSi} is, therefore, found from

$$C_{\mathrm{SS}} = \varepsilon_{\mathrm{OX}} \cdot \left(\frac{a}{t_{\mathrm{OX}}}\right) + 1.5\varepsilon_{\mathrm{OX}} \cdot \left(\frac{a}{t_{\mathrm{OX}}}\right)^{0.1} \tag{15}$$

where the first part of the equation defines the capacitance when fringing effects are neglected. The relation in (15) is only approximate; methods for more accurately computing the fringing effects can be found in [23].

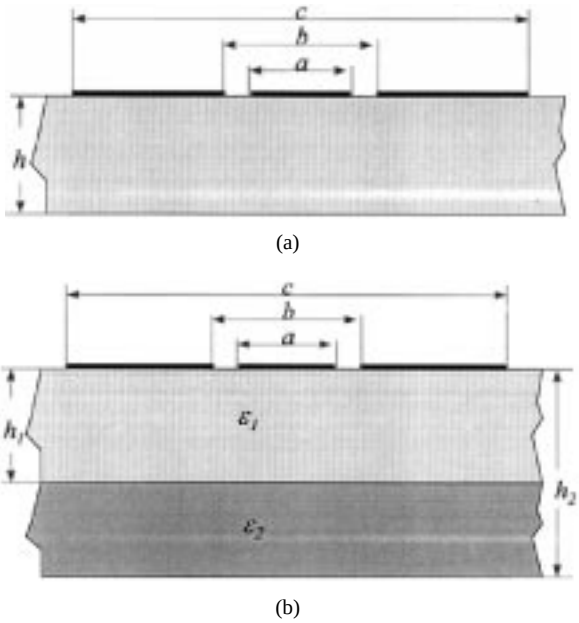


Fig. 7. Simplified cross section of zero-thickness CPW with multilayer dielectric to determine capacitance due to one of the layers.

The transverse-field effects in the substrate are approximated as a parallel G_{Si} and C_{Si} equivalent circuit. The field distribution in the substrate and the total electric energy stored are approximated by the conformal mapping of the multilayer dielectric structure in Fig. 7. Using the partial-capacitance approach and conformal mapping method, as described in detail in Appendix A, we find the geometry factor F_{Si}

$$F_{\mathrm{Si}} = F(\infty) - F(h). \tag{16}$$

The transverse-drift current flow, represented by conductance G_{Si}, is approximated by

$$G_{\mathrm{Si}} = 2 \cdot \sigma_{\mathrm{Si}} \cdot F_{\mathrm{Si}}. \tag{17}$$

Because the analysis must be valid at frequencies where the substrate acts as a dielectric, i.e., where the assumption $\sigma_{\mathrm{Si}} \gg \omega \cdot \varepsilon_{\mathrm{Si}}$ is not valid, the transverse capacitance C_{Si} is included in the model. The capacitance is also approximated from the geometric factor F as

$$C_{\mathrm{Si}} = 2 \cdot \varepsilon_{\mathrm{Si}} \cdot F_{\mathrm{Si}}. \tag{18}$$

The capacitance between the signal line and the ground lines in the slow-wave limit C_{SG} should be determined such that the total capacitance in the limit of frequency equal to infinity corresponds to C_d as follows:

$$C_d = C_{\mathrm{SG}} + \frac{C_{\mathrm{SS}} \cdot C_{\mathrm{Si}}}{C_{\mathrm{SS}} + C_{\mathrm{Si}}}. \tag{19}$$

The capacitance in the high-frequency limit for a CPW is commonly found from the air capacitance C_0 and the high-frequency effective dielectric constant as follows:

$$C_d = C_0 \cdot \varepsilon_{\text{eff}} = C_0 \cdot \frac{(\varepsilon_{\text{Si}} + 1)}{2}. \tag{20}$$

The capacitance C_d can be found much more accurately by again referring to the method described in Appendix A, and computing the total capacitance of a uniform transmission line as a superposition of partial capacitances due to each dielectric layer. Because of the different structures above and below the CPW, the total capacitance C_d can be expressed as

$$\begin{aligned} C_d &= C_{\text{upper\_half}} + C_{\text{lower\_half}} + C_{ba} \\ &= \{2[(\varepsilon_{\text{OX}} - 1) \cdot F(h_U) + F(\infty)]\} \\ &\quad + \{2[(\varepsilon_{\text{OX}} - \varepsilon_{\text{Si}}) \cdot F(h_L) + \varepsilon_{\text{Si}} F(\infty)]\} + 4 \cdot \frac{\varepsilon_{\text{OX}} \cdot t}{b - a}. \end{aligned} \tag{21}$$

In (21), C_{ba} corresponds to the capacitance between the vertical walls of conductors.

The propagation constant measurements showed a slower phase velocity than is predicted by the circuit. This can be seen in the simulation results in Figs. 5 and 6. To account for this in the empirical model of Fig. 2(b), we changed C_{SG} to

$$C'_{\text{SG}} = C_d. \tag{22}$$

From the shunt circuit elements, the total shunt admittance per unit length is found from

$$Y = \frac{1}{\frac{1}{j \cdot \omega \cdot C_{\text{SS}}} + \frac{1}{j \cdot \omega \cdot C_{\text{Si}} + G_{\text{Si}}}} + j \cdot \omega \cdot C_{\text{SG}}. \tag{23}$$

The complex propagation constant γ and the complex characteristic impedance Z_0 are determined from Z and Y as follows:

$$\gamma = \alpha + j \cdot \beta = \sqrt{Z \cdot Y} \tag{24}$$

$$Z_0 = Z' + j \cdot Z'' = \sqrt{\frac{Z}{Y}}. \tag{25}$$

V. Comparison of Model to Measurement

We have simulated our transmission line using the models from the previous sections for the given line dimensions and calculated the complex propagation constant and complex characteristic impedance at interval frequencies from 0.1 to 40 GHz. For the simulations, values for line dimensions and process parameters from Table I were used. The results of the calculations of the complex propagation constants for data-set 2 are shown in Fig. 5 in terms of the loss per centimeter length and normalized phase factor, respectively.

The attenuation measurements reflect the change from slow-wave propagation to dielectric quasi-TEM propagation. The attenuation rises nearly linearly with increasing frequency. The different regions of propagation are seen with different slopes. The same trend is found in the models, where the transition was imposed by properly selecting shunt circuit capacitances. Model A [see Fig. 2(a)] exhibits excellent agreement with measurement at low frequencies, but in the quasi-TEM dielectric "mode" it becomes inadequate. The improved empirical model [in Fig. 2(b)] shows excellent agreement at high frequencies.

The transition from the slow-wave "mode" to the dielectric quasi-TEM "mode" is more evident in the effective permittivity measurements and model results. The effective permittivity is extremely high at the lower end of frequencies where very low-phase velocities were expected and measured. At frequencies above 20 GHz, the permittivity became nearly level, with a phase velocity expected from a mixed dielectric of Si and air. But the comparison of phase velocities in Fig. 5(b) shows a clear difference at high frequencies. The measurements indicate more capacitance than the models do. In the empirical model, we increased C_{SG} to C_d to meet the additional capacitance requirement. Also, the transition region between the slow-wave "mode" and the quasi-TEM dielectric "mode" is much wider in the measurement.

Fig. 6 compares the RLGC parameters computed from the equivalent-circuit models to those extracted from Z_0 and γ measurements. Though Model A is better at predicting G, and is not significantly different than Model B in predicting L, the empirical model (Model B) is significantly better at predicting the measured R and C values. For the particular test set under consideration (test-set #2), Model B predicts the frequency-dependent transmission-line parameters within the measurement uncertainty limits from 1 to 18 GHz, and remains close all the way to 40 GHz. Model A (primarily in R values) exceeds the measurement uncertainty limit for frequencies greater than 5 GHz.

VI. Discussion

We observed two deviations from the theoretical expectations. The change of the attenuation and the phase velocity above 20 GHz differs significantly from the previous theoretical expectations [4], [6]. The observed linear increase of attenuation in decibels/centimeters with frequency cannot be modeled using a skin-effect resistor in series in the longitudinal circuit alone. On the other hand, the physical nature of the problem requires that the longitudinal losses in the substrate be included in series in the longitudinal circuit. We used an empirical resistance R_l, which roughly corresponds to two-dimensional skin effect independent from the geometry of the CPW.

Another important result is that the capacitance in the transverse circuit of Model A did not fully account for the measured propagation constant of the lines. The additional capacitance in Model B provided the necessary correction while improving the agreement with measured R and C data. However, the additional capacitance required here may indicate a missing delay element in the longitudinal model, such as an inductive term related to the induced currents in the semiconductor. Currently, such a term could not be determined in closed form.

A result that is particularly interesting due to CMOS fabrication is the large difference in attenuation among the three data-sets #2–#4. All three of those CPW designs have the same transverse (CAD layout) dimensions, but were designed using different combinations of the two metal layers available

through the CMOS process. Firstly, as expected for data-sets #2 and #4, the attenuation data is almost the same, with a slightly larger attenuation for data-set #2. This is due to the thicker conductors used in data-set #2, which are made by combining first- and second-layer metals. However, data-set #3 has the lowest attenuation of all five sets. This is also expected, since in this case, only the second-layer metal was used which is higher above the Si substrate, as shown by the largest parameter h_L in Table I. This again shows that the substrate losses dominate our transmission lines, and that the propagation characteristics for CPW's in CMOS are largely a function of the type and thickness of dielectric in the process.

VII. Conclusion

We have measured and simulated CPW's with different dimensions fabricated on Si substrates of commercial CMOS processes. Our measurements give an accurate characterization of the complex propagation constant in these lines. Along with the measured characteristic impedance, the measurements provide the RLGC line parameters which allow us to better determine the necessary elements of equivalent-model circuits. The developed model predicts the measured frequency-dependent transmission-line parameters over a very broad frequency range from 0.1 to 40 GHz. We have, however, also identified a number of limitations in the models and measurements, setting the pace for future work.

Appendix A
Multilayer Capacitance Determination by Conformal Mapping

In a more general way, the geometrical factor in (4) can be defined as a function of the thickness of the nearest dielectric layer. Fig. 7(a) shows a hypothetical structure which consists of only zero-thickness conductors and a dielectric layer with thickness h. The geometrical factor for such a structure is given as

$$F(h) = \frac{K(k'(h))}{K(k(h))} \tag{26}$$

where the arguments are expressed in terms of the dimensions

$$k(h) = \frac{c(h)}{b(h)}\sqrt{\frac{b^2(h) - a^2(h)}{c^2(h) - a^2(h)}}. \tag{27}$$

Here, $a(h)$, $b(h)$, and $c(h)$ are the transformed dimensions and transformation defined as

$$x(h) = \sinh\left(\frac{\pi \cdot x}{2h}\right), \qquad x = a, b, c. \tag{28}$$

The multilayer structures can be expressed as a superposition of hypothetical layers [15]. For example, the structure in Fig. 7(b) can be expressed as a superposition of two layers: one with thickness h_2 and dielectric constant ε_2, and one with h_1 and $(\varepsilon_1 - \varepsilon_2)$, respectively. Then using these hypothetical layers, the capacitance of the real structure is calculated. In our case, the total half-plane capacitance for the structure in Fig. 7(b) is

$$C_{\text{half-plane}} = \varepsilon_0[\varepsilon_2 \cdot F(h_2) + (\varepsilon_1 - \varepsilon_2) \cdot F(h_1)] \tag{29}$$

or

$$C_{\text{half-plane}} = \varepsilon_0[\varepsilon_2 \cdot (F(h_2) - F(h_1)) + \varepsilon_1 \cdot F(h_1)]. \tag{30}$$

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