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Electrical Measurements of Microwave Flip-Chip Interconnections

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Abstract

We apply custom calibration standards and software to the accurate on-wafer measurement of components on flip-chip coplanar-waveguide MMICs. We characterize transmission lines, MIM capacitors, and spiral inductors and develop equivalent circuit models. The results are applicable to the development of an accurate CAD database.

Key words: coplanar waveguide; electronics packaging; flip-chip; interconnection; MMIC; transmission line

INTRODUCTION

This paper describes microwave measurements of passive components on monolithic microwave integrated circuits (MMICs) built using coplanar waveguide (CPW) transmission lines and designed for flip-chip mounting. We use custom, on-wafer calibration standards along with the calibration software MultiCal, which implements the multiline TRL (through-reflect-line) calibration [1] with correction for nonideal characteristic impedance [2,3]. This method, which provides precisely defined measurement reference planes and reference impedance, has been used by industry as a benchmark for determining the accuracy of commercial on-wafer calibrations [4]. Here we use the method to characterize transmission lines, on-chip metal-insulator-metal (MIM) capacitors, and spiral inductors, in all cases comparing to equivalent circuit models. Much of this work has been reported in prior conferences [5,6].

Flip-chip mounting, a natural packaging technique for coplanar waveguide components, has recently come into use. The process has the potential for low-cost, high-yield, high-volume applications. However, one potential roadblock is the lack of accurate electrical data for use in computer-aided design (CAD). Here we apply our measurements to determine parameters of component models, as would be useful in CAD. We are also pursuing the characterization of flip-chip bumps and the effect of mounting substrates on electrical performance.

Conventional wafer-probe calibrations make use of commercial artifact standards. Such "off-wafer" calibrations may be adequate in some cases but fail entirely in others [7]. Even for relatively simple problems such as those considered here, commercial techniques imprecisely specify the reference plane and thereby introduce uncertainty into the model.

FABRICATION

We fabricated coplanar waveguide structures on 625 μm GaAs. In some cases, a 0.1 μm layer of Si_3N_4 was deposited on the GaAs before metallization. The transmission lines were composed of approximately 6 μm of evaporated Ti/Au followed by 3 μm of plated Au. A 0.2 μm layer of Si_3N_4 was deposited after the first evaporated metal layer and etched off of all metal surfaces except the capacitors. After the second metal layer, the surface was passivated with 2 μm of SiO_2. This oxide layer, which supports the plating used to interconnect the CPW ground planes, spiral inductors, etc., was etched away from the transmission lines before plating. Finally, a second SiO_2 layer of 0.5 μm, 1 μm, or 2 μm, depending on the wafer, passivated the entire structure.

The CPW lines had nominal center conductor and gap widths of 50 μm. The ground planes were approximately 440 μm wide.

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CALIBRATION & MEASUREMENT

We calibrated a network analyzer and on-wafer probes using the multiline TRL calibration [1], which provides scattering (S) parameters normalized to the characteristic impedance Z_o of the line. For each wafer, we used two on-wafer lines of length 1.0 mm and 5.8 mm as calibration standards. Since we had only two line standards available, our calibration accuracy is poor near multiples of 12 GHz, where the difference in line lengths corresponds to multiples of half a wavelength [1]. Our measurements covered 0.25 to 40 GHz.

In each case, we moved the reference plane up to the test device using the line's propagation constant and loss; which are calibration by-products.

We determined Z_o of the CPW lines using the method of [2]. This method requires a knowledge of C_{dc}, the dc capacitance per unit length of the line. We measured C_{dc} by a modified version [5] of the "direct comparison method" of [3]. With Z_o determined, we could transform measured S parameters into Y or Z parameters.

TRANSMISSION LINES

We probed the surface of the CPW lines using a mechanical surface profilometer. Typical results are shown in Fig. 1. We observed the ground planes to be somewhat more than 1 μm thicker than the center conductors. We also found large wafer-to-wafer variations in metal thickness. The primary parameters of the lines are given in Table 1. The conductivity is computed using the measured dc resistance R_{dc}, assuming a rectangular center conductor and ignoring ground plane resistance.

Figure 2 shows the measured relative effective permittivity. The differences are due to dielectric as well as metal variations. However, the difference between lines B and H is attributable to conductor variations only, since no passivation was applied to these. Figure 2 also shows data obtained from a published CPW model [8], which assumes uniform metal thickness and ignores passivation.

The real part of the characteristic impedance Z_o is displayed in Fig. 3. It varies significantly with frequency and with CPW construction.

One good test of the CPW model is to plot the inductance per unit length L (Fig. 4), since L is virtually independent of dielectric and the computable for all lines. The measured and modeled results are well correlated.

COMPONENTS AND MODELING

If a component can be modeled as a π equivalent circuit, the series admittance y_s and the shunt admittances y_{p1} and y_{p2} can be easily extracted from the measured Y-parameters [9,6]. If y_s, y_{p1}, and y_{p2} are themselves described by simple networks, the network parameter values can be determined with little or no fitting. This fact was exploited in [9] for the modeling of microstrip spiral inductors. Here we use it in analyzing MIM capacitors (Fig. 5) and spiral inductors (Fig. 6).

MIM CAPACITORS

The series capacitors (Fig. 5) were composed of square parallel plates. The lower plate connected to port 1; the upper plate was built from second-layer metal and connected to port 2 using bridge metal. A 0.2 μm layer of Si_3N_4 separated the two plates. Based on prior processing experience, we estimated a capacitance of 282 pF/μm^2; this corresponds to a Si_3N_4 permittivity of 6.37. On each of four different wafers, we measured capacitors of three sizes. Capacitor 1 was 20 μm square, Capacitor 2 was 50 μm square, and Capacitor 3 was 132 μm square.

The measured and modeled Y parameters of Capacitors 2 and 3 showed prominent resonances (see Figs. 7-8). We used our measured Y parameters to determine the values in the equivalent circuit model inset in Fig. 7. As shown in Table 2, the measured values of C_s agree well with the estimates based on the plate size. The table includes the resonant frequency $f_r = \left(2\pi\sqrt{L_s C_s}\right)^{-1}$, which agrees closely with the observed value $f_r(Y_{12})$, obtained from $\mathrm{Im}(Y_{12})=0$. We ignored R_1 and R_2, since they were negligible.

SPIRAL INDUCTORS

Square spiral inductors (Fig. 6) were formed using 10 μm wide conductors. The outside of the spiral was connected to port 1 and the inside to port 2. The turns of the spiral crossed over this connection using bridge metal. Inductors 2 and 3 were formed from the same 6 μm metallization used in the transmission lines, with a spacing of 15 μm between the turns. Inductor 1 was built using only the 1.5 μm first metal layer, with 10 μm between the turns.

We analyzed the spiral inductors using the equivalent-circuit model inset in Fig. 9, identical to that used by [10] for microstrip spiral inductors.

We determined that C_s, G_1, and G_2 were negligible. The remaining parameters are shown in Table 3. Measured and modeled Y-parameters are shown in Fig. 9 and 10. The two agree well except near the measured 35 GHz resonance, which is not represented in the model.

CONCLUSIONS

With its potential for low cost and high reliability, the flip-chip CPW MMIC holds promise for large-scale introduction into consumer electronics. Design of such circuits, however, is hampered by the lack of reliable electrical data on circuit elements. Such data are difficult to obtain theoretically. On the other hand, carefully designed and conducted measurements can provide accurate data, with well-defined reference planes, that can readily be integrated into a CAD database for high-quality, first-pass circuit design.

Here, we have presented data on the characterization of on-chip components. Although the measured S, Y, or Z parameters may be used directly in CAD, a parameter-based representation is much more efficient in terms of data storage. Such a representation hinges on the development of appropriate models. If the models are based on the physical structure, the extracted values are also useful in component design. The models used here are a useful starting point but require refinement in order to represent the significant features.

In order to extend this work to the characterization of solder joints using the two-tier TRL calibration process, we have built an additional set of calibration structures on the ceramic mounting substrate. This will also allow the study of substrate loading effects.

Accurate TRL calibration over a broad band requires the use of multiple transmission lines as calibration standards. Our future work will incorporate additional standards.

ACKNOWLEDGEMENTS

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Table 1: Transmission Line Properties.

Line Label	Nitride Layer (μm)	First Oxide (μm)	Second Oxide (μm)	Measured R_{dc} (Ω/cm)	Measured C_{dc} (pF/cm)	Center Conductor Width	Gap Width (μm)	Ground Plane Thickness	Center Conductor Thickness	Measured Conductivity (S/m)
A	0.1	2	2	0.89	1.72	53 μm	48	7.9 μm	6.8 μm	$3.1 \cdot 10^7$
B	0	0	0	1.23	1.62	53 μm	48	5.4 μm	4.2 μm	$3.7 \cdot 10^7$
D	0	2	1	1.02	1.69	53 μm	48	6.9 μm	5.3 μm	$3.5 \cdot 10^7$
F	0	2	0.5	0.92	1.68	53 μm	48	7.5 μm	5.9 μm	$3.5 \cdot 10^7$
H	0	0	0	1.31	–	53 μm	48	5.3 μm	4.1 μm	$3.5 \cdot 10^7$

Table 2: Equivalent Circuit Values of Capacitors.

Capacitor Label	Wafer Label	Nitride Layer	1st Oxide	2nd Oxide	f_r (GHz)	$f_r(Y_{12})$ (GHz)	C_1,C_2 (fF)	R_S (Ω)	L_S (pH)	C_S (pF)	C_{est} (pF)
1	A	0.1 μm	2 μm	2 μm	81.7	>40	3.72	2.1	28.5	0.133	0.133
(20x20 μm)	B	0	0	0	85.6	>40	3.60	2.2	28.2	0.123	0.133
	D	0	2 μm	1 μm	84.0	>40	4.50	2.2	26.3	0.137	0.133
	F	0	2 μm	0.5 μm	79.1	>40	4.44	1.7	30.6	0.132	0.133
2	A	0.1 μm	2 μm	2 μm	31.5	31.6	7.71	0.18	34.4	0.743	0.705
(50x50 μm)	B	0	0	0	31.9	30.3	7.61	0.27	34.5	0.721	0.705
	D	0	2 μm	1 μm	31.2	30.1	8.53	0.32	35.0	0.745	0.705
	F	0	2 μm	0.5 μm	31.1	30.2	8.00	0.20	35.7	0.732	0.705
3	A	0.1 μm	2 μm	2 μm	9.69	9.63	26.1	0.11	54.2	4.98	4.91
(132x132 μm)	B	0	0	0	9.31	9.33	25.3	2.4	58.8	4.97	4.91
	D	0	2 μm	1 μm	9.58	9.37	28.6	0.17	55.5	4.97	4.91
	F	0	2 μm	0.5 μm	9.60	9.39	26.3	0.10	56.1	4.90	4.91

Table 3: Equivalent Circuit Values of Inductors.

Inductor Label	Wafer Label	Nitride Layer	1st Oxide	2nd Oxide	$f_r(Y_{12})$ (GHz)	C_1 (pF)	C_2 (pF)	R_S (Ω)	L_S (nH)
1	A	0.1 μm	2 μm	2 μm	>40	0.057	0.046	1.50	0.565
(2.5 turns)	D	0	2 μm	1 μm	>40	0.058	0.049	1.44	0.573
	F	0	2 μm	0.5 μm	>40	0.056	0.047	1.46	0.570
2	A	0.1 μm	2 μm	2 μm	34.5	0.111	0.066	1.50	2.12
(4.5 turns)	D	0	2 μm	1 μm	34.3	0.110	0.069	1.56	2.18
	F	0	2 μm	0.5 μm	35.4	0.106	0.066	1.53	2.11
3	A	0.1 μm	2 μm	2 μm	6.97	0.295	0.114	4.09	23.1
(10.5 turns)	D	0	2 μm	1 μm	6.90	0.289	0.117	3.66	23.7
	F	0	2 μm	0.5 μm	7.13	0.277	0.120	6.67	11.5

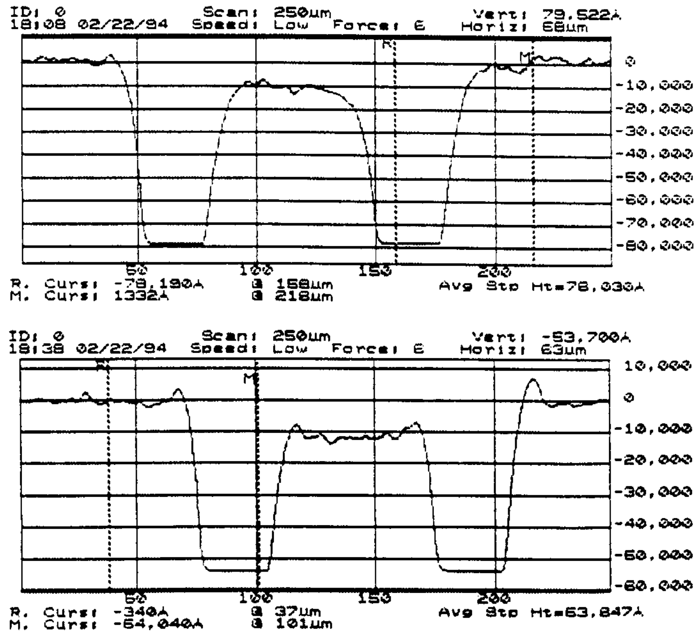

Fig. 1: Surface Profiles of Lines from Wafer A (top) and B (bottom)

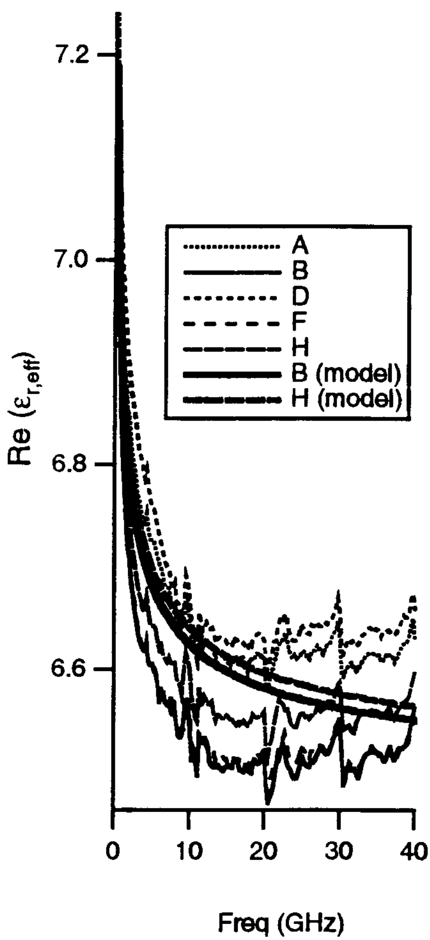

Fig. 2: Effective Relative Permittivity

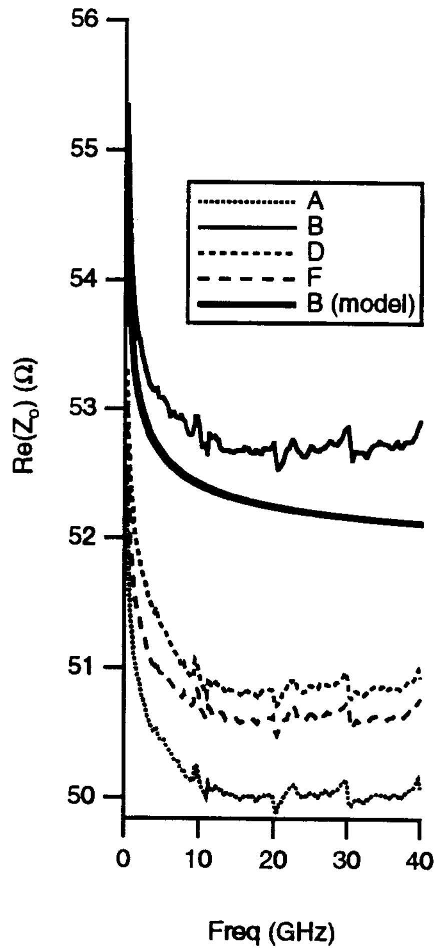

Fig. 3: Characteristic Impedance

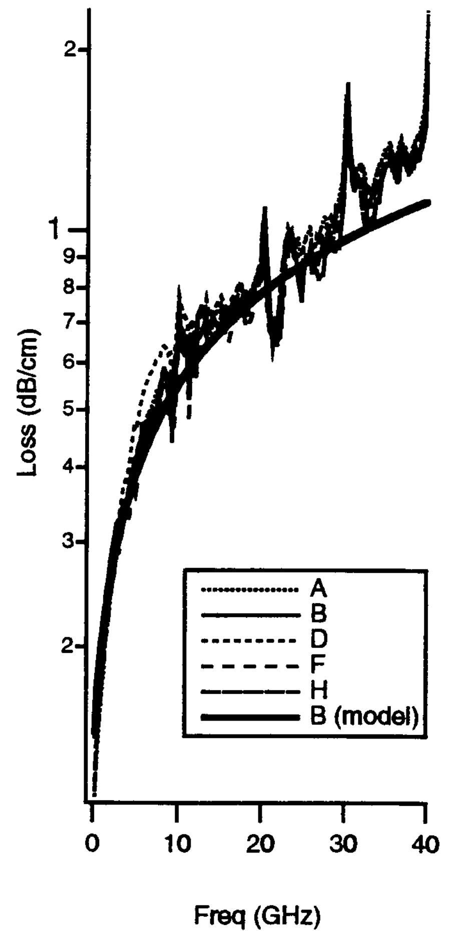

Fig. 4: Inductance per Unit Length

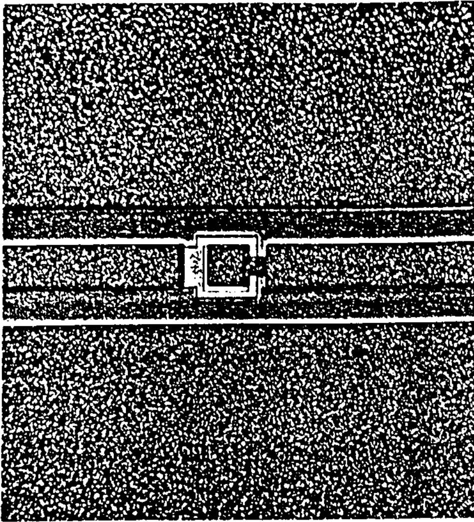

Fig. 5: Photo of Capacitor

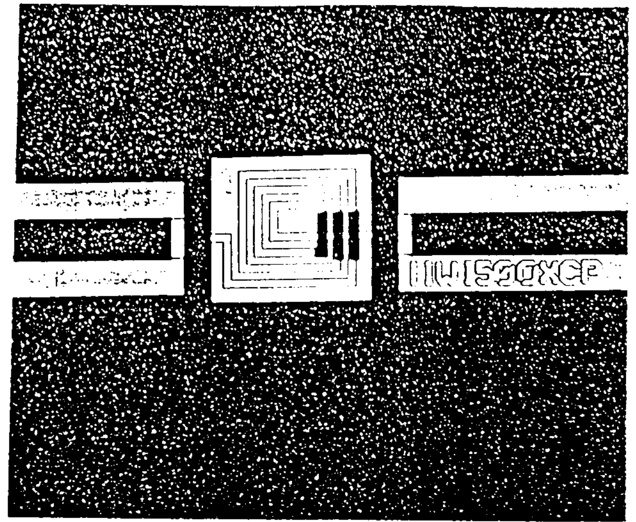

Fig. 6: Photo of Inductor

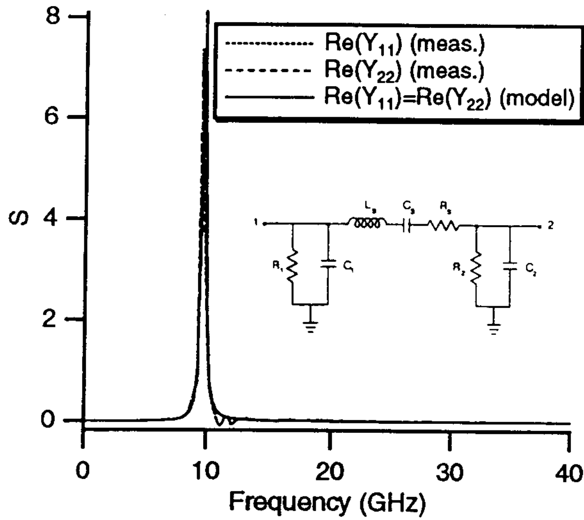

Fig. 7: $\mathrm{Re}(Y_{11})$ and $\mathrm{Re}(Y_{22})$, Capacitor 3, Wafer A

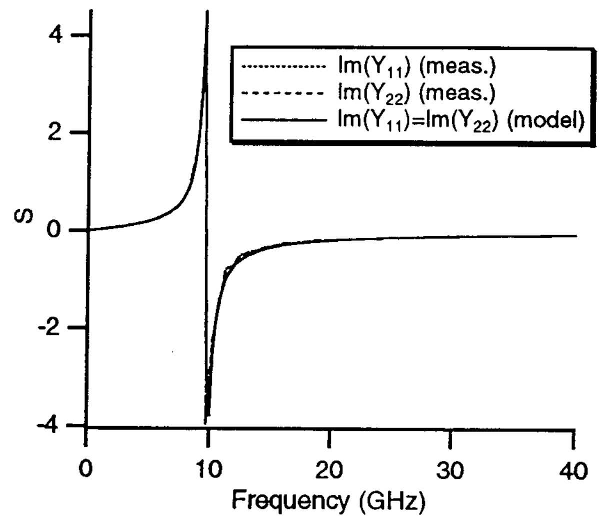

Fig. 8: $\mathrm{Im}(Y_{11})$ and $\mathrm{Im}(Y_{22})$, Capacitor 3, Wafer A

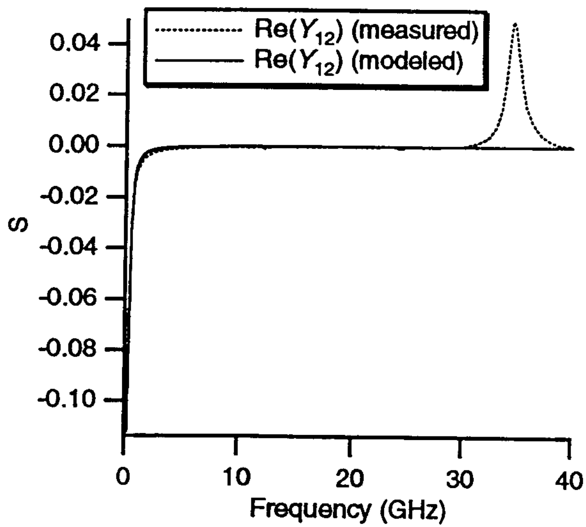

Fig. 9: $\mathrm{Re}(Y_{12})$ for Inductor 2, Wafer A

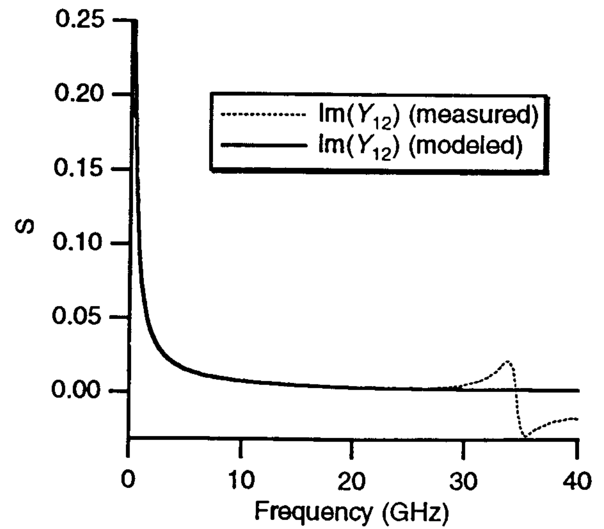

Fig. 10: $\mathrm{Im}(Y_{12})$ for Inductor 2, Wafer A