Microwave Characterization of Flip-Chip MMIC Components

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Abstract — **We apply custom calibration standards and software to the accurate on-wafer measurement of MIM capacitors and spiral inductors on flip-chip coplanar-waveguide MMICs. We suggest equivalent circuit models and document their deficiencies. The results are applicable to the development of an accurate CAD database.**

Introduction

In this paper, we report microwave measurements of passive components on monolithic microwave integrated circuits (MMICs) that are constructed using coplanar waveguide (CPW) transmission lines and designed for flip-chip mounting. We use custom, on-wafer calibration standards along with the calibration software MultiCal, which implements the multiline TRL (through-reflect-line) calibration [1] with correction for nonideal characteristic impedance [2,3]. This method, which provides precisely defined measurement reference planes and reference impedance, has been used by industry as a benchmark for determining the accuracy of commercial on-wafer calibrations [4]. For the flip-chip CPW considered here, it has been used to characterize transmission lines and determine their equivalent circuits [5]. Here we use the method to characterize on-chip metal-insulator-metal (MIM) capacitors and spiral inductors.

Flip-chip mounting, a natural packaging technique for coplanar waveguide components, has recently come into use [6,7,8]. The process has the potential for low-cost, high-yield, high-volume applications. However, one potential roadblock is the lack of accurate electrical data for use in computer-aided design (CAD). Here we apply our measurements to determine parameters of component models, as would be useful in CAD.

Conventional wafer-probe calibrations make use of commercial artifact standards. Such "off-wafer" calibrations may be adequate in some cases but fail entirely in others [9]. Even for relatively simple problems such as those considered here, commercial techniques imprecisely specify the reference plane and thereby introduce uncertainty into the model.

Fabrication

We fabricated coplanar waveguide structures using technology similar to that of [6] and [8]. The substrate was 625 μm GaAs. In some cases, a 0.1 μm layer of Si_3N_4 was deposited on the GaAs before metallization. The transmission lines were composed of approximately 6 μm of metal: 1.5 μm each of two layers of evaporated Ti/Au, followed by 3 μm of plated Au. A 0.2 μm layer of Si_3N_4 was deposited after the first evaporated metal layer and etched off of all metal surfaces except the capacitors. After the second metal layer, the surface was passivated with 2 μm of SiO_2. This oxide layer, which supports the plating used to interconnect the CPW ground planes, spiral inductors, etc., was etched away from the transmission lines before plating. Finally, a second SiO_2 layer of 0.5 μm, 1 μm, or 2 μm, depending on the wafer, passivated the entire structure. Tables 1 and 2 list the properties of the lines whose measurements are reported here.

The CPW lines had center conductor and gap widths of 50 μm and a ground plane width of approximately 440 μm.

Calibration and Measurement

We calibrated a frequency-domain network analyzer and on-wafer probe using the multiline TRL calibration [1], which provides scattering (S) parameters normalized to the characteristic impedance Z_o of the line. For each wafer, we used two on-wafer lines of length 1.0 mm and 5.8 mm as calibration standards. Since we had only two line standards available, our calibration accuracy is poor near multiples of 12 GHz, where the difference in line lengths corresponds to multiples of half a wavelength [1]. Our measurements covered 0.25 to 40 GHz.

Since the calibration also provides a measurement of the propagation constant and loss of the line, we are able to move the reference plane at will. In each case, we placed the reference plane in the uniform transmission line adjacent to the test device.

We determined Z_o using the method of [2]. This method requires a knowledge of C_{dc}, the dc capacitance per unit length of the line. We measured C_{dc} by a modified version [5] of the "direct comparison method" of [3].

A detailed study of the transmission line parameters is presented in [5]. Here we discuss only the characteristic impedance Z_o, the real part of which is displayed in Fig. 1 for several lines. The significant feature is that Z_o varies significantly with frequency and with CPW construction. As shown in [5], it can also vary greatly between nominally identical wafers due to variations in metal thickness or conductivity from lot to lot.

Due to these wide variations in Z_o, S parameters with reference impedance equal to Z_o will also vary greatly from lot to lot, even if the devices of interest are quite similar. Under these circumstances, the value of S parameters in CAD is limited unless the calibration method is able to measure and compensate for Z_o. One possibility is to transform to a 50 Ω reference impedance. Another is to use Z_o and the S parameters to compute the impedance (Z) or

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admittance (Y) parameters. Since these are largely insensitive to Z_o, we expect them to be much more repeatable, from lot to lot, than scattering parameters and therefore more suitable for use in a CAD database. Furthermore, Z or Y parameters are required for most lumped element models, including those presented below.

MODELING

If a component can be modeled as a π equivalent circuit, the three admittances y_s, y_{p1}, and y_{p2} (see Fig. 2) can be easily extracted from the measured Y-parameters by the equations

$$y_s = -Y_{12} = -Y_{21},$$

$$y_{p1} = Y_{11} + Y_{12},$$

and

$$y_{p2} = Y_{22} + Y_{12}.$$

If y_p, y_{s1}, and y_{s2} are themselves described by simple networks, the network parameter values can be determined from the measured Y-parameters with little or no fitting.

This fact was exploited in [10] for the modeling of microstrip spiral inductors. Here we consider the model of [10] for our spiral inductors and a similar model for our MIM capacitors. Although these models provide a simple and useful starting point, they turn out to have significant limitations.

MIM CAPACITORS

The series capacitors were composed of square parallel plates embedded in transmission lines identical to the calibration structures. The lower plate was composed of first-layer metal extending from the transmission line at port 1; the upper plate, was built from second-layer metal but connected to port 2 using bridge metal only. A 0.2 µm layer of Si_3N_4 separated the two plates. Based on prior processing experience, we estimated a capacitance of 282 pF/µm^2; this corresponds to a Si_3N_4 permittivity of 6.37. On each of four different wafers, we measured capacitors of three sizes. Capacitor 1 was 20 µm square, Capacitor 2 was 50 µm square, and Capacitor 3 was 132 µm square.

The measured Y parameters of Capacitors 2 and 3 showed prominent resonances (see Figs. 8-11). We determined resonance frequencies $f_r(Y_{12})$ for these devices by looking for a sign change in $\mathrm{Im}(Y_{12})$.

We used our measured Y parameters to determine the values in the equivalent circuit model of Fig. 3. In this model, we can solve explicitly, at each frequency, for the parameters R_1, R_2, C_1, C_2, and R_s. In order to determine C_s and L_s, we performed a quadratic, least-squares curve fit. Fig. 4 plots the measured quantity $\omega\,\mathrm{Im}(-1/Y_{12})$ along with the modeled estimate $\omega^2 L_s - 1/C_s$ for two capacitors on Wafer A. The agreement is excellent.

As shown in Table 1, the measured values of C_s agree well with the estimates based on the plate size. The table includes the resonant frequency $f_r = \left(2\pi\sqrt{L_s C_s}\right)^{-1}$, which agrees closely with $f_r(Y_{12})$.

In performing the least-squares fits, we used only frequencies up to $f_r(Y_{12})$. However, since the data for R_1, R_2, and R_s were strongly affected by the presence of calibration errors at multiples of 12 GHz, we limited the averaging interval for these parameters to 10 GHz. The measured R_1 and R_2 were so small as to virtually indistinguishable from 0. Therefore, we ignored them. R_s is included in Table 1.

C_1 and C_2 were problematic. Figure 5, which is typical, plots the extracted C_1 and C_2 of Capacitor 3 of Wafer A. The resonance in f_r clearly demonstrates that the model fails to properly account for the parallel parasitics. Based on the frequencies at which they occur, these resonances are clearly related to L_s C_s and not to the 12 GHz calibration errors. Above the resonance, $C_1 \approx C_2$, but $C_1 \gg C_2$ for low frequencies. The low frequency asymmetry is unsurprising in view of the asymmetry of the capacitor. However, the mean of C_1 and C_2 is, curiously, almost frequency-independent. Clearly, the model is inadequate. An improved model must account for the inductance of the bridge contact to the top plate. Our preliminary investigations have indicated that a series inductance on port 2 does indeed force a resonance, quite like the ones we observed, in C_1 and C_2, but more study is required in order to specify the parameter values.

Here, we estimated both parameters C_1 and C_2 by averaging their mean over the entire measured band. Table 1 gives the results.

This failure of the model does not necessarily limit its application as a representation of S or Y parameters, This is illustrated by Figs. 6-11, which show a good fit for the capacitor illustrated in Fig. 5.

SPIRAL INDUCTORS

Square spiral inductors were formed using 10 µm wide conductors. The outside of the spiral was connected to port 1; the inside was connected to port 2 using the first metal layer only. The turns of the spiral crossed over this connection using bridge metal. Inductors 2 and 3 were formed from the same 6 µm metallization used in the transmission lines, with a spacing of 15 µm between the turns. Inductor 1 was built using only the 1.5 µm first metal layer, with 10 µm between the turns.

We began analyzing the spiral inductors using the equivalent-circuit model of Fig. 12, which is identical to that proposed by [10] for microstrip spiral inductors. All of the terms except C_s can be determined uniquely at each frequency once C_s has been assigned. In [10], C_s is chosen so as to minimize the frequency-dependence of L_s. After estimating it the same way, we determined that C_s is not a critical parameter and has little significant effect. We therefore deleted it from the model. We also eliminated G_1 and G_2 after ascertaining their insignificance. We averaged C_1, C_2, and L_s over a frequency range up to half the resonant frequency $f_r(Y_{12})$, which we defined to be the frequency at which the phase of Y_{12} first crossed 0. However, we never extended our fitting interval past 10 GHz so as to avoid the 12 GHz calibration error. R_s turned out to increase with frequency, presumably due to skin effect, and we found a better fit using the dc extrapolation than the average. The estimated parameters are shown in Table 2.

Representative curves illustrating the frequency-dependent values of several parameters are shown in Figs. 13-15. Calibration errors at multiples of 12 GHz are again obvious. However, resonances akin to those seen in modeling the MIM capacitor are in evidence at the frequency f_r. Comparison of the modeled data to the measured data (Figs. 16-23) show that the model does not account for this resonance

but provides a good representation below the resonance frequency.

Measurement of Inductor 3 showed this resonance to recur quasiperiodically in frequency.

Conclusions

With its potential for low cost and high reliability, the flip-chip CPW MMIC holds promise for large-scale introduction into consumer electronics. Design of such circuits, however, is hampered by the lack of reliable electrical data on circuit elements. Such data are difficult to obtain theoretically. On the other hand, carefully designed and conducted measurements can provide accurate data, with well-defined reference planes, that can readily be integrated into a CAD database for high-quality, first-pass circuit design.

Here, we have presented data on the characterization of on-chip components. Although the measured *S*, *Y*, or *Z* parameters may be used directly in CAD, a parameter-based representation is much more efficient in terms of data storage. Such a representation hinges on the development of appropriate models. If the models are based on the physical structure, the extracted values are also useful in component design. The models used here are a useful starting point but require refinement in order to represent the significant features.

In order to extend this work to the characterization of solder joints using the two-tier TRL calibration process, we have built an additional set of calibration structures on the ceramic mounting substrate. This will also allow the study of substrate loading effects.

Accurate TRL calibration over a broad band requires the use of multiple transmission lines as calibration standards. Our future work will incorporate additional standards.

Acknowledgements

This work was supported by the Advanced Technology Program of the National Institute of Standards and Technology. Dylan Williams offered several helpful suggestions regarding the manuscript.

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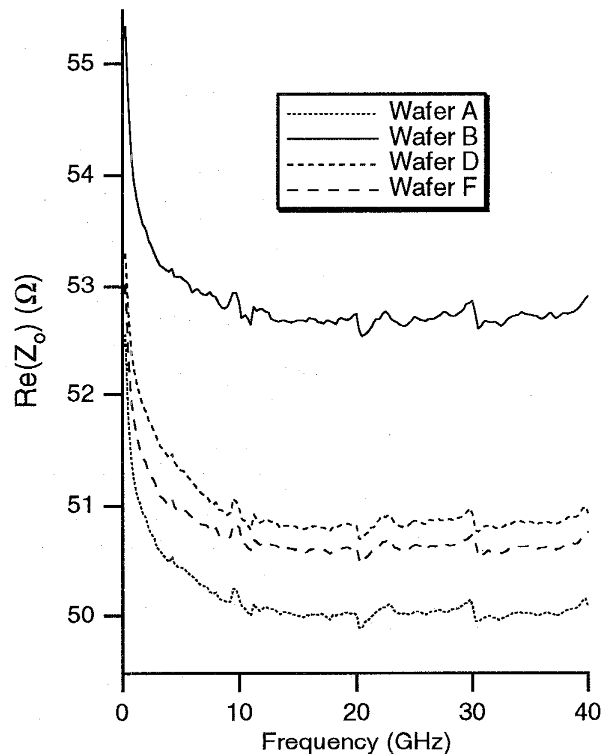

Figure 1: Real part of Z_0 for CPW lines on four wafers

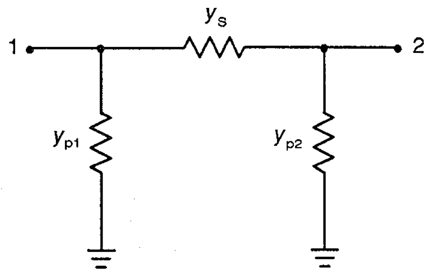

Figure 2: π circuit model

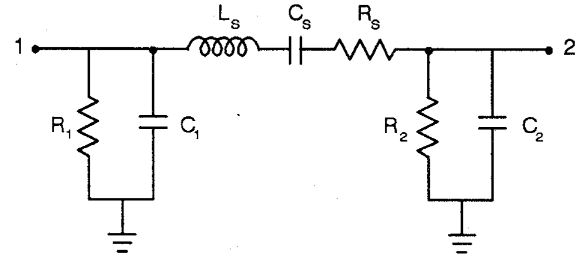

Figure 3: Capacitor circuit model

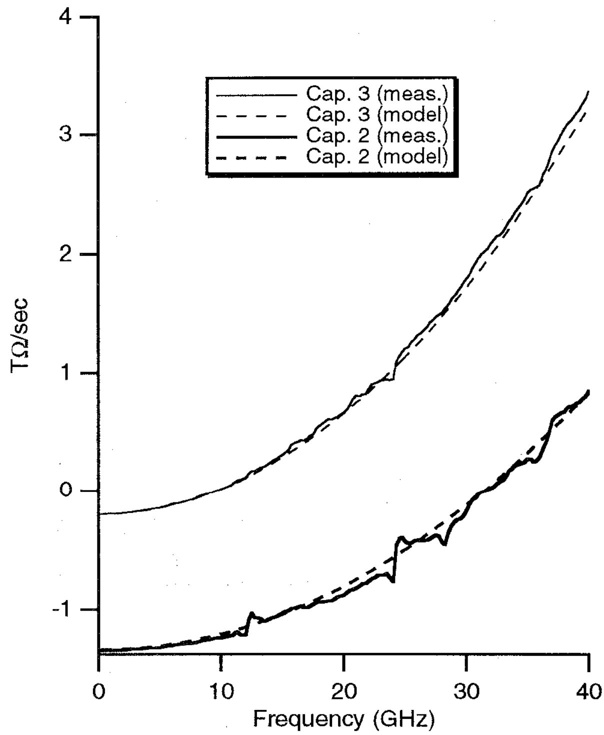

Figure 4: $\omega \mathrm{Im}(-1/Y_{12})$ for Capacitors 2 & 3

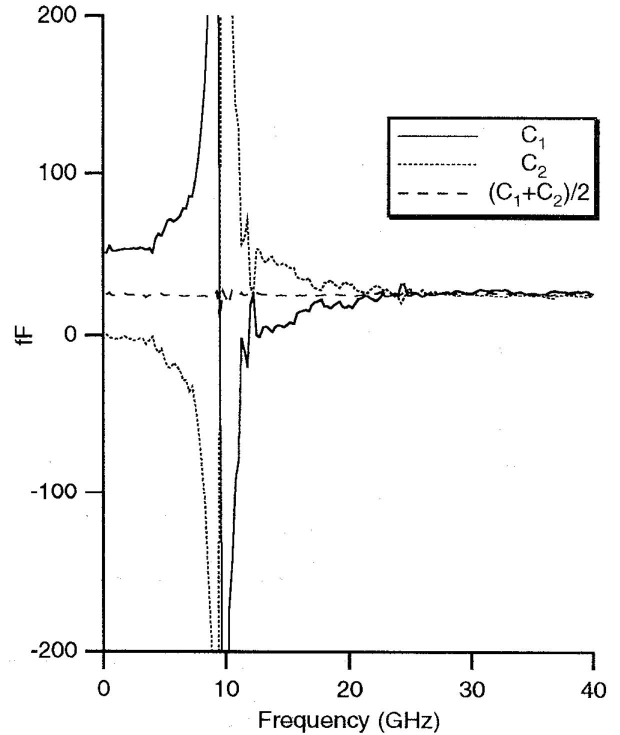

Figure 5: C_1, C_2, and their mean for Capacitor 3

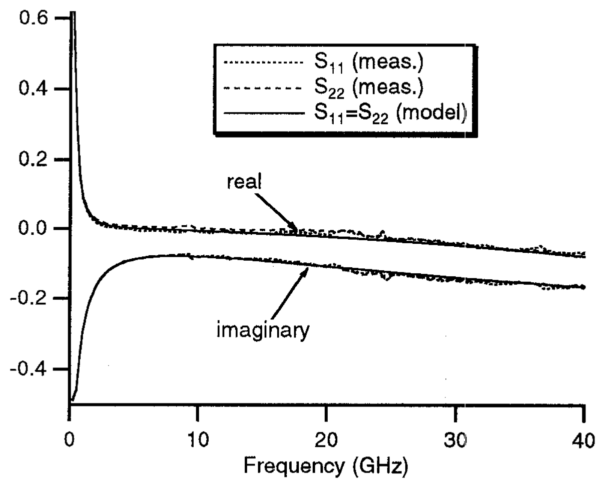

Fig. 6: S_{11} and S_{22}, Capacitor 3, Wafer A

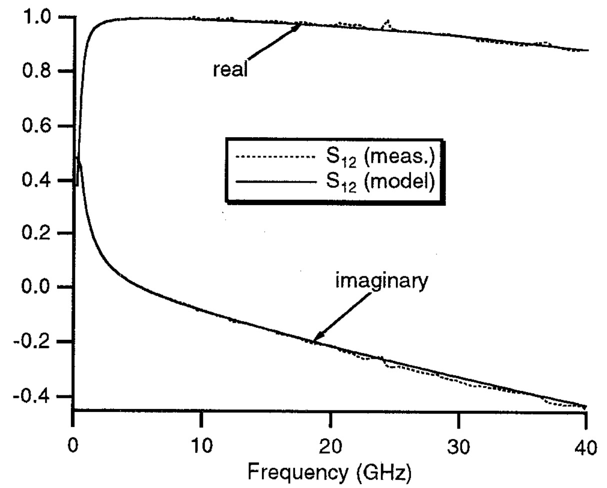

Fig. 7: S_{12}, Capacitor 3, Wafer A

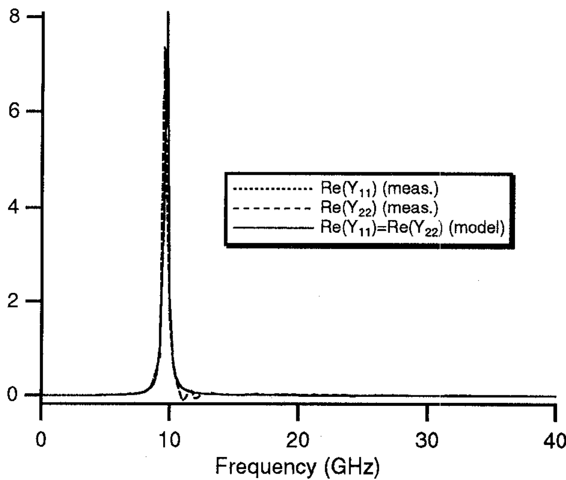

Fig. 8: $\mathrm{Re}(Y_{11})$ and $\mathrm{Re}(Y_{22})$, Capacitor 3, Wafer A

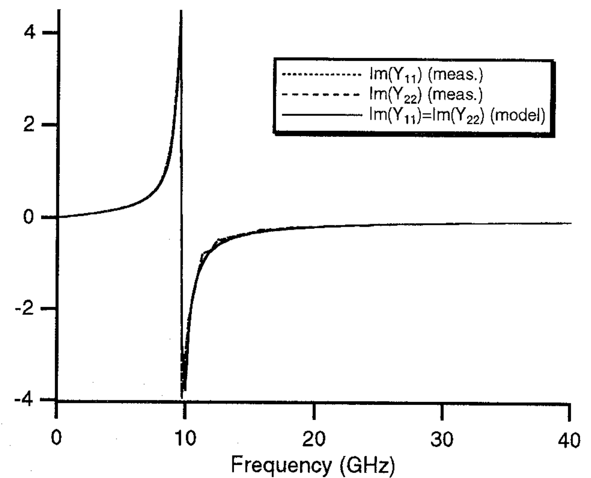

Fig. 9: $\mathrm{Im}(Y_{11})$ and $\mathrm{Im}(Y_{22})$, Capacitor 3, Wafer A

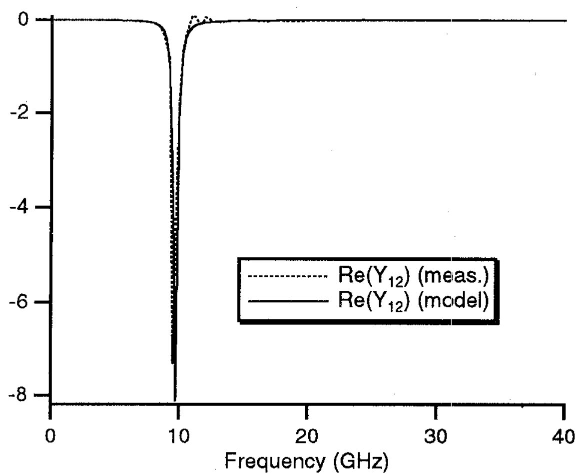

Fig. 10: $\mathrm{Re}(Y_{12})$, Capacitor 3, Wafer A

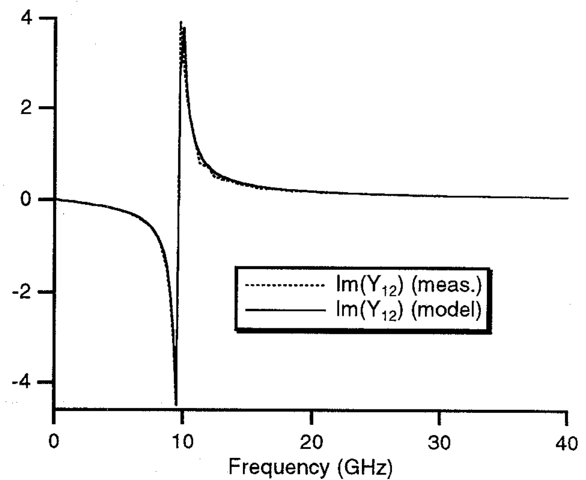

Fig. 11: $\mathrm{Im}(Y_{12})$, Capacitor 3, Wafer A

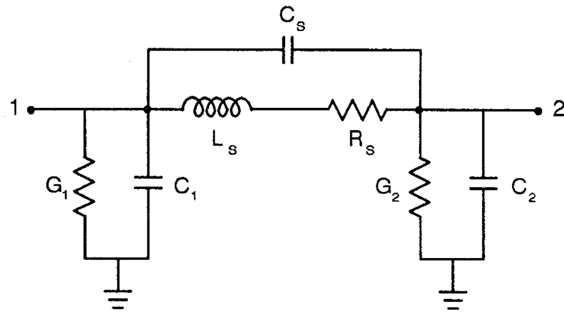

Fig. 12: Inductor Circuit Model

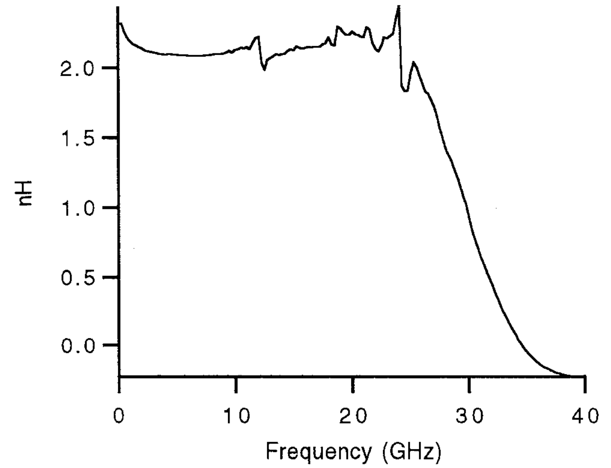

Fig. 13: L_s of Inductor 2, Wafer A

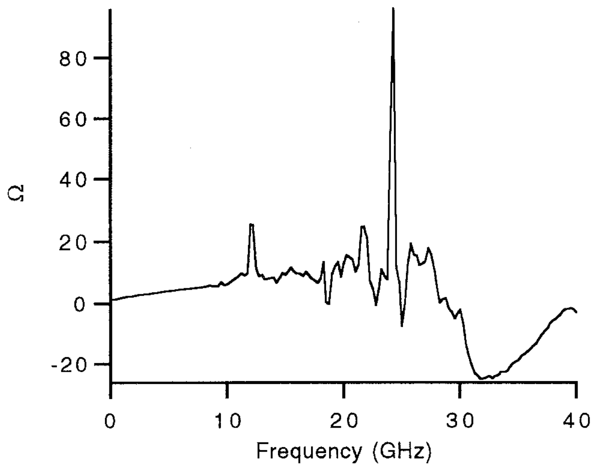

Fig. 14: R_s of Inductor 2, Wafer A

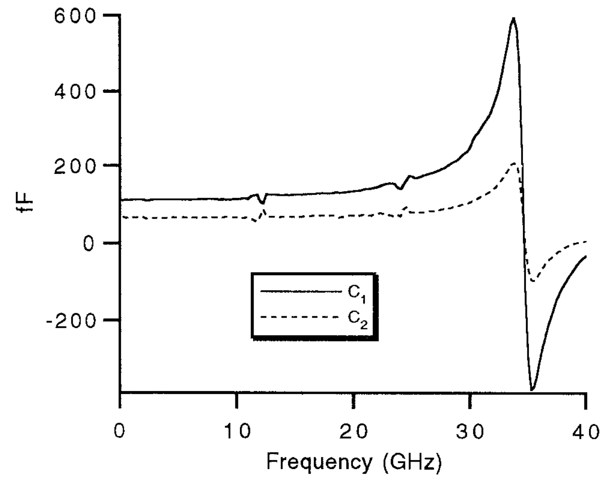

Fig. 15: C_1 and C_2 of Inductor 2, Wafer A

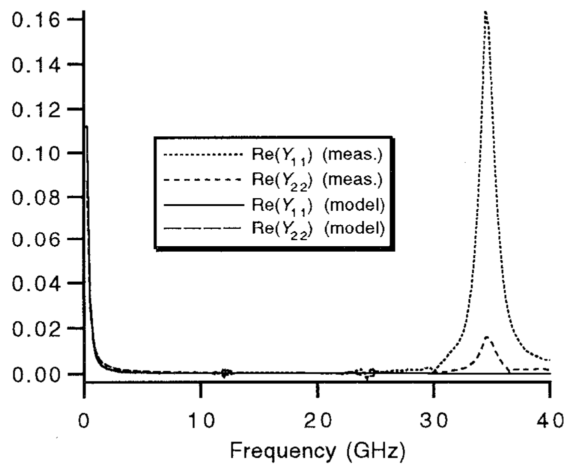

Fig. 16: $\mathrm{Re}(Y_{11})$ and $\mathrm{Re}(Y_{22})$ for Inductor 2, Wafer A

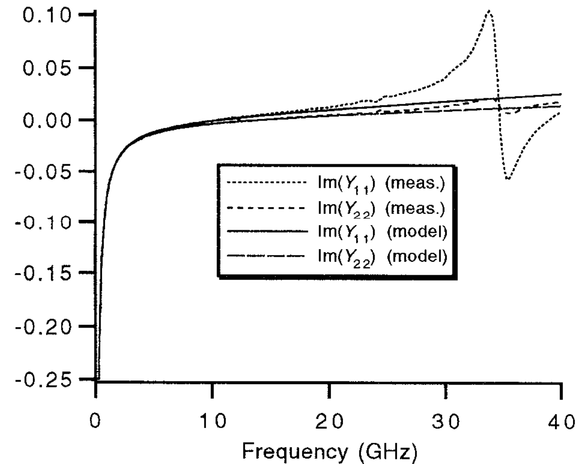

Fig. 17: $\mathrm{Im}(Y_{11})$ and $\mathrm{Im}(Y_{22})$ for Inductor 2, Wafer A

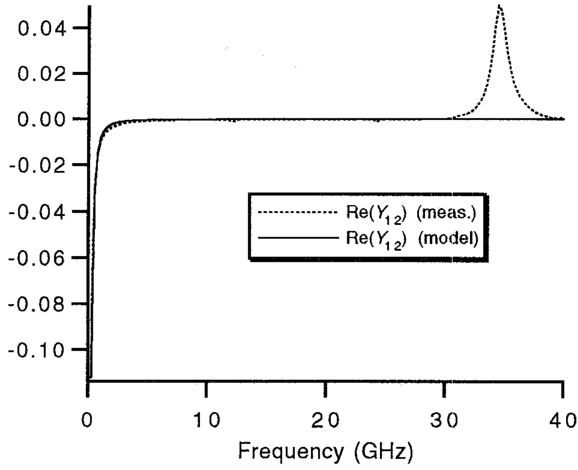

Fig. 18: Re(Y_{12}) for Inductor 2, Wafer A

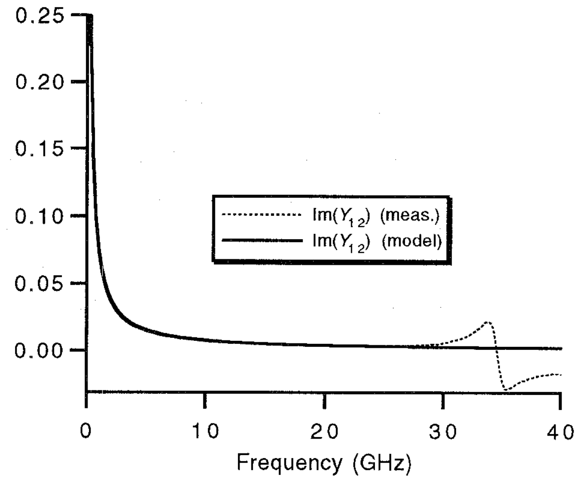

Fig. 19: Im(Y_{12}) for Inductor 2, Wafer A

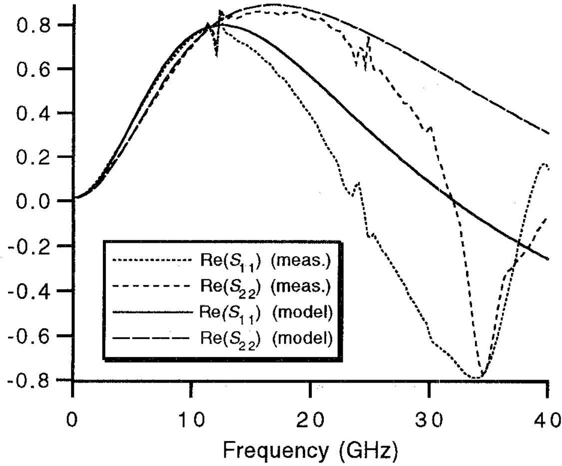

Fig. 20: Re(S_{11}) and Re(S_{22}) for Inductor 2, Wafer A

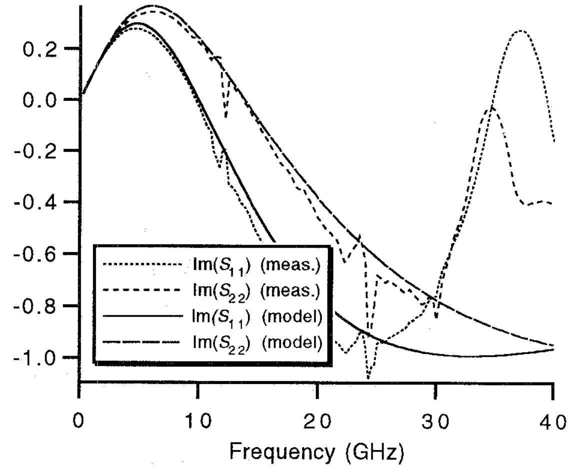

Fig. 21: Im(S_{11}) and Im(S_{22}) for Inductor 2, Wafer A

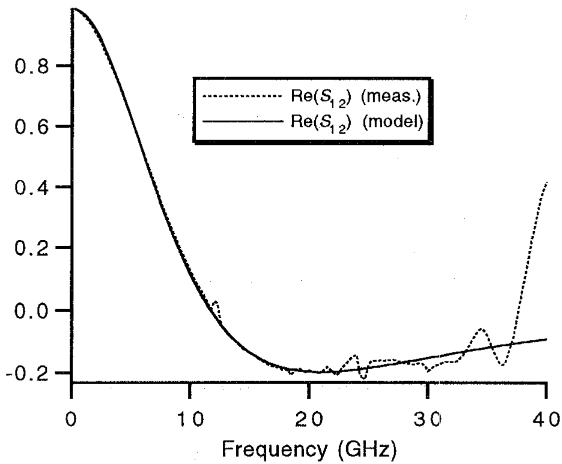

Fig. 22: Re(S_{12}) for Inductor 2, Wafer A

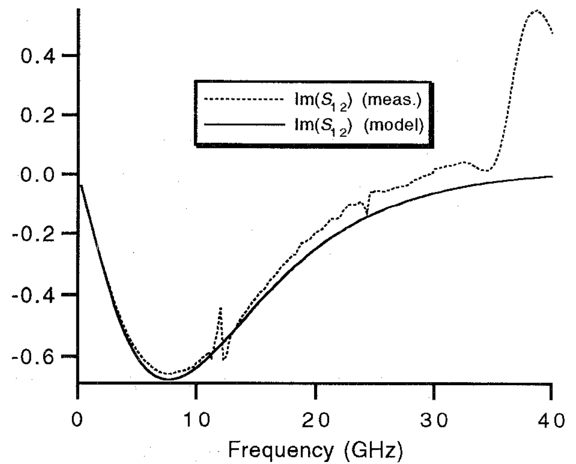

Fig. 23: Im(S_{12}) for Inductor 2, Wafer A

Capacitor Number	Wafer Label	Nitride Layer (μm)	1st Oxide (μm)	2nd Oxide (μm)	f_r (GHz)	$f_r(Y_{12})$ (GHz)	C_1,C_2 (fF)	R_S (Ω)	L_S (pH)	C_S (pF)	C_{est} (pF)
1	A	0.1	2	2	81.7	>40	3.72	2.1	28.5	0.133	0.133
(20×20 μm)	B	0	0	0	85.6	>40	3.60	2.2	28.2	0.123	0.133
	D	0	2	1	84.0	>40	4.50	2.2	26.3	0.137	0.133
	F	0	2	0.5	79.1	>40	4.44	1.7	30.6	0.132	0.133
2	A	0.1	2	2	31.5	31.6	7.71	0.18	34.4	0.743	0.705
(50×50 μm)	B	0	0	0	31.9	30.3	7.61	0.27	34.5	0.721	0.705
	D	0	2	1	31.2	30.1	8.53	0.32	35.0	0.745	0.705
	F	0	2	0.5	31.1	30.2	8.00	0.20	35.7	0.732	0.705
3	A	0.1	2	2	9.69	9.63	26.1	0.11	54.2	4.98	4.91
(132×132 μm)	B	0	0	0	9.31	9.33	25.3	2.4	58.8	4.97	4.91
	D	0	2	1	9.58	9.37	28.6	0.17	55.5	4.97	4.91
	F	0	2	0.5	9.60	9.39	26.3	0.10	56.1	4.90	4.91

Table 1. Equivalent circuit values of capacitors.

Inductor Number	Wafer Label	Nitride Layer (μm)	1st Oxide (μm)	2nd Oxide (μm)	$f_r(Y_{12})$ (GHz)	C_1 (pF)	C_2 (pF)	R_S (Ω)	L_S (nH)
1	A	0.1	2	2	>40	0.057	0.046	1.50	0.565
(2.5 turns)	D	0	2	1	>40	0.058	0.049	1.44	0.573
	F	0	2	0.5	>40	0.056	0.047	1.46	0.570
2	A	0.1	2	2	34.5	0.111	0.066	1.50	2.12
(4.5 turns)	D	0	2	1	34.3	0.110	0.069	1.56	2.18
	F	0	2	0.5	35.4	0.106	0.066	1.53	2.11
3	A	0.1	2	2	6.97	0.295	0.114	4.09	23.1
(10.5 turns)	D	0	2	1	6.90	0.289	0.117	3.66	23.7
	F	0	2	0.5	7.13	0.277	0.120	6.67	11.5

Table 2. Equivalent circuit values of inductors.