Monolithic Preamplifiers for Low-Capacitance Detectors

when an FET is not an FET
when a resistor is not a resistor

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OUTLINE:

- Capacitive matching of detector and input transistor
- Design of DC feedback circuit
- Results on CMOS preamplifiers
- Results on Bipolar preamplifiers

Capacitive match

1. Constant current density (discrete FETs)

$$\frac{g_m}{C_{gs}} = \omega_T, \text{ constant}$$

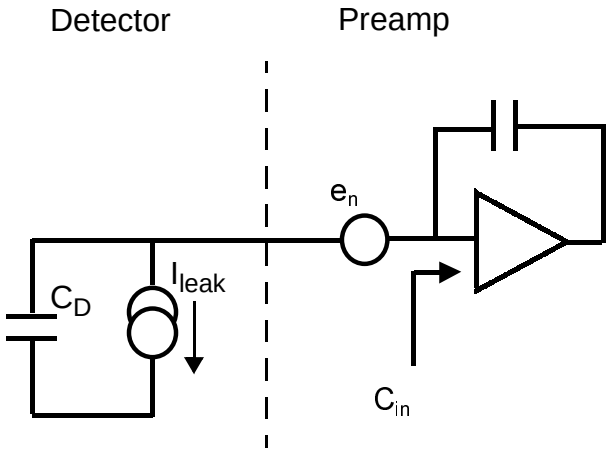
$$ENC = K \cdot \frac{C_D + C_{gs}}{\sqrt{g_m}} = K' \cdot \frac{C_D + C_{gs}}{\sqrt{C_{gs}}}$$

$$\left(\frac{d}{dC_{gs}} ENC = 0\right) \Rightarrow C_{gs} = C_D$$

2. Constant drain current (monolithics)

Strong inversion (S.I.)	Weak inversion (W.I.)
$g_m = \sqrt{\frac{2\mu I_D C_{gs}}{L^2}}$ $ENC = \frac{K(C_{gs} + C_D)}{g_m} = K'\left(C_D C_{gs}^{-\frac{1}{4}} + C_{gs}^{\frac{3}{4}}\right)$ $\frac{d}{dC_{gs}} ENC = 0 \Rightarrow C_{gs} = \frac{C_D}{3}$	$g_m = \frac{I_D}{nU_T}$, indep. of C_{gs}. $ENC = K(C_D + C_{gs})$ $C_{gs} \to 0$ -- but this brings device into S.I. optimum when $C_{gs} = \frac{2I_D L^2 C_{ox}}{K'(3U_T)^2}$ S.I. - W.I border

Series Noise Matching



$$ENC = \frac{K_1 e_n (C_D + C_{in})}{t_s}$$

$$e_n = \begin{pmatrix} \frac{4kT\Gamma}{g_m} & \text{thermal} \\ \frac{4kTK_F}{C_{gs}} & 1/f \end{pmatrix}$$

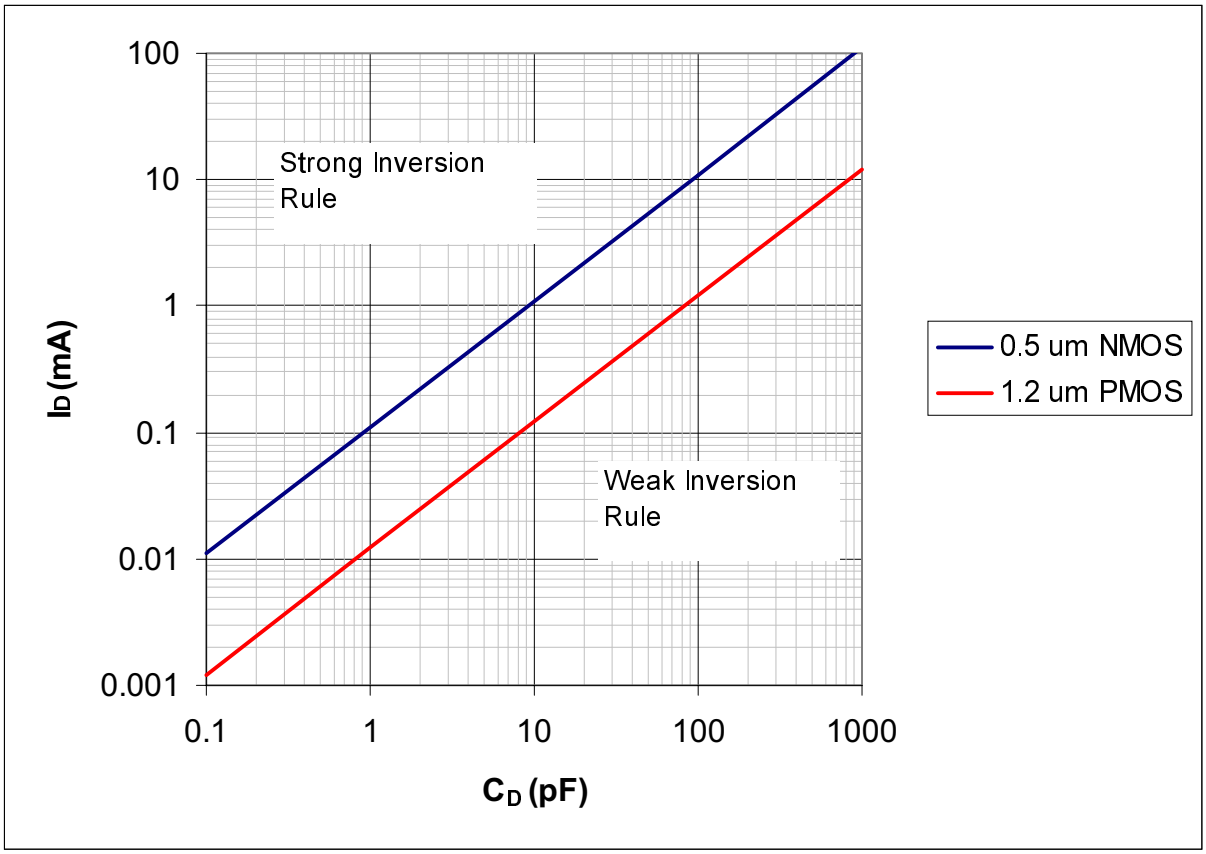
Ideal:

Cin = 0

$e_n = 0$ or $g_m = \infty$

$\rightarrow$ highest f_T

Minimum current for S.I. capacitive match

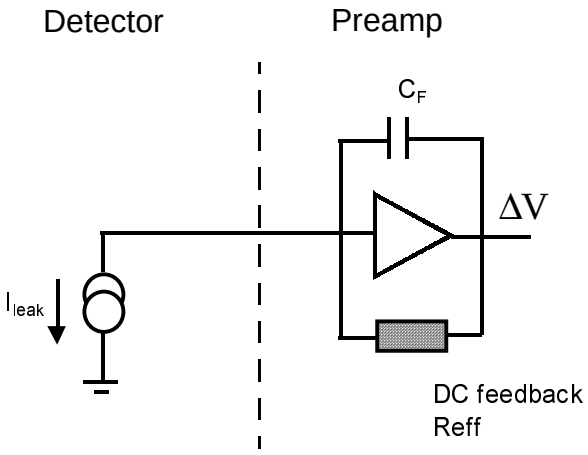


Capacitive match -- Example

0.5 µm NMOS input device
C_D = 10 pF, I_D = 0.2 mA
Conventional $C_D/3$ match gives W = 1543 µm.
g_m = 5 mS
$C_{gs} + C_D$ = 13.3 pF

Sizing device to W.I. - S.I. border gives W = 281µm.
g_m = 5 mS
$C_{gs} + C_D$ = 10.6 pF

Parallel Noise Management



$ENC_{par} \sim 1/R_{eff}$

$\Delta V = I_{leak} \cdot R_{eff}$

Ideal:

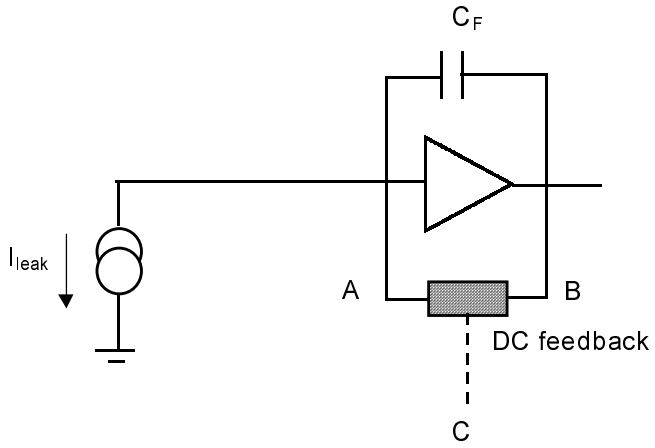
$R_{eff} = 2kT/qI_{leak}$

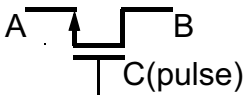
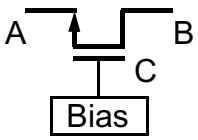
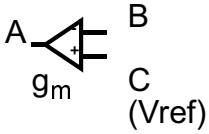
$\rightarrow$ lowest ΔV with no noise penalty

$\tau_{decay} = R_{eff} \cdot C_F$

$\rightarrow$ can effect gain if $\tau_{decay} \sim \tau_{shaper}$

DC Feedback

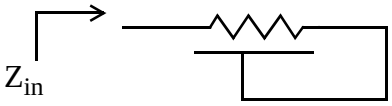


Feedback type	Circuit	R_{eff} (I_{leak} =0)	Advantages/ Disadvantages
Physical resistor		R	+ simple - hard to make large R - parasitic C - doesn't adjust to I_{leak}
MOS switch		$\frac{1}{C_F \cdot f_{reset}}$	+ simple - dead time - switch noise
Triode MOS		$\frac{1}{\beta \cdot (V_{gs} - V_T)}$	+ compact + adjusts to I_{leak} - nonlinear
Feedback g_m		$\frac{1}{g_m}$	+ adjusts to I_{leak} - complex - excess noise - nonlinear
Attenuating current mirror		$\frac{R}{A_i}$	+ aux. output for PZC - doesn't adjust to I_{leak}

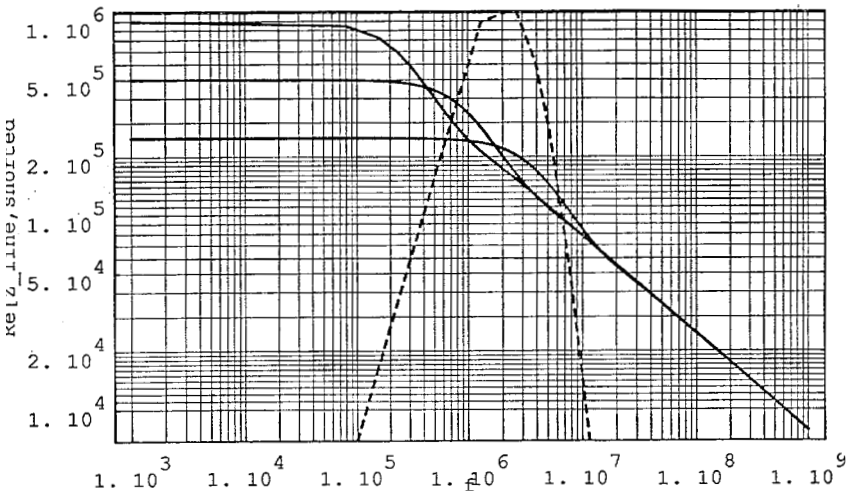
Resistor parasitic capacitance

For implanted resistor in MAXIM process, parasitic resistance is 1.3 fF/kΩ.

$$i_n^2 = \frac{4kT}{Re\{Z_{in}\}}$$

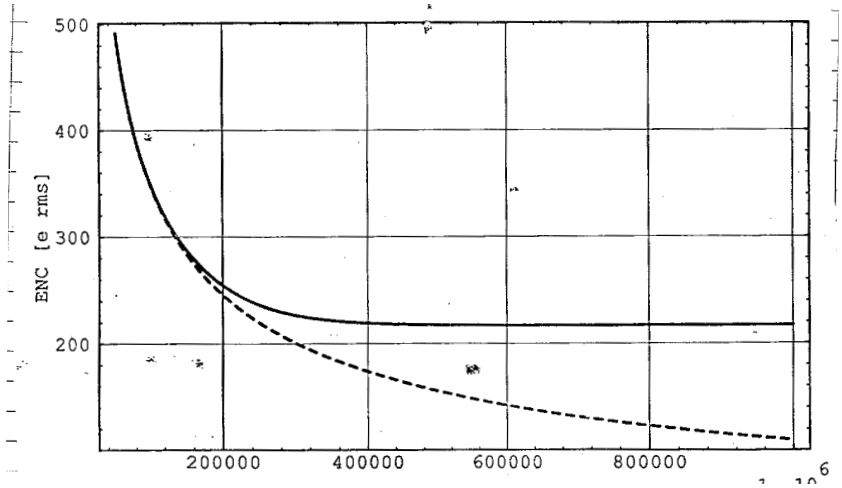


Real part of impedance of a shorted diffusive line



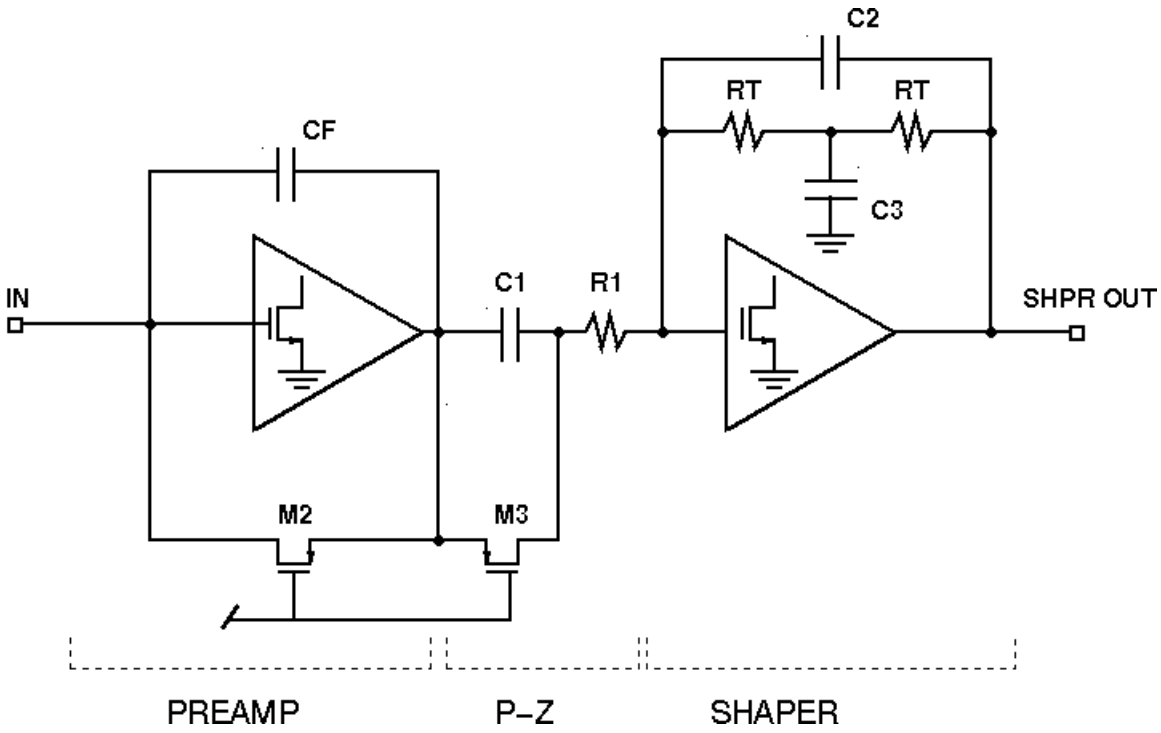
R=50 kΩ/section
C=0.65 pF/section
250 kΩ, 500kΩ, 1MΩ

ENC contribution of the diffusive feedback line



R=250K, Ctot=0.32pF
H(s)=1/(1+s tau)^4 tau=12 ns tpeak=30 ns

Adaptive Pole-Zero Cancellation



CF R(M2) = C1 R(M3)

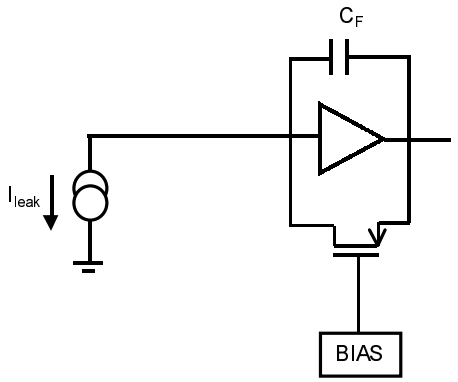
$V_G(M2) = V_G(M3)$
$V_S(M2) = V_S(M3)$
$V_D(M2) = V_D(M3)$

MOS Resistor

Behavior with Ileak = 0:

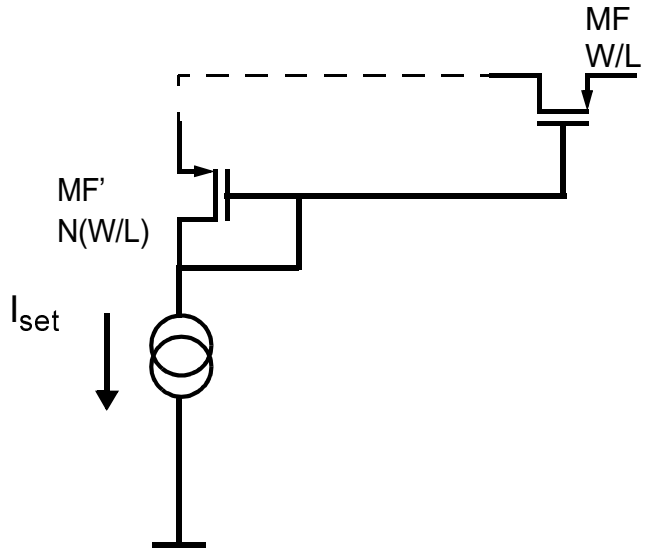
Strong inversion (S.I.)	Weak inversion (W.I.)
$I_d = \frac{\beta}{2} \cdot (V_{GS} - V_T)^2 \cdot V_{DS}$	$I_d = I_{do} e^{\frac{qV_{GS}}{nU_T}} \left(1 - e^{-\frac{V_{DS}}{U_T}} \right)$
$R = \frac{1}{\beta \cdot (V_{GS} - V_T)}$	$R = \frac{U_T \cdot e^{-\frac{qV_{GS}}{nU_T}}}{I_{do}}$

With Ileak and feedback:



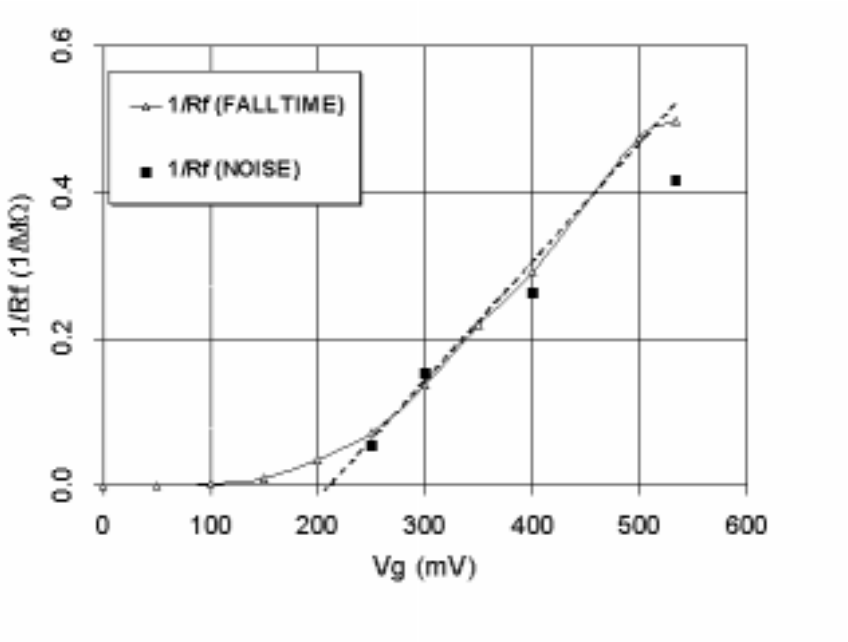
Strong inversion (S.I.)	Weak inversion (W.I.)
$R = \frac{R_0}{1 + \beta R_0^2 I_{leak}}$	$R = \frac{U_T}{I_{leak} + I_{do} e^{\frac{qV_{GS}}{nU_T}} \cdot e^{-\frac{V_D}{U_T}}}$ $\rightarrow$ current controlled!

Bias circuit for MOS feedback resistor

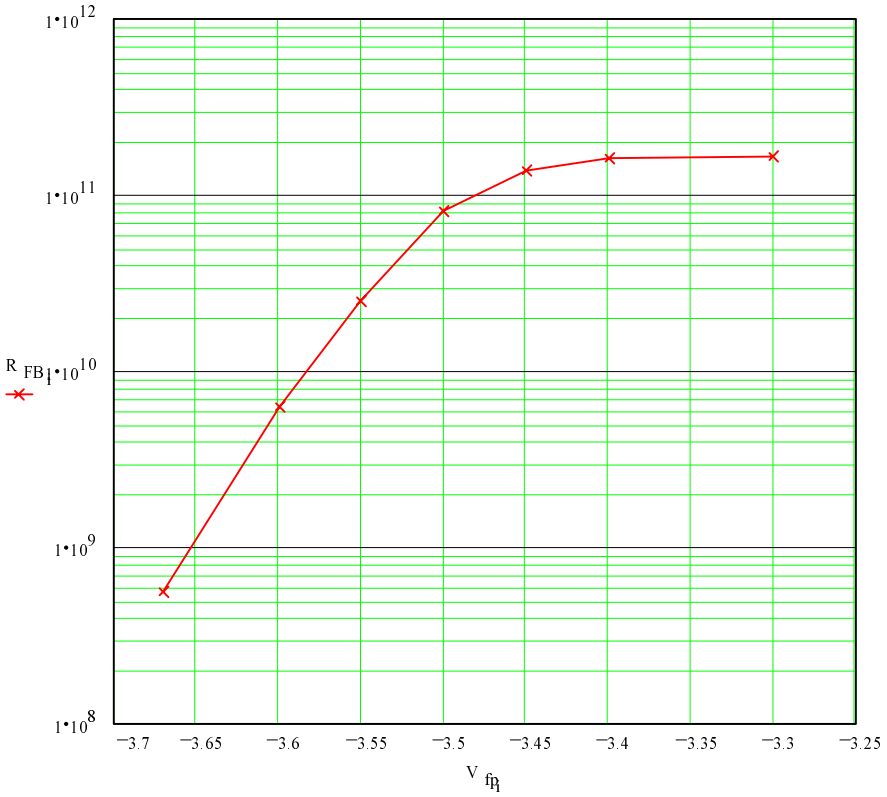


MF	MF'	R_{MF}
S.I.	S.I.	$\sqrt{\frac{N}{2K'(W/L)I_{set}}}$
W.I.	W.I.	$\frac{NU_T}{I_{set}}$
S.I.	W.I.	$\frac{1}{K'\frac{W}{L}\left(nU_T \cdot \ln\left[\frac{I_{set}}{I_0(W/L)N}\right]\right)}$

MOS Resistor in Stong Inversion:



MOS Resistor in Weak Inversion



Low-capacitance preamplifiers compared

	Bipolar MAXIM SH-Pi	CMOS "Tracker" HP 1.2μm	CMOS "X-ray" HP 1.2μm	 AMS 1.2μm
Input device	npn	NMOS 250/1.2	PMOS 100/1.2	PMOS 82/1.2
Current	9μA	400 μA	1.2 mA	1.2 mA
gm	0.17 mS	3.5 mS	2.1 mS	1.9 mS
Cin		400 fF	190 fF	130 fF
Intended C_D	0.8 pF	0.8 pF	0.1 pF	0.1 pF
Feedback	Implanted Resistor	PMOS 3/20 μm	PMOS 3/3 μm	PMOS 3/3 μm
RF	250 KΩ	6 MΩ	280 MΩ	1 GΩ
Parasitic C	0.32 pF	0.10 pF	0.016 fF	0.016 fF
CF	100 fF	100 fF	15 fF	15 fF
Shaper	50 ns internal	50 ns internal	1 - 20 μs external	1 - 20 μs external