CMOS Preamp/Shaper for STAR SVT

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Goal:

A CMOS preamp/shaper for particle tracking using Silicon Drift Detectors

C_{det}	0.8 pF
t_s	50 nsec unipolar
ENC	< 250 e^- rms
P_{diss}	< 5 mW
I_{leak}	to 100 nA

INITIAL DESIGN STUDY AUG. - SEPT. 1994

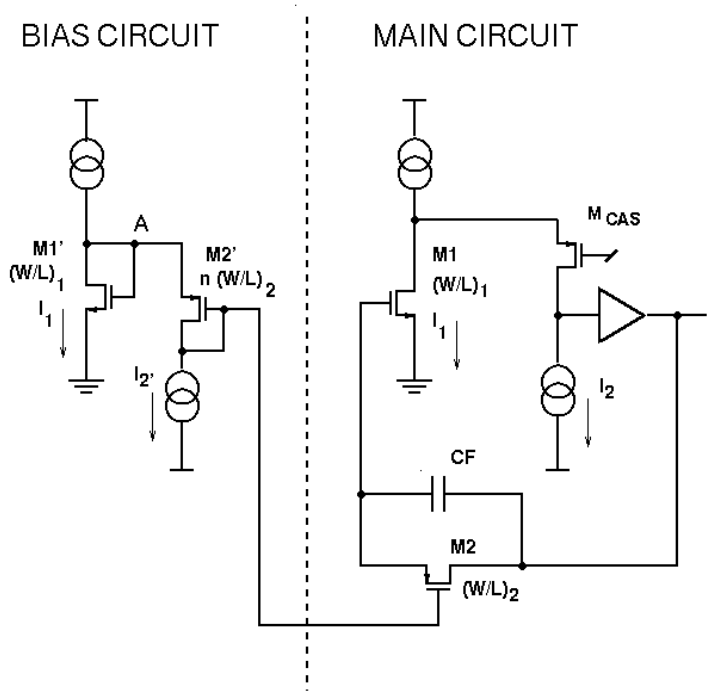
STRATEGIES

- **Series noise: capacitive match**
- **Parallel noise:**

No high-value resistor available in CMOS process

=> Use MOS feedback resistor (PMOS transistor in triode region)

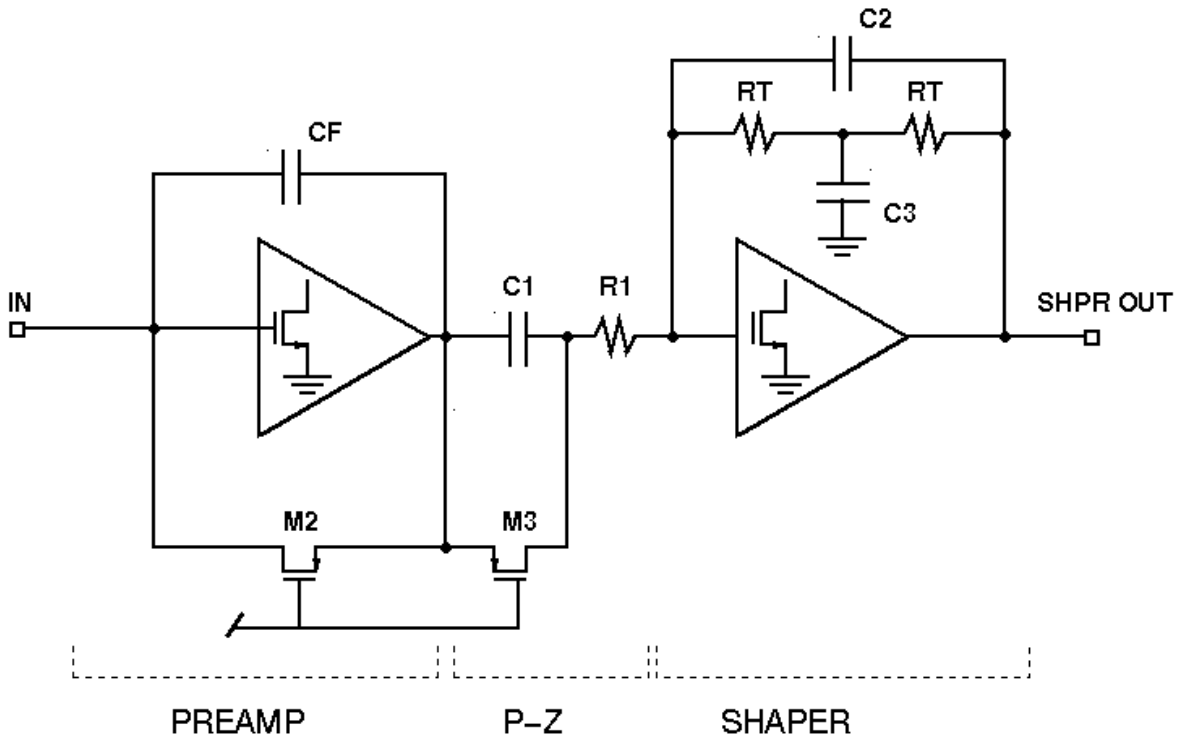
> Self-bias circuit for feedback MOSFET gate:



- high stability, low capacitance in feedback MOSFET without critical adjustments

- RF ~ 5 MΩ

> Adaptive pole-zero cancellation



- increases linearity

- adjusts to high-leakage, high-signal conditions

> Power dissipation

- use minimum current needed for speed and noise

- Class AB output stage

FABRICATION HISTORY

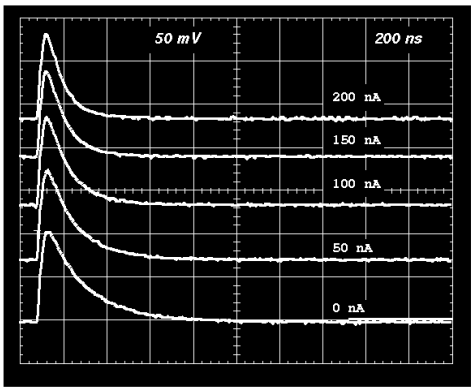
First prototype May 1995

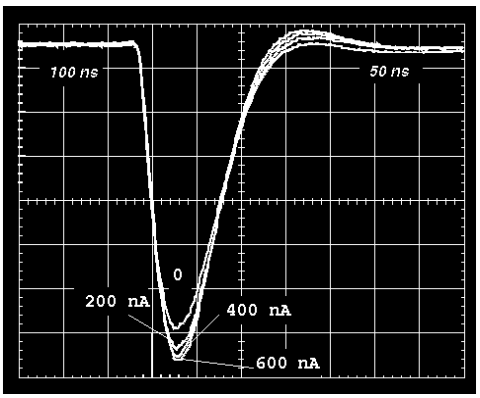
- **Orbit 2.0 micron process**
- **6 circuit variations**
- **Verify self-bias and pole-zero schemes**
- **Study interface to detector**
- **Results:**

  - Feedback resistor scheme works well

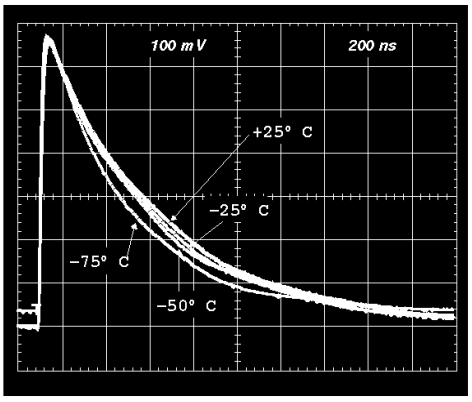
  - Low noise

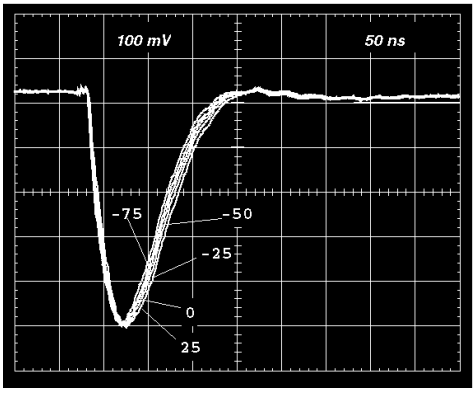
  - Handles 1.5uA leakage current





VS. I_{LEAK}





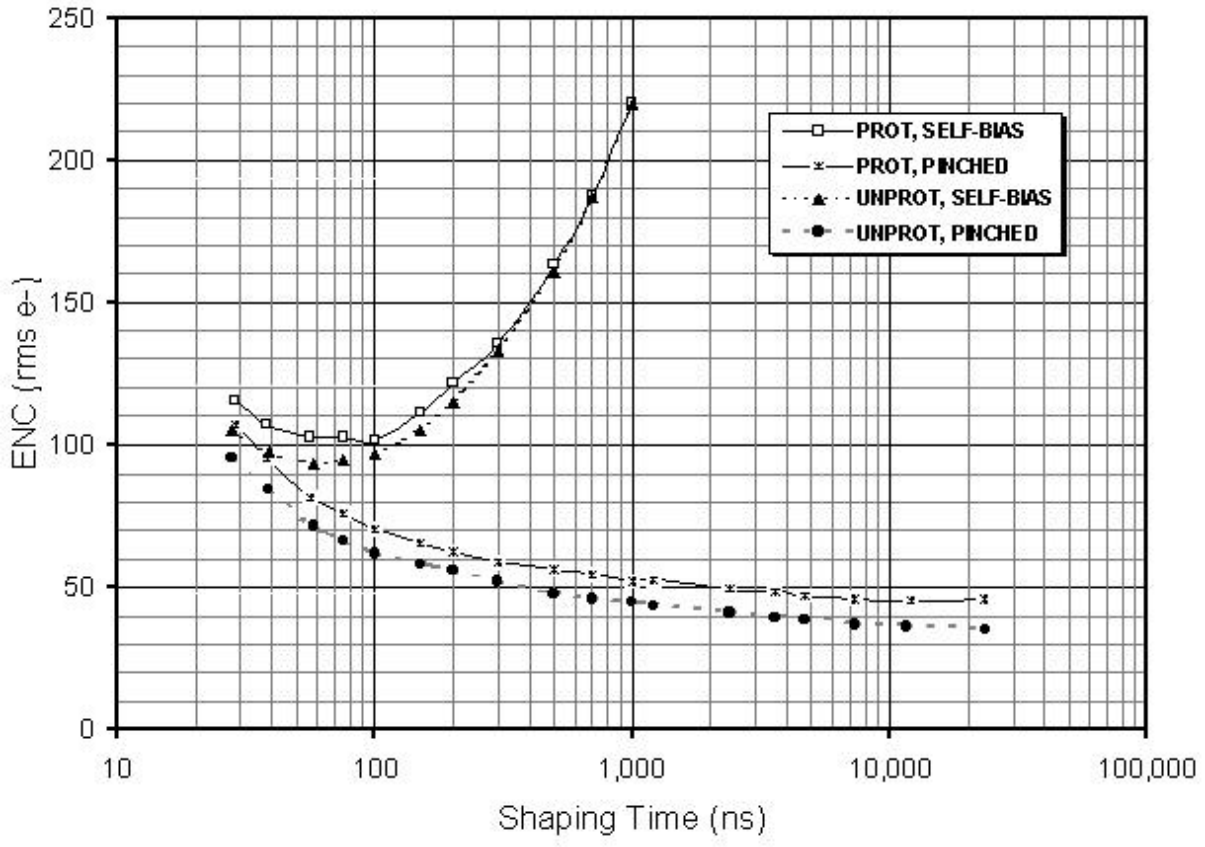
VS. TEMP.

PREAMP WAVEFORMS

PREAMP/SHAPER WAVEFORMS

Second prototype Aug. 1995

- **Convert 6-channel design to HP 1.2 micron technology**
- **Same behavior as first run except lower noise**



Third prototype Sept. 1995

- **16 channel design**
- **added driver stage**
- **serially-controlled calibration and channel disable**
- **shared bias over 16 channels**
- **ESD protection experiment**
- **channel pitch 167 microns**
- **3 power supplies (+3.7, +2.5, -2.5)**
- **RESULTS**

  Noise, gain, waveform as before

  Power dissipation 11.5 mW/chan

  Crosstalk 0.8% (nearest neighbor); 0.3% (others)

  Gain variation 0.6% channel-to-channel

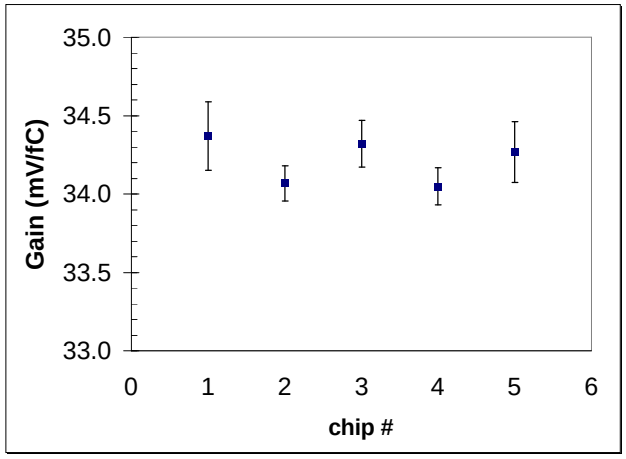
  Studied power reduction strategies

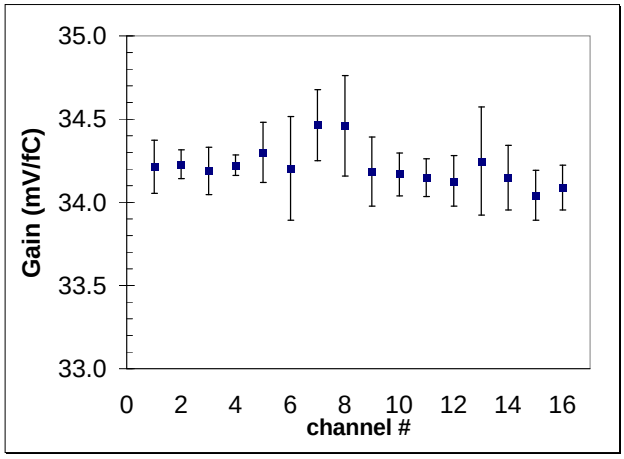
- **developed carrier board, test box for IC testing**

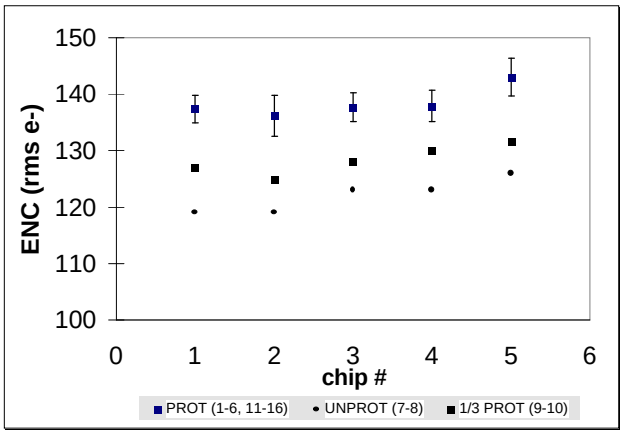
Fourth (Mar. 1996) and fifth (May 1996) prototypes

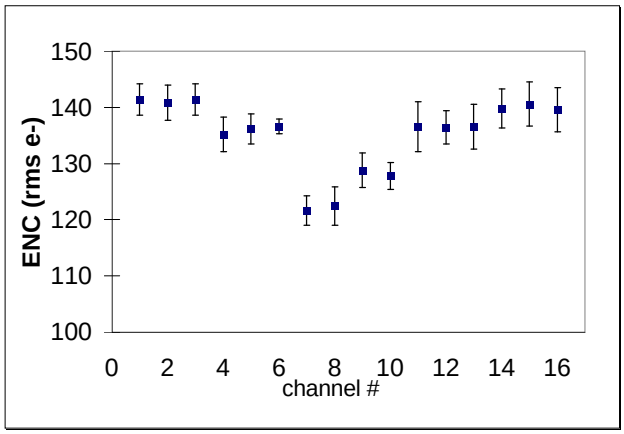
- 16 channel version matched to bipolar PASA footprint
- Power decreased to 6.5 mW/channel
- 2 supplies +3.7V, -2.5V
- Deleted serially-controlled calibration and channel disable
- added gain control, DC sense mode, high drive capability
- layout error in original submission

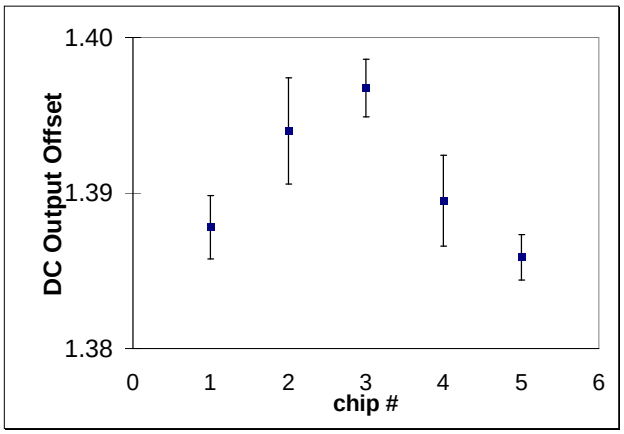
IC37 Results: Gain, Noise, and Offset Uniformity

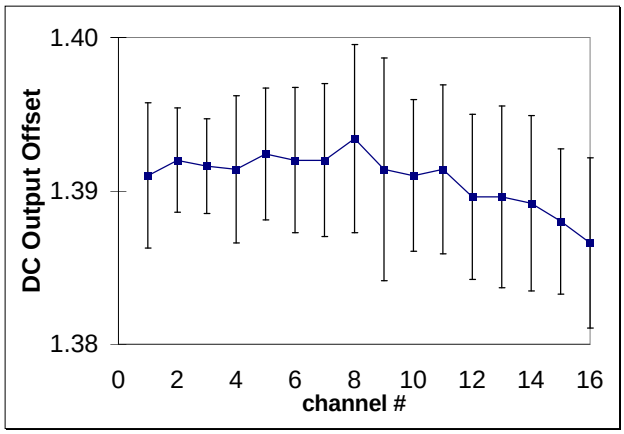












CMOS PASA Compared to Bipolar PASA

1. Higher RF, no IB
    - lower parallel noise, ENC0
2. Higher gm in input transistor
    - lower “noise slope” dENC/dCdet
    - higher Pdiss
3. Larger linear dynamic range
4. No external components needed
5. All channels testable using internal calibration capacitors
6. Lower development cost and faster turnaround

Status and Plans

Chips available

- **4 tested carrier boards w/pins**
  - *for test on PASA/SCA board*
- **2 tested carrier boards w/o pins**
  - *for SDD/PASA tests*
- **11 untested bare die**
  - *for hybrid tests*

No further design for STAR

No further chip production