Advanced Readout ASICs for Multi-Element CdZnTe Sensors

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Outline

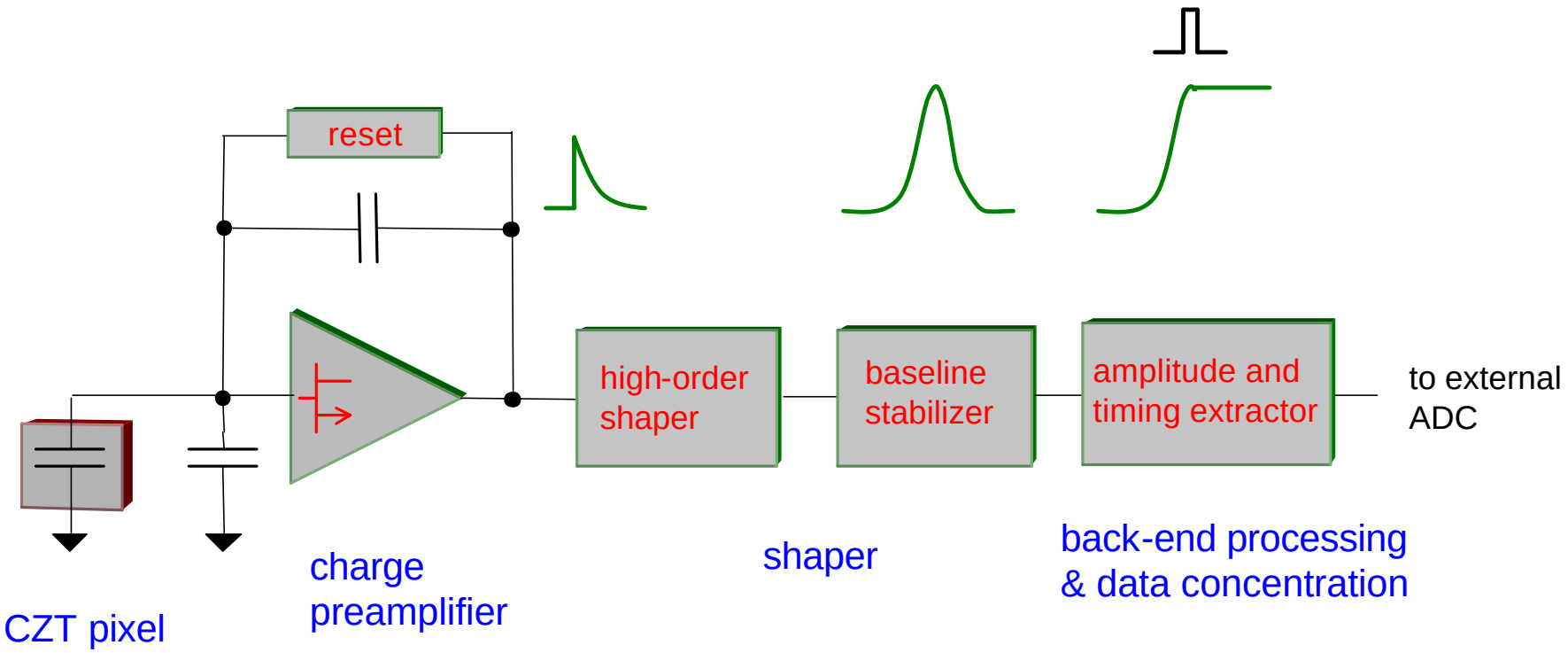
- Front-end ASICs
  - input MOSFET optimization
  - self-adaptive continuous reset of the preamplifier
  - high order shaping
  - output baseline stabilizer (BLH)
  - summary of the first generation
- Data-concentration ASICs
  - two-phase peak detector
  - derandomization process
  - the 32-channel prototype

    - high reliability
    - high stability
    - ease of use (plug & play)
    - spectroscopic quality
    - data concentration optimization

The BNL-eV cooperation

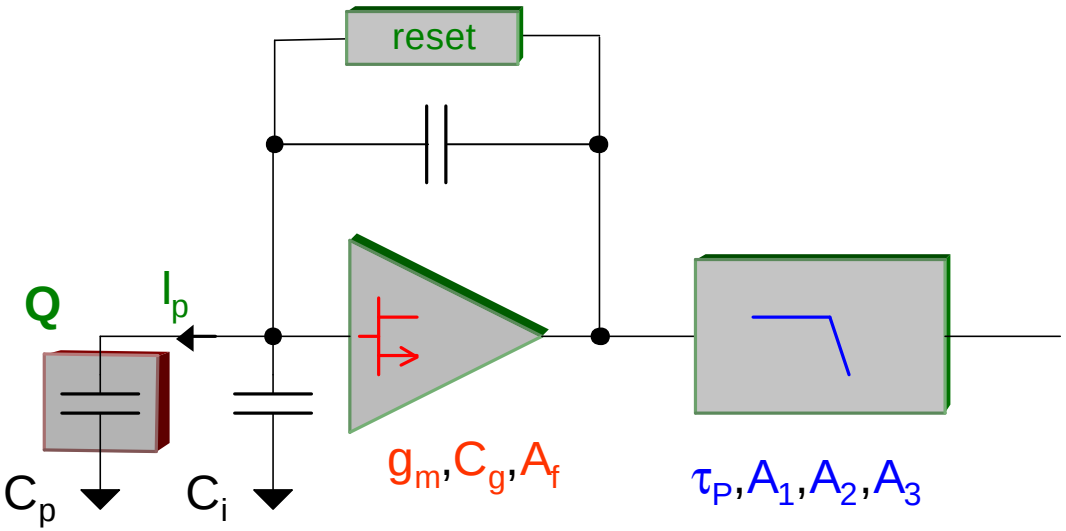
- Started in September **1997**
- First 4 channel front-end ASIC prototype available in April **1999**
- As of Jun **2002** :
    - four front-end ASICs completed (three in production)
        - number of channels (4 - 16)
        - gain (30 - 240 mV/fC, settable)
        - speed (unipolar/bipolar shaping, 0.2 - 4 μs peaking time, settable)
        - input MOSFET (matching 3 or 12 pF input capacitance)
    - one 32-channels arbitration - multiplexing mixed-signal ASIC completed
    - one 32-channels arbitration - peak detection - derandomizing - multiplexing mixed-signal ASIC prototype under development (in fabrication)

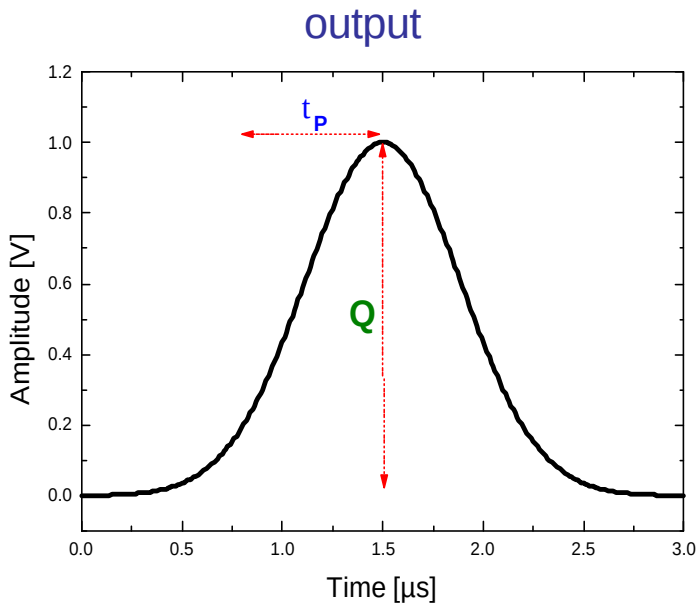
Preamplification and processing of signals from CZT



- high reliability
- ease of use
- spectroscopic quality
- data concentration optimization

Input MOSFET optimization

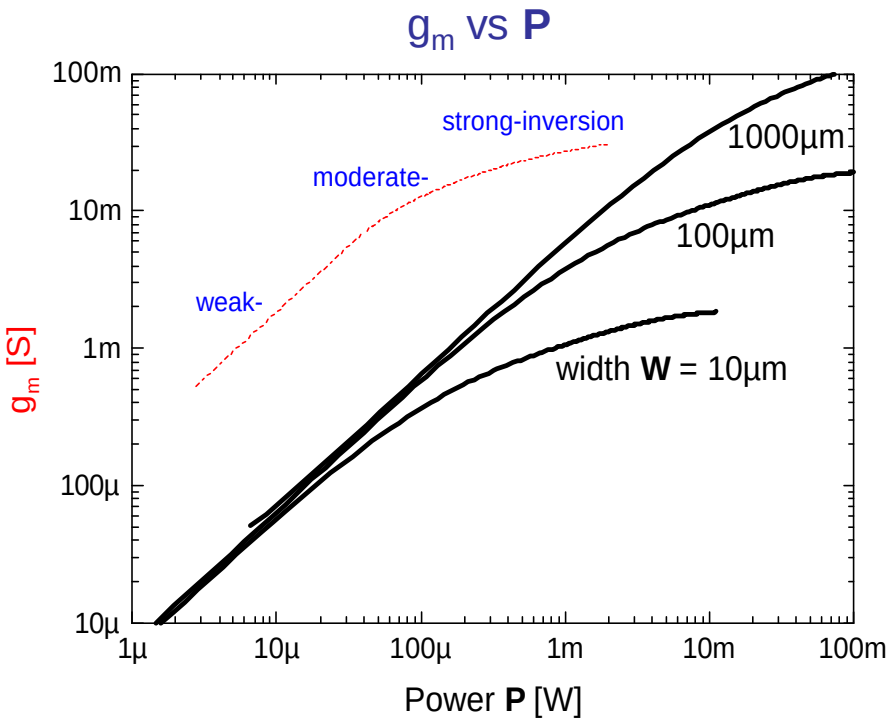


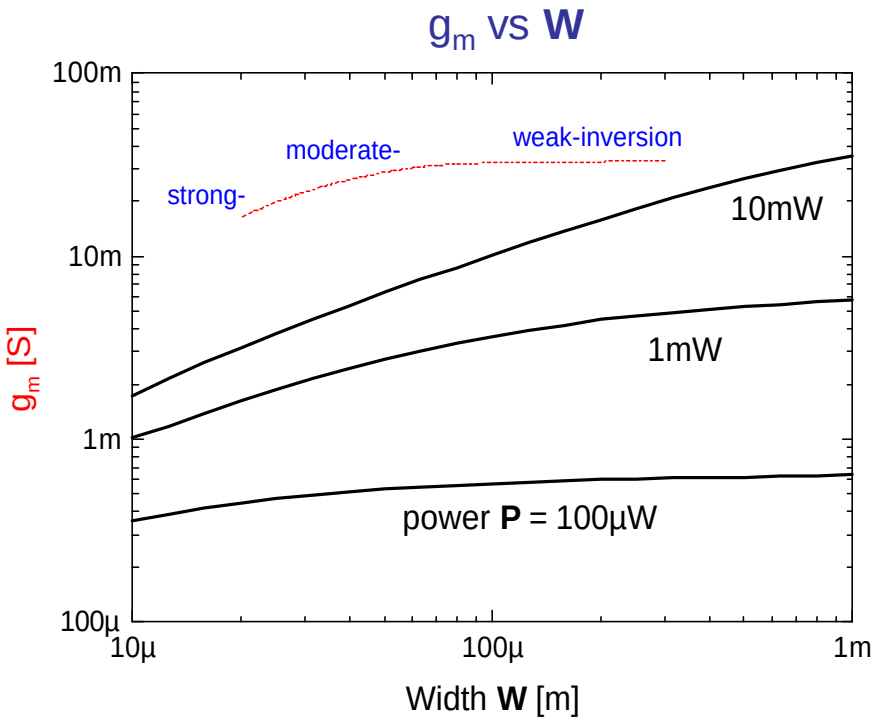


$$ENC^2 = A_1\tau_P\frac{(C_p + C_i + C_g)^2}{g_m} + A_2 A_f (C_p + C_i + C_g)^2 + \frac{A_3}{\tau_P}(I_p + I_{rst})$$

g_m, C_g, A_f , are functions of input MOSFET width **W** and power **P**

Input MOSFET optimization

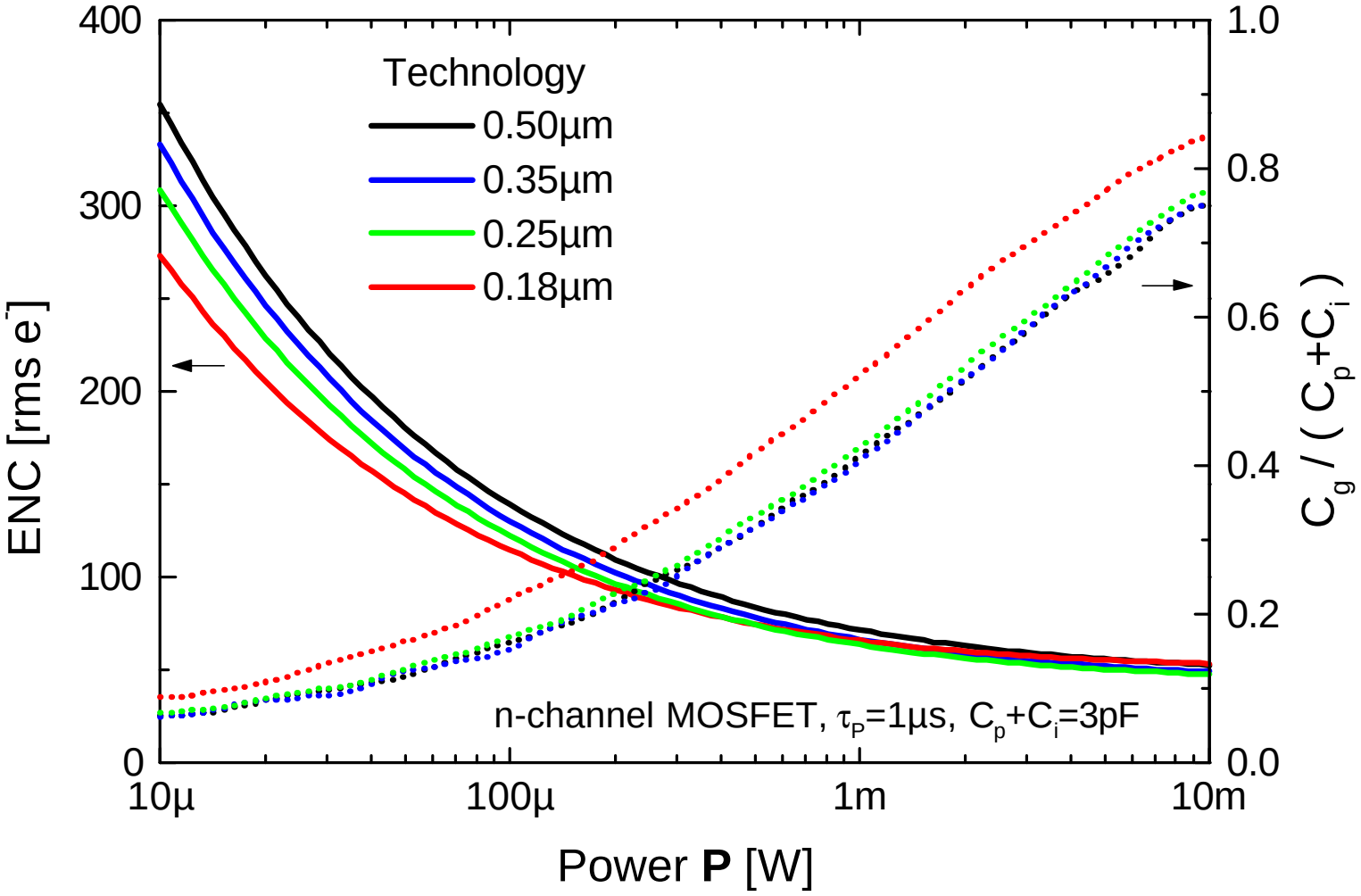




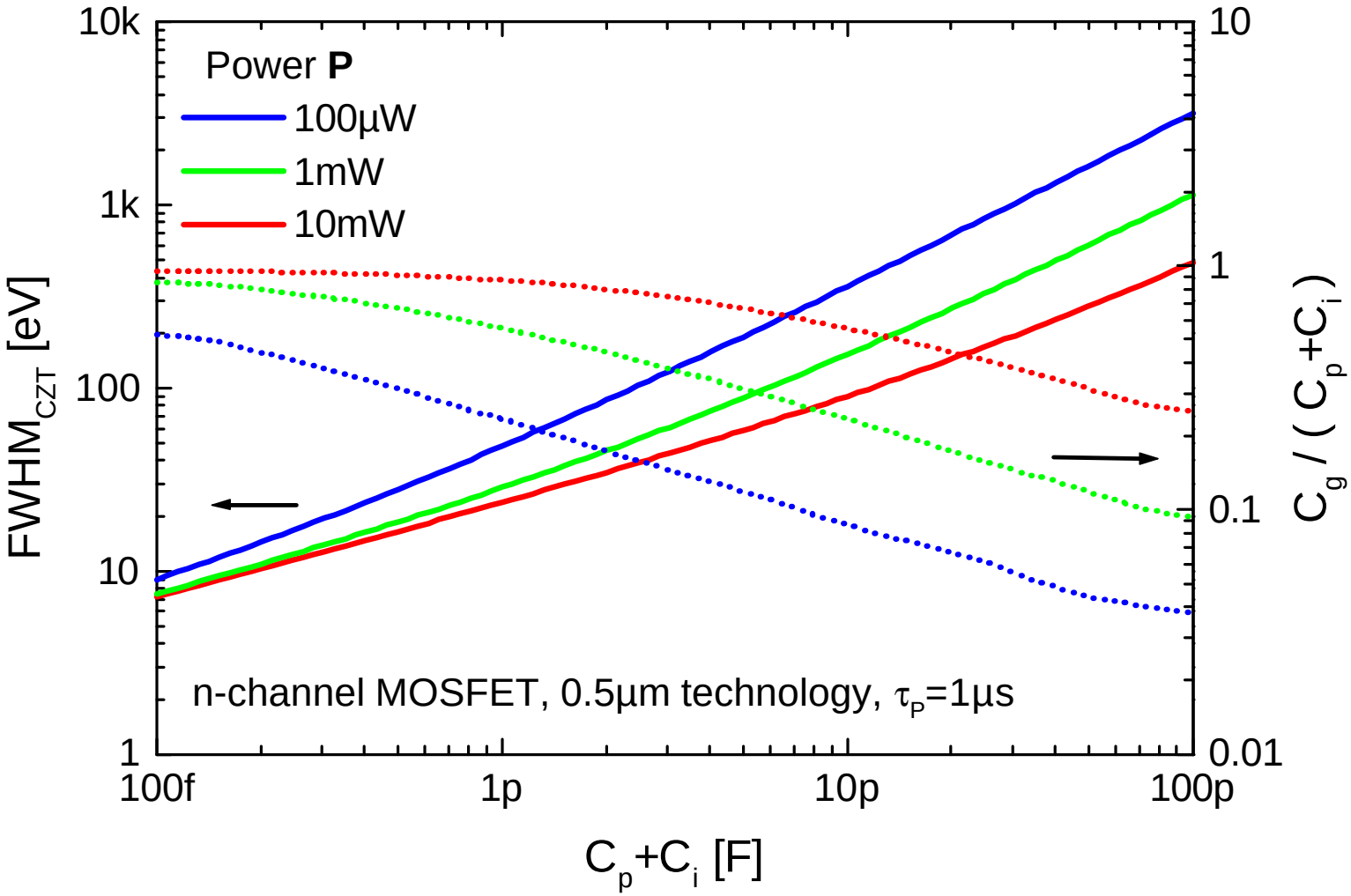
$$C_g \approx (C_{ox}L + C_{ov}) \cdot \mathbf{W}$$

$$A_f \approx K_f / (C_{ox}L \cdot \mathbf{W})$$

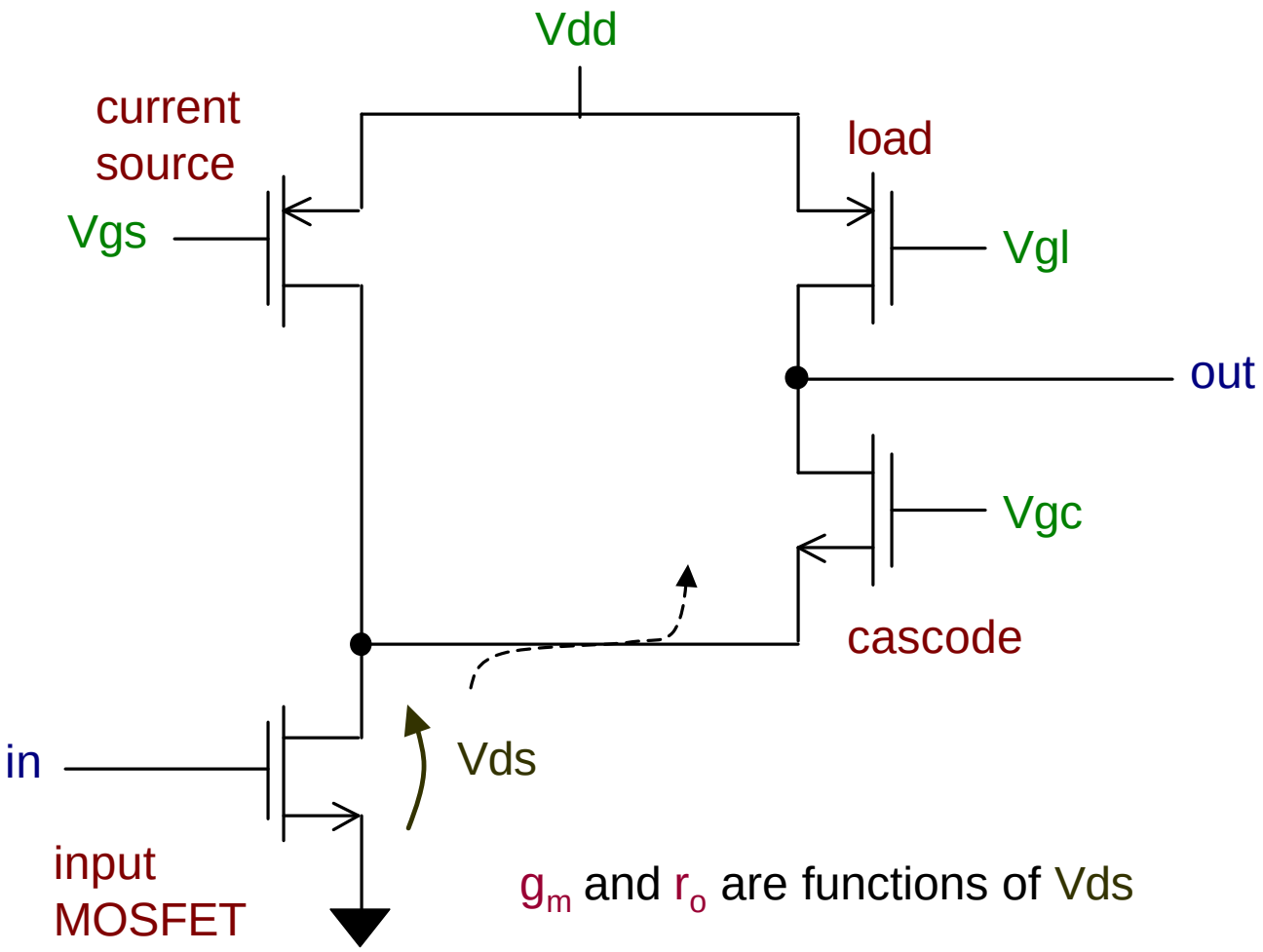
Input MOSFET optimization



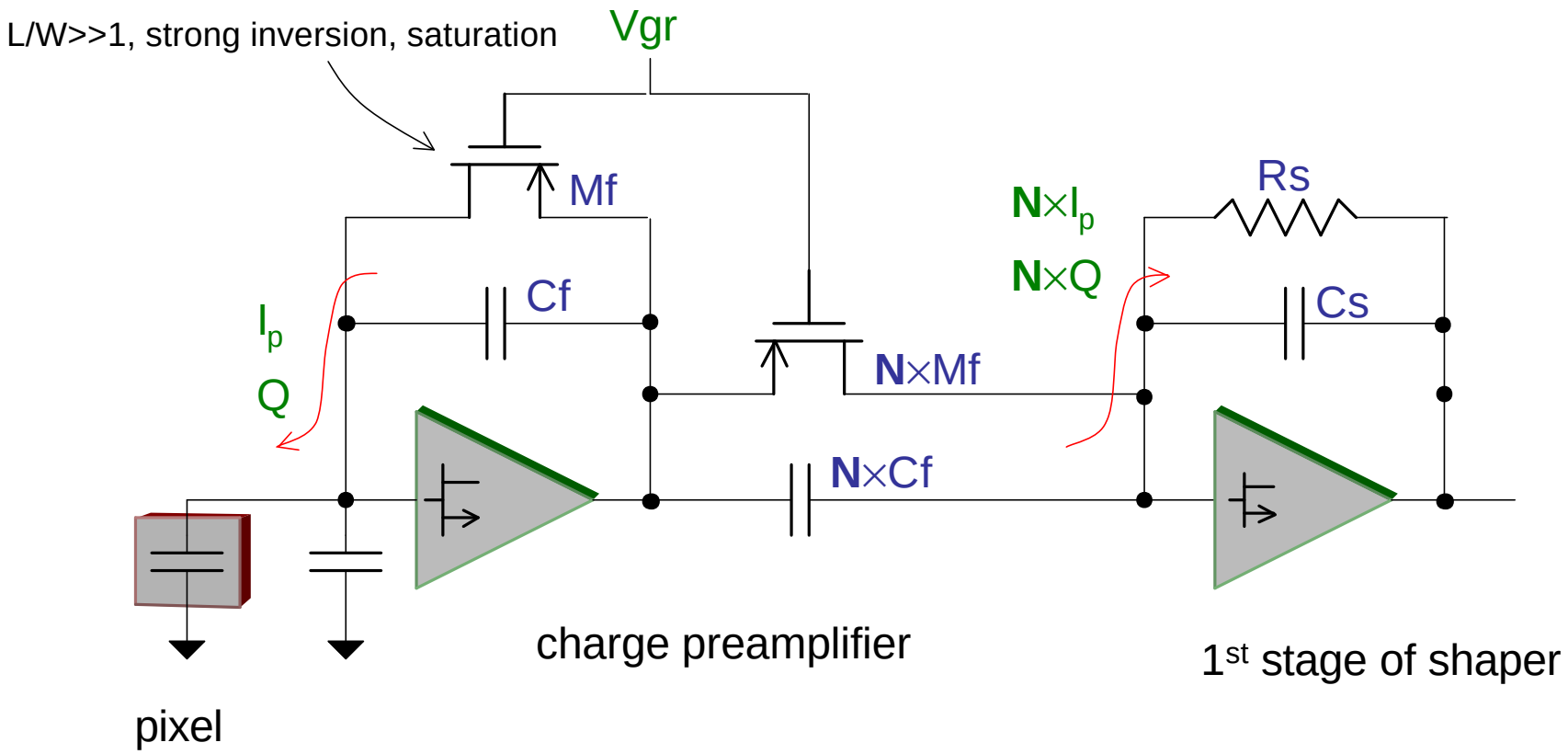
Input MOSFET optimization



Input MOSFET optimization



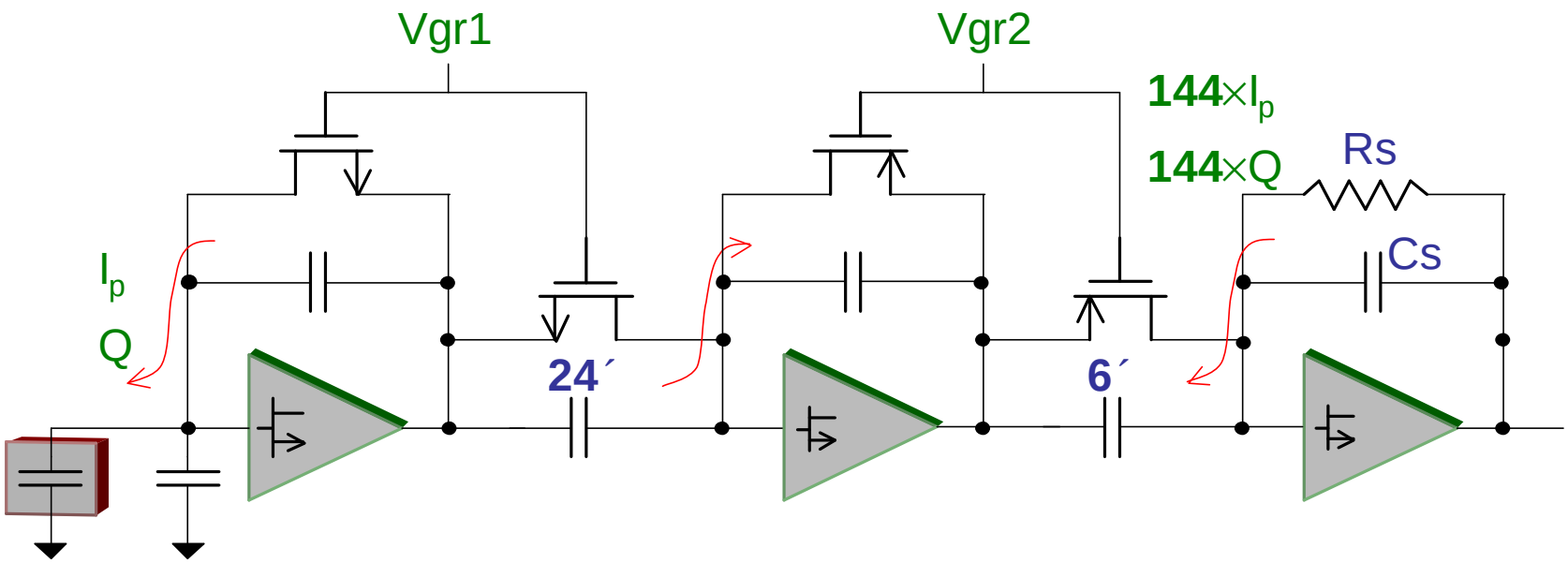
Continuous reset of the preamplifier



- current gain equal to **N**
- fully linear
- **self-adapts** to leakage current
- minimum noise contribution

Continuous reset of the preamplifier

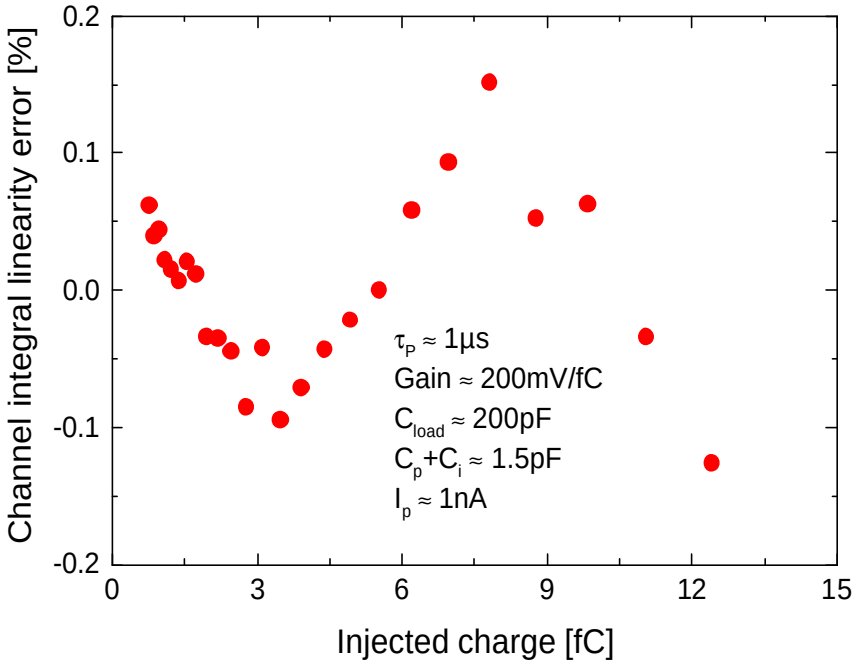
$$\frac{2kT}{Rs}\frac{1}{N^2} \equiv q \cdot I_{eq} \qquad Rs \approx 100kO \rightarrow I_{eq} \approx 1nA$$



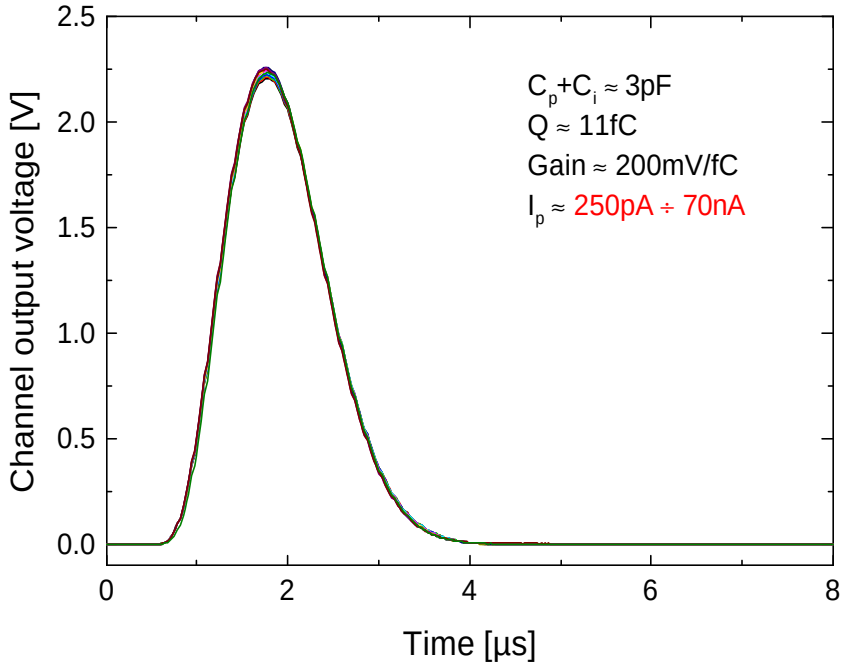
$$Rs \approx 100kO \rightarrow I_{eq} \approx 25pA$$

Continuous reset of the preamplifier

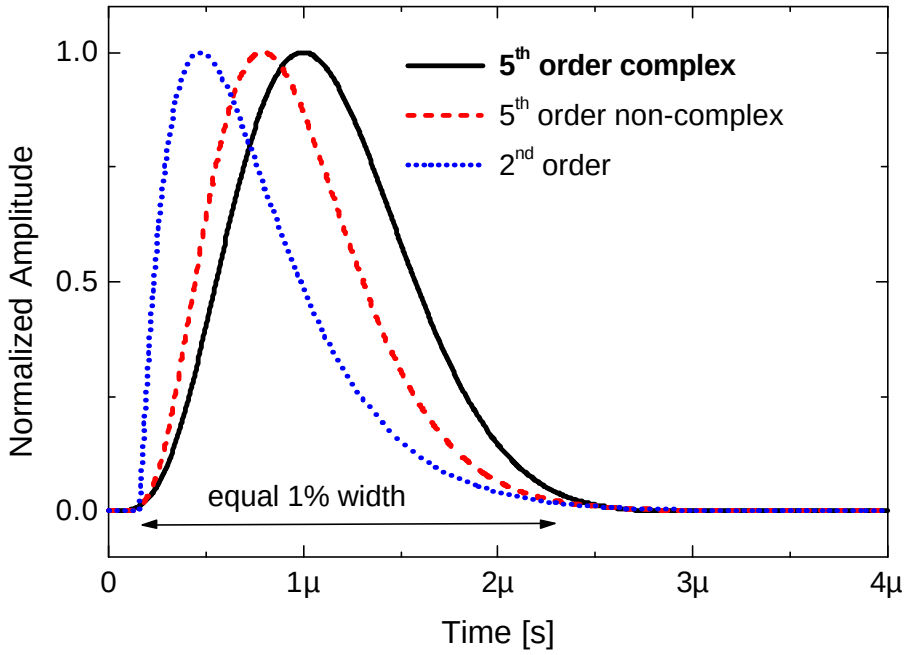
linearity



output vs pixel leakage current



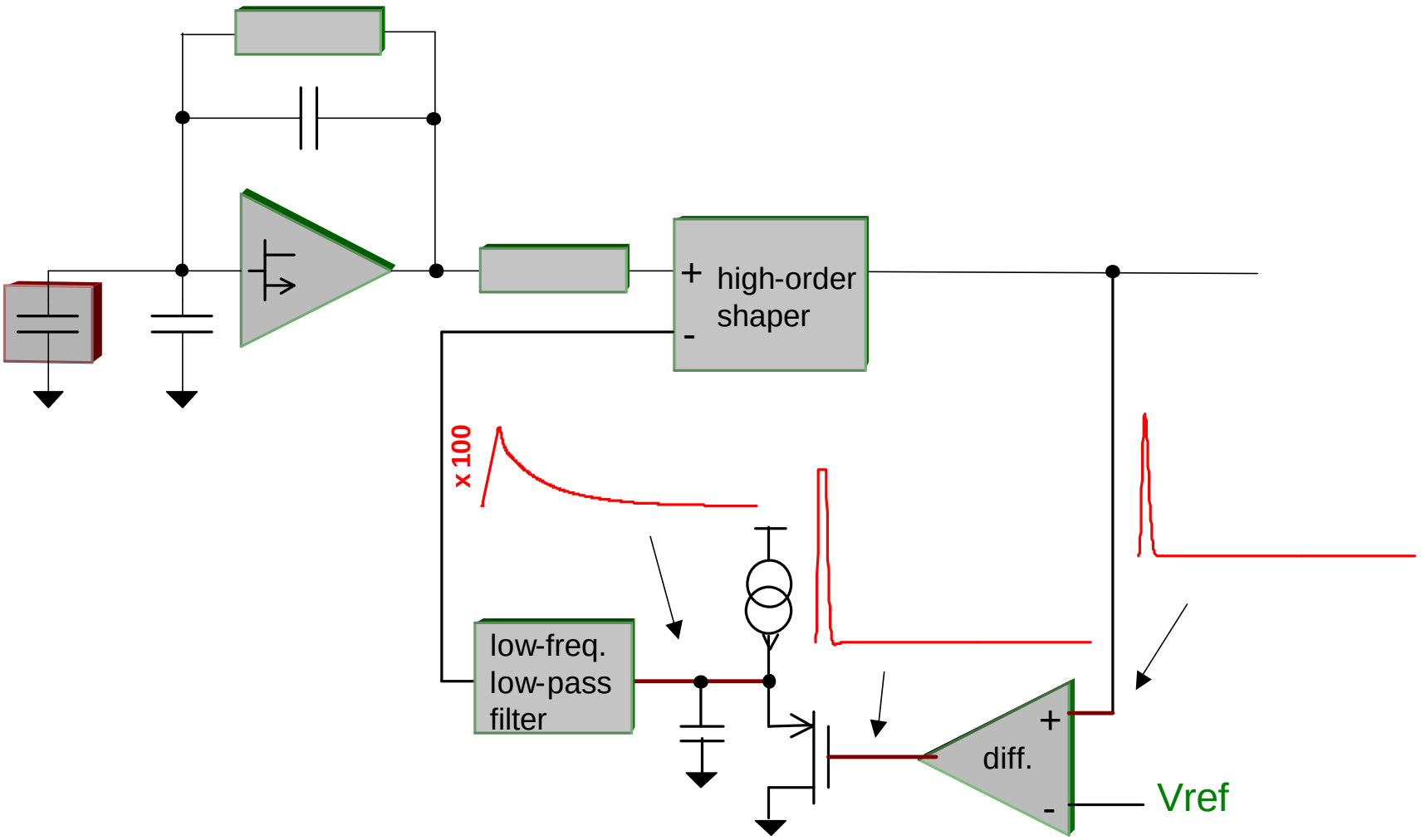
High order shaping



	a
5th cpx	**1**
5th	1.24
2nd	2.64

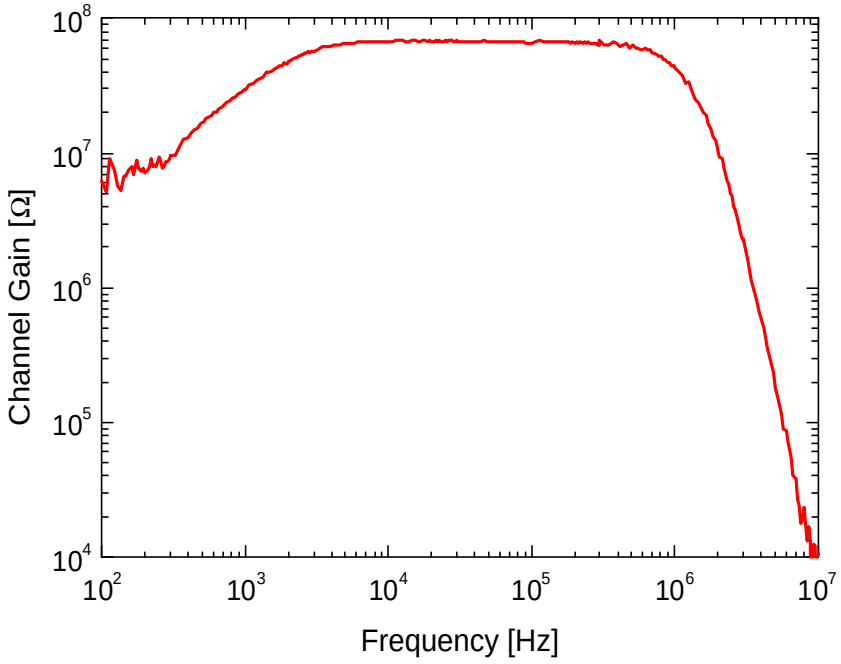
$$ENC^2 = a\, A_w t_w \frac{\left(C_p + C_i + C_g\right)^2}{g_m} + \ldots$$

Output baseline stabilizer

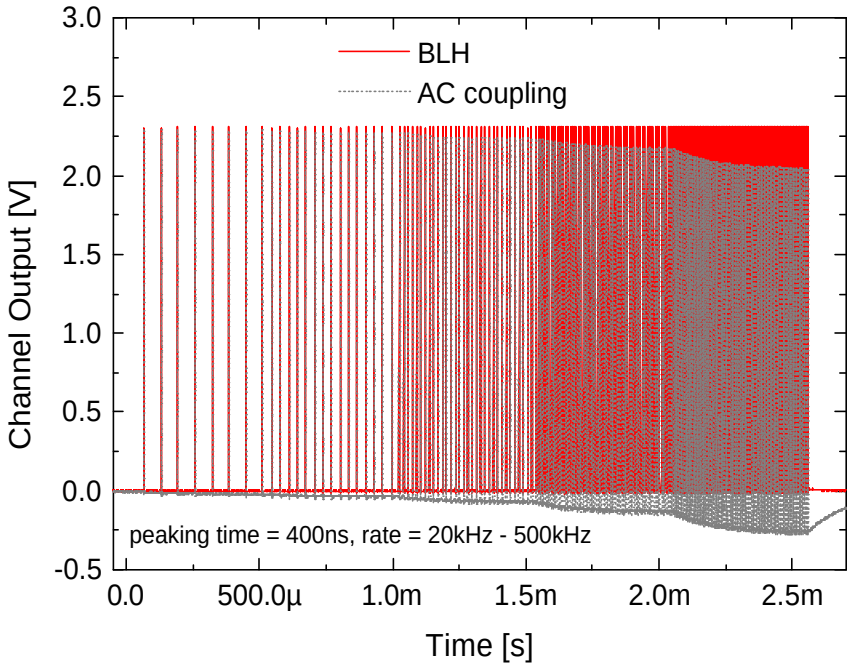


Output baseline stabilizer

transfer function



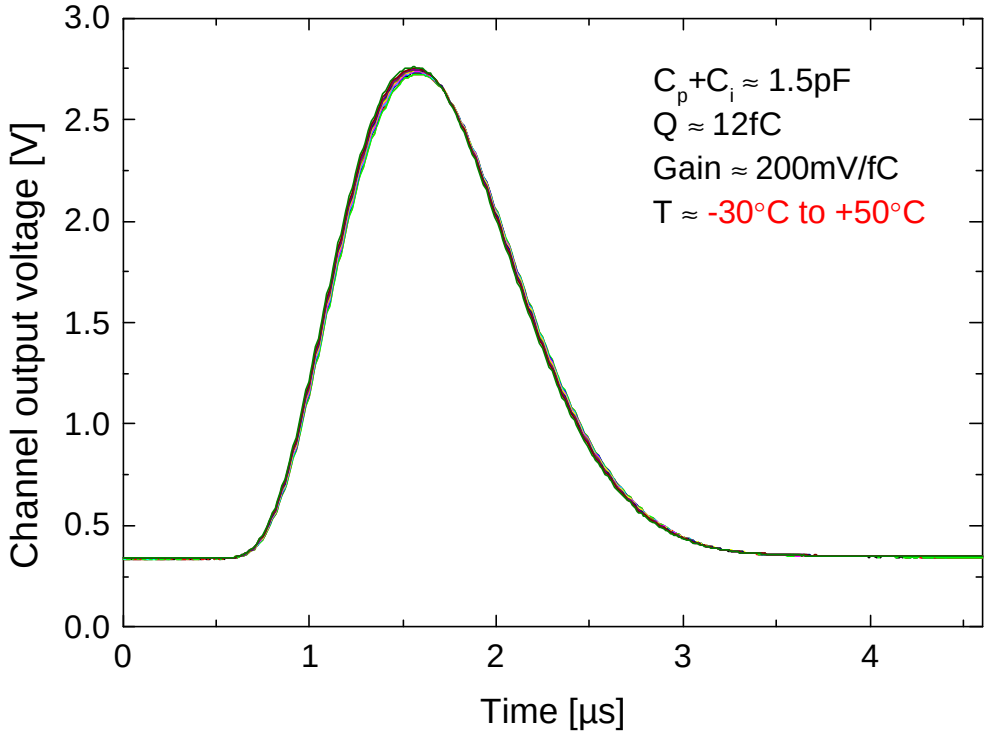
performance at high rate



First generation of front-end ASICs

other features

- plug & play
- per-channel test capacitor
- programmable gain
- programmable peaking time
- high output drive capability
- high stability vs temperature



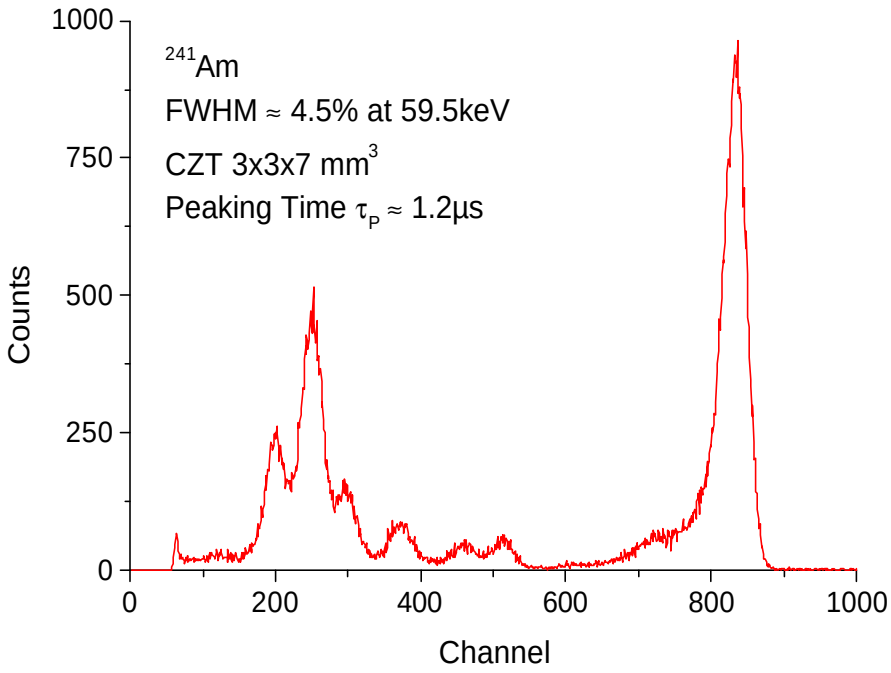
The first generation of front-end ASICs

ASIC	Pixel capacitance [pF]	Channel count	Peaking time [µs]	Gain [mV/fC]	Power / channel [mW]	ENC [rms. e-]	Applications
General purpose	3	16	0.6, 1.2, 2.0, 4.0	30, 50, 100, 200	18	30+20/pF	*LFOV Gamma Camera* *SFOV Gamma Camera* *Nuclear Safeguards*
Medium speed	3	4	0.4	200	18	29+27/pF	*Down Hole Well Logging* *X-Ray Diffraction Gauges*
High speed bipolar	3	8	0.2	240	18	42+44/pF	*Bone Densitometry* *Pulse Mode CT* *Industrial X-Ray*
High capacitance	12	8	0.6, 1.2, 2.0, 4.0	30, 50, 100, 200	35	57+10/pF	*Industrial Strip Detectors* *Backscatter Gauges* *Large Area Detector*

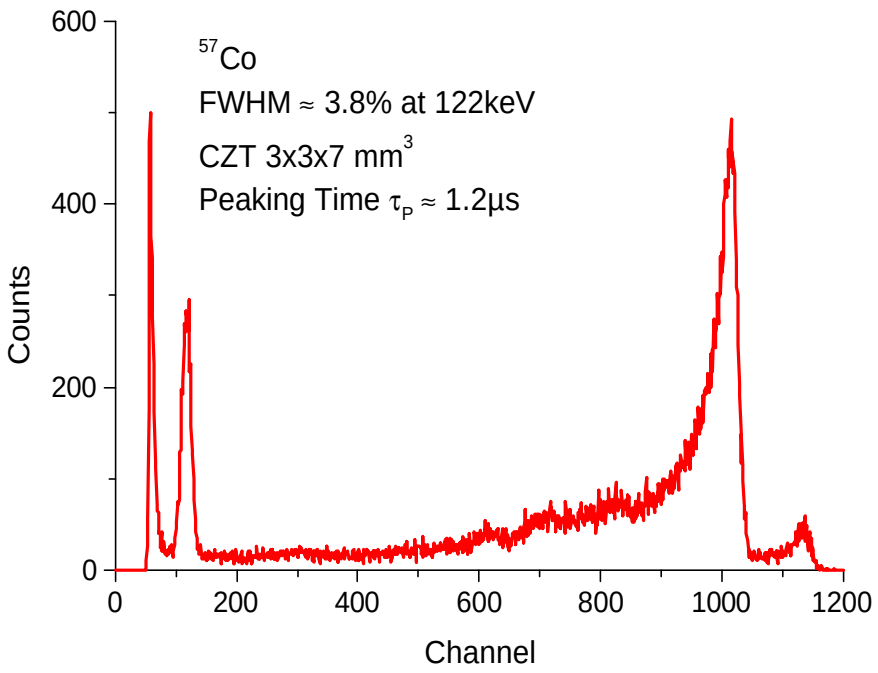
Technology : 0.5µm CMOS SP3M

CZT – ASIC spectra measurements

^{241}Am spectrum



^{57}Co spectrum



CZT – ASIC spectra measurements

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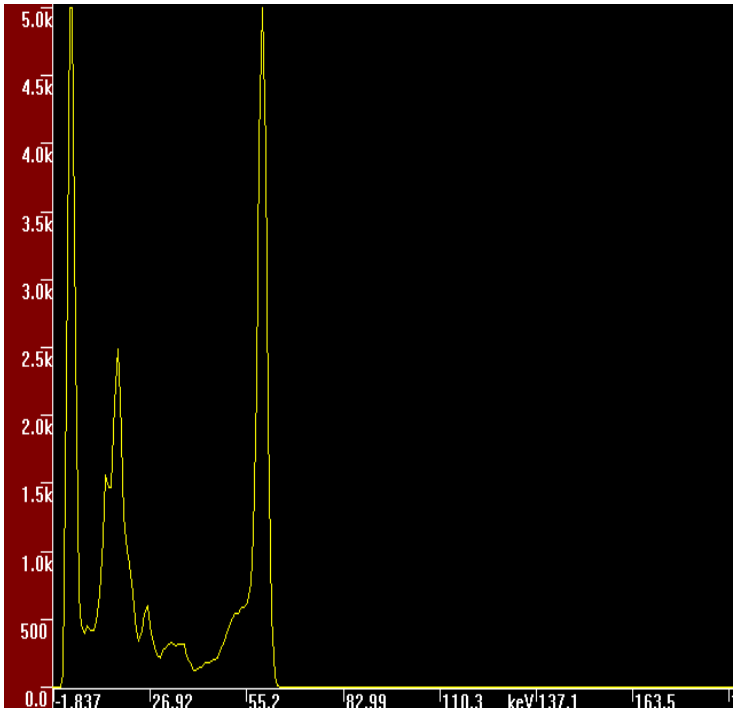
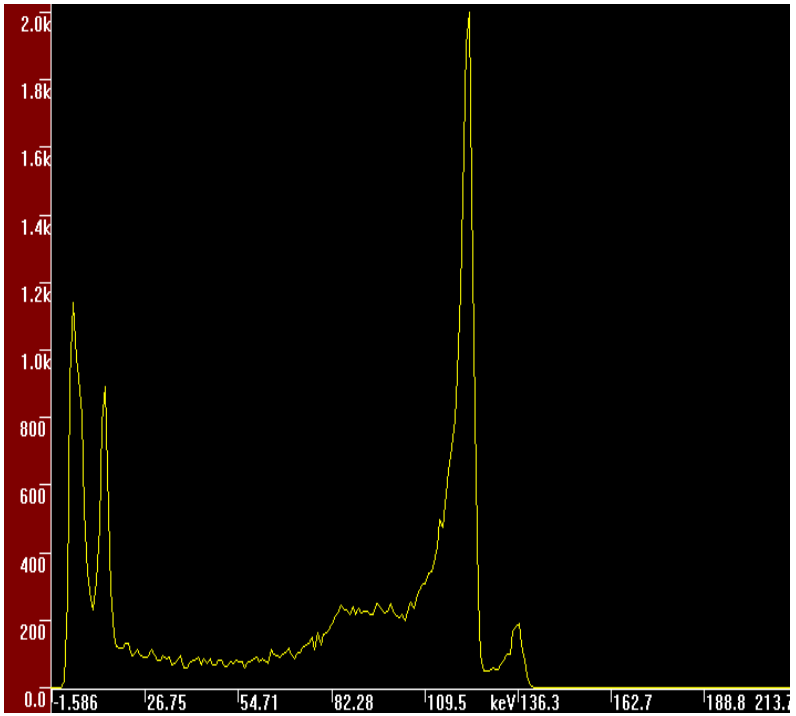


- detector thickness 3mm
- detector bias -600V
- resolution 4.3% at 59keV
- gain 200mV/fC
- peaking time 1.2µs

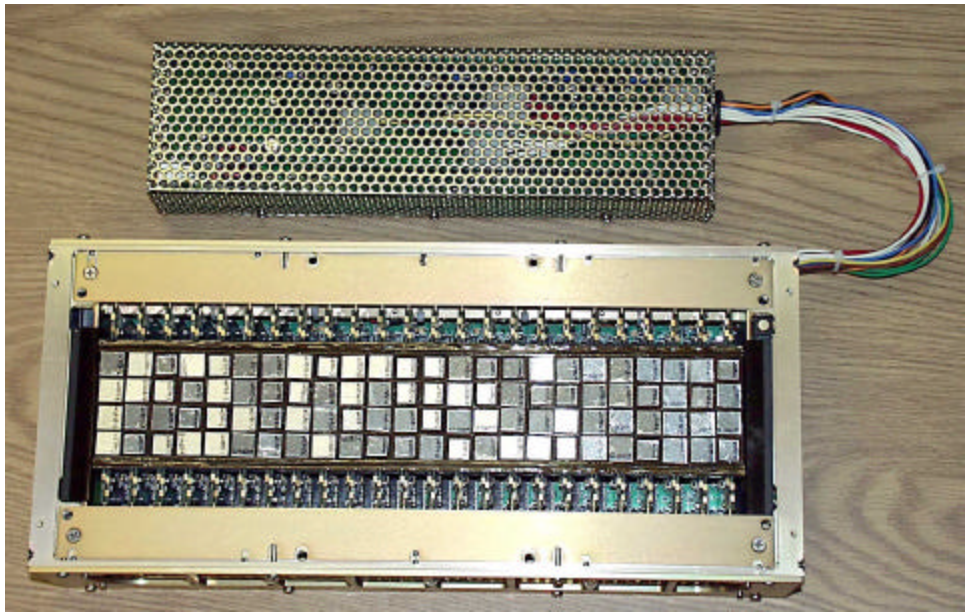
^{57}Co spectrum



- detector thickness 3mm
- detector bias -600V
- resolution 3.5% at 122keV, 21.8% at 14keV
- gain 200mV/fC
- peaking time 1.2µs

CZT – ASIC applications

Solstice Gamma camera



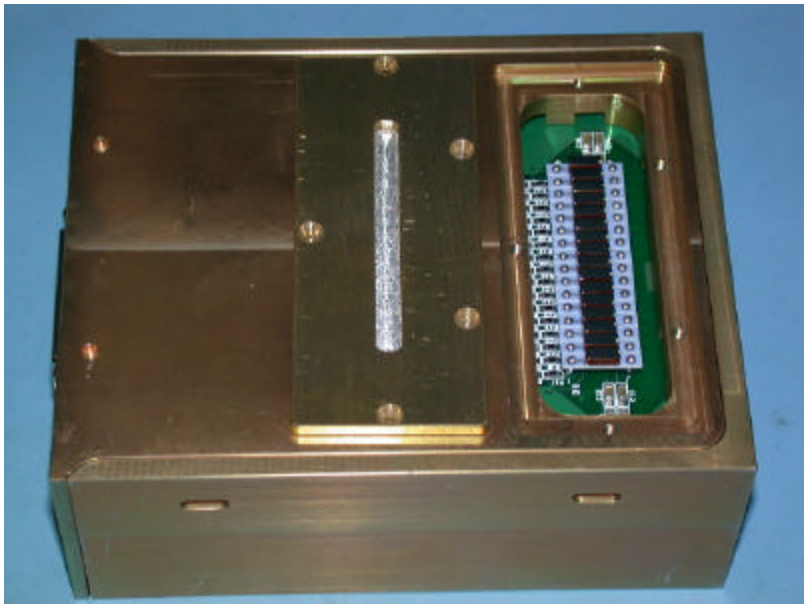
- 96 CZT crystals
- 3072 pixels
- 196 front-end ASICs
- 1.3M events/second
- average FWHM 3.8% at 122keV

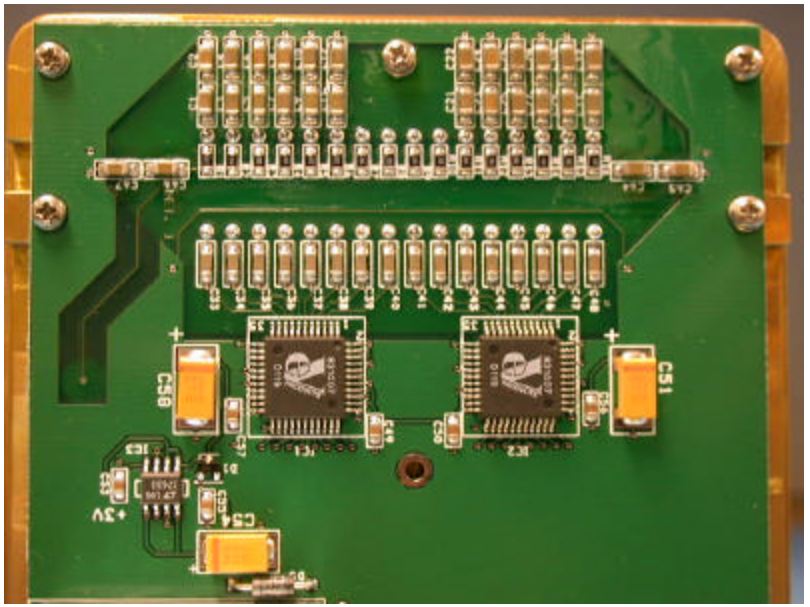
eZ-SCOPE hand held Gamma camera

- 1 CZT crystal
- 256 pixels
- 16 front-end ASICs
- 4.8M events/second
- average FWHM 4.0% at 122keV

CZT – ASIC applications

Bone Densitometry – GE Lunar Detector

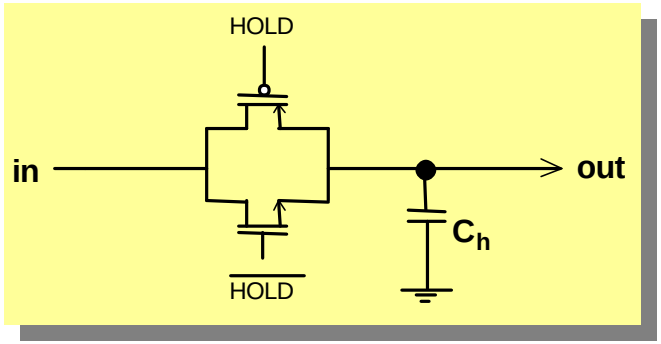




- 16 CZT crystals
- 16 pixels 3 x 7 x 3 mm^3
- 2 front-end ASICs
- DEXA (Dual Energy X-ray Absorptiometry)
- ASICs replaced 17 circuit boards (over 500 components) and improved performances

Pulse amplitude extraction : classical CMOS configurations

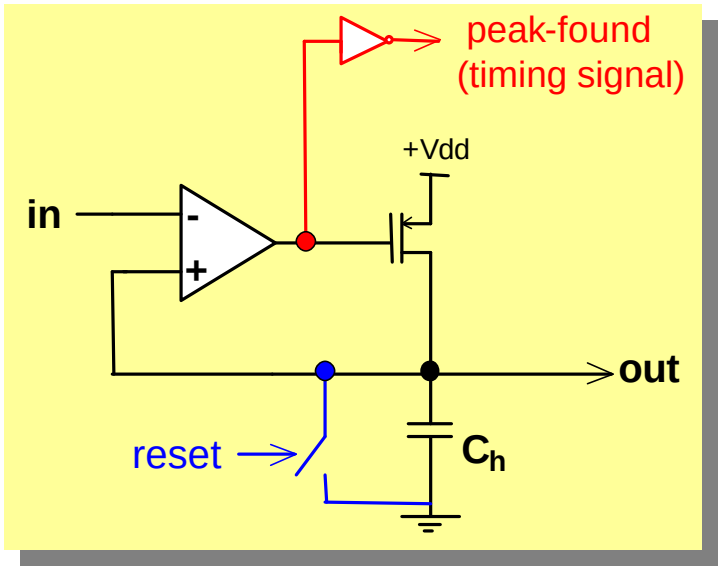
sample/hold



- **timing signal needed**
- switch charge injection
- poor drive capability
- deadtime until readout

+ power dissipation

peak detect/hold (PDH)



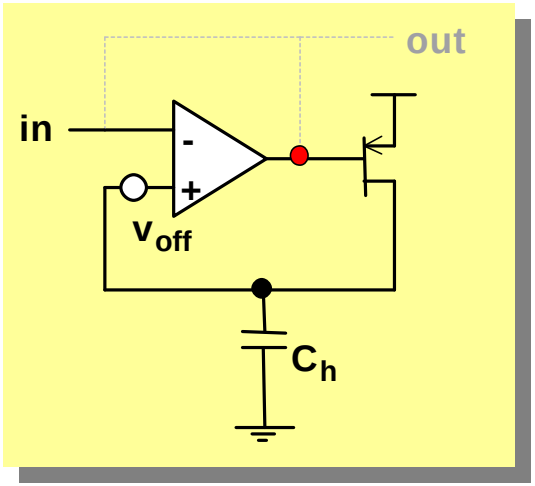
- accuracy impaired by op-amp **offsets** and **CMRR**
- poor drive capability
- deadtime until readout

+ **self-triggered**
+ **timing signal**

The two-phase PDH concept

Write phase

• behaves like classical configuration



Read phase

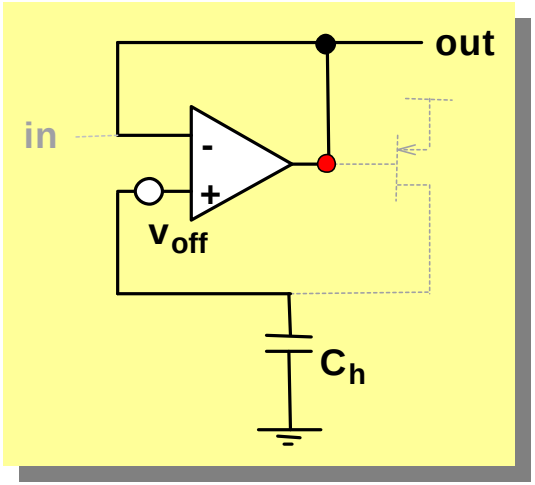
• op-amp re-used as buffer

• **offset** and **CMMR** **errors canceled**

• enables **rail-to-rail** sensing

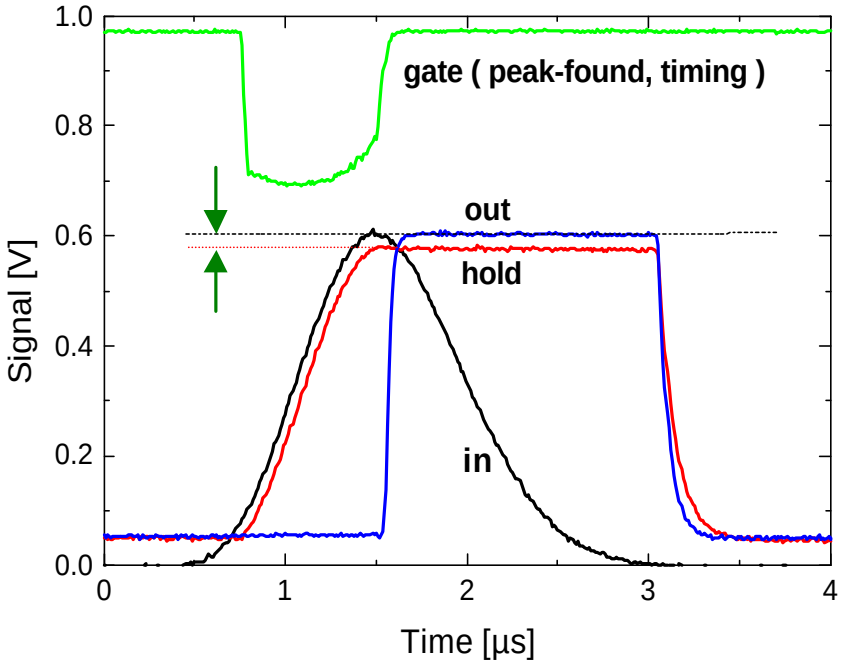
• good **drive capability**

• **self-switching** (peak found)

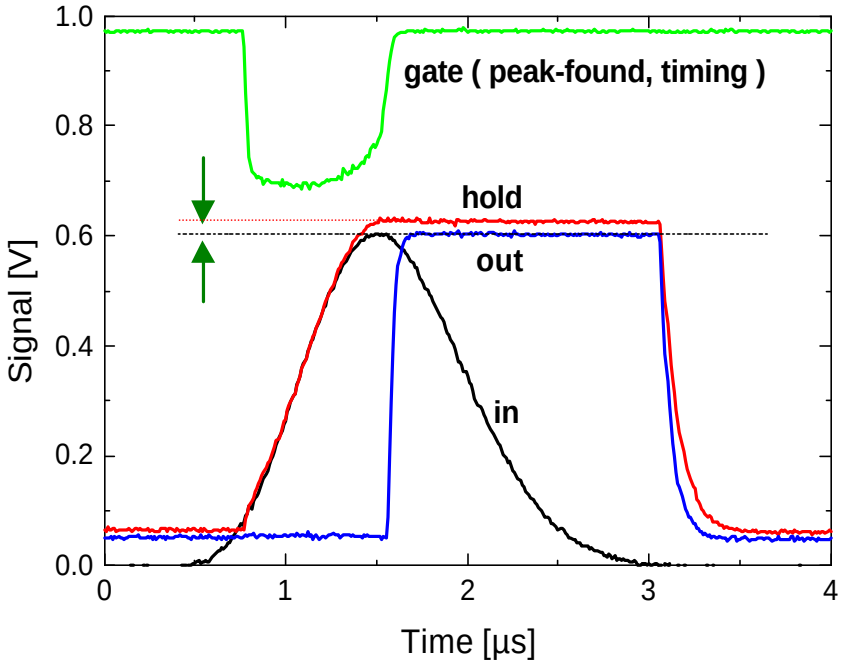


Two-phase PDH : offset cancellation

chip 1 – negative offset

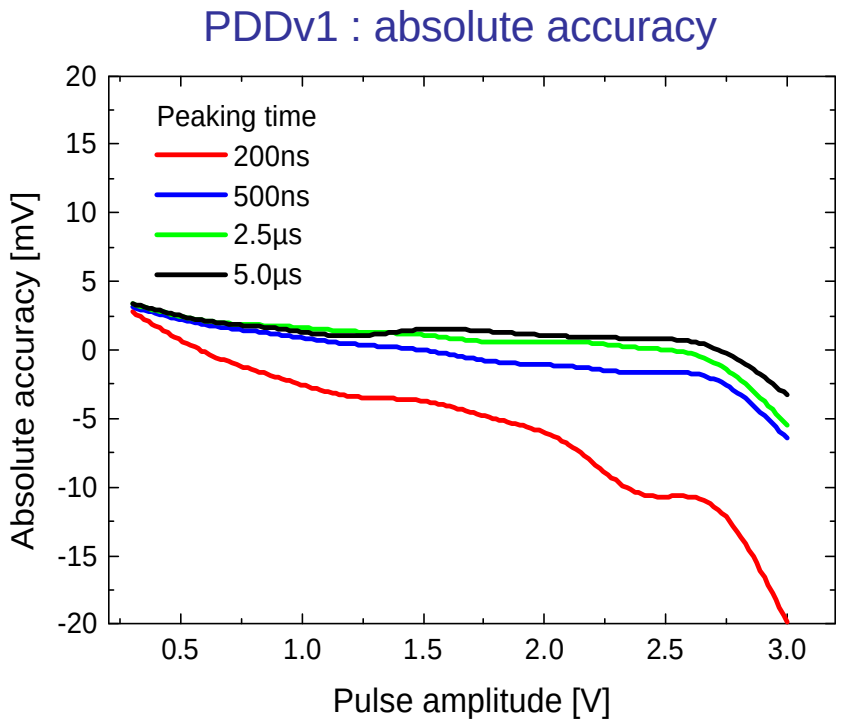


chip 2 – positive offset

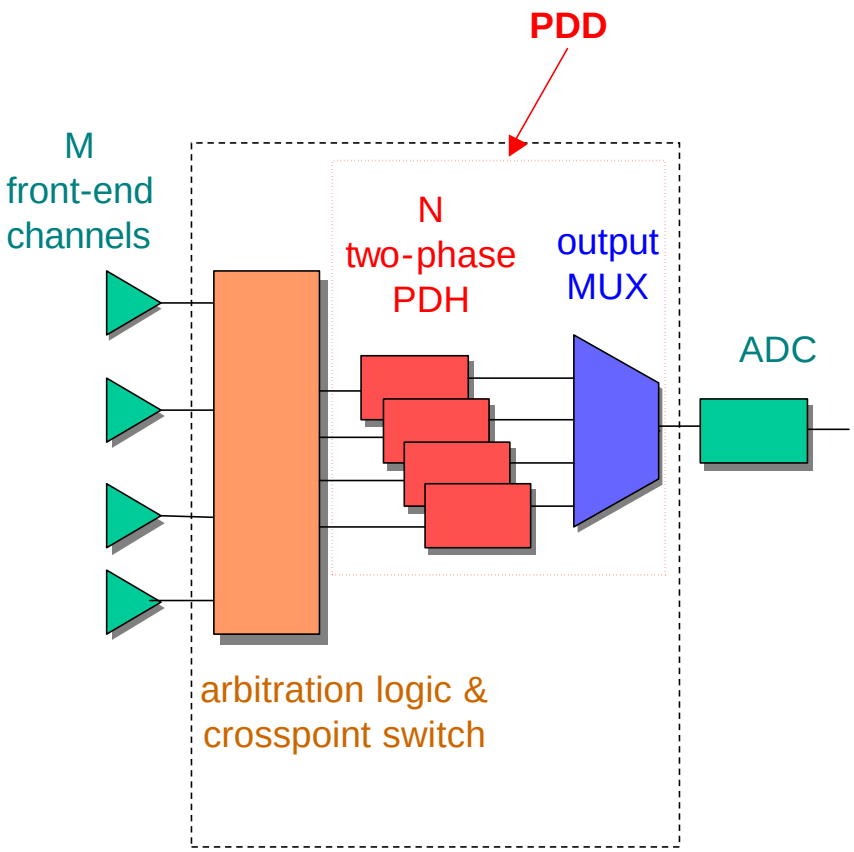


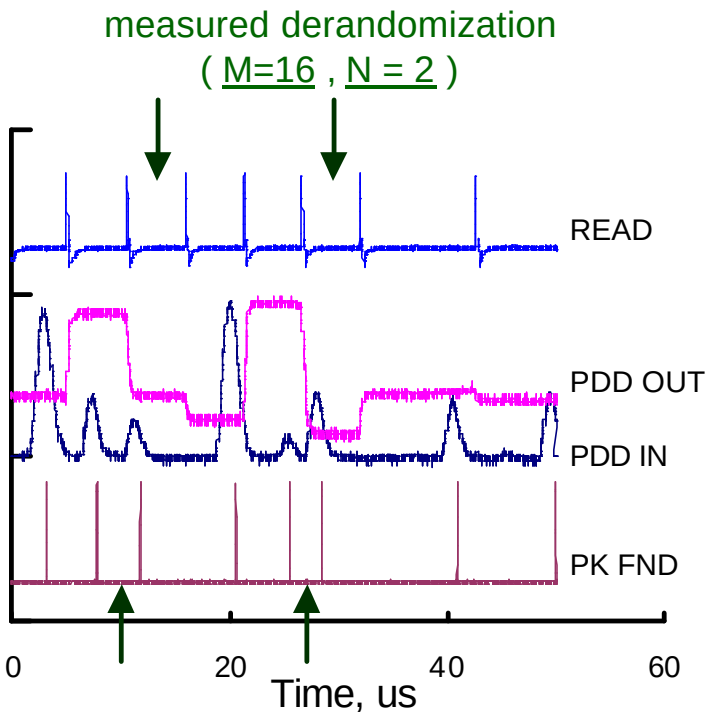
Two-phase PDH : performance

Parameter:	Value: PDDv1 *(PDDv2)*
Technology	0.35 um CMOS DP4M
Supply voltage	3.3V
Input voltage range	0.3 - 3.0 V
Minimum peaking time	**500 *(50)* ns**
Absolute accuracy	**< 0.20%**
Linearity	< 0.05%
Droop rate	250 mV/s
Timing accuracy	5 ns
Power dissipation	3.5 (2.0) mW/ch

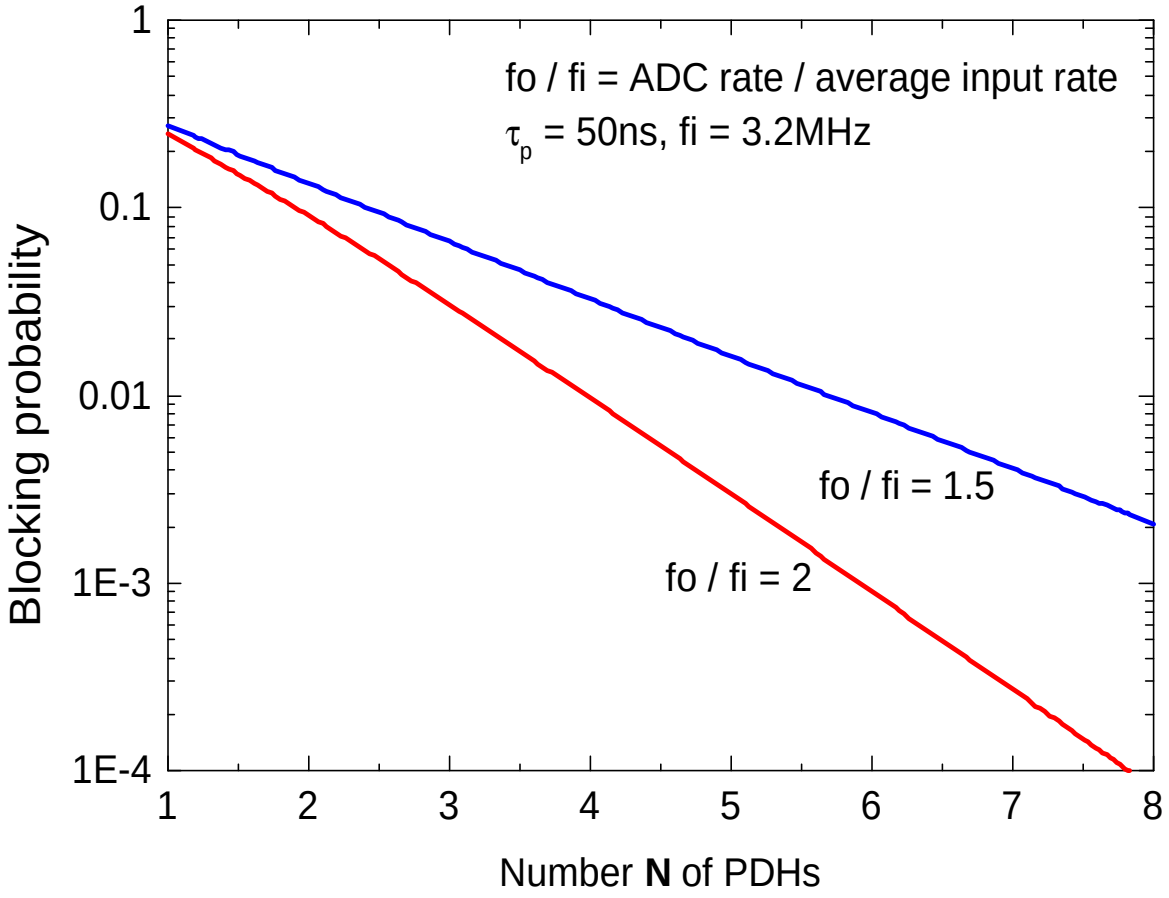


Derandomization with N two-phase PDHs (PDD)





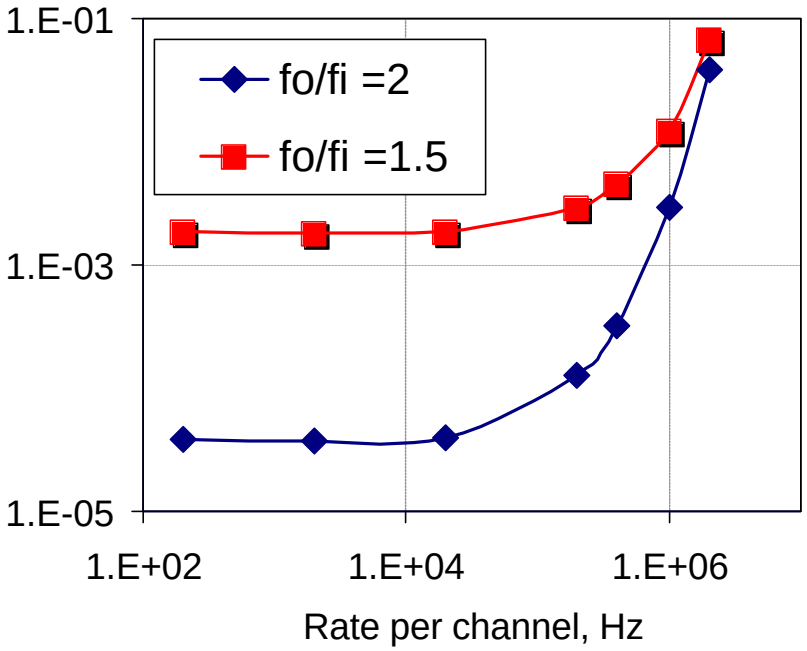
Derandomization efficiency vs N



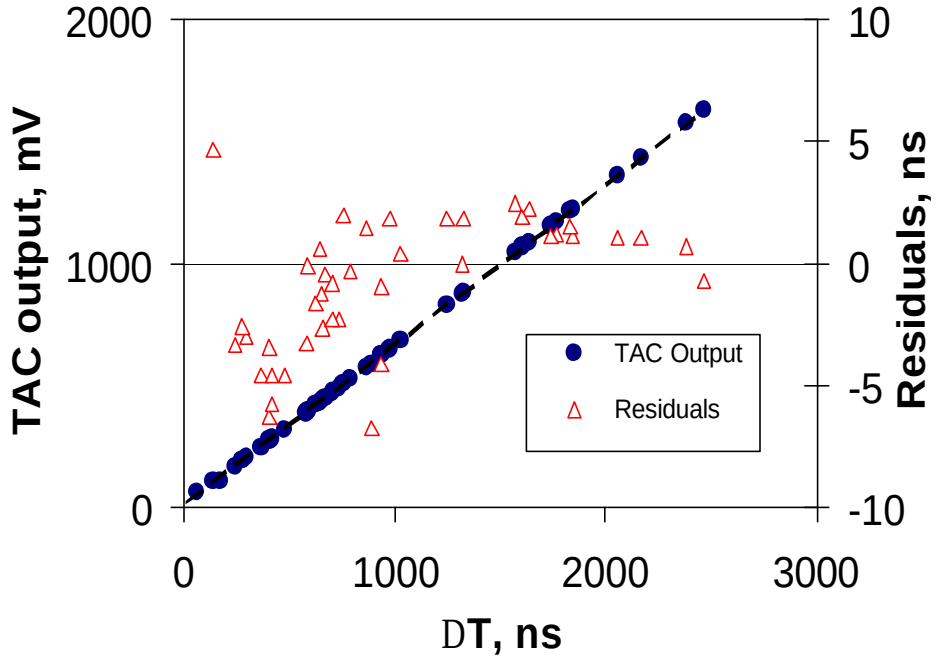
The larger is **N**, the lower can be the **fo/fi** ratio

Derandomization efficiency and TAC linearity

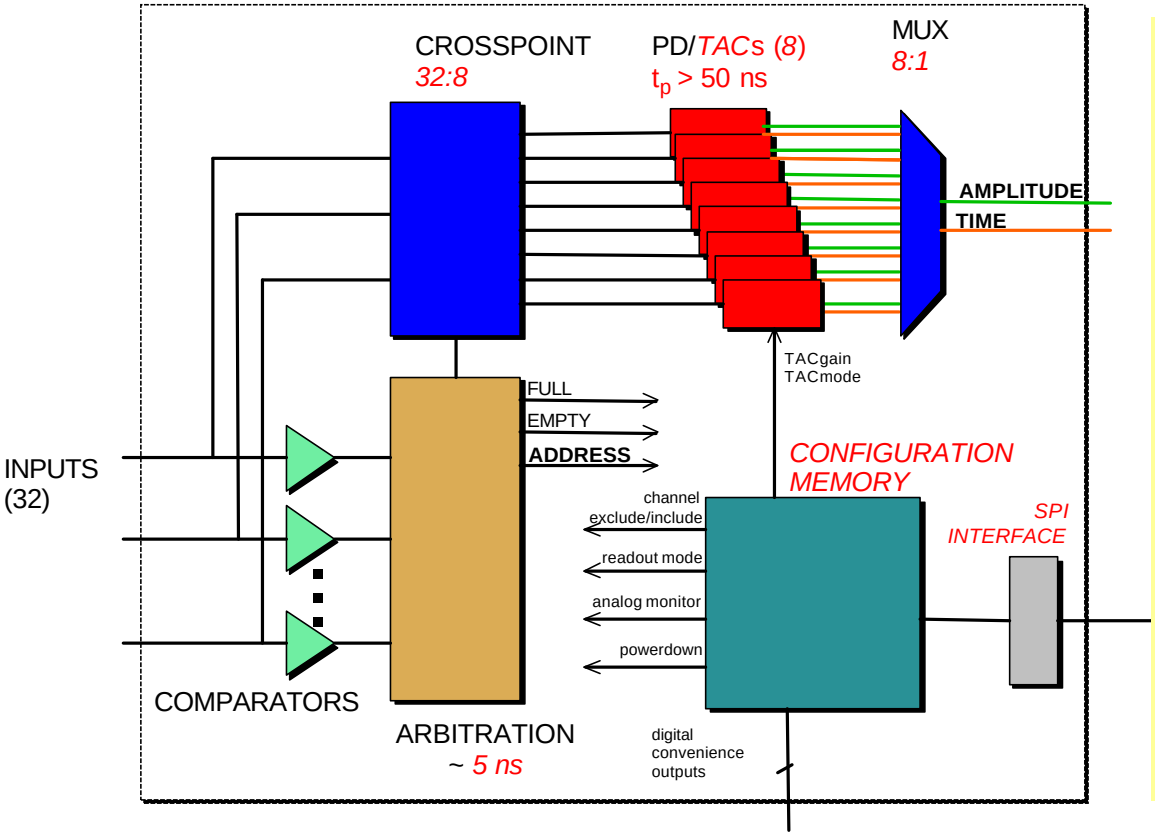
blocking probability



TAC linearity

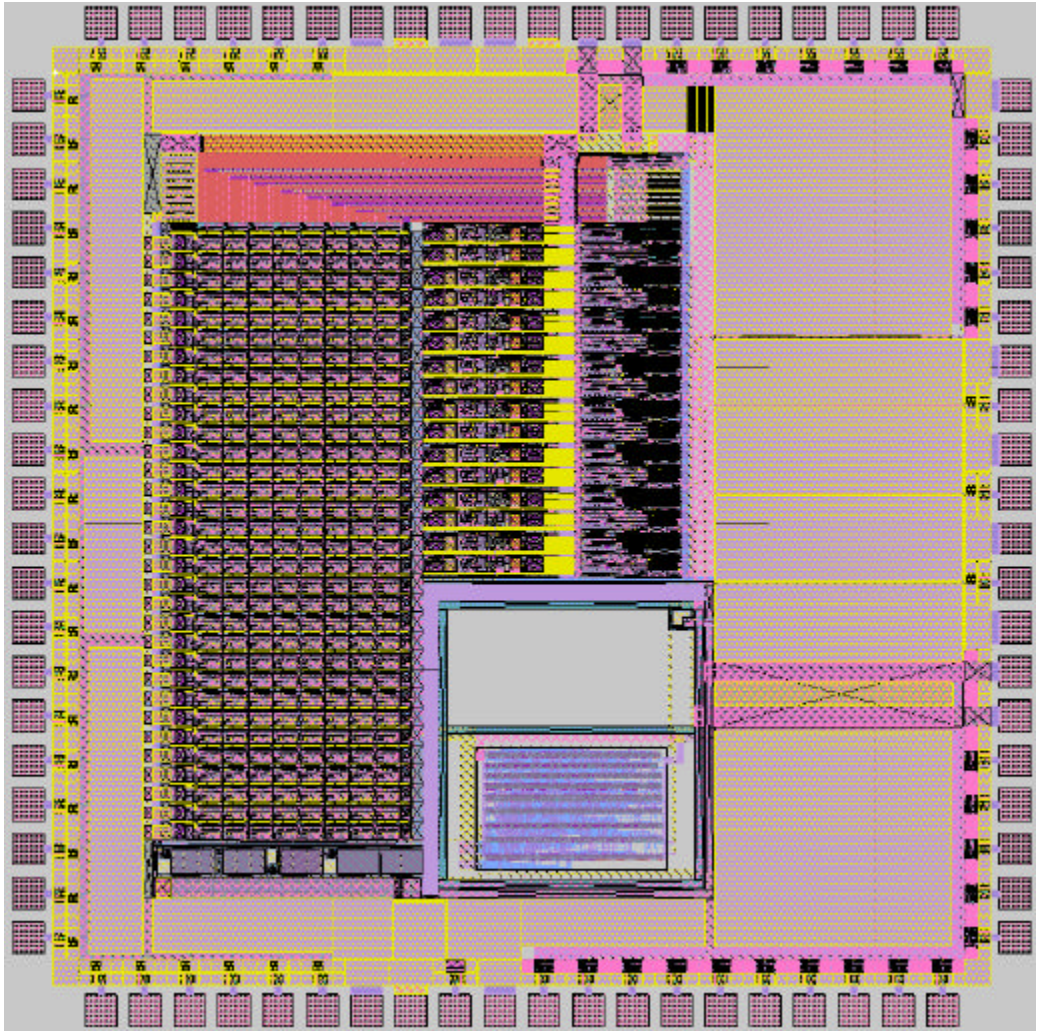


32-channels PDD ASIC



- One-chip solution
- $N_{CHAN} = 32$, $N_{PD} = 8$
- Dual-mode **TAC**
  - risetime
  - time of occurrence
- **Amplitude, address, timing outputs**
- 50 ns minimum pulsewidth
- $t_{ARB} \sim 5$ ns
- Rate capability ~ 10 MHz
- SPI interface:
  - serial configuration of TAC gain and mode
  - arbitration locking
  - channel exclusion
  - powerdown
  - analog monitor
  - Digital convenience outputs (used for configuring companion amplifier chip)
- FIFO-like control and readout interface

32-channels PDD ASIC : layout



size : 3.2 x 3.2 mm²
power : 2mW / channel
technology: 0.35µm CMOS DP4M

Summary

- A generation of high-performance **front-end ASICs** has been developed
  - advanced circuit solutions
  - high reliability, stability, ease of use
  - produced in large quantity
  - implemented in products commercialized by eV
- A generation of **data concentration ASICs** is being developed
  - based on a high-performance peak detector of novel concept
  - self-triggering, multiplexing, derandomizing, sparsifying
  - providing amplitude, timing and address information per event
  - a 32-channels, 8 PDs, 10MHz prototype is in fabrication